

**PI3HDX511F**

**Ultra-low Stand-by Power HDMI1.4b 3.4Gbps ReDriver DP++ Level-Shifter with 6-step 15dB EQ, DDC Buffer, Channel Swap for Sink Application**

**Description**

PI3HDX511F is a ultra-low power HDMI 1.4b ReDriver and dual-mode DisplayPort level shifter up to 3.4Gbps data rate with 48-bpp Deep Color support.

In the mobile platforms, extending battery hours have been one of the most challenges for system designers. PI3HDX511F has rich power saving features to extend the battery life with 2uA stand-by current and other features like LDO disable pins, Active/Passive DDC switch, Output squelch and HPD (Hot plug Detect) detection.

PI3HDX511F can support both source and sink side system application. For Sink side (Recepticle) application, it supports 6-step input EQ adjustment and data/clock pin order swap.

**Features**

- Ultra-low power HDMI 1.4b compliant Redriver
- Dual-mode DisplayPort Level Shifter/Redriver with pin option
- Operation up to 3.4 Gbps per lane ( 340MHz pixel clock)
- Sink-side application support with TMDS Data & Clock pin swaps and high 15dB EQ options
- 4K2K Ultra-HD, 3D Video formats (1080p, 1080i, 720p), 48-bit per pixel Deep Color support
- Ultra-low standby current 2uA with DDC passive switch mode
- Flexible 6 steps input equalization control steps: 2.5/5/7.5 dB for short cable range and 5/10/15 dB for long cable modes.
- Pre-emphasis 3 steps setting: 0/1.5/2.5 dB
- Automatic TMDS output disable with squelch or HPD detection in the no-signal input condition
- Selectable Active DDC buffer mode for 1.8-3.3V DDC
- Max 120mW with LDO Bypass 1.5V power supply mode
- Integrated ESD protection: 8kV HBM for all IO pins per JEDEC standard
- Power supply: 3.3V single or 3.3/1.5V dual power supply

→ Package: 40-pin TQFN (3x6mm)

**Applications**

- Notebook, Desktop computers
- Displays, Monitors
- A/V receivers, Set Top Box, Video Players
- Repeaters and switch boxes



Figure 1-1. DP++ level shifter in Notebook PC

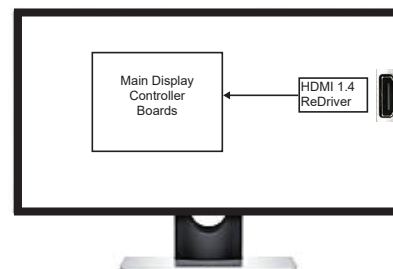


Figure 1-2. HDMI Port in All-In-One PC

**Ordering Information**

Ordering Number	Package Code	Package Description
PI3HDX511F ZLE(X)	ZL	40-pin TQFN, Lead Free & Green, Tray(Tape & Reels)
PI3HDX511F ZLIE(X)	ZL	Industrial temp support. 40-TQFN, Lead Free & Green

Note: Suffix I = Industrial temp, E = Pb-free and Green, Suffix X = Tape/Reel

## 2. General Information

### 2.1 Revision History

Revision	Description of Changes
June, 2016	P10 - Add Eye opening measurement with different test set-up in the functional description. Expand I-temp grade support in the ordering information.
July, 2016	Add more contents to assist the system design-in in Application page 20 eg. PCB layout, HDMI compliance report.
Sep, 2016	Add clarity for the total power dissipation in the Open-drain and the Double termination modes in p1, p12 and p13.
Feb, 2017	Add Via in the package mechanical drawing
Jun, 2017	I-temp ordering part number added . Diodes Datasheet style updated.
Nov, 2017	Package outline drawing updated.

### 2.2 Products Comparison

	PI3HDX511F	PI3HDX511D	PI3VDP1431	PI3HDX511E
<b>Package</b>	40-pin contact	30-pin contact	32-pin contact	32-pin contact
<b>Body Size(mm)</b>	3x9	2,5x4.5	3x9	3x9
<b>Power Supply</b>	1.5V Core, 3.3V IO power	3.3V	3.3V	3.3V
<b>Data/Clock Pin Swap</b>	Yes	No	No	No
<b>Low Power LDO Bypass</b>	Yes	No	No	No
<b>Power Dissipation</b>	70mA@1.5V, 3mA@3.3V	120mA @ 3.3V	120mA @ 3.3V	120mA @ 3.3V
<b>DDC channels</b>	Passive Switch or Buffers	Passive Switch only	Passive Switch or Buffers	Passive Switch or Buffers
<b>Applications</b>	TMDS ReDriver DP++ Level Shifter	TMDS ReDriver DP++ level shifter	DP++ level shifter	TMDS ReDriver DP++ level shifter
	Sink and Source devices. Power consumption critical Active Cable/Dongle.	Space-limited ultra mobile system	Source Devices like NoteBook PC system	Source Devices requires P2P with PI3HDMI511 earlier part.

## 2.3 Related Products

Part Number	Product Description
PI3DPX1203B	8.1Gbps Displayport 1.4 Linear Redriver. Low-jitter, Latency Free.
PI3HDX1204B1	6Gbps HDMI 2.0 Redriver and Displayport Level Shifter, Low-jitter, High EQ.
PI3HDX414	1:4 Active 3.4Gbps HDMI 1.4b Splitter/DeMux with Signal Conditioning
PI3HDX412BD	1:2 Active 3.4Gbps HDMI 1.4b Splitter/DeMux with Signal Conditioning
PI3HDX621	2:1 Active 3.4Gbps HDMI 1.4b Switch
PI3HDMI336	3:1 Active 2.5Gbps HDMI Switch with I2C control and ARC Transmitter
PI3DPX1202	5.4Gbps Displayport 1.2 Redriver with built-in auto test mode
PI3WVR12612	Wide Voltage Range DisplayPort™ & HDMI Video 1:2 Mux/DeMux

## 2.4 Reference Documents

Document	Description
HDMI 1.4	High-Definition Multimedia Interface Specification Version 1.4, HDMI Licensing, LLC

## 2.5 Product Status Definition

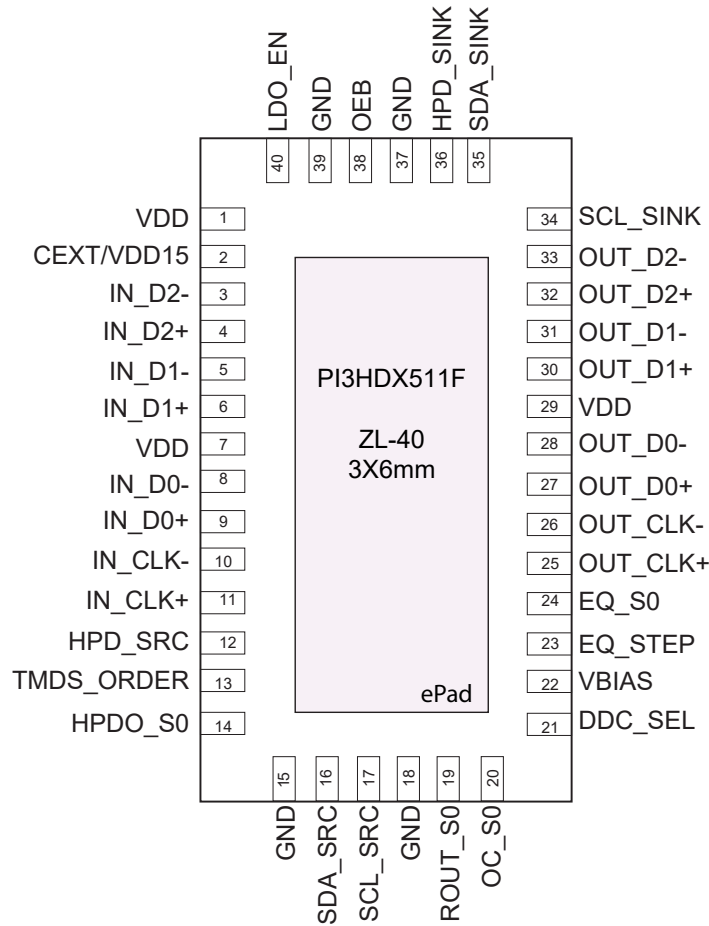
	Product Status	Definition
Advanced	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Diodes Incorporated reserves the right to make product specification changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Diodes Incorporated reserves the right to make changes at any time without notice to improve datasheet informative or reference contents.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Diodes Incorporated. The datasheet is for reference information only.

## Contents

1. Product Summary.....	1
2. General Information.....	2
2.1 Revision History.....	2
2.2 Products Comparison.....	2
2.3 Related Products .....	3
2.4 Reference Documents .....	3
2.5 Product Status Definition.....	3
3. Pin Configuration.....	5
3.1 Package Pin-out.....	5
3.2 Pin Description .....	6
4. Functional.....	8
4.1 IC Block Diagram .....	8
4.2 Functional Description .....	9
5. Electrical Specification .....	12
5.1 Absolute Maximum Ratings.....	12
5.2 Recommended Operation Conditions .....	12
5.3 Electrical Characteristics .....	12
5.4 Output Eye: EQ Settings and Input Trace Length (Informative).....	18
6. Application .....	20
6.1 HDMI 1.8V DDC Buffer Usage Case .....	20
6.2 Application Block Diagram .....	21
6.3 Output Eye Measurement Data.....	22
6.4 Layout Guidelines .....	23
6.5 HDMI Compliance Test.....	29
7. Mechanical Packaging .....	32
7.1 Mechanical Outline .....	32
7.2 Part Marking Information .....	33
7.3 Tape & Reel Materials and Design.....	34
8. Important Notice .....	37

### 3. Pin Configuration

#### 3.1 Package Pin-out



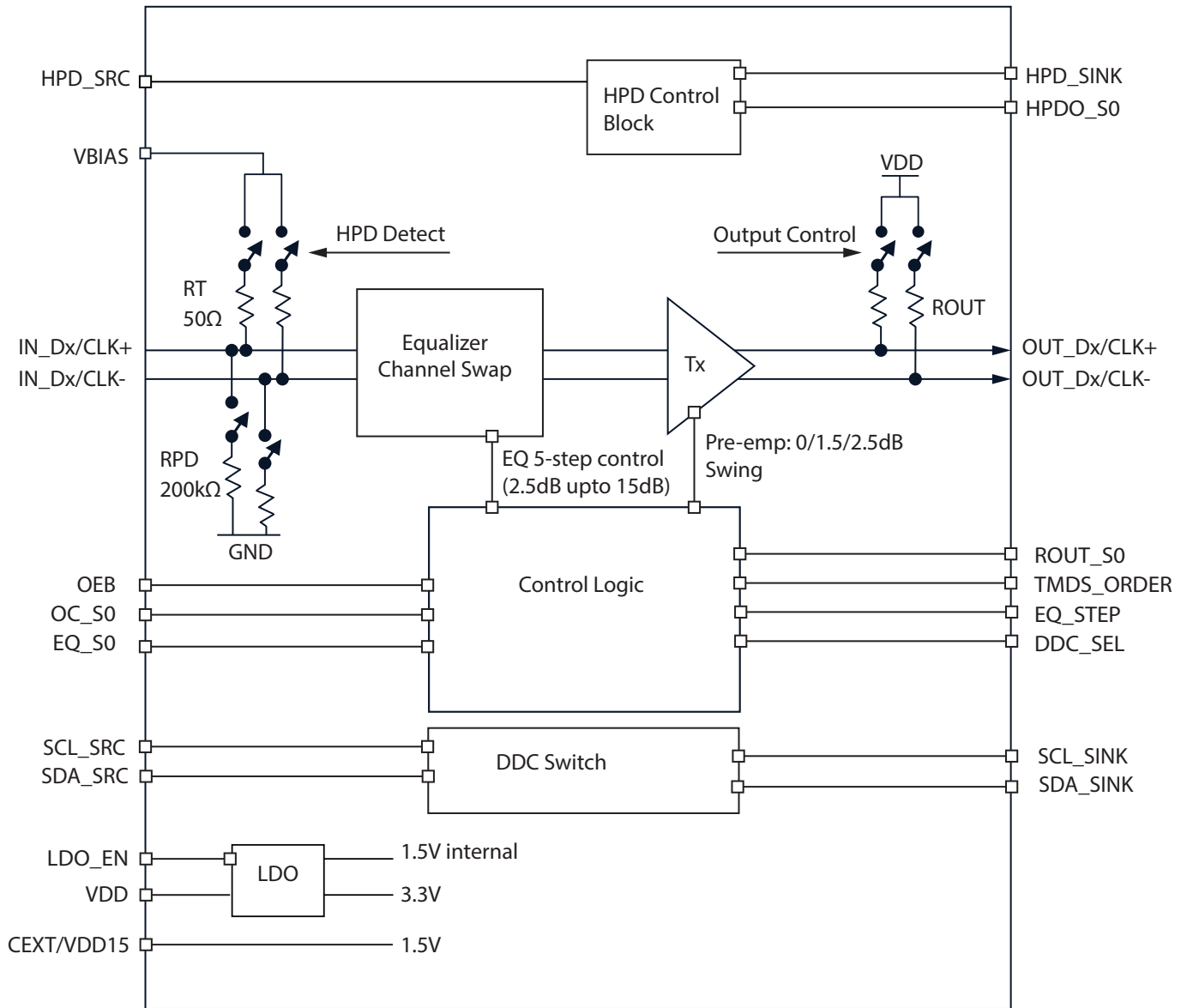
### 3.2 Pin Description

Pin #	Pin Name	Type	Description
1	VDD	PWR	3.3V power supply. Add external 0.1uF decoupling capacitor to GND.
2	CEXT/VDD15	PWR	LDO output for internal core power supplier. VDD15: When LDO_EN is low "0", this shared pin be a VDD15 in dual power supply operation. Apply 1.5V power CEXT: When LDO_EN is high "1", this pin be a CEXT in 3.3V single power supply operation. Add external capacitor (2.2uF-4.7uF) to GND.
3	IN_D2-	I	TMDS inputs. RT=50Ω and RPD=200 kΩ.
4	IN_D2+	I	TMDS inputs. RT=50Ω and RPD=200 kΩ.
5	IN_D1-	I	TMDS inputs. RT=50Ω and RPD=200 kΩ.
6	IN_D1+	I	TMDS inputs. RT=50Ω and RPD=200 kΩ.
7	VDD	PWR	3.3V power supply. Add external 0.1uF decoupling capacitor to GND.
8	IN_D0-	I	TMDS inputs. RT=50Ω and RPD=200 kΩ.
9	IN_D0+	I	TMDS inputs. RT=50Ω and RPD=200 kΩ.
10	IN_CLK-	I	TMDS inputs. RT=50Ω and RPD=200 kΩ.
11	IN_CLK+	I	TMDS inputs. RT=50Ω and RPD=200 kΩ.
12	HPD_SRC	O	HPD output to source side
13	TMDS_ORDER	I	TMDS pin order swap control with internal pull high. Default is D2/D1/D0/CLK input sequence.
14	HPDO_S0	I	HPD_SRC output control with internal pull high. Default is Open drain output
15	GND	GND	Ground
16	SDA_SRC	IO	Source side DDC Data
17	SCL_SRC	IO	Source side DDC Clock
18	GND	GND	Ground
19	ROUT_S0	I	TMDS output enable with double termination or open-drain selection. Default is Active high, double termination output. Active low is open-drain output. Internal pull high to VDD.
20	OC_S0	I	TMDS output pre-emphasis value selection. Default is 1.5dB pre-emphasis setting. Internally tied with 50% of VDD (or VDD/2).
21	DDC_SEL	I	DDC buffer or Passive switch control. Default is Passive switch mode. Internal pull high.
22	VBIAS	I	TMDS input termination voltage control. Default is HDMI input mode. Internally pull high. Pull-down is for Displayport input mode.
23	EQ_STEP	I	EQ_step selection control. Default is low-side setting of 2.5/5/7.5dB. Internally pull high. High-side EQ values are 5/10/15dB with external pull-down.
24	EQ_S0	I	TMDS input three-level equalization selection. Default is middle EQ value setting. Internally 50% of VDD (VDD/2).
25	OUT_CLK+	O	TMDS outputs with ROUT=50Ω, when ROUT_S0= "1"
26	OUT_CLK-	O	TMDS outputs with ROUT=50Ω, when ROUT_S0= "1"
27	OUT_D0+	O	TMDS outputs with ROUT=50Ω, when ROUT_S0= "1"
28	OUT_D0-	O	TMDS outputs with ROUT=50Ω, when ROUT_S0= "1"

Pin #	Pin Name	Type	Description
29	VDD	PWR	3.3V power supply. Add external 0.1uF decoupling capacitor to GND.
30	OUT_D1+	O	TMDS outputs with ROUT=50Ω, when ROUT_S0= "1"
31	OUT_D1-	O	TMDS outputs with ROUT=50Ω, when ROUT_S0= "1"
32	OUT_D2+	O	TMDS outputs with ROUT=50Ω, when ROUT_S0= "1"
33	OUT_D2-	O	TMDS outputs with ROUT=50Ω, when ROUT_S0= "1"
34	SCL_SINK	IO	Sink side DDC Clock for connector
35	SDA_SINK	IO	Sink side DDC Data for connector
36	HPD_SINK	I	Sink side HPD (Hot Plug Detect) input. Active high pin. Default is inactive for power saving. Internally pull-down at 120 kOhm.
37	GND	GND	Ground
38	OEB	I	Output Enable control. Active low for normal operation. Active high for disable output HDMI signals. Internally pull-down with 100 kΩ.
39	GND	GND	Ground
40	LDO_EN	I	Power supply mode control pin for 1.5/3.3V or 3.3V Default is 3.3V operation with active high. Internally pull high. 1.5/3.3V dual power is active low.
EPAD	EPAD	GND	Ground

**4. Functional**

**4.1 IC Block Diagram**



## 4.2 Functional Description

### Squelch Mode

Automatic output squelch function disables TMDS output when no Input signal presents. Output Disable (Squelch) Mode uses TMDS Clock signal detection. When low voltage levels on the TMDS input clock are detected, Squelch state enables and TMDS outputs shall be disabled. When the TMDS clock inputs are above the pre-determined threshold voltage, TMDS outputs shall return to the normal swing voltage levels.

### TMDS Output Shut Down

When HPD\_SINK pin floats or ties to GND, TMDS outputs shall shut down to sleep mode; HPD\_SINK does not control DDC channel. TMDS Pin Order Configuration Table

TMDS_ORDER	Functional Description	Note
"0"	CLK/D0/D1/D2 pin order	
"1" or "NC"	D2/D1/D0/CLK pin order	Default

### DDC mode selection DDC\_SEL Configuration Table

DDC_SEL	Functional Description	Note
"0"	Active DDC Buffer	
"1" or "NC"	Passive Switch	Default

### LDO Enable Configuration Table

LDO_EN	Pin 1	Pin 2	Functional Description
"0"	3.3V	1.5V	Dual power supply mode 3.3/1.5V
"1"	3.3V	External capacitor	Default. Recommend 2.2~4.7uF pull down capacitor.

### Pre-emphasis Truth Table

ROUT_S0	OC_S0	Single-end Vswing	Pre-emphasis	Functional Description
"0"	"0"	500 mV	0 dB	Open drain output.
	"NC" or VDD/2	500 mV	1.5 dB	Open drain output(Default)
	"1"	500 mV	2.5 dB	Open drain output
"1"	"0"	500 mV	0 dB	Double termination
	"NC" or VDD/2	500 mV	1.5 dB	Double termination(Default)
	"1"	500 mV	2.5 dB	Double termination

### TMDS Input Termination Voltage Control VBIAS

VBIAS	Functional Description
"1", "NC"	HDMI input. VBIAS ties to VDD.
"0"	DisplayPort input. VBIAS ties to GND.

### EQ Step Selection Control EQ\_STEP

EQ_STEP	Functional Description
"1", "NC"	2.5, 5, 7.5dB EQ setting with EQ_S0 control pin
"0"	5, 10, 15dB EQ setting with EQ_S0 control pin

### Output Data Signals EQ\_S0 Configuration

EQ_S0	Functional Description		Note
	EQ_STEP = "1"	EQ_STEP = "0"	
"0"	2.5 dB	5 dB	TMDS Clock(CLK) channel EQ is always fixed as 3dB without pre-emphasis.
"NC", "VDD/2"	5 dB	10 dB	
"1"	7.5 dB	15 dB	

### Sink side Hot Plug Detect HPD\_SINK

HPD_SINK	Functional Description
"1"	Normal mode
"0"	Disable output signal for power saving mode

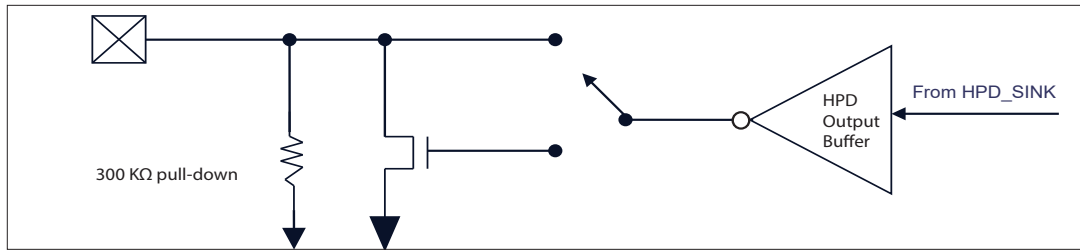
### Source side Hot Plug Detect Output Control HPDO\_S0

HPDO_S0	Functional Description
"1" or "NC"	Open drain output (Default)
"0"	Inverted Buffer output of HPD_SINK signal

### Output Enable Control Truth Table

OEB	Functional Description
"0"	Active Low. Normal mode
"1"	Disable output signal for power saving mode

### Source-side Output Block Diagram



Note:

(1) Open drain buffer is recommended with external pull-up resistor to < 4.5V power supply.

## 5. Electrical Specification

### 5.1 Absolute Maximum Ratings

Supply Voltage to Ground Potential.....	-0.5 to +4.5V
All input and Output pins .....	-0.5 to 4.5V
5V Tolerance I/O Pins (SDA_SINK, SCL_SINK, HPD_SINK) .....	-0.5 to 5.5V
Power Dissipation Continuous.....	1.0W
ESD, HBM .....	-2kV to 2kV
Storage Temperature .....	-65 °C to +150 °C
Junction temperature T <sub>J</sub> .....	125°C

Note:  
 (1) Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to beyond the absolute maximum rating conditions for extended periods may affect inoperability and degradation of device reliability and performance.

### 5.2 Recommended Operation Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Power Supply Voltage	2.89	3.3	3.6	V
		1.42	1.5	1.57	
T <sub>A</sub>	Ambient Operating Temperature	0		70	°C
	Industrial Operating Temperature	-40		85	°C

Note  
 (1) Industrial temperature -40 to +85 °C can be guaranteed by design. Commercial temperature 0 to +70 °C is supported by the production-tested.

### 5.3 Electrical Characteristics

#### 5.3.1 DC electrical

##### Power Consumption

Sym- bol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Single power supply						
I <sub>DD33</sub>	3.3V Power @ 0dB Pre-Emp	Outputs Enable (open drain 500mV, 0 dB pre-emphasis). terminated OUT_D [0:2] and CLK with 50 ohms to VDD. Exclude 40mA current pass-through from source devices		110		mA
I <sub>DD33</sub>	3.3V Power@ 0dB Pre-Emp	Outputs Enable (Double termination 500mV, 0 dB pre-emphasis). terminated OUT_D [0:2] and CLK with 50 ohms to VDD. Exclude 40mA current pass-through from source devices		180		mA

Sym- bol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_{DD33}$	3.3V Power @ 2.5dB Pre-Emp	Outputs Enable (Open Drain 500mV, 2.5 dB pre-emphasis). terminated OUT_D [0:2] and CLK with 50 ohms to VDD. Exclude 40mA current pass-through from source devices		133		mA
$I_{DD33}$	3.3V Power @ 2.5dB Pre-Emp	Outputs Enable (Double termination 500mV, 2.5 dB pre-emphasis). terminated OUT_D [0:2] and CLK with 50 ohms to VDD. Exclude 40mA current pass-through from source devices		211		mA
<b>Dual power supply</b>						
$I_{DD15}$	1.5V @ open drain 500mV, 0 dB	Outputs Enable ( open drain 500mV, 0 dB pre-emphasis), terminated OUT_D [0:2] and CLK with 50 ohms to Vdd		58	70	mA
	1.5V @ double termination 500mV, 0 dB	Outputs Enable ( open drain 500mV, 0 dB pre-emphasis), terminated OUT_D [0:2] and CLK with 50 ohms to Vdd		78.2		mA
	1.5V @ double termination 500mV, 2.5 dB	Outputs Enable ( open drain 500mV, 0 dB pre-emphasis), terminated OUT_D [0:2] and CLK with 50 ohms to Vdd		93.2		mA
$I_{DD33}$	3.3V IO current			2	3	mA
<b>Stand-by current</b>						
$I_{STB}$	Standby mode Current; VDD = 3.6V	DDC passive switch ( open drain & double termination); OEB = 1, HPD_SINK = 0		40 <sup>(1)</sup>		$\mu$ A
		DDC active buffer ( open drain & double termination); OEB = 1, HPD_SINK = 0,		1.5		mA
		DDC Passive Switch ( open drain & double termination); OEB= 1 and HPD_SINK = 0		0		mA
		DDC active buffer ( open drain & double termination); OEB= 0 and HPD_SINK = 0		1.44		mA
<b>Squelch Current</b>						
$I_{SQLH}$	Squelch mode current; VDD = 3.6V	DDC passive switch; No input clock VDD=3.6V, HPD_SINK=3.6V		2.68	3.0	mA
		DDC active buffer; No input clock VDD=3.6V, HPD_SINK=3.6V		3.52	4.1	mA

Note:  
(1) Current is due to internal 100k $\Omega$  pull-down of OE pin drawing extra current (~36 $\mu$ A). If forced by a separate power supply with all other control pins open, lower current is seen (~4 $\mu$ A).

### HPD Pins

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>HPD_SRC</b>						
V <sub>OL</sub>	Buffer Output Low Voltage	IOL = 4 mA			0.4	V
	Open Drain Output Low Voltage	IOL = 4 mA	0		0.4	V
V <sub>OH</sub>	Buffer Output High Voltage	IOH = 0.1 mA	VDD-1.55			V
I <sub>OFF</sub>	Off leakage current	VDD=0, VIN=3.6V			25	uA
I <sub>OZ</sub>	Open drain Output leakage current	VDD=3.6V, VIN=3.6V			25	
<b>HPD_SINK</b>						
I <sub>TH</sub>	High level digital input current	VIH =5.5V	-10		80	μA
I <sub>IL</sub>	Low level digital input current	VIL = GND	-10		10	μA
V <sub>IH</sub>	High level digital input voltage	VDD=3.3V	2.0			V
V <sub>IL</sub>	Low level digital input voltage		0		0.8	V

### Control pins

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>OEB with 100k pull to GND</b>						
I <sub>TH</sub>	High level digital input current	VIH = 3.3V, VDD=3.3V	-10		80	μA
I <sub>IL</sub>	Low level digital input current	VIL = GND	-10		10	μA
V <sub>IH</sub>	High level digital input voltage		2.0			V
V <sub>IL</sub>	Low level digital input voltage		0		0.8	V
<b>EQ_S0, OC_S0 with 100k pull high and 100k pull low when TMDS is active</b>						
I <sub>TH</sub>	High level digital input current	VIH =3.3V, VDD=3.3V	-10		40	μA
I <sub>IL</sub>	Low level digital input current	VIL = GND, VDD=3.3V	-40		10	μA
<b>ROUT_S0, TMDS_ORDER, EQ_STEP, VBIAS, LDO_EN, DDC_SEL, HPDO_S0</b>						
I <sub>TH</sub>	High level digital input current	VIH =VDD	-10		10	μA
I <sub>IL</sub>	Low level digital input current	VIL = GND	-20		10	μA
V <sub>IH</sub>	High level digital input voltage		2.0			V
V <sub>IL</sub>	Low level digital input voltage		0		0.8	V

### DDC Channel Switch

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I <sub>LK</sub>	Input leakage current	DDC switch is off, Vin = 5.5V	-10		30	μA
C <sub>IO</sub>	Input/Output capacitance when passive switch on	V <sub>Ipp</sub> (peak-peak) = 1V, 100 kHz		10		pF
R <sub>ON</sub>	Passive Switch resistance	IO = 3mA, VO = 0.4V		30	50	Ω
V <sub>PASS</sub>	Switch Output voltage	VI=3.3V, II=100uA VDD=3.3V	1.5	2.0	2.5	V

### DDC Channel Buffers

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{IH\_SRC}$	Source Side DDC Buffer Input High Voltage		0.6			V
$V_{IL\_SRC}$	Source Side DDC Buffer Input Low Voltage				0.4	V
$V_{OL\_SRC}$	Source Side DDC Buffer Output Low Voltage	External pull-up to VDD from 1.5k $\Omega$ to 10k $\Omega$	0.47	0.52	0.6	V
$V_{OL\_SINK}$	Sink Side DDC Buffer Output Low Voltage				0.2	V
$V_{IH\_SINK}$	Sink Side DDC Buffer Input High Voltage		2.0			V
$V_{IL\_SINK}$	Sink Side DDC Buffer Input Low Voltage				0.8	V
$C_{L\_SRC}$	Source side DDC capacitance when active switch is on, or passive switch off	V <sub>Ipp</sub> (peak-peak)=1V, 100 KHz		5		pF
$C_{L\_SINK}$	Sink side DDC capacitance when active switch is on, or passive switch off			5		pF

### TMDS Differential Pins

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{OH}$	Single-ended high level output voltage	VDD = 3.3V, ROUT=50 $\Omega$	VDD-10		VDD+10	mV
$V_{OL}$	Single-ended low level output voltage		VDD-600		VDD-400	mV
$V_{SWING}$	Single-ended output swing voltage		400		600	mV
$V_{OD(O)}^{*1}$	Overshoot of output differential voltage				180 <sup>*1</sup>	mV
$V_{OD(U)}^{*2}$	Undershoot of output differential voltage				200 <sup>*2</sup>	mV
$V_{OC(SS)}$	Change in steady-state common- mode output voltage between logic states				5	mV
$I_{OS}$	Short Circuit output current at open drain mode	Short to VDD	-12		12	mA
	Short Circuit output current at double termination mode	Short to VDD	-24		24	mA
$V_{I(open)}$	Single-ended input voltage under high impedance or open case	I <sub>I</sub> = 10uA	VDD-10		VDD+10	mV
$R_T$	Input termination resistance	V <sub>IN</sub> = 2.9V	45	50	55	$\Omega$
$I_{OZ}$	Leakage current with Hi-Z I/O	VDD = 3.6V			30	$\mu$ A

Note

- (1) Overshoot of output differential voltage  $V_{OD(O)} = (V_{SWING(MAX)} * 2) * 15\%$   
(2) Undershoot of output differential voltage  $V_{OD(U)} = (V_{SWING(MIN)} * 2) * 25\%$

### 5.3.2 AC Electrical

#### TMDS differential pins

Symbol	Parameter	Test	Min.	Typ.	Max.	Units	
$t_{pd}$	Propagation delay	VDD = 3.3V, ROUT = 50Ω			2000	ps	
$t_r/t_f$	Differential output signal rise/fall time (20% - 80%), open drain, 0dB pre-emphasis				120		
	Differential output signal rise/fall time (20% - 80%), open drain, 2.5dB pre-emphasis				100		
$t_{sk}(p)$	Pulse skew				10		50
$t_{sk}(D)$	Intra-pair differential skew				23		50
$t_{sk}(o)$	Inter-pair differential skew						100
$t_{jit}(pp)$	Peak-to-peak output jitter CLK residual jitter	Data Input = 3.4 Gbps		30	60		
$t_{jit}(pp)$	Peak-to-peak output jitter DATA residual Jitter			40	70		
$t_{en}$	Enable time				50	μs	
$t_{dis}$	Disable time				0.01		

#### DDC I/O pins (Passive switch mode)

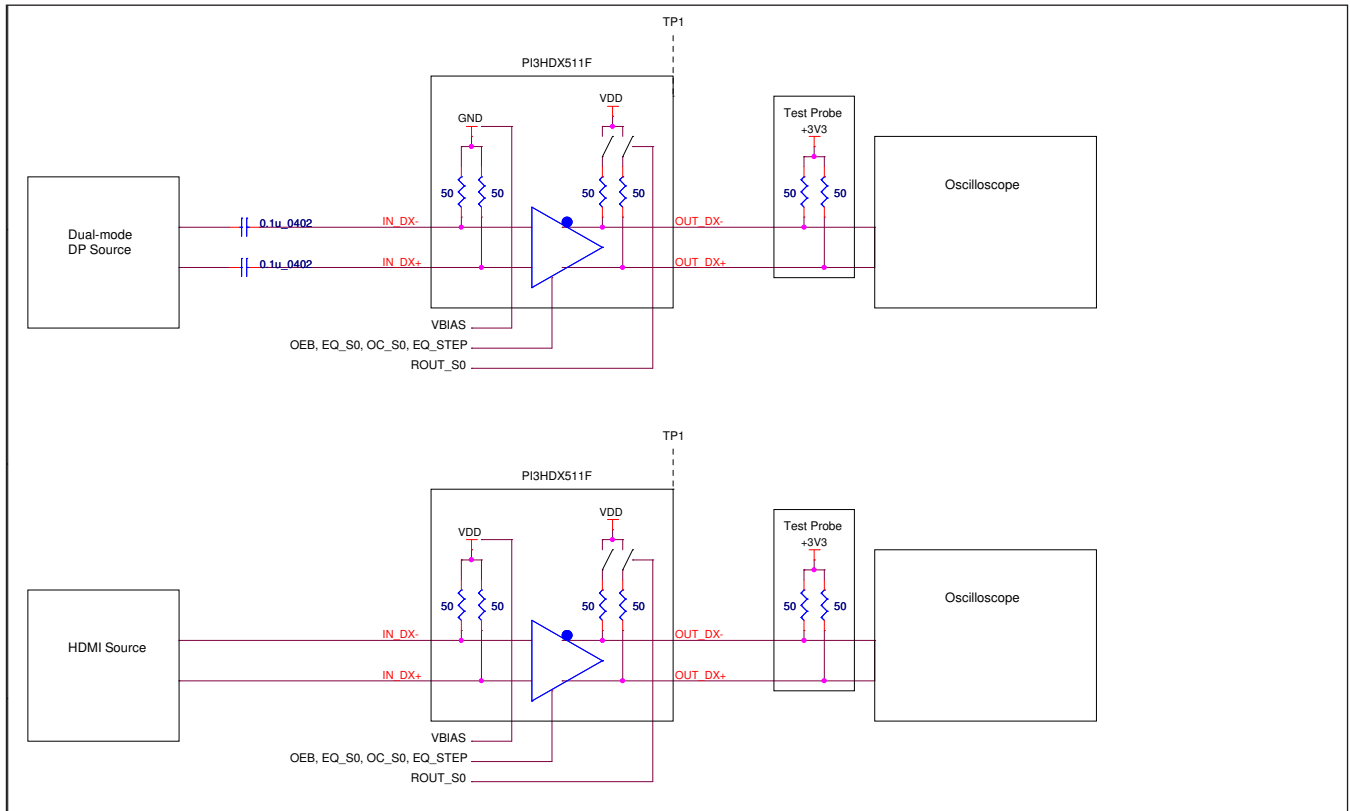
Symbol	Parameter	Test	Min.	Typ.	Max.	Units
$t_{pd}(DDC)$	Propagation delay from SCL_SINK/SDA_SINK to SCL/SDA, or SCL/ SDA to SCL_SINK/SDA_SINK in passive switch.	CL = 10pF in passive switch			5	ns

#### DDC I/O pins (Active buffer mode)

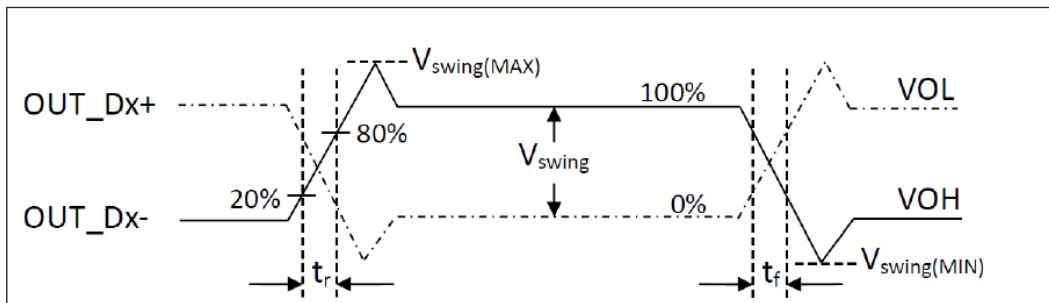
Symbol	Parameter	Test	Min.	Typ.	Max.	Units
$t_{PLH}$	LOW-to-HIGH propagation delay	SCL/SDA to SCL/SDA_SINK		169	255	ns
$t_{PHL}$	HIGH-to-LOW propagation delay	SCL/SDA to SCL/SDA_SINK	10	103	300	ns
$t_{PLH}$	LOW-to-HIGH propagation delay	SCL/SDA_SINK to SCL/SDA	25	67	110	ns
$t_{PHL}$	HIGH-to-LOW propagation delay	SCL/SDA_SINK to SCL/SDA		118	230	ns

#### Control and Status pins (HPD\_SINK, HPD)

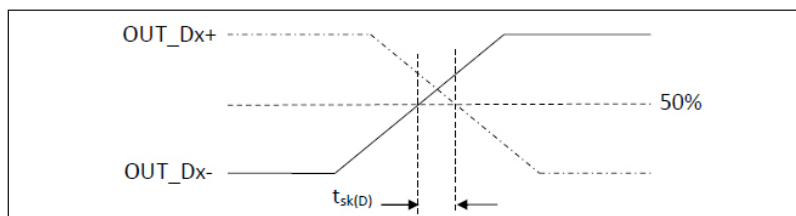
Symbol	Parameter	Test	Min.	Typ.	Max.	Units
$t_{pd}(HPD)$	Propagation delay from HPD_SINK to the active port of HPD, high to low	CL = 10pF, pull high resistor=1kΩ		10		ns



**Figure 5-1 Electrical Characteristic Test Circuit**



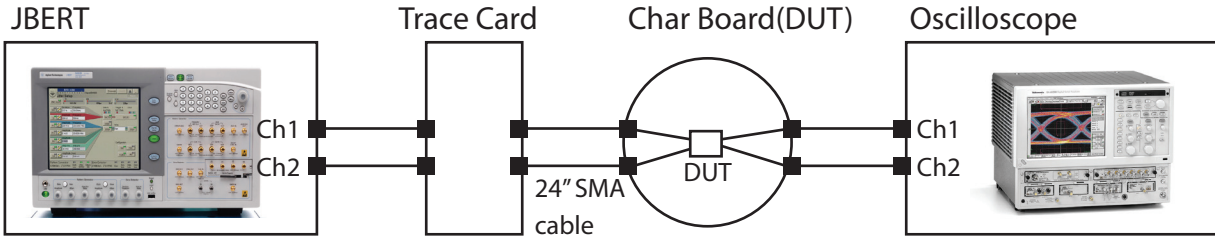
**Figure 5-2 Vswing,  $t_r/t_f$  Definition**



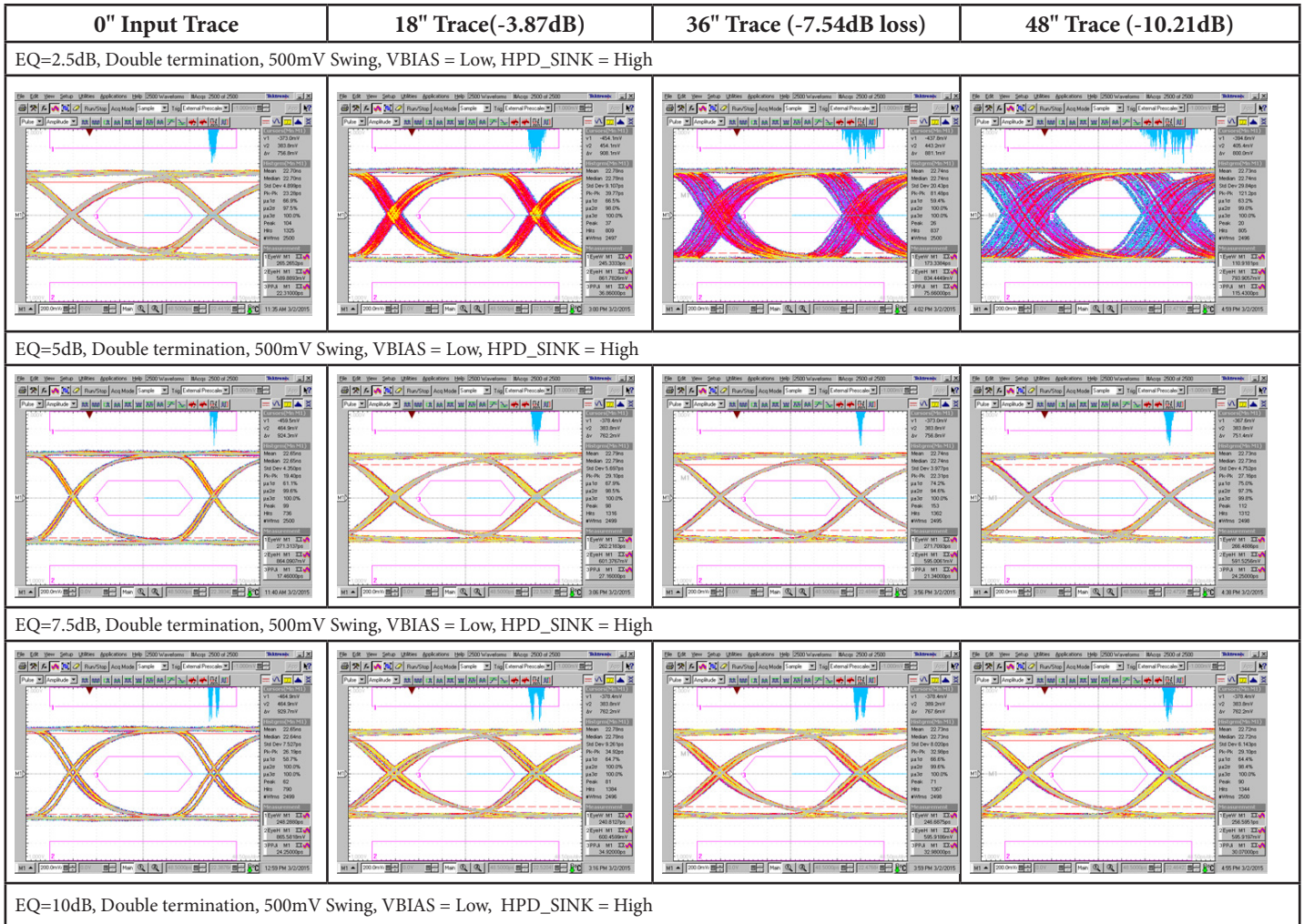
**Figure 5-3 Intra-pair Skew( $t_{sk(D)}$ ) Definition**

**5.4 Output Eye: EQ Settings and Input Trace Length (Informative)**

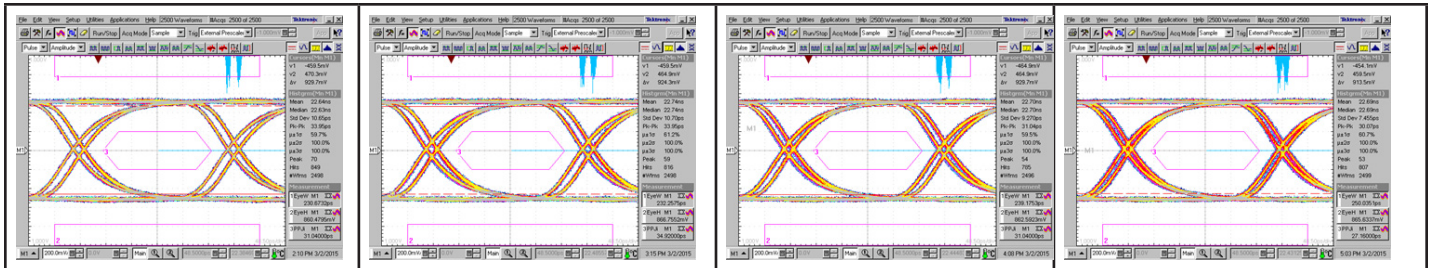
**5.4.1 Test Setup**



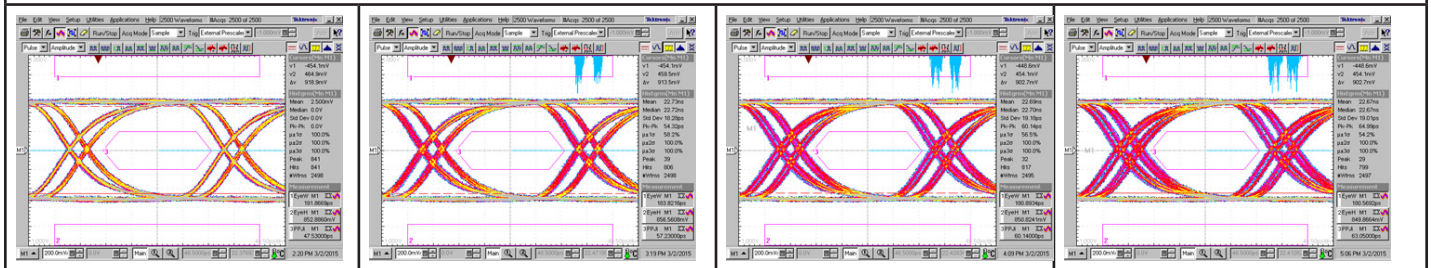
**5.4.2 Output waveforms**



**PI3HDX511F**



EQ=15dB, Double termination 500mV Swing, VBIAS = Low, HPD\_SINK = High

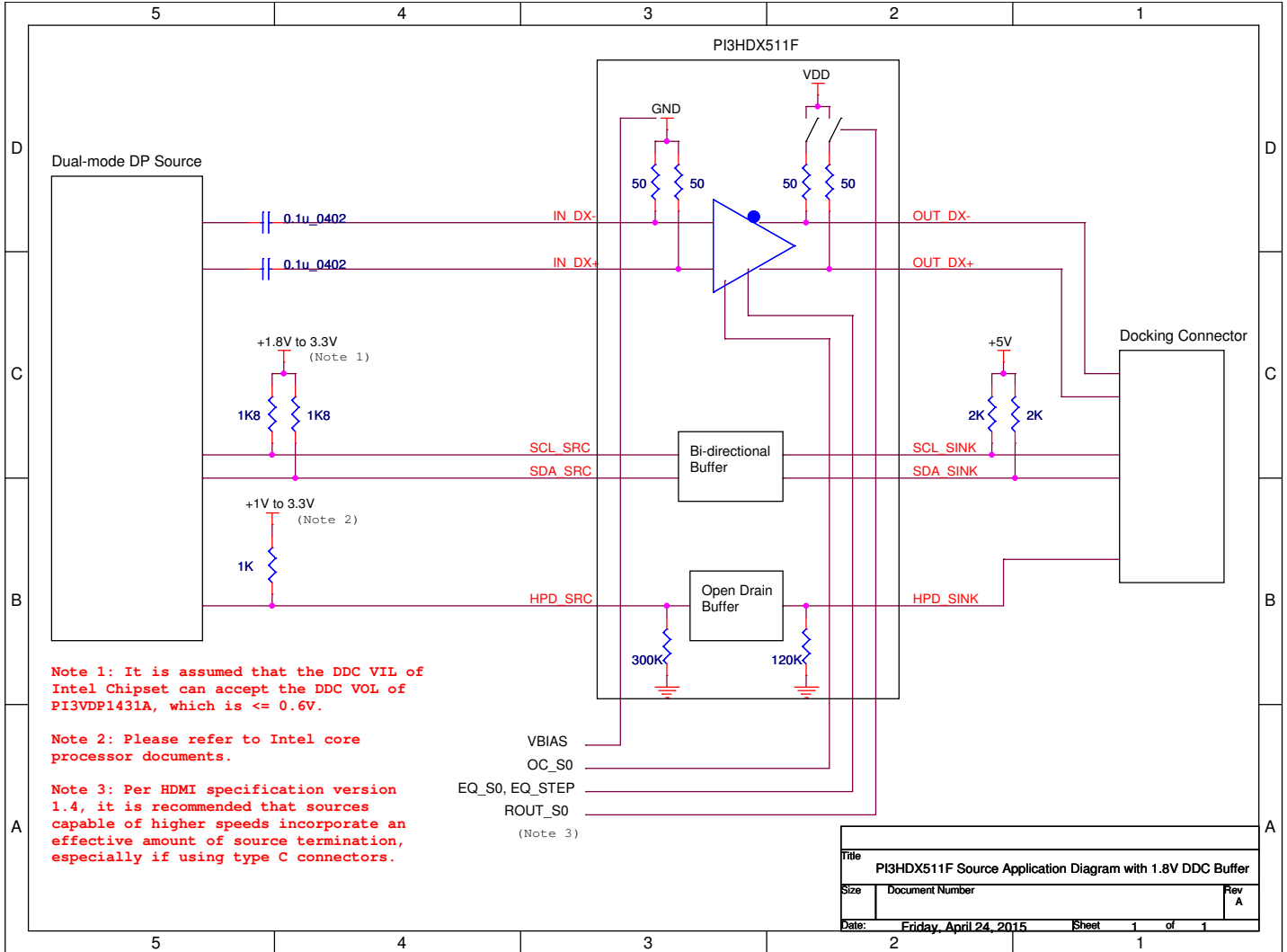


Note: For system designers reference, characterization trace board insertion Loss Informations and picture image are shown below.

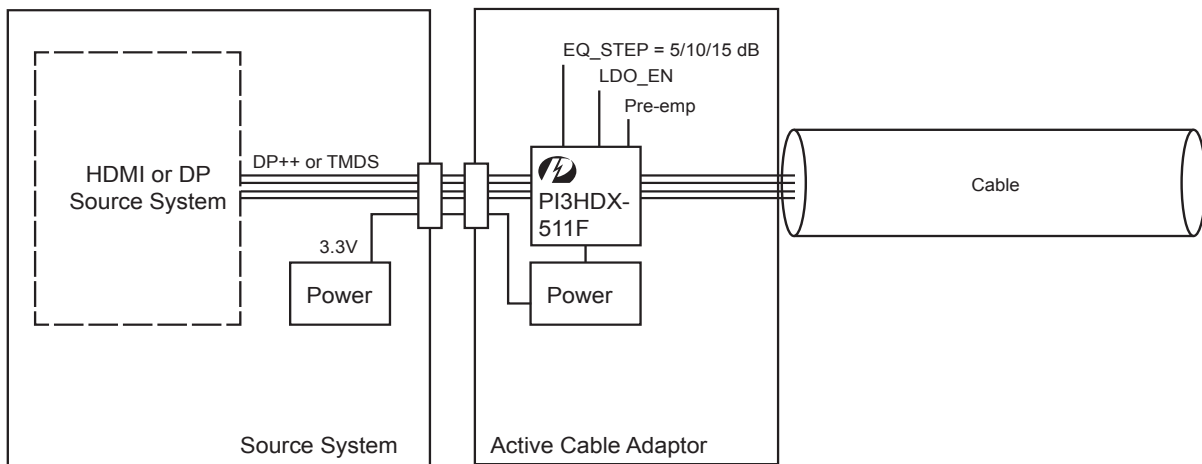
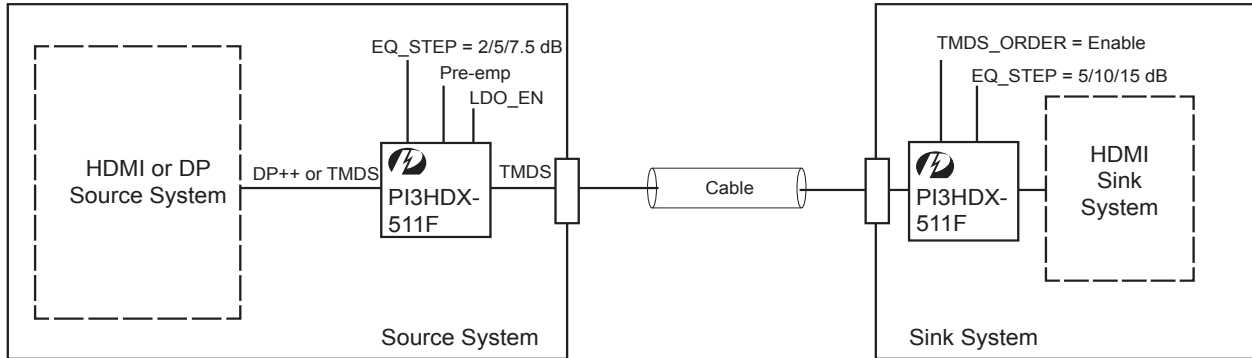
Frequency @3.4Gbps	4-in	6-in	12-in	18-in	24-in	30-in	36-in	48-in	Unit
Insertion Loss	-0.9	-1.34	-2.54	-3.87	-5.17	-6.34	-7.54	-10.21	dB

**6. Application**

**6.1 HDMI 1.8V DDC Buffer Usage Case**

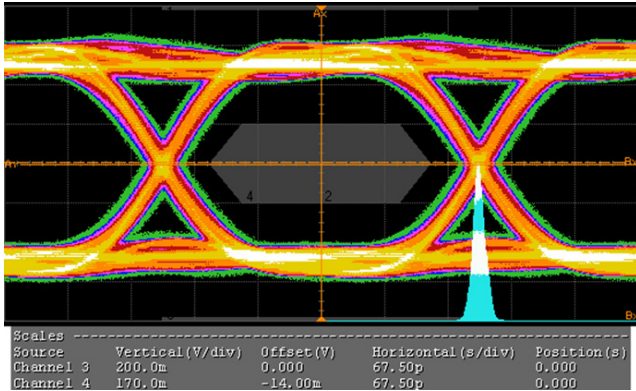


**6.2 Application Block Diagram**

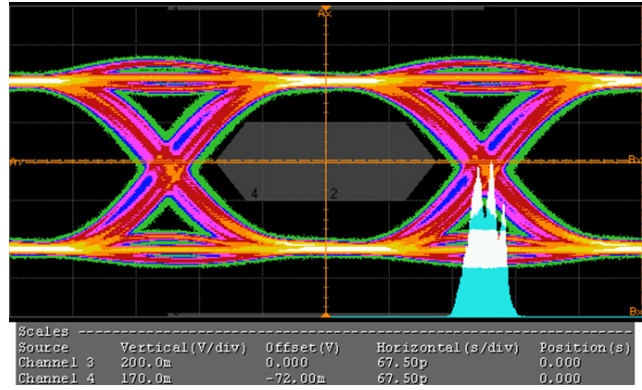


### 6.3 Output Eye Measurement Data

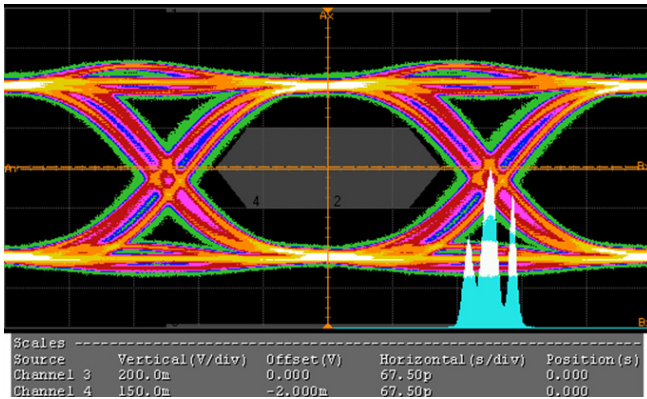
Sink Apps test set-up: Output Eye Diagram with different EQ settings of 1.5dB, 10dB and 15 dB. Trace Cards used with 24", 48" and 84" with 2 meter HDMI Cable with proper pre-emphasis setting.



24" Input (-15.46dB loss) , EQ=2.5dB, 500mV Swing, Pre-emp =1.5dB, Rout\_S0=1



48" Input, EQ=10dB, 500mV Swing, Pre-emp=0dB, Rout\_S0=1



84" Input, EQ=15dB, 500mV Swing, Pre-emp=0dB, Rout\_S0=1

Note: For system designers reference, AE-trace board information are shown below. Insertion loss is measured in the 3GHz (6.0 Gbps) speed.

FR4 trace length	0-in	6-in	12-in	18-in	24-in	30-in	36-in	Units
Insertion loss (dB)	-5.52	-9.35	-10.07	-12.66	-15.46	-16.57	-20.81	dB

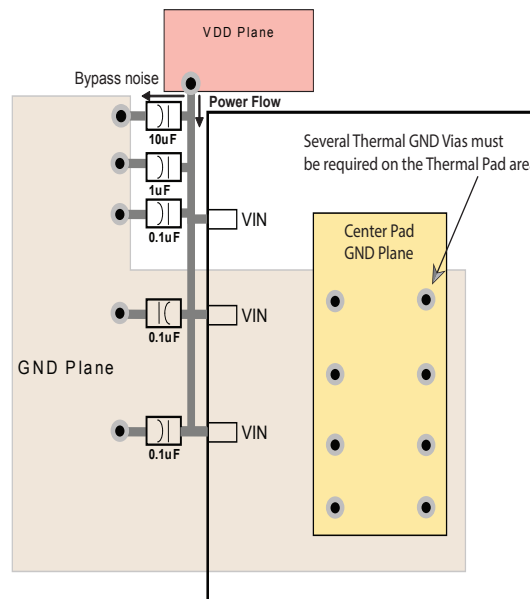
## 6.4 Layout Guidelines

As transmission data rate increases rapidly, any flaws and/or mis-matches on PCB layout are amplified in terms of signal integrity. Layout guideline for high-speed transmission is highlighted in this application note.

### 6.4.1 Power and Ground

To provide a clean power supply for Pericom high-speed device, few recommendations are listed below:

- Power (VDD) and ground (GND) pins should be connected to corresponding power planes of the printed circuit board directly without passing through any resistor.
- The thickness of the PCB dielectric layer should be minimized such that the VDD and GND planes create low inductance paths.
- One low-ESR 0.1uF decoupling capacitor should be mounted at each VDD pin or should supply bypassing for at most two VDD pins. Capacitors of smaller body size, i.e. 0402 package, is more preferable as the insertion loss is lower. The capacitor should be placed next to the VDD pin.
- One capacitor with capacitance in the range of 4.7uF to 10uF should be incorporated in the power supply decoupling design as well. It can be either tantalum or an ultra-low ESR ceramic.
- A ferrite bead for isolating the power supply for Pericom high-speed device from the power supplies for other parts on the printed circuit board should be implemented.
- Several thermal ground vias must be required on the thermal pad. 25-mil or less pad size and 14-mil or less finished hole are recommended.



**Figure 6-1 Decoupling Capacitor Placement Diagram**

### 6.4.2 High-speed signal Routing

Well-designed layout is essential to prevent signal reflection:

- For 90Ω differential impedance, width-spacing-width micro-strip of 6-7-6 mils is recommended; for 100Ω differential impedance, width-spacing-width micro-strip of 5-7-5 mils is recommended.
- Differential impedance tolerance is targeted at  $\pm 15\%$ .

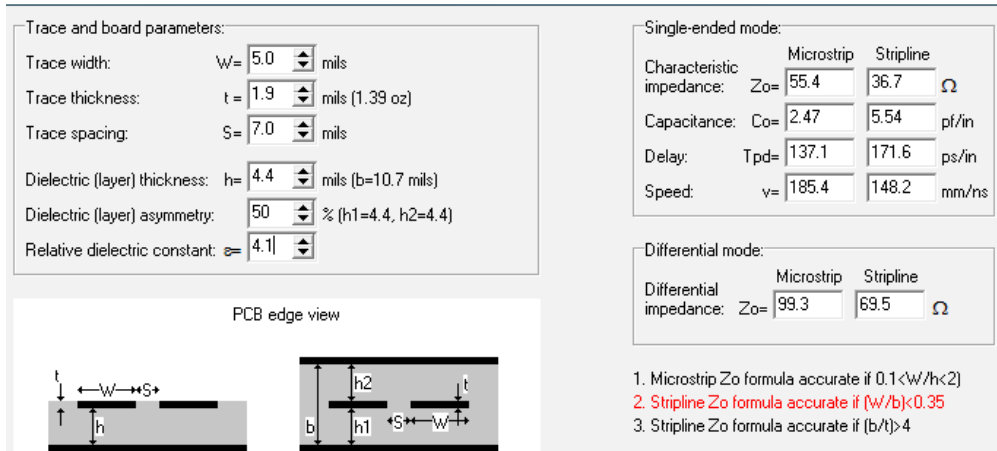
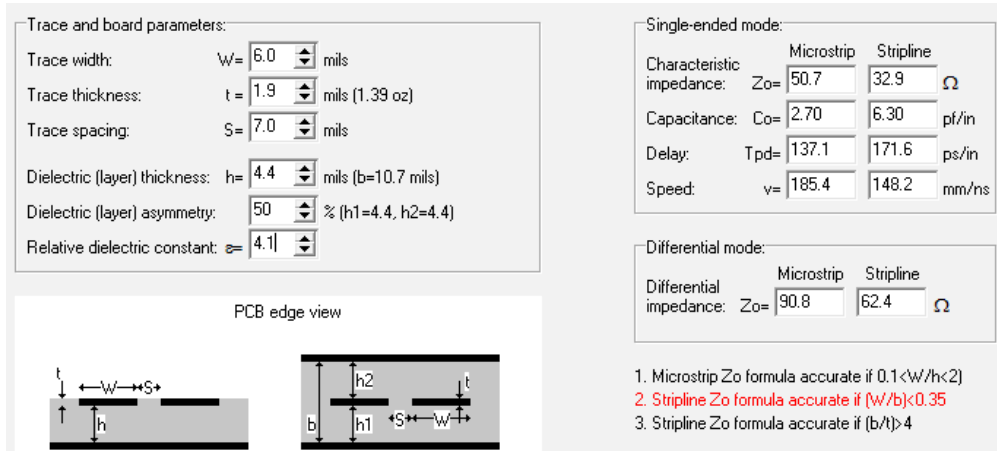


Figure 6-2 Trace Width and Clearance of Micro-strip and Strip-line

- For micro-strip, using 1/2oz Cu is fine. For strip-line in 6+ PCB layers, 1oz Cu is more preferable.

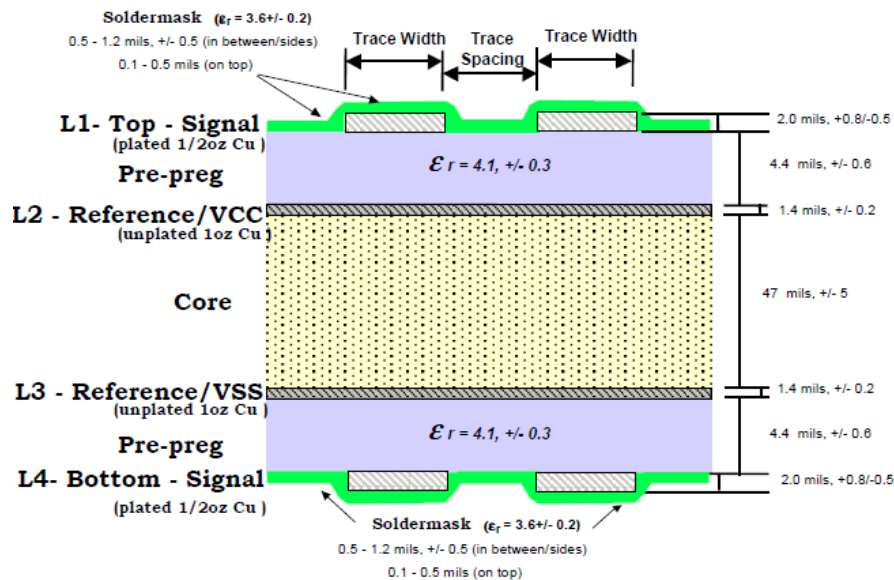
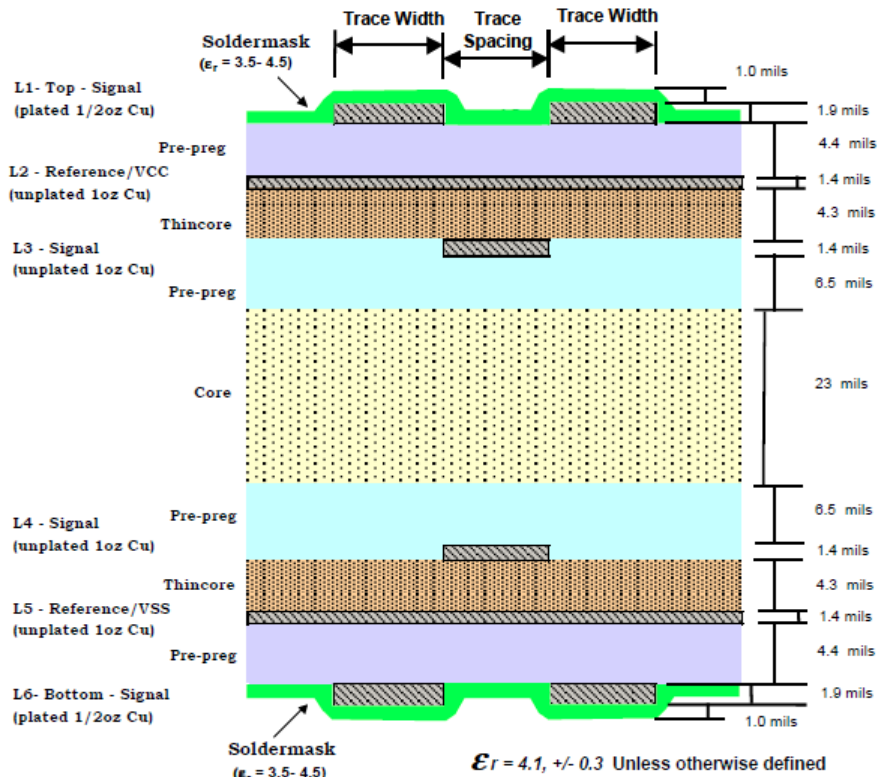
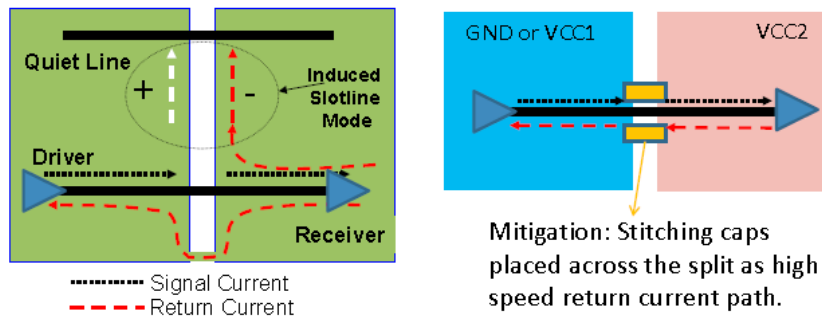


Figure 6-3 4-Layer PCB Stack-up Example



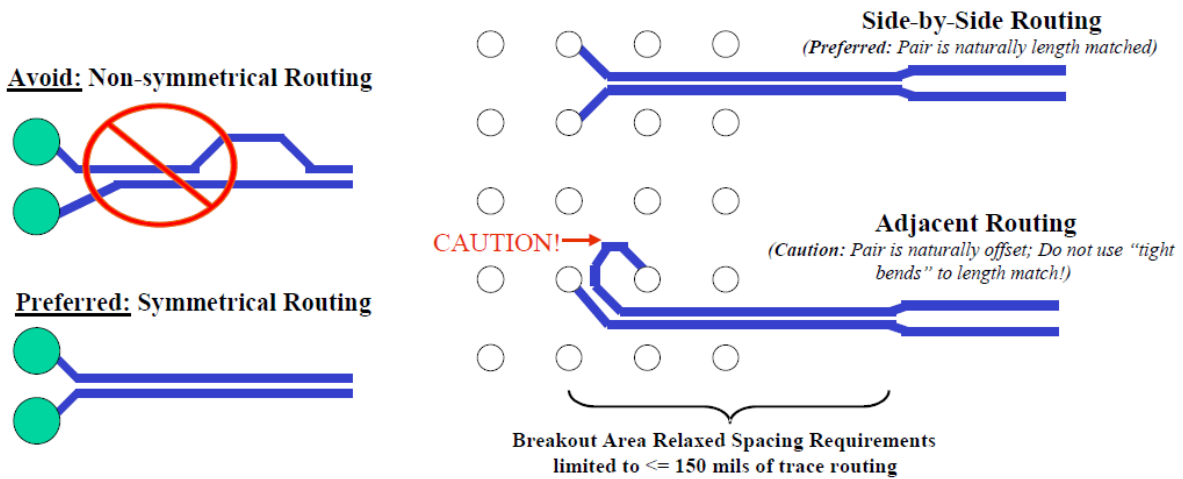
**Figure 6-4 6-Layer PCB Stack-up Example**

- Ground referencing is highly recommended. If unavoidable, stitching capacitors of 0.1uF should be placed when reference plane is changed.



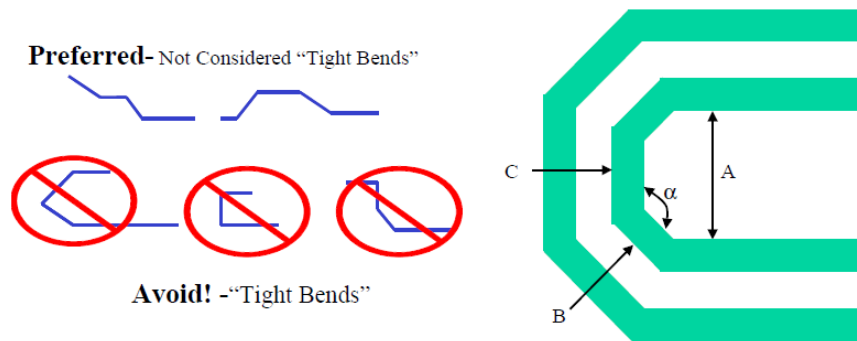
**Figure 6-5 Stitching Capacitor Placement**

- To keep the reference unchanged, stitching vias must be used when changing layers.
- Differential pair should maintain symmetrical routing whenever possible. The intra-pair skew of micro-strip should be less than 5 mils.
- To keep the reference unchanged, stitching vias must be used when changing layers.
- Differential pair should maintain symmetrical routing whenever possible. The intra-pair skew of micro-strip should be less than 5 mils.



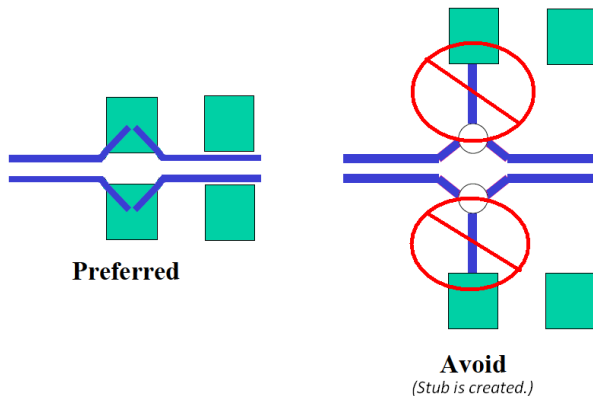
**Figure 6-6 Layout Guidance of Matched Differential Pair**

- For minimal crosstalk, inter-pair spacing between two differential micro-strip pairs should be at least 20 mils or 4 times the dielectric thickness of the PCB.
- Wider trace width of each differential pair is recommended in order to minimize the loss, especially for long routing. More consistent PCB impedance can be achieved by a PCB vendor if trace is wider.
- Differential signals should be routed away from noise sources and other switching signals on the printed circuit board.
- To minimize signal loss and jitter, tight bend is not recommended. All angles  $\alpha$  should be at least 135 degrees. The inner air gap A should be at least 4 times the dielectric thickness of the PCB.



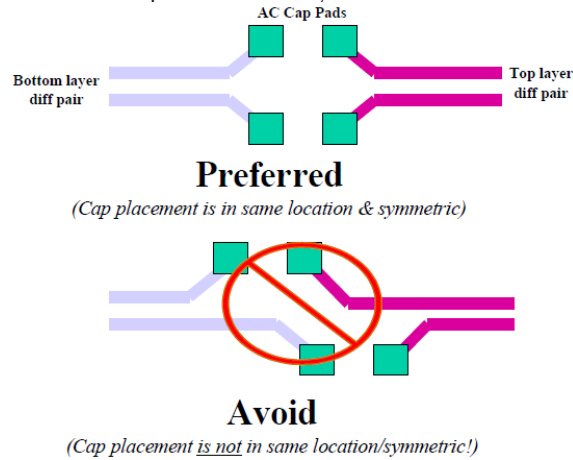
**Figure 6-7 Layout Guidance of Bends**

- Stub creation should be avoided when placing shunt components on a differential pair.



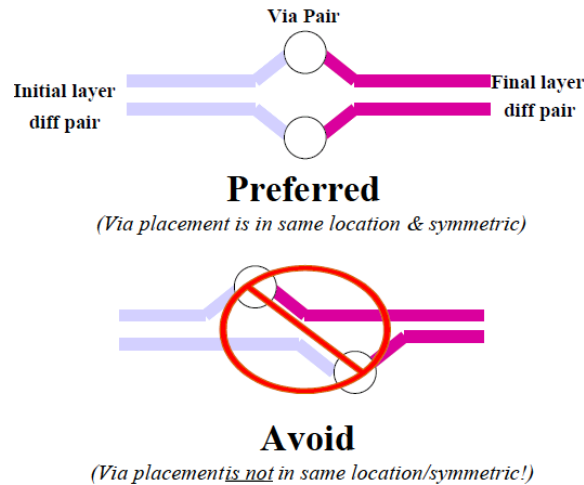
**Figure 6-8 Layout Guidance of Shunt Component**

- Placement of series components on a differential pair should be symmetrical.



**Figure 6-9 Layout Guidance of Series Component**

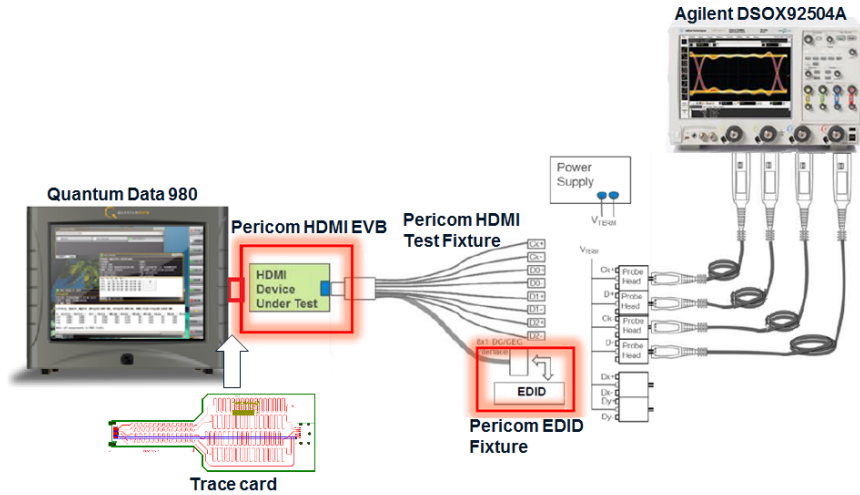
- Stitching vias or test points must be used sparingly and placed symmetrically on a differential pair.



**Figure 6-10 Layout Guidance of Stitching Via**

**6.5 HDMI Compliance Test**

**6.5.1 Test Set-up**



**Figure 6-11 HDMI CTS test setup**

Note:

(1) Application Trace Card Information

HDMI FR4 trace	0 in	6 in	12 in	18 in	24 in	30 in	36 in	Units
Insertion loss @ 3Gbps (estimated)	-2.96	-4.88	-5.24	-6.53	-7.94	-8.49	-10.60	dB

**6.5.2 HDMI Compliance Test Report: Pass**

Test Setup : Pericom SMA-to-HDMI Test Fixture, 12” and 36” SMA Cables, Pericom 36” FR4 Trace Cards, 2m 28AWG HDMI Cable.

## HDMI Test Report

**Overall Result:** PASS

Test Configuration Details	
Device Description	
Device ID	Transmitter
Fixture Type	Other
Probe Connection	4 Probes
Probe Head Type	N5444A
Lane Connection	1 Data Lane
HDMI Specification	2.0
HDMI Test Type	TMDS Physical Layer Tests
Test Session Details	
Infiniium SW Version	05.20.0013
Infiniium Model Number	DSOX92504A
Infiniium Serial Number	MY54410104
Application SW Version	2.11
Debug Mode Used	No
Probe (Channel 1)	Model: N2801A Serial: US54094067 Head: N5444A Atten: Calibrated (18 FEB 2015 11:16:48), Using Cal Atten (5.7831E+000) Skew: Calibrated (18 FEB 2015 11:16:56), Using Cal Skew
Probe (Channel 2)	Model: N2801A Serial: US54094054 Head: N5444A Atten: Calibrated (18 FEB 2015 11:19:29), Using Cal Atten (5.5882E+000) Skew: Calibrated (18 FEB 2015 11:13:57), Using Cal Skew
Probe (Channel 3)	Model: N2801A Serial: US54094059 Head: N5444A Atten: Calibrated (18 FEB 2015 11:15:19), Using Cal Atten (5.7320E+000) Skew: Calibrated (18 FEB 2015 11:15:29), Using Cal Skew
Probe (Channel 4)	Model: N2801A Serial: US54094057 Head: N5444A Atten: Calibrated (18 FEB 2015 11:11:30), Using Cal Atten (5.5123E+000) Skew: Calibrated (18 FEB 2015 11:12:12), Using Cal Skew
Last Test Date	2016-01-26 13:06:09 UTC +08:00

## Summary of Results

Test Statistics	
Failed	0
Passed	15
Total	15

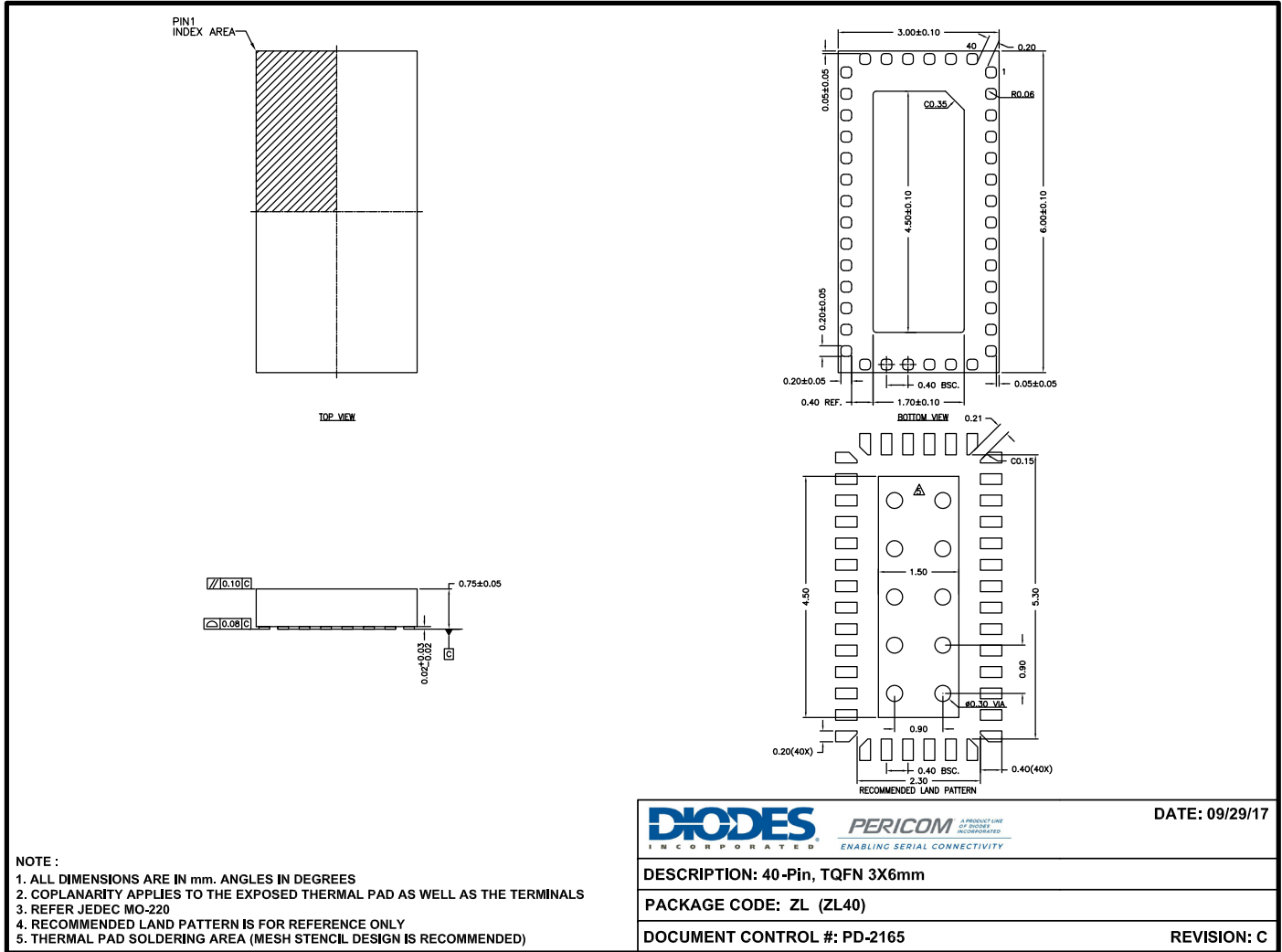
Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	7-9: Clock Jitter	144 mTbit	42.4 %	VALUE <= 250 mTbit
✓	0	1	7-4: Clock Rise Time	123.410 ps	64.5 %	VALUE >= 75.000 ps
✓	0	1	7-4: Clock Fall Time	122.160 ps	62.9 %	VALUE >= 75.000 ps
✓	0	1	7-8: Clock Duty Cycle(Minimum)	49.470	23.7 %	>=40%
✓	0	1	7-8: Clock Duty Cycle(Maximum)	50.130	16.5 %	<=60%
✓	0	1	7-10: D0 Data Jitter	249 m	17.0 %	<=0.3Tbit
✓	0	1	7-4: D0 Rise Time	104.503 ps	39.3 %	VALUE >= 75.000 ps
✓	0	1	7-4: D0 Fall Time	108.363 ps	44.5 %	VALUE >= 75.000 ps
✓	0	1	7-2: VL Clock +	2.853 V	15.7 %	LowerLimit V <= VALUE <= 2.900 V
✓	0	1	7-2: VL Clock -	2.845 V	18.3 %	LowerLimit V <= VALUE <= 2.900 V
✓	0	1	7-7: Intra-Pair Skew - Clock	115 mTbit	11.7 %	-150 mTbit <= VALUE <= 150 mTbit
✓	0	1	7-2: VL D0+	2.848 V	17.3 %	LowerLimit V <= VALUE <= 2.900 V
✓	0	1	7-2: VL D0-	2.853 V	15.7 %	LowerLimit V <= VALUE <= 2.900 V
✓	0	1	7-7: Intra-Pair Skew - Data Lane 0	81 mTbit	23.0 %	-150 mTbit <= VALUE <= 150 mTbit
✓	0	1	7-10: D0 Mask Test	0.000	50.0 %	No Mask Failures

**PI3HDX511F**

**7. Mechanical Packaging**

**7.1 Mechanical Outline**

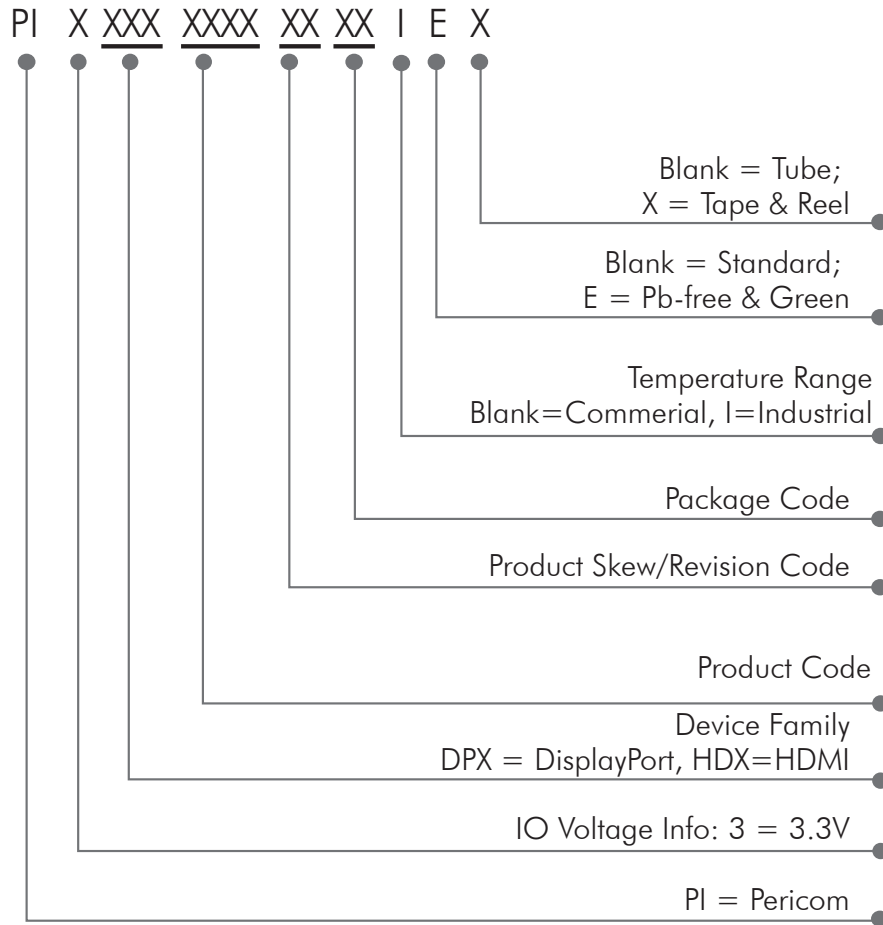


**NOTE:**

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS
3. REFER JEDEC MO-220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED)

**7.2 Part Marking Information**

Our standard product mark follows our standard part number ordering information, except for those products with a speed letter code. The speed letter code mark is placed after the package code letter, rather than after the device number as it is ordered. After electrical test screening and speed binning has been completed, we then perform an “add mark” operation which places the speed code letter at the end of the complete part number.



**Figure 7-1 Part marketing information**

### 7.3 Tape & Reel Materials and Design

#### Carrier Tape

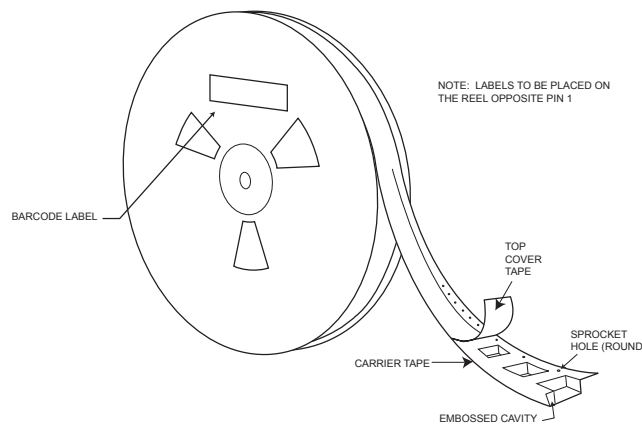
The Pocketed Carrier Tape is made of Conductive Polystyrene plus Carbon material (or equivalent). The surface resistivity is  $10^6 \text{ Ohm/sq.}$  maximum. Pocket tapes are designed so that the component remains in position for automatic handling after cover tape is removed. Each pocket has a hole in the center for automated sensing if the pocket is occupied or not, thus facilitating device removal. Sprocket holes along the edge of the center tape enable direct feeding into automated board assembly equipment. See Figures 3 and 4 for carrier tape dimensions.

#### Cover Tape

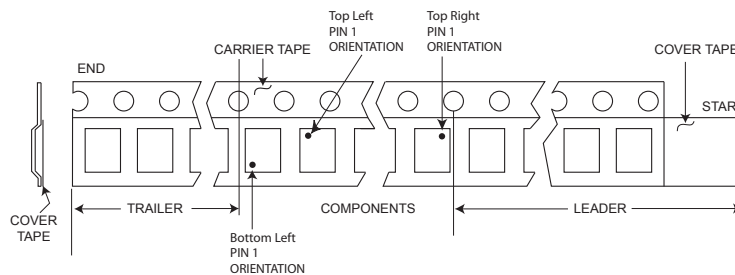
Cover tape is made of Anti-static Transparent Polyester film. The surface resistivity is  $10^7 \text{ Ohm/Sq.}$  Minimum to  $10^{11} \text{ Ohm sq.}$  maximum. The cover tape is heat-sealed to the edges of the carrier tape to encase the devices in the pockets. The force to peel back the cover tape from the carrier tape shall be a MEAN value of 20 to 80gm (2N to 0.8N).

#### Reel

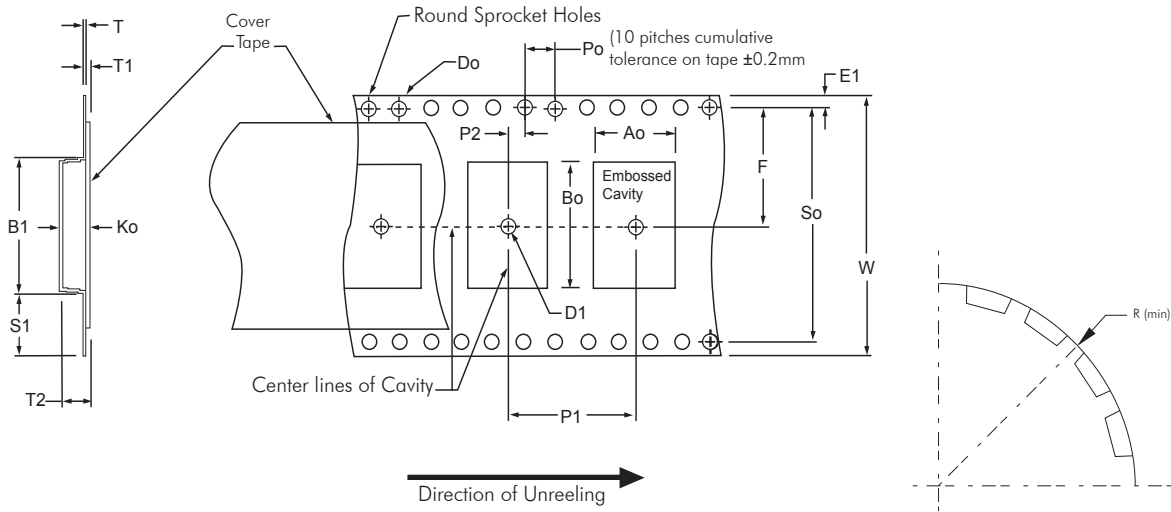
The device loading orientation is in compliance with EIA-481, current version (Figure 2). The loaded carrier tape is wound onto either a 13-inch reel, (Figure 4) or 7-inch reel. The reel is made of Antistatic High-Impact Polystyrene. The surface resistivity  $10^7 \text{ Ohm/sq.}$  minimum to  $10^{11} \text{ Ohm/sq.}$  max.



**Figure 7-2 Tape & Reel label information**



**Figure 7-3 Tape leader and trailer pin 1 orientations**



**Figure 7-4 Standard embossed carrier tape dimensions**

**Table 7-1. Constant Dimensions**

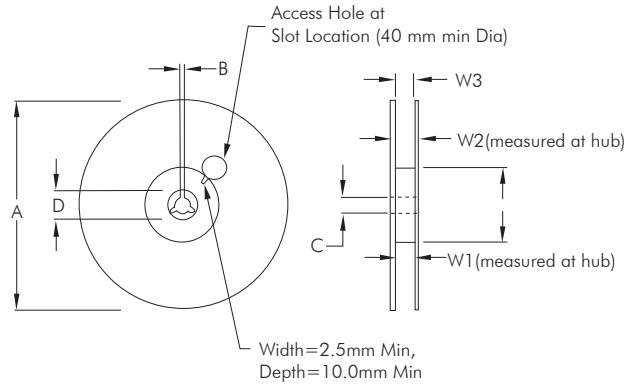
Tape Size	D0	D1 (Min)	E1	P0	P2	R (See Note 2)	S1 (Min)	T (Max)	T1 (Max)
8mm	1.5 +0.1 -0.0	1.0	1.75 ± 0.1	4.0 ± 0.1	2.0 ± 0.05	25	0.6	0.6	0.1
12mm		1.5			2.0 ± 0.1	30			
16mm									
24mm		2.0			2.0 ± 0.1	50	N/A (See Note 3)		
32mm									
44mm									

**Table 7-2. Variable Dimensions**

Tape Size	P <sub>1</sub>	B <sub>1</sub> (Max)	E <sub>2</sub> (Min)	F	So	T <sub>2</sub> (Max.)	W (Max)	A <sub>0</sub> , B <sub>0</sub> , & K <sub>0</sub>
8mm	Specific per package type. Refer to FR-0221 (Tape and Reel Packing Information)	4.35	6.25	3.5 ± 0.05	N/A (see note 4)	2.5	8.3	See Note 1
12mm		8.2	10.25	5.5 ± 0.05		6.5	12.3	
16mm		12.1	14.25	7.5 ± 0.1		8.0	16.3	
24mm		20.1	22.25	11.5 ± 0.1	12.0	24.3		
32mm		23.0	N/A	14.2 ± 0.1		28.4 ± 0.1	32.3	
44mm		35.0	N/A	20.2 ± 0.15	40.4 ± 0.1	16.0	44.3	

**NOTES:**

- A<sub>0</sub>, B<sub>0</sub>, and K<sub>0</sub> are determined by component size. The cavity must restrict lateral movement of component to 0.5mm maximum for 8mm and 12mm wide tape and to 1.0mm maximum for 16,24,32, and 44mm wide carrier. The maximum component rotation within the cavity must be limited to 20° maximum for 8 and 12 mm carrier tapes and 10° maximum for 16 through 44mm.
- Tape and components will pass around reel with radius “R” without damage.
- S<sub>1</sub> does not apply to carrier width ≥32mm because carrier has sprocket holes on both sides of carrier where D<sub>0</sub> ≥ S<sub>1</sub>.
- So does not exist for carrier ≤32mm because carrier does not have sprocket hole on both side of carrier.



**Table 7-3. Reel dimensions by tape size**

Tape Size	A	N (Min) See Note A	W1	W2(Max)	W3	B (Min)	C	D (Min)
8mm	178±2.0mm or 330±2.0mm	60 ±2.0mm or 100±2.0mm	8.4 +1.5/-0.0 mm	14.4 mm	Shall Accommodate Tape Width Without Interference	1.5mm	13.0 +0.5/-0.2 mm	20.2mm
12mm			12.4 +2.0/-0.0 mm	18.4 mm				
16mm	330 ±2.0mm	100 ±2.0mm	16.4 +2.0/-0.0 mm	22.4 mm				
24mm			24.4 +2.0/-0.0 mm	30.4 mm				
32mm			32.4 +2.0/-0.0 mm	38.4 mm				
44mm			44.4 +2.0/-0.0 mm	50.4 mm				

**NOTE:**

A. If reel diameter A=178 ±2.0mm, then the corresponding hub diameter (N(min)) will be 60 ±2.0mm. If reel diameter A=330±2.0mm, then the corresponding hub diameter (N(min)) will be 100±2.0mm.

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1. are intended to implant into the body, or
2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

Customers represent that they have all necessary expertise in the safety and regulatory ramifications of their life support devices or systems, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of Diodes Incorporated products in such safety-critical, life support devices or systems, notwithstanding any devices- or systems-related information or support that may be provided by Diodes Incorporated. Further, Customers must fully indemnify Diodes Incorporated and its representatives against any damages arising out of the use of Diodes Incorporated products in such safety-critical, life support devices or systems.

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