PGA900 Pressure and Temperature Sensor Signal Conditioner

1 Features

- Analog Features
  - Analog Front-End for Resistive Bridge Sensors
  - On-Chip Temperature Sensor
  - Programmable Gain
  - 24-Bit Sigma-Delta Analog-to-Digital Converter for Signal Channel and Temperature Channel
  - 14-Bit Output DAC
- Digital Features
  - Microcontroller Core
    - ARM® Cortex®-M0 at 1 MHz
    - On-Chip Oscillator
  - Memory
    - 8 KB OTP Memory
      - 8 KB of Development RAM for Software Development
    - 128 Bytes EEPROM
    - 1 KB Data SRAM
- Peripheral Features
  - Serial Peripheral Interface (SPI)
  - Inter-Integrated Circuit (I^2C)
  - One-Wire Interface (OWI)
  - 4- to 20-mA Current Loop Interface
  - Ratiometric and Absolute Voltage Output
  - PWM Output
  - Power Management Control
  - Analog Low-Voltage Detect
- General Features
  - Industrial Temperature Range: –40°C to 150°C
  - Power Supply:
    - Depletion MOSFET Gate Controller
    - Absolute Maximum: –28 to 33 V
    - Operational: 3.3 to 30 V
  - WCSP-36 and QFN-36 Package Options

2 Applications

- Resistive Bridge Sensor Signal Conditioning
- Thermocouple, Thermistor, and 2-Wire RTD Sensor Signal Conditioning

3 Description

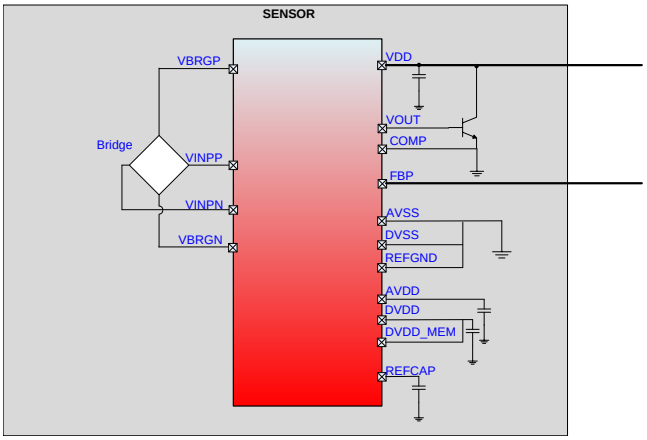
The PGA900 is an interface device for piezoresistive and strain gauge pressure sense elements, and thermocouple, thermistor, and 2-wire RTD temperature sensor elements. The device incorporates analog front end that directly connects to the sensing element and has voltage regulators and an oscillator. The device also includes two sigma-delta analog-to-digital converters, an ARM® Cortex®-M0 microprocessor and OTP memory. Sensor compensation algorithms can be implemented in software. The PGA900 includes multiple output interfaces including absolute voltage, ratiometric voltage, and 4- to 20-mA current output.

Device Information(1)

ORDER NUMBER	PACKAGE	BODY SIZE (NOM)
PGA900ARHHR	VQFN (36)	6.00 mm x 6.00 mm
PGA900AYZSR	DSBGA (36)	3.66 mm x 3.66 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Bridge Sensor Connections to PGA900 Configured in Current Mode



PRODUCT PREVIEW

4 Device and Documentation Support

4.1 Trademarks

ARM, Cortex are registered trademarks of ARM Ltd.
All other trademarks are the property of their respective owners.

4.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

4.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

5 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PRODUCT PREVIEW

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PGA900ARHHR	PREVIEW	VQFN	RHH	36	60	TBD	Call TI	Call TI	-40 to 150	PGA900A RHH	
PGA900AYZSR	PREVIEW	DSBGA	YZS	36	2500	TBD	Call TI	Call TI	-40 to 150		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

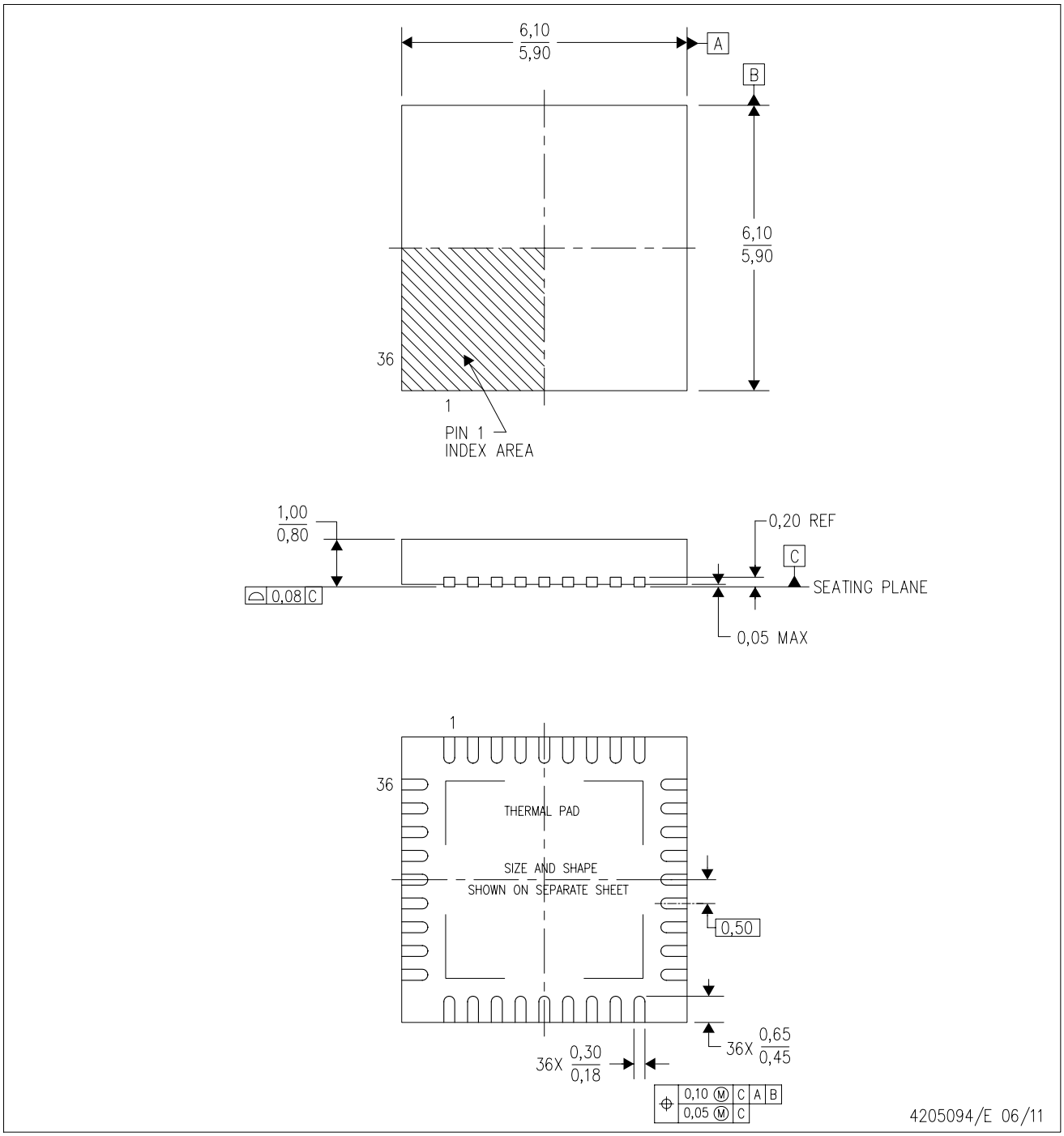
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

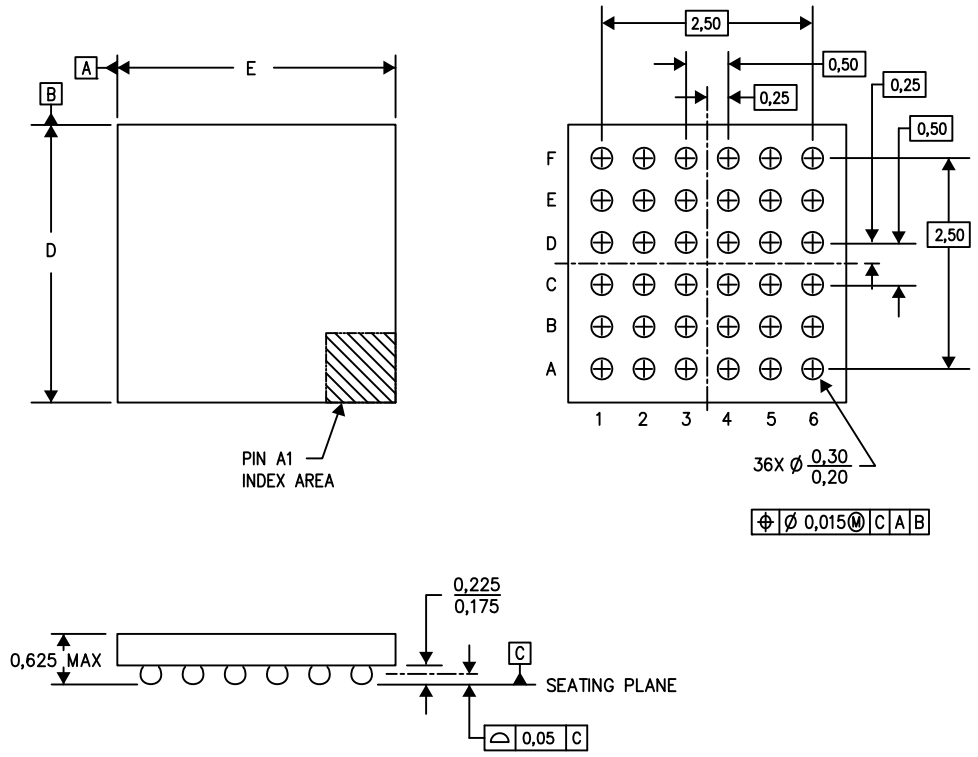
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

RHH (S–PVQFN–N36) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

YZS (S–XBGA–N36) DIE–SIZE BALL GRID ARRAY



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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