

# PFS1200-12-054xD Series

## DC-DC Front End Power Supply

The PFS1200-12-054xD Series is a 1200 watt DC to DC power supply that converts DC input into a main output of 12 VDC for powering intermediate bus architectures (IBA) in high performance and reliability servers, routers, and network switches.

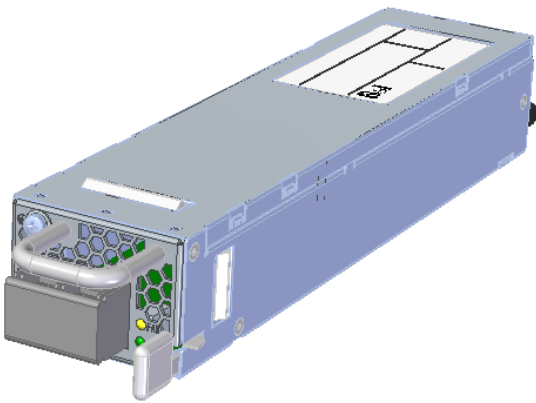
The PFS1200 Series meets international safety standards and displays the CE-Mark for the European Low Voltage Directive (LVD).

### Key Features & Benefits

- High Efficiency, typ. 94% efficiency at half load
- Wide input voltage range: -40 to -72 VDC
- Always-On 12 V standby output (Option for 3.3 / 5 Vsb available)
- Hot-plug capable
- Parallel operation with active digital current sharing
- Small form factor (WxHxL): 54.5 x 40.0 x 228 mm (2.15 x 1.57 x 8.98 in)
- I2C communication interface for control, programming and monitoring with Power Management Bus protocol and PSMI Protocol
- overvoltage and overcurrent protection
- 256 Bytes of EEPROM for user information
- 2 Status LEDs: OK and FAIL with fault signaling

### Applications

- High Performance Servers
- Routers
- Switches



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## 1. ORDERING INFORMATION

PFS	1200	-	12	-	054	X	D	X
Product Family	Power Level	Dash	V1 Output	Dash	Width	Airflow <sup>1</sup>	Input	Options
PFS Front-Ends	1200 W		12 V		54 mm	N: Normal R: Reverse	D: DC Input	B: 3.3/5 Vsb <sup>2</sup>

- <sup>1</sup> N = Normal Airflow from Output connector to Input AC socket  
R = Reverse Airflow from Input AC socket to Output connector
- <sup>2</sup> B = Standby voltage of 3.3/5 Vsb (programmable). Consult factor for availability.

## 2. OVERVIEW

The PFS1200 Series DC/DC power supply is a DSP controlled, highly efficient front-end power supply. It incorporates state of the art technology and uses an interleaved forward converter topology with active clamp and synchronous rectification to reduce component stresses, thus providing increased system reliability and very high efficiency. With a wide input DC voltage range the PFS1200 Series maximizes power availability in demanding server, network, and other high availability applications. The supply is fan cooled and ideally suited for integration with a matching airflow path.

An active OR-ing device on the output ensures no reverse load current and renders the supply ideally suited for operation in redundant power systems.

The always-on standby output provides power to external power distribution and management controllers. It is protected with an active OR-ing device for maximum reliability.

Status information is provided with a front-panel LED. In addition, the power supply can be controlled and the fan speed set via the I2C bus. The I2C bus allows full monitoring of the supply, including input and output voltage, current, power, and inside temperatures. Cooling is managed by a fan controlled by the DSP controller. The fan speed is adjusted automatically depending on the actual power demand and supply temperature and can be overridden through the I2C bus.

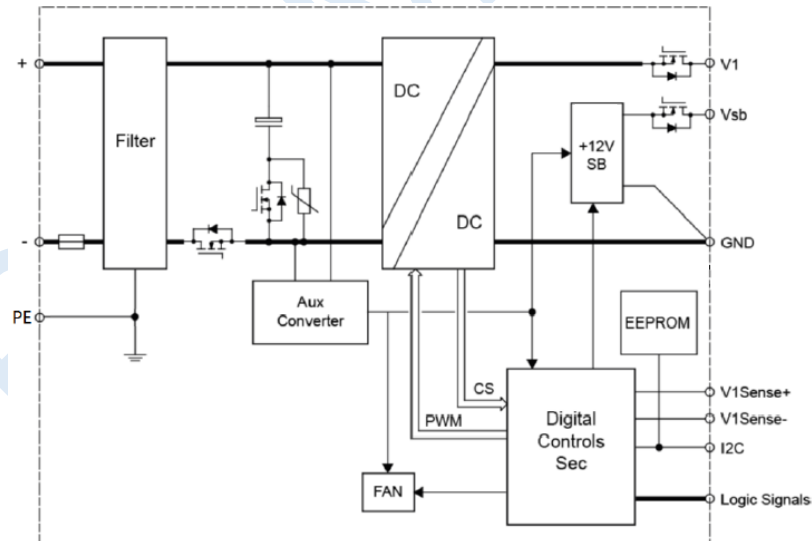


Figure 1. Block Diagram

### 3. ABSOLUTE MAXIMUM RATINGS

Stresses in excess of the absolute maximum ratings may cause performance degradation, adversely affect long-term reliability, and cause permanent damage to the supply.

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_{i\ maxc}$	Maximum Input Voltage			-75	VDC

### 4. INPUT SPECIFICATIONS

General Condition:  $T_A = 0 \dots 45^\circ\text{C}$  unless otherwise specified.

PARAMETER	CONDITIONS / DESCRIPTION	MIN	NOM	MAX	UNIT
$V_{nom}$	Nominal input voltage	-48		-60	VDC
$V_i$	Input voltage ranges	Normal operating ( $V_{i\ min}$ to $V_{i\ max}$ )		-72	VDC
$I_{max}$	Max input current	$V_i > V_{i\ min}$		36	$A_{rms}$
$I_p$	Inrush Current Limitation	$V_{i\ min}$ to $V_{i\ max}$ , $T_A = 25^\circ\text{C}$ , cold start		50	$A_p$
$V_{i\ VSB\_on}$	Turn-on standby input voltage	Ramping up		-32	VDC
$V_{i\ VSB\_off}$	Turn-off standby input voltage	Ramping down		-30	VDC
$V_{i\ V1\_on}$	Turn-on V1 input voltage	Ramping up		-40	VDC
$V_{i\ V1\_off}$	Turn-off V1 input voltage	Ramping down		-39	VDC
$T_{V1\_holdup}$	Hold-up Time V1	$V_i > 10.8\text{ V}$ , $V_{SB}$ within regulation, $V_i = -48\text{ VDC}$ , $P_{D\ nom}$ (from DC input lost to V1 lost to 10.8V)		1	ms
$T_{VSB\_holdup}$	Hold-up time Vsb	Vsb full load		5	ms

#### 4.1 INPUT FUSE

A fast-acting 40 A input fuse in the negative voltage path inside the power supply protect against severe defects. The fuse is not accessible from the outside and are therefore not serviceable parts.

#### 4.2 INRUSH CURRENT

Internal bulk capacitors will be charged through resistors connected from bulk cap minus pin to the DC rail minus, thus limiting the inrush current. After the inrush phase, NTC resistors are then shorted with MOSFETs connected in parallel. The Inrush control is managed by the digital controller (DSP).

#### 4.3 INPUT UNDER-VOLTAGE

If the input voltage stays below the input under voltage lockout threshold  $V_{i\ on}$ , the supply will be inhibited. Once the input voltage returns within the normal operating range, the supply will return to normal operation again.

#### 4.4 EFFICIENCY

The topologies minimizing switching losses and a full digital control scheme. Synchronous rectifiers on the output reduce the losses in the high current output path. The speed of the fan is digitally controlled to keep all components at an optimal operating temperature regardless of the ambient temperature and load conditions.

## 4.5 DC LINE TRANSIENT TEST

### MINUS 72 VDC LINE TRANSIENT TEST

A standard line voltage momentary transient test is shown below. This test simulates a momentary voltage overshoot. This should not affect the operation of the PSU, the output voltage should remain in regulation. This test shall be conducted every 10 sec for 30 min (180 times total).

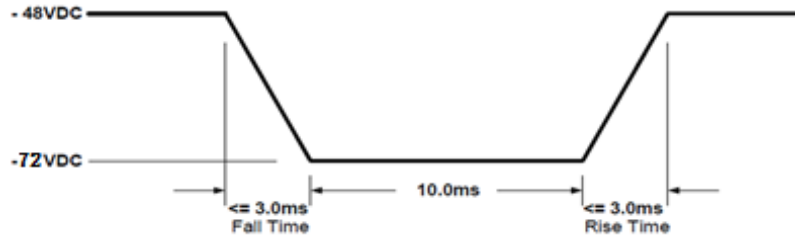


Figure 2. Minus 72 VDC Line Transient Test

### 0 V LINE TRANSIENT TEST

A standard line voltage momentary blackout test is shown below. This test simulates a momentary switch throw off-on, see graph below. The power supply should restart, not latch. This test shall be conducted 3 times in 10 min intervals. Practically a blackout of any duration should not damage the power supply in any way and not cause a latch off condition.

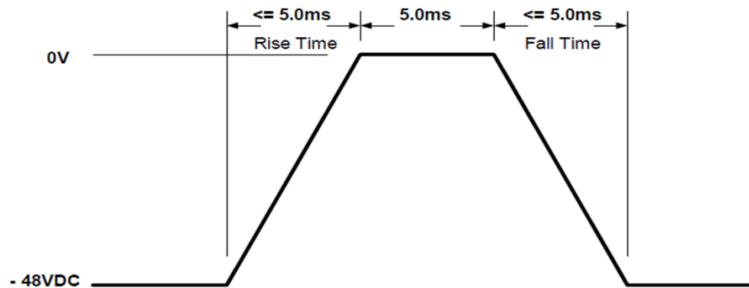


Figure 3. 0 V Line Transient Test



12 V <sub>SB</sub> Standby Output					
V <sub>SB nom</sub>	Nominal Output Voltage		12		VDC
V <sub>SB set</sub>	Output Setpoint Accuracy	0.5 · I <sub>SB nom</sub> , T <sub>amb</sub> = 25 °C	-1	+1	% V <sub>I nom</sub>
dV <sub>SB tot</sub>	Total Regulation	V <sub>I min</sub> to V <sub>I max</sub> , 0 to 100% I <sub>SB nom</sub> , T <sub>a min</sub> to T <sub>a max</sub>	-3	+3	% V <sub>SB nom</sub>
P <sub>SB nom</sub>	Nominal Output Power		36		W
I <sub>SB nom</sub>	Nominal Output Current		3		A
V <sub>SB pp</sub>	Output Ripple Voltage	V <sub>SB nom</sub> , I <sub>SB nom</sub> , 20 MHz BW, (See Section 5.1)	60	120	mVpp
dV <sub>SB</sub>	Drop	0 - 100 % I <sub>SB nom</sub>	250		mV
dV <sub>SB dyn</sub>	Dynamic Load Regulation	ΔI <sub>SB</sub> = 50% I <sub>SB nom</sub> , I <sub>SB</sub> = 5 ... 100% I <sub>SB nom</sub> , dI/dt = 0.5 A/μs, recovery within 1% of V <sub>I nom</sub>	-5	+5	% V <sub>SB nom</sub>
T <sub>rec</sub>	Recovery Time		2		ms
T <sub>DC VSB</sub>	Start-Up Time from DC Input	V <sub>SB</sub> = 90% V <sub>SB nom</sub>		2	sec
t <sub>VSB rise</sub>	Rise Time	V <sub>SB</sub> = 10...90% V <sub>SB nom</sub>	4	20	ms
C <sub>Load</sub>	Capacitive Loading	T <sub>amb</sub> = 25 °C		1500	μF

### 5.1 RIPPLE / NOISE

Internal capacitance at the 12 V output (behind the OR-ing circuitry) is minimized to prevent disturbances during hot plug. In order to provide low output ripple voltage in the application, external capacitors (a parallel combination of 10 μF tantalum capacitor in parallel with 0.1 μF ceramic capacitors) should be added close to the power supply output. The setup of Error! Reference source not found. has been used to evaluate suitable capacitor types. The capacitor combinations of Error! Reference source not found. and Error! Reference source not found. should be used to reduce the output ripple voltage. The ripple voltage is measured with 20 MHz BWL, close to the external capacitors.

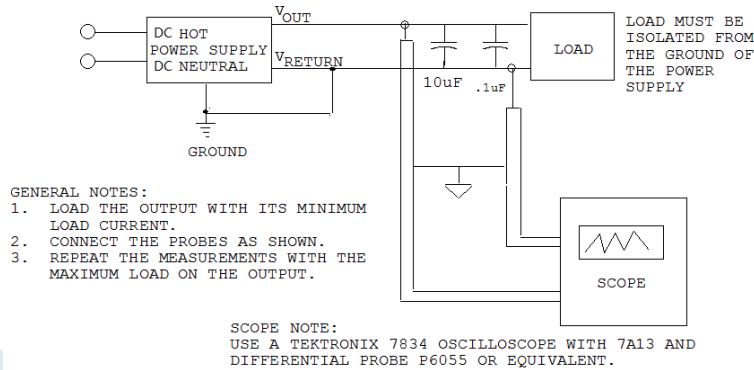


Figure 4. Output ripple test setup

**NOTE:** Care must be taken when using ceramic capacitors with a total capacitance of 1 μF to 50 μF on output V1, due to their high-quality factor the output ripple voltage may be increased in certain frequency ranges due to resonance effects.

EXTERNAL CAPACITOR V1	DV1MAX	UNIT
Standard test condition:		
1 Pc 10 μF / 63 V Electrolytic Capacitor	150	mVpp
1 pc 0.1 uF / 100 V ceramic capacitor		
1Pcs 1000μF/16V/Low ESR Aluminum/ø10x20	120	mVpp
2Pcs 47μF/16V/X5R/1210 plus		
1Pcs 1000μF Low ESR AICap	90	mVpp

Table 1. Suitable capacitors for V1

EXTERNAL CAPACITOR VSB	DV1MAX	UNIT
Standard test condition:		
1 pc 10 μF / 63 V Electrolytic Capacitor	100	mVpp
1 pc 0.1 uF / 100 V ceramic capacitor		
Add 1 pc 10μF/16 V/X5R/1206	50	mVpp
Add 2 pcs 10μF/1V/X5R/1206	40	mVpp

Table 2. Suitable capacitors for 3.3V<sub>SB</sub> and 5V<sub>SB</sub>

The output ripple voltage on V<sub>SB</sub> is influenced by the main output V<sub>1</sub>. Evaluating V<sub>SB</sub> output ripple must be done when maximum load is applied to V<sub>1</sub>.

## 6. PROTECTION SPECIFICATIONS

General Condition:  $T_a = 0 \dots 45^\circ\text{C}$  unless otherwise specified.

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT	
$F$	Input Fuse (L)	Not user accessible		40	A	
$V_{1\text{OV}}$	OV Threshold $V_1$	13.0		14.5	VDC	
$t_{\text{OV}V1}$	OV Latch Off Time $V_1$	V1 with half load		1	ms	
$V_{\text{SB}OV}$	OV Threshold $V_{\text{SB}}$	110		120	% $V_{\text{SB}}$	
$t_{\text{OV}V\text{SB}}$	OV Latch Off Time $V_{\text{SB}}$	Vsb with half load		1	ms	
$I_{1\text{lim}}$	Over Current Limitation $V_1$	$T_a < 45^\circ\text{C}$		105	A	
$I_{\text{VSB}lim}$	Over Current Limitation $V_{\text{SB}}$	$T_a < 45^\circ\text{C}$ for		12 $V_{\text{SB}}$	3.3	3.6
				5.0 $V_{\text{SB}}$	3.45	4.5
				3.3 $V_{\text{SB}}$	5.25	6.2
$t_{1\text{SC}}$	Short Circuit Regulation Time	$V_1 < 3\text{V}$ , time until $I_{1\text{SC}}$ is limited to $< I_{1\text{SC}}$			2	ms
$T_{\text{SD}}$	Over Temperature on Heat Sinks	Automatic shut-down		115	$^\circ\text{C}$	

### 6.1 OVERVOLTAGE PROTECTION

The PFS front-ends provide a fixed threshold overvoltage (OV) protection implemented with a HW comparator. Once an OV condition has been triggered, the supply will shut down and latch the fault condition. The latch can be unlocked by disconnecting the supply from the DC mains or by toggling the PSON\_L input.

### 6.2 VSB UNDERVOLTAGE DETECTION

Both main and standby outputs are monitored.

#### 12 $V_{\text{SB}}$

LED and PWOK\_L pin signal if the output voltage exceeds  $\pm 7\%$  of its nominal voltage. Output under voltage protection is provided on both outputs. When either V1 or VSB falls below 93% of its nominal voltage, the output is inhibited.

#### 3.3 / 5 $V_{\text{SB}}$

LED and PWOK\_H pin signal if the output voltage exceeds  $\pm 5\%$  of its nominal voltage. Output under voltage protection is provided on the standby output only. When VSB falls below 75% of its nominal voltage, the main output V1 is inhibited.

### 6.3 CURRENT LIMITATION

#### 6.3.1 MAIN OUTPUT

When main output runs in current limitation mode its output will turn OFF below 2 V but will retry to recover every 1 s interval. If current limitation mode is still present after the unit retry, output will continuously perform this routine until current is below the current limitation point. The supply will go through soft start every time it retries from current limitation mode.

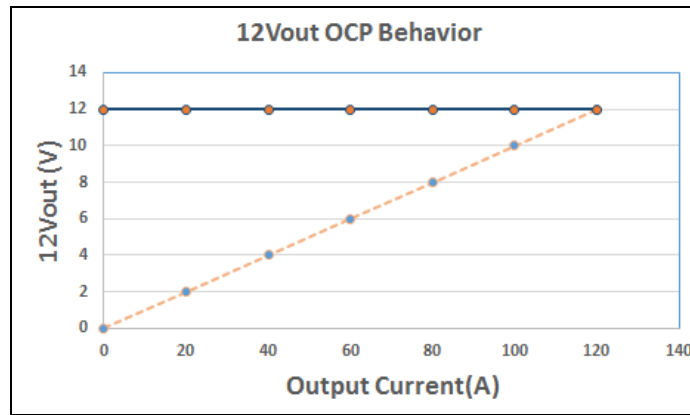


Figure 5. Current Limitation on V1

The main output current limitation will decrease if the ambient (inlet) temperature increases beyond 45°C.

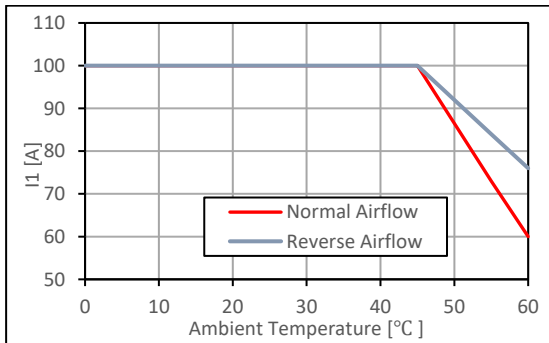


Figure 6. Iout Derating Curve for ambient above 45°C

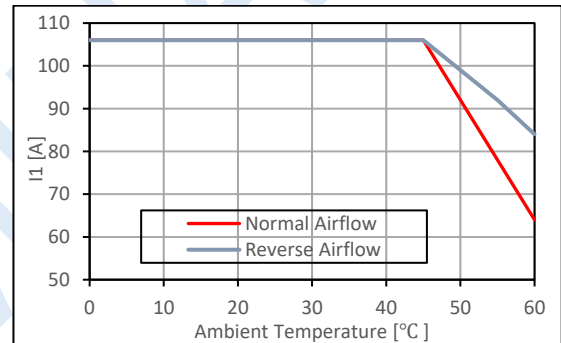


Figure 7. OCP Derating Curve with Ambient Temperature

### 6.3.2 STANDBY OUTPUT

#### 3.3 / 5 V<sub>SB</sub>

The standby output exhibits a substantially rectangular output characteristic down to 0 V (no hiccup mode / latch off). If it runs in current limitation and its output voltage drops below the UV threshold, then the main output will be inhibited (standby remains on). The current limitation of the standby output is independent of the DC input voltage.

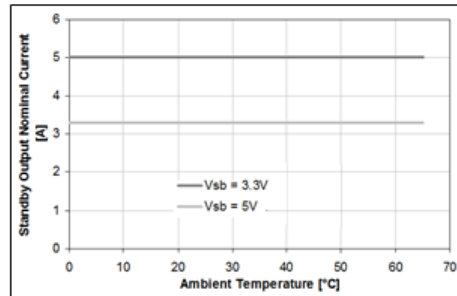
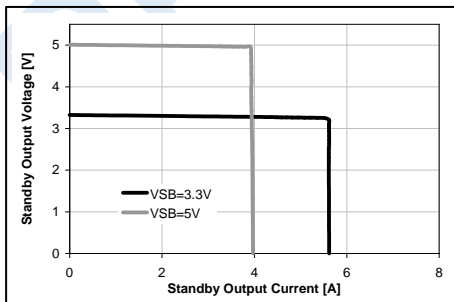


Figure 8. Current Limitation and Temperature Derating on 3.3 / 5 V<sub>SB</sub>

**12 V<sub>SB</sub>**

On the standby output, a hiccup type over current protection is implemented. This protection will shut down the standby output immediately when standby current reaches or exceeds  $I_{SB\ lim}$ . After an off-time of 1s the output automatically tries to restart. If the overload condition is removed the output voltage will reach again its nominal value. At continuous overload condition the output will repeatedly trying to restart with 1s intervals. A failure on the Standby output will shut down both Main and Standby outputs.

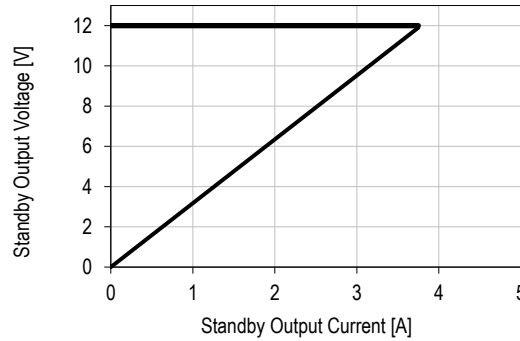


Figure 9. Current Limitation on 12 V<sub>SB</sub>

**7. MONITORING**

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_{i\ mon}$	Input Voltage $V_{i\ min} \leq V_i \leq V_{i\ max}$	-2		+2	VDC
$I_{i\ mon}$	Input Current	-1		+1	A
$P_{i\ mon}$	True Input Power $I_1 > 25\ A$ $I_1 \leq 25\ A$	-4 25		+4 25	% W
$V_{i\ mon}$	V <sub>1</sub> Voltage	-2		+2	%
$I_{i\ mon}$	V <sub>1</sub> Current $I_1 > 25\ A$ $I_1 \leq 25\ A$	-2 -1.5		+2 +1.5	% A
$P_{o\ nom}$	Total Output Power $P_o > 120\ W$ $P_o \leq 120\ W$	-5 -15		+5 +15	% W
$V_{SB\ mon}$	Standby Voltage	-0.3		+0.3	V
$I_{SB\ mon}$	Standby Current $I_{SB} \leq I_{SB\ nom}$	-0.5		+0.5	A

## 8. SIGNAL & CONTROL SPECIFICATIONS

### 8.1 ELECTRICAL CHARACTERISTICS

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
<b><i>PSKILL_H / PSON_L / VSB_SEL / HOTSTANDBYEN_H Inputs</i></b>					
$V_L$	Input Low Level Voltage	-0.2		0.8	V
$V_H$	Input High Level Voltage	2.4		3.5	V
$I_{L,H}$	Maximum Input Sink or Source Current	0		1	mA
$R_{puPSKILL\_H}$	Internal Pull Up Resistor on PSKILL_H		100		k $\Omega$
$R_{puPSON\_L}$	Internal Pull Up Resistor on PSON_L		10		k $\Omega$
$R_{puHOTSTANDBYEN\_H}$	Internal Pull Up Resistor on HOTSTANDBYEN_H		10		k $\Omega$
$R_{LOW}$	Resistance Pin to SGND for Low Level	0		1	k $\Omega$
$R_{HIGH}$	Resistance Pin to SGND for High Level	50			k $\Omega$
<b><i>PWOK_H Output</i></b>					
$V_{OL}$	Output Low Level Voltage			0.4	V
		$I_{sink} < 4 \text{ mA}$			
$V_{OH}$	Output High Level Voltage	2.6		3.5	V
		$I_{source} < 0.5 \text{ mA}$			
$R_{puPWOK\_H}$	Internal Pull Up Resistor on PWOK_H		1		k $\Omega$
<b><i>VINOK_H Output</i></b>					
$V_{OL}$	Output Low Level Voltage			0.4	V
		$I_{sink} < 2 \text{ mA}$			
$V_{OH}$	Output High Level Voltage	2.6		3.5	V
		$I_{source} < 50 \mu\text{A}$			
$R_{puVINOK\_H}$	Internal Pull Up Resistor on VINOK_H		10		k $\Omega$
<b><i>SMB_ALERT_L Output</i></b>					
$V_{ext}$	Maximum External Pull Up Voltage			12	V
$V_{OL}$	Output Low Level Voltage			0.4	V
		$I_{source} < 4 \text{ mA}$			
$I_{OH}$	Maximum High Level Leakage Current			10	$\mu\text{A}$
$R_{puSMB\_ALERT\_L}$	Internal Pull Up Resistor on SMB_ALERT_L		None		k $\Omega$

### 8.2 INTERFACING WITH SIGNALS

All signal pins have protection diodes implemented to protect internal circuits. When the power supply is not powered, the protection devices start clamping at signal pin voltages exceeding  $\pm 0.5 \text{ V}$ . Therefore all input signals should be driven only by an open collector/drain to prevent back feeding inputs when the power supply is switched off. If interconnecting of signal pins of several power supplies is required, then this should be done by decoupling with small signal schottky diodes, except for SMB\_ALERT\_L, ISHARE and I<sup>2</sup>C pins. SMB\_ALERT\_L pins can be interconnected without decoupling diodes, since these pins have no internal pull up resistor and use a 15 V zener diode as protection device against positive voltage on pins. ISHARE pins must be interconnected without any additional components. This in-/output is disconnected from internal circuits when the power supply is switched off.

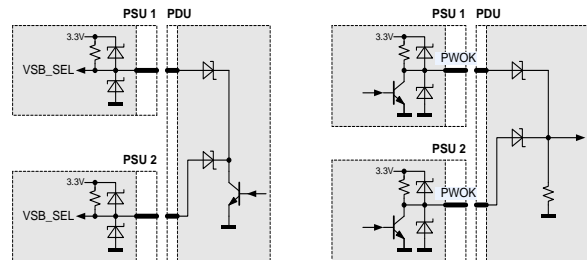


Figure 10. Interconnection of Signal Pins

### 8.3 FRONT LEDS

There will be 2 separate LED indicators, one green and one amber to indicate the power supply status. There will be a (slow) blinking green POWER LED (OK) to indicate that DC is applied to the PSU and the Standby Voltage is available. This same LED shall go steady to indicate that all the Power Outputs are available. This same LED or separate one will blink (slow) or be solid ON amber to indicate that the power supply has failed or reached a warning status and therefore a replacement of the unit is/maybe necessary. The LED are visible on the power supply's exterior face. The LED location meets ESD Requirements.

POWER SUPPLY CONDITION	GREEN (OK) LED STATUS	AMBER (FAIL) LED STATUS
No DC power to all power supplies	OFF	OFF
Power Supply Failure (includes over voltage, over current, over temperature and fan failure)	OFF	ON
Power Supply Warning events where the power supply continues to operate (high temperature, high power and slow fan)	OFF	Blinking
DC Present / V <sub>SB</sub> on (PSU OFF)	Blinking	OFF
Power Supply ON and OK	ON	OFF

Table 3. LED Status

### 8.4 PRESENT\_L

This signaling pin is recessed within the connector and will contact only once all other connector contacts are closed. This active-low pin is used to indicate to a power distribution unit controller that a supply is plugged in. The maximum current on PRESENT\_L pin should not exceed 10 mA.

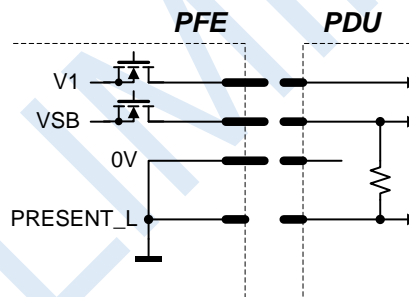


Figure 11. PRESENT\_L signal pin

### 8.5 PSKILL\_H INPUT

The PSKILL\_H input is active-high and is located on a recessed pin on the connector and is used to disconnect the main output as soon as the power supply is being plugged out. This pin should be connected to SGND in the power distribution unit. The standby output will remain on regardless of the PSKILL\_H input state.

## 8.6 VINOK\_H

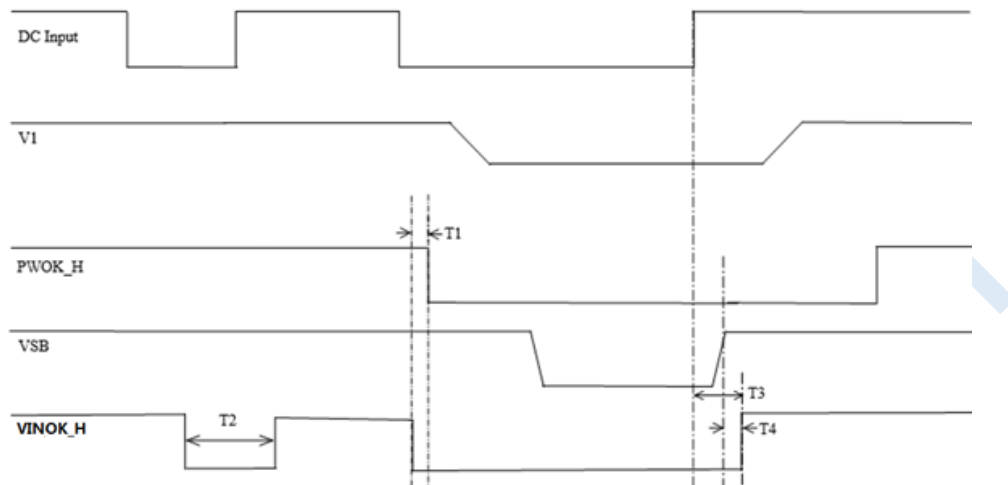


Figure 12. VINOK\_H Timing

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
T1	VIN_OK_H & PWOK_H	0.5			ms
T2	VIN_OK_H Dwell Time	75		120	ms
T3	VIN_OK_H delay to DC			1700	ms
T4	VIN_OK_H to VSB			20	ms

Table 4. VINOK\_H Timing Requirement

### 8.7 TIMING REQUIREMENTS

These are the timing requirements for the power supply operation. The output voltages must rise from 10% to within regulation limits ( $T_{vout\_rise}$ ) within 1 to 70 ms. All outputs must rise monotonically. The Table below shows the timing requirements for the power supply being turned on and off two ways; 1) via the DC input with PSON\_L held low; 2) via the PSON\_L signal with the DC input applied. The PSU needs to remain off for 1 second minimum after PWOK\_H is de-asserted.

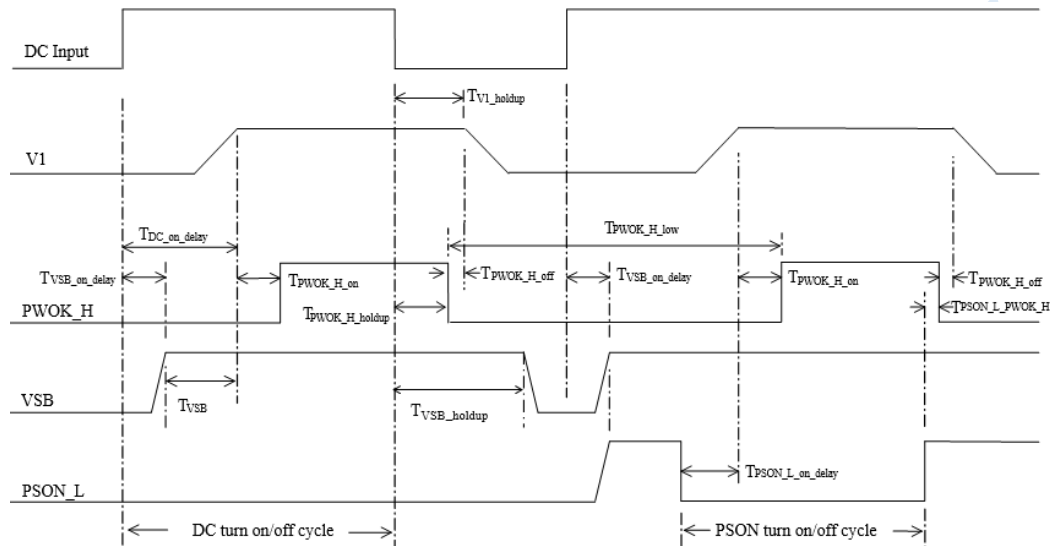


Figure 13. Timing Requirement

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$T_{V1\_rise}$	Output voltage rise time	1.0		70	ms
$T_{VSB\_on\_delay}$	Delay from DC being applied to VSB being within regulation.			1500	ms
$T_{DC\_on\_delay}$	Delay from DC being applied to all output voltages being within regulation.			3000	ms
$T_{V1\_holdup}$	Time 12 V output voltage stay within regulation after loss of DC.	2			ms
$T_{PWOK\_H\_holdup}$	Delay from loss of DC to de-assertion of PWOK_H	1			ms
$T_{PSON\_L\_on\_delay}$	Delay from PSON_L active to output voltages within regulation limits.	5		400	ms
$T_{PSON\_L\_PWOK\_H}$	Delay from PSON_L deactivate to PWOK_H being de-asserted.			5	ms
$T_{PWOK\_H\_on}$	Delay from output voltages within regulation limits to PWOK_H asserted at turn on.	100		500	ms
$T_{PWOK\_H\_off}$	Delay from PWOK_H de-asserted to output voltages dropping out of regulation limits.	0.5			ms
$T_{PWOK\_H\_low}$	Duration of PWOK_H being in the de-asserted state during an off/on cycle using PSON_L signal.	100			ms
$T_{VSB}$	Delay from VSB being in regulation to O/Ps being in regulation at DC turn on.	50		1000	ms
$T_{VSB\_holdup}$	Time the VSB output voltage stays within regulation after loss of DC.	5			ms
$T_{DC\_off\_SMB\_ALERT\_L}$	The power supply shall assert the SMB_ALERT_L signal quickly after a loss of DC input voltage.			2	ms

## 8.8 CURRENT SHARE

The PFS front-ends have an active current share scheme implemented for  $V_1$ . All the ISHARE current share pins need to be interconnected in order to activate the sharing function. If a supply has an internal fault or is not turned on, it will disconnect its ISHARE pin from the share bus. This will prevent dragging the output down (or up) in such cases.

The current share function uses a digital bi-directional data exchange on a recessive bus configuration to transmit and receive current share information. The controller implements a Master/Slave current share function. The power supply providing the largest current among the group is automatically the Master. The other supplies will operate as Slaves and increase their output current to a value close to the Master by slightly increasing their output voltage. The voltage increase is limited to +250 mV. The standby output uses a passive current share method (droop output voltage characteristic).

## 8.9 SENSE INPUTS

The main output has sense lines implemented to compensate for voltage drop on load wires. The maximum allowed voltage drop is 200 mV on the positive rail and 50 mV on the PGND rail.

With open sense inputs the main output voltage will rise by 250 mV. Therefore, if not used, these inputs should be connected to the power output and PGND close to the power supply connector. The sense inputs are protected against short circuit. In this case the power supply will shut down.

## 8.10 HOT-STANDBY OPERATION

The hot-standby operation is an operating mode allowing to further increase efficiency at light load conditions in a redundant power supply system. Under specific conditions one of the power supplies is allowed to disable its Oring gate. This will save the power losses associated with this power supply and at the same time the other power supply will operate in a load range having a better efficiency. In order to enable the hot standby operation, the HOTSTANDBYEN\_H and the ISHARE pins need to be interconnected. A power supply will only be allowed to enter the hot-standby mode, when the HOTSTANDBYEN\_H pin is high, the load current is low and the supply was allowed to enter the hot-standby mode by the system controller via the appropriate I<sup>2</sup>C command (by default disabled). The system controller needs to ensure that only one of the power supplies is allowed to enter the hot-standby mode.

If a power supply is in a fault condition, it will pull low its active-high HOTSTANDBYEN\_H pin which indicates to the other power supply that it is not allowed to enter the hot-standby mode or that it needs to return to normal operation should it already have been in the hot-standby mode.

**NOTE:** The system controller needs to ensure that only one of the power supplies is allowed to enter the hot-standby model.

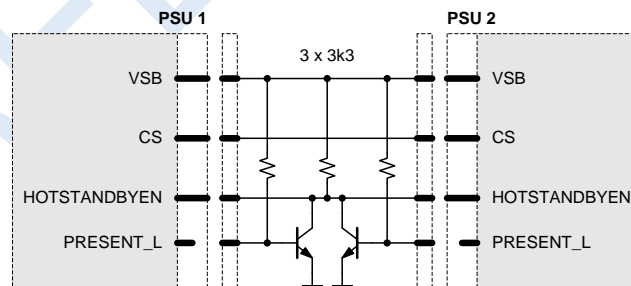


Figure 14. Recommended hot-standby configuration

In order to prevent voltage dips when the active power supply is unplugged while the other is in hot-standby mode, it is strongly recommended to add the external circuit as shown in *Figure*. If the PRESENT\_L pin status needs also to be read by the system controller, it is recommended to exchange the bipolar transistors with small signal MOS transistors or with digital transistors.

### 8.11 PSON\_L INPUT

The PSON\_L is an internally pulled-up (3.3 V) input signal to enable/disable the main output V1 of the front-end. With low level input the main output is enabled. This active-low pin is also used to clear any latched fault condition. The PSON\_L can be either controlled by an open collector device or by a voltage source.

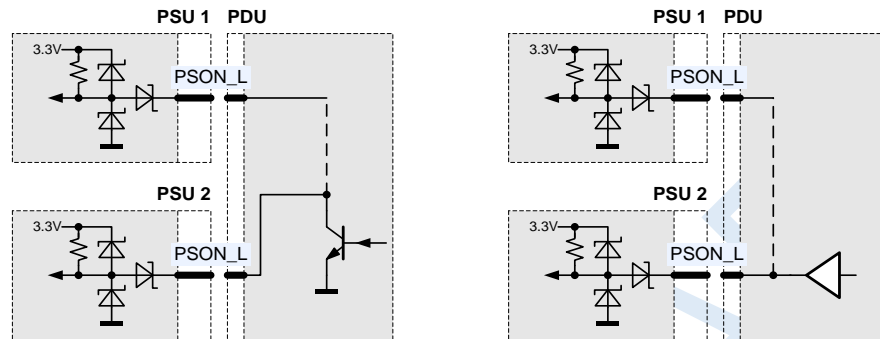


Figure 15. PSON\_L connection

### 8.12 I2C / SMBUS COMMUNICATION

The interface driver in the PFS supply is referenced to the V1 Return. The PFS supply is a communication Slave device only; it never initiates messages on the I2C/SMBus by itself. The communication bus voltage and timing is defined in Table 5 further characterized through:

- There are no internal pull-up resistors
- The SDA/SCL IOs are 3.3/5 V tolerant
- Full SMBus clock speed of 100 kbps
- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognizes any time Start/Stop bus conditions

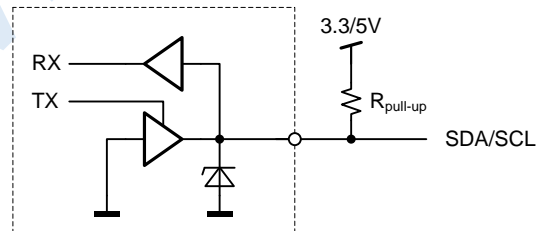


Figure 16. Physical layer of communication interface

The SMB\_ALERT\_L signal indicates that the power supply is experiencing a problem that the system agent should investigate. This is a logical OR of the Shutdown and Warning events. The power supply responds to a read command on the general SMB\_ALERT\_L call address 25(0x19) by sending its status register.

Communication to the DSP or the EEPROM will be possible as long as the input DC voltage is provided. If no DC is present, communication to the unit is possible as long as it is connected to a life V1 output (provided e.g. by the redundant unit). If only VSB is provided, communication is not possible.

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_{IL}$	Input low voltage	-0.5		1.0	V
$V_{IH}$	Input high voltage	2.3		5.5	V
$V_{hys}$	Input hysteresis	0.15			V
$V_{oL}$	Output low voltage	3 mA sink current		0.4	V
$t_r$	Rise time for SDA and SCL	$20+0.1Cb^1$		300	Ns
$t_{of}$	Output fall time $V_{IHmin} \rightarrow V_{ILmax}$	$10 \text{ pF} < C_b^2 < 400 \text{ pF}$	$20+0.1Cb^2$	250	Ns
$I_i$	Input current SCL/SDA	$0.1 \text{ VDD} < V_i < 0.9 \text{ VDD}$		10	$\mu\text{A}$
$C_i$	Internal Capacitance for each SCL/SDA			50	pF
$f_{SCL}$	SCL clock frequency	0		100	kHz
$R_{pu}$	External pull-up resistor	$f_{SCL} \leq 100 \text{ kHz}$		1000 ns / $C_b$	$\Omega$
$t_{HDSTA}$	Hold time (repeated) START	$f_{SCL} \leq 100 \text{ kHz}$	4.0		$\mu\text{s}$
$t_{LOW}$	Low period of the SCL clock	$f_{SCL} \leq 100 \text{ kHz}$	4.7		$\mu\text{s}$
$t_{HIGH}$	High period of the SCL clock	$f_{SCL} \leq 100 \text{ kHz}$	4.0		$\mu\text{s}$
$t_{SUSTA}$	Setup time for a repeated START	$f_{SCL} \leq 100 \text{ kHz}$	4.7		$\mu\text{s}$
$t_{HDDAT}$	Data hold time	$f_{SCL} \leq 100 \text{ kHz}$	0	3.45	$\mu\text{s}$
$t_{SUDAT}$	Data setup time	$f_{SCL} \leq 100 \text{ kHz}$	250		ns
$t_{SUSTO}$	Setup time for STOP condition	$f_{SCL} \leq 100 \text{ kHz}$	4.0		$\mu\text{s}$
$t_{BUF}$	Bus free time between STOP and START	$f_{SCL} \leq 100 \text{ kHz}$	5		ms

Table 3. I2C / SMBus Specification

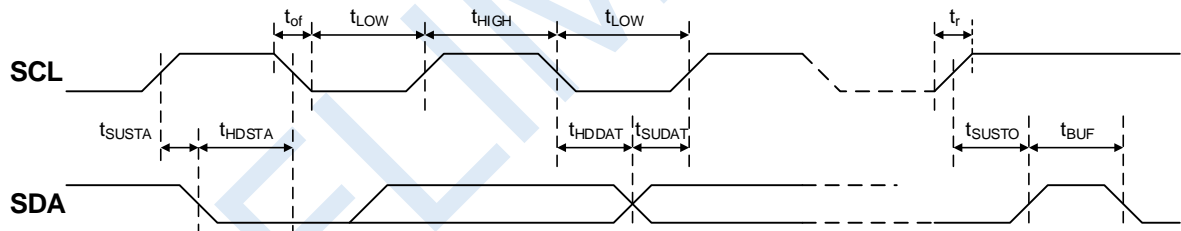


Figure 18. I2C / SMBus Timing

### 8.13 ADDRESS / PROTOCOL SELECTION (APS)

The APS pin provides the possibility to select the address by connecting a resistor to V1 return (0 V). A fixed addressing offset exists between the Controller and the EEPROM.

#### NOTES:

- If the APS pin is left open, the supply will operate with the Power Management Bus protocol at controller / EEPROM addresses 0xB6 / 0xA6.
- The APS pin is only read at start-up of the power supply. Therefore, it is not possible to change address dynamically.

<sup>1</sup>  $C_b$  = Capacitance of bus line in pF, typically in the range of 10...400 pF

R <sub>APS</sub> (Ω) <sup>2</sup>	Protocol	I2C Address <sup>3</sup>	
		Controller	EEPROM
820		0xB0	0xA0
2700	Power	0xB2	0xA2
5600	Management Bus	0xB4	0xA4
8200		0xB6	0xA6

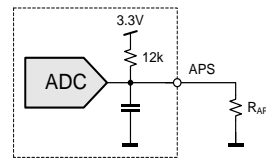


Figure 19. I2C address and protocol setting

### 8.14 CONTROLLER AND EEPROM ACCESS

The controller and the EEPROM in the power supply share the same I2C bus physical layer (see Figure 20). An I2C driver device assures logic level shifting (3.3/5 V) and a glitch-free clock stretching. The driver also pulls the SDA/SCL line to nearly 0 V when driven low by the DSP or the EEPROM providing maximum flexibility when additional external bus repeaters are needed. Such repeaters usually encode the low state with different voltage levels depending on the transmission direction.

The DSP will automatically set the I2C address of the EEPROM with the necessary offset when its own address is changed / set. In order to write to the EEPROM, first the write protection needs to be disabled by sending the appropriate command to the DSP. By default, the write protection is on.

The EEPROM provides 256 bytes of user memory. None of the bytes are used for the operation of the power supply.

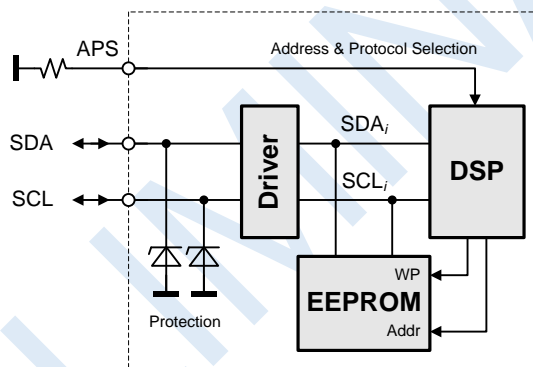


Figure 20. I2C Bus to DPS and EEPROM

### 8.15 EEPROM PROTOCOL

The EEPROM follows the industry communication protocols used for this type of device. Even though page write / read commands are defined, it is recommended to use the single byte write / read commands.

#### WRITE

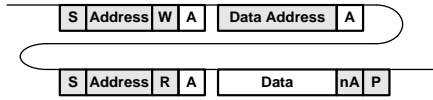
The write command follows the SMBus 1.1 Write Byte protocol. After the device address with the write bit cleared a first byte with the data address to write to is sent followed by the data byte and the STOP condition. A new START condition on the bus should only occur after 5ms of the last STOP condition to allow the EEPROM to write the data into its memory.



<sup>1</sup> E12 resistor values, use max 5% resistors  
<sup>2</sup> The LSB of the address byte is the R/W bit

**READ**

The read command follows the SMBus 1.1 Read Byte protocol. After the device address with the write bit cleared the data address byte is sent followed by a repeated start, the device address and the read bit set. The EEPROM will respond with the data byte at the specified location.



**8.16 POWER MANAGEMENT BUS PROTOCOL**

The Power Management Bus is an open standard protocol that defines means of communicating with power conversion and other devices. For more information, please see the System Management Interface Forum web site at [www.powerSIG.org](http://www.powerSIG.org).

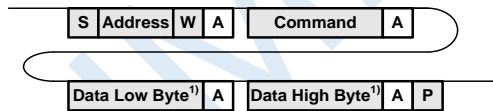
Power Management Bus command codes are not register addresses. They describe a specific command to be executed.

The PFS1200 supply supports the following basic command structures:

- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognized any time Start/Stop bus conditions

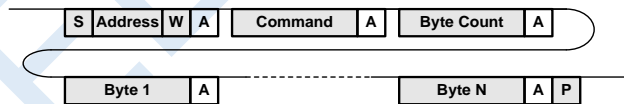
**WRITE**

The write protocol is the SMBus 1.1 Write Byte/Word protocol. Note that the write protocol may end after the command byte or after the first data byte (Byte command) or then after sending 2 data bytes (Word command).



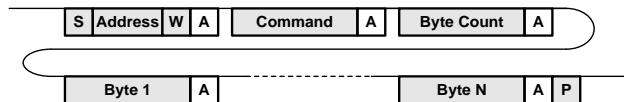
<sup>1)</sup> Optional

In addition, Block write commands are supported with a total maximum length of 255 bytes. See PFS Programming Manual for further information.

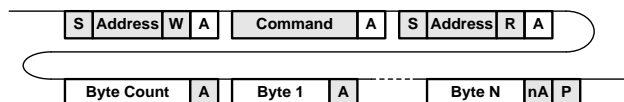


**READ**

The read protocol is the SMBus 1.1 Read Byte/Word protocol. Note that the read protocol may request a single byte or word.



In addition, Block read commands are supported with a total maximum length of 255 bytes. See PFS Programming Manual BCA.00006 for further information.



### 8.17 GRAPHICAL USER INTERFACE

Bel Power Solutions provide with its “Bel Power Solutions I2C Utility” a Windows® XP/Vista/Win7 compatible graphical user interface allowing the programming and monitoring of the PFS1200 Front-End. The utility can be downloaded on: [belfuse.com/power-solutions](http://belfuse.com/power-solutions) and supports Power Management Bus protocols.

The GUI allows automatic discovery of the units connected to the communication bus and will show them in the navigation tree. In the monitoring view the power supply can be controlled and monitored.

If the GUI is used in conjunction with the SNP-OP-BOARD-01 or YTM.G1Q01.0 Evaluation Kit it is also possible to control the PSON\_L pin(s) of the power supply.

Further there is a button to disable the internal fan for approximately 10 seconds. This allows the user to take input power measurements without fan consumptions to check efficiency compliance to the Climate Saver Computing Platinum specification.

The monitoring screen also allows to enable the hot-standby mode on the power supply. The mode status is monitored and by changing the load current it can be monitored when the power supply is being disabled for further energy savings. This obviously requires 2 power supplies being operated as a redundant system (as in the evaluation kit).

**NOTE:** The user of the GUI needs to ensure that only one of the power supplies have the hot-standby mode enabled.

## 9. TEMPERATURE AND FAN CONTROL

To achieve best cooling results sufficient airflow through the supply must be ensured. Do not block or obstruct the airflow at the rear of the supply by placing large objects directly at the output connector. The PFS1200-12NDS412 and PFS1200-12-054ND is provided with normal airflow, which means the air enters through the DC-output of the supply and leaves at the DC input connector. PFS supplies have been designed for horizontal operation.

The fan inside of the supply is controlled by a microprocessor. The RPM of the fan is adjusted to ensure optimal supply cooling and is a function of output power and the inlet temperature.

For the normal airflow version additional constraints apply because of the DC-connector. In a normal airflow unit, the hot air is exiting the power supply unit at the DC-inlet.

**NOTE:** It is the responsibility of the user to check the front temperature in such cases. The unit is not limiting its power automatically to meet such a temperature limitation.

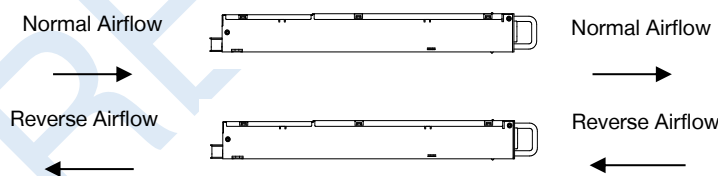


Figure 21. Airflow direction

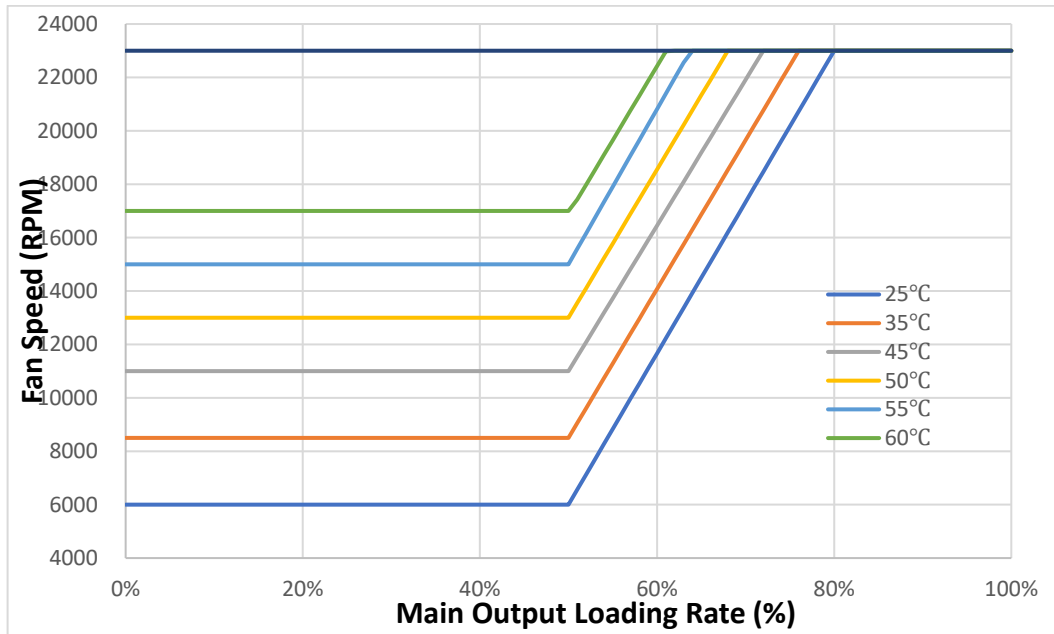


Figure 22. Fan speed vs. main output load

## 10. ELECTROMAGNETIC COMPATIBILITY

### 10.1 IMMUNITY

**NOTE:** Most of the immunity requirements are derived from EN 55024:2010/A1:2015.

TEST	STANDARD / DESCRIPTION	CRITERIA
ESD Contact Discharge	IEC / EN 61000-4-2, ±8 kV, 25+25 discharges per test point (metallic case, LEDs, connector body)	A
ESD Air Discharge	IEC / EN 61000-4-2, ±15 kV, 25+25 discharges per test point (non-metallic user accessible surfaces)	A
Radiated Electromagnetic Field	EN 55024: 2010/A1: 2015 using the IEC 61000-4-3: 2002-09 test standard and performance criteria A defined in Annex B of CISPR 24	A
Burst	IEC / EN 61000-4-4, level 3 Input DC port ±1 kV, 1 minute DC port ±0.5 kV, 1 minute	A
Surge	IEC / EN 61000-4-5 Line to earth: ±1 kV Line to line: ±0.5 kV	A
RF Conducted Immunity	IEC/EN 61000-4-6, Level 3, 10 Vrms, CW, 0.1 ... 80 MHz	A

### 10.2 EMISSION

TEST	STANDARD / DESCRIPTION	CRITERIA
Conducted Emission	EN55032 / CISPR 32: 0.15 ... 30 MHz, QP and AVG, single unit.	Class A
	EN55032 / CISPR 32: 0.15 ... 30 MHz, QP and AVG, 2 units in rack system.	Class A
Radiated Emission	EN55032 / CISPR 32: 30 MHz ... 1 GHz, QP, single unit.	Class A
	EN55032 / CISPR 32: 30 MHz ... 1 GHz, QP, 2 units in rack system.	Class A

## 11. ELECTROMAGNETIC COMPATIBILITY

Maximum electric strength testing is performed in the factory according to IEC/EN 60950/62368, and UL 60950/62368. Input-to-output electric strength tests should not be repeated in the field. Bel Power Solutions will not honor any warranty claims resulting from electric strength field tests.

PARAMETER	DESCRIPTION / CONDITION	NOTE
Agency Approvals	Approved to latest edition of the following standards: UL/ CSA 62368-1 (USA / Canada) EN60950-1/ EN62368-1 (Europe) IEC60950-1/ IEC62368-1 (International) CB Certificate & Report, IEC60950-1/ IEC62368-1 (report to include all country national deviations) CE - Low Voltage Directive 2014/35/EC GB4943.1- CNCA Certification (China)	Pending
Isolation Strength	Input (L/N) to chassis (PE)	Basic
	Input (L/N) to output	Basic
Electrical Strength Test	Output to chassis	None (Direct connection)
	Input to output	1500 VDC
	Input to chassis	1500 VDC

## 12. ENVIRONMENTAL SPECIFICATIONS

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$T_A$	Ambient Temperature	$V_{Imin}$ to $V_{Imax}$ , $I_{Inom}$ , $I_{SBnom}$		+45	°C
$T_{Aext}$	Extended Temp. Range	Derated output	+46	+60	°C
$T_S$	Storage Temperature	Non-operational	-20	+70	°C
	Altitude	Operational, above Sea Level, refer derating to $T_a$	-	10,000	Feet

## 13. MECHANICAL SPECIFICATIONS

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Dimensions	Width		54.5		
	Height		40.0		mm
	Depth		228		

**NOTE:** Tolerance (unless otherwise stated): 0-30 mm: +/- 0.2 mm; 30-120 mm: +/- 0.4 mm; 120-400 mm: +/-0.6 mm

**NOTES:** A 3D step file of the power supply casing is available on request.  
 Unlatching the supply is performed by pulling the green trigger in the handle

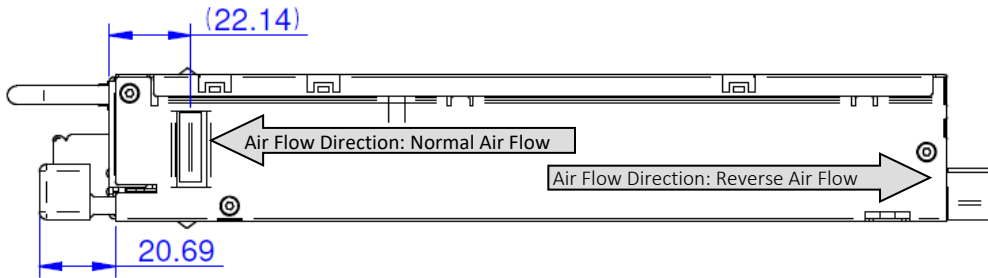


Figure 23. Side View 1

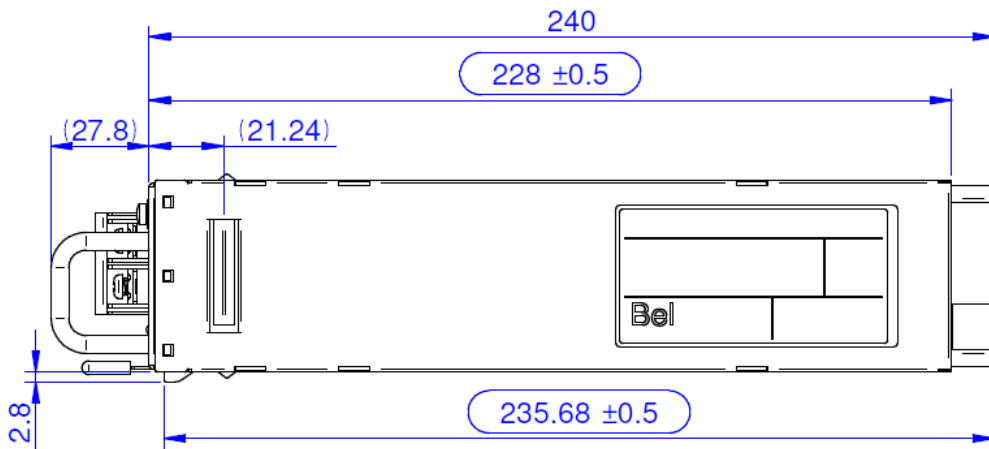


Figure 24. Top View

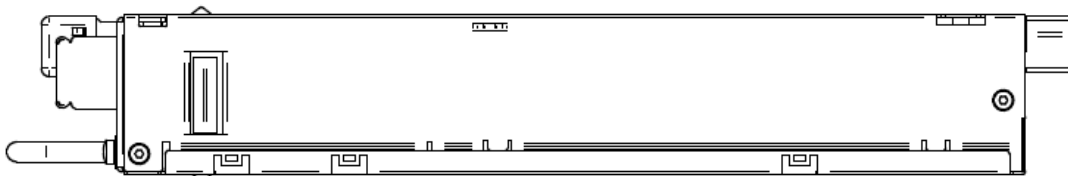


Figure 25. Side View 2

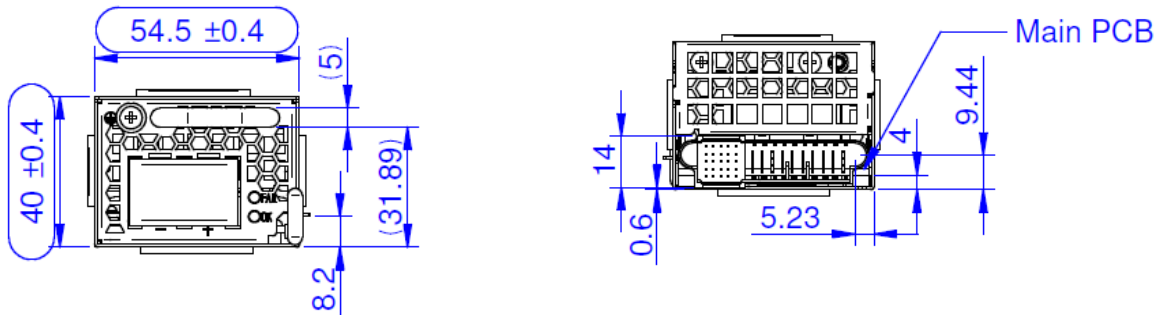
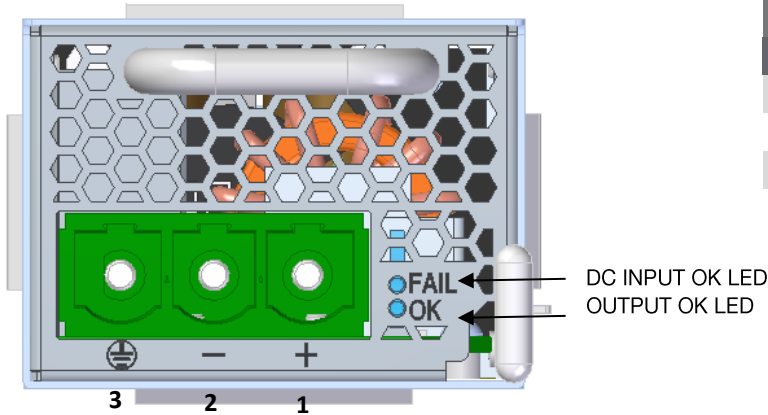


Figure 26. Front and Rear View

14. CONNECTIONS

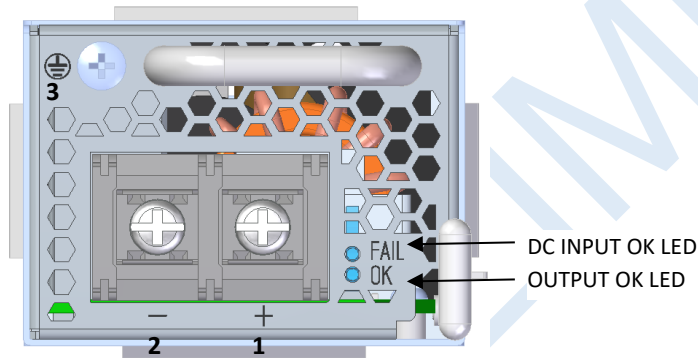
14.1 INPUT CONNECTOR (PFS1200-12-054xD)



PIN	NAME	DESCRIPTION
<i>Input</i>		
1	Vin+	Input positive
2	Vin-	Input negative
3	PE	Ground (⏚)

Unit: Three pole Phoenix Contact (P/N PC 6-16/ 3-G1-10,16, Code 1998946)  
 Counter part: Three pole Phoenix Contact (P/N SPC 16/ 3-ST-10,16, Code 1711271) with push-in spring connection (no tools required)

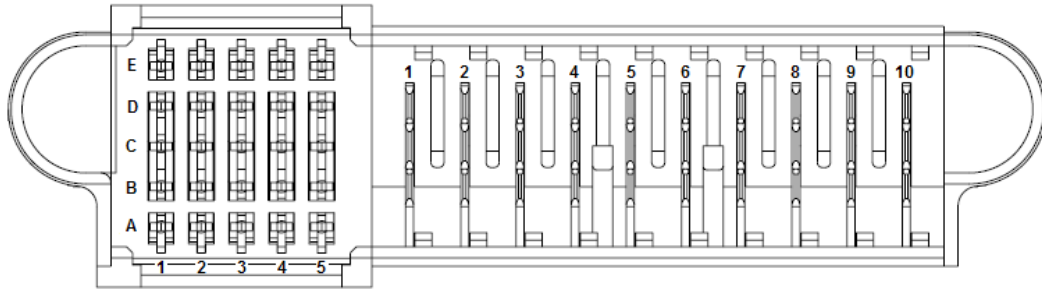
14.2 INPUT CONNECTOR (PFS1200-12-054xDB)



PIN	NAME	DESCRIPTION
<i>Input</i>		
1	Vin+	Input positive
2	Vin-	Input negative
3	PE	Ground (⏚)

DC input connector: Dinkle DT-7C-B14W-02

### 14.3 OUTPUT CONNECTOR



Power Supply Connector: Tyco Electronics P/N 2-1926736-3 (**NOTE: Column 5 is recessed (short pins)**)


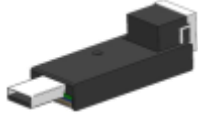

Mating Connector: Tyco Electronics P/N 2-1926739-5 or FCI 10108888-R10253SLF

#### 14.3.1 PIN DEFINITION

PIN	NAME	DESCRIPTION
<i>Output</i>		
6, 7, 8, 9, 10	V1	+12 VDC main output
1, 2, 3, 4, 5	PGND	Power ground (return)
<i>Control Pins</i>		
A1	VSB	Standby positive output (+3.3/5 V <sub>SB</sub> or 12 V <sub>SB</sub> )
B1	VSB	Standby positive output (+3.3/5 V <sub>SB</sub> or 12 V <sub>SB</sub> )
C1	VSB	Standby positive output (+3.3/5 V <sub>SB</sub> or 12 V <sub>SB</sub> )
D1	VSB	Standby positive output (+3.3/5 V <sub>SB</sub> or 12 V <sub>SB</sub> )
E1	VSB	Standby positive output (+3.3/5 V <sub>SB</sub> or 12 V <sub>SB</sub> )
A2	SGND	Signal ground (return)
B2	SGND	Signal ground (return)
C2	HOTSTANDBYEN_H	Hot standby enable signal: active-high
D2	VSB_SENSE_R	Standby output negative sense ( <b>Not used for 12 V<sub>SB</sub> model</b> )
E2	VSB_SENSE	Standby output positive sense ( <b>Not used for 12 V<sub>SB</sub> model</b> )
A3	APS	I <sup>2</sup> C address and protocol selection (select by a pull down resistor)
B3	N/C	Reserved
C3	SDA	I <sup>2</sup> C data signal line
D3	V1_SENSE_R	Main output negative sense
E3	V1_SENSE	Main output positive sense
A4	SCL	I <sup>2</sup> C clock signal line
B4	PSON_L	Power supply on input (connect to A2/B2 to turn unit on): active-low
C4	SMB_ALERT_L	SMB Alert signal output: active-low
D4	N/C	Reserved
E4	VINOK_H	DC input OK signal: active-high
A5	PSKILL_H	Power supply kill (lagging pin): active-high
B5	ISHARE	Current share bus (lagging pin)
C5	PWOK_H	Power OK signal output (lagging pin): active-high
D5	VSB_SEL	Standby voltage selection (lagging pin) ( <b>Not used for 12 V<sub>SB</sub> model</b> )
E5	PRESENT_L	Power supply present (lagging pin): active-low

Table 4. Pin Description

15. ACCESSORIES

ITEM	DESCRIPTION	ORDERING PART NUMBER	SOURCE
	<p><b>I<sup>2</sup>C Utility</b> Windows XP/Vista/7 compatible GUI to program, control and monitor PFS Front-Ends (and other I<sup>2</sup>C units)</p>	<p>N/A</p>	<p><a href="http://belfuse.com/power-solutions">belfuse.com/power-solutions</a></p>
	<p><b>USB to I<sup>2</sup>C Converter</b> Master I<sup>2</sup>C device to program, control and monitor I<sup>2</sup>C units in conjunction with the <i>I<sup>2</sup>C Utility</i></p>	<p>ZM-00056</p>	<p>Bel Power Solutions</p>
	<p><b>Dual Connector Board</b> Connector board to operate 2 PFS units in parallel. Includes an on-board USB to I<sup>2</sup>C converter (use <i>I<sup>2</sup>C Utility</i> as desktop software)</p>	<p>SNP-OP-BOARD-01 YTM.G1Q01.0</p>	<p>Bel Power Solutions</p>

PRELIMINARY

## 6 REVISION HISTORY

DATE	REVISION	SECTION	ISSUE	PREPARED BY	APPROVED BY
2019/01/11	Preliminary		First release	Mike Chen	-

For more information on these products consult: [tech.support@psbel.com](mailto:tech.support@psbel.com)

**NUCLEAR AND MEDICAL APPLICATIONS** - Products are not designed or intended for use as critical components in life support systems, equipment used in hazardous environments, or nuclear control systems.

**TECHNICAL REVISIONS** - The appearance of products, including safety agency certifications pictured on labels, may change depending on the date manufactured. Specifications are subject to change without notice.



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