

Product Description

The PE42543 is a HaRP™ technology-enhanced absorptive SP4T RF switch designed for use in Test/ATE, microwave and other wireless applications. This broadband general purpose switch is a pin-compatible version of the PE42542 with faster switching time and settling time. It exhibits low insertion loss, high isolation and linearity performance from 9 kHz through 18 GHz. No blocking capacitors are required if DC voltage is not present on the RF ports.

The PE42543 is manufactured on pSemi's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate.

pSemi's HaRP technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Features

- HaRP technology-enhanced
 - Fast settling time
 - No gate and phase lag
 - No drift in insertion loss and phase
- Fast switching time of 500 ns
- Low insertion loss
 - 1.20 dB @ 3 GHz
 - 2.30 dB @ 13.5 GHz
 - 3.10 dB @ 16 GHz
 - 4.10 dB @ 18 GHz
- High isolation
 - 55 dB @ 3 GHz
 - 32 dB @ 13.5 GHz
 - 28 dB @ 16 GHz
 - 25 dB @ 18 GHz
- ESD performance
 - 2000V HBM on all pins
 - 150V MM on all pins
 - 250V CDM on all pins

Figure 1. Functional Diagram

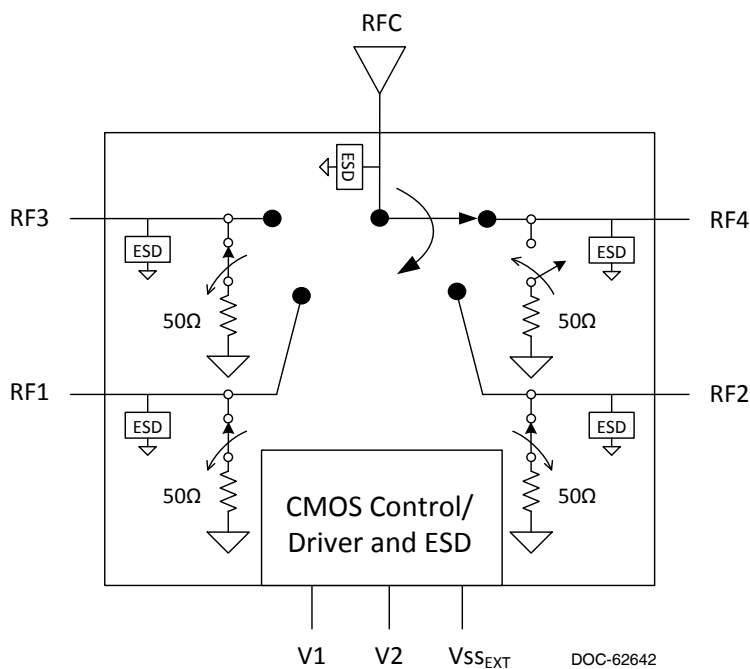


Figure 2. Package Type
29-lead 4 × 4 mm LGA

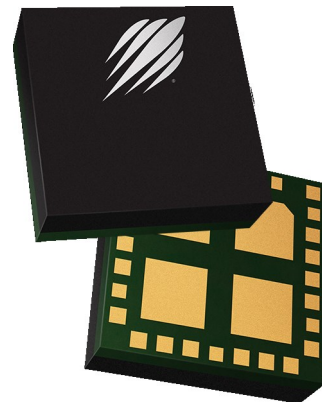


Table 1. Electrical Specifications @ 25°C ($Z_S = Z_L = 50\Omega$), unless otherwise noted
Normal Mode¹: $V_{DD} = 3.3V$, $V_{SS_EXT} = 0V$ or Bypass Mode²: $V_{DD} = 3.4V$, $V_{SS_EXT} = -3.4V$

| Parameter | Path | Condition | Min | Typ | Max | Unit |
|--|---------|---------------------------------------|-----|---------------|------|---------|
| Operating frequency | | | 9 k | | 18 G | Hz |
| Insertion loss | RFC–RFX | 9 kHz–10 MHz | | 0.70 | 0.85 | dB |
| | | 10–3000 MHz | | 1.20 | 1.50 | dB |
| | | 3000–7500 MHz | | 1.65 | 2.05 | dB |
| | | 7500–10000 MHz | | 2.10 | 2.55 | dB |
| | | 10000–13500 MHz | | 2.30 | 2.80 | dB |
| | | 13500–16000 MHz | | 3.10 | 3.60 | dB |
| | | 16000–18000 MHz | | 4.10 | 4.70 | dB |
| Isolation | RFX–RFX | 9 kHz–10 MHz | 80 | 90 | | dB |
| | | 10–3000 MHz | 53 | 55 | | dB |
| | | 3000–7500 MHz | 46 | 48 | | dB |
| | | 7500–10000 MHz | 41 | 43 | | dB |
| | | 10000–13500 MHz | 36 | 38 | | dB |
| | | 13500–16000 MHz | 31 | 33 | | dB |
| | | 16000–18000 MHz | 27 | 29 | | dB |
| Isolation | RFC–RFX | 9 kHz–10 MHz | 78 | 90 | | dB |
| | | 10–3000 MHz | 54 | 55 | | dB |
| | | 3000–7500 MHz | 41 | 42 | | dB |
| | | 7500–10000 MHz | 36 | 38 | | dB |
| | | 10000–13500 MHz | 31 | 32 | | dB |
| | | 13500–16000 MHz | 27 | 28 | | dB |
| | | 16000–18000 MHz | 24 | 25 | | dB |
| Return loss (active and common port) | RFC–RFX | 9 kHz–10 MHz | | 22 | | dB |
| | | 10–3000 MHz | | 15 | | dB |
| | | 3000–18000 MHz | | 14 | | dB |
| Return loss (terminated port) | RFX | 9 kHz–18000 MHz | | 14 | | dB |
| Input 0.1dB compression point ³ | RFC–RFX | | | <i>Fig. 4</i> | | dBm |
| Input IP2 | RFC–RFX | 30–18000 MHz | | 113 | | dBm |
| Input IP3 | RFC–RFX | 30–18000 MHz | | 59 | | dBm |
| Settling time | | 50% CTRL to 0.05 dB final value | | 2 | 3 | μ s |
| Switching time | | 50% CTRL to 90% or 10% of final value | | 500 | 800 | ns |

Notes: 1. Normal mode: connect V_{SS_EXT} (pin 29) to GND ($V_{SS_EXT} = 0V$) to enable internal negative voltage generator.

2. Bypass mode: use V_{SS_EXT} (pin 29) to bypass and disable internal negative voltage generator.

3. The input 0.1dB compression point is a linearity figure of merit. Refer to *Table 3* for the RF input power P_{MAX} (50 Ω).

Table 4. Absolute Maximum Ratings

| Parameter/Condition | Symbol | Min | Max | Unit |
|--|-------------------------|------|--------------|------------|
| Maximum junction tempera- | | | +150 | °C |
| Storage temperature range | T _{ST} | -60 | +150 | °C |
| Supply voltage | V _{DD} | -0.3 | 5.5 | V |
| Digital input voltage (V1, V2) | V _{CTRL} | -0.3 | 3.6 | V |
| RF input power, CW (RFC-RFX) ¹ 9 kHz–27.5 MHz ≥ 27.5 MHz–18 GHz | P _{MAX,ABS} | | Fig. 4 33 | dBm dBm |
| RF input power, pulsed (RFC-RFX) ² 9 kHz–27.5 MHz ≥ 27.5 MHz–18 GHz | P _{MAX,PULSED} | | Fig. 4 34 | dBm dBm |
| RF input power into terminated ports, CW (RFX) ¹ 9 kHz–18.8 MHz ≥ 18.8 MHz–18 GHz | P _{MAX,TERM} | | Fig. 4 22 | dBm dBm |
| Storage temperature range | T _{ST} | -65 | +150 | °C |
| ESD voltage HBM ³ , all pins | V _{ESD,HBM} | | 2000 | V |
| ESD voltage MM ⁴ , all pins | V _{ESD,MM} | | 150 | V |
| ESD voltage CDM ⁵ , all pins | V _{ESD,CDM} | | 250 | V |

Notes: 1. 100% duty cycle, all bands, 50Ω
2. Pulsed, 5% duty cycle of 4620 μs period, 50Ω
3. Human Body Model (MIL-STD 883 Method 3015)
4. Machine Model (JEDEC JESD22-A115)
5. Charged Device Model (JEDEC JESD22-C101)

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Switching Frequency

The PE42543 has a maximum 25 kHz switching rate when the internal negative voltage generator is used (pin 29 = GND). Switching frequency describes the time duration between switching events. Switching time is the duration between the point the control signal reaches 50% of the final value and the point the output signal reaches within 10% or 90% of its target value.

Optional External V_{SS} Control (V_{SS_EXT})

For proper operation, the V_{SS_EXT} control pin must be grounded or tied to the V_{SS} voltage specified in Table 3. When the V_{SS_EXT} control pin is grounded, FETs in the switch are biased with an internal negative voltage generator. For applications that require the lowest possible spur performance, V_{SS_EXT} can be applied externally to bypass the internal negative voltage generator.

Spurious Performance

The typical spurious performance of the PE42543 is -150 dBm when V_{SS_EXT} = 0V (pin 29 = GND). If further improvement is desired, the internal negative voltage generator can be disabled by setting V_{SS_EXT} = -3.4V.

Table 5. Truth Table

| State | V1 | V2 |
|--------|----|----|
| RF1 on | 0 | 0 |
| RF2 on | 1 | 0 |
| RF3 on | 0 | 1 |
| RF4 on | 1 | 1 |

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE42543 in the 29-lead 4 × 4 mm LGA package is MSL3.

Hot-Switching Capability

The maximum hot switching capability of the PE42543 is 20 dBm from 18.8 MHz to 18 GHz. The maximum hot switching capability below 18.8 MHz does not exceed the maximum RF CW terminated power, see Figure 4. Hot switching occurs when RF power is applied while switching between RF ports.

Figure 4a. Power De-rating Curve for 9 kHz–18 GHz @ 25°C Ambient (50Ω)

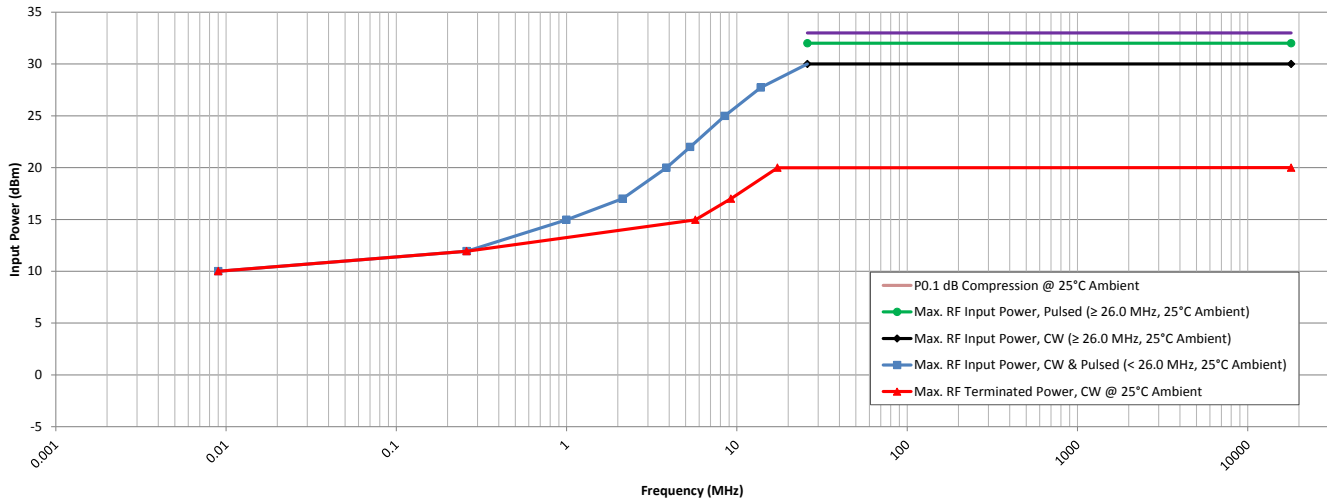
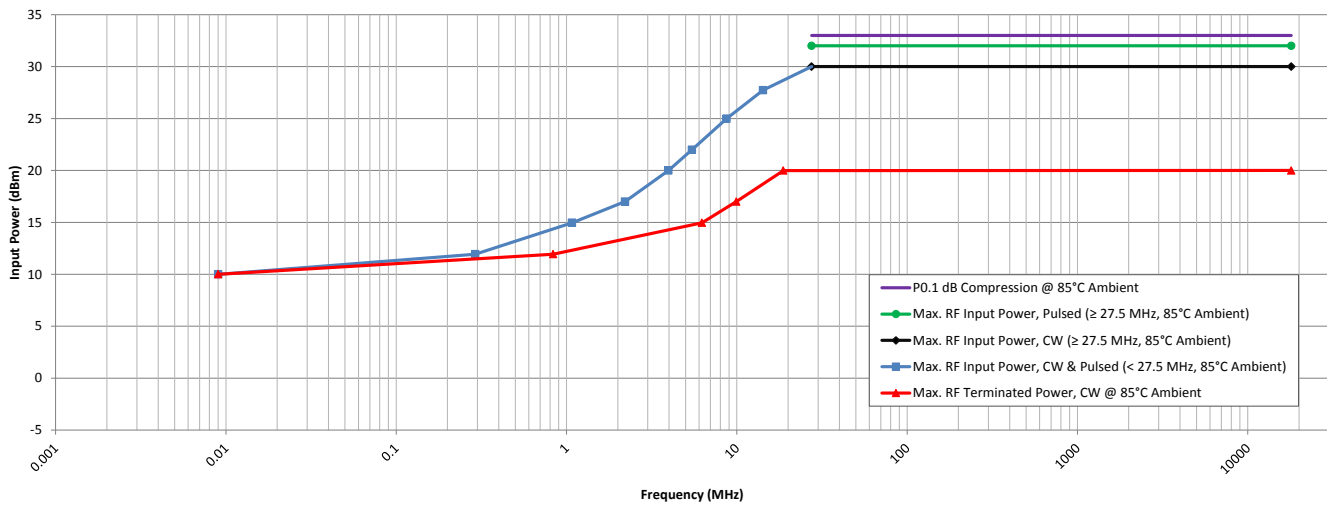


Figure 4b. Power De-rating Curve for 9 kHz–18 GHz @ 85°C Ambient (50Ω)



Typical Performance Data @ 25°C and $V_{DD} = 3.3V$ ($Z_S = Z_L = 50\Omega$), unless otherwise noted

Figure 5. Insertion Loss (RFC–RFX)

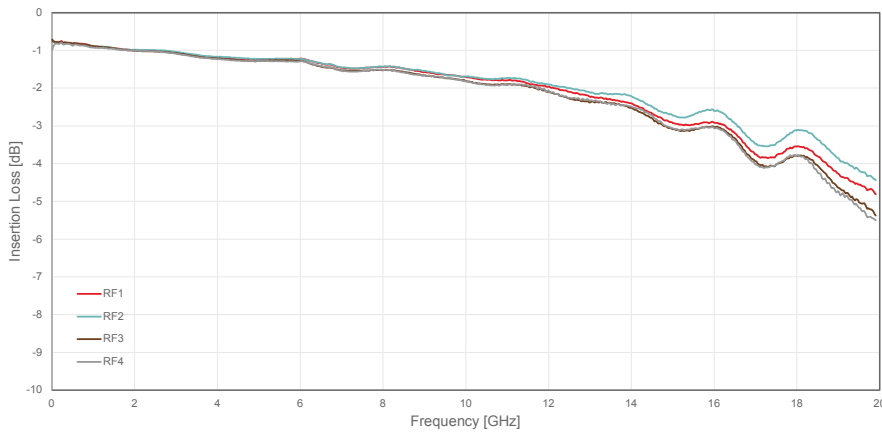


Figure 6. Insertion Loss vs. Temp (RFC–RFX)

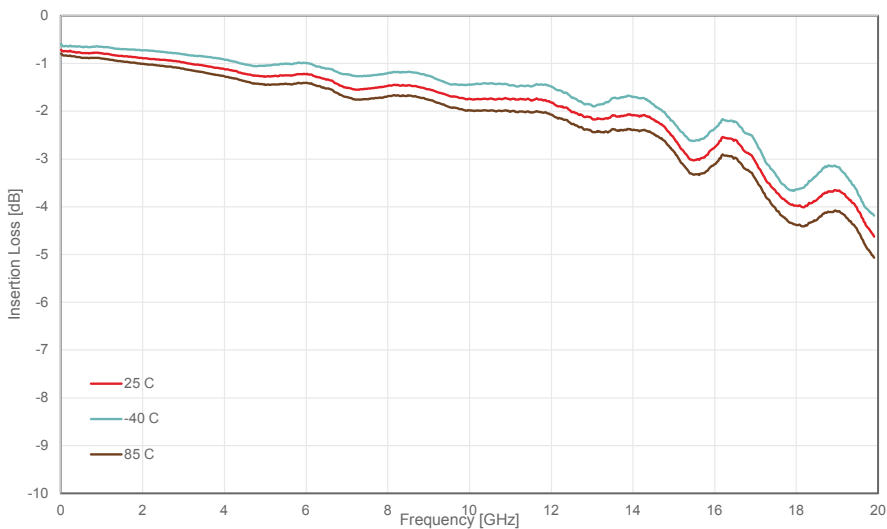
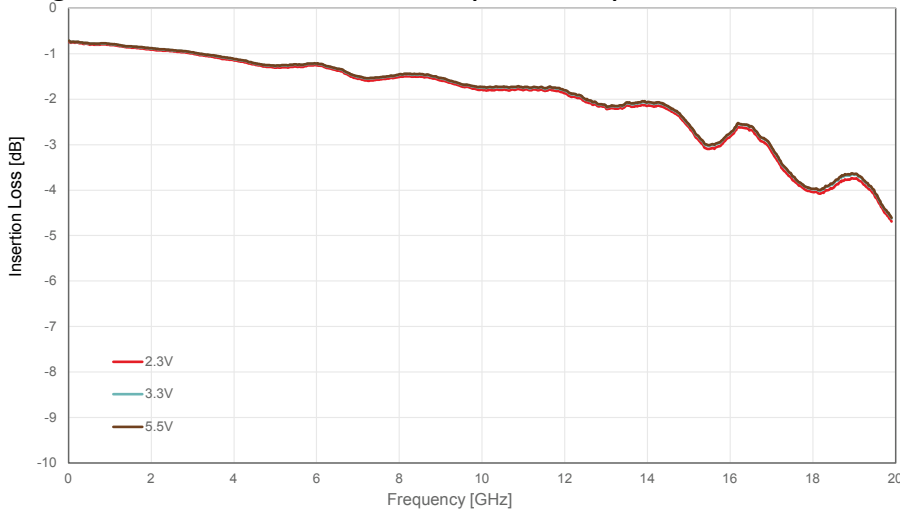


Figure 7. Insertion Loss vs. V_{DD} (RFC–RFX)



Typical Performance Data @ 25°C and $V_{DD} = 3.3V$ ($Z_S = Z_L = 50\Omega$), unless otherwise noted

Figure 8. RFC Port Return Loss vs. Temp

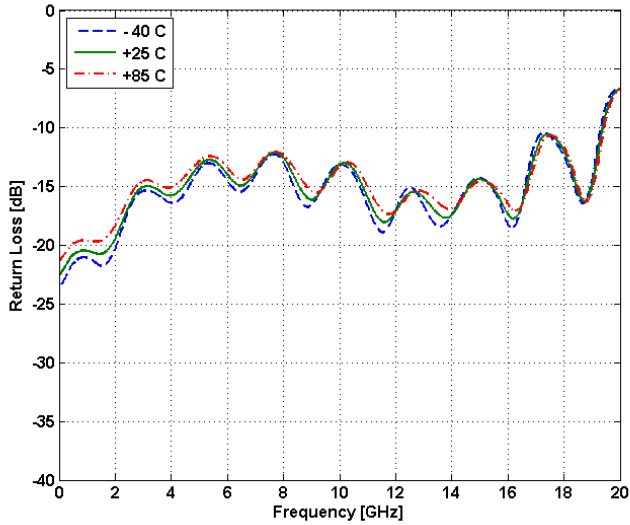


Figure 9. RFC Port Return Loss vs. V_{DD}

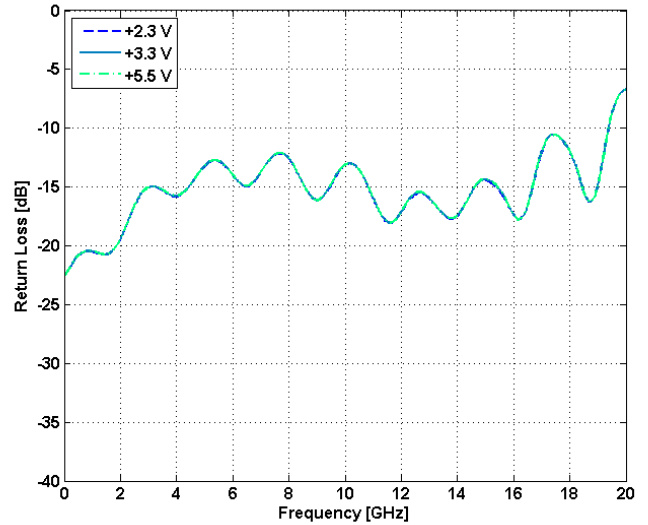


Figure 10. Active Port Return Loss vs. Temp

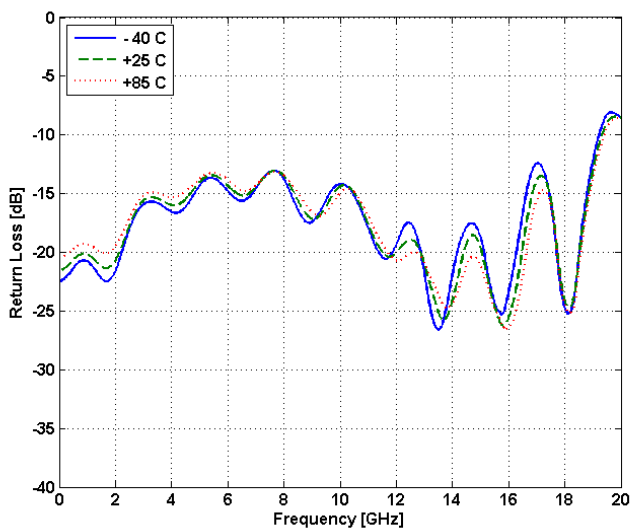
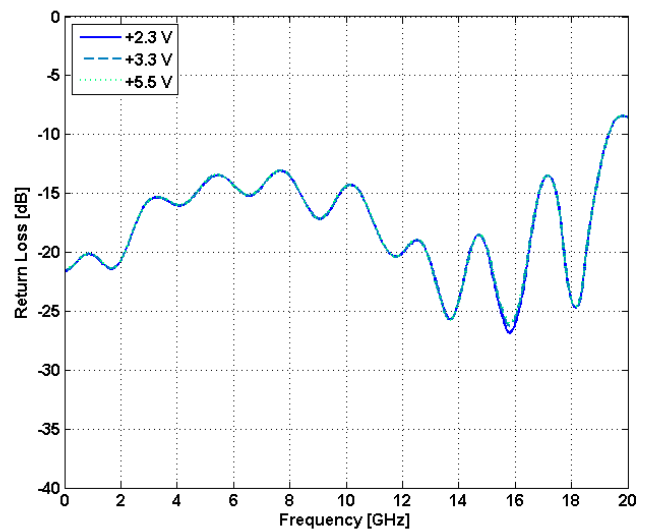


Figure 11. Active Port Return Loss vs. V_{DD}



Typical Performance Data @ 25°C and $V_{DD} = 3.3V$ ($Z_S = Z_L = 50\Omega$), unless otherwise noted

Figure 12. Terminated Port Return Loss vs. Temp

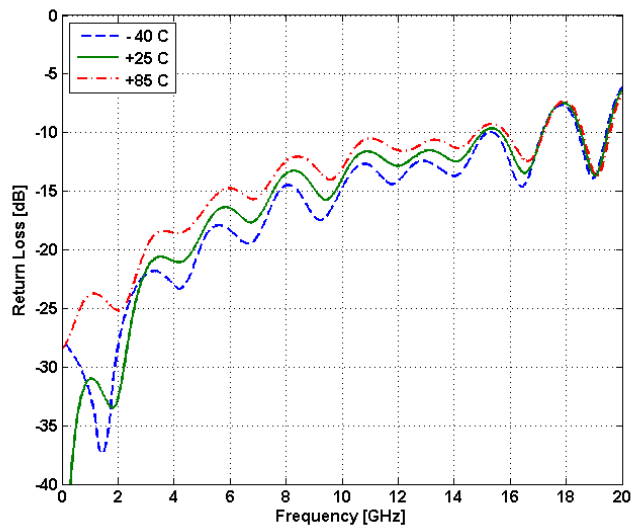
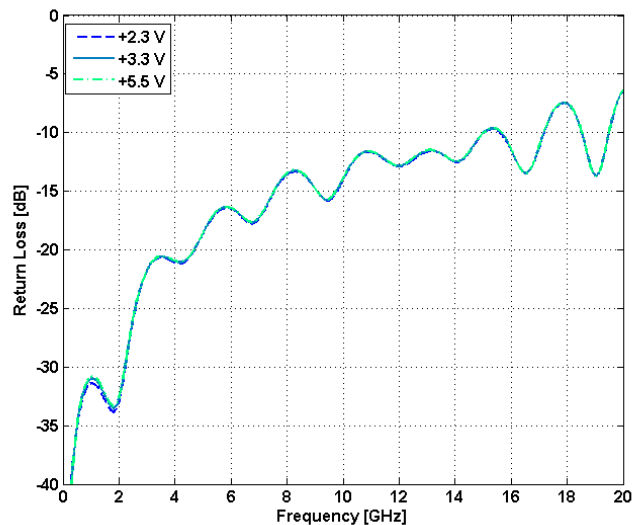


Figure 13. Terminated Port Return Loss vs. V_{DD}



Typical Performance Data @ 25°C and $V_{DD} = 3.3V$ ($Z_S = Z_L = 50\Omega$), unless otherwise noted

Figure 14. Isolation vs. Temp (RFX–RFX)*

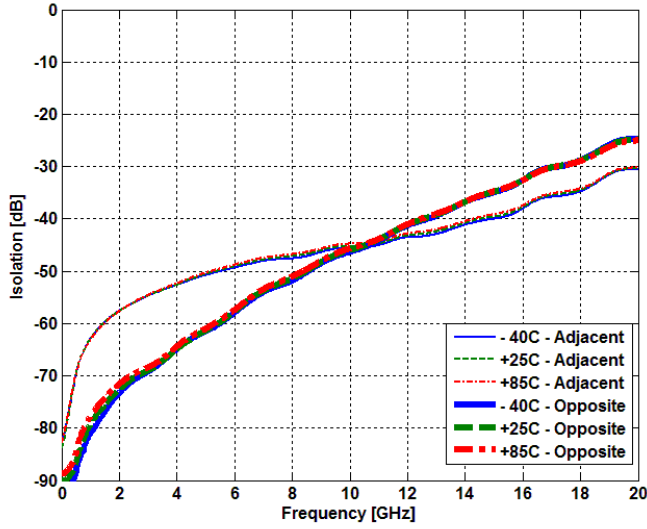
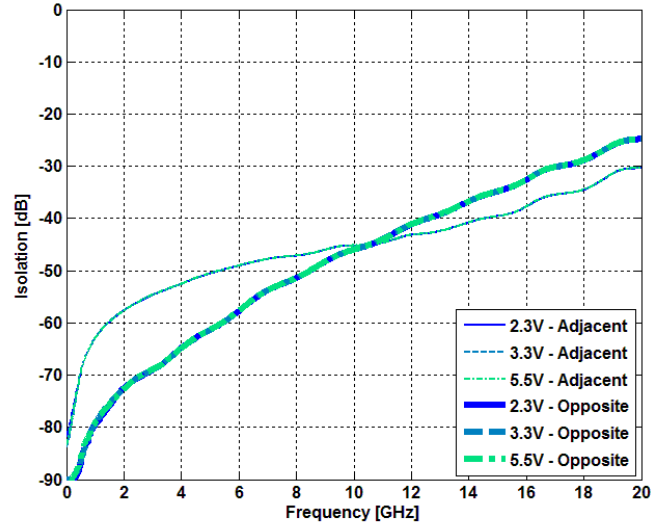


Figure 15. Isolation vs. V_{DD} (RFX–RFX)*



Note: * RF1 adjacent to RF3
RF2 adjacent to RF4
RF1 and RF3 opposite to RF2 and RF4

Typical Performance Data @ 25°C and $V_{DD} = 3.3V$ ($Z_S = Z_L = 50\Omega$), unless otherwise noted

Figure 16. Isolation vs. Temp
(RFC–RFX, RF1 or RF2 Active)*

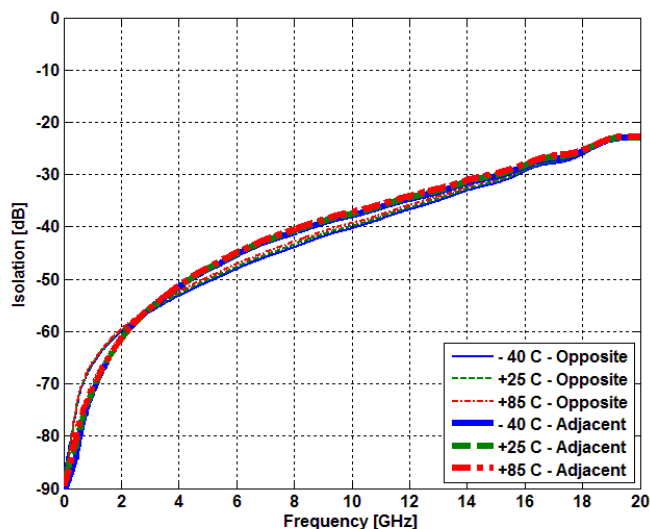


Figure 17. Isolation vs. V_{DD}
(RFC–RFX, RF1 or RF2 Active)*

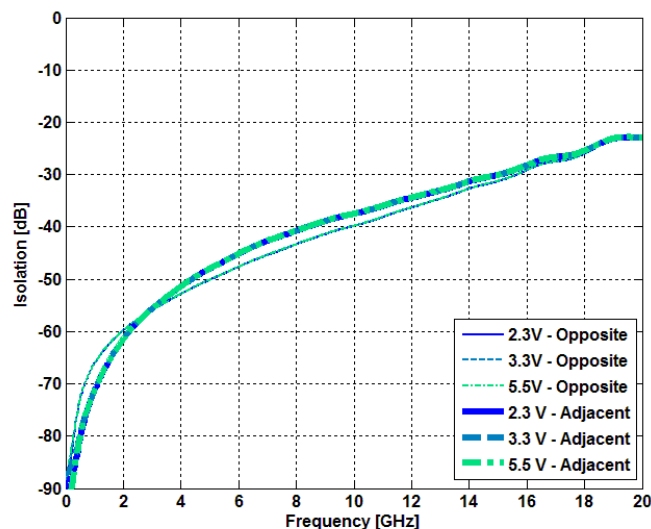


Figure 18. Isolation vs. Temp
(RFC–RFX, RF3 or RF4 Active)*

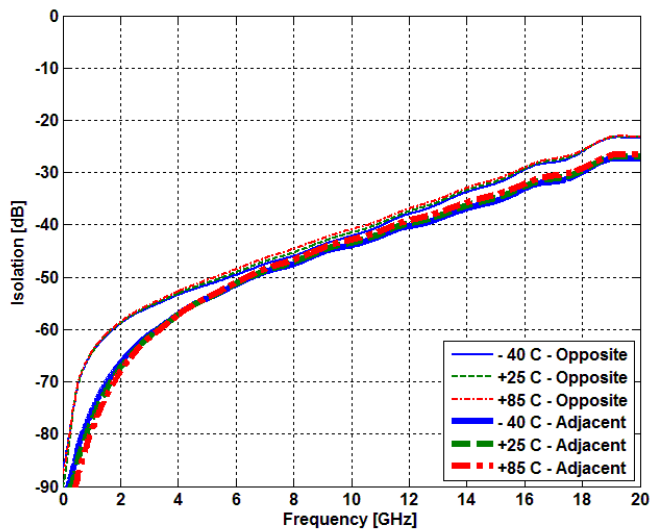
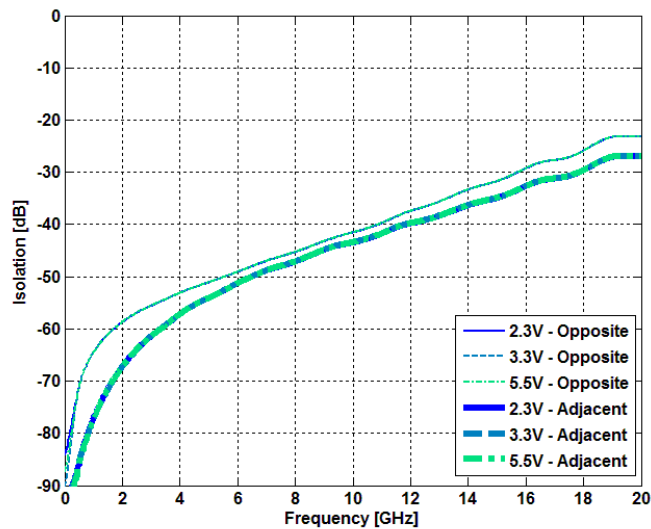


Figure 19. Isolation vs. V_{DD}
(RFC–RFX, RF3 or RF4 Active)*



Note: * RF1 adjacent to RF3
RF2 adjacent to RF4
RF1 and RF3 opposite to RF2 and RF4

Evaluation Kit

The SP4T switch evaluation board was designed to ease customer evaluation of pSemi's PE42543. The RF common port is connected through a 50Ω transmission line via the SMA connector, J1. RF1, RF2, RF3 and RF4 ports are connected through 50Ω transmission lines via SMA connectors J4, J3, J2 and J5, respectively. A 50Ω through transmission line is available via SMA connectors J6 and J7, which can be used to de-embed the loss of the PCB. J13 provides DC and digital inputs to the device.

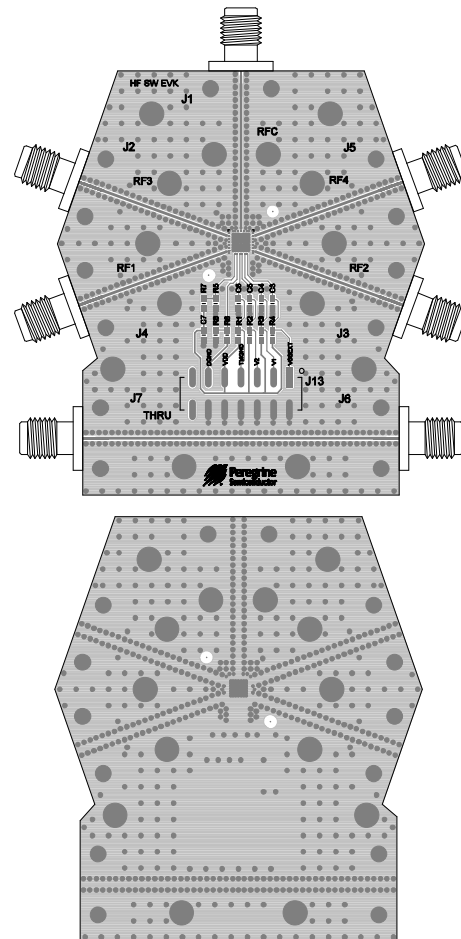
The board is constructed of a four metal layer material with a total thickness of 62 mils. The top RF layer is Rogers 4360 material with a thickness of 32 mils and the $\epsilon_r = 6.4$. The middle layers provide ground for the transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 18 mils, trace gaps of 7 mils and metal thickness of 2.1 mils.

For the true performance of the PE42543 to be realized, the PCB should be designed in such a way that RF transmission lines and sensitive DC I/O traces are heavily isolated from one another.

High frequency insertion loss and return loss can be further improved by external series inductive tuning traces in the customer application board layout. For example, to improve 12–18 GHz performance, use ~ 180 pH for RFX ports and ~ 50 pH for RFC port.

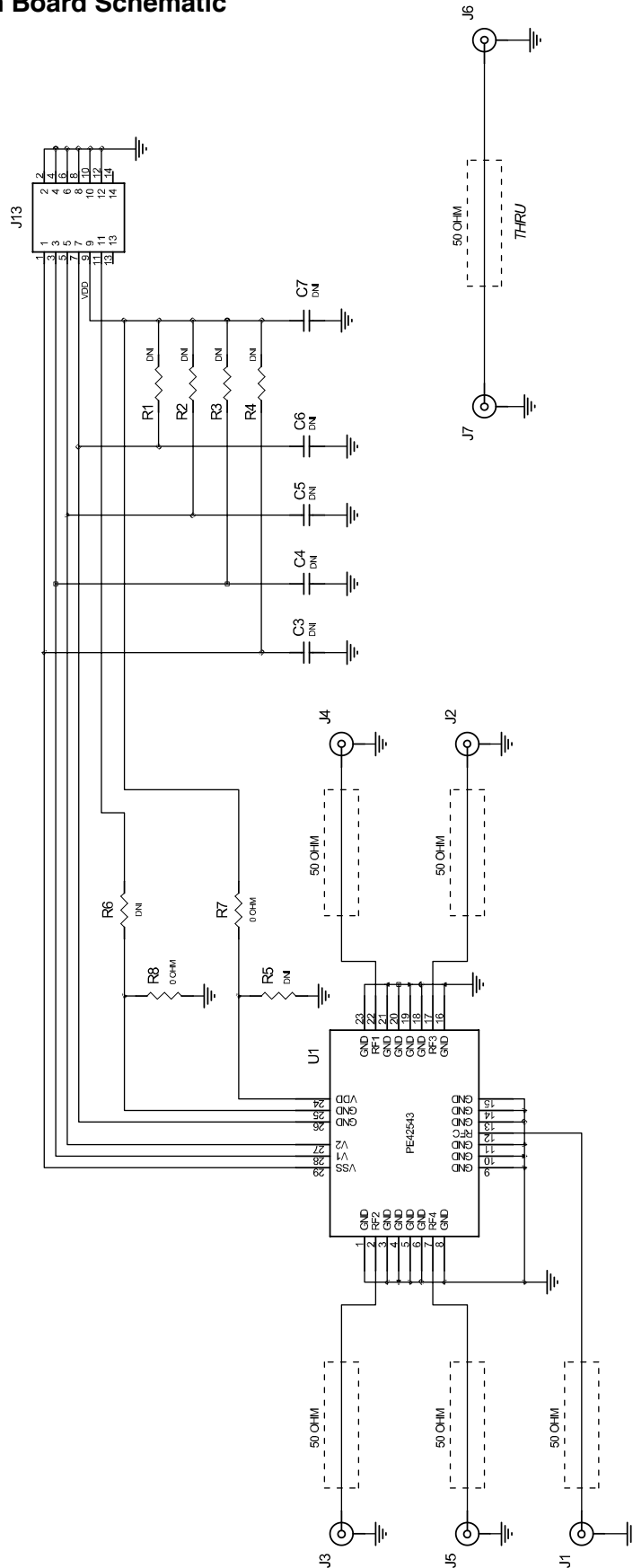
Vector de-embed is recommended to more accurately calculate the performance of the DUT. Refer to Application Note 39 "*Vector De-embedding of the PE42542 and PE42543 SP4T RF Switches*" for additional information. The half thru line data file can be downloaded from pSemi's website to facilitate the vector de-embedding.

Figure 20. Evaluation Board Layout



PRT-09205

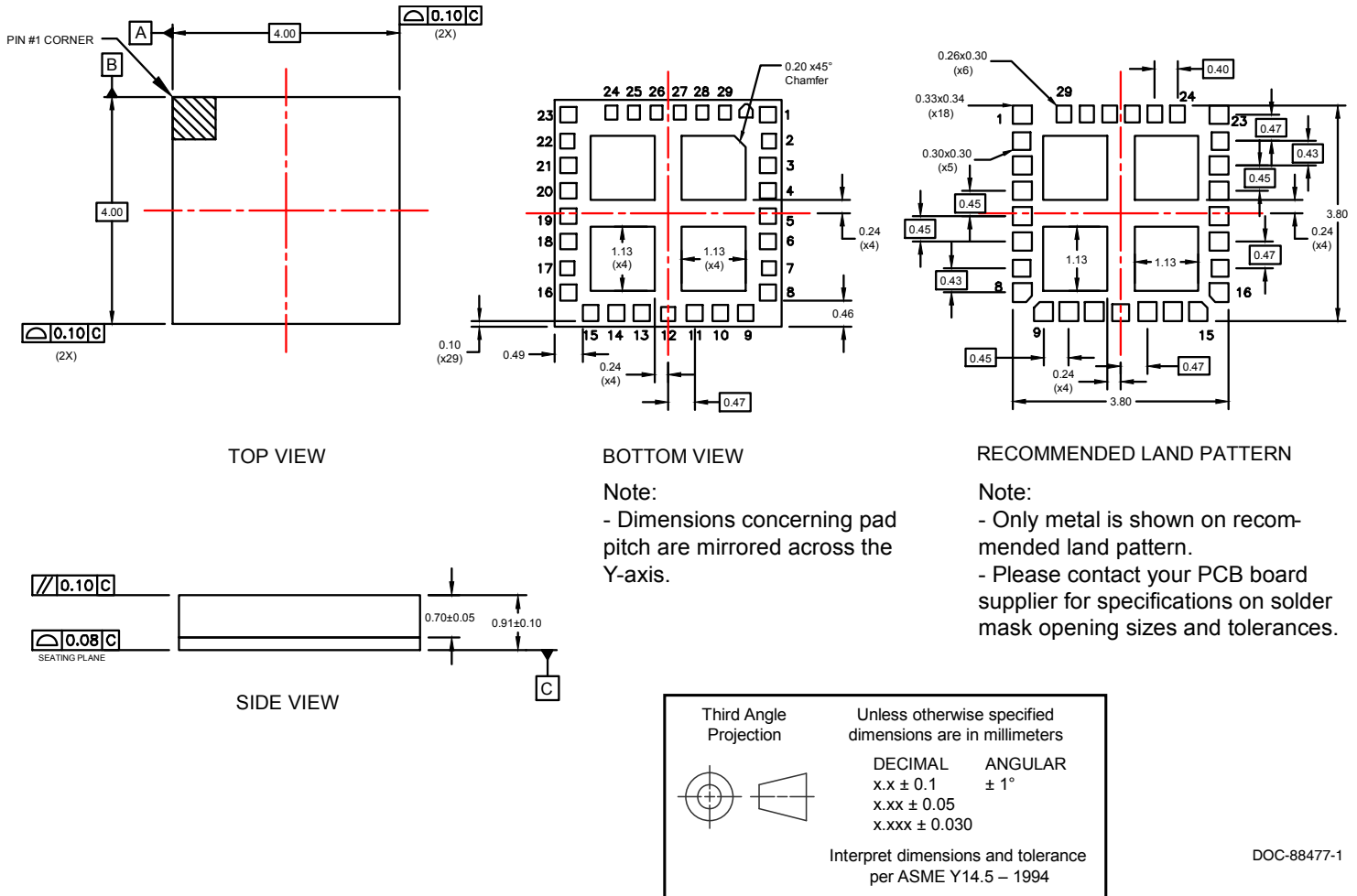
Figure 21. Evaluation Board Schematic



CAUTION: Contains parts and assemblies susceptible to damage by electrostatic discharge (ESD).

DOC-12327

Figure 22. Package Drawing
29-lead 4 × 4 mm LGA



DOC-88477-1

Figure 23. Top Marking Specification



- = Pin 1 designator
- YYWW = Date code, last two digits of assembly year and work week
- ZZZZZZ = Last six characters of the assembly lot code

DOC-65745

Figure 24. Tape and Reel Drawing

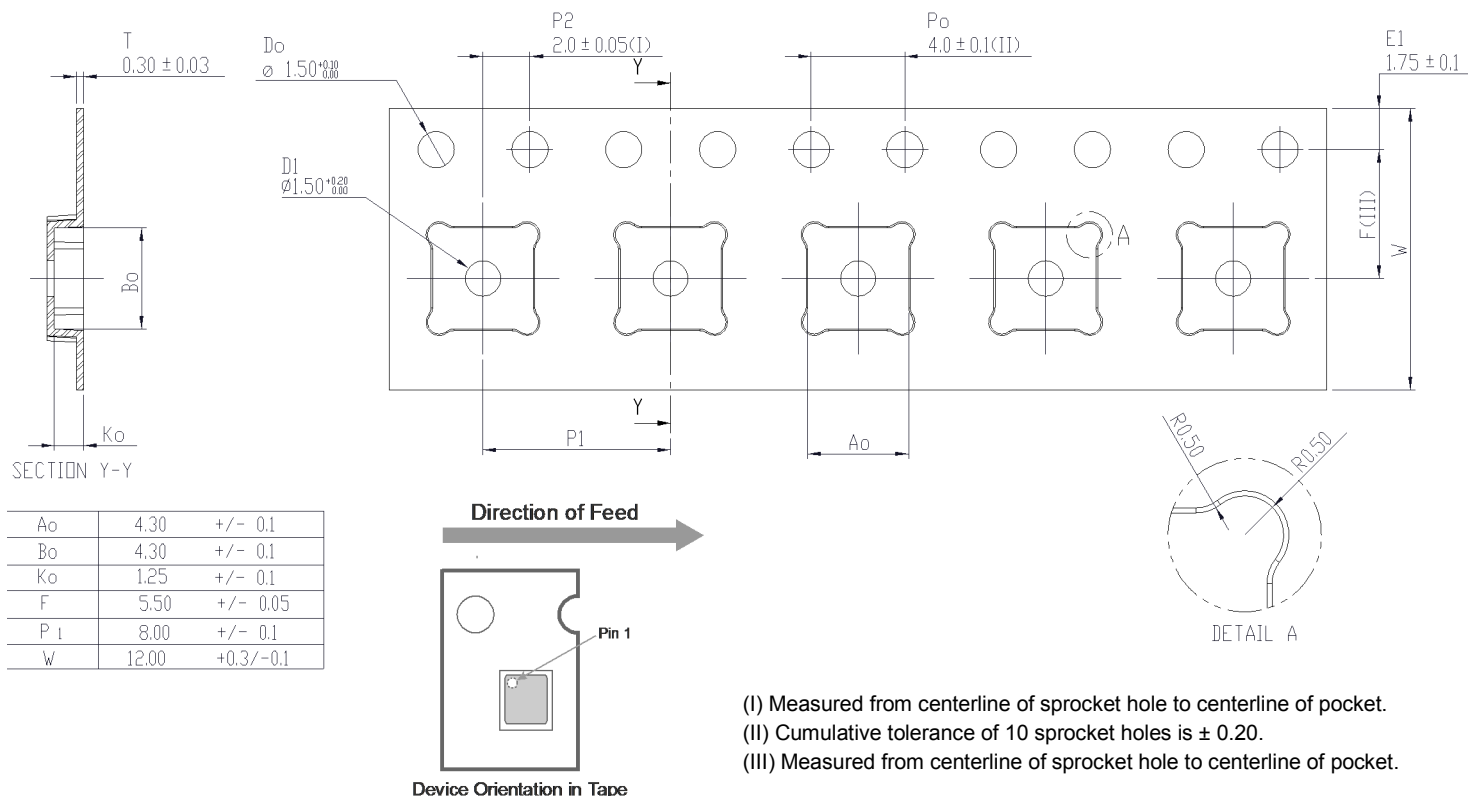


Table 7. Ordering Information

| Order Code | Description | Package | Shipping Method |
|------------|------------------------|----------------------|-----------------|
| PE42543B-X | PE42543 SP4T RF switch | 29-lead 4 x 4 mm LGA | 500 units / T&R |
| EK42543-03 | PE42543 Evaluation kit | Evaluation kit | 1 / Box |

Sales Contact and Information

For sales and contact information please visit www.psemi.com.

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