PCA9536

4-bit I²C-bus and SMBus I/O port

Rev. 03 — 9 October 2006 Product data sheet

1. General description

The PCA9536 is an 8-pin CMOS device that provides 4 bits of General Purpose parallel Input/Output (GPIO) expansion for I²C-bus/SMBus applications and was developed to enhance the NXP Semiconductors family of I²C-bus I/O expanders. I/O expanders provide a simple solution when additional I/O is needed for ACPI power switches, sensors, push buttons, LEDs, fans, etc.

The PCA9536 consists of a 4-bit Configuration register (input or output selection), 4-bit Input Port register, 4-bit Output Port register and a 4-bit Polarity Inversion register (active HIGH or active LOW operation). The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input Port or Output Port register. The polarity of the read register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

The power-on reset sets the registers to their default values and initializes the device state machine.

The I²C-bus address is fixed and allows only one device on the same I²C-bus/SMBus.

2. Features

- 4-bit I²C-bus GPIO
- Operating power supply voltage range of 2.3 V to 5.5 V
- 5 V tolerant I/Os
- Polarity Inversion register
- Active LOW interrupt output
- Low standby current
- Noise filter on SCL/SDA inputs
- No glitch on power-up
- Internal power-on reset
- 4 I/O pins which default to 4 inputs with 100 kΩ internal pull-up resistor
- 0 Hz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: SO8, TSSOP8 (MSOP8), HVSON8

founded by Philips

3. Ordering information

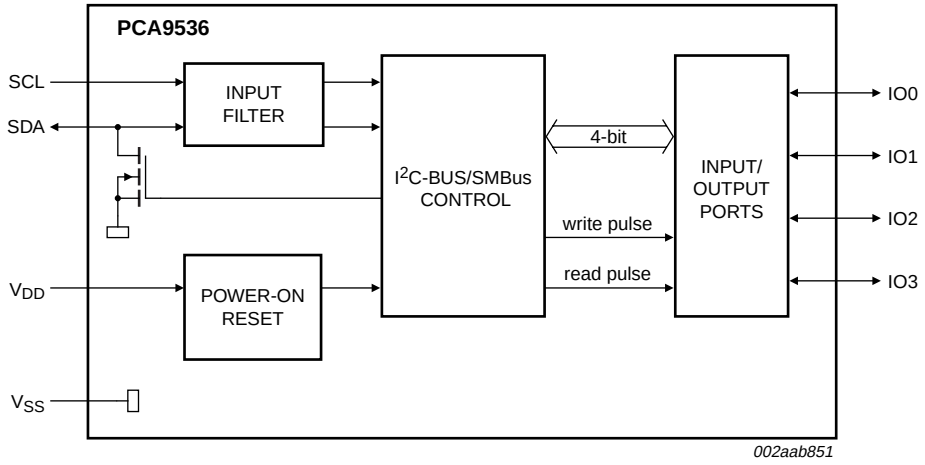
Table 1. Ordering information

T_{amb} = −40 °C to +85 °C

Type number	Topside mark	Package		
		Name	Description	Version
PCA9536D	PCA9536	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
PCA9536DP	9536	TSSOP8[1]	plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1
PCA9536TK	9536	HVSON8	plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 × 3 × 0.85 mm	SOT908-1

[1] Also known as MSOP8.

4. Block diagram



All I/Os are set to inputs at reset.

Fig 1. Block diagram of PCA9536

© NXP B.V. 2006. All rights reserved.

5. Pinning information

5.1 Pinning

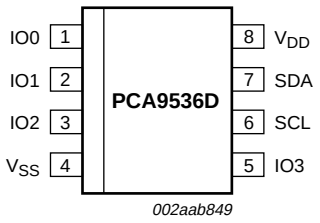


Fig 2. Pin configuration for SO8

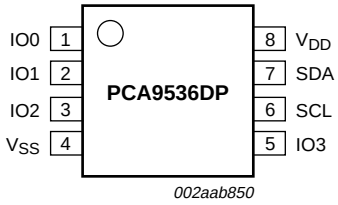


Fig 3. Pin configuration for TSSOP8

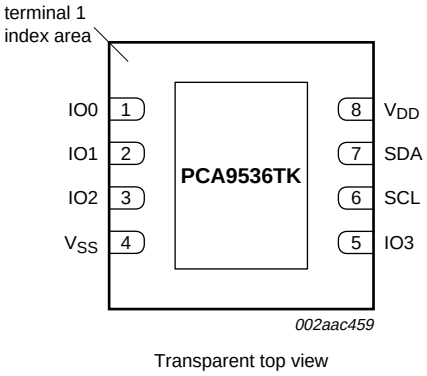


Fig 4. Pin configuration for HVSON8

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
IO0	1	input/output 0
IO1	2	input/output 1
IO2	3	input/output 2
V_{SS}	4	supply ground
IO3	5	input/output 3
SCL	6	serial clock line
SDA	7	serial data line
V_{DD}	8	supply voltage

© NXP B.V. 2006. All rights reserved.

6. Functional description

Refer to Figure 1 “Block diagram of PCA9536”.

6.1 Registers

6.1.1 Command byte

Table 3. Command byte

Command	Protocol	Function
0	read byte	Input Port register
1	read/write byte	Output Port register
2	read/write byte	Polarity Inversion register
3	read/write byte	Configuration register

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

6.1.2 Register 0 - Input Port register

This register is a read-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 3. Writes to this register have no effect.

The default ‘X’ is determined by the externally applied logic level, normally logic 1 when no external signal externally applied because of the internal pull-up resistors.

Table 4. Register 0 - Input Port register bit description

*Legend: * default value*

Bit	Symbol	Access	Value	Description
7	I7	read only	1*	not used
6	I6	read only	1*	
5	I5	read only	1*	
4	I4	read only	1*	
3	I3	read only	X	determined by externally applied logic level
2	I2	read only	X	
1	I1	read only	X	
0	I0	read only	X	

© NXP B.V. 2006. All rights reserved.

6.1.3 Register 1 - Output Port register

This register reflects the outgoing logic levels of the pins defined as outputs by Register 3. Bit values in this register have no effect on pins defined as inputs. Reads from this register return the value that is in the flip-flop controlling the output selection, **not** the actual pin value.

'Not used' bits can be programmed with either logic 0 or logic 1.

Table 5. Register 1 - Output Port register bit description

*Legend: * default value*

Bit	Symbol	Access	Value	Description
7	O7	R	1*	not used
6	O6	R	1*	
5	O5	R	1*	
4	O4	R	1*	
3	O3	R	1*	reflects outgoing logic levels of pins defined as outputs by Register 3
2	O2	R	1*	
1	O1	R	1*	
0	O0	R	1*	

6.1.4 Register 2 - Polarity Inversion register

This register allows the user to invert the polarity of the Input Port register data. If a bit in this register is set (written with '1'), the corresponding Input Port data is inverted. If a bit in this register is cleared (written with a '0'), the Input Port data polarity is retained.

'Not used' bits can be programmed with either logic 0 or logic 1.

Table 6. Register 2 - Polarity Inversion register bit description

*Legend: * default value*

Bit	Symbol	Access	Value	Description
7	N7	R/W	0*	not used
6	N6	R/W	0*	
5	N5	R/W	0*	
4	N4	R/W	0*	
3	N3	R/W	0*	inverts polarity of Input Port register data 0 = Input Port register data retained (default value) 1 = Input Port register data inverted
2	N2	R/W	0*	
1	N1	R/W	0*	
0	N0	R/W	0*	

© NXP B.V. 2006. All rights reserved.

6.1.5 Register 3 - Configuration register

This register configures the directions of the I/O pins. If a bit in this register is set, the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared, the corresponding port pin is enabled as an output. At reset, the I/Os are configured as inputs with a weak pull-up to V_{DD}.

'Not used' bits can be programmed with either logic 0 or logic 1.

Table 7. Register 3 - Configuration register bit description

*Legend: * default value*

Bit	Symbol	Access	Value	Description
7	C7	R/W	1*	not used
6	C6	R/W	1*	
5	C5	R/W	1*	
4	C4	R/W	1*	
3	C3	R/W	1*	configures the directions of the I/O pins
2	C2	R/W	1*	0 = corresponding port pin enabled as an output
1	C1	R/W	1*	1 = corresponding port pin configured as input (default value)
0	C0	R/W	1*	

6.2 Power-on reset

When power is applied to V_{DD}, an internal Power-On Reset (POR) holds the PCA9536 in a reset condition until V_{DD} has reached V_{POR}. At that point, the reset condition is released and the PCA9536 registers and state machine will initialize to their default states. Thereafter, V_{DD} must be lowered below 0.2 V to reset the device.

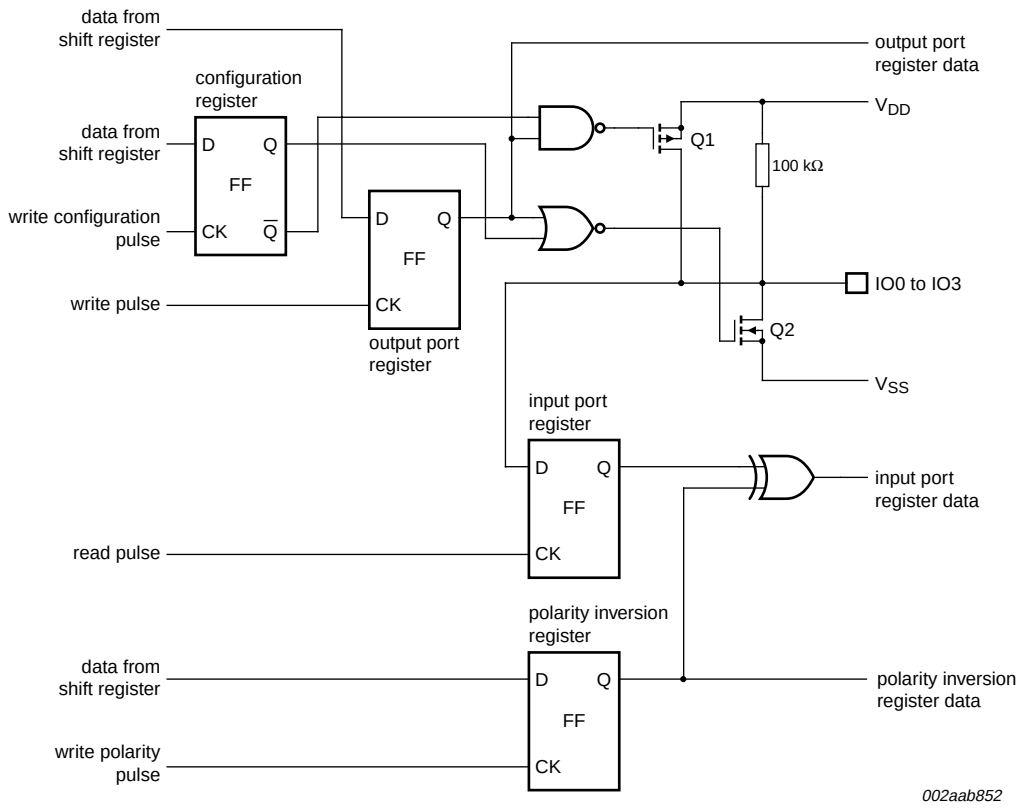
For a power reset cycle, V_{DD} must be lowered below 0.2 V and then restored to the operating voltage.

6.3 I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input with a weak pull-up (100 kΩ typ.) to V_{DD}. The input voltage may be raised above V_{DD} to a maximum of 5.5 V.

If the I/O is configured as an output, then either Q1 or Q2 is enabled, depending on the state of the Output Port register. Care should be exercised if an external voltage is applied to an I/O configured as an output because of the low-impedance paths that exist between the pin and either V_{DD} or V_{SS}.

© NXP B.V. 2006. All rights reserved.



Remark: At power-on reset, all registers return to default values.

Fig 5. Simplified schematic of IO0 to IO3

6.4 Device address

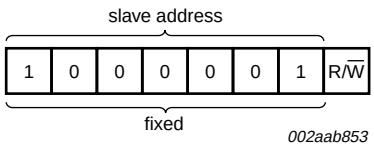


Fig 6. PCA9536 device address

6.5 Bus transactions

Data is transmitted to the PCA9536 registers using the Write mode as shown in Figure 7 and Figure 8. Data is read from the PCA9536 registers using the Read mode as shown in Figure 9 and Figure 10. These devices do not implement an auto-increment function, so once a command byte has been sent, the register which was addressed will continue to be accessed by reads until a new command byte has been sent.

© NXP B.V. 2006. All rights reserved.

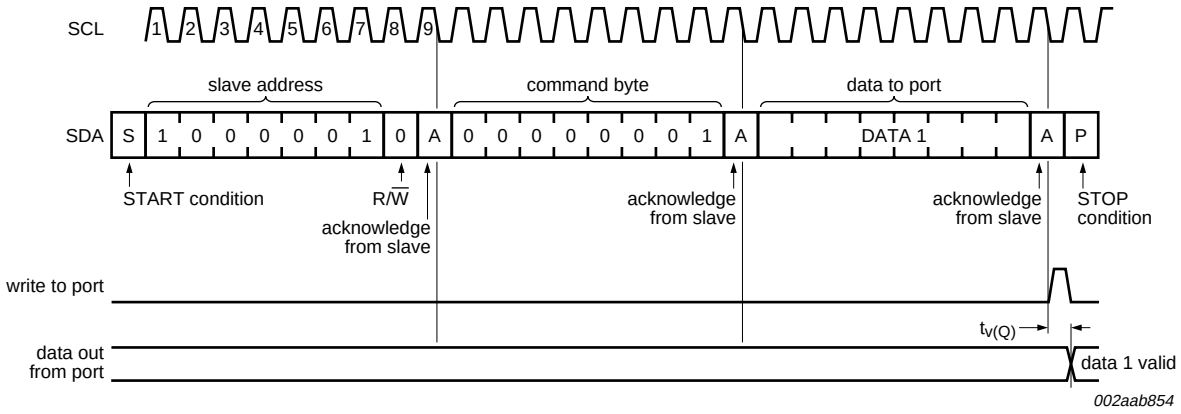


Fig 7. Write to Output Port register

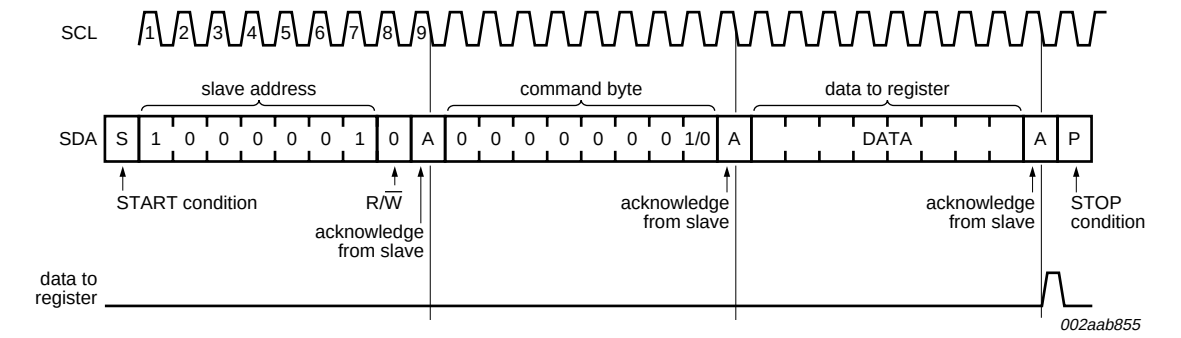


Fig 8. Write to Configuration register or Polarity Inversion register

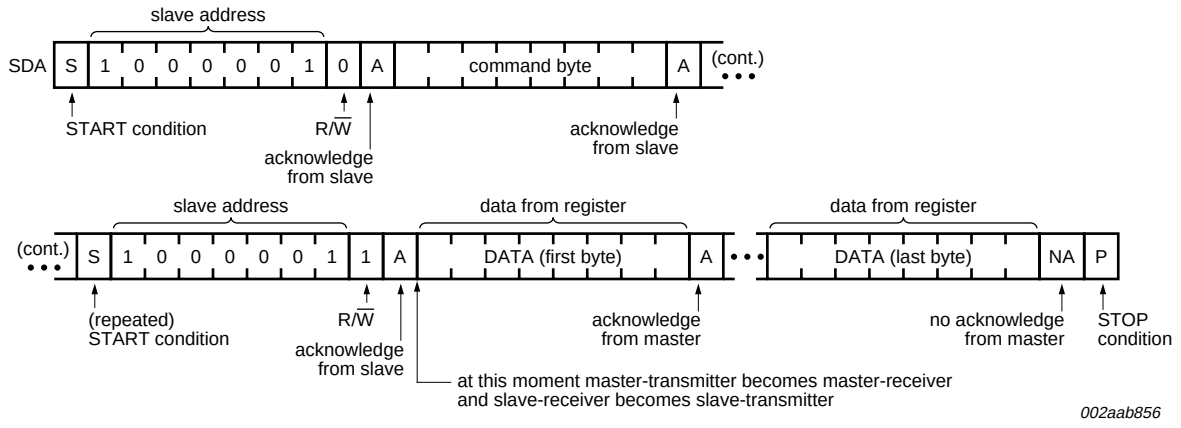
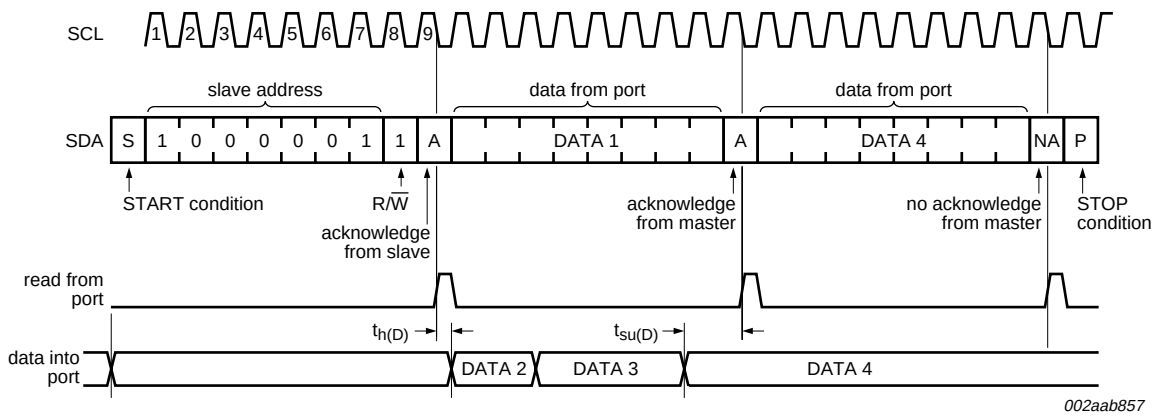


Fig 9. Read from register

© NXP B.V. 2006. All rights reserved.

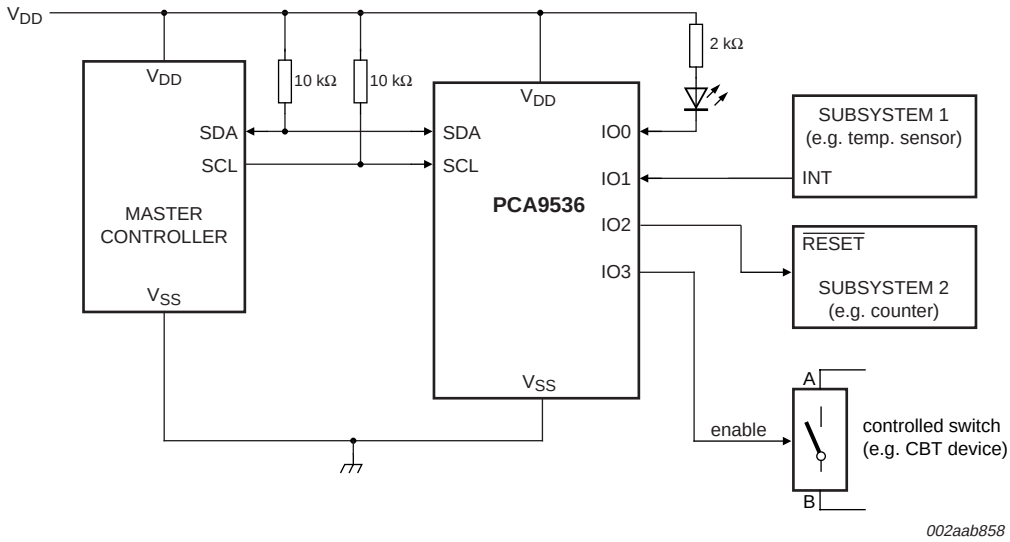


This figure assumes the command byte has previously been programmed with 00h.

Transfer of data can be stopped at any moment by a STOP condition.

Fig 10. Read Input Port register

7. Application design-in information



Device address is 1000 001X; IO0, IO2, IO3 configured as outputs; IO1 configured as input.

Fig 11. Typical application

© NXP B.V. 2006. All rights reserved.

8. Limiting values

Table 8. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	+6.0	V
I_I	input current		-	±20	mA
$V_{I/O}$	voltage on an input/output pin		V_{SS} – 0.5	5.5	V
$I_{O(IOn)}$	output current on pin IOn		-	±50	mA
I_{DD}	supply current		-	85	mA
I_{SS}	ground supply current		-	100	mA
P_{tot}	total power dissipation		-	200	mW
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	ambient temperature		–40	+85	°C
$T_{j(max)}$	maximum junction temperature		-	+125	°C

© NXP B.V. 2006. All rights reserved.

9. Static characteristics

Table 9. Static characteristics

V_{DD} = 2.3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD}	supply voltage			2.3	-	5.5	V
I_{DD}	supply current	operating mode; V_{DD} = 5.5 V; no load; f_{SCL} = 100 kHz		-	104	175	µA
I_{stb}	standby current	Standby mode; V_{DD} = 5.5 V; no load; $V_I = V_{SS}$; f_{SCL} = 0 kHz; I/O = inputs		-	225	350	µA
		Standby mode; V_{DD} = 5.5 V; no load; $V_I = V_{DD}$; f_{SCL} = 0 kHz; I/O = inputs		-	0.25	1	µA
V_{POR}	power-on reset voltage		[1]	-	1.5	1.65	V
Input SCL; input/output SDA							
V_{IL}	LOW-level input voltage			−0.5	-	$+0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		3	6	-	mA
I_L	leakage current	$V_I = V_{DD} = V_{SS}$		−1	-	+1	µA
C_i	input capacitance	$V_I = V_{SS}$		-	6	10	pF
I/Os							
V_{IL}	LOW-level input voltage			−0.5	-	+0.8	V
V_{IH}	HIGH-level input voltage			2.0	-	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.5 V; V_{DD} = 2.3 V	[2]	8	10	-	mA
		V_{OL} = 0.7 V; V_{DD} = 2.3 V	[2]	10	13	-	mA
		V_{OL} = 0.5 V; V_{DD} = 3.0 V	[2]	8	14	-	mA
		V_{OL} = 0.7 V; V_{DD} = 3.0 V	[2]	10	19	-	mA
		V_{OL} = 0.5 V; V_{DD} = 4.5 V	[2]	8	17	-	mA
		V_{OL} = 0.7 V; V_{DD} = 4.5 V	[2]	10	24	-	mA
V_{OH}	HIGH-level output voltage	I_{OH} = −8 mA; V_{DD} = 2.3 V	[3]	1.8	-	-	V
		I_{OH} = −10 mA; V_{DD} = 2.3 V	[3]	1.7	-	-	V
		I_{OH} = −8 mA; V_{DD} = 3.0 V	[3]	2.6	-	-	V
		I_{OH} = −10 mA; V_{DD} = 3.0 V	[3]	2.5	-	-	V
		I_{OH} = −8 mA; V_{DD} = 4.75 V	[3]	4.1	-	-	V
		I_{OH} = −10 mA; V_{DD} = 4.75 V	[3]	4.0	-	-	V
I_{LIH}	HIGH-level input leakage current	V_{DD} = 3.6 V; $V_I = V_{DD}$		-	-	1	µA
I_{LIL}	LOW-level input leakage current	V_{DD} = 5.5 V; $V_I = V_{SS}$		-	-	−100	µA
C_i	input capacitance			-	3.7	5	pF
C_o	output capacitance			-	3.7	5	pF

[1] V_{DD} must be lowered to 0.2 V in order to reset part.

[2] Each I/O must be externally limited to a maximum of 25 mA and the device must be limited to a maximum current of 100 mA.

[3] The total current sourced by all I/Os must be limited to 85 mA.

© NXP B.V. 2006. All rights reserved.

10. Dynamic characteristics

Table 10. Dynamic characteristics

Symbol	Parameter	Conditions	Standard-mode I²C-bus		Fast-mode I²C-bus		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	100	0	400	kHz
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		4.0	-	0.6	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	µs
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	0.6	-	µs
$t_{HD;DAT}$	data hold time		0	-	0	-	µs
$t_{VD;ACK}$	data valid acknowledge time	[1]	0.3	3.45	0.1	0.9	µs
$t_{VD;DAT}$	data valid time	[2]	300	-	50	-	ns
$t_{SU;DAT}$	data set-up time		250	-	100	-	ns
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	µs
t_r	rise time of both SDA and SCL signals		-	1000	$20 + 0.1C_b$ [3]	300	ns
t_f	fall time of both SDA and SCL signals		-	300	$20 + 0.1C_b$ [3]	300	µs
t_{SP}	pulse width of spikes that must be suppressed by the input filter		-	50	-	50	ns
Port timing							
$t_{v(Q)}$	data output valid time		-	200	-	200	ns
$t_{su(D)}$	data input setup time		100	-	100	-	ns
$t_{h(D)}$	data input hold time		1	-	1	-	µs

[1] $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.

[2] $t_{VD;DAT}$ = minimum time for SDA data output to be valid following SCL LOW.

[3] C_b = total capacitance of one bus line in pF.

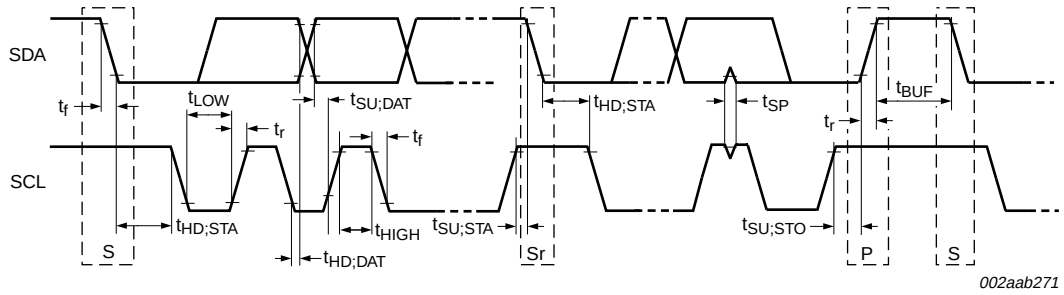
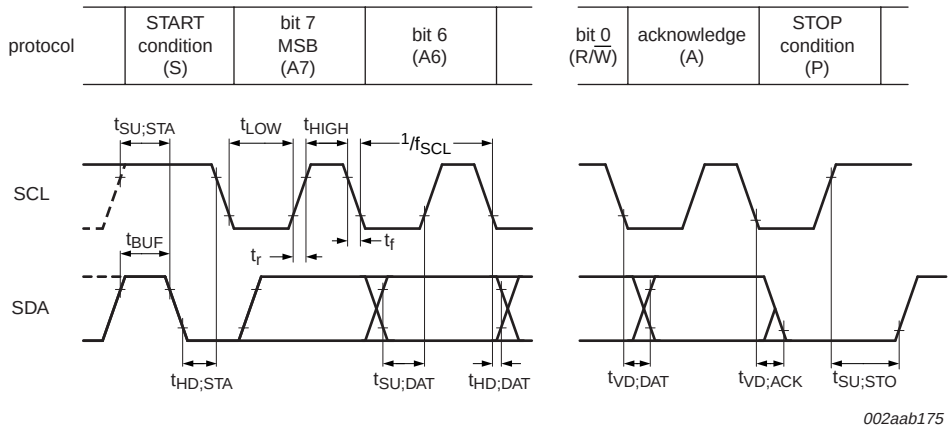


Fig 12. Definition of timing

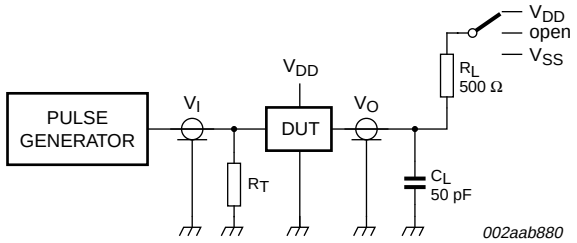
© NXP B.V. 2006. All rights reserved.



Rise and fall times refer to V_{IL} and V_{IH}

Fig 13. I²C-bus timing diagram

11. Test information



R_L = load resistor.

C_L = load capacitance includes jig and probe capacitance.

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generators.

Fig 14. Test circuitry for switching times

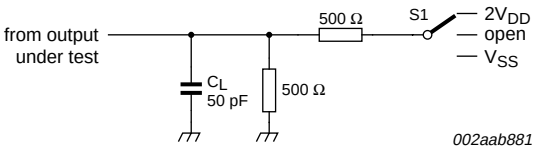


Fig 15. Test circuit

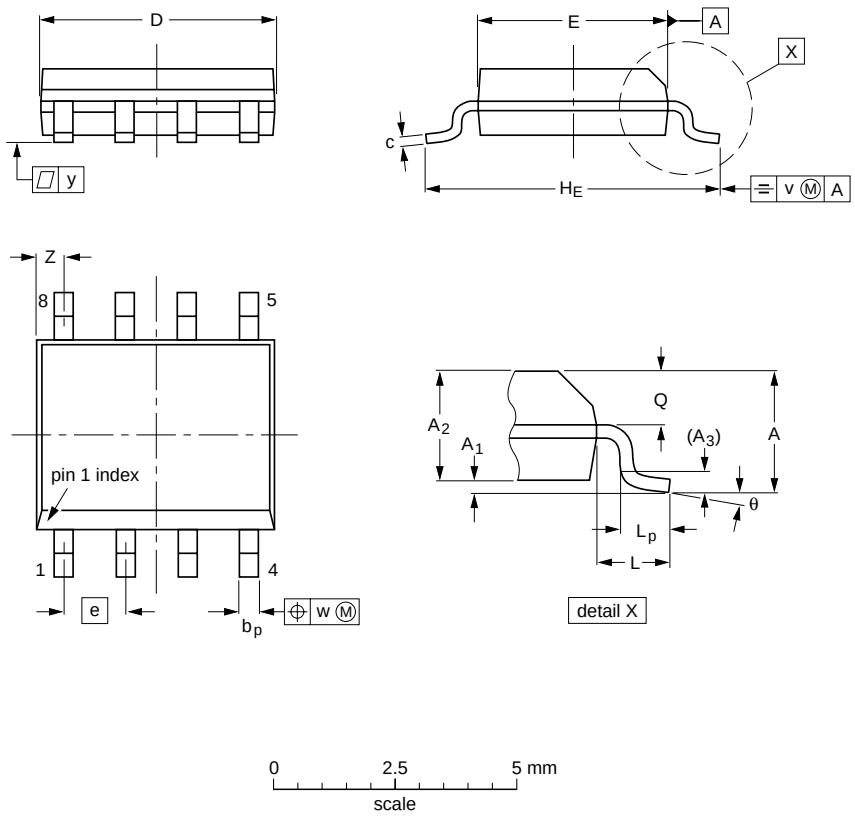
Table 11. Test data

Test	Load		Switch
	C_L	R_L	
$t_{v(Q)}$	50 pF	500 Ω	$2V_{DD}$

© NXP B.V. 2006. All rights reserved.

12. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

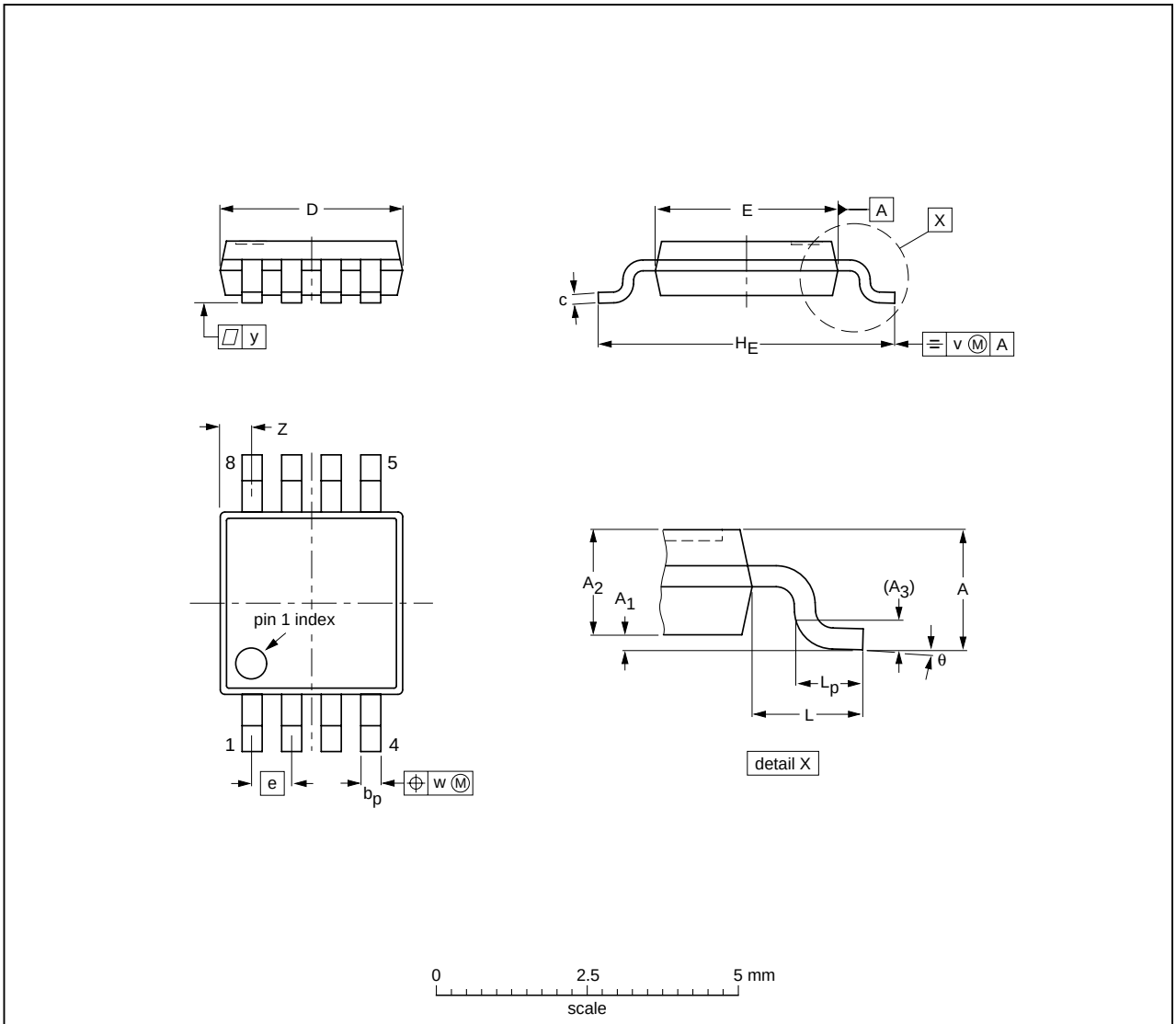
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 16. Package outline SOT96-1 (SO8)

© NXP B.V. 2006. All rights reserved.

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

Notes

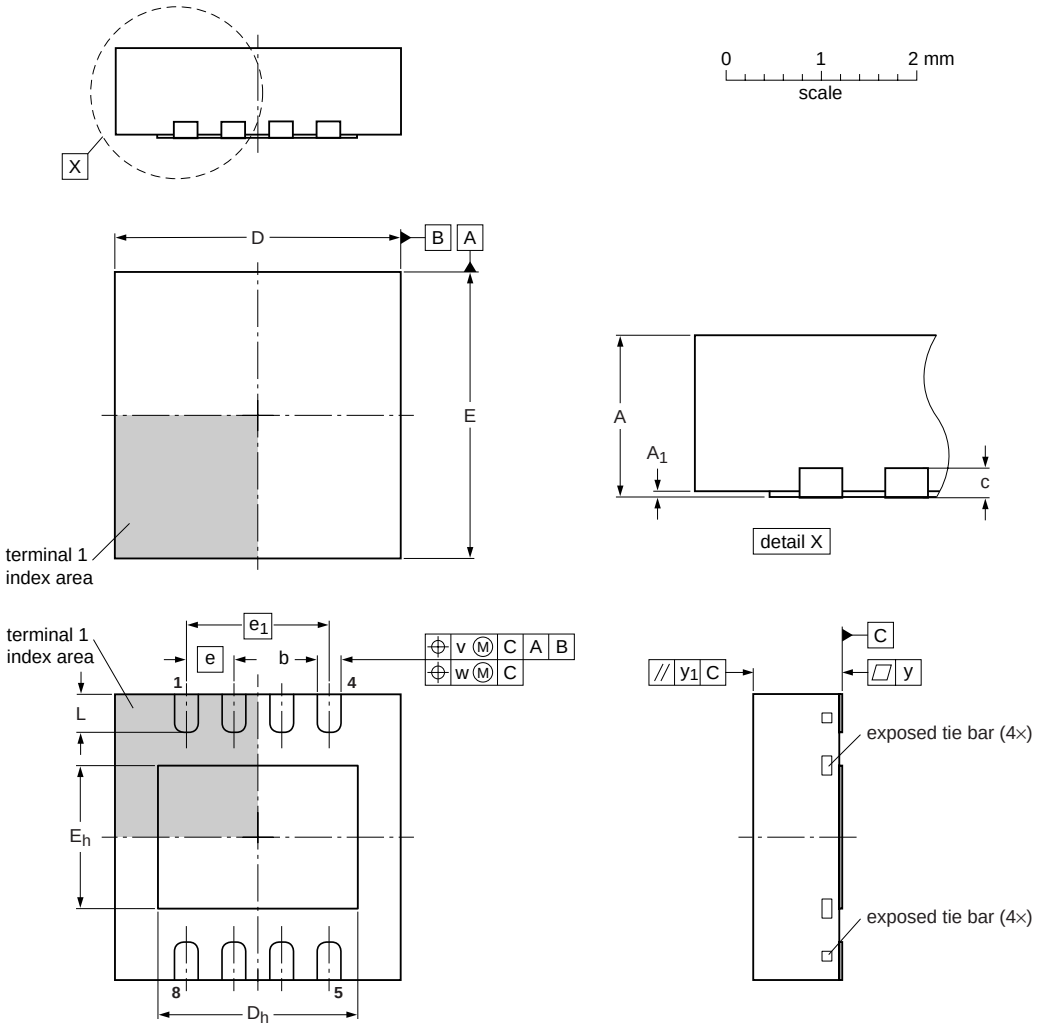
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-1						~~99-04-09~~ 03-02-18

Fig 17. Package outline SOT505-1 (TSSOP8)

© NXP B.V. 2006. All rights reserved.

HVSON8: plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 x 3 x 0.85 mm **SOT908-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.3 0.2	0.2	3.1 2.9	2.25 1.95	3.1 2.9	1.65 1.35	0.5	1.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT908-1		MO-229				~~05-09-26~~ 05-10-05

Fig 18. Package outline SOT908-1 (HVSON8)

© NXP B.V. 2006. All rights reserved.

13. Handling information

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe you must take normal precautions appropriate to handling integrated circuits.

14. Soldering

14.1 Introduction to soldering surface mount packages

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

14.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow temperatures range from 215 °C to 260 °C depending on solder paste material. The peak top-surface temperature of the packages should be kept below:

Table 12. SnPb eutectic process - package peak reflow temperatures (from *J-STD-020C*)

Package thickness	Volume mm^3 < 350	Volume mm^3 ≥ 350
< 2.5 mm	240 °C + 0/–5 °C	225 °C + 0/–5 °C
≥ 2.5 mm	225 °C + 0/–5 °C	225 °C + 0/–5 °C

Table 13. Pb-free process - package peak reflow temperatures (from *J-STD-020C*)

Package thickness	Volume mm^3 < 350	Volume mm^3 350 to 2000	Volume mm^3 > 2000
< 1.6 mm	260 °C + 0 °C	260 °C + 0 °C	260 °C + 0 °C
1.6 mm to 2.5 mm	260 °C + 0 °C	250 °C + 0 °C	245 °C + 0 °C
≥ 2.5 mm	250 °C + 0 °C	245 °C + 0 °C	245 °C + 0 °C

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

14.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

© NXP B.V. 2006. All rights reserved.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

14.5 Package related soldering information

Table 14. Suitability of surface mount IC packages for wave and reflow soldering

Package[1]	Soldering method	
	Wave	Reflow[2]
BGA, HTSSON..T[3], LBGA, LFBGA, SQFP, SSOP..T[3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
CWQCCN..L[8], PMFP[9], WQCCN..L[8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your NXP Semiconductors sales office.

© NXP B.V. 2006. All rights reserved.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

15. Abbreviations

Table 15. Abbreviations

Acronym	Description
ACPI	Advanced Configuration and Power Interface
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
GPIO	General Purpose Input/Output
HBM	Human Body Model
I²C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
LED	Light-Emitting Diode
MM	Machine Model
POR	Power-On Reset
SMBus	System Management Bus

© NXP B.V. 2006. All rights reserved.

16. Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9536_3	20061009	Product data sheet	-	PCA9536_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • pin names I/O0, I/O1, I/O2, I/O3 changed to IO0, IO1, IO2, IO3 • pin name GND changed to V_{SS} • added HVSON8 package • Figure 5 “Simplified schematic of IO0 to IO3” modified: removed ESD protection diodes • symbol (t_{pv} and t_{PV}) changed to $t_{v(Q)}$ • symbol (t_{ph} and t_{PH}) changed to $t_{h(D)}$ • symbol (t_{ps} and t_{PS}) changed to $t_{su(D)}$ • Table 9 “Static characteristics” – sub-section “Input SCL; input/output SDA”, symbol I_{OL}: minimum value changed from “tbd” to 6 mA – sub-section “I/Os”: changed symbol/parameter “I_{IH}, input leakage current” to “I_{LIH}, HIGH-level input leakage current” – sub-section “I/Os”: changed symbol/parameter “I_{IL}, input leakage current” to “I_{LIL}, LOW-level input leakage current” • added Section 15 “Abbreviations”			
PCA9536_2 (9397 750 14124)	20040930	Objective data sheet	-	PCA9536_1
PCA9536_1 (9397 750 12895)	20040820	Objective data sheet	-	-

© NXP B.V. 2006. All rights reserved.

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

17.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

17.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of a NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

17.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

I²C-bus — logo is a trademark of NXP B.V.

18. Contact information

For additional information, please visit: **http://www.nxp.com**

For sales office addresses, send an email to: **salesaddresses@nxp.com**

© NXP B.V. 2006. All rights reserved.

19. Contents

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2006. **All rights reserved.**

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 9 October 2006
Document identifier: PCA9536_3

founded by

PHILIPS