

OPA2314-Q1 3-MHz, Low-Power, Low-Noise, RRIO, 1.8-V CMOS Operational Amplifier

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
 - Device Temperature Grade : -40°C to 125°C Ambient Operating Temperature Range
 - Device HBM Classification Level 2
 - Device CDM Classification Level C6
- Low I_Q : 150 $\mu\text{A}/\text{ch}$
- Wide Supply Range: 1.8 V to 5.5 V
- Low Noise: 14 $\text{nV}/\sqrt{\text{Hz}}$ at 1 kHz
- Gain Bandwidth: 3 MHz
- Low Input Bias Current: 0.2 pA
- Low Offset Voltage: 0.5 mV
- Unity-Gain Stable
- Internal RF/EMI Filter
- Specified Temperature Range: -40°C to 125°C

2 Applications

- Battery-Powered Instruments:
 - Consumer, Industrial, Medical
 - Notebooks, Portable Media Players
- Photodiode Amplifiers
- Active Filters
- Remote Sensing
- Wireless Metering
- Handheld Test Equipment

3 Description

The OPA2314-Q1 device is a dual-channel operational amplifier (op-amp) that represents a new generation of low-power, general-purpose CMOS amplifiers. Rail-to-rail input and output swings, low quiescent current (150 μA typ at 5 V_S) combined with a wide bandwidth of 3 MHz, and very low noise (14 $\text{nV}/\sqrt{\text{Hz}}$ at 1 kHz) make this device very attractive for a variety of battery-powered applications that require a good balance between cost and performance. The low input bias current supports applications with mega-ohm source impedances.

The robust design of the OPA2314-Q1 device provides ease-of-use to the circuit designer: unity-gain stability with capacitive loads of up to 300 pF, an integrated RF/EMI rejection filter, no phase reversal in overdrive conditions, and high electrostatic discharge (ESD) protection (4-kV HBM).

The device is optimized for low-voltage operation as low as 1.8 V (± 0.9 V) and up to 5.5 V (± 2.75 V), and is specified over the full extended temperature range of -40°C to 125°C .

The device is offered in an SO-8 package.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA2314-Q1	SOIC (8)	4.90 mm x 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

EMIRR vs Frequency

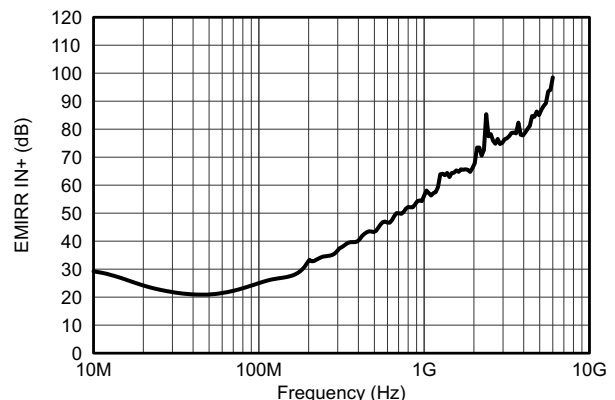


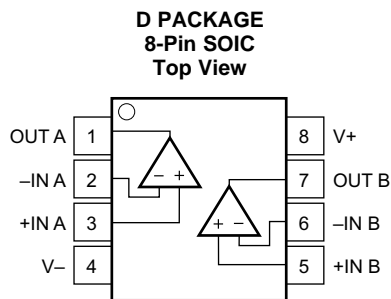
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4 Revision History

Changes from Original (December 2014) to Revision A	Page
• Changed the device status from <i>Product Preview</i> to <i>Production Data</i>	1

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN A	3	I	Noninverting input, channel A
-IN A	2	I	Inverting input, channel A
+IN B	5	I	Noninverting input, channel B
-IN B	6	I	Inverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V+	8	—	Positive (highest) power supply
V-	4	—	Negative (lowest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

	MIN	MAX	UNIT
Supply voltage		7	V
Voltage ⁽²⁾	Signal input terminals	(V-) - 0.5 (V+) + 0.5	V
Current ⁽²⁾	Signal input terminals	±10	mA
Output short-circuit ⁽³⁾		Continuous	mA
Operating temperature, T _A	-40	150	°C
Junction temperature, T _J		150	°C
Storage temperature, T _{stg}	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less.
- (3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

	VALUE	UNIT
V _(ESD)	Electrostatic discharge	
	Human body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000
	Charged device model (CDM), per AEC Q100-011	±1000

- (1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage	1.8 (± 0.9)		5.5 (± 2.75)	V
T_A	Ambient operating temperature	-40		125	$^{\circ}\text{C}$

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		D 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	138.4	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	89.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	78.6	
Ψ_{JT}	Junction-to-top characterization parameter	29.9	
Ψ_{JB}	Junction-to-board characterization parameter	78.1	

 (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

 At $T_A = 25^{\circ}\text{C}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$, $V_S = 1.8\text{ V}$ to 5.5 V , unless otherwise noted. The phrase *over temperature* refers to values over the specified temperature range of $T_A = -40^{\circ}\text{C}$ to 125°C .⁽¹⁾

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE					
V_{OS}	Input offset voltage $V_{CM} = (V_{S+}) - 1.3\text{ V}$		0.5	2.5	mV
dV_{OS}/dT	Input offset voltage vs temperature		1		$\mu\text{V}/^{\circ}\text{C}$
PSRR	vs power supply $V_{CM} = (V_{S+}) - 1.3\text{ V}$	78	92		dB
	Input offset voltage over temperature	74			dB
	Channel separation, DC		10		$\mu\text{V}/\text{V}$
INPUT VOLTAGE RANGE					
V_{CM}	Common-mode voltage range	$(V_-) - 0.2$		$(V_+) + 0.2$	V
CMRR	Common-mode rejection ratio	$V_S = 1.8\text{ V}$ to 5.5 V , $(V_{S-}) - 0.2\text{ V} < V_{CM} < (V_{S+}) - 1.3\text{ V}$	75	96	dB
		$V_S = 5.5\text{ V}$, $V_{CM} = -0.2\text{ V}$ to $5.7\text{ V}^{(2)}$	66	80	dB
	Common-mode rejection ratio over temperature	$V_S = 1.8\text{ V}$, $(V_{S-}) - 0.2\text{ V} < V_{CM} < (V_{S+}) - 1.3\text{ V}$	70	86	dB
		$V_S = 5.5\text{ V}$, $(V_{S-}) - 0.2\text{ V} < V_{CM} < (V_{S+}) - 1.3\text{ V}$	73	90	dB
		$V_S = 5.5\text{ V}$, $V_{CM} = -0.2\text{ V}$ to $5.7\text{ V}^{(2)}$	60		dB
INPUT BIAS CURRENT					
I_B	Input bias current		± 0.2	± 10	pA
	Input bias current over temperature			± 600	pA
I_{OS}	Input offset current		± 0.2	± 10	pA
	Input offset current over temperature			± 600	pA
NOISE					
	Input voltage noise (peak-to-peak)	$f = 0.1\text{ Hz}$ to 10 Hz	5		μV_{PP}
e_n	Input voltage noise density	$f = 10\text{ kHz}$	13		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$	14		$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input current noise density	$f = 1\text{ kHz}$	5		$\text{fA}/\sqrt{\text{Hz}}$

- Parameters with minimum or maximum specification limits are 100% production tested at 25°C , unless otherwise noted. Over temperature limits are based on characterization and statistical analysis.
- Specified by design and characterization; not production tested.

Electrical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$, $V_S = 1.8\text{ V}$ to 5.5 V , unless otherwise noted. The phrase *over temperature* refers to values over the specified temperature range of $T_A = -40^\circ\text{C}$ to 125°C .⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CAPACITANCE						
C_{IN}	Differential	$V_S = 5\text{ V}$		1		pF
	Common-mode	$V_S = 5\text{ V}$		5		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	$V_S = 1.8\text{ V}$, $0.2\text{ V} < V_O < (V+) - 0.2\text{ V}$, $R_L = 10\text{ k}\Omega$	90	115		dB
		$V_S = 5.5\text{ V}$, $0.2\text{ V} < V_O < (V+) - 0.2\text{ V}$, $R_L = 10\text{ k}\Omega$	100	128		dB
		$V_S = 1.8\text{ V}$, $0.5\text{ V} < V_O < (V+) - 0.5\text{ V}$, $R_L = 2\text{ k}\Omega$ ⁽²⁾	90	100		dB
		$V_S = 5.5\text{ V}$, $0.5\text{ V} < V_O < (V+) - 0.5\text{ V}$, $R_L = 2\text{ k}\Omega$ ⁽²⁾	94	110		dB
	Open-loop voltage gain Over temperature	$V_S = 5.5\text{ V}$, $0.2\text{ V} < V_O < (V+) - 0.2\text{ V}$, $R_L = 10\text{ k}\Omega$	90	110		dB
		$V_S = 5.5\text{ V}$, $0.5\text{ V} < V_O < (V+) - 0.2\text{ V}$, $R_L = 2\text{ k}\Omega$		100		dB
	Phase margin	$V_S = 5\text{ V}$, $G = +1$, $R_L = 10\text{ k}\Omega$		65		deg
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	$V_S = 1.8\text{ V}$, $R_L = 10\text{ k}\Omega$, $C_L = 10\text{ pF}$		2.7		MHz
		$V_S = 5\text{ V}$, $R_L = 10\text{ k}\Omega$, $C_L = 10\text{ pF}$		3		MHz
SR	Slew rate ⁽³⁾	$V_S = 5\text{ V}$, $G = +1$		1.5		V/ μs
t_S	Settling time	To 0.1%, $V_S = 5\text{ V}$, 2-V step, $G = 1$		2.3		μs
		To 0.01%, $V_S = 5\text{ V}$, 2-V step, $G = 1$		3.1		μs
	Overload recovery time	$V_S = 5\text{ V}$, $V_{IN} \times \text{Gain} > V_S$		5.2		μs
THD+N	Total harmonic distortion + noise ⁽⁴⁾	$V_S = 5\text{ V}$, $V_O = 1\text{ V}_{RMS}$, $G = 1$, $f = 1\text{ kHz}$, $R_L = 10\text{ k}\Omega$		0.001%		
OUTPUT						
V_O	Voltage output swing from supply rails	$V_S = 1.8\text{ V}$, $R_L = 10\text{ k}\Omega$		5	15	mV
		$V_S = 5.5\text{ V}$, $R_L = 10\text{ k}\Omega$		5	20	mV
		$V_S = 1.8\text{ V}$, $R_L = 2\text{ k}\Omega$		15	30	mV
		$V_S = 5.5\text{ V}$, $R_L = 2\text{ k}\Omega$		22	40	mV
	Voltage output swing from supply rails over temperature	$V_S = 5.5\text{ V}$, $R_L = 10\text{ k}\Omega$			30	mV
		$V_S = 5.5\text{ V}$, $R_L = 2\text{ k}\Omega$		60		mV
I_{SC}	Short-circuit current	$V_S = 5\text{ V}$		± 20		mA
R_O	Open-loop output impedance	$V_S = 5.5\text{ V}$, $f = 100\text{ Hz}$		570		Ω
POWER SUPPLY						
V_S	Specified voltage range		1.8		5.5	V
I_Q	Quiescent current per amplifier	$V_S = 1.8\text{ V}$, $I_O = 0\text{ mA}$		130	180	μA
		$V_S = 5\text{ V}$, $I_O = 0\text{ mA}$		150	190	μA
	Quiescent current per amplifier over temperature	$V_S = 5\text{ V}$, $I_O = 0\text{ mA}$			220	μA
	Power-on time	$V_S = 0\text{ V}$ to 5 V , to 90% I_Q level		44		μs
TEMPERATURE						
	Specified range		-40		125	$^\circ\text{C}$
	Operating range		-40		150	$^\circ\text{C}$
	Storage range		-65		150	$^\circ\text{C}$

(3) Signifies the slower value of the positive or negative slew rate.

(4) Third-order filter; bandwidth = 80 kHz at -3 dB.

6.6 Typical Characteristics

At $T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

Table 1. Characteristic Performance Measurements

TITLE	FIGURE
Open-Loop Gain and Phase vs Frequency	Figure 1
Open-Loop Gain vs Temperature	Figure 2
Quiescent Current vs Supply Voltage	Figure 3
Quiescent Current vs Temperature	Figure 4
Offset Voltage Production Distribution	Figure 5
Offset Voltage Drift Distribution	Figure 6
Offset Voltage vs Common-Mode Voltage (Maximum Supply)	Figure 7
Offset Voltage vs Temperature	Figure 8
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CMRR and PSRR vs Temperature	Figure 10
0.1-Hz to 10-Hz Input Voltage Noise (5.5 V)	Figure 11
Input Voltage Noise Spectral Density vs Frequency (1.8 V, 5.5 V)	Figure 12
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THD+N vs Amplitude ($G = -1, 2\text{ k}\Omega, 10\text{ k}\Omega$)	Figure 30
THD+N vs Frequency ($0.5\text{ V}_{RMS}, G = +1, 2\text{ k}\Omega, 10\text{ k}\Omega$)	Figure 31
EMIRR	Figure 32

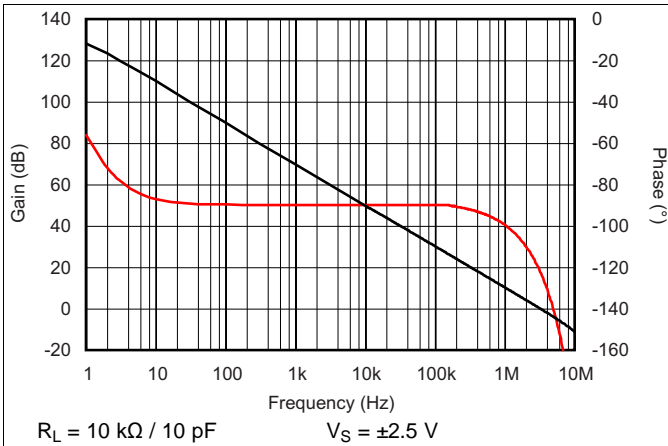


Figure 1. Open-loop Gain and Phase vs Frequency

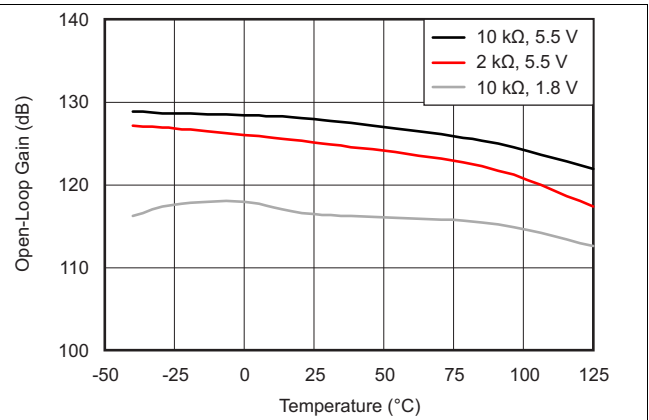


Figure 2. Open-Loop Gain vs Temperature

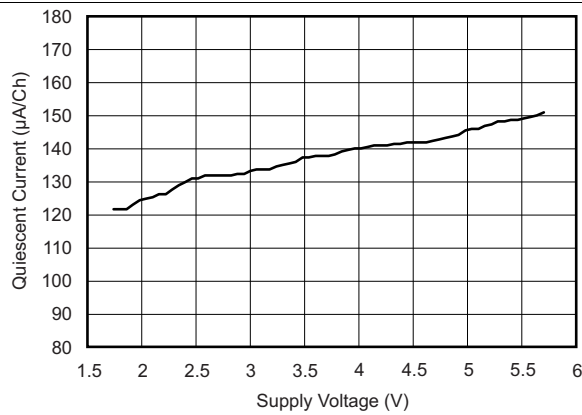


Figure 3. Quiescent Current vs Supply

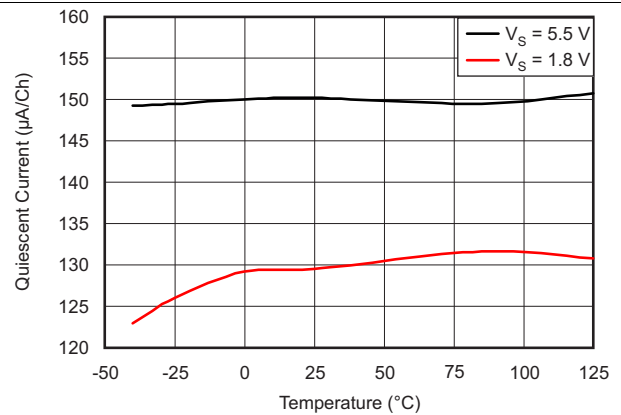


Figure 4. Quiescent Current vs Temperature

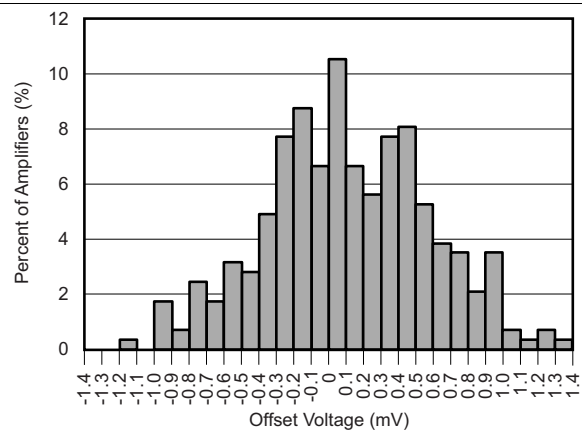


Figure 5. Offset Voltage Production Distribution

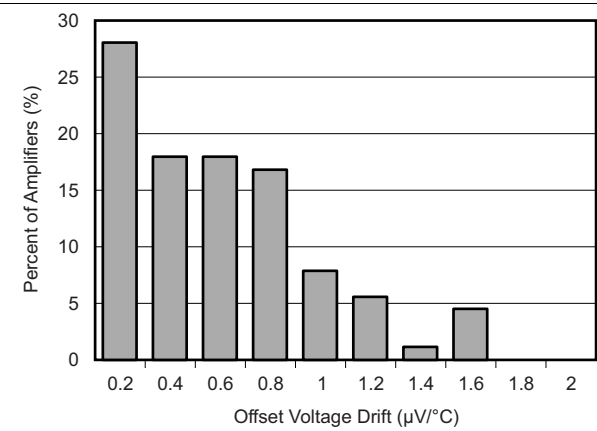


Figure 6. Offset Voltage Drift Distribution

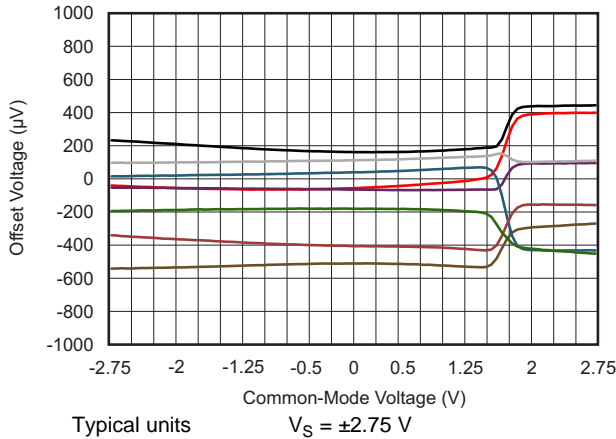


Figure 7. Offset Voltage vs Common-mode Voltage

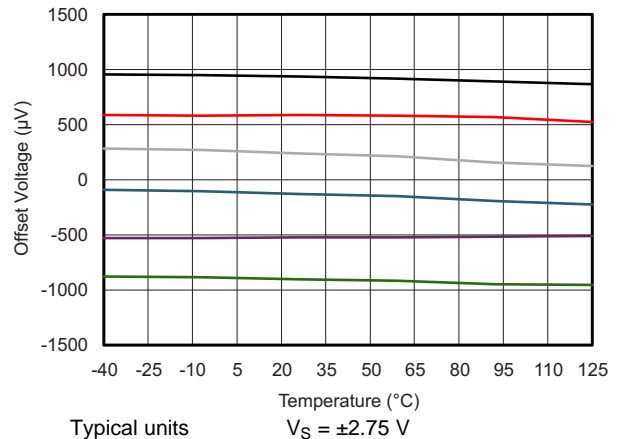


Figure 8. Offset Voltage vs Temperature

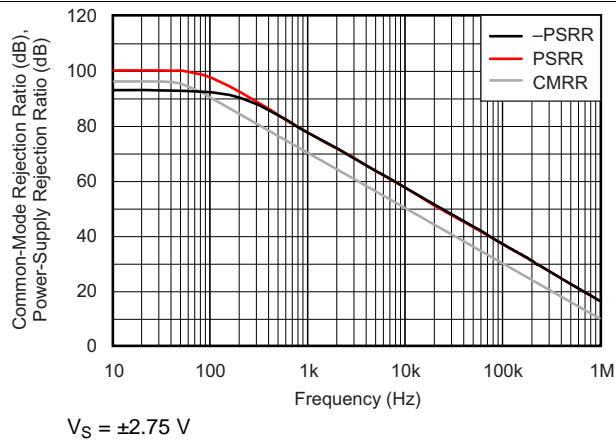


Figure 9. CMRR and PSRR vs Frequency (Referred-to-Input)

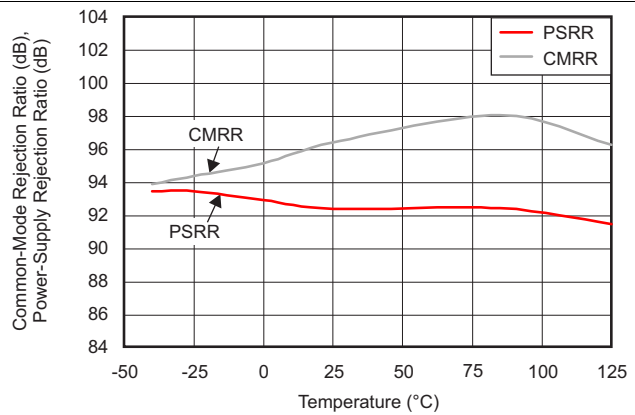


Figure 10. CMRR and PSRR vs Temperature

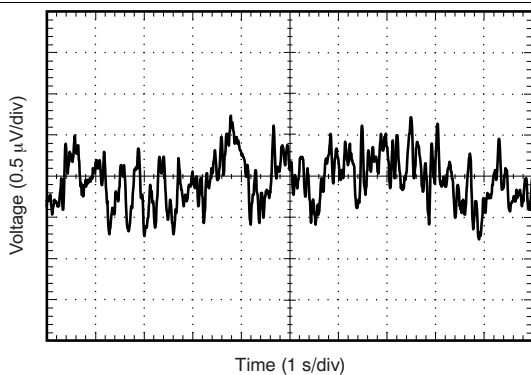


Figure 11. 0.1-Hz to 10-Hz Input Voltage Noise

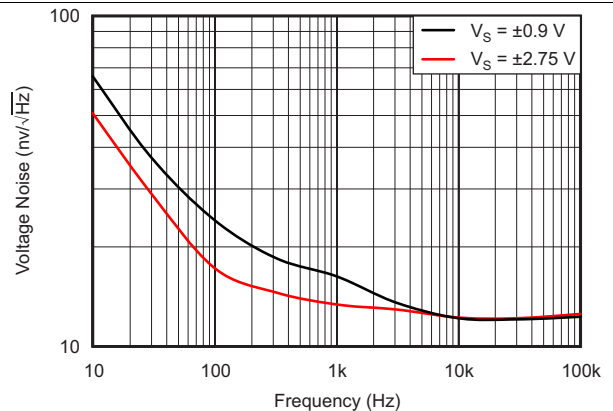


Figure 12. Input Voltage Noise Spectral Density vs Frequency

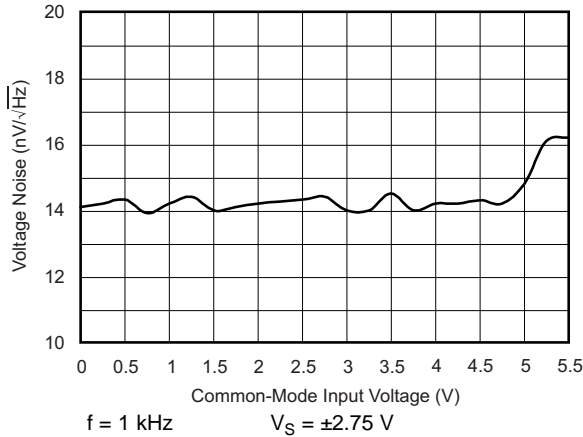


Figure 13. Voltage Noise vs Common-Mode Voltage

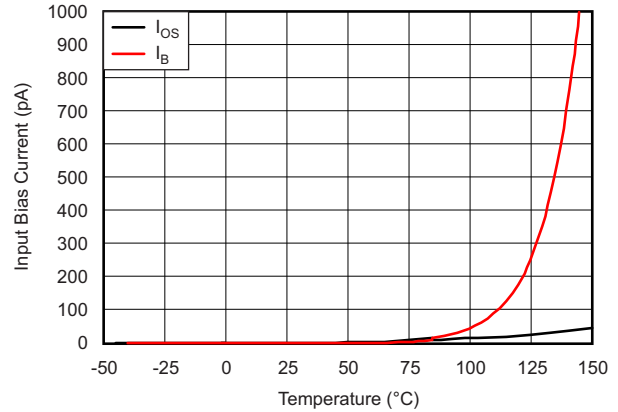


Figure 14. Input Bias and Offset Current vs Temperature

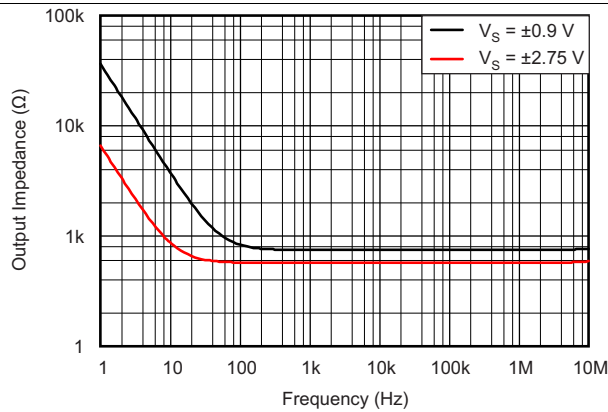
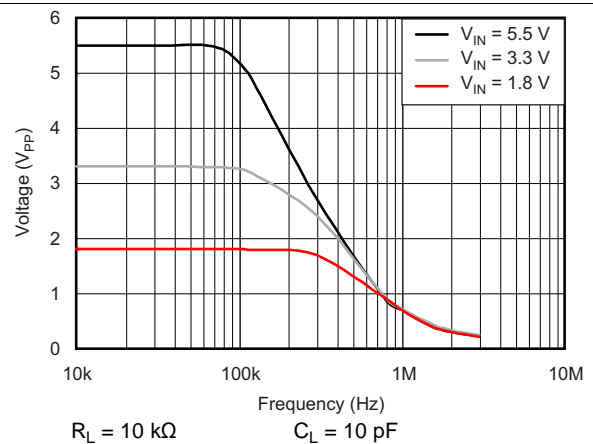
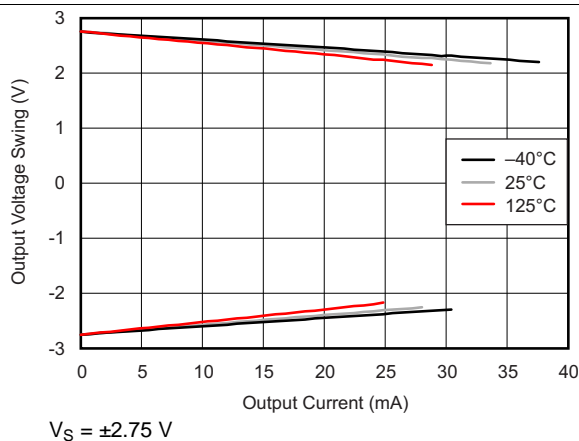


Figure 15. Open-Loop Output Impedance vs Frequency



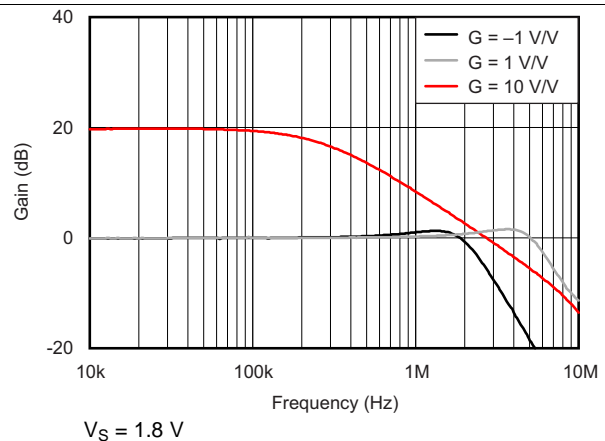
$R_L = 10\text{ k}\Omega$ $C_L = 10\text{ pF}$

Figure 16. Maximum Output Voltage vs Frequency and Supply Voltage



$V_S = \pm 2.75\text{ V}$

Figure 17. Output Voltage Swing vs Output Current (Over Temperature)



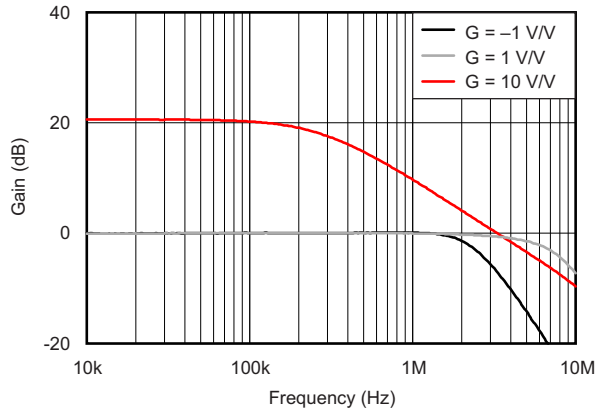
$V_S = 1.8\text{ V}$

Figure 18. Closed-Loop Gain vs Frequency

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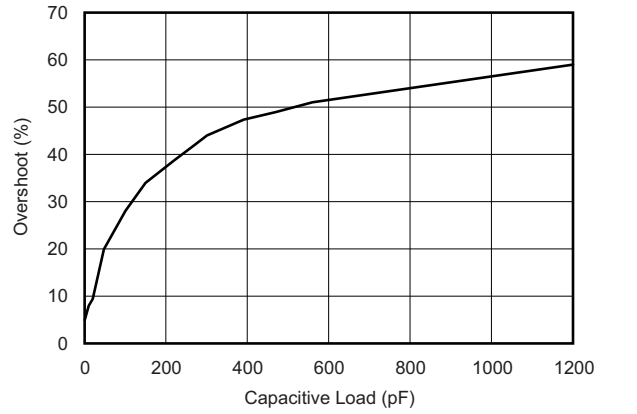
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$V_S = 5.5\text{ V}$

Figure 19. Closed-Loop Gain vs Frequency

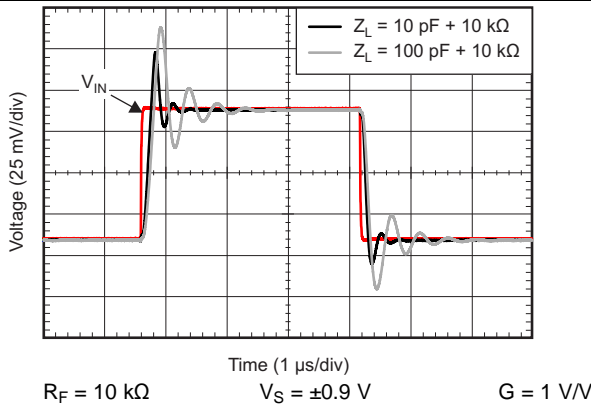


$R_L = 10\text{ k}\Omega$

$V_S = \pm 2.75\text{ V}$

$G = 1\text{ V/V}$

Figure 20. Small-Signal Overshoot vs Load Capacitance

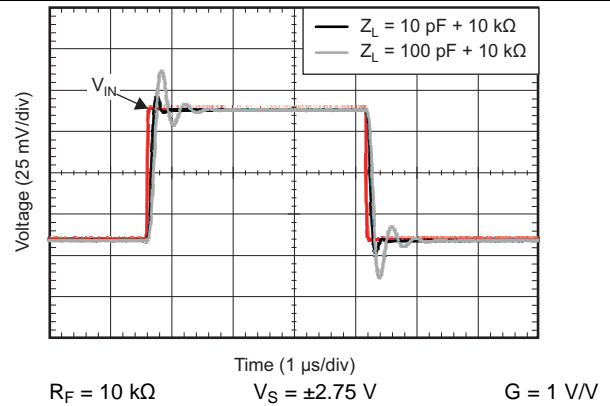


$R_F = 10\text{ k}\Omega$

$V_S = \pm 0.9\text{ V}$

$G = 1\text{ V/V}$

Figure 21. Small-Signal Pulse Response (Noninverting)

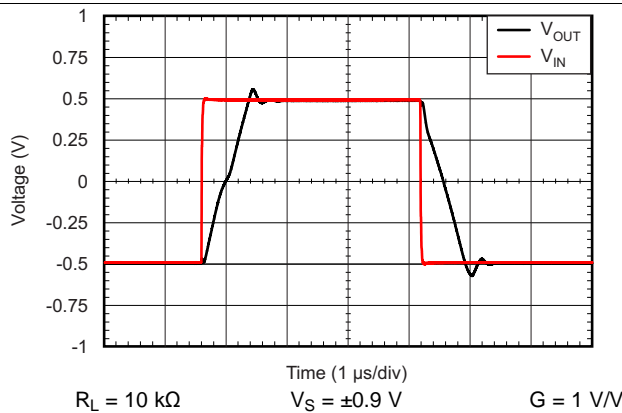


$R_F = 10\text{ k}\Omega$

$V_S = \pm 2.75\text{ V}$

$G = 1\text{ V/V}$

Figure 22. Small-Signal Pulse Response (Inverting)

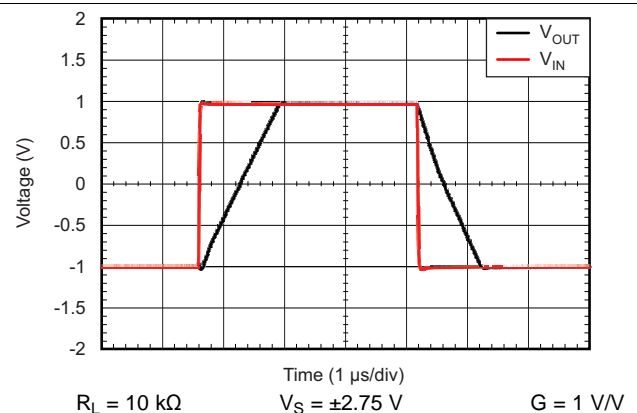


$R_L = 10\text{ k}\Omega$

$V_S = \pm 0.9\text{ V}$

$G = 1\text{ V/V}$

Figure 23. Large-Signal Pulse Response (Noninverting)



$R_L = 10\text{ k}\Omega$

$V_S = \pm 2.75\text{ V}$

$G = 1\text{ V/V}$

Figure 24. Large-Signal Pulse Response (Inverting)

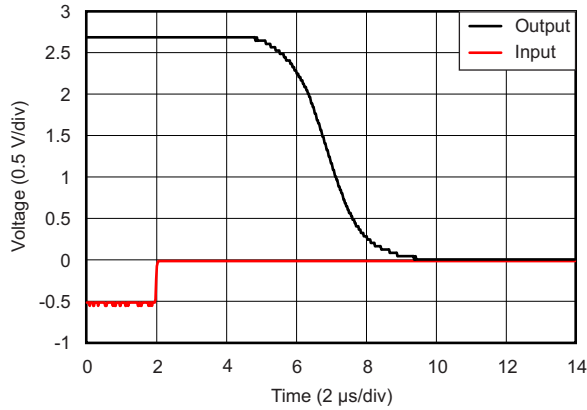


Figure 25. Positive Overload Recovery

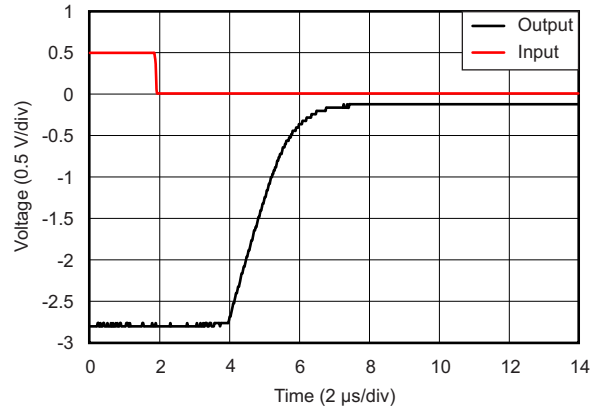


Figure 26. Negative Overload Recovery

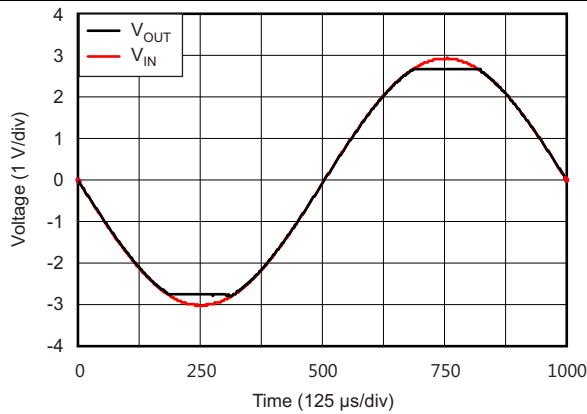


Figure 27. No Phase Reversal

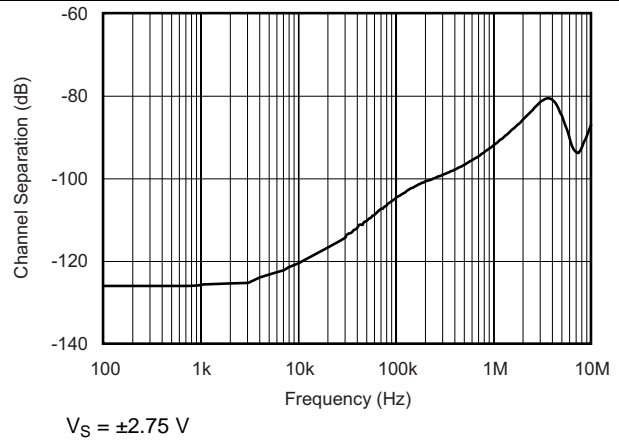


Figure 28. Channel Separation vs Frequency

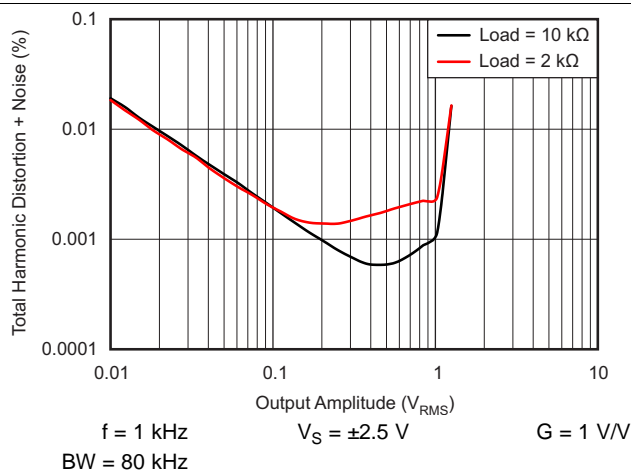


Figure 29. THD+N vs Output Amplitude (G = 1 V/V)

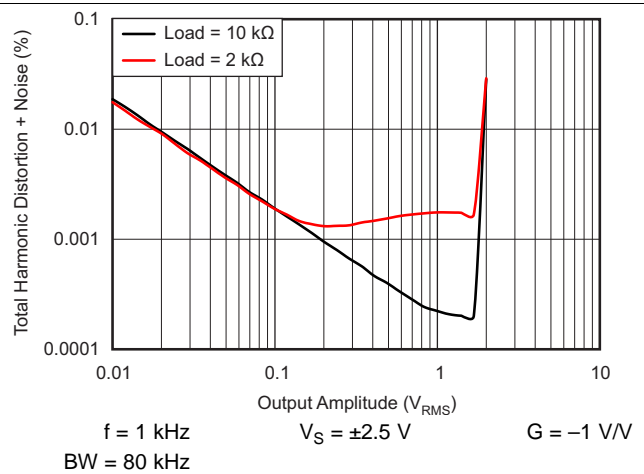
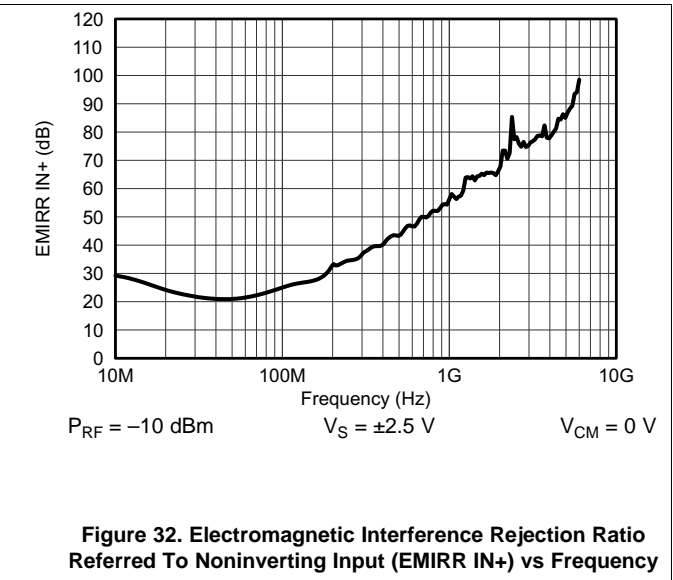
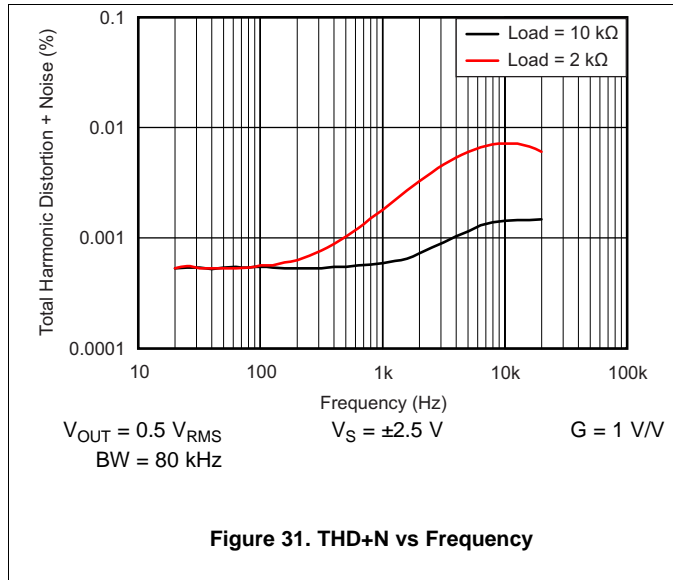


Figure 30. THD+N vs Output Amplitude (G = -1 V/V)

OPA2314-Q1

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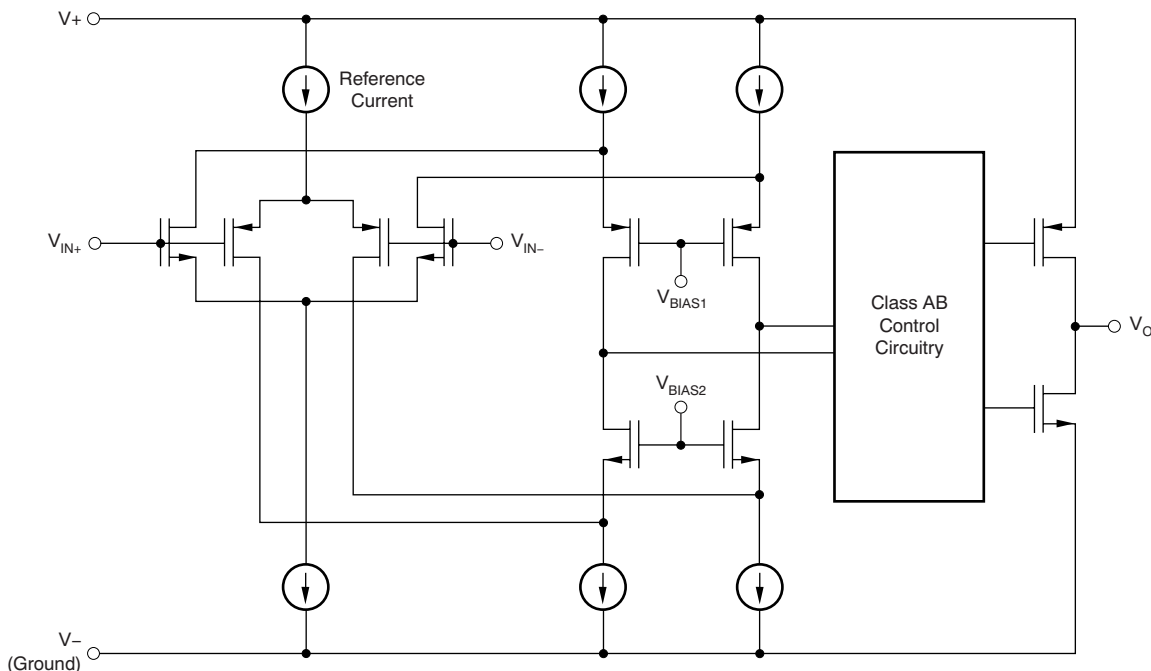


7 Detailed Description

7.1 Overview

The OPA314-Q1 is a family of low-power, rail-to-rail input and output operational amplifiers. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and are suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving $\leq 10\text{-k}\Omega$ loads connected to any point between V_+ and ground. The input common-mode voltage range includes both rails and allows the OPA314 series to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes them ideal for driving sampling analog-to-digital converters (ADCs).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Voltage

The OPA2314-Q1 op-amp is fully specified and ensured for operation from 1.8 V to 5.5 V. In addition, many specifications apply from -40°C to 125°C . Parameters that vary significantly with operating voltages or temperature are shown in the [Typical Characteristics](#) section. Power-supply pins should be bypassed with 0.01- μF ceramic capacitors.

7.3.2 Rail-to-Rail Input

The input common-mode voltage range of the OPA2314-Q1 device extends 200 mV beyond the supply rails. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair. The N-channel pair is active for input voltages close to the positive rail, typically $(V_+) - 1.3\text{ V}$ to 200 mV above the positive supply. The P-channel pair is on for inputs from 200 mV below the negative supply to approximately $(V_+) - 1.3\text{ V}$. A small transition region exists, typically $(V_+) - 1.4\text{ V}$ to $(V_+) - 1.2\text{ V}$, in which both pairs are on. This 200-mV transition region can vary up to 300 mV with process variation. Thus, the transition region (both stages on) can range from $(V_+) - 1.7\text{ V}$ to $(V_+) - 1.5\text{ V}$ on the low end, up to $(V_+) - 1.1\text{ V}$ to $(V_+) - 0.9\text{ V}$ on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD may be degraded compared to device operation outside this region.

Feature Description (continued)

7.3.3 Input and ESD Protection

The OPA2314-Q1 device incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in the [Absolute Maximum Ratings](#) table. [Figure 33](#) shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value should be kept to a minimum in noise-sensitive applications.

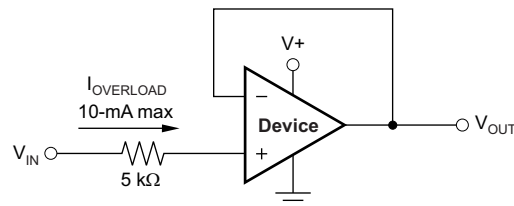


Figure 33. Input Current Protection

7.3.4 Common-Mode Rejection Ratio (CMRR)

CMRR for the OPA2314-Q1 device is specified in several ways so the best match for a given application may be used; see the [Electrical Characteristics](#) table. First, the CMRR of the device in the common-mode range below the transition region [$V_{CM} < (V+) - 1.3\text{ V}$] is given. This specification is the best indicator of the capability of the device when the application requires use of one of the differential input pairs. Second, the CMRR over the entire common-mode range is specified at ($V_{CM} = -0.2\text{ V}$ to 5.7 V). This last value includes the variations seen through the transition region (see [Figure 7](#)).

7.3.5 EMI Susceptibility and Input Filtering

Op-amps vary with regard to the susceptibility of the device to electromagnetic interference (EMI). If conducted EMI enters the op-amp, the dc offset observed at the amplifier output may shift from the nominal value while EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. While all op-amp pin functions can be affected by EMI, the signal input pins are likely to be the most susceptible. The OPA2314-Q1 device incorporates an internal input low-pass filter that reduces the amplifiers response to EMI. Both common-mode and differential mode filtering are provided by this filter. The filter is designed for a cutoff frequency of approximately 80 MHz (–3 dB), with a roll-off of 20 dB per decade.

Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. The EMI rejection ratio (EMIRR) metric allows op-amps to be directly compared by the EMI immunity. [Figure 32](#) shows the results of this testing on the OPA2314-Q1 device. Detailed information can also be found in the application report, *EMI Rejection Ratio of Operational Amplifiers* ([SBOA128](#)), available for download from www.ti.com.

7.3.6 Rail-to-Rail Output

Designed as a micro-power, low-noise operational amplifier, the OPA2314-Q1 device delivers a robust output drive capability. A class AB output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. For resistive loads up to 10 k Ω , the output swings typically to within 5 mV of either supply rail regardless of the power-supply voltage applied. Different load conditions change the ability of the amplifier to swing close to the rails; refer to the graph, [Output Voltage Swing vs Output Current](#).

7.4 Device Functional Modes

The OPA2314-Q1 device is powered on when the supply is connected. The device can be operated as a single-supply operational amplifier or a dual-supply amplifier, depending on the application.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

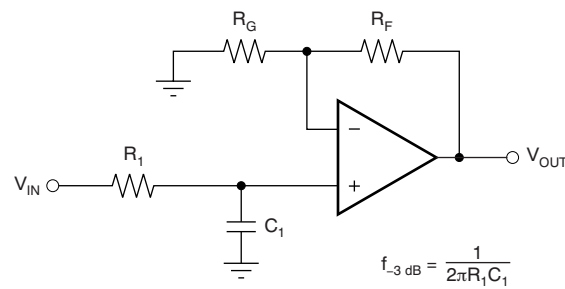
8.1 Application Information

The OPA2314-Q1 device is a low-power, rail-to-rail input and output operational amplifier specifically designed for portable applications. The device operates from 1.8 V to 5.5 V, is unity-gain stable, and suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving $\leq 10\text{-k}\Omega$ loads connected to any point between $V+$ and ground. The input common-mode voltage range includes both rails, and allows the OPA2314-Q1 device to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes the device ideal for driving sampling analog-to-digital converters (ADCs).

The OPA2314-Q1 device features a 3-MHz bandwidth and $1.5\text{-V}/\mu\text{s}$ slew rate with only $150\text{-}\mu\text{A}$ supply current per channel, providing good AC performance at very low power consumption. DC applications are also well served with a very-low input noise voltage of $14\text{ nV}/\sqrt{\text{Hz}}$ at 1 kHz, low-input bias current (0.2 pA), and an input offset voltage of 0.5 mV (typical).

8.1.1 General Configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to establish this limited bandwidth is to place an RC filter at the noninverting terminal of the amplifier, as shown in Figure 34.



$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right) \left(\frac{1}{1 + sR_1C_1}\right)$$

Figure 34. Single-Pole Low-Pass Filter

If additional attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task, as shown in Figure 35. For best results, the amplifier should have a bandwidth that is eight to ten times the filter frequency bandwidth. Failure to follow this guideline can result in phase shift of the amplifier.

Application Information (continued)

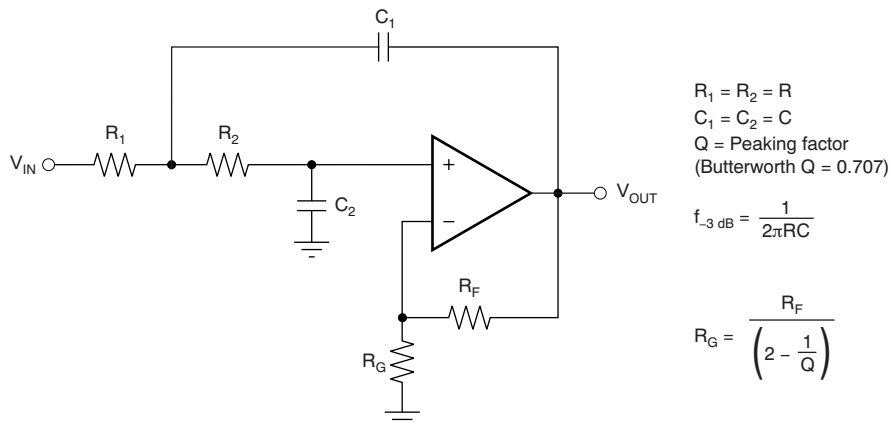


Figure 35. Two-Pole Low-Pass Sallen-Key Filter

8.1.2 Capacitive Load and Stability

The OPA2314-Q1 device is designed to be used in applications where driving a capacitive load is required. As with all op-amps, specific instances can occur where the OPA2314-Q1 device can become unstable. The particular op-amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether or not an amplifier is stable in operation. An op-amp in the unity-gain (1 V/V) buffer configuration that drives a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the op-amp output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases. When operating in the unity-gain configuration, the OPA2314-Q1 device remains stable with a pure capacitive load up to approximately 1 nF. The equivalent series resistance (ESR) of some very large capacitors (C_L greater than 1 μF) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when observing the overshoot response of the amplifier at higher voltage gains. See the graph, [Small-Signal Overshoot vs. Capacitive Load](#).

One technique for increasing the capacitive load drive capability of the amplifier operating in a unity-gain configuration is to insert a small resistor, typically 10 Ω to 20 Ω , in series with the output, as shown in [Figure 36](#). This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. One possible problem with this technique, however, is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing.

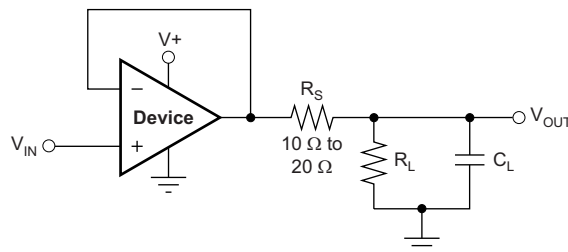


Figure 36. Improving Capacitive Load Drive

8.2 Typical Application

Some applications require differential signals. [Figure 37](#) shows a simple circuit to convert a single-ended input of 0.1 V to 2.4 V into a differential output of ± 2.3 V on a single 2.7-V supply. The output range is intentionally limited to maximize linearity. The circuit is composed of two amplifiers. One amplifier functions as a buffer and creates a voltage, V_{OUT+} . The second amplifier inverts the input and adds a reference voltage to generate V_{OUT-} . Both V_{OUT+} and V_{OUT-} range from 0.1 V to 2.4 V. The difference, V_{DIFF} , is the difference between V_{OUT+} and V_{OUT-} . This makes the differential output voltage range 2.3 V.

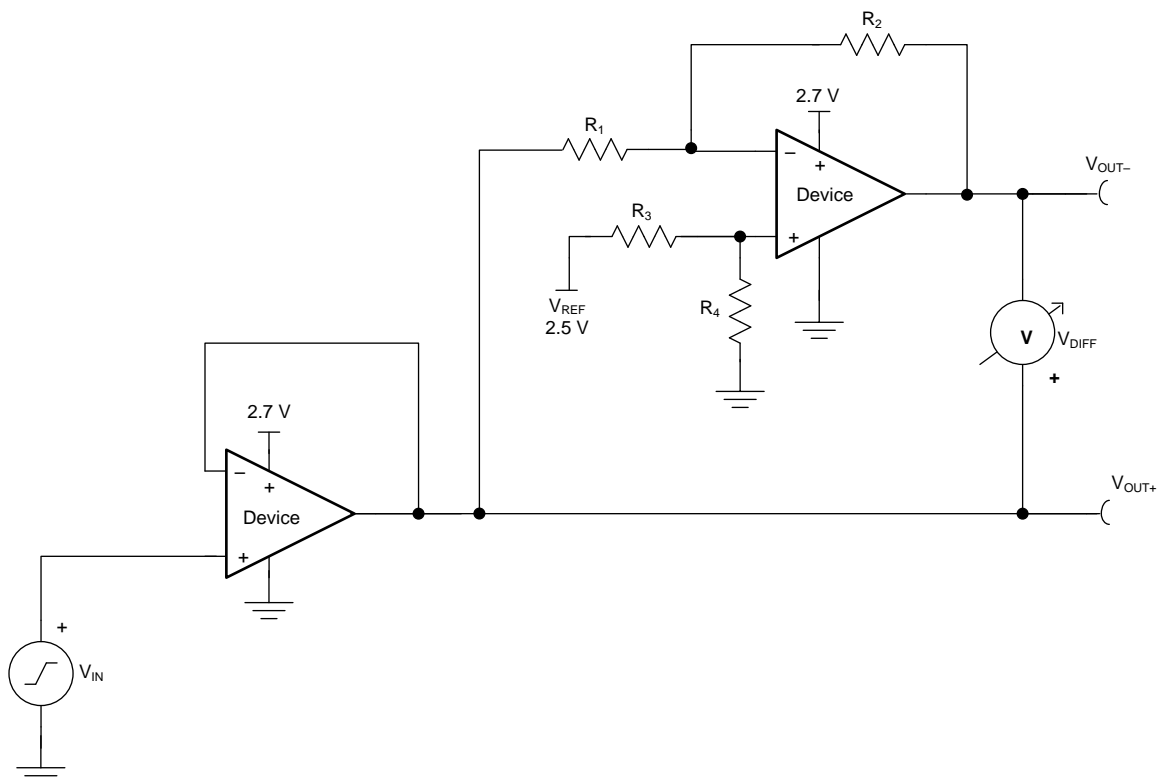


Figure 37. Schematic for a Single-Ended Input to Differential Output Conversion

8.2.1 Design Requirements

The design requirements are as follows:

- Supply voltage: 2.7 V
- Reference voltage: 2.5 V
- Input: 0.1 V to 2.4 V
- Output differential: ± 2.3 V
- Output common-mode voltage: 1.25 V
- Small-signal bandwidth: 1 MHz

8.2.2 Detailed Design Procedure

The circuit in [Figure 37](#) takes a single-ended input signal, V_{IN} , and generates two output signals, V_{OUT+} and V_{OUT-} using two amplifiers and a reference voltage, V_{REF} . V_{OUT+} is the output of the first amplifier and is a buffered version of the input signal, V_{IN} (as shown in [Equation 1](#)). V_{OUT-} is the output of the second amplifier which uses V_{REF} to add an offset voltage to V_{IN} and feedback to add inverting gain. The transfer function for V_{OUT-} is given in [Equation 2](#).

$$V_{OUT+} = V_{IN} \tag{1}$$

$$V_{OUT-} = V_{REF} \times \left(\frac{R_4}{R_3 + R_4} \right) \times \left(1 + \frac{R_2}{R_1} \right) - V_{IN} \times \frac{R_2}{R_1} \tag{2}$$

Typical Application (continued)

The differential output signal, V_{DIFF} , is the difference between the two single-ended output signals, V_{OUT+} and V_{OUT-} . Equation 3 shows the transfer function for V_{DIFF} . By applying the conditions that $R_1 = R_2$ and $R_3 = R_4$, the transfer function is simplified into Equation 6. Using this configuration, the maximum input signal is equal to the reference voltage and the maximum output of each amplifier is equal to V_{REF} . The differential output range is $2 \times V_{REF}$. Furthermore, the common-mode voltage is one half of V_{REF} (see Equation 7).

$$V_{DIFF} = V_{OUT+} - V_{OUT-} = V_{IN} \times \left(1 + \frac{R_2}{R_1}\right) - V_{REF} \times \left(\frac{R_4}{R_3 + R_4}\right) \times \left(1 + \frac{R_2}{R_1}\right) \quad (3)$$

$$V_{OUT+} = V_{IN} \quad (4)$$

$$V_{OUT-} = V_{REF} - V_{IN} \quad (5)$$

$$V_{DIFF} = 2 \times V_{IN} - V_{REF} \quad (6)$$

$$V_{CM} = \left(\frac{V_{OUT+} + V_{OUT-}}{2}\right) = \frac{1}{2} V_{REF} \quad (7)$$

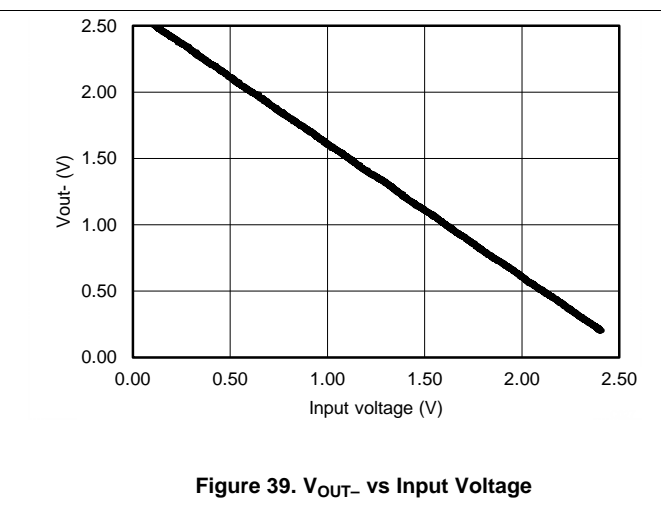
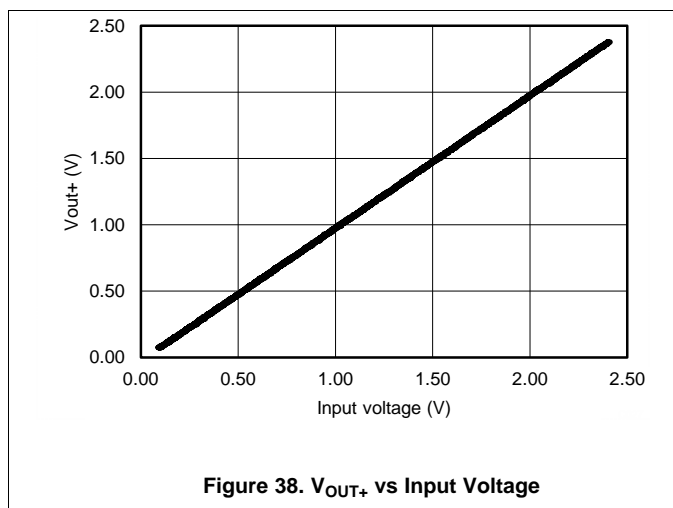
8.2.2.1 Amplifier Selection

Linearity over the input range is key for good dc accuracy. The common-mode input range and output swing limitations determine the linearity. In general, an amplifier with rail-to-rail input and output swing is required. Bandwidth is a key concern for this design, so the OPA2314-Q1 device is selected because its bandwidth is greater than the target of 1 MHz. The bandwidth and power ratio makes this device power efficient and the low offset and drift ensure good accuracy for moderate precision applications.

8.2.2.2 Passive Component Selection

Because the transfer function of V_{out-} is heavily reliant on resistors (R_1 , R_2 , R_3 , and R_4), use resistors with low tolerances to maximize performance and minimize error. This design uses resistors with resistance values of 49.9 k Ω and tolerances of 0.1%. However, if the noise of the system is a key parameter, smaller resistance values (6 k Ω or lower) can be selected to keep the overall system noise low. This ensures that the noise from the resistors is lower than the amplifier noise.

8.2.3 Application Curves



Typical Application (continued)

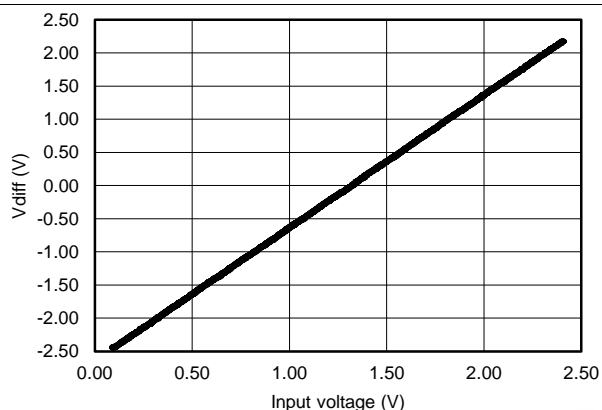


Figure 40. V_{DIFF} vs Input Voltage

9 Power Supply Recommendations

The OPA2314-Q1 device is specified for operation from 1.8 V to 5.5 V (± 0.9 V to ± 2.75 V); many specifications apply from -40°C to 125°C . The [Typical Characteristics](#) presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 7 V can permanently damage the device (see the [Absolute Maximum Ratings](#)).

Place 0.1- μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to the [Layout Guidelines](#) section.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1- μ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to *Circuit Board Layout Techniques*, [SLOA089](#).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in [Figure 41](#).
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example

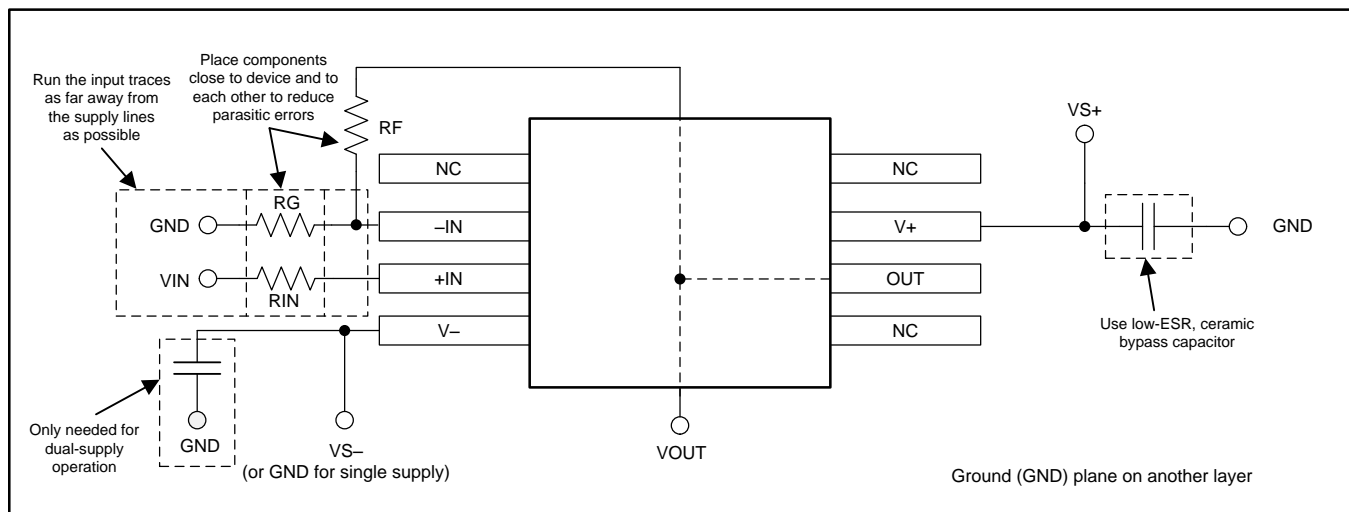
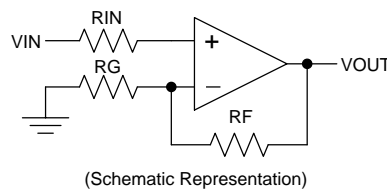


Figure 41. Operational Amplifier Board Layout for Noninverting Configuration

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *Circuit Board Layout Techniques*, [SLOA089](#)
- *EMI Rejection Ratio of Operational Amplifiers*, [SBOA128](#)

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2314AQDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	O2314Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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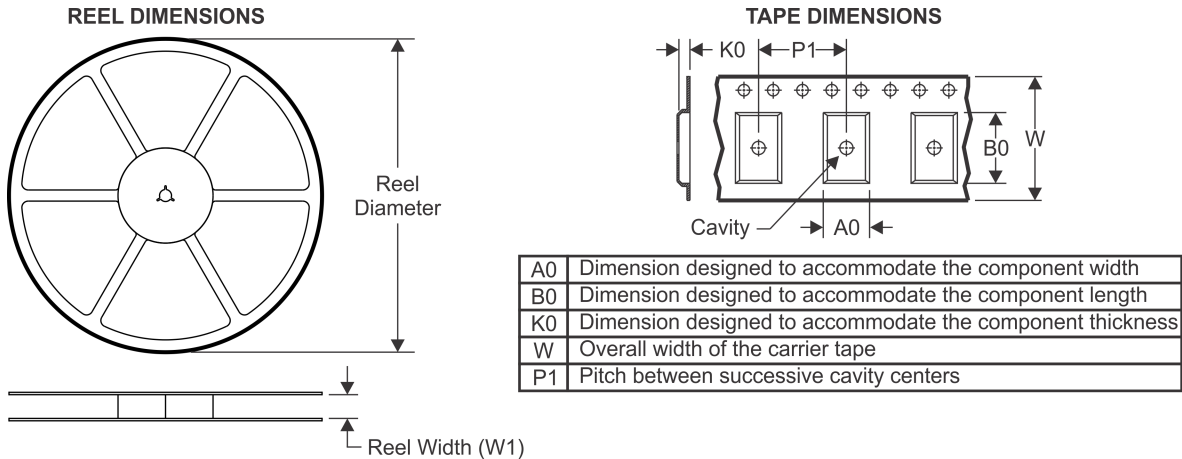
OTHER QUALIFIED VERSIONS OF OPA2314-Q1 :

- Catalog: [OPA2314](#)
- Enhanced Product: [OPA2314-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2314AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

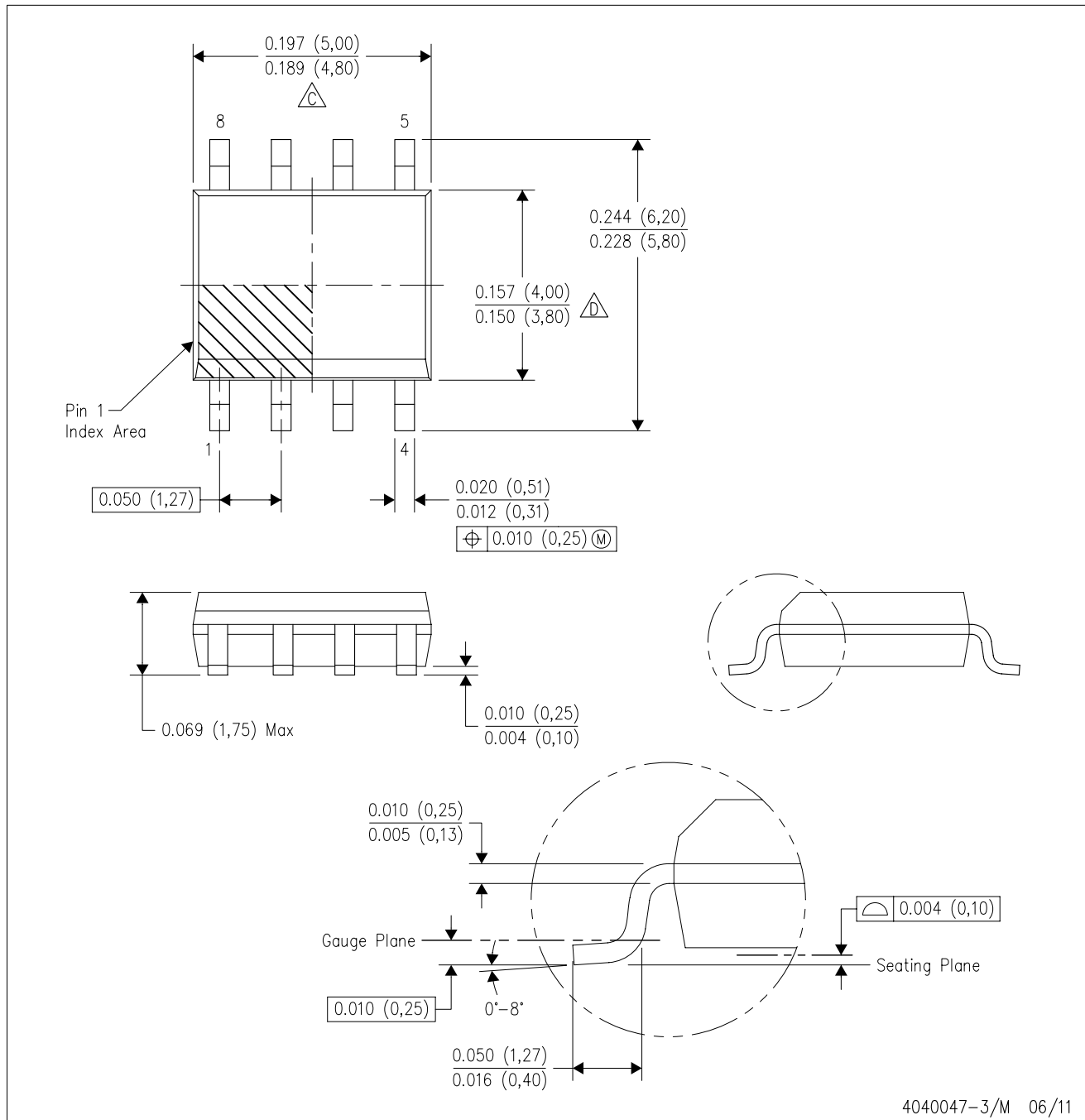


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2314AQDRQ1	SOIC	D	8	2500	367.0	367.0	35.0

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

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