

# MOSFET - Power, Single N-Channel, WDFN9

## 25 V, 0.85 mΩ, 247 A



ON Semiconductor®

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### Product Preview

## NTTFSS1D1N02P1E

#### Features

- Advanced Source-Down Package Technology (3.3x3.3mm) with Excellent Thermal Conduction
- Ultra Low  $R_{DS(on)}$  to Improve System Efficiency
- Low  $Q_G$  and Capacitance to Minimize Driver Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

#### Typical Applications

- DC-DC Switching Applications
- ORing Applications
- Power Load Switch
- Battery Management and Protection

#### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		$V_{DSS}$	25	V	
Gate-to-Source Voltage		$V_{GS}$	$\pm 16$	V	
Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady State	$T_C = 25^\circ\text{C}$	$I_D$	247	A
		$T_C = 85^\circ\text{C}$		178	
Power Dissipation $R_{\theta JC}$ (Note 2)		$T_C = 25^\circ\text{C}$	$P_D$	83	W
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$	41	A
		$T_A = 85^\circ\text{C}$		30	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		$T_A = 25^\circ\text{C}$	$P_D$	2.3	W
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	$I_{DM}$	TBD	A	
Single Pulse Drain-to-Source Avalanche Energy ( $I_{L(pk)} = \text{TBD A}, L = 0.3 \text{ mH}$ )		$E_{AS}$	TBD	mJ	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$	
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)		$T_L$	260	$^\circ\text{C}$	

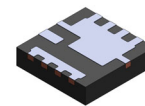
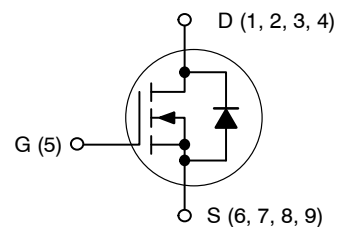
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using a 1 in<sup>2</sup> pad size, 1 oz Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are valid for the particular conditions noted.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

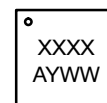
$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
25 V	0.85 mΩ @ 10 V	247 A
	1.04 mΩ @ 4.5 V	

#### NMOS



WDFN9  
CASE 511EB

#### MARKING DIAGRAM



- XXXX = Specific Device Code  
 A = Assembly Location  
 L = Wafer Lot  
 Y = Year  
 W = Work Week  
 ■ = Pb-Free Package

#### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# NTTFSS1D1N02P1E

## THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Case – Steady State (Note 1)	$R_{\theta JC}$	1.5	°C/W
Junction-to-Ambient – Steady State (Note 1, 2)	$R_{\theta JA}$	54.8	

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	25			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 250\ \mu\text{A}$ , ref to $25^\circ\text{C}$		TBD		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		100	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = 16\text{ V}$			100	nA

## ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 934\ \mu\text{A}$	1.2		2.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	$I_D = 934\ \mu\text{A}$ , ref to $25^\circ\text{C}$		TBD		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 27\text{ A}$	0.70	0.85	mΩ
		$V_{GS} = 4.5\text{ V}$	$I_D = 27\text{ A}$	0.83	1.04	
Forward Transconductance	$g_{FS}$	$V_{DS} = 3\text{ V}, I_D = 27\text{ A}$		TBD		S
Gate Resistance	$R_G$	$T_A = 25^\circ\text{C}$		TBD		Ω

## CHARGES & CAPACITANCES

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, V_{DS} = 13\text{ V}, f = 1\text{ MHz}$		4758		pF
Output Capacitance	$C_{OSS}$			1295		
Reverse Capacitance	$C_{RSS}$			61		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 13\text{ V}; I_D = 27\text{ A}$		28.5		nC
Threshold Gate Charge	$Q_{G(TH)}$			TBD		
Gate-to-Drain Charge	$Q_{GD}$			4.2		
Gate-to-Source Charge	$Q_{GS}$			11.4		

## SWITCHING CHARACTERISTICS, $V_{GS} = 10\text{ V}$ (Note 3)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DD} = 13\text{ V}, I_D = 30\text{ A}, R_G = 3\ \Omega$		TBD		ns
Rise Time	$t_r$			TBD		
Turn-Off Delay Time	$t_{d(OFF)}$			TBD		
Fall Time	$t_f$			TBD		

## SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 27\text{ A}$	$T_J = 25^\circ\text{C}$	0.78	1.2	V
			$T_J = 125^\circ\text{C}$	TBD		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, di/dt = 100\text{ A}/\mu\text{s}, I_S = 27\text{ A}$		TBD		ns
Reverse Recovery Charge	$Q_{RR}$			TBD		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures.

## ORDERING INFORMATION

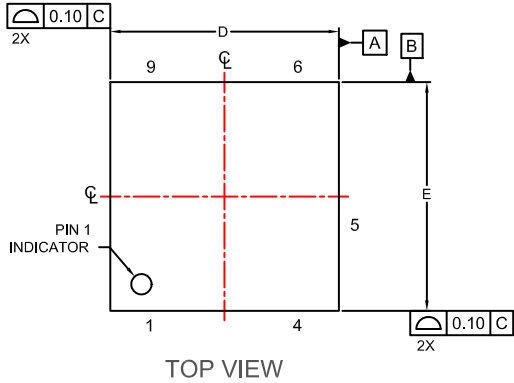
Device	Marking	Package	Shipping†
NTTFSS1D1N02P1E	TBD	WDFN9 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

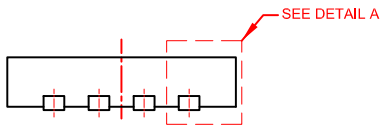
# NTTFSS1D1N02P1E

## PACKAGE DIMENSIONS

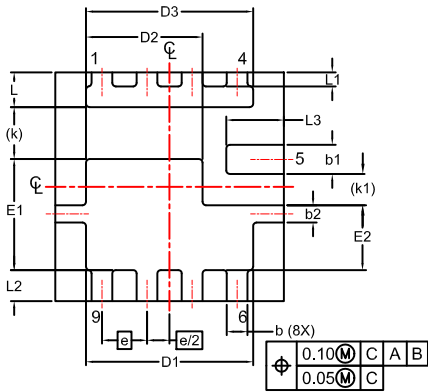
WDFN9 3.3x3.3, 0.65P  
CASE 511EB  
ISSUE A



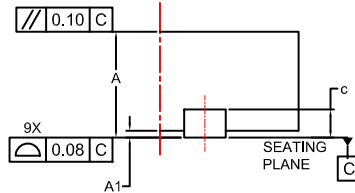
TOP VIEW



FRONT VIEW



BOTTOM VIEW

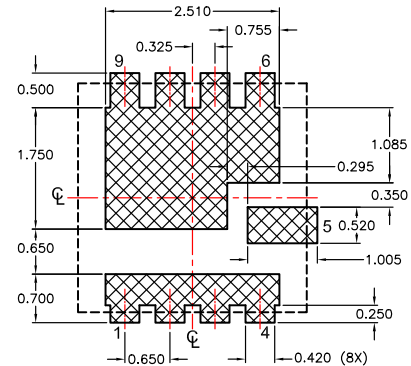


DETAIL A  
SCALE: 2:1

NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS
2. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
3. DIMENSIONS D1, D2, E1 AND E2 DO NOT INCLUDE MOLD FLASH.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

UNIT IN MILLIMETER			
DIM	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.25	0.30	0.35
b1	0.37	0.42	0.47
b2	0.20	0.25	0.30
c	0.17	0.22	0.27
D	3.20	3.30	3.40
D1	2.31	2.41	2.51
D2	1.58	1.68	1.78
D3	2.31	2.41	2.51
E	3.20	3.30	3.40
E1	1.50	1.60	1.70
E2	0.84	0.94	1.04
e	0.650 BSC		
e/2	0.325 BSC		
k	0.75 REF		
k1	0.45 REF		
L	0.40	0.50	0.60
L1	0.10	0.20	0.30
L2	0.35	0.45	0.55
L3	0.73	0.83	0.93



LAND PATTERN  
RECOMMENDATION

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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