

NTMFD4C86N

Advance Information

PowerPhase, Dual N-Channel SO8FL

30 V, High Side 20 A / Low Side 32 A

Features

- Co-Packaged Power Stage Solution to Minimize Board Space
- Minimized Parasitic Inductances
- Optimized Devices to Reduce Power Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- DC-DC Converters
- System Voltage Rails
- Point of Load

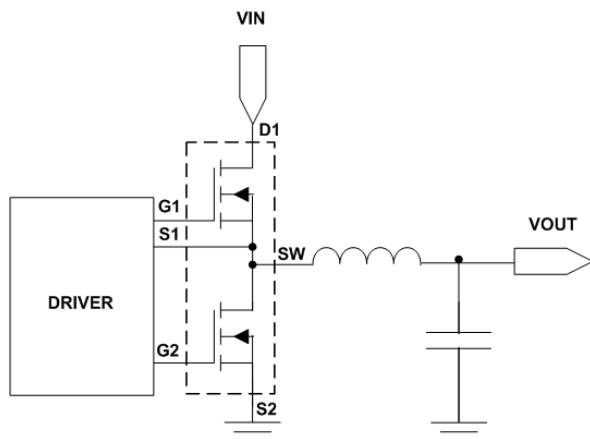


Figure 1. Typical Application Circuit

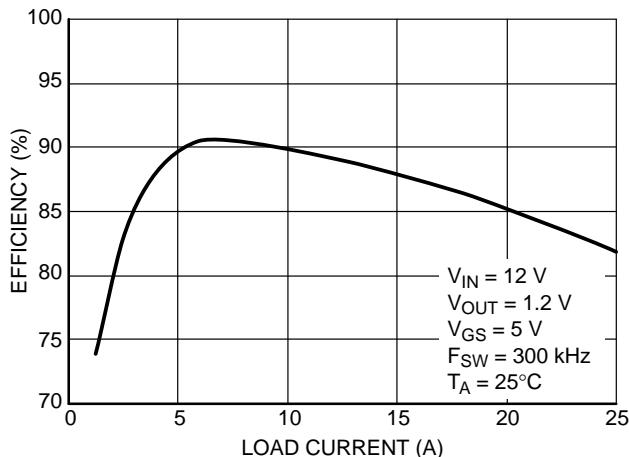


Figure 2. Typical Efficiency Performance
POWERPHASEGEVB Evaluation Board

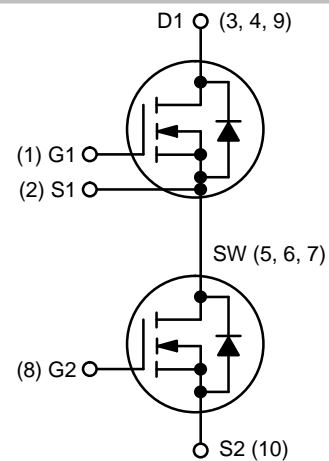
This document contains information on a new product. Specifications and information herein are subject to change without notice.



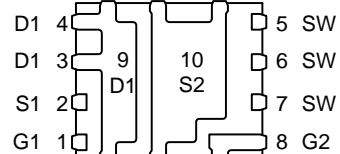
ON Semiconductor®

<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on) MAX}$	$I_D MAX$
Q1 Top FET 30 V	5.4 mΩ @ 10 V	20 A
	8.1 mΩ @ 4.5 V	
Q2 Bottom FET 30 V	2.6 mΩ @ 10 V	32 A
	3.4 mΩ @ 4.5 V	

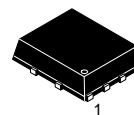


PIN CONNECTIONS



(Bottom View)

MARKING DIAGRAM



DFN8
CASE 506CR



4C86N = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

NTMFD4C86N

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter			Symbol	Value	Unit		
Drain-to-Source Voltage	Q1		V_{DSS}	30	V		
Drain-to-Source Voltage	Q2						
Gate-to-Source Voltage	Q1		V_{GS}	± 20	V		
Gate-to-Source Voltage	Q2						
Continuous Drain Current $R_{\theta JA}$ (Note 1)		Steady State	Q1	$T_A = 25^\circ\text{C}$	14.8	A	
				$T_A = 85^\circ\text{C}$	10.7		
			Q2	$T_A = 25^\circ\text{C}$	23.7		
				$T_A = 85^\circ\text{C}$	17.1		
Power Dissipation $R_{\theta JA}$ (Note 1)			Q1	$T_A = 25^\circ\text{C}$	P_D	1.89	W
Continuous Drain Current $R_{\theta JA} \leq 10$ s (Note 1)		Steady State	Q1	$T_A = 25^\circ\text{C}$	20.2	A	
				$T_A = 85^\circ\text{C}$	14.5		
			Q2	$T_A = 25^\circ\text{C}$	32.3		
				$T_A = 85^\circ\text{C}$	23.3		
Power Dissipation $R_{\theta JA} \leq 10$ s (Note 1)			Q1	$T_A = 25^\circ\text{C}$	P_D	3.51	W
Continuous Drain Current $R_{\theta JA}$ (Note 2)		Steady State	Q1	$T_A = 25^\circ\text{C}$	11.3	A	
				$T_A = 85^\circ\text{C}$	8.1		
			Q2	$T_A = 25^\circ\text{C}$	18.1		
				$T_A = 85^\circ\text{C}$	13.0		
Power Dissipation $R_{\theta JA}$ (Note 2)			Q1	$T_A = 25^\circ\text{C}$	P_D	1.10	W
Pulsed Drain Current			Q1	$T_A = 25^\circ\text{C}$ $t_p = 10 \mu\text{s}$	I_{DM}	160	A
						Q2	
Operating Junction and Storage Temperature	Q1			T_J, T_{STG}	-55 to +150	$^\circ\text{C}$	
	Q2						
Source Current (Body Diode)	Q1			I_S	10	A	
	Q2				10		
Drain to Source DV/DT				dV/dt	6	V/ns	
Single Pulse Drain-to-Source Avalanche Energy ($T_J = 25^\circ\text{C}$, $V_{DD} = 50$ V, $V_{GS} = 10$ V, $L = 0.1$ mH, $R_G = 25 \Omega$)	$I_L = 20$ A _{pk}	Q1	EAS	20	mJ		
	$I_L = 40$ A _{pk}	Q2	EAS	80			
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)				T_L	260	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Surface-mounted on FR4 board using 1 sq-in pad, 2 oz Cu.
- Surface-mounted on FR4 board using the minimum recommended pad size of 100 mm².

NTMFD4C86N

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	66.0	°C/W
Junction-to-Ambient – Steady State (Note 4)	$R_{\theta JA}$	113.7	
Junction-to-Ambient – ($t \leq 10$ s) (Note 3)	$R_{\theta JA}$	35.6	

3. Surface-mounted on FR4 board using 1 sq-in pad, 2 oz Cu.

4. Surface-mounted on FR4 board using the minimum recommended pad size of 100 mm².

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	FET	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Break-down Voltage	Q1	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
	Q2			30			
Drain-to-Source Break-down Voltage Temperature Coefficient	Q1	$V_{(BR)DSS} / T_J$			17		mV / °C
	Q2				16.5		
Zero Gate Voltage Drain Current	Q1	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$	$T_J = 25^\circ\text{C}$		1	μA
				$T_J = 125^\circ\text{C}$		10	
	Q2		$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$	$T_J = 25^\circ\text{C}$		1	
Gate-to-Source Leakage Current	Q1	I_{GSS}	$V_{GS} = 0\text{ V}, V_{DS} = \pm 20\text{ V}$			100	nA
	Q2					100	

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	Q1	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.3		2.2	V
	Q2			1.3		2.2	
Negative Threshold Temperature Coefficient	Q1	$V_{GS(TH)} / T_J$			4.5		mV / °C
	Q2				4.6		
Drain-to-Source On Resistance	Q1	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 30\text{ A}$	4.3	5.4	$\text{m}\Omega$
			$V_{GS} = 4.5\text{ V}$	$I_D = 18\text{ A}$	6.5	8.1	
	Q2		$V_{GS} = 10\text{ V}$	$I_D = 30\text{ A}$	1.7	2.6	
			$V_{GS} = 4.5\text{ V}$	$I_D = 12.5\text{ A}$	2.4	3.4	
Forward Transconductance	Q1	g_{FS}	$V_{DS} = 1.5\text{ V}, I_D = 30\text{ A}$		TBD		S
	Q2				TBD		

CAPACITANCES

Input Capacitance	Q1	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 15\text{ V}$		1153		pF
	Q2				1541		
Output Capacitance	Q1	C_{OSS}			532		
	Q2				764		
Reverse Capacitance	Q1	C_{RSS}			107		
	Q2				42		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

6. Switching characteristics are independent of operating junction temperatures.

NTMFD4C86N

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	FET	Symbol	Test Condition	Min	Typ	Max	Unit		
CHARGES, CAPACITANCES & GATE RESISTANCE									
Total Gate Charge	Q1	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}; I_D = 30\text{ A}$		10.9		nC		
	Q2				21.6				
Threshold Gate Charge	Q1	$Q_{G(TH)}$			TBD				
	Q2				TBD				
Gate-to-Source Charge	Q1	Q_{GS}			3.4				
	Q2				8.6				
Gate-to-Drain Charge	Q1	Q_{GD}			5.4				
	Q2				5.5				
Total Gate Charge	Q1	$Q_{G(TOT)}$		$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}; I_D = 30\text{ A}$		22.2			nC
	Q2					47.5			
Gate Resistance	Q1	R_G	$T_A = 25^\circ\text{C}$		1.0		Ω		
	Q2				1.0				

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	Q1	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V},$ $I_D = 15\text{ A}, R_G = 3.0\ \Omega$		8.9		ns
	Q2				8.3		
Rise Time	Q1	t_r			21.2		
	Q2				15.1		
Turn-Off Delay Time	Q1	$t_{d(OFF)}$			15.3		
	Q2				19.3		
Fall Time	Q1	t_f			4.4		
	Q2				4.2		

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	Q1	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V},$ $I_D = 15\text{ A}, R_G = 3.0\ \Omega$		6.7		ns
	Q2				6.3		
Rise Time	Q1	t_r			19.5		
	Q2				13.8		
Turn-Off Delay Time	Q1	$t_{d(OFF)}$			20.1		
	Q2				22.8		
Fall Time	Q1	t_f			2.8		
	Q2				3.2		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Voltage	Q1	V_{SD}	$V_{GS} = 0\text{ V},$ $I_S = 10\text{ A}$	$T_J = 25^\circ\text{C}$		0.80	V
				$T_J = 125^\circ\text{C}$		0.60	
	Q2			$T_J = 25^\circ\text{C}$		0.78	
				$T_J = 125^\circ\text{C}$		0.62	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

6. Switching characteristics are independent of operating junction temperatures.

NTMFD4C86N

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	FET	Symbol	Test Condition	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS							
Reverse Recovery Time	Q1	t _{RR}	V _{GS} = 0 V, d _{IS} /d _t = 100 A/μs, I _S = 30 A		29.1		ns
	Q2				33.7		
Charge Time	Q1	t _a			14.5		
	Q2				17.4		
Discharge Time	Q1	t _b			14.6		
	Q2				16.3		
Reverse Recovery Charge	Q1	Q _{RR}			21		nC
	Q2				27.5		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

6. Switching characteristics are independent of operating junction temperatures.

NTMFD4C86N

TYPICAL CHARACTERISTICS – Q1

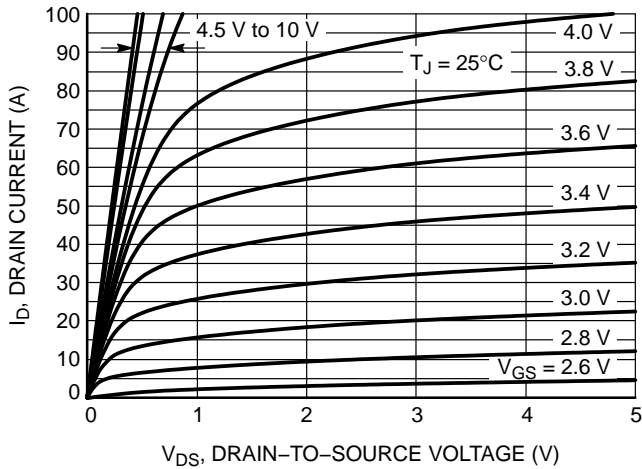


Figure 3. On-Region Characteristics

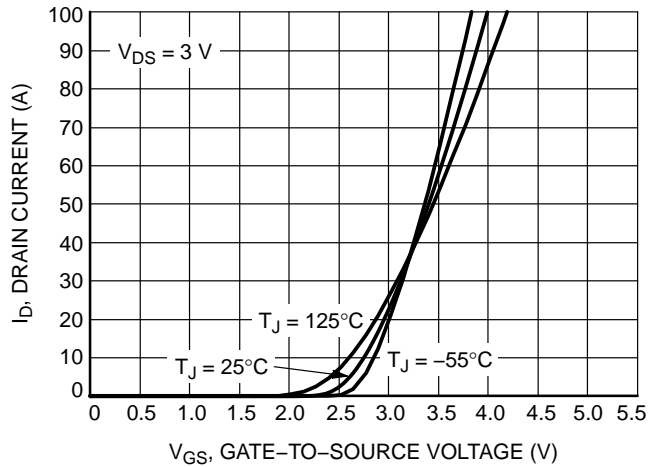


Figure 4. Transfer Characteristics

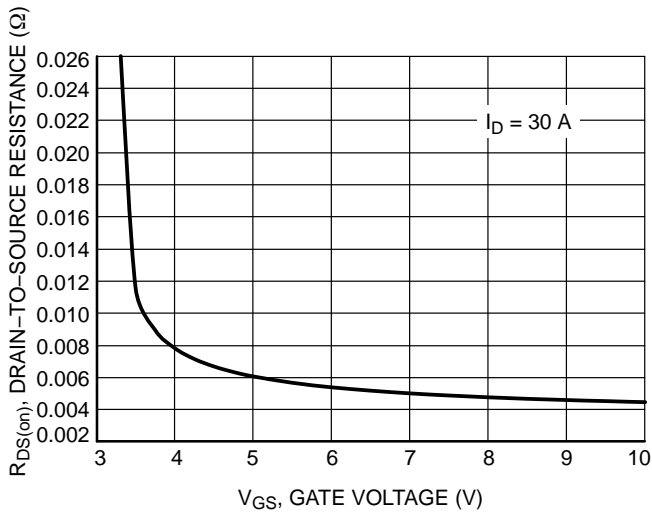


Figure 5. On-Resistance vs. Gate-to-Source Voltage

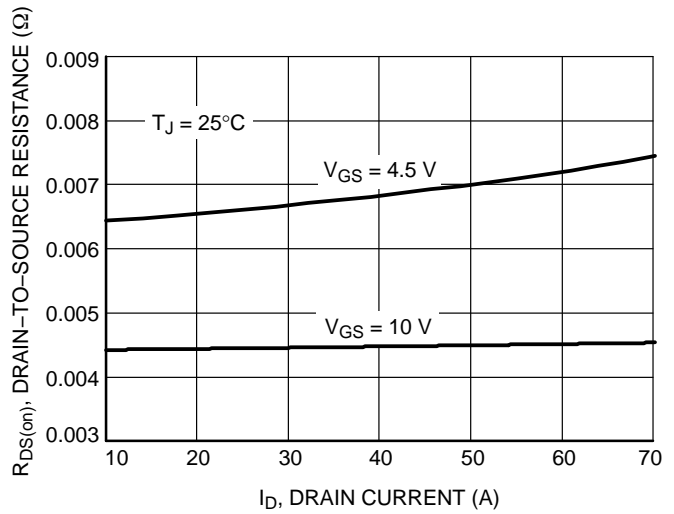


Figure 6. On-Resistance vs. Drain Current and Gate Voltage

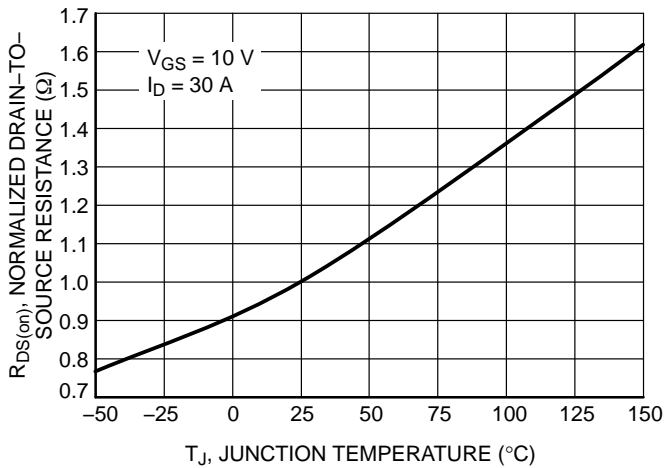


Figure 7. On-Resistance Variation with Temperature

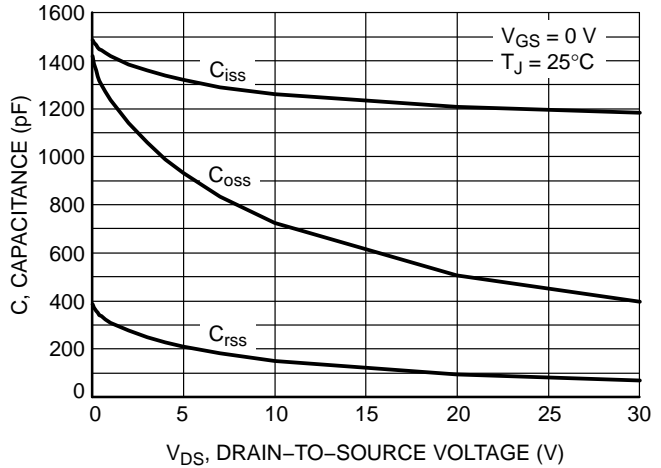


Figure 8. Capacitance Variation

NTMFD4C86N

TYPICAL CHARACTERISTICS – Q1

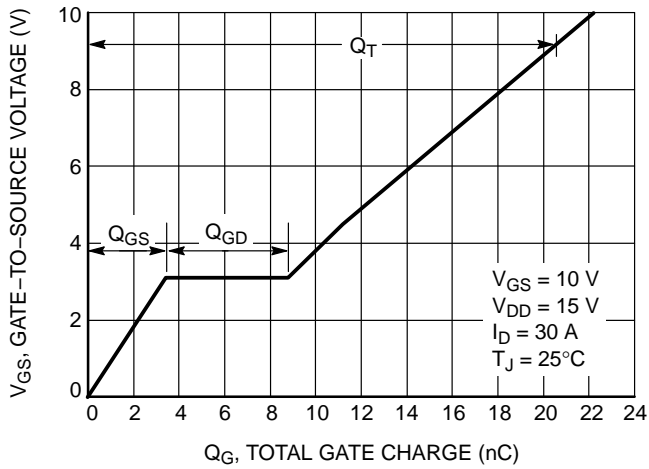


Figure 9. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

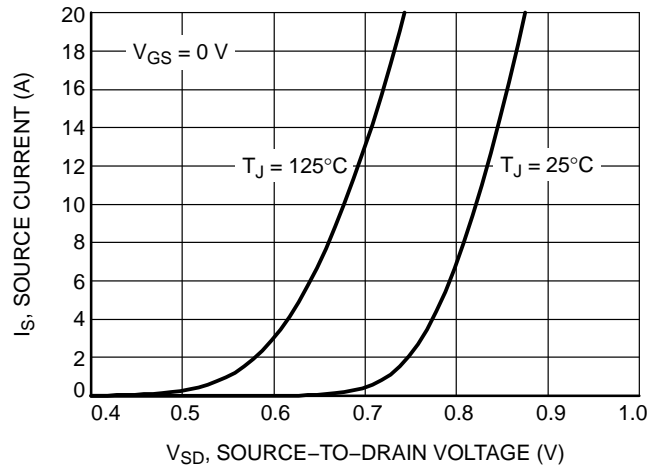


Figure 10. Diode Forward Voltage vs. Current

NTMFD4C86N

TYPICAL CHARACTERISTICS – Q2

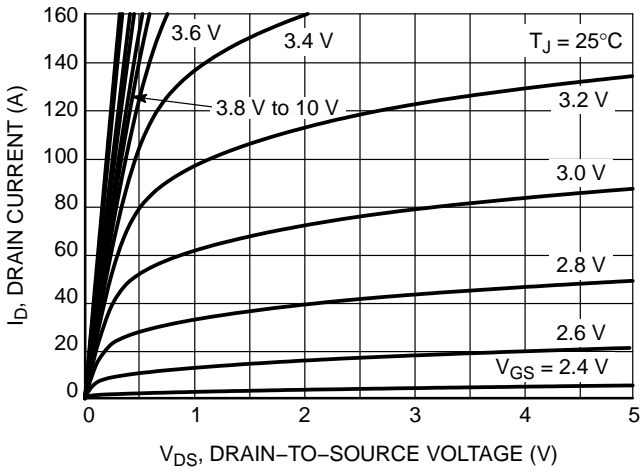


Figure 11. On-Region Characteristics

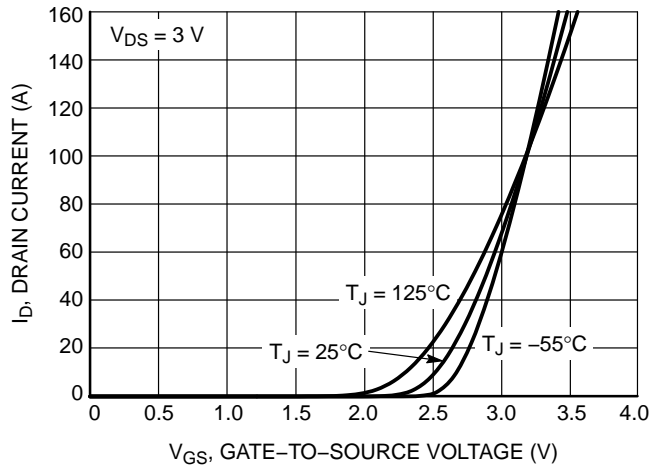


Figure 12. Transfer Characteristics

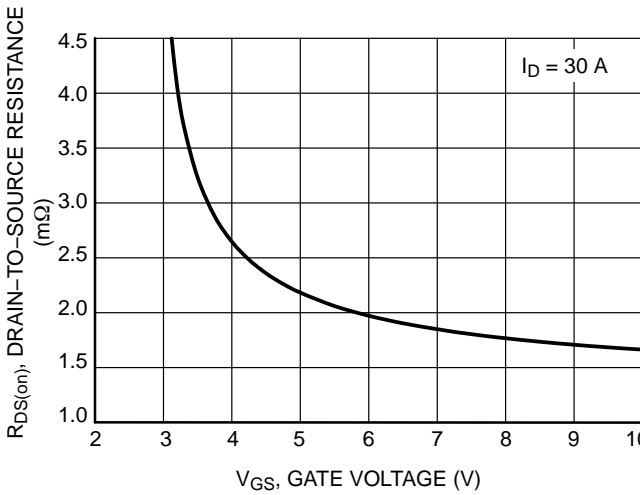


Figure 13. On-Resistance vs. Gate-to-Source Voltage

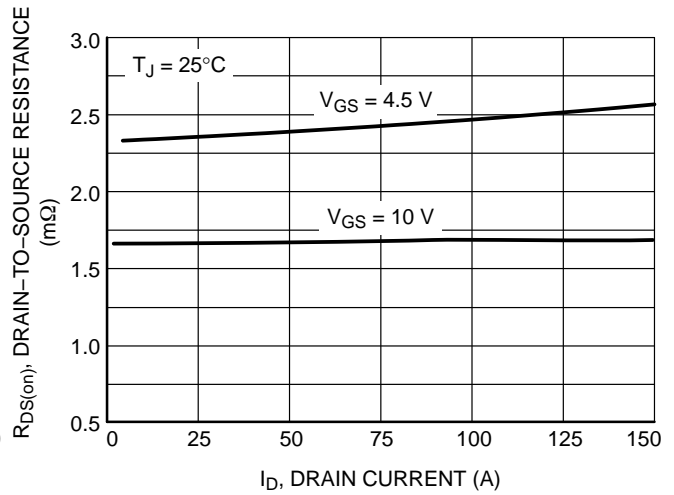


Figure 14. On-Resistance vs. Drain Current and Gate Voltage

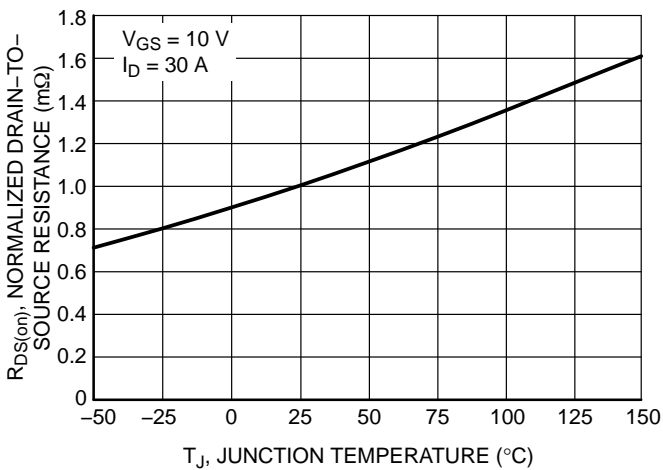


Figure 15. On-Resistance Variation with Temperature

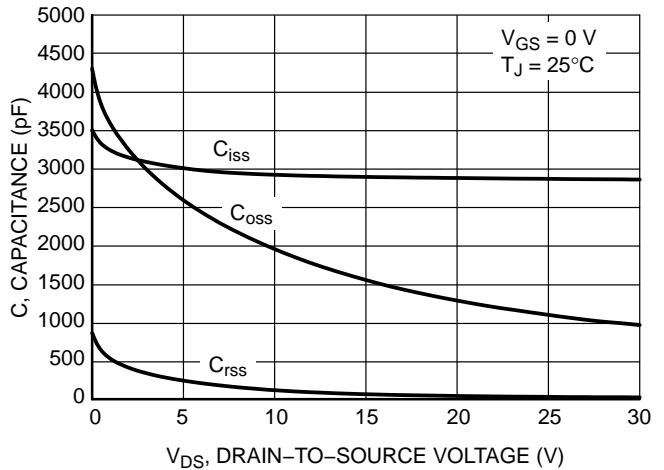


Figure 16. Capacitance Variation

NTMFD4C86N

TYPICAL CHARACTERISTICS – Q2

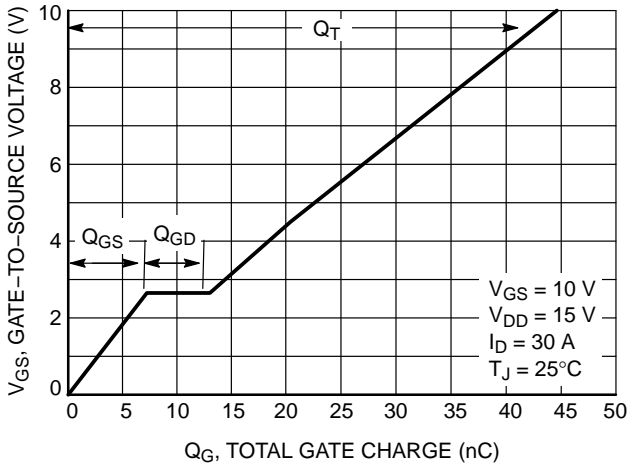


Figure 17. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

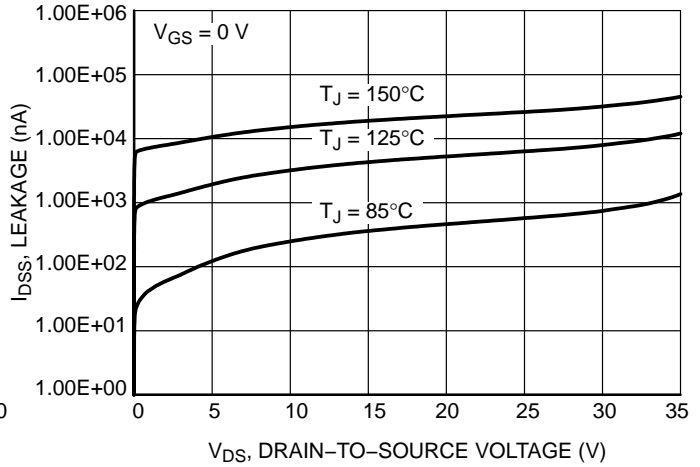


Figure 18. Drain-to-Source Leakage Current vs. Voltage

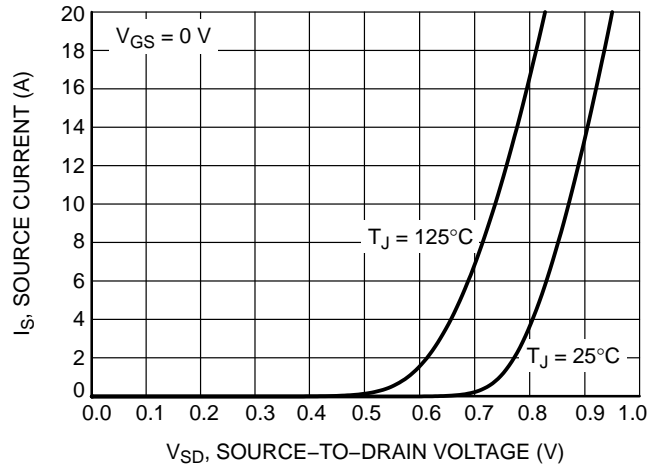


Figure 19. Diode Forward Voltage vs. Current

ORDERING INFORMATION

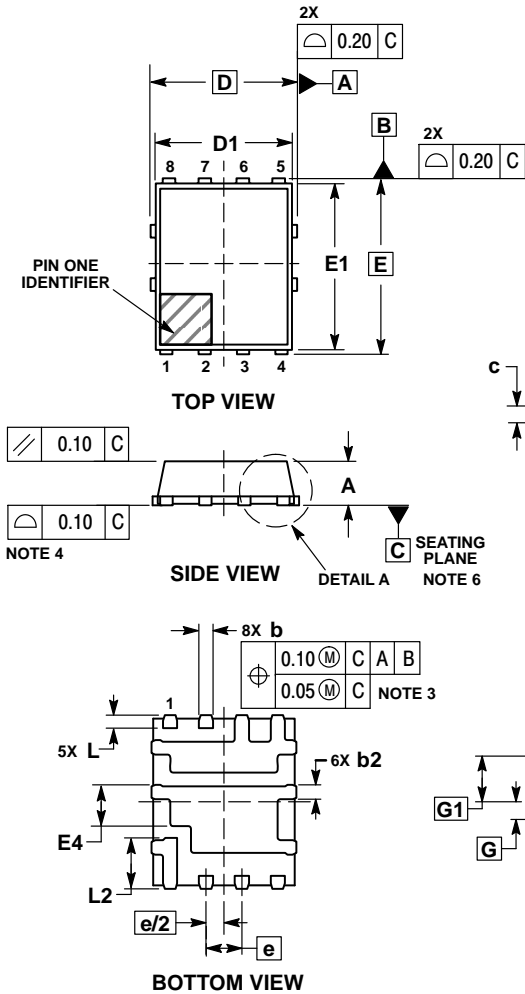
Device	Package	Shipping†
NTMFD4C86NT1G	DFN8 (Pb-Free)	1500 / Tape & Reel
NTMFD4C86NT3G	DFN8 (Pb-Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTMFD4C86N

PACKAGE DIMENSIONS

DFN8 5x6, 1.27P PowerPhase FET CASE 506CR ISSUE A

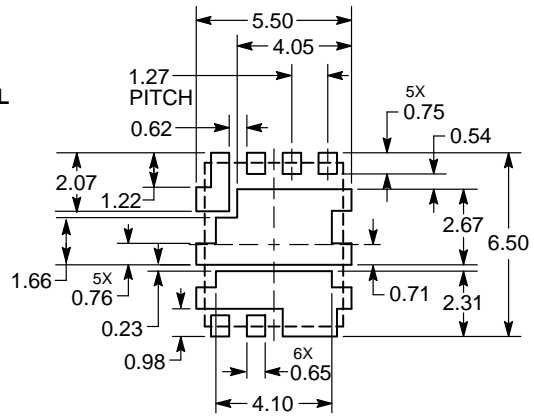


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b AND b1 APPLY TO PLATED TERMINAL AND ARE MEASURED BETWEEN 0.15 AND 0.25 MM FROM THE TIPS.
4. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.


DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.55
A1	0.00	0.05
b	0.40	0.60
b2	0.40	0.60
c	0.20	0.30
D	5.15 BSC	
D1	4.90	5.10
D2	3.70	3.90
D3	2.96	3.16
E	6.15 BSC	
E1	5.80	6.00
E2	2.37	2.57
E3	1.05	1.25
E4	1.36	1.56
e	1.27 BSC	
G	0.625 BSC	
G1	1.615 BSC	
h	---	12°
L	0.34	0.59
L2	1.68	1.93

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local
Sales Representative