

MOSFET – Power, Single, P-Channel, Schottky Diode, Schottky Barrier Diode -30 V, -4.0 A, 20 V, 2.2 A

NTMD4184PF

Features

- FETKY™ Surface Mount Package Saves Board Space
- Independent Pin-Out for MOSFET and Schottky Allowing for Design Flexibility
- Low $R_{DS(on)}$ MOSFET and Low V_F Schottky to Minimize Conduction Losses
- Optimized Gate Charge to Minimize Switching Losses
- This is a Pb-Free Device

Applications

- Disk Drives
- DC-DC Converters
- Printers

MOSFET MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Rating			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DS}	-30	V
Gate-to-Source Voltage			V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JA}$ (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	I_D	-3.3	A
		$T_A = 70^\circ\text{C}$		-2.6	
		$T_A = 25^\circ\text{C}$	P_D	1.6	W
		$T_A = 25^\circ\text{C}$	I_D	-2.3	A
		$T_A = 70^\circ\text{C}$		-1.8	
		$T_A = 25^\circ\text{C}$	P_D	0.77	W
Continuous Drain Current $R_{\theta JA}$ (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	I_D	-4.0	A
Power Dissipation $R_{\theta JA}$ (Note 2)		$T_A = 70^\circ\text{C}$		-3.2	
Continuous Drain Current $R_{\theta JA} \ t < 10 \text{ s}$ (Note 1)		$T_A = 25^\circ\text{C}$	P_D	2.31	W
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$		I_{DM}	-10	A
Operating Junction and Storage Temperature			T_J, T_{STG}	-55 to +150	$^\circ\text{C}$
Source Current (Body Diode)			I_S	-1.3	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	$^\circ\text{C}$

SCHOTTKY MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Peak Repetitive Reverse Voltage			V_{RRM}	20	V
DC Blocking Voltage			V_R	20	V
Average Rectified Forward Current, (Note 1)	Steady State		I_F	2.2	A
	$t < 10 \text{ s}$			3.2	



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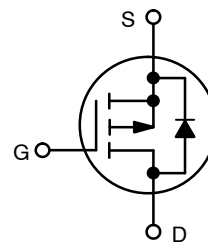
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P-CHANNEL MOSFET

$V_{(BR)DSS}$	$R_{DS(on)}$ Max	I_D Max
-30 V	95 m Ω @ -10 V	-4.0 A
	165 m Ω @ -4.5 V	

SCHOTTKY DIODE

V_R Max	V_F Max	I_F Max
20 V	0.58 V	2.2 A

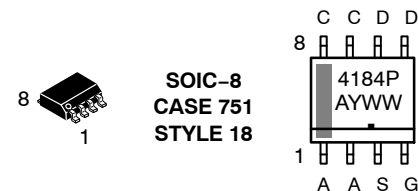


P-Channel MOSFET



Schottky Diode

MARKING DIAGRAM & PIN ASSIGNMENT



4184P = Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NTMD4184PFR2G	SOIC-8 (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTMD4184PF

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter MOSFET & Schottky	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	79	$^{\circ}\text{C/W}$
Junction-to-Ambient – $t \leq 10$ s Steady State (Note 1)	$R_{\theta JA}$	54	
Junction-to-FOOT (Drain) Equivalent to $R_{\theta JC}$	$R_{\theta JF}$	50	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	163	

1. Surface-mounted on FR4 board using 1 inch sq pad size, 1 oz Cu.
2. Surface-mounted on FR4 board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	-30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			30		$\text{mV}/^{\circ}\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = -24\text{ V}$			-1.0	μA
		$T_J = 125^{\circ}\text{C}$			-10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	-1.0		-3.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			4.4		$\text{mV}/^{\circ}\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -3.0\text{ A}$		70	95	$\text{m}\Omega$
		$V_{GS} = -4.5\text{ V}, I_D = -1.5\text{ A}$		120	165	
Forward Transconductance	g_{FS}	$V_{DS} = -1.5\text{ V}, I_D = -3.0\text{ A}$		5.0		S

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = -10\text{ V}$		280	360	pF
Output Capacitance	C_{OSS}			80	110	
Reverse Transfer Capacitance	C_{RSS}			52	80	
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -4.5\text{ V}, V_{DS} = -10\text{ V}, I_D = -3.0\text{ A}$		2.8	4.2	nC
Threshold Gate Charge	$Q_{G(TH)}$			0.4		
Gate-to-Source Charge	Q_{GS}			1.1		
Gate-to-Drain Charge	Q_{GD}			1.1		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -10\text{ V}, V_{DS} = -10\text{ V}, I_D = -3.0\text{ A}$		5.8	8.8	nC

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -10\text{ V}, V_{DS} = -10\text{ V}, I_D = -1.0\text{ A}, R_G = 6.0\text{ }\Omega$		7.2	15	ns
Rise Time	t_r			12	24	
Turn-Off Delay Time	$t_{d(OFF)}$			18	36	
Fall Time	t_f			2.6	6.0	

DRAIN-TO-SOURCE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_D = -1.3\text{ A}$	$T_J = 25^{\circ}\text{C}$		-0.8	-1.0	V
			$T_J = 125^{\circ}\text{C}$		0.7		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = -1.3\text{ A}$		12.8			ns
Charge Time	t_a			10			
Discharge Time	t_b			2.8			
Reverse Recovery Time	Q_{RR}			7.4			nC

NTMD4184PF

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
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SCHOTTKY DIODE ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Instantaneous Forward Voltage	V_F	$I_F = 1.0\text{ A}$	$T_J = 25^\circ\text{C}$	0.43	0.50	V
			$T_J = 125^\circ\text{C}$	0.35	0.39	
		$I_F = 2.0\text{ A}$	$T_J = 25^\circ\text{C}$	0.5	0.58	
			$T_J = 125^\circ\text{C}$	0.45	0.53	
Maximum Instantaneous Reverse Current	I_R	$V_R = 10\text{ V}$	$T_J = 25^\circ\text{C}$	0.001	0.02	mA
			$T_J = 125^\circ\text{C}$	1.2	14	
		$V_R = 20\text{ V}$	$T_J = 25^\circ\text{C}$	0.004	0.05	
			$T_J = 125^\circ\text{C}$	2.0	18	

- Pulse Test: pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

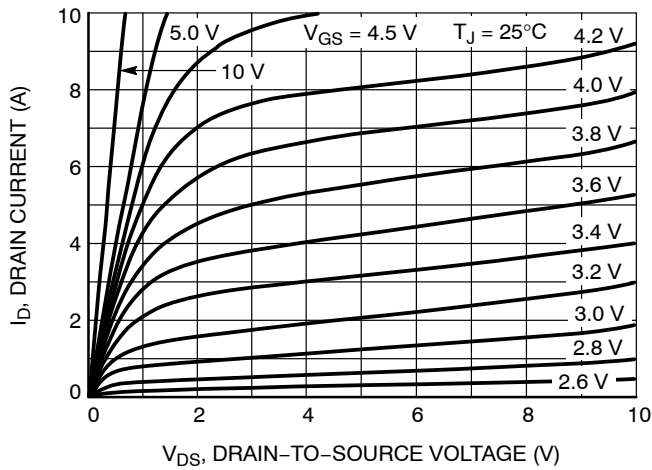


Figure 1. On-Region Characteristics

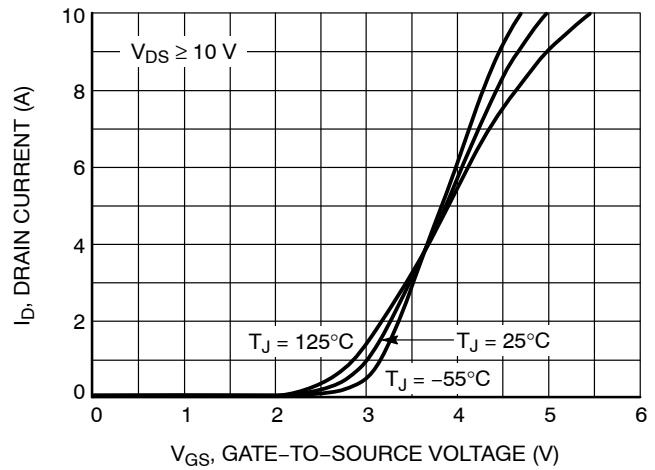


Figure 2. Transfer Characteristics

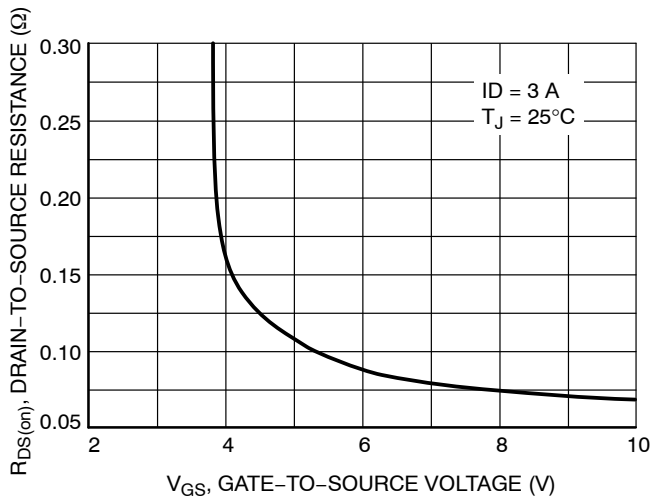


Figure 3. On-Resistance vs. Gate Voltage

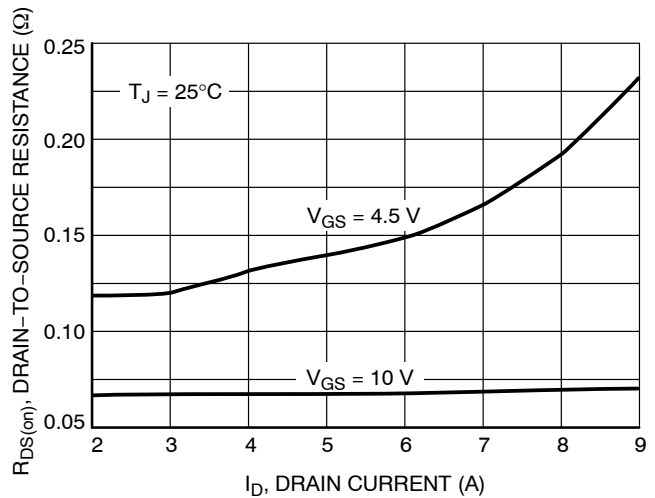


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

TYPICAL CHARACTERISTICS

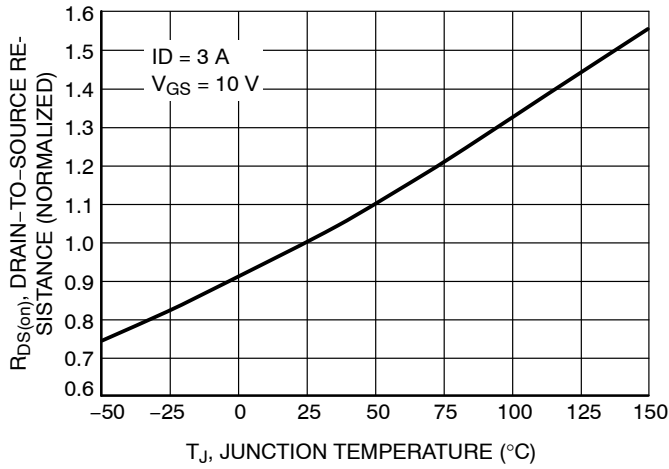


Figure 5. On-Resistance Variation with Temperature

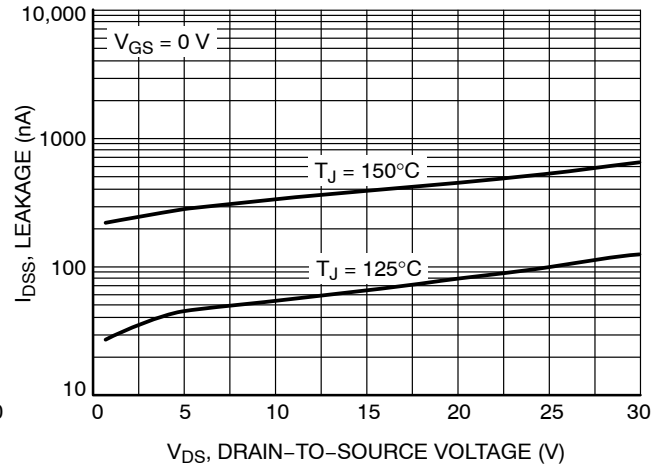


Figure 6. Drain-to-Source Leakage Current vs. Voltage

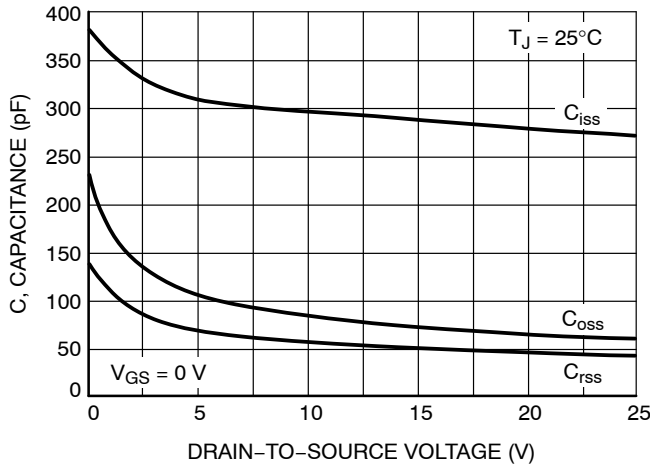


Figure 7. Capacitance Variation

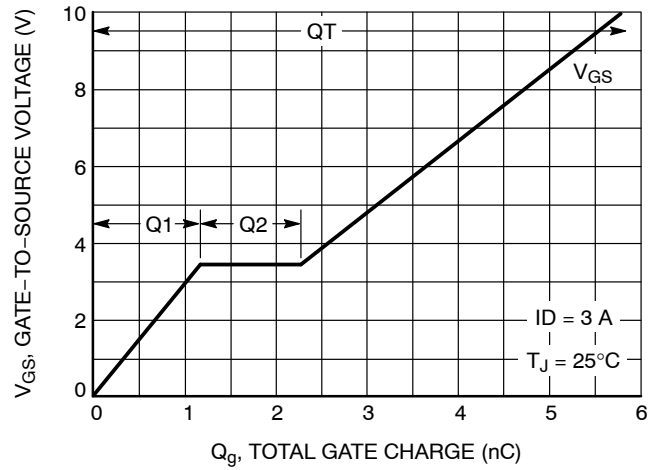


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

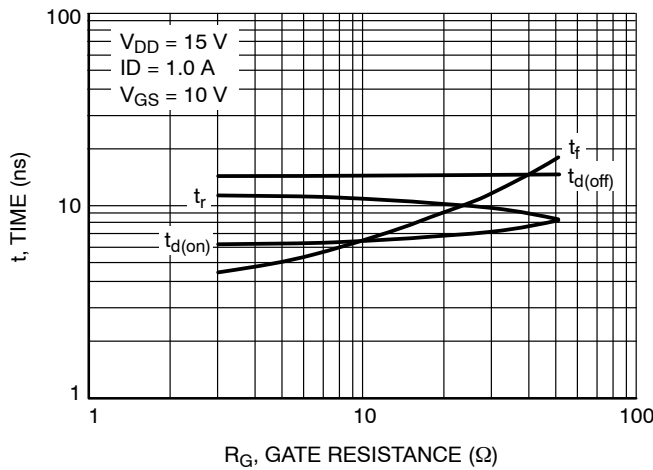


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

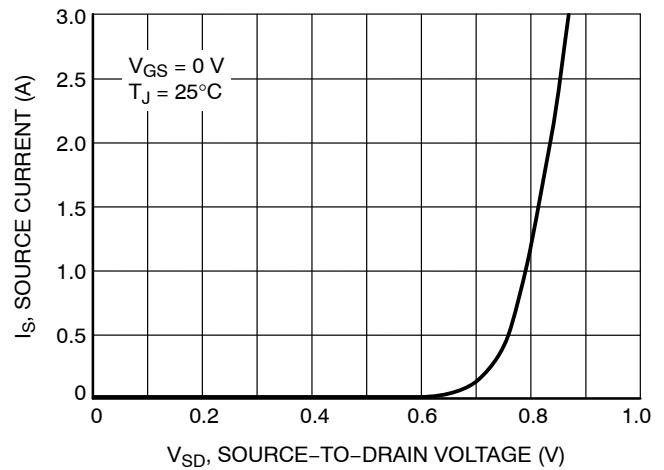


Figure 10. Diode Forward Voltage vs. Current

TYPICAL CHARACTERISTICS

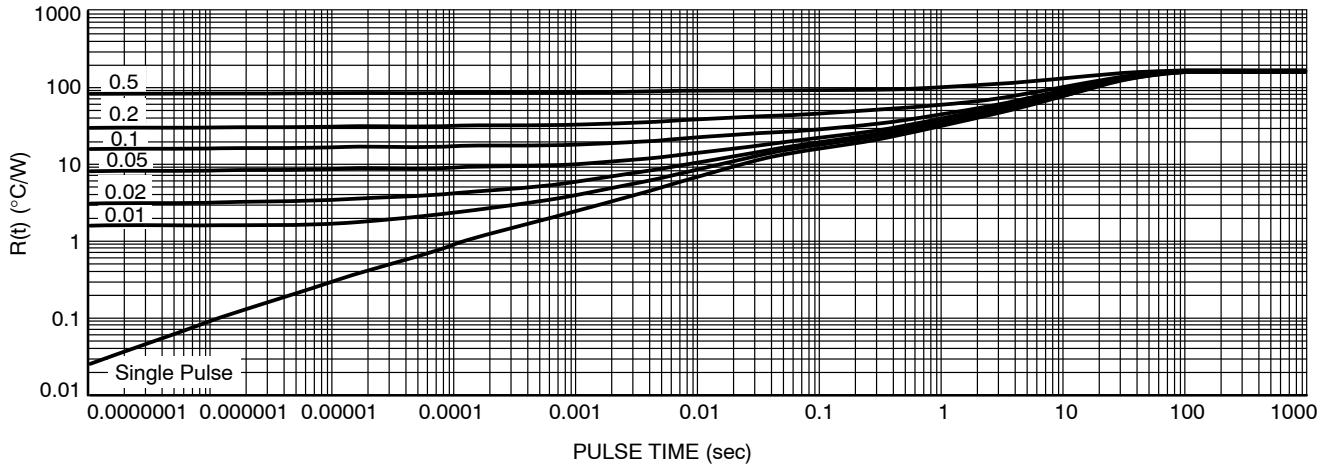


Figure 11. Thermal Response – $R_{\theta JA}$ at Steady State (min pad)

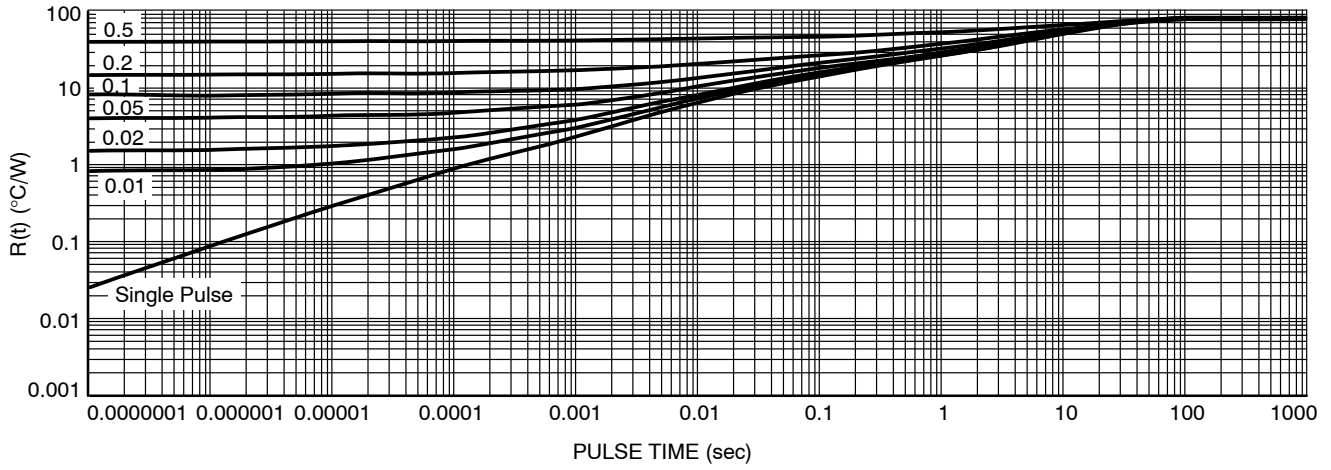


Figure 12. Thermal Response – $R_{\theta JA}$ at Steady State (1 inch sq pad)

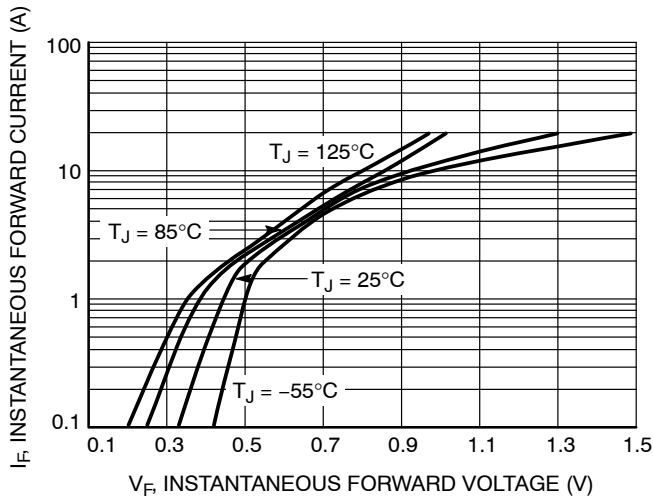


Figure 13. Typical Forward Voltage

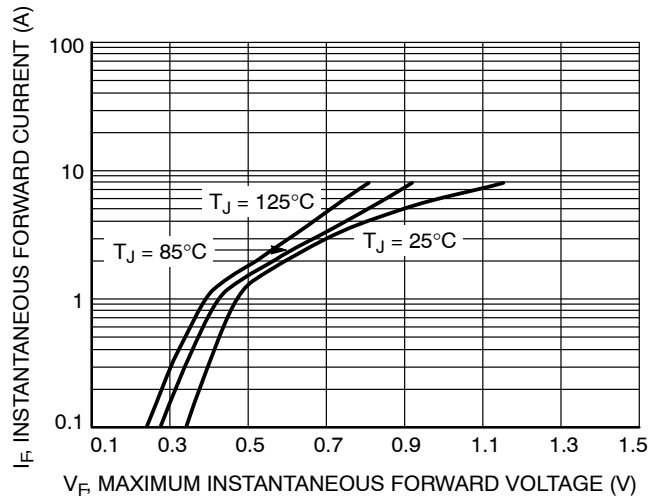


Figure 14. Maximum Forward Voltage

NTMD4184PF

TYPICAL CHARACTERISTICS

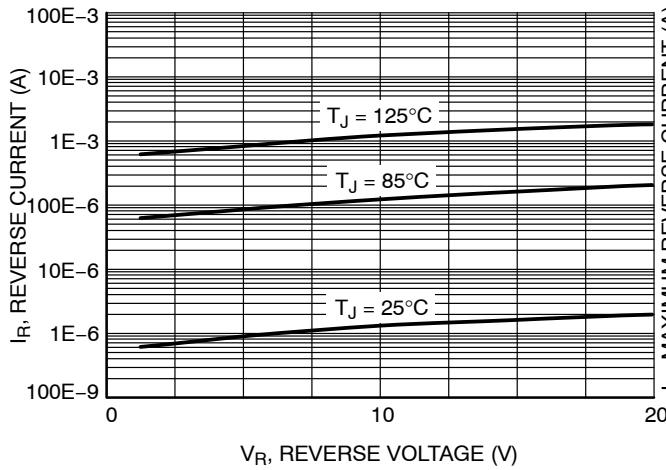


Figure 15. Typical Reverse Current

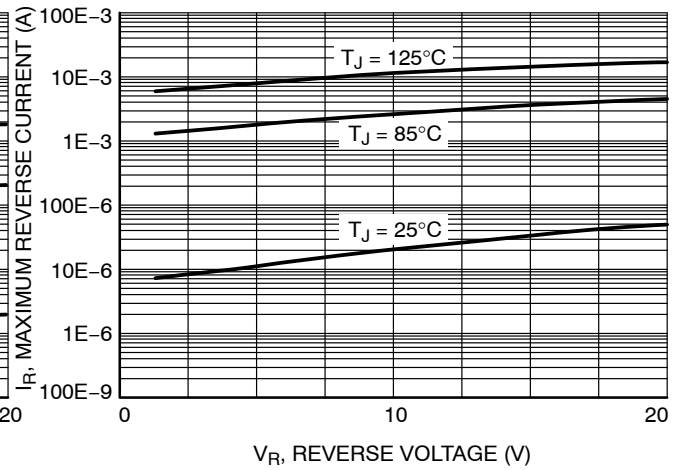


Figure 16. Maximum Reverse Current

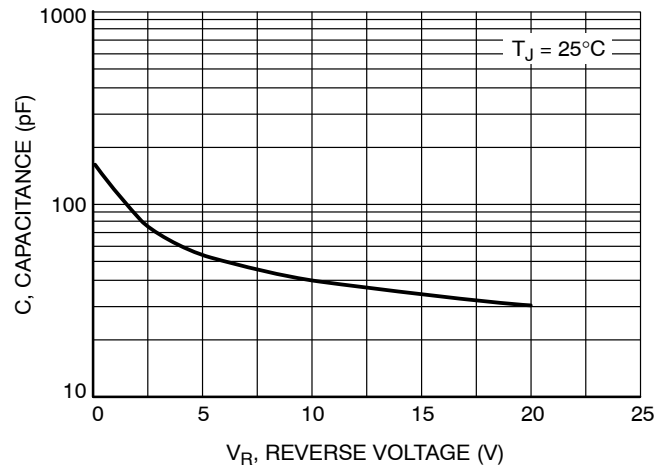
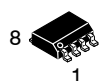


Figure 17. Capacitance

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

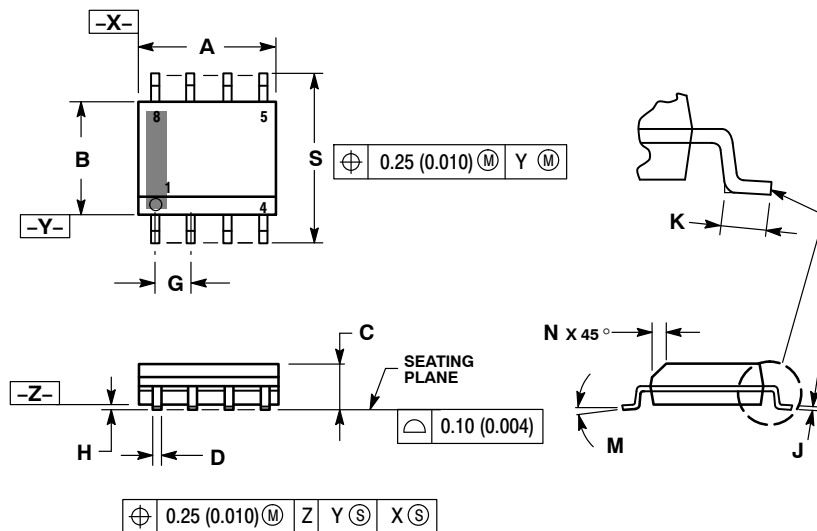
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SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

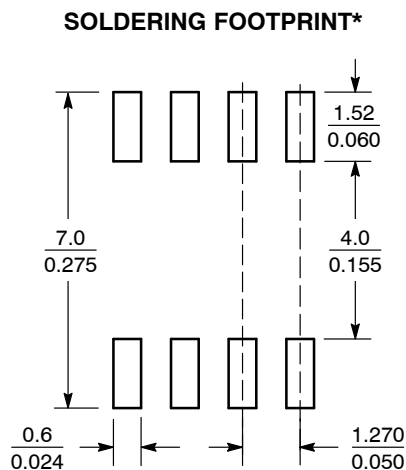


NOTES:

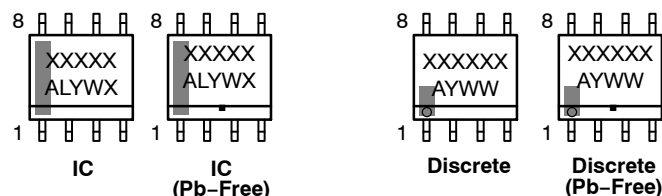
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

GENERIC MARKING DIAGRAM*



SCALE 6:1 (mm/inches)



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
■ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

STYLE 1: PIN 1. EMITTER 2. COLLECTOR 3. COLLECTOR 4. EMITTER 5. EMITTER 6. BASE 7. BASE 8. EMITTER	STYLE 2: PIN 1. COLLECTOR, DIE, #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. BASE, #2 6. EMITTER, #2 7. BASE, #1 8. EMITTER, #1	STYLE 3: PIN 1. DRAIN, DIE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. GATE, #2 6. SOURCE, #2 7. GATE, #1 8. SOURCE, #1	STYLE 4: PIN 1. ANODE 2. ANODE 3. ANODE 4. ANODE 5. ANODE 6. ANODE 7. ANODE 8. COMMON CATHODE
STYLE 5: PIN 1. DRAIN 2. DRAIN 3. DRAIN 4. DRAIN 5. GATE 6. GATE 7. SOURCE 8. SOURCE	STYLE 6: PIN 1. SOURCE 2. DRAIN 3. DRAIN 4. SOURCE 5. SOURCE 6. GATE 7. GATE 8. SOURCE	STYLE 7: PIN 1. INPUT 2. EXTERNAL BYPASS 3. THIRD STAGE SOURCE 4. GROUND 5. DRAIN 6. GATE 3 7. SECOND STAGE Vd 8. FIRST STAGE Vd	STYLE 8: PIN 1. COLLECTOR, DIE #1 2. BASE, #1 3. BASE, #2 4. COLLECTOR, #2 5. COLLECTOR, #2 6. EMITTER, #2 7. EMITTER, #1 8. COLLECTOR, #1
STYLE 9: PIN 1. EMITTER, COMMON 2. COLLECTOR, DIE #1 3. COLLECTOR, DIE #2 4. EMITTER, COMMON 5. EMITTER, COMMON 6. BASE, DIE #2 7. BASE, DIE #1 8. EMITTER, COMMON	STYLE 10: PIN 1. GROUND 2. BIAS 1 3. OUTPUT 4. GROUND 5. GROUND 6. BIAS 2 7. INPUT 8. GROUND	STYLE 11: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1	STYLE 12: PIN 1. SOURCE 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
STYLE 13: PIN 1. N.C. 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN	STYLE 14: PIN 1. N-SOURCE 2. N-GATE 3. P-SOURCE 4. P-GATE 5. P-DRAIN 6. P-DRAIN 7. N-DRAIN 8. N-DRAIN	STYLE 15: PIN 1. ANODE 1 2. ANODE 1 3. ANODE 1 4. ANODE 1 5. CATHODE, COMMON 6. CATHODE, COMMON 7. CATHODE, COMMON 8. CATHODE, COMMON	STYLE 16: PIN 1. EMITTER, DIE #1 2. BASE, DIE #1 3. EMITTER, DIE #2 4. BASE, DIE #2 5. COLLECTOR, DIE #2 6. COLLECTOR, DIE #2 7. COLLECTOR, DIE #1 8. COLLECTOR, DIE #1
STYLE 17: PIN 1. VCC 2. V2OUT 3. V1OUT 4. TXE 5. RXE 6. VEE 7. GND 8. ACC	STYLE 18: PIN 1. ANODE 2. ANODE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. CATHODE 8. CATHODE	STYLE 19: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. MIRROR 2 7. DRAIN 1 8. MIRROR 1	STYLE 20: PIN 1. SOURCE (N) 2. GATE (N) 3. SOURCE (P) 4. GATE (P) 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
STYLE 21: PIN 1. CATHODE 1 2. CATHODE 2 3. CATHODE 3 4. CATHODE 4 5. CATHODE 5 6. COMMON ANODE 7. COMMON ANODE 8. CATHODE 6	STYLE 22: PIN 1. I/O LINE 1 2. COMMON CATHODE/VCC 3. COMMON CATHODE/VCC 4. I/O LINE 3 5. COMMON ANODE/GND 6. I/O LINE 4 7. I/O LINE 5 8. COMMON ANODE/GND	STYLE 23: PIN 1. LINE 1 IN 2. COMMON ANODE/GND 3. COMMON ANODE/GND 4. LINE 2 IN 5. LINE 2 OUT 6. COMMON ANODE/GND 7. COMMON ANODE/GND 8. LINE 1 OUT	STYLE 24: PIN 1. BASE 2. EMITTER 3. COLLECTOR/ANODE 4. COLLECTOR/ANODE 5. CATHODE 6. CATHODE 7. COLLECTOR/ANODE 8. COLLECTOR/ANODE
STYLE 25: PIN 1. VIN 2. N/C 3. REXT 4. GND 5. IOUT 6. IOUT 7. IOUT 8. IOUT	STYLE 26: PIN 1. GND 2. dv/dt 3. ENABLE 4. ILIMIT 5. SOURCE 6. SOURCE 7. SOURCE 8. VCC	STYLE 27: PIN 1. ILIMIT 2. OVLO 3. UVLO 4. INPUT+ 5. SOURCE 6. SOURCE 7. SOURCE 8. DRAIN	STYLE 28: PIN 1. SW_TO_GND 2. DASIC_OFF 3. DASIC_SW_DET 4. GND 5. V_MON 6. VBULK 7. VBULK 8. VIN
STYLE 29: PIN 1. BASE, DIE #1 2. EMITTER, #1 3. BASE, #2 4. EMITTER, #2 5. COLLECTOR, #2 6. COLLECTOR, #2 7. COLLECTOR, #1 8. COLLECTOR, #1	STYLE 30: PIN 1. DRAIN 1 2. DRAIN 1 3. GATE 2 4. SOURCE 2 5. SOURCE 1/DRAIN 2 6. SOURCE 1/DRAIN 2 7. SOURCE 1/DRAIN 2 8. GATE 1		

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