

MOSFET - Power, Single N-Channel, TOLL 80 V, 1.05 mΩ, 351 A



ON Semiconductor®

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NTBLS1D1N08H

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- Lowers Switching Noise/EMI
- These Devices are Pb-Free and are RoHS Compliant

Typical Applications

- Power Tools, Battery Operated Vacuums
- UAV/Drones, Material Handling
- BMS/Storage, Home Automation

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	V_{DSS}	80	V	
Gate-to-Source Voltage	V_{GS}	± 20	V	
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	$T_C = 25^\circ\text{C}$	351	A
		$T_C = 100^\circ\text{C}$	248	
Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	311	W
		$T_C = 100^\circ\text{C}$	156	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	$T_A = 25^\circ\text{C}$	41	A
		$T_A = 100^\circ\text{C}$	29	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25^\circ\text{C}$	4.2	W
		$T_A = 100^\circ\text{C}$	2.1	
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	I_{DM}	900	A
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +175	$^\circ\text{C}$	
Source Current (Body Diode)	I_S	259	A	
Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 31.9 \text{ A}$)	E_{AS}	1580	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$	

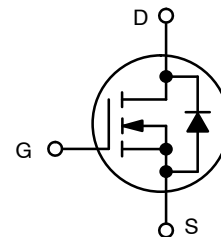
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State	$R_{\theta JC}$	0.48	$^\circ\text{C}/\text{W}$
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	35.8	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(ON) MAX}$	$I_D MAX$
80 V	1.05 mΩ @ 10 V	351 A

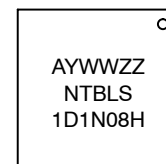


N-CHANNEL MOSFET



TOLL
CASE 100CU

MARKING DIAGRAM



NTBLS1D1N08H = Specific Device Code

A = Assembly Location

Y = Year

WW = Work Week

ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			57		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 80 V	T _J = 25 °C		10	μA
			T _J = 125°C		250	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = 20 V			100	nA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 650 μA	2.0	2.9	4.0	V
Threshold Temperature Coefficient	V _{GS(TH)} /T _J			-7.7		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 50 A		0.92	1.05	mΩ
Forward Transconductance	g _{FS}	V _{DS} = 5 V, I _D = 50 A		213		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 40 V		11200		pF
Output Capacitance	C _{OSS}			1600		
Reverse Transfer Capacitance	C _{RSS}			49		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 64 V; I _D = 50 A		166		nC
Threshold Gate Charge	Q _{G(TH)}			29		
Gate-to-Source Charge	Q _{GS}			44		
Gate-to-Drain Charge	Q _{GD}			35		
Plateau Voltage	V _{GP}			4		V

SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = 10 V, V _{DS} = 64 V, I _D = 50 A, R _G = 6 Ω		45		ns
Rise Time	t _r			43		
Turn-Off Delay Time	t _{d(OFF)}			141		
Fall Time	t _f			43		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 50 A	T _J = 25°C		0.76	1.2	V
			T _J = 125°C		0.6		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 50 A		92		ns	
Reverse Recovery Charge	Q _{RR}			234		nC	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

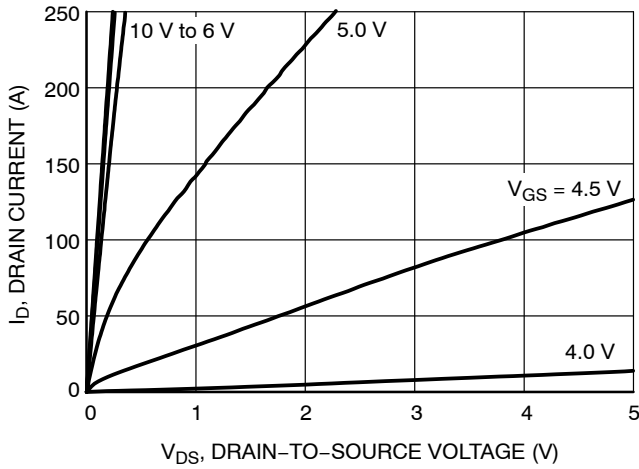


Figure 1. On-Region Characteristics

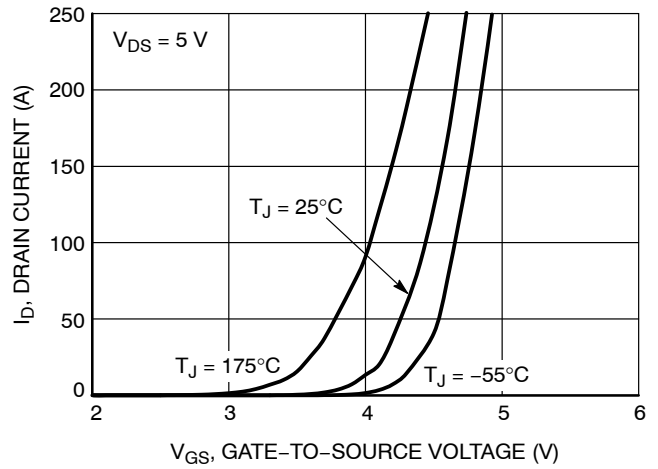


Figure 2. Transfer Characteristics

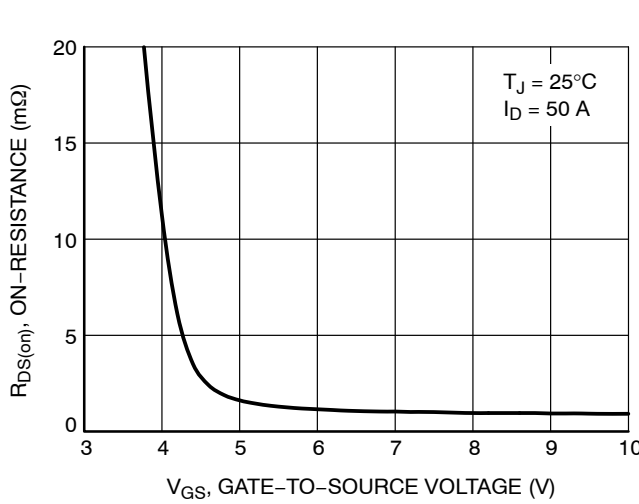


Figure 3. On-Resistance vs. Gate-to-Source Voltage

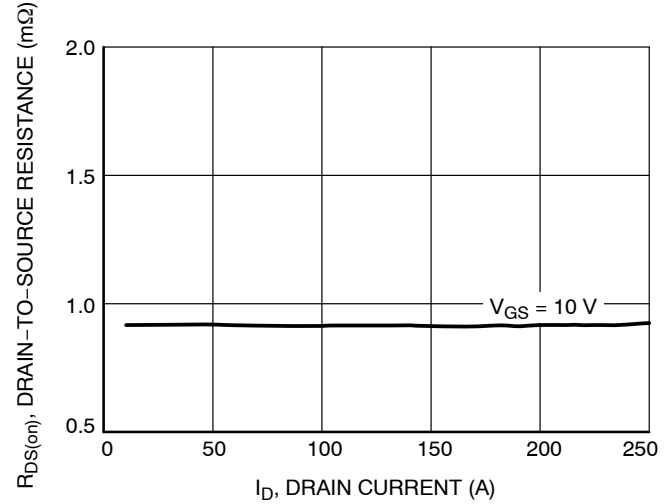


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

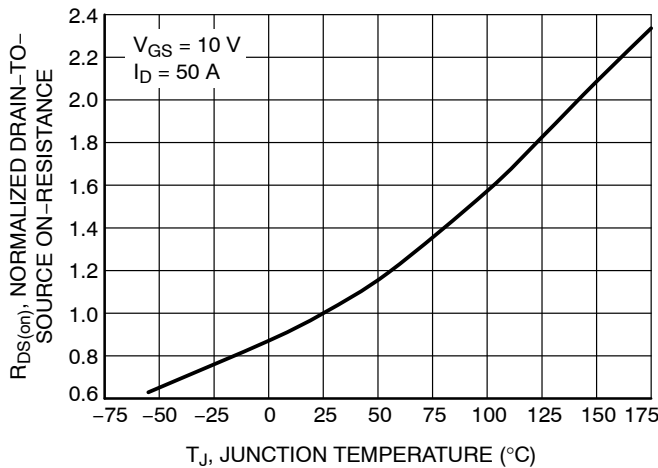


Figure 5. On-Resistance Variation with Temperature

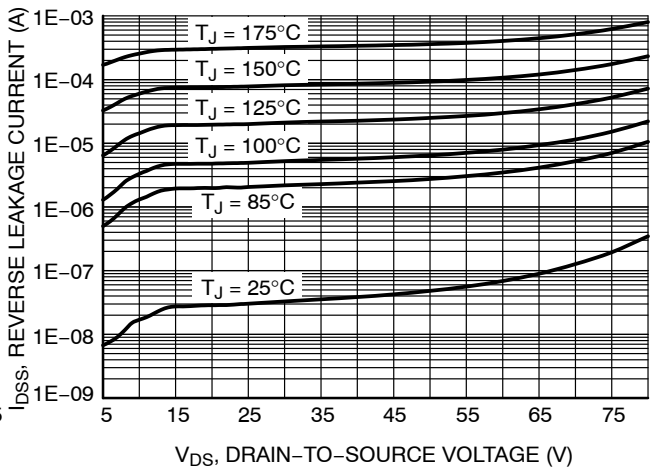


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

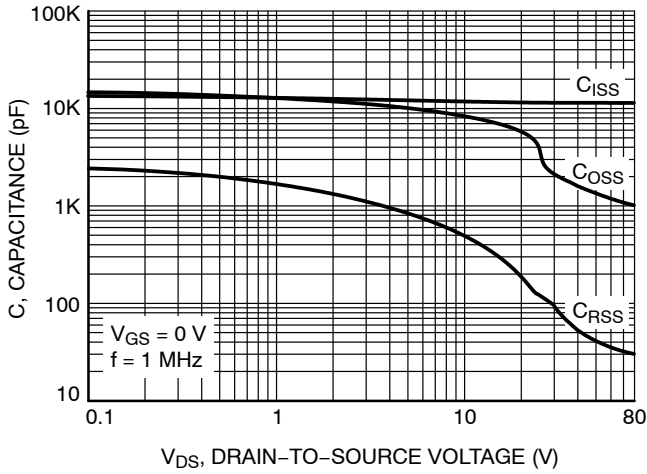


Figure 7. Capacitance Variation

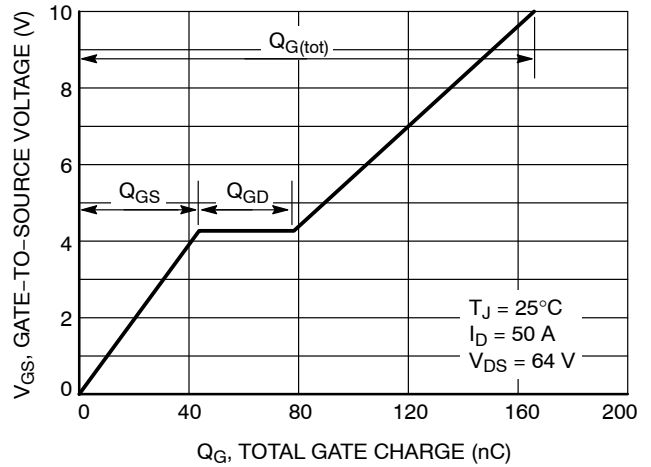


Figure 8. Gate-to-Source Voltage vs. Total Charge

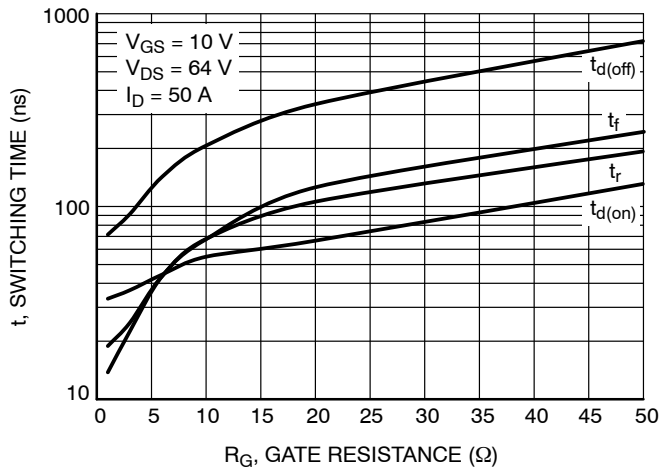


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

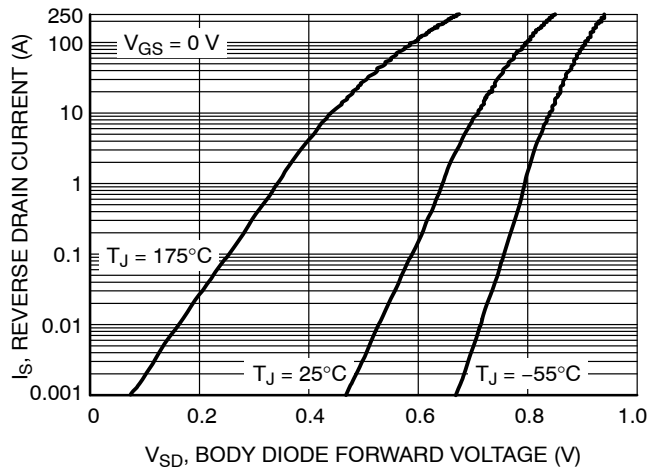


Figure 10. Diode Forward Voltage vs. Current

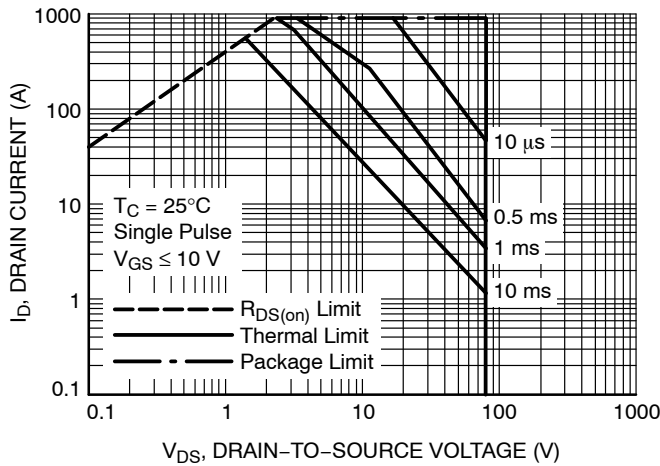


Figure 11. Maximum Rated Forward Biased Safe Operating Area

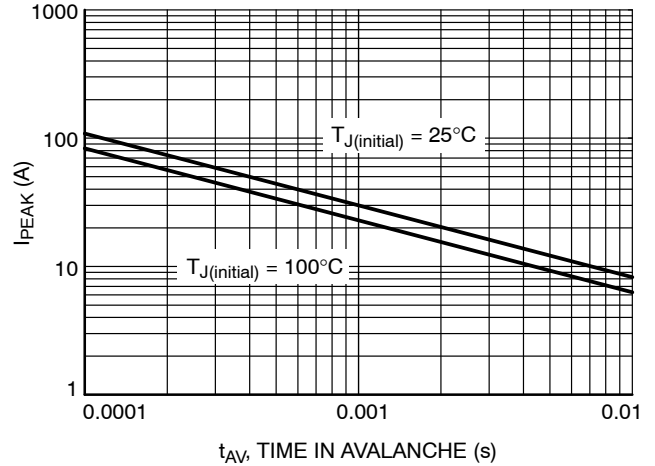


Figure 12. Maximum Drain Current vs. Time in Avalanche

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TYPICAL CHARACTERISTICS

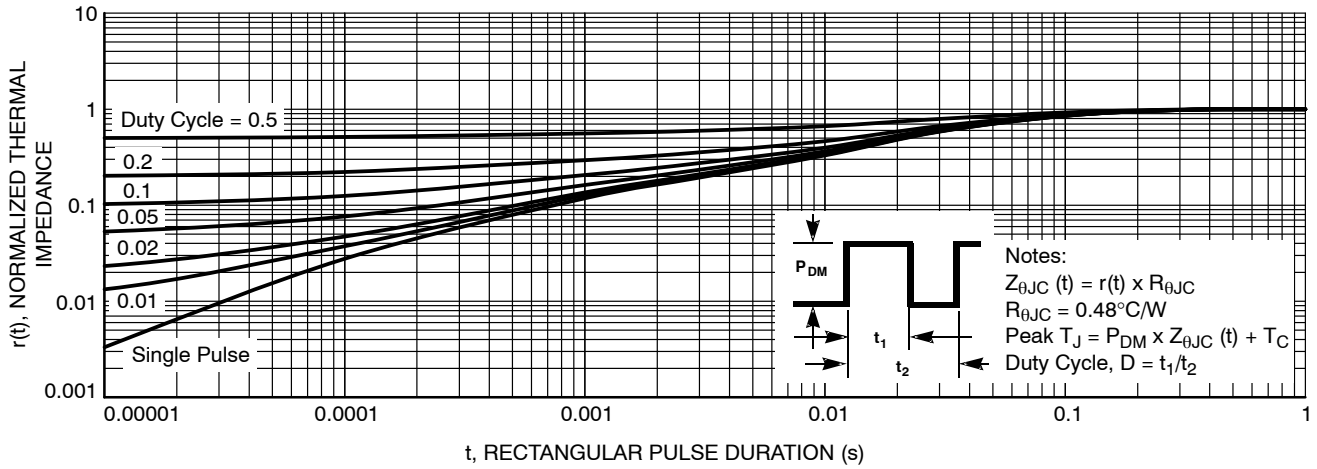


Figure 13. Transient Thermal Impedance

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NTBLS1D1N08H	NTBLS 1D1N08H	M0-299A (Pb-Free)	2000 / Tape & Reel

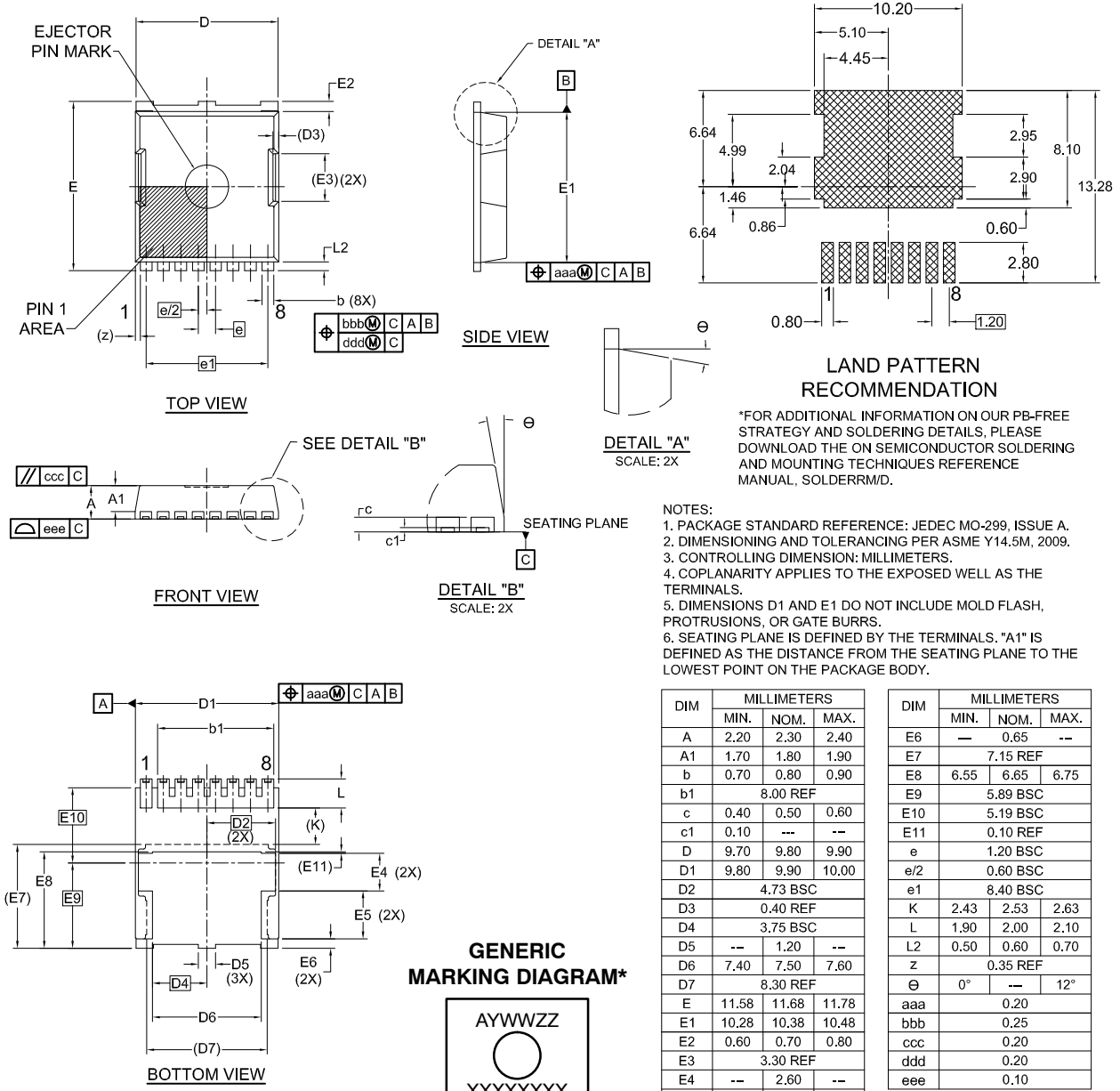
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



H-PSOF8L 11.68x9.80 CASE 100CU ISSUE B

DATE 20 MAY 2022



LAND PATTERN RECOMMENDATION

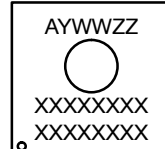
*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

- NOTES:
1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE A.
 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
 3. CONTROLLING DIMENSION: MILLIMETERS.
 4. COPLANARITY APPLIES TO THE EXPOSED WELL AS THE TERMINALS.
 5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
 6. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	8.00 REF		
c	0.40	0.50	0.60
c1	0.10	---	---
D	9.70	9.80	9.90
D1	9.80	9.90	10.00
D2	4.73 BSC		
D3	0.40 REF		
D4	3.75 BSC		
D5	---	1.20	---
D6	7.40	7.50	7.60
D7	8.30 REF		
E	11.58	11.68	11.78
E1	10.28	10.38	10.48
E2	0.60	0.70	0.80
E3	3.30 REF		
E4	---	2.60	---
E5	---	3.30	---

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E6	---	0.65	---
E7	7.15 REF		
E8	6.55	6.65	6.75
E9	5.89 BSC		
E10	5.19 BSC		
E11	0.10 REF		
e	1.20 BSC		
e/2	0.60 BSC		
e1	8.40 BSC		
K	2.43	2.53	2.63
L	1.90	2.00	2.10
L2	0.50	0.60	0.70
z	0.35 REF		
θ	0°	---	12°
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.10		

GENERIC MARKING DIAGRAM*



- A = Assembly Location
- Y = Year
- WW = Work Week
- ZZ = Assembly Lot Code
- XXXX = Specific Device Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "a", may or may not be present. Some products may not follow the Generic Marking.

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