

# nRF5340

## Objective Product Specification

v0.5

# nRF5340 features

## Features:

- 1.7 V to 5.5 V supply voltage range
- Single 32 MHz crystal operation
- Package: aQFN-94
- 1.8 V to 3.3 V regulated supply for external components
- Operating temperature: -40 to +105 °C

## Application core:

- Arm® Cortex®-M33 with TrustZone® technology
  - 128 MHz or 64 MHz operation
  - 510 EEMBC CoreMark score running from flash memory
  - Single-precision floating-point unit (FPU)
  - Digital signal processing (DSP) instructions
  - Data watchpoint and trace (DWT), embedded trace macrocell (ETM), instrumentation trace macrocell (ITM), and cross trigger interface (CTI)
  - Serial wire debug (SWD)
  - Trace port interface unit (TPIU)
    - 4-bit parallel trace of ITM and ETM trace data
    - Serial wire output (SWO) trace of ITM data
- 1 MB flash and 512 kB low leakage RAM
- Arm TrustZone CryptoCell™ -312 security subsystem
  - NIST 800-90B, AIS-31, and FIPS 140-2 compliant random number generator
  - AES-128 and 256: ECB, CBC, CMAC/CBC-MAC, CTR, CCM/CCM\*, GCM
  - SHA-1, SHA-2 up to 256 bits
  - Keyed-hash message authentication code (HMAC)
  - RSA public key cryptography with up to 3072-bit key size
  - ECC support for most used curves
  - Application key management using derived key model
- Two-way set associative cache towards flash and QSPI XIP code regions
- QSPI peripheral for communicating with an external flash memory device
- Near field communication (NFC-A) tag with wake-on field
  - Touch-to-pair support
- Up to 3x SPI master/slave with EasyDMA
- Up to 2x I2C compatible two-wire master/slave with EasyDMA
- Up to 2x UART (CTS/RTS) with EasyDMA
  - Optional, built-in, flow control (CTS, RTS)
- Audio peripherals: I2S, digital microphone interface (PDM)
- Up to 3x pulse width modulator (PWM) units with EasyDMA
- 12-bit, 200 ksp/s ADC with EasyDMA - eight configurable channels with programmable gain
- Up to 3x 32-bit timer with counter mode
- Up to 2x 24-bit real-time counter (RTC)
- Quadrature decoder (QDEC)
- Distributed programmable peripheral interconnect (DPPI)
- Inter-processor communication (IPC)
- Mutually exclusive peripheral (MUTEX)
- 48 general purpose I/O pins

## Network core:

- Arm Cortex-M33
  - 64 MHz operation
  - 238 EEMBC CoreMark score running from flash memory
  - Cross trigger interface (CTI)
  - Serial wire debug (SWD)
  - SWO trace port
- 256 kB flash
- 64 kB low leakage RAM
- Bluetooth® 5.1, IEEE 802.15.4-2006, 2.4 GHz transceiver
  - -97.5 dBm sensitivity in 1 Mbps Bluetooth low energy mode
  - -20 to +3 dBm configurable TX power
- On-air compatible with nRF52, nRF51, nRF24L, and nRF24AP Series
- Supported data rates:
  - Bluetooth 5.1: 2 Mbps, 1 Mbps, 500 kbps, and 125 kbps
  - IEEE 802.15.4-2006: 250 kbps
  - Proprietary 2.4 GHz: 2 Mbps, 1 Mbps
- Single-ended antenna output (on-chip balun)
- 128-bit AES/ECB/CCM/AAR co-processor (on-the-fly packet encryption)
- 3.2 mA run current in TX (0 dBm)
- 2.6 mA run current in RX
- RSSI (1 dB resolution)
- SPI master/slave with EasyDMA
- I2C compatible two-wire master/slave with EasyDMA
- UART (CTS/RTS) with EasyDMA
- Up to 3x 32-bit timer with counter mode
- Up to 2x real-time counter (RTC)
- Temperature sensor
- Distributed programmable peripheral interconnect (DPPI)
- Inter-processor communication (IPC)
- Mutually exclusive peripheral (MUTEX)

**Applications:**

- Advanced computer peripherals and I/O devices
  - Multi-touch trackpad
- Advanced wearables
  - Health/fitness sensor and monitor devices
  - Wireless payment enabled devices
- Internet of things (IoT)
  - Smart home sensors and controllers
  - Industrial IoT sensors and controllers
- Interactive entertainment devices
  - Remote controls
  - Gaming controllers

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# 1 Revision history

| Date          | Version | Description   |
|---------------|---------|---------------|
| November 2019 | 0.5     | First release |

# 2 About this document

This document is organized into chapters that are based on the modules and peripherals available in the IC.

## 2.1 Document status

The document status reflects the level of maturity of the document.

| Document name                         | Description                                                                                                                                                                                                                                                      |
|---------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Objective Product Specification (OPS) | Applies to document versions up to 1.0.<br><br>This document contains target specifications for product development.                                                                                                                                             |
| Product Specification (PS)            | Applies to document versions 1.0 and higher.<br><br>This document contains final product specifications. Nordic Semiconductor ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |

Table 1: Defined document names

## 2.2 Peripheral chapters

Every peripheral has a unique capitalized name or an abbreviation of its name, e.g. TIMER, used for identification and reference. This name is used in chapter headings and references, and it will appear in the ARM Cortex Microcontroller Software Interface Standard (CMSIS) hardware abstraction layer to identify the peripheral.

The peripheral instance name, which is different from the peripheral name, is constructed using the peripheral name followed by a numbered postfix, starting with 0, for example, TIMER0. A postfix is normally only used if a peripheral can be instantiated more than once. The peripheral instance name is also used in the CMSIS to identify the peripheral instance.

The chapters describing peripherals may include the following information:

- A detailed functional description of the peripheral
- Register configuration for the peripheral
- Electrical specification tables, containing performance data which apply for the operating conditions described in [Recommended operating conditions](#) on page 773.

## 2.3 Register tables

Individual registers are described using register tables. These tables are built up of two sections. The first three colored rows describe the position and size of the different fields in the register. The following rows describe the fields in more detail.

### 2.3.1 Fields and values

The **Id (Field Id)** row specifies the bits that belong to the different fields in the register. If a field has enumerated values, then every value will be identified with a unique value id in the **Value Id** column.

A blank space means that the field is reserved and read as undefined, and it also must be written as 0 to secure forward compatibility. If a register is divided into more than one field, a unique field name is specified for each field in the **Field** column. The **Value Id** may be omitted in the single-bit bit fields when values can be substituted with a Boolean type enumerator range, e.g. true/false, disable(d)/enable(d), on/off, and so on.

Values are usually provided as decimal or hexadecimal. Hexadecimal values have a 0x prefix, decimal values have no prefix.

The **Value** column can be populated in the following ways:

- Individual enumerated values, for example 1, 3, 9.
- Range of values, e.g. [0..4], indicating all values from and including 0 and 4.
- Implicit values. If no values are indicated in the **Value** column, all bit combinations are supported, or alternatively the field's translation and limitations are described in the text instead.

If two or more fields are closely related, the **Value Id**, **Value**, and **Description** may be omitted for all but the first field. Subsequent fields will indicate inheritance with '..'.

A feature marked **Deprecated** should not be used for new designs.

### 2.3.2 Permissions

Different fields in a register might have different access permissions enforced by hardware.

The access permission for each register field is documented in the **Access** column in the following ways:

| Access | Description     | Hardware behavior                                                                                                      |
|--------|-----------------|------------------------------------------------------------------------------------------------------------------------|
| RO     | Read-only       | Field can only be read. A write will be ignored.                                                                       |
| WO     | Write-only      | Field can only be written. A read will return an undefined value.                                                      |
| RW     | Read-write      | Field can be read and written multiple times.                                                                          |
| W1     | Write-once      | Field can only be written once per reset. Any subsequent write will be ignored. A read will return an undefined value. |
| RW1    | Read-write-once | Field can be read multiple times, but only written once per reset. Any subsequent write will be ignored.               |

Table 2: Register field permission schemes

## 2.4 Registers

| Register | Offset | Security | Description                                       |
|----------|--------|----------|---------------------------------------------------|
| DUMMY    | 0x514  |          | Example of a register controlling a dummy feature |

Table 3: Register overview

### 2.4.1 DUMMY

Address offset: 0x514

Example of a register controlling a dummy feature

| Bit number       |      |         | 31           | 30 | 29     | 28 | 27                                                              | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1          | 0 |
|------------------|------|---------|--------------|----|--------|----|-----------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|------------|---|
| ID               |      |         |              |    |        |    | D                                                               | D  | D  | D  |    |    |    |    | C  | C  | C  |    |    |    |    | B  |    |    |   |   | A | A |   |   |   |   |            |   |
| Reset 0x00050002 |      |         | 0            | 0  | 0      | 0  | 0                                                               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1          | 0 |
| ID               | Acce | Field   | Value ID     |    | Value  |    | Description                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |            |   |
| A                | RW   | FIELD_A |              |    |        |    | Example of a read-write field with several enumerated values    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |            |   |
|                  |      |         | Disabled     |    | 0      |    | The example feature is disabled                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |            |   |
|                  |      |         | NormalMode   |    | 1      |    | The example feature is enabled in normal mode                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |            |   |
|                  |      |         | ExtendedMode |    | 2      |    | The example feature is enabled along with extra functionality   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |            |   |
| B                | RW   | FIELD_B |              |    |        |    | Example of a deprecated read-write field                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | Deprecated |   |
|                  |      |         | Disabled     |    | 0      |    | The override feature is disabled                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |            |   |
|                  |      |         | Enabled      |    | 1      |    | The override feature is enabled                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |            |   |
| C                | RW   | FIELD_C |              |    |        |    | Example of a read-write field with a valid range of values      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |            |   |
|                  |      |         | ValidRange   |    | [2..7] |    | Example of allowed values for this field                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |            |   |
| D                | RW   | FIELD_D |              |    |        |    | Example of a read-write field with no restriction on the values |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |            |   |

# 3 Product overview

nRF5340 is a wireless ultra-low power multicore System on Chip (SoC), integrating two fully programmable Arm Cortex-M33 processors, advanced security features, a range of peripherals, and a multiprotocol 2.4 GHz transceiver. The transceiver supports Bluetooth Low Energy, ANT<sup>™</sup>, and 802.15.4 and allows the implementation of proprietary 2.4 GHz protocols.

The two Arm Cortex-M33 processors share the power, clock, and peripheral architecture with Nordic Semiconductor nRF51, nRF52, and nRF91 Series of PAN/LAN SoCs, ensuring minimal porting efforts. The application core is a full-featured Arm Cortex-M33 processor including DSP instructions and FPU and running at up to 128 MHz with 1 MB of flash and 512 kB of RAM. The option to run the application processor at 64 MHz allows the CPU to increase energy efficiency. The network core is an Arm Cortex-M33 processor with a reduced feature set, designed for ultra-low power operation. It runs at a fixed 64 MHz frequency and contains 256 kB of flash and 64 kB of RAM.

The peripheral set offers a variety of analog and digital functionality enabling single-chip implementation of a wide range of applications. Arm TrustZone technology, Arm CryptoCell-312, and supporting blocks for system protection and key management are embedded for the advanced security needed for IoT applications.

## 3.1 Block diagram

The block diagram illustrates the overall system. More detailed diagrams of the two cores, including pins and EasyDMA connectivity, can be found in [Application core overview](#) on page 92 and [Network core overview](#) on page 122.

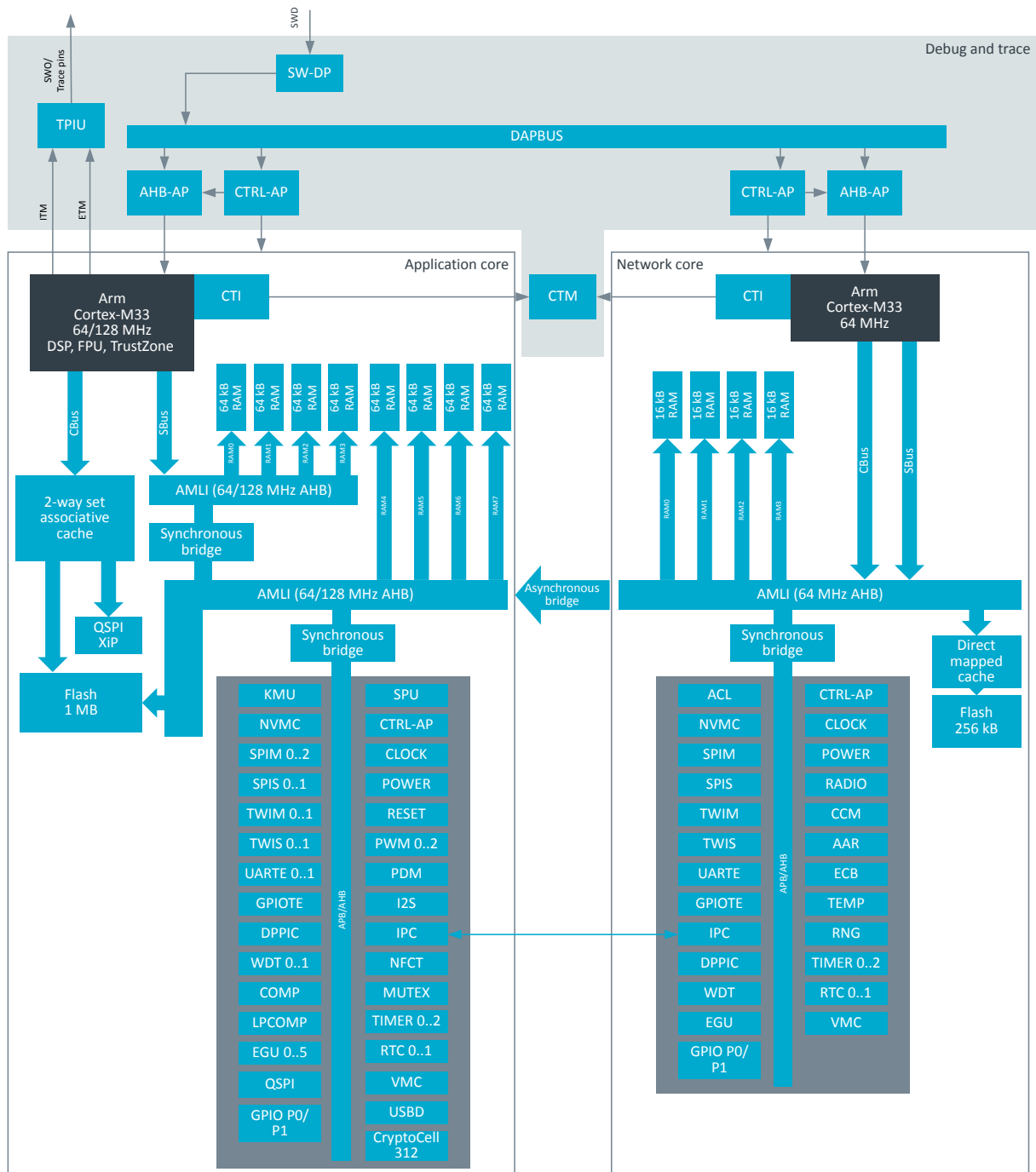


Figure 1: Simplified block diagram

## 3.2 Memory

The nRF5340 SoC contains two processor cores each with flash and RAM that can be used for code and data storage.

| Core             | RAM                                                                                                                                              | Flash                 |
|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|
| Application core | 512 kB, arranged as follows: <ul style="list-style-type: none"> <li>• 256 kB CPU single-cycle RAM</li> <li>• 256 kB of peripheral RAM</li> </ul> | 1024 kB in 4 kB pages |
| Network core     | 64 kB total                                                                                                                                      | 256 kB in 2 kB pages  |

Table 4: nRF5340 memory configuration

All memory and registers are found in the same address space, as shown in [Figure 2: Memory map](#) on page 20. This includes the two blocks of 256 kB RAM, which are accessible in the memory map as one contiguous 512 kB block of RAM.

The application core memory is mapped to the network core memory map. This means that the network core can access and use the application core memory for shared memory communication. The application core can restrict network core access through the domain configuration (DCNF) PROTECT registers, see [DCNF — Domain configuration](#) on page 186. Access to secure memory or peripherals as defined by the [SPU — System protection unit](#) on page 568 is also prevented when the network core is marked as non-secure in an application using TrustZone technology.

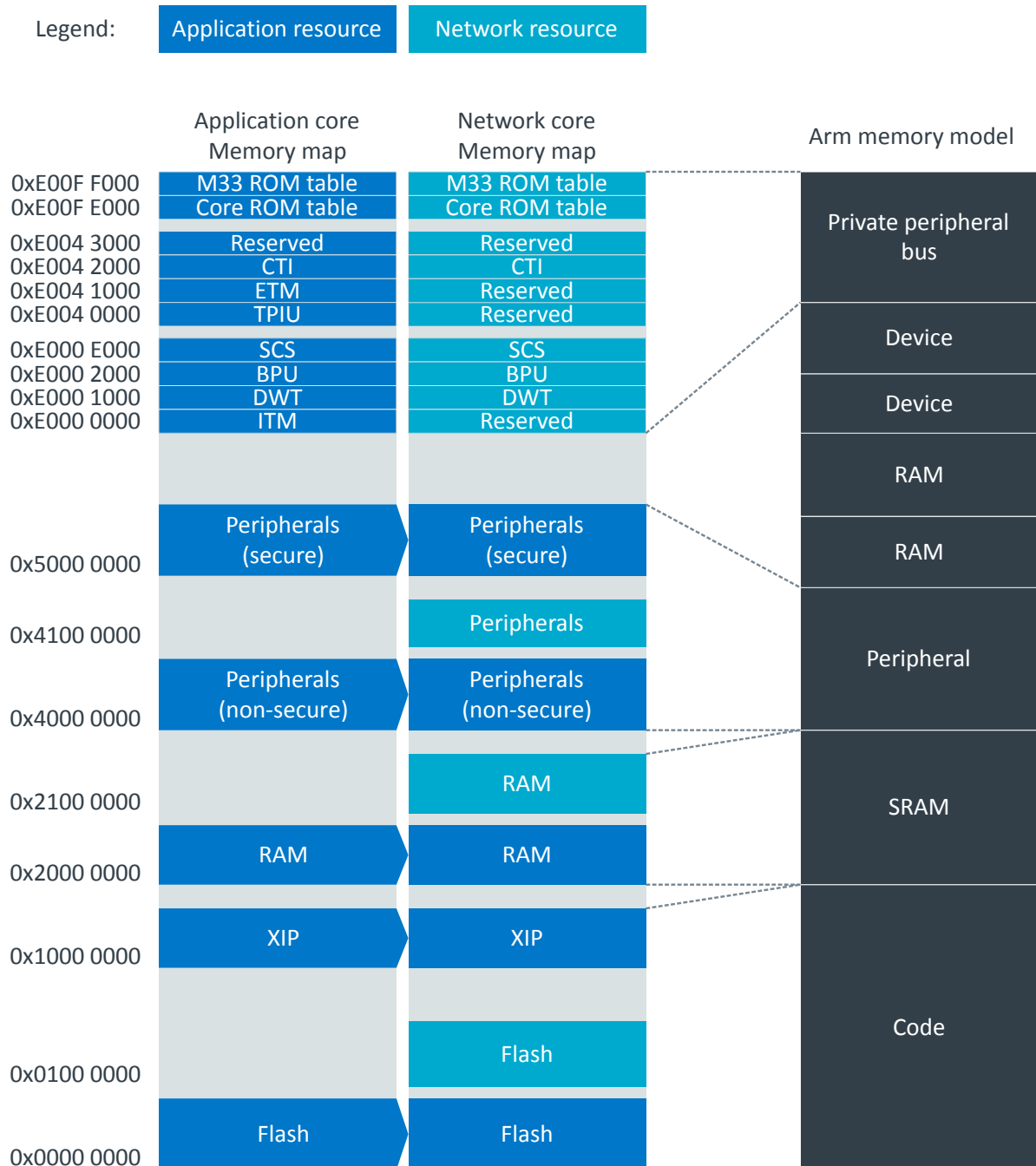


Figure 2: Memory map

### 3.2.1 RAM - Random access memory

RAM can be read and written an unlimited number of times.

Each RAM AHB slave within a core is connected to one or more RAM sections that has separate power control for System ON and System OFF mode operation. For details, see [VMC — Volatile memory controller](#) on page 719.

### 3.2.2 Flash (non-volatile memory)

Flash memory can be read an unlimited number of times by the CPU, but is restricted in the number of times it can be written to or erased, and in how it can be written.

Writing to flash memory is managed by the non-volatile memory controller (NVMC), see [NVMC — Non-volatile memory controller](#) on page 318.



Flash memory is divided in pages, as listed in [Table 4: nRF5340 memory configuration](#) on page 19.

### 3.2.3 XIP - Execute in place

Execute in Place (XIP) allows the CPU to execute program code directly from the external flash memory device using the Quad serial peripheral interface (QSPI).

For details, see [QSPI — Quad serial peripheral interface](#) on page 380.

### 3.2.4 Access latency

When accessing memories or peripherals across bus bridges, additional access latency will occur. An example of such a case is network core access to application core memory or peripherals.

# 4 Power and clock management

## 4.1 Overview

The power and clock management system in nRF5340 is optimized for ultra-low power applications to ensure maximum power efficiency.

The core of the power and clock management system is the power management unit (PMU) shown in the following figure.

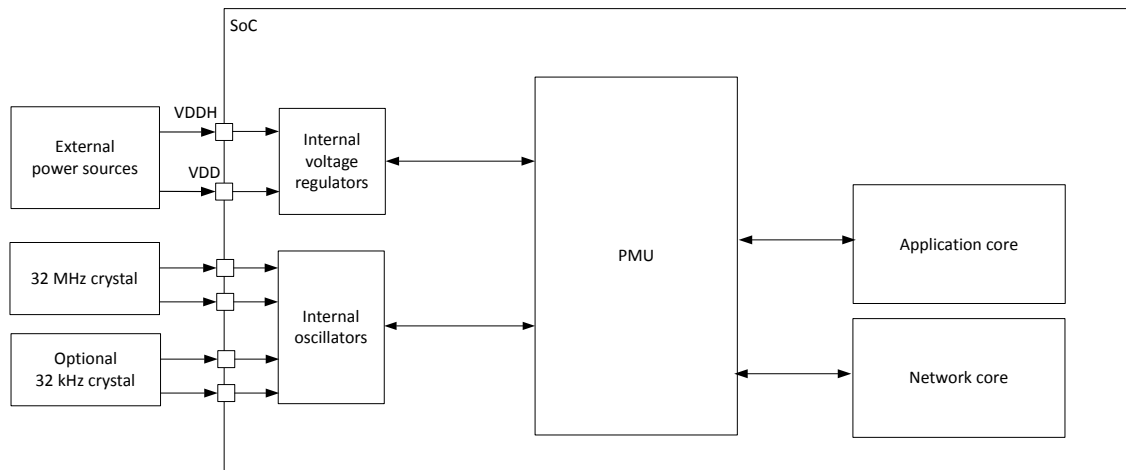


Figure 3: Power management unit

The PMU automatically tracks the power and clock resources required by the different components in the system at any given time. To achieve the lowest power consumption possible, the PMU optimizes the system by evaluating power and clock requests, automatically starting and stopping clock sources, and choosing regulator operation modes.

### 4.1.1 System ON mode

System ON is the default operation mode after power-on reset.

In System ON, all functional blocks, such as the CPU and peripherals, can be in an idle or run state depending on the configuration set by the software and the state of the executing application. The network core's CPU and peripherals can be in an idle state, run state, System OFF mode (see [System OFF mode](#) on page 23), or Force-off mode (see [Core Force-off mode](#) on page 24).

The PMU can switch the appropriate internal power sources on and off, depending on how much power is needed at any given time. The power requirement of a peripheral is directly related to its activity level, which increases and decreases when specific tasks are triggered or events are generated.

### Voltage and frequency scaling

nRF5340 allows frequency scaling of the application core. Changing the frequency of the application core's clock will change the internal voltage to optimize power efficiency, which is a trade off between performance and power consumption. For more information, see [Application core frequency scaling](#) on page 64.

#### 4.1.1.1 Power submodes

In System ON mode, when the CPU and all peripherals are IDLE, the system can reside in one of two power submodes.

The power submodes are:

- Constant latency
- Low-power

In Constant latency, the CPU wakeup latency and the PPI task response will be constant and kept at a minimum. This is secured by a set of resources that are always enabled. Compared to Low-power, the advantage of having a constant and predictable latency comes at a cost of increased power consumption. Constant latency is selected by triggering the [CONSTLAT](#) task.

In Low-power, the most power efficient supply option is chosen by the automatic power management system. Achieving the lowest power possible is at the expense of variations in CPU wakeup latency and PPI task response. Low-power is selected by triggering the [LOWPWR](#) task.

When the system enters System ON, it is by default in the Low-power submode.

#### 4.1.2 System OFF mode

System OFF is the deepest power-saving mode the system can enter. In this mode, the system's core functionality is powered down and all ongoing tasks are terminated.

The device can be put into System OFF mode using the register [SYSTEMOFF](#) on page 44 . The following signals/actions cause a wakeup from System OFF:

- The DETECT signal, generated by the GPIO peripheral
- The ANADETECT signal, generated by the LPCOMP peripheral
- The SENSE signal, generated by the NFCT peripheral to wake-on-field
- A valid USB voltage on the VBUS pin is detected
- A debug session is started
- Pin reset

When the device wakes up from System OFF, a system reset is performed. For more details, see [Application core reset behavior](#) on page 57.

One or more RAM sections can be retained in System OFF depending on the RAM retention settings in the peripheral [VMC — Volatile memory controller](#) on page 719.

Before entering System OFF, all on-going EasyDMA transactions should be completed. This is accomplished by making sure that the EasyDMA enabled peripheral is not active when entering System OFF. It is also recommended that the network core is in an idle state (i.e. peripherals are stopped and CPU is idle).

##### 4.1.2.1 Emulated System OFF mode

When the device is in Debug Interface mode, System OFF is emulated to ensure that all required resources needed for debugging are available during System OFF.

Required resources needed for debugging include the following key components:

- [Debug interface mode](#) on page 731
- [CLOCK — Clock control](#) on page 61
- [POWER — Power control](#) on page 36
- [OSCILLATORS — Oscillator control](#) on page 88
- [REGULATORS - Regulator control](#) on page 41
- [RESET - Reset control](#) on page 55
- [NVMC — Non-volatile memory controller](#) on page 318
- CPU

- Flash memory
- RAM

Because the CPU is kept on in an emulated System OFF mode, it is recommended to add an infinite loop directly after entering System OFF, to prevent the CPU from executing code that normally should not be executed. For more information, see [Overview](#) on page 730.

### 4.1.3 Core Force-off mode

Core Force-off is only applicable for the network core.

The register interface [RESET - Reset control](#) on page 55 is used by the application core to set the network core to Force-off mode. This stops the network core in order to achieve the lowest power consumption possible. When the network core is in Force-off mode, only the application core can release the mode, causing the network core to wake up and start the CPU again.

Before the application core sets the network core to Force-off mode, it is recommended that the network core is in an idle state (i.e. peripherals are stopped and CPU is idle).

When the network core wakes up from Force-off mode, it is reset. For more details, see [Network core reset behavior](#) on page 58.

Several RAM sections can be retained in Force-off mode depending on the RAM retention settings in the peripheral [VMC — Volatile memory controller](#) on page 719.

#### 4.1.3.1 Emulated Force-off mode

If the device is in Debug Interface mode, Force-off mode will be emulated to secure the required resources needed for debugging.

When Force-off mode is emulated, the CPU and all peripherals are reset. The CPU is prevented from running during debug access to a core's resources, including writing to RAM, flash, and/or peripherals. See [Overview](#) on page 730 for more information.

## 4.2 Current consumption

Because the Power Management Unit (PMU) is constantly adjusting the different power and clock sources, estimating an application's current consumption can be challenging when the measurements cannot be performed directly on the hardware. To facilitate the estimation process, a set of current consumption scenarios is provided to show the typical current drawn from the VDD or VDDH supply.

Each scenario specifies a set of operations and conditions applying to the given scenario. All scenarios are listed in [Electrical specification](#) on page 26. The following table shows a set of common conditions used in all scenarios, unless otherwise stated in the description of a given scenario.

| Condition               | Value                                                                                                                                                                                                                                                              | Note                                                                                                                                                                              |
|-------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Supply                  | 3 V on VDD/VDDH (normal voltage mode)                                                                                                                                                                                                                              |                                                                                                                                                                                   |
| Temperature             | 25 °C                                                                                                                                                                                                                                                              |                                                                                                                                                                                   |
| CPU                     | WFI (wait for interrupt)/WFE (wait for event) sleep                                                                                                                                                                                                                |                                                                                                                                                                                   |
| Peripherals             | All idle                                                                                                                                                                                                                                                           |                                                                                                                                                                                   |
| Clock                   | HFCLK = HFINT @ 64 MHz, LFCLK = Not running                                                                                                                                                                                                                        |                                                                                                                                                                                   |
| Regulator               | DC/DC on VREGMAIN, VREGRADIO, and VREGH (when used)                                                                                                                                                                                                                |                                                                                                                                                                                   |
| Application core RAM    | 8 kB                                                                                                                                                                                                                                                               | In System ON, RAM value refers to the amount of RAM that is switched on. The remainder of RAM is non retained. In System OFF, RAM value refers to amount of RAM that is retained. |
| Network core RAM        | 0 kB                                                                                                                                                                                                                                                               |                                                                                                                                                                                   |
| Compiler                | GCC version 7.3.1 20180622 (arm-none-eabi-gcc). Compiler flags:- mcpu=cortex-m33 -mthumb -mabi=aapcs -mfpv5-sp-d16 -mfloat-abi=hard -O3 -ffunction-sections -fdata-sections -fno-strict-aliasing -fno-builtin --short-enums -falign-functions=16 -std=gnu99 -Wall. |                                                                                                                                                                                   |
| Cache enabled           | Yes                                                                                                                                                                                                                                                                | Only applies when the CPU is running from flash memory.                                                                                                                           |
| Network core forced off | Yes                                                                                                                                                                                                                                                                |                                                                                                                                                                                   |
| 32 MHz crystal          | SMD 2520, 32 MHz, 10 pF +/- 10 ppm                                                                                                                                                                                                                                 | Only applies when the high frequency crystal oscillator (HFXO) is running. HFXO is used when the radio is running.                                                                |
| 32 kHz crystal          | SMD 3215, 32.768 kHz, 9 pF +/- 50 ppm                                                                                                                                                                                                                              | Only applies when the low frequency crystal oscillator (LFXO) is running.                                                                                                         |
| Inductors               | Murata LQH2MPN100MGR                                                                                                                                                                                                                                               |                                                                                                                                                                                   |

Table 5: Current consumption scenarios, common conditions

## 4.2.1 Electrical specification

### 4.2.1.1 Sleep

| Symbol                | Description                                                                                                      | Min. | Typ. | Max. | Units |
|-----------------------|------------------------------------------------------------------------------------------------------------------|------|------|------|-------|
| I <sub>ON_IDLE1</sub> | System ON, wake on any event, power-fail comparator enabled                                                      |      | 1.5  |      | uA    |
| I <sub>ON_IDLE2</sub> | System ON, wake on GPIOTE input (event mode)                                                                     | ..   | ..   | ..   | uA    |
| I <sub>ON_IDLE3</sub> | System ON, wake on GPIOTE PORT event                                                                             | ..   | ..   | ..   | uA    |
| I <sub>ON_IDLE4</sub> | System ON, 0 kB application RAM, wake on RTC (running from LFXO clock)                                           | ..   | ..   | ..   | uA    |
| I <sub>ON_IDLE5</sub> | System ON, wake on RTC (running from LFXO clock)                                                                 | ..   | ..   | ..   | uA    |
| I <sub>ON_IDLE6</sub> | System ON, 0 kB application RAM, wake on RTC (running from LFXO clock), 5 V supply on VDDH, VREGH output = 3.3 V | ..   | ..   | ..   | uA    |
| I <sub>ON_IDLE7</sub> | System ON, 0 kB network RAM, wake on network RTC (running from LFXO clock)                                       |      | 1.6  |      | uA    |
| I <sub>ON_IDLE8</sub> | System ON, 64 kB network RAM, wake on network RTC (running from LFXO clock)                                      |      | 1.8  |      | uA    |
| I <sub>ON_IDLE9</sub> | System ON, 0 kB application RAM, wake on RTC (running from LFRC clock)                                           |      | 2.3  |      | uA    |
| I <sub>OFF0</sub>     | System Off, 0 kB application RAM, wake on reset                                                                  |      | 1.1  |      | uA    |
| I <sub>OFF1</sub>     | System Off, 0 kB application RAM, wake on LPCOMP                                                                 | ..   | ..   | ..   | uA    |
| I <sub>OFF2</sub>     | System Off, wake on reset                                                                                        | ..   | ..   | ..   | uA    |
| I <sub>OFF3</sub>     | System Off, 0 kB application RAM, wake on reset, 5 V supply on VDDH, VREGH output = 3.3V                         | ..   | ..   | ..   | uA    |
| I <sub>OFF4</sub>     | System Off, 512 kB application RAM + 64 kB network RAM, wake on reset                                            | ..   | ..   | ..   | uA    |

### 4.2.1.2 Application CPU running

**Note:** Compiler: ARM version 6.12 (armclang). Compiler flags: -std=c99 --target=arm-arm-none-eabi -mcpu=cortex-m33 -mfpu=fpv5-sp-d16 -mfloat-abi=hard -fno-rtti -flto -funsigned-char -mcmse -Omax -ffunction-sections. Linker flags: -Omax. Amount of RAM in Application CPU set to 20 kB in flash cases and 44 kB in RAM cases.

| Symbol                | Description                                                         | Min. | Typ. | Max. | Units |
|-----------------------|---------------------------------------------------------------------|------|------|------|-------|
| I <sub>APPCPU0</sub>  | CPU running CoreMark from flash, regulator = LDO, clock = HFINT128M |      | 14.0 |      | mA    |
| I <sub>APPCPU1</sub>  | CPU running CoreMark from flash, regulator = LDO                    | ..   | ..   | ..   | mA    |
| I <sub>APPCPU2</sub>  | CPU running CoreMark from flash, clock = HFXO128M                   |      | 7.3  |      | mA    |
| I <sub>APPCPU3</sub>  | CPU running CoreMark from flash, clock = HFXO64M                    |      | 3.4  |      | mA    |
| I <sub>APPCPU4</sub>  | CPU running CoreMark from flash, clock = HFINT128M                  |      | 7.1  |      | mA    |
| I <sub>APPCPU5</sub>  | CPU running CoreMark from flash                                     | ..   | ..   | ..   | mA    |
| I <sub>APPCPU6</sub>  | CPU running CoreMark from RAM, regulator = LDO, clock = HFINT128M   | ..   | ..   | ..   | mA    |
| I <sub>APPCPU7</sub>  | CPU running CoreMark from RAM, regulator = LDO                      | ..   | ..   | ..   | mA    |
| I <sub>APPCPU8</sub>  | CPU running CoreMark from RAM, clock = HFINT128M                    | ..   | ..   | ..   | mA    |
| I <sub>APPCPU9</sub>  | CPU running CoreMark from RAM                                       | ..   | ..   | ..   | mA    |
| I <sub>APPCPU10</sub> | CPU running CoreMark from RAM, clock = HFXO128M                     | ..   | ..   | ..   | mA    |
| I <sub>APPCPU11</sub> | CPU running CoreMark from RAM, clock = HFXO64M                      | ..   | ..   | ..   | mA    |

#### 4.2.1.3 Network CPU running

**Note:** Compiler: ARM version 6.12 (armclang). Compiler flags: -std=c99 --target=arm-arm-none-eabi -mcpu=cortex-m33+nodsp -mfpv=none -mfloat-abi=soft -fno-rtti -flto -funsigned-char -Omax -ffunction-sections. Linker flags: -Omax. Amount of RAM in Network CPU set to 20 kB in flash cases and 40 kB in RAM cases. Clock and regulator settings only apply to Network CPU. Settings in Application CPU equal those in common conditions table above.

| Symbol               | Description                                      | Min. | Typ. | Max. | Units |
|----------------------|--------------------------------------------------|------|------|------|-------|
| I <sub>NETCPU0</sub> | CPU running CoreMark from flash, regulator = LDO |      | 4.7  |      | mA    |
| I <sub>NETCPU1</sub> | CPU running CoreMark from flash                  |      | 2.4  |      | mA    |
| I <sub>NETCPU2</sub> | CPU running CoreMark from flash, clock = HFXO64M |      | 2.5  |      | mA    |
| I <sub>NETCPU3</sub> | CPU running CoreMark from RAM, regulator = LDO   | ..   | ..   | ..   | mA    |
| I <sub>NETCPU4</sub> | CPU running CoreMark from RAM                    | ..   | ..   | ..   | mA    |
| I <sub>NETCPU5</sub> | CPU running CoreMark from RAM, clock = HFXO64M   | ..   | ..   | ..   | mA    |

#### 4.2.1.4 COMP active

| Symbol                 | Description                   | Min. | Typ. | Max. | Units |
|------------------------|-------------------------------|------|------|------|-------|
| I <sub>COMP,LP</sub>   | COMP enabled, low-power mode  | ..   | ..   | ..   | uA    |
| I <sub>COMP,NORM</sub> | COMP enabled, normal mode     | ..   | ..   | ..   | uA    |
| I <sub>COMP,HS</sub>   | COMP enabled, high-speed mode | ..   | ..   | ..   | uA    |

#### 4.2.1.5 LPCOMP active

| Symbol                 | Description    | Min. | Typ. | Max. | Units |
|------------------------|----------------|------|------|------|-------|
| I <sub>LPCOMP,EN</sub> | LPCOMP enabled | ..   | ..   | ..   | uA    |

#### 4.2.1.6 NFCT active

| Symbol                 | Description                                                                       | Min. | Typ. | Max. | Units |
|------------------------|-----------------------------------------------------------------------------------|------|------|------|-------|
| I <sub>SENSE</sub>     | System ON, current in SENSE STATE (this current does not apply when in NFC field) | ..   | ..   | ..   | uA    |
| I <sub>ACTIVATED</sub> | System ON, current in ACTIVATED STATE, clock = HFXO64M                            | ..   | ..   | ..   | uA    |

#### 4.2.1.7 RADIO transmitting/receiving

**Note:** Amount of RAM in Network CPU set to 64 kB. Clock and regulator settings only apply to Network CPU. Settings in Application CPU equal those in common conditions table above.

| Symbol                 | Description                                                                                                               | Min. | Typ. | Max. | Units |
|------------------------|---------------------------------------------------------------------------------------------------------------------------|------|------|------|-------|
| I <sub>RADIO_TX0</sub> | Radio transmitting @ +3 dBm output power, 1 Mbps<br>Bluetooth low energy (BLE) mode, clock = HFXO64M                      |      | 5.3  |      | mA    |
| I <sub>RADIO_TX1</sub> | Radio transmitting @ 0 dBm output power, 1 Mbps<br>Bluetooth low energy (BLE) mode, clock = HFXO64M                       |      | 4.2  |      | mA    |
| I <sub>RADIO_TX2</sub> | Radio transmitting @ -40 dBm output power, 1 Mbps<br>Bluetooth low energy (BLE) mode, clock = HFXO64M                     | ..   | ..   | ..   | mA    |
| I <sub>RADIO_TX3</sub> | Radio transmitting @ 0 dBm output power, 1 Mbps<br>Bluetooth low energy (BLE) mode, clock = HFXO64M;<br>regulator = LDO   |      | 8.8  |      | mA    |
| I <sub>RADIO_TX4</sub> | Radio transmitting @ -40 dBm output power, 1 Mbps<br>Bluetooth low energy (BLE) mode, clock = HFXO64M;<br>regulator = LDO | ..   | ..   | ..   | mA    |
| I <sub>RADIO_TX5</sub> | Radio transmitting @ 0 dBm output power, 2 Mbps<br>Bluetooth low energy (BLE) mode, clock = HFXO64M                       | ..   | ..   | ..   | mA    |



| Symbol                 | Description                                                                                                              | Min. | Typ. | Max. | Units |
|------------------------|--------------------------------------------------------------------------------------------------------------------------|------|------|------|-------|
| I <sub>RADIO_TX6</sub> | Radio transmitting @ 0 dBm output power, 500 kbps<br>Bluetooth low energy (BLE) long-range (LR) mode, clock =<br>HFXO64M | ..   | ..   | ..   | mA    |
| I <sub>RADIO_TX7</sub> | Radio transmitting @ 0 dBm output power, 125 kbps<br>Bluetooth low energy (BLE) long-range (LR) mode, clock =<br>HFXO64M | ..   | ..   | ..   | mA    |
| I <sub>RADIO_TX8</sub> | Radio transmitting @ 0 dBm output power, 250 kbps IEEE<br>802.15.4-2006 mode, clock = HFXO64M                            | ..   | ..   | ..   | mA    |
| I <sub>RADIO_RX0</sub> | Radio receiving @ 1 Mbps Bluetooth low energy (BLE) mode,<br>clock = HFXO64M                                             |      | 3.8  |      | mA    |
| I <sub>RADIO_RX1</sub> | Radio receiving @ 1 Mbps Bluetooth low energy (BLE) mode,<br>clock = HFXO64M; regulator = LDO                            |      | 8.0  |      | mA    |
| I <sub>RADIO_RX2</sub> | Radio receiving @ 2 Mbps Bluetooth low energy (BLE) mode,<br>clock = HFXO64M                                             |      | 4.4  |      | mA    |
| I <sub>RADIO_RX3</sub> | Radio receiving @ 500 kbps Bluetooth low energy (BLE)<br>long-range (LR) mode, clock = HFXO64M                           | ..   | ..   | ..   | mA    |
| I <sub>RADIO_RX4</sub> | Radio receiving @ 125 kbps Bluetooth low energy (BLE)<br>long-range (LR) mode, clock = HFXO64M                           | ..   | ..   | ..   | mA    |
| I <sub>RADIO_RX5</sub> | Radio receiving @ 250 kbps IEEE 802.15.4-2006 mode, clock<br>= HFXO64M                                                   | ..   | ..   | ..   | mA    |

#### 4.2.1.8 RNG active

| Symbol            | Description                    | Min. | Typ. | Max. | Units |
|-------------------|--------------------------------|------|------|------|-------|
| I <sub>RNG0</sub> | RNG running, 64 kB network RAM | ..   | ..   | ..   | uA    |

#### 4.2.1.9 SAADC active

| Symbol                  | Description                                                                                         | Min. | Typ. | Max. | Units |
|-------------------------|-----------------------------------------------------------------------------------------------------|------|------|------|-------|
| I <sub>SAADC_RUN</sub>  | SAADC sampling @ 16 ksps, acquisition time = 20 us, clock =<br>HFXO64M                              | ..   | ..   | ..   | uA    |
| I <sub>SAADC_TASK</sub> | SAADC sampling @ 1 kHz from RTC in task mode, acquisition<br>time = 20 us, clock = HFXO64M and LFXO | ..   | ..   | ..   | uA    |

#### 4.2.1.10 TEMP active

| Symbol             | Description                     | Min. | Typ. | Max. | Units |
|--------------------|---------------------------------|------|------|------|-------|
| I <sub>TEMP0</sub> | TEMP started, 64 kB network RAM | ..   | ..   | ..   | uA    |

#### 4.2.1.11 TIMER running

| Symbol              | Description                                         | Min. | Typ. | Max. | Units |
|---------------------|-----------------------------------------------------|------|------|------|-------|
| I <sub>TIMER0</sub> | One TIMER running @ 16 MHz                          |      | 450  |      | uA    |
| I <sub>TIMER1</sub> | One TIMER running @ 16 MHz, clock = HFXO64M         |      | 625  |      | uA    |
| I <sub>TIMER2</sub> | One TIMER running @ 1 MHz                           | ..   | ..   | ..   | uA    |
| I <sub>TIMER3</sub> | One TIMER running @ 1 MHz, clock = HFXO64M          | ..   | ..   | ..   | uA    |
| I <sub>TIMER4</sub> | One network TIMER running @ 16 MHz                  | ..   | ..   | ..   | uA    |
| I <sub>TIMER5</sub> | One network TIMER running @ 16 MHz, clock = HFXO64M | ..   | ..   | ..   | uA    |
| I <sub>TIMER6</sub> | One network TIMER running @ 1 MHz                   | ..   | ..   | ..   | uA    |
| I <sub>TIMER7</sub> | One network TIMER running @ 1 MHz, clock = HFXO64M  | ..   | ..   | ..   | uA    |

#### 4.2.1.12 WDT active

| Symbol               | Description                                | Min. | Typ. | Max. | Units |
|----------------------|--------------------------------------------|------|------|------|-------|
| I <sub>WDT,APP</sub> | Application MCU WDT started                | ..   | ..   | ..   | uA    |
| I <sub>WDT,NET</sub> | Network MCU WDT started, 64 kB network RAM | ..   | ..   | ..   | uA    |

#### 4.2.1.13 Compounded

**Note:** The amount of RAM in the application CPU is set to 20 kB. The amount of RAM in the network CPU is set to 64 kB. The clock and regulator settings are common to both the application CPU and the network CPU in all cases except when it's only the network CPU, in which case they only apply to the network CPU.

| Symbol          | Description                                                                                                                                                                             | Min. | Typ. | Max. | Units |
|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|-------|
| I <sub>S0</sub> | Application CPU running CoreMark from flash, radio transmitting @ 0 dBm output power, 1 Mbps Bluetooth low energy (BLE) mode; clock = HFXO64M                                           | ..   | ..   | ..   | mA    |
| I <sub>S1</sub> | Application CPU running CoreMark from flash, radio receiving @ 1 Mbps Bluetooth low energy (BLE) mode; clock = HFXO64M                                                                  | ..   | ..   | ..   | mA    |
| I <sub>S2</sub> | Application CPU running CoreMark from flash, radio transmitting @ 0 dBm output power, 1 Mbps Bluetooth low energy (BLE) mode; clock = HFXO64M, regulator = LDO                          | ..   | ..   | ..   | mA    |
| I <sub>S3</sub> | Application CPU running CoreMark from flash, radio receiving @ 1 Mbps Bluetooth low energy (BLE) mode; clock = HFXO64M, regulator = LDO                                                 | ..   | ..   | ..   | mA    |
| I <sub>S4</sub> | Application CPU running CoreMark from flash, radio transmitting @ 0 dBm output power, 1 Mbps Bluetooth low energy (BLE) mode; clock = HFXO64M, 5 V supply on VDDH, VREGH output = 3.3 V | ..   | ..   | ..   | mA    |
| I <sub>S5</sub> | Application CPU running CoreMark from flash, radio receiving @ 1 Mbps Bluetooth low energy (BLE) mode; clock = HFXO64M, 5 V supply on VDDH, VREGH output = 3.3 V                        | ..   | ..   | ..   | mA    |
| I <sub>S6</sub> | Network CPU running CoreMark from flash, radio transmitting @ 0 dBm output power, 1 Mbps Bluetooth low energy (BLE) mode, clock = HFXO64M                                               | ..   | ..   | ..   | mA    |
| I <sub>S7</sub> | Network CPU running CoreMark from flash, radio receiving @ 1 Mbps Bluetooth low energy (BLE) mode, clock = HFXO64M                                                                      | ..   | ..   | ..   | mA    |
| I <sub>S8</sub> | Application + Network CPU running CoreMark from flash, radio transmitting @ 0 dBm output power, 1 Mbps Bluetooth low energy (BLE) mode; clock = HFXO64M                                 | ..   | ..   | ..   | mA    |
| I <sub>S9</sub> | Application + Network CPU running CoreMark from flash, radio receiving @ 1 Mbps Bluetooth low energy (BLE) mode; clock = HFXO64M                                                        | ..   | ..   | ..   | mA    |

#### 4.2.1.14 USB active

| Symbol                 | Description                                                                                                                        | Min. | Typ. | Max. | Units   |
|------------------------|------------------------------------------------------------------------------------------------------------------------------------|------|------|------|---------|
| $I_{USB,ACTIVE,VBUS}$  | Current from VBUS supply, USB active                                                                                               | ..   | ..   | ..   | mA      |
| $I_{USB,SUSPEND,VBUS}$ | Current from VBUS supply, USB suspended, CPU sleeping                                                                              | ..   | ..   | ..   | $\mu$ A |
| $I_{USB,ACTIVE,VDD}$   | Current from VDD supply (normal voltage mode), all RAM retained, regulator=LDO, CPU running, USB active                            | ..   | ..   | ..   | mA      |
| $I_{USB,SUSPEND,VDD}$  | Current from VDD supply (normal voltage mode), all RAM retained, regulator=LDO, CPU sleeping, USB suspended                        | ..   | ..   | ..   | $\mu$ A |
| $I_{USB,ACTIVE,VDDH}$  | Current from VDDH supply (high voltage mode), VDD=3 V (VREGH output), all RAM retained, regulator=LDO, CPU running, USB active     | ..   | ..   | ..   | mA      |
| $I_{USB,SUSPEND,VDDH}$ | Current from VDDH supply (high voltage mode), VDD=3 V (VREGH output), all RAM retained, regulator=LDO, CPU sleeping, USB suspended | ..   | ..   | ..   | $\mu$ A |
| $I_{USB,DISABLED,VDD}$ | Current from VDD supply, USB disabled, VBUS supply connected, all RAM retained, regulator=LDO, CPU sleeping                        | ..   | ..   | ..   | $\mu$ A |

### 4.3 Power supply modes and regulators

nRF5340 supports two different power supply voltage ranges, each having a corresponding power supply pin. The PMU automatically activates the correct voltage regulator depending on which power supply pin is used.

The nRF5340 PMU controls three different regulators to support the following power supply modes:

- **Normal voltage mode** on page 32 - Powers the device through the VDD pin
- **High voltage mode** on page 33 - Powers the device through the VDDH pin

The three regulators and how they are connected to the supply pins are shown in the following figure.

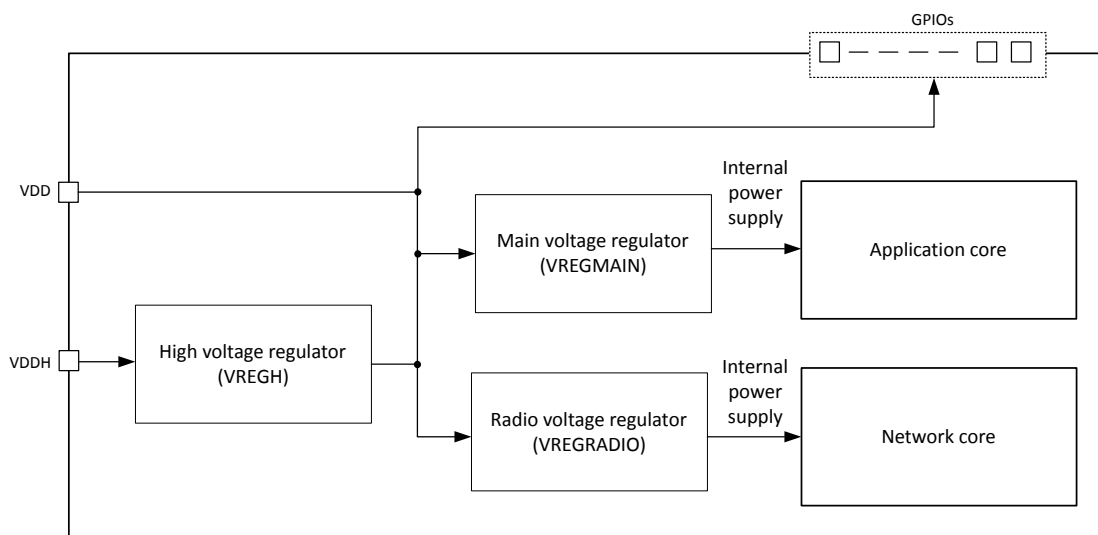


Figure 4: Regulators used in nRF5340

#### 4.3.1 Normal voltage mode

When the device operates in normal voltage mode, only the main voltage regulator (VREGMAIN) and the radio voltage regulator (VREGRADIO) are used.

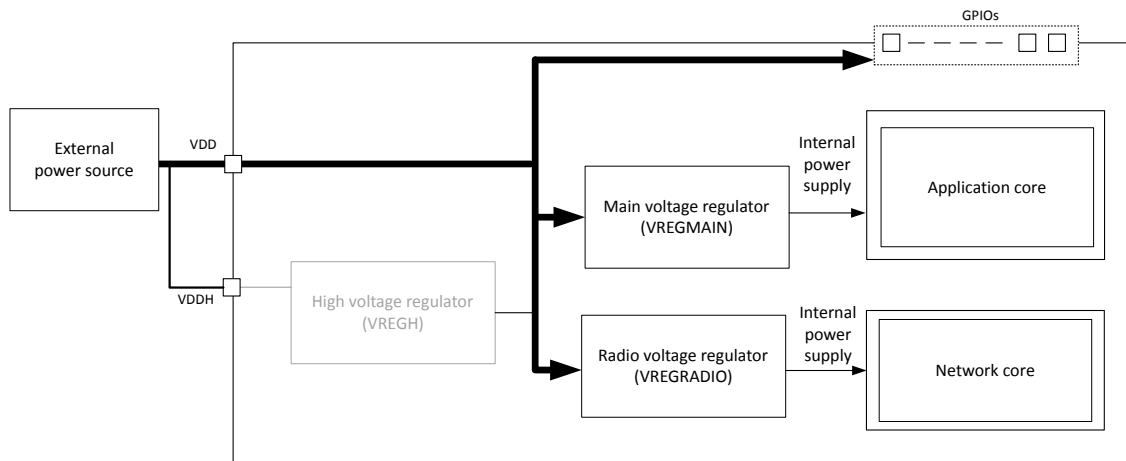


Figure 5: Regulator usage in Normal voltage mode

The external power supply is connected to the VDD pin. The VDDH pin is connected to VDD, but the VREGH regulator is deactivated.

In normal voltage mode, each regulator can operate in LDO or DC/DC mode. See [Normal voltage mode - detailed setup](#) on page 41 for details about configuration of the regulators in this mode.

### 4.3.2 High voltage mode

When the device operates in high voltage mode, the high voltage regulator (VREGH), the main voltage regulator (VREGMAIN) and the radio voltage regulator (VREGRADIO) are used.

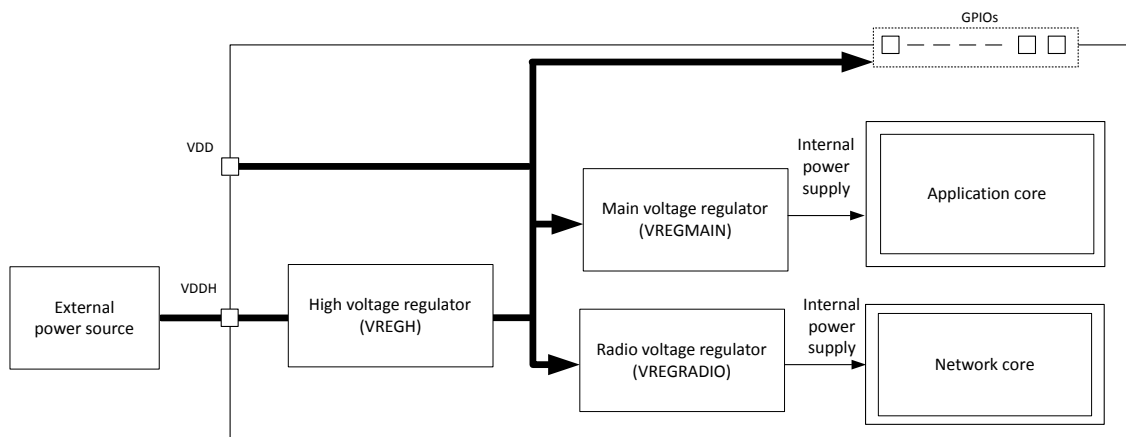


Figure 6: Regulator usage in High voltage mode

The external power supply is connected to the VDDH pin. The VREGMAIN and VREGRADIO regulators are used to power the internal circuitry from the VDD pin. The VDD pin is supplied by the VREGH regulator.

In high voltage mode, each of the three regulators can operate in LDO or DC/DC mode. See [High voltage mode - detailed setup](#) on page 42 for details about configuring the regulators in this mode.

### 4.3.3 Power supply supervisor

Several voltage monitoring devices, enabled through the power management unit (PMU), are used to monitor the connected power supply.

The following figure illustrates the main components for power supply supervision.

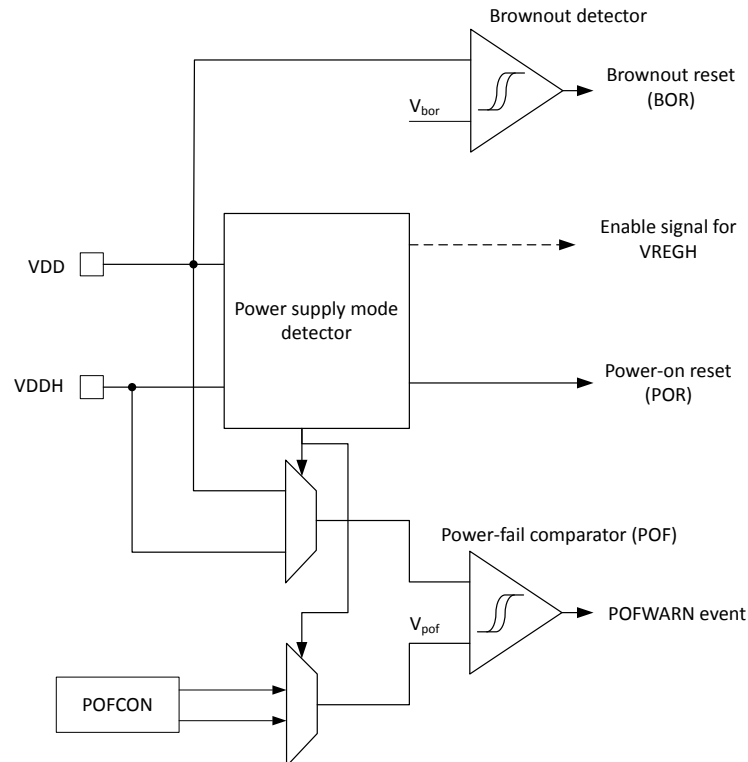


Figure 7: Power supply supervision in nRF5340

The power supply mode detector determines which supply pin is used when the device is powered up. It selects the power supply mode accordingly, and generates a power-on reset (POR) which initializes the device. For an overview of the different supply modes, see [Power supply modes and regulators](#) on page 32.

The brownout detector monitors the VDD supply (input of the VREGMAIN regulator) to ensure safe operation, and generates a brownout reset (BOR) if the voltage is too low, holding the device in reset when the voltage is too low for safe operation. The brownout reset voltage is defined in parameters  $V_{BOR,OFF}$  and  $V_{BOR,ON}$ .

The optional power-fail comparator (POF) can be used to signal the application when the supply voltage drops below a configured threshold. For details on the POF, see [Power-fail comparator](#) on page 34.

#### 4.3.3.1 Power-fail comparator

The power-fail comparator (POF) can provide the CPU with an early warning of an impending power supply failure.

The POF can be used to signal the application when the supply voltage drops below a configured threshold. The POF will not reset the system, but instead give the CPU time to prepare for an orderly power-down. The following figure shows the main elements of the POF.

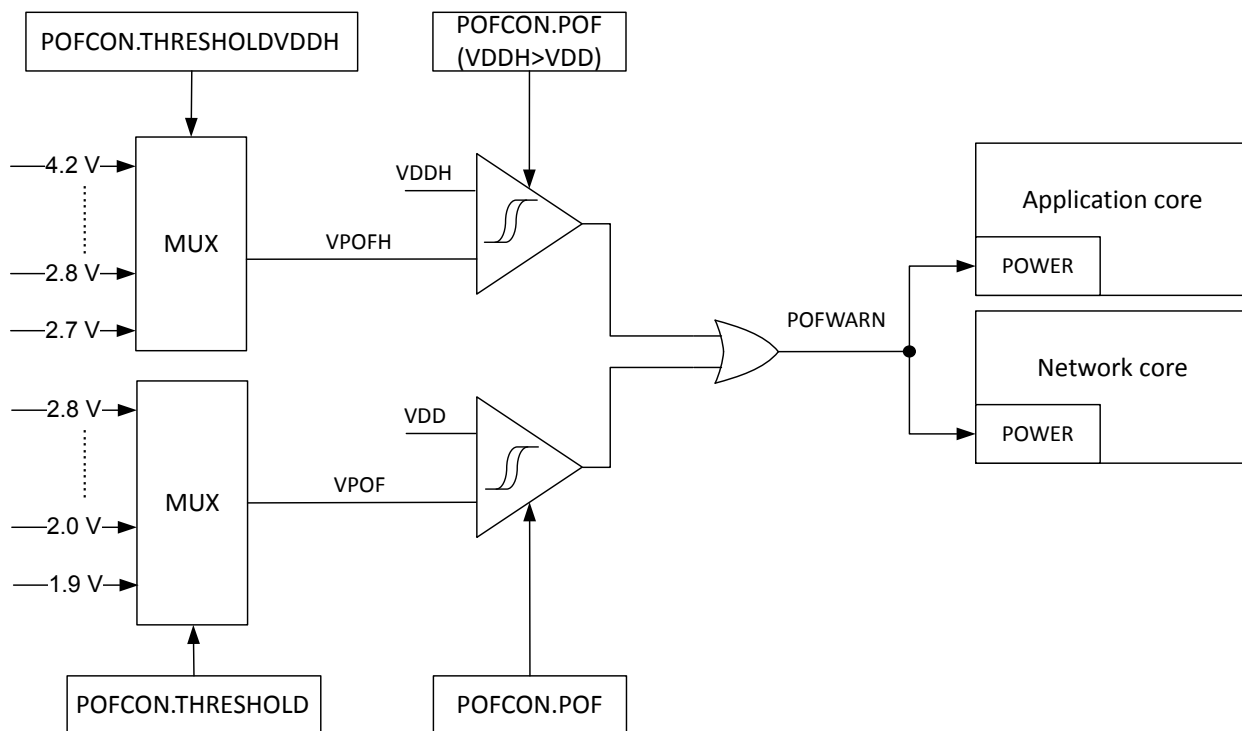


Figure 8: Power-fail comparator

Using the POF is optional, and must be enabled and configured through the register [POFCON \( Retained \)](#) on page 45.

Depending on the supply mode (see [Power supply modes and regulators](#) on page 32), the thresholds  $V_{POF}$  and  $V_{POFH}$  must be configured to a suitable level through the [POFCON](#) register. When the supply voltage falls below the defined threshold, the POF will generate the event [POFWARN](#) that is sent to the [POWER](#) module within both the application and network cores. Software running on the two cores can use this signal to prepare for a power failure. This event is also generated when the supply voltage is already below the threshold at the time the power-fail comparator is enabled, or if the threshold is reconfigured to a level above the supply voltage.

If the POF is enabled and the supply voltage is below the threshold, the POF will prevent the [NVMC](#) from performing write operations to the NVM.

To save power, the POF is not active in System OFF.

The POF features a hysteresis of  $V_{POFHYST}$ , as illustrated in the following figure.

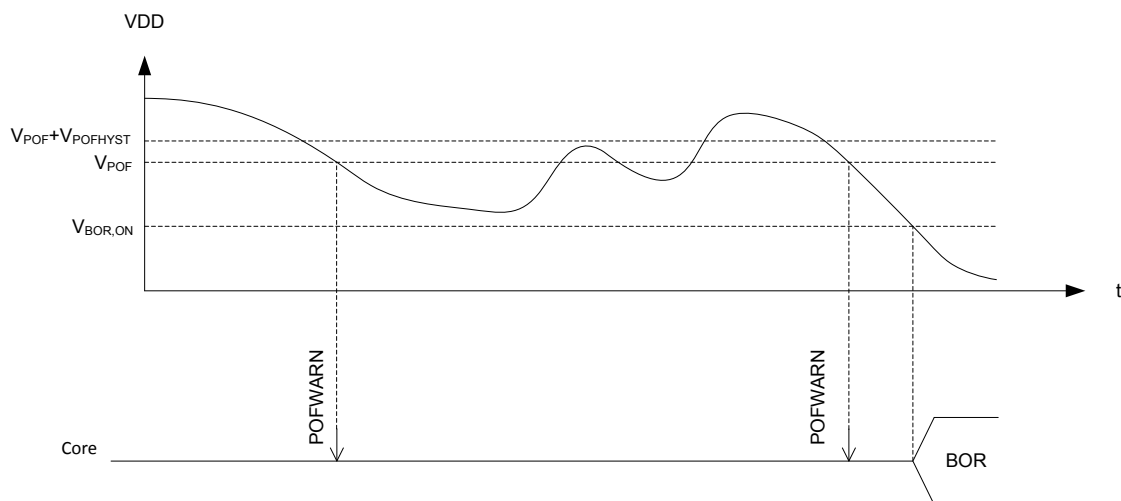


Figure 9: POF hysteresis and POFWARN event (BOR = brownout reset)

The POF hysteresis voltage is defined with the  $V_{POFHYST}$  parameter in [Electrical specification](#) on page 46.

## 4.4 POWER — Power control

The POWER peripheral provides an interface for the power and clock subsystem for task, event, and interrupt related settings.

Each core has its own POWER peripheral that is responsible for requesting resources from the power and clock subsystem. The power and clock subsystem ensure that the power mode with the proper latency settings is selected when requested by an instance of the POWER peripheral. This means that the Constant latency mode is prioritized over Low-power mode. For an overview of power modes, see [Power submodes](#) on page 23.

The **POFWARN** event is a system level event that enables each core to react quickly if there is a power failure. The power-fail comparator must be configured and enabled in order to receive the event, see [Power-fail comparator](#) on page 34 for more information.

**Note:** Registers [INTEN](#) on page 40, [INTENSET](#) on page 40, and [INTENCLR](#) on page 40 are the same (at the same address) as corresponding registers in [CLOCK peripheral](#).

**Note:** Power control of the RAM blocks is controlled by the Volatile memory controller (VMC), see [VMC — Volatile memory controller](#) on page 719.

### 4.4.1 Registers

| Base address | Domain      | Peripheral | Instance   | Secure mapping | DMA security | Description   | Configuration |
|--------------|-------------|------------|------------|----------------|--------------|---------------|---------------|
| 0x50005000   | APPLICATION | POWER      | POWER : S  | US             | NA           | Power control |               |
| 0x40005000   |             |            | POWER : NS |                |              |               |               |
| 0x41005000   | NETWORK     | POWER      | POWER      | NS             | NA           | Power control |               |

Table 6: Instances



| Register           | Offset | Security | Description                                                |
|--------------------|--------|----------|------------------------------------------------------------|
| TASKS_CONSTLAT     | 0x78   |          | Enable constant latency mode                               |
| TASKS_LOWPWR       | 0x7C   |          | Enable low power mode (variable latency)                   |
| SUBSCRIBE_CONSTLAT | 0xF8   |          | Subscribe configuration for task <a href="#">CONSTLAT</a>  |
| SUBSCRIBE_LOWPWR   | 0xFC   |          | Subscribe configuration for task <a href="#">LOWPWR</a>    |
| EVENTS_POFWARN     | 0x108  |          | Power failure warning                                      |
| EVENTS_SLEEPENTER  | 0x114  |          | CPU entered WFI/WFE sleep                                  |
| EVENTS_SLEEPEXIT   | 0x118  |          | CPU exited WFI/WFE sleep                                   |
| PUBLISH_POFWARN    | 0x188  |          | Publish configuration for event <a href="#">POFWARN</a>    |
| PUBLISH_SLEEPENTER | 0x194  |          | Publish configuration for event <a href="#">SLEEPENTER</a> |
| PUBLISH_SLEEPEXIT  | 0x198  |          | Publish configuration for event <a href="#">SLEEPEXIT</a>  |
| INTEN              | 0x300  |          | Enable or disable interrupt                                |
| INTENSET           | 0x304  |          | Enable interrupt                                           |
| INTENCLR           | 0x308  |          | Disable interrupt                                          |
| GPREGRET[n]        | 0x51C  |          | General purpose retention register <span>Retained</span>   |

Table 7: Register overview

#### 4.4.1.1 TASKS\_CONSTLAT

Address offset: 0x78

Enable constant latency mode

|                  |            |                |          |   |       |              |             |                              |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------------|----------|---|-------|--------------|-------------|------------------------------|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                |          |   |       |              |             |                              |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |                |          |   |       |              |             |                              |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |
| Reset 0x00000000 |            |                |          |   |       |              |             |                              |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |                | Value ID |   | Value |              | Description |                              |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_CONSTLAT |          |   |       |              |             | Enable constant latency mode |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Trigger        |          | 1 |       | Trigger task |             |                              |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

#### 4.4.1.2 TASKS\_LOWPWR

Address offset: 0x7C

Enable low power mode (variable latency)

|                  |            |              |          |   |       |                                          |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------------|----------|---|-------|------------------------------------------|-------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |              |          |   |       |                                          |             |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |              |          |   |       |                                          |             |  |  | A  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |              |          |   |       |                                          |             |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |              | Value ID |   | Value |                                          | Description |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_LOWPWR |          |   |       | Enable low power mode (variable latency) |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Trigger      |          | 1 |       | Trigger task                             |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

#### 4.4.1.3 SUBSCRIBE\_CONSTLAT

Address offset: 0xF8

Subscribe configuration for task [CONSTLAT](#)

|                  |            |          |          |    |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |   |   |   |   |   |
|------------------|------------|----------|----------|----|-----------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|--|---|---|---|---|---|---|
| Bit number       |            |          | 31       | 30 | 29                                                  | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |  |   |   |   |   |   |   |
| ID               |            |          | B        |    |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   |   |   |   |   |  |  |  | A | A | A | A | A | A |
| Reset 0x00000000 |            |          | 0        | 0  | 0                                                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |   |   |   |   |   |   |
| ID               | Acce Field | Value ID | Value    |    | Description                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] |    | Channel that task <b>CONSTLAT</b> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |   |   |   |   |   |
| B                | RW EN      |          |          |    |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |   |   |   |   |   |
|                  |            | Disabled | 0        |    | Disable subscription                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |   |   |   |   |   |
|                  |            | Enabled  | 1        |    | Enable subscription                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |   |   |   |   |   |

#### 4.4.1.4 SUBSCRIBE\_LOWPWR

Address offset: 0xFC

Subscribe configuration for task **LOWPWR**

|                  |            |  |          |  |          |  |                                                   |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|--|----------|--|---------------------------------------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          |  |          |  |                                                   |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |
| ID               |            |  |          |  |          |  |                                                   |  |  | B  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  |    |    |    |   |   |   |   |   |   | A | A | A | A | A | A | A |   |
| Reset 0x00000000 |            |  |          |  |          |  |                                                   |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID |  | Value    |  | Description                                       |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          |  | [255..0] |  | Channel that task <b>LOWPWR</b> will subscribe to |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |  |          |  |                                                   |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled |  | 0        |  | Disable subscription                              |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  |  | 1        |  | Enable subscription                               |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 4.4.1.5 EVENTS\_POFWARN

Address offset: 0x108

Power failure warning

|                  |            |                |              |                       |                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|------------------|------------|----------------|--------------|-----------------------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|---|
| Bit number       |            |                |              | 31                    | 30                  | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |   |
| ID               |            |                |              |                       |                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | A |
| Reset 0x00000000 |            |                |              | 0                     | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |   |
| ID               | Acce Field | Value ID       | Value        | Description           |                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
| A                | RW         | EVENTS_POFWARN |              | Power failure warning |                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            |                | NotGenerated | 0                     | Event not generated |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            |                | Generated    | 1                     | Event generated     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |

#### 4.4.1.6 EVENTS\_SLEEPENTER

Address offset: 0x114

CPU entered WFI/WFE sleep

|                  |            |                   |       |    |    |                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|------------------|------------|-------------------|-------|----|----|---------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|---|
| Bit number       |            |                   | 31    | 30 | 29 | 28                        | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |   |
| ID               |            |                   |       |    |    |                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | A |
| Reset 0x00000000 |            |                   | 0     | 0  | 0  | 0                         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |   |
| ID               | Acce Field | Value ID          | Value |    |    | Description               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
| A                | RW         | EVENTS_SLEEPENTER |       |    |    | CPU entered WFI/WFE sleep |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | NotGenerated      | 0     |    |    | Event not generated       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | Generated         | 1     |    |    | Event generated           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |

#### 4.4.1.7 EVENTS\_SLEEPEXIT

Address offset: 0x118

## CPU exited WFI/WFE sleep

| Bit number       |            |                  | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|------------------|---------------------------------------------------------------------------------------|--------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |            |                  | A                                                                                     |                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |                  | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID         | Value                                                                                 | Description              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | EVENTS_SLEEPEXIT |                                                                                       | CPU exited WFI/WFE sleep |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | NotGenerated     | 0                                                                                     | Event not generated      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Generated        | 1                                                                                     | Event generated          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

## 4.4.1.8 PUBLISH\_POFWARN

Address offset: 0x188

Publish configuration for event [POFWARN](#)

|                  |            |  |          |                                                                                       |  |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|--|----------|---------------------------------------------------------------------------------------|--|----------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |  |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |  |          | B                                                                                     |  |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |  |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |  |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field |  | Value ID | Value                                                                                 |  | Description                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |  |          | [255..0]                                                                              |  | Channel that event <b>POFWARN</b> will publish to. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |  |          |                                                                                       |  |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            |  | Disabled | 0                                                                                     |  | Disable publishing                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            |  | Enabled  | 1                                                                                     |  | Enable publishing                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

## 4.4.1.9 PUBLISH\_SLEEPENTER

Address offset: 0x194

Publish configuration for event [SLEEPENTER](#)

|                  |            |          |                                                                                       |                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|-------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          | B A A A A A A A                                                                       |                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                              | Channel that event <b>SLEEPENTER</b> will publish to. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW EN      |          |                                                                                       |                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Disable publishing                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Enable publishing                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

## 4.4.1.10 PUBLISH\_SLEEPEXIT

Address offset: 0x198

Publish configuration for event [SLEEPEXIT](#)

|                  |            |          |                                                                                       |                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          | B A A A A A A A                                                                       |                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                              | Channel that event <span>SLEEPEXIT</span> will publish to. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW EN      |          |                                                                                       |                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Disable publishing                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Enable publishing                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |



| Bit number       |               |          | 31    | 30 | 29                                                                  | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
|------------------|---------------|----------|-------|----|---------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| ID               |               |          |       |    |                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | C | B | A |   |   |
| Reset 0x00000000 |               |          | 0     | 0  | 0                                                                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field    | Value ID | Value |    | Description                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW SLEEPENTER | Disabled | 0     |    | Read: Disabled                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |               | Enabled  | 1     |    | Read: Enabled                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |               | Clear    | 1     |    | Write '1' to disable interrupt for event <a href="#">SLEEPENTER</a> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |               | Disabled | 0     |    | Disable                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |               | Enabled  | 1     |    | Read: Disabled                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| C                | RW SLEEPEXIT  | Disabled | 0     |    | Read: Disabled                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |               | Enabled  | 1     |    | Read: Enabled                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |               | Clear    | 1     |    | Write '1' to disable interrupt for event <a href="#">SLEEPEXIT</a>  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |               | Disabled | 0     |    | Disable                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |               | Enabled  | 1     |    | Read: Disabled                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

#### 4.4.1.14 GPREGRET[n] (n=0..1) ( Retained )

Address offset: 0x51C + (n × 0x4)

This register is a retained register

General purpose retention register

|                  |      |          |       |    |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |                                      |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|----------|-------|----|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--------------------------------------|------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |          |       | 31 | 30    | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |                                      |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |          |       |    |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A | A | A | A | A | A | A | A |  |  |                                      |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |          |       | 0  | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |                                      |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field    | Value | ID | Value |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |                                      | Description                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW   | GPREGRET |       |    |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |                                      | General purpose retention register |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |          |       |    |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  | This register is a retained register |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

## 4.5 REGULATORS - Regulator control

All system components are powered from the on-chip voltage regulators. These regulators are responsible for converting the voltage supplied on the VDD or VDDH pins to adequate voltages to be used internally.

The available regulators can be configured in multiple ways to accommodate different input voltage ranges. Some modes support sourcing power to external circuitry. The voltage modes that are supported by nRF5340 are listed in the following table.

| Voltage mode        | Input voltage range | Output voltage range |
|---------------------|---------------------|----------------------|
| Normal voltage mode | 1.7 V - 3.6 V       | -                    |
| High voltage mode   | 2.5 V - 5.5 V       | 1.8 V - 3.3 V        |

Table 8: Supported voltage modes

For an overview on the available regulators, see [Power supply modes and regulators](#) on page 32.

### 4.5.1 Normal voltage mode - detailed setup

Normal voltage mode uses the main regulator (VREGMAIN) and the radio regulator (VREGRADIO).

The VREGMAIN and VREGRADIO regulators operate in LDO mode by default. DC/DC mode can be enabled independently for each regulator using [VREGMAIN.DCDCEN \( Retained \)](#) on page 45 and [VREGRADIO.DCDCEN \( Retained \)](#) on page 46 respectively.

When configured as shown in the following figure, the nRF5340 enters normal voltage mode. Here both regulators are in DC/DC mode. An external LC filter is required for each regulator in DC/DC mode. If a regulator is only to be used in LDO mode, the inductor for this regulator is not needed. In this mode, the VDDH pin must be connected to VDD, even if the high voltage regulator (VREGH) is not in use.

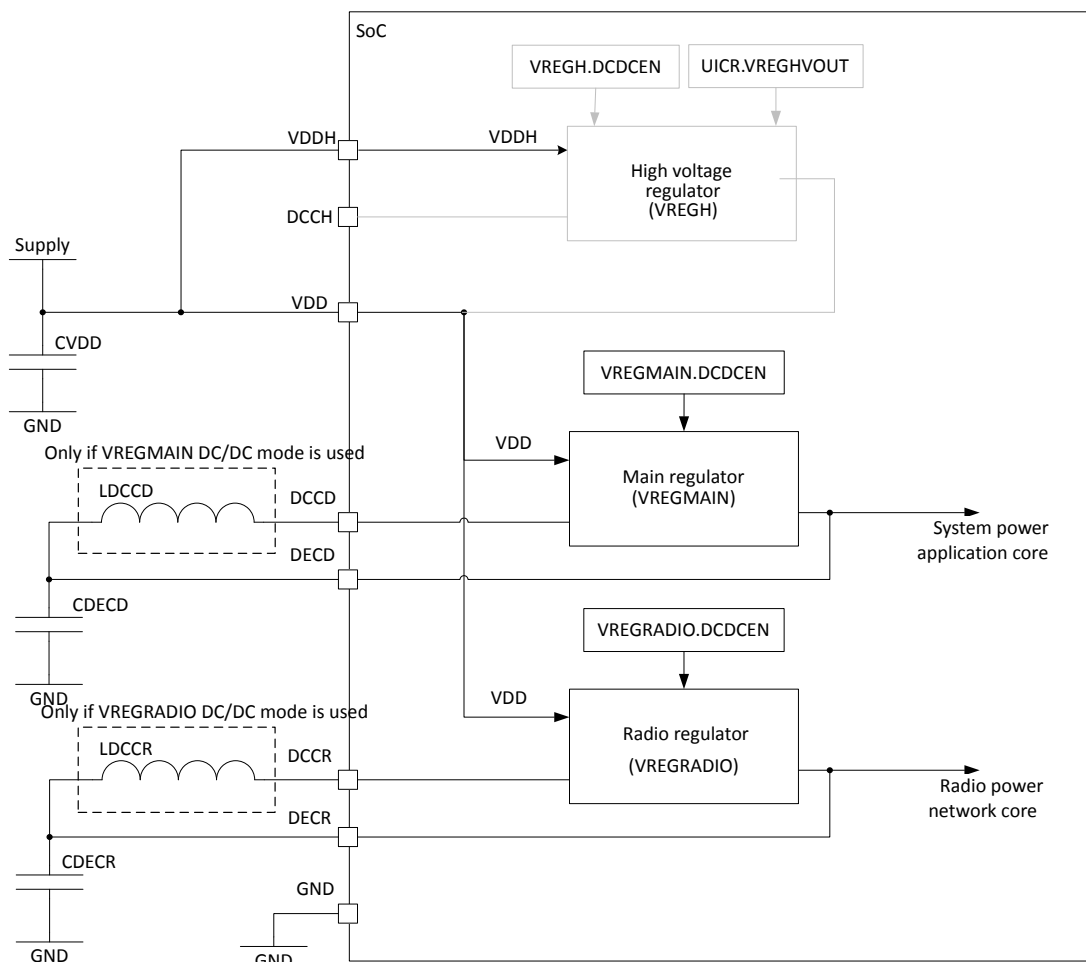


Figure 10: Normal voltage mode

The advantage of using a regulator in DC/DC mode is that the overall power consumption is reduced. This is because the regulator in DC/DC mode has a higher efficiency than in LDO mode. Regulator efficiency in DC/DC mode varies depending on the supply voltage and the current drawn from the regulators.

### 4.5.2 High voltage mode - detailed setup

High voltage mode uses the main regulator (VREGMAIN), the high voltage regulator (VREGH), and the radio regulator (VREGRADIO).

All regulators operate in LDO mode by default. DC/DC mode can be enabled independently for each regulator using [VREGMAIN.DCDCEN \(Retained\)](#) on page 45, [VREGH.DCDCEN \(Retained\)](#) on page 46, and [VREGRADIO.DCDCEN \(Retained\)](#) on page 46.

When configured as shown in the following figure, the nRF5340 enters high voltage mode. Here all three regulators are in DC/DC mode. An external LC filter is required for each of the regulators in DC/DC mode. If a regulator is only to be used in LDO mode, the inductor for this regulator is not needed.

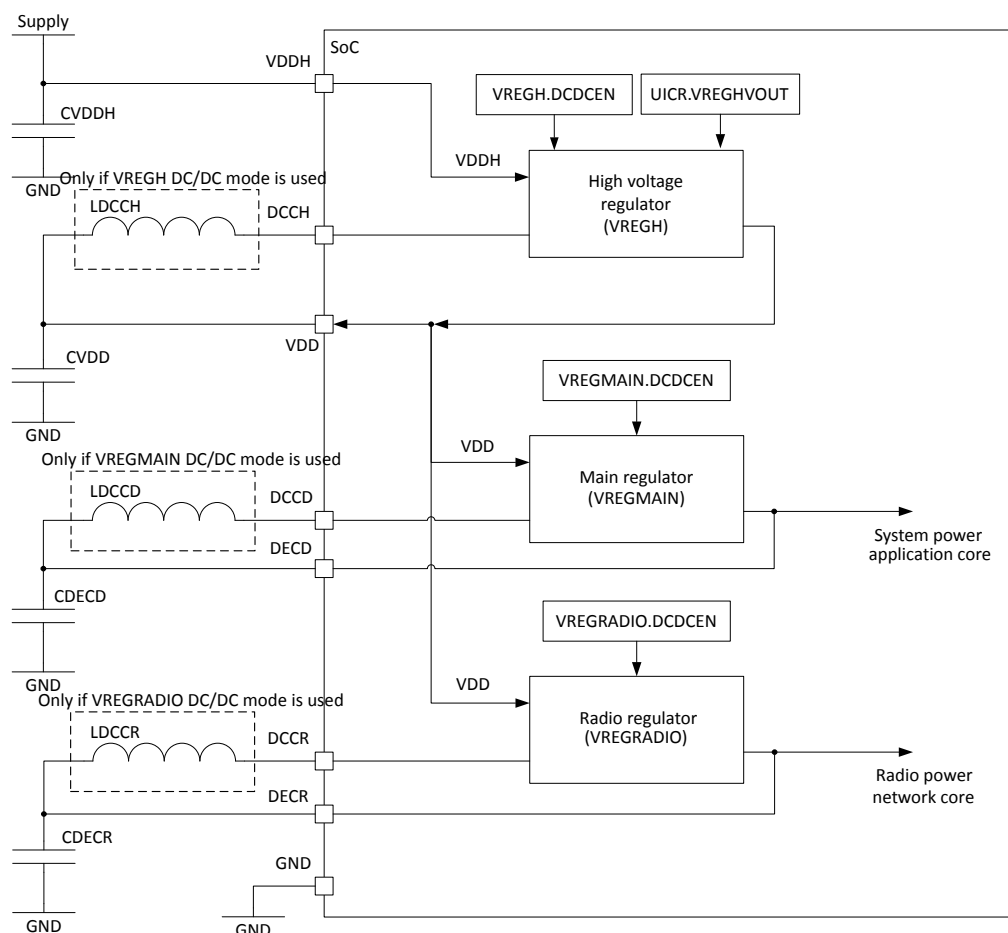


Figure 11: High voltage mode

The advantage of using a regulator in DC/DC mode is that the overall power consumption is reduced. This is because the regulator in DC/DC mode has higher efficiency than when in LDO mode. Regulator efficiency in DC/DC mode varies depending on the supply voltage and the current drawn from the regulators.

#### 4.5.2.1 External circuitry supply

In high voltage mode, the output from VREGH can be used to supply external circuitry from the VDD pin.

As illustrated in [High voltage mode - detailed setup](#) on page 42, external circuitry can be powered from the VDD pin once it is enabled in the register [EXTSUPPLY](#) on page 116.

The VDD output voltage is programmed in the register [VREGHVOUT](#) on page 116.

The supported output voltage range depends on the supply voltage provided to the VDDH pin. The difference between voltage supplied on the VDDH pin and the voltage output on the VDD pin is defined by the  $V_{\text{REGH,DROP}}$  parameter in [Regulator specifications, VREGH stage](#) on page 48.

Supplying power to external circuitry is allowed in both System OFF and System ON mode.

**Note:** The maximum allowed current drawn by external circuitry is dependent on the total internal current draw. The maximum current that can be drawn externally from REGH is defined in [Regulator specifications, VREGH stage](#) on page 48).

### 4.5.3 GPIO levels

The GPIO high reference voltage depends on the regulator voltage mode.

In normal voltage mode, the GPIO high level equals the voltage supplied to the VDD pin. In high voltage mode, it equals the level specified in the **VREGHVOUT** register.

### 4.5.4 Registers

| Base address | Domain      | Peripheral | Instance     | Secure mapping | DMA security | Description             | Configuration |
|--------------|-------------|------------|--------------|----------------|--------------|-------------------------|---------------|
| 0x50004000   | APPLICATION | REGULATORS | REGULATORS : | US             | NA           | Regulator configuration |               |
| 0x40004000   |             |            | S            |                |              |                         |               |
|              |             |            | REGULATORS : |                |              |                         |               |
|              |             |            | NS           |                |              |                         |               |

Table 9: Instances

| Register         | Offset | Security | Description                         |          |
|------------------|--------|----------|-------------------------------------|----------|
| MAINREGSTATUS    | 0x428  |          | Main supply status                  | Retained |
| SYSTEMOFF        | 0x500  |          | System OFF register                 |          |
| POFCON           | 0x510  |          | Power-fail comparator configuration | Retained |
| VREGMAIN.DCDCEN  | 0x704  |          | DC/DC enable register for VREGMAIN  | Retained |
| VREGRADIO.DCDCEN | 0x904  |          | DC/DC enable register for VREGRADIO | Retained |
| VREGH.DCDCEN     | 0x800  |          | DC/DC enable register for VREGH     | Retained |

Table 10: Register overview

#### 4.5.4.1 MAINREGSTATUS ( Retained )

Address offset: 0x428

This register is a retained register

Main supply status

|                  |            |       |          |    |       |    |                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-------|----------|----|-------|----|--------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |       |          |    | 31    | 30 | 29                                                     | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |       |          |    | A     |    |                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |       |          |    | 0     | 0  | 0                                                      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |       | Value    | ID | Value |    | Description                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | R          | VREGH |          |    |       |    | VREGH status                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |       | Inactive | 0  |       |    | Normal voltage mode. Voltage supplied on VDD and VDDH. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |       | Active   | 1  |       |    | High voltage mode. Voltage supplied on VDDH.           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

#### 4.5.4.2 SYSTEMOFF

Address offset: 0x500

System OFF register

|                  |            |           |          |       |                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-----------|----------|-------|------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |           |          |       | 31                     | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |           |          |       | A                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |           |          |       | 0                      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |           | Value ID | Value | Description            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | SYSTEMOFF |          |       | Enable System OFF mode |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |           | Enter    | 1     | Enable System OFF mode |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |



#### 4.5.4.3 POFCON ( Retained )

Address offset: 0x510

This register is a retained register

## Power-fail comparator configuration

|                  |      |               |          |                                                                                       |       |                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|---------------|----------|---------------------------------------------------------------------------------------|-------|--------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |               |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |               |          | D D D D B B B B A                                                                     |       |                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |               |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |       |                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field         | Value    | ID                                                                                    | Value | Description                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW   | POF           |          |                                                                                       |       | Enable or disable power-fail comparator                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Disabled | 0                                                                                     |       | Disable                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Enabled  | 1                                                                                     |       | Enable                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW   | THRESHOLD     |          |                                                                                       |       | Power-fail comparator threshold setting                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | V19      | 6                                                                                     |       | Set threshold to 1.9 V                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | V20      | 7                                                                                     |       | Set threshold to 2.0 V                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | V21      | 8                                                                                     |       | Set threshold to 2.1 V                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | V22      | 9                                                                                     |       | Set threshold to 2.2 V                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | V23      | 10                                                                                    |       | Set threshold to 2.3 V                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | V24      | 11                                                                                    |       | Set threshold to 2.4 V                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | V25      | 12                                                                                    |       | Set threshold to 2.5 V                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | V26      | 13                                                                                    |       | Set threshold to 2.6 V                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | V27      | 14                                                                                    |       | Set threshold to 2.7 V                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | V28      | 15                                                                                    |       | Set threshold to 2.8 V                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| D                | RW   | THRESHOLDVDDH |          |                                                                                       |       | Power-fail comparator threshold setting for voltage supply on VDDH |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | V27      | 0                                                                                     |       | Set threshold to 2.7 V                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | V28      | 1                                                                                     |       | Set threshold to 2.8 V                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | V29      | 2                                                                                     |       | Set threshold to 2.9 V                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | V30      | 3                                                                                     |       | Set threshold to 3.0 V                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | V31      | 4                                                                                     |       | Set threshold to 3.1 V                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | V32      | 5                                                                                     |       | Set threshold to 3.2 V                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | V33      | 6                                                                                     |       | Set threshold to 3.3 V                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | V34      | 7                                                                                     |       | Set threshold to 3.4 V                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | V35      | 8                                                                                     |       | Set threshold to 3.5 V                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | V36      | 9                                                                                     |       | Set threshold to 3.6 V                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | V37      | 10                                                                                    |       | Set threshold to 3.7 V                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | V38      | 11                                                                                    |       | Set threshold to 3.8 V                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | V39      | 12                                                                                    |       | Set threshold to 3.9 V                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | V40      | 13                                                                                    |       | Set threshold to 4.0 V                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | V41      | 14                                                                                    |       | Set threshold to 4.1 V                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | V42      | 15                                                                                    |       | Set threshold to 4.2 V                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

#### 4.5.4.4 VREGMAIN.DCDCEN ( Retained )

Address offset: 0x704

This register is a retained register

## DC/DC enable register for VREGMAIN

|                  |            |        |  |          |          |  |       |                                   |  |             |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------|--|----------|----------|--|-------|-----------------------------------|--|-------------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |        |  |          |          |  |       |                                   |  | 31          | 30      | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |        |  |          |          |  |       |                                   |  |             |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |   |
| Reset 0x00000000 |            |        |  |          |          |  |       |                                   |  | 0           | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |        |  | Value ID |          |  | Value |                                   |  | Description |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | DCDCEN |  |          |          |  |       | Enable or disable DC/DC converter |  |             |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |        |  |          | Disabled |  |       | 0                                 |  |             | Disable |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |        |  |          | Enabled  |  |       | 1                                 |  |             | Enable  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 4.5.4.5 VREGRADIO.DCDCEN ( Retained )

Address offset: 0x904

This register is a retained register

DC/DC enable register for VREGRADIO

|                  |            |        |          |                                   |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |
|------------------|------------|--------|----------|-----------------------------------|----|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|
| Bit number       |            |        |          | 31                                | 30 | 29          | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |
| ID               |            |        |          |                                   |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |  |
| Reset 0x00000000 |            |        |          | 0                                 | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |
| ID               | Acce Field |        | Value ID | Value                             |    | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |
| A                | RW         | DCDCEN |          | Enable or disable DC/DC converter |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |            |        | Disabled | 0                                 |    | Disable     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |            |        | Enabled  | 1                                 |    | Enable      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |

#### 4.5.4.6 VREGH.DCDCEN ( Retained )

Address offset: 0xB00

This register is a retained register

DC/DC enable register for VREGH

|                  |            |          |  |          |   |  |       |                                   |  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|--|----------|---|--|-------|-----------------------------------|--|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |  |          |   |  |       |                                   |  | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |          |  |          |   |  |       |                                   |  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |
| Reset 0x00000000 |            |          |  |          |   |  |       |                                   |  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |          |  | Value ID |   |  | Value |                                   |  | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | DCDCEN   |  |          |   |  |       | Enable or disable DC/DC converter |  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled |  |          | 0 |  |       | Disable                           |  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  |  |          | 1 |  |       | Enable                            |  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 4.5.5 Electrical specification

#### 4.5.5.1 Regulator startup times

| Symbol                | Description                                                                                                                          | Min. | Typ. | Max. | Units |
|-----------------------|--------------------------------------------------------------------------------------------------------------------------------------|------|------|------|-------|
| t <sub>POR</sub>      | Time in power-on reset after VDD reaches 1.7 V for all supply voltages and temperatures. Dependent on supply rise time. <sup>1</sup> | ..   | ..   | ..   |       |
| t <sub>POR,10us</sub> | VDD rise time 10 μs                                                                                                                  | ..   | ..   | ..   | ms    |
| t <sub>POR,10ms</sub> | VDD rise time 10 ms                                                                                                                  | ..   | ..   | ..   | ms    |
| t <sub>POR,60ms</sub> | VDD rise time 60 ms                                                                                                                  | ..   | ..   | ..   | ms    |

<sup>1</sup> A step increase in supply voltage of 300 mV or more, with rise time of 300 ms or less, within the valid supply range, may result in a system reset.

| Symbol                      | Description                                                                                                                                                                                                         | Min. | Typ. | Max. | Units |
|-----------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|-------|
| $t_{RISE,VREGHOUT}$         | VREGH output (VDD) rise time after VDDH reaches minimum VDDH supply voltage                                                                                                                                         | ..   | ..   | ..   |       |
| $t_{RISE,VREGHOUT,10\mu s}$ | VDDH rise time 10 $\mu s$                                                                                                                                                                                           | ..   | ..   | ..   | ms    |
| $t_{RISE,VREGHOUT,10ms}$    | VDDH rise time 10 ms                                                                                                                                                                                                | ..   | ..   | ..   | ms    |
| $t_{RISE,VREGHOUT,50ms}$    | VDDH rise time 50 ms                                                                                                                                                                                                | ..   | ..   | ..   | ms    |
| $t_{PINR}$                  | If a GPIO pin is configured as reset, the maximum time taken to pull up the pin and release reset after power on reset.<br>Dependent on the pin capacitive load (C). <sup>2</sup> : $t=5RC$ , $R=13\text{ k}\Omega$ | ..   | ..   | ..   |       |
| $t_{PINR,500nF}$            | $C = 500\text{ nF}$                                                                                                                                                                                                 | ..   | ..   | ..   | ms    |
| $t_{PINR,10\mu F}$          | $C = 10\text{ }\mu F$                                                                                                                                                                                               | ..   | ..   | ..   | ms    |

#### 4.5.5.2 Application core startup times

| Symbol               | Description                                                                                             | Min. | Typ. | Max. | Units   |
|----------------------|---------------------------------------------------------------------------------------------------------|------|------|------|---------|
| $t_{R2ON}$           | Time from reset to ON (CPU execute)                                                                     | ..   | ..   | ..   |         |
| $t_{R2ON,NOTCONF}$   | If reset pin not configured                                                                             | ..   | ..   | ..   | ms      |
| $t_{R2ON,CONF}$      | If reset pin configured                                                                                 | ..   | ..   | ..   | ms      |
| $t_{OFF2ON,NM}$      | Time from OFF to CPU execute when in normal voltage mode (supply on VDD)                                | ..   | ..   | ..   | $\mu s$ |
| $t_{OFF2ON,LDO,HV}$  | Time from OFF to CPU execute when in high voltage mode (supply on VDDH) and VREGH using LDO regulator   | ..   | ..   | ..   | $\mu s$ |
| $t_{OFF2ON,DCDC,HV}$ | Time from OFF to CPU execute when in high voltage mode (supply on VDDH) and VREGH using DC/DC regulator | ..   | ..   | ..   | $\mu s$ |
| $t_{IDLE2CPU}$       | Time from IDLE to CPU execute                                                                           | ..   | ..   | ..   | $\mu s$ |
| $t_{EVTSET,CL1}$     | Time from HW event to PPI event in constant latency System ON mode                                      | ..   | ..   | ..   | $\mu s$ |
| $t_{EVTSET,CL0}$     | Time from HW event to PPI event in low power System ON mode                                             | ..   | ..   | ..   | $\mu s$ |

#### 4.5.5.3 Network core startup times

| Symbol               | Description                                                                      | Min. | Typ. | Max. | Units   |
|----------------------|----------------------------------------------------------------------------------|------|------|------|---------|
| $t_{NET,EVTSET,CL1}$ | Time from HW event to PPI event in constant latency System ON mode               | ..   | ..   | ..   | $\mu s$ |
| $t_{NET,EVTSET,CL0}$ | Time from HW event to PPI event in low power System ON mode                      | ..   | ..   | ..   | $\mu s$ |
| $t_{NET,IDLE2CPU}$   | Time from IDLE to CPU execute                                                    | ..   | ..   | ..   | $\mu s$ |
| $t_{FO2ON,NET64}$    | Time for network core from OFF to CPU execute after NETWORK.FORCEOFF is released | ..   | ..   | ..   | $\mu s$ |

<sup>2</sup> To decrease maximum time a device could hold in reset, a strong external pullup resistor can be used.

#### 4.5.5.4 Power-fail comparator

| Symbol               | Description                                                                                                                                                                    | Min. | Typ. | Max. | Units |
|----------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|-------|
| V <sub>POF,NV</sub>  | Nominal power level warning thresholds (falling supply voltage) in normal voltage mode (supply on VDD). Levels are configurable between min. and max. in increments of 100 mV. | ..   | ..   | ..   | V     |
| V <sub>POF,HV</sub>  | Nominal power level warning thresholds (falling supply voltage) in high voltage mode (supply on VDDH). Levels are configurable between min. and max. in increments of 100 mV.  | ..   | ..   | ..   | V     |
| V <sub>POF,LV</sub>  | Nominal power level warning thresholds (falling supply voltage) in low voltage mode (supply on VDDL). Levels are configurable between min. and max. in increments of 100 mV.   | ..   | ..   | ..   | V     |
| V <sub>POFTOL</sub>  | Threshold voltage tolerance (applies in both normal voltage mode and high voltage mode)                                                                                        | ..   | ..   | ..   | %     |
| V <sub>POFHYST</sub> | Threshold voltage hysteresis (applies in both normal voltage mode and high voltage mode)                                                                                       | ..   | ..   | ..   | mV    |
| V <sub>BOR,OFF</sub> | Brownout reset voltage range System OFF mode. Brownout only applies to the voltage on VDD.                                                                                     | ..   | ..   | ..   | V     |
| V <sub>BOR,ON</sub>  | Brownout reset voltage range System ON mode. Brownout only applies to the voltage on VDD.                                                                                      | ..   | ..   | ..   | V     |

#### 4.5.5.5 Regulator specifications, VREGH stage

| Symbol                 | Description                                                                                                                                 | Min. | Typ. | Max. | Units |
|------------------------|---------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|-------|
| V <sub>DDOUT</sub>     | VDD output voltage.                                                                                                                         | ..   | ..   | ..   | V     |
| I <sub>EXT,OFF</sub>   | External current draw <sup>3</sup> allowed in High voltage mode (supply on VDDH) during System OFF.                                         | ..   | ..   | ..   | mA    |
| I <sub>EXT,LOW</sub>   | External current draw <sup>3</sup> allowed in High voltage mode (supply on VDDH) when radio output power is higher than TBD dBm.            | ..   | ..   | ..   | mA    |
| I <sub>EXT,HIGH</sub>  | External current draw <sup>3</sup> allowed in High voltage mode (supply on VDDH) when radio output power is lower than or equal to TBD dBm. | ..   | ..   | ..   | mA    |
| V <sub>REGH,DROP</sub> | Minimum voltage drop in REGH (difference between voltage supplied on VDDH pin and voltage output on VDD pin).                               | ..   | ..   | ..   | V     |

### 4.6 USBREG - USB regulator control

The USB peripheral has its own voltage regulator. When using the USB peripheral, a 5 V USB supply needs to be provided on the VBUS pin.

The USB peripheral has a dedicated internal voltage regulator for converting the VBUS supply to 3.3 V to be used by the USB signalling interface (D+ and D- lines, and pull-up on D+). The rest of the USB peripheral (USBD) is supplied through the main supply like other on-chip features. As a consequence, both VBUS and combinations of VDDH and VDD are required for USB peripheral operation. For details on configuring the main supplies, see [Power supply modes and regulators](#) on page 32.

<sup>3</sup> External current draw is defined as the sum of all GPIO currents and the current being drawn from VDD.

When VBUS rises into its valid range, the software is notified through the [USBDETECTED](#) event. The [USBREMOVED](#) event is sent when VBUS goes below its valid range. Use these events to implement the USB startup sequence described in [USB power-up sequence](#) on page 678.

When VBUS rises into its valid range while the device is in System OFF, the device resets and transitions to System ON mode. The [RESETREAS](#) register will have the VBUS bit set to indicate the source of the wakeup.

See [VBUS detection specifications](#) on page 54 for the voltage level where events are sent ( $V_{BUS,DETECT}$  and  $V_{BUS,REMOVE}$ ) or where the system causes a wakeup from System OFF ( $V_{BUS,DETECT}$ ).

When the USB peripheral is enabled through the [ENABLE](#) register and VBUS is detected, the regulator is turned on. A [USBPWRRDY](#) event is sent when the regulator's worst case settling time has elapsed, indicating to the software that it can enable the USB pull-up to signal a USB connection to the host.

The software can read the state of the VBUS detection and regulator output readiness at any time through the [USBREGSTATUS](#) register.

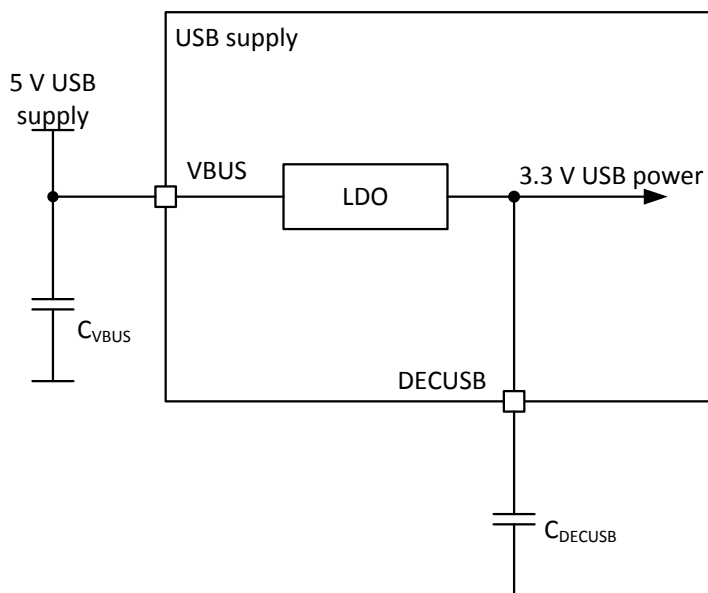


Figure 12: USB voltage regulator

To ensure stability, the input and output of the USB regulator need to be decoupled with a suitable decoupling capacitor  $C_{VBUS}$ . See [Reference circuitry](#) on page 768 for the recommended values.

### 4.6.1 Registers

| Base address | Domain      | Peripheral | Instance             | Secure mapping | DMA security | Description           | Configuration |
|--------------|-------------|------------|----------------------|----------------|--------------|-----------------------|---------------|
| 0x50037000   | APPLICATION | USBREG     | USBREGULATOR :       |                |              |                       |               |
|              |             |            | S                    |                |              |                       |               |
| 0x40037000   |             |            | US<br>USBREGULATOR : |                | NA           | USB regulator control |               |
|              |             |            | NS                   |                |              |                       |               |

Table 11: Instances

| Register            | Offset | Security | Description                                                 |
|---------------------|--------|----------|-------------------------------------------------------------|
| EVENTS_USBDETECTED  | 0x100  |          | Voltage supply detected on VBUS                             |
| EVENTS_USBREMOVED   | 0x104  |          | Voltage supply removed from VBUS                            |
| EVENTS_USBPWRRDY    | 0x108  |          | USB 3.3 V supply ready                                      |
| PUBLISH_USBDETECTED | 0x180  |          | Publish configuration for event <a href="#">USBDETECTED</a> |
| PUBLISH_USBREMOVED  | 0x184  |          | Publish configuration for event <a href="#">USBREMOVED</a>  |
| PUBLISH_USBPWRRDY   | 0x188  |          | Publish configuration for event <a href="#">USBPWRRDY</a>   |
| INTEN               | 0x300  |          | Enable or disable interrupt                                 |
| INTENSET            | 0x304  |          | Enable interrupt                                            |
| INTENCLR            | 0x308  |          | Disable interrupt                                           |
| USBREGSTATUS        | 0x400  |          | USB supply status                                           |

Table 12: Register overview

#### 4.6.1.1 EVENTS\_USBDETECTED

Address offset: 0x100

Voltage supply detected on VBUS

|                  |            |                    |       |                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------------------|-------|---------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                    |       | 31                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |                    |       |                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |
| Reset 0x00000000 |            |                    |       | 0                               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |
| ID               | Acce Field | Value ID           | Value | Description                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | EVENTS_USBDETECTED |       | Voltage supply detected on VBUS |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | NotGenerated       | 0     | Event not generated             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Generated          | 1     | Event generated                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

#### 4.6.1.2 EVENTS\_USBREMOVED

Address offset: 0x104

Voltage supply removed from VBUS

|                  |            |                   |       |                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-------------------|-------|----------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                   |       | 31                               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |                   |       |                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |
| Reset 0x00000000 |            |                   |       | 0                                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |
| ID               | Acce Field | Value ID          | Value | Description                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | EVENTS_USBREMOVED |       | Voltage supply removed from VBUS |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | NotGenerated      | 0     | Event not generated              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Generated         | 1     | Event generated                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

#### 4.6.1.3 EVENTS\_USBPWRRDY

Address offset: 0x108

USB 3.3 V supply ready

|                  |            |                  |       |    |    |                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|------------------|------------|------------------|-------|----|----|------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|--|
| Bit number       |            |                  | 31    | 30 | 29 | 28                     | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |
| ID               |            |                  | A     |    |    |                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| Reset 0x00000000 |            |                  | 0     | 0  | 0  | 0                      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |  |
| ID               | Acce Field | Value ID         | Value |    |    | Description            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| A                | RW         | EVENTS_USBPWRRDY |       |    |    | USB 3.3 V supply ready |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | NotGenerated     | 0     |    |    | Event not generated    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | Generated        | 1     |    |    | Event generated        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |

#### 4.6.1.4 PUBLISH\_USBDETECTED

Address offset: 0x180

Publish configuration for event **USBDETECTED**

|                  |            |          |                                                                                       |                    |                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|--------------------|--------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                    |                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |          | B                                                                                     |                    |                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |                    |                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 |                    | Description                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                              |                    | Channel that event <b>USBDETECTED</b> will publish to. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |                                                                                       |                    |                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Disable publishing |                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Enable publishing  |                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

#### 4.6.1.5 PUBLISH\_USBREMOVED

Address offset: 0x184

Publish configuration for event **USBREMOVED**

|                  |            |          |          |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|----------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |          |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |          |          | B                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value    | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0] | Channel that event <b>USBREMOVED</b> will publish to.                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |          |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0        | Disable publishing                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1        | Enable publishing                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

#### 4.6.1.6 PUBLISH\_USBPWRRDY

Address offset: 0x188

Publish configuration for event **USBPWRRDY**

|                  |            |          |                                                                                       |  |                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|--|------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |          | B                                                                                     |  |                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |  |                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 |  | Description                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                              |  | Channel that event <b>USBPWRRDY</b> will publish to. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |                                                                                       |  |                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     |  | Disable publishing                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     |  | Enable publishing                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

#### 4.6.1.7 INTEN

Address offset: 0x300

Enable or disable interrupt

| Bit number       |                |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|----------------|----------|---------------------------------------------------------------------------------------|-------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |                |          | C B A                                                                                 |                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |                |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field     | Value ID | Value                                                                                 | Description                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW USBDETECTED |          |                                                                                       | Enable or disable interrupt for event <a href="#">USBDETECTED</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                | Disabled | 0                                                                                     | Disable                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                | Enabled  | 1                                                                                     | Enable                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW USBREMOVED  |          |                                                                                       | Enable or disable interrupt for event <a href="#">USBREMOVED</a>  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                | Disabled | 0                                                                                     | Disable                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                | Enabled  | 1                                                                                     | Enable                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW USBPWRRDY   |          |                                                                                       | Enable or disable interrupt for event <a href="#">USBPWRRDY</a>   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                | Disabled | 0                                                                                     | Disable                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                | Enabled  | 1                                                                                     | Enable                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

#### 4.6.1.8 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number       |                |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|----------------|----------|---------------------------------------------------------------------------------------|---------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |                |          | C B A                                                                                 |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |                |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| D                | Acce Field     | Value ID | Value                                                                                 | Description                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW USBDETECTED |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">USBDETECTED</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                | Set      | 1                                                                                     | Enable                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                | Disabled | 0                                                                                     | Read: Disabled                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                | Enabled  | 1                                                                                     | Read: Enabled                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW USBREMOVED  |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">USBREMOVED</a>  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                | Set      | 1                                                                                     | Enable                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                | Disabled | 0                                                                                     | Read: Disabled                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                | Enabled  | 1                                                                                     | Read: Enabled                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW USBPWRRDY   |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">USBPWRRDY</a>   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                | Set      | 1                                                                                     | Enable                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                | Disabled | 0                                                                                     | Read: Disabled                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                | Enabled  | 1                                                                                     | Read: Enabled                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

#### 4.6.1.9 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number       |                |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|----------------|----------|---------------------------------------------------------------------------------------|----------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |                |          | C B A                                                                                 |                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |                |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field     | Value ID | Value                                                                                 | Description                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW USBDETECTED |          |                                                                                       | Write '1' to disable interrupt for event <a href="#">USBDETECTED</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                | Clear    | 1                                                                                     | Disable                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                | Disabled | 0                                                                                     | Read: Disabled                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                | Enabled  | 1                                                                                     | Read: Enabled                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW USBREMOVED  |          |                                                                                       | Write '1' to disable interrupt for event <a href="#">USBREMOVED</a>  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                | Clear    | 1                                                                                     | Disable                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                | Disabled | 0                                                                                     | Read: Disabled                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                | Enabled  | 1                                                                                     | Read: Enabled                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |



|                  |            |           |       |                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-----------|-------|--------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |           |       | 31                                                                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |           |       |                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | C | B | A |
| Reset 0x00000000 |            |           |       | 0                                                                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce Field | Value ID  | Value | Description                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| C                | RW         | USBPWRRDY |       | Write '1' to disable interrupt for event <a href="#">USBPWRRDY</a> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Clear     | 1     | Disable                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled  | 0     | Read: Disabled                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled   | 1     | Read: Enabled                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 4.6.1.10 USBREGSTATUS

Address offset: 0x400

USB supply status

| Bit number       |      |            |             | 31    | 30                                                                                                | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
|------------------|------|------------|-------------|-------|---------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| ID               |      |            |             |       |                                                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | B | A |
| Reset 0x00000000 |      |            |             | 0     | 0                                                                                                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |
| ID               | Acce | Field      | Value ID    | Value | Description                                                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | R    | VBUSDETECT |             |       | VBUS input detection status (USBDETECTED and USBREMOVED events are derived from this information) |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |            | NoVbus      | 0     | VBUS voltage below valid threshold                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |            | VbusPresent | 1     | VBUS voltage above valid threshold                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | R    | OUTPUTRDY  |             |       | USB supply output settling time elapsed                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |            | NotReady    | 0     | USBREG output settling time not elapsed                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |            | Ready       | 1     | USBREG output settling time elapsed (same information as USBPWRRDY event)                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 4.6.2 Electrical specification

#### 4.6.2.1 USB operating conditions

| Symbol            | Description                | Min. | Typ. | Max. | Units |
|-------------------|----------------------------|------|------|------|-------|
| V <sub>BUS</sub>  | Supply voltage on VBUS pin | ..   | ..   | ..   | V     |
| V <sub>DPDM</sub> | Voltage on D+ and D- lines | ..   | ..   | ..   | V     |

#### 4.6.2.2 USB regulator specifications

| Symbol                   | Description                                                                         | Min. | Typ. | Max. | Units |
|--------------------------|-------------------------------------------------------------------------------------|------|------|------|-------|
| I <sub>USB,QUIES</sub>   | USB regulator quiescent current drawn from VBUS (USB enabled)                       | ..   | ..   | ..   | μA    |
| t <sub>USBPWRDY</sub>    | Time from USB enabled to USBPWRDY event triggered, V <sub>BUS</sub> supply provided | ..   | ..   | ..   | ms    |
| V <sub>USB33</sub>       | On voltage at the USB regulator output (DECUSB pin)                                 | ..   | ..   | ..   | V     |
| R <sub>SOURCE,VBUS</sub> | Maximum source resistance on VBUS, including cable                                  | ..   | ..   | ..   | Ω     |
| C <sub>DECUSB</sub>      | Decoupling capacitor on the DECUSB pin                                              | ..   | ..   | ..   | μF    |

### 4.6.2.3 VBUS detection specifications

| Symbol                  | Description                                                  | Min. | Typ. | Max. | Units |
|-------------------------|--------------------------------------------------------------|------|------|------|-------|
| V <sub>BUS,DETECT</sub> | Voltage at which rising VBUS gets reported by USBDETECTED    | ..   | ..   | ..   | V     |
| V <sub>BUS,REMOVE</sub> | Voltage at which decreasing VBUS gets reported by USBREMOVED | ..   | ..   | ..   | V     |

## 4.7 VREQCTRL - Voltage request control

The VREQCTRL can request additional voltage on the VREGRADIO regulated supply to support +3 dBm TX power on RADIO.

Setting the [VREGRADIO.VREQH](#) register will request high voltage. The request is active until the register is cleared. Status register [VREGRADIO.VREQHREADY](#) indicates when the regulator has changed to high voltage.

### 4.7.1 Registers

| Base address | Domain  | Peripheral | Instance | Secure mapping | DMA security | Description             | Configuration |
|--------------|---------|------------|----------|----------------|--------------|-------------------------|---------------|
| 0x41004000   | NETWORK | VREQCTRL   | VREQCTRL | NS             | NA           | Voltage request control |               |

Table 13: Instances

| Register                             | Offset | Security | Description                                                                                                         |
|--------------------------------------|--------|----------|---------------------------------------------------------------------------------------------------------------------|
| <a href="#">VREGRADIO.VREQH</a>      | 0x500  |          | Request high voltage on RADIO<br>After requesting high voltage, the user must wait until VREQHREADY is set to Ready |
| <a href="#">VREGRADIO.VREQHREADY</a> | 0x508  |          | High voltage on RADIO is ready                                                                                      |

Table 14: Register overview

#### 4.7.1.1 VREGRADIO.VREQH ( Retained )

Address offset: 0x500

This register is a retained register

Request high voltage on RADIO

After requesting high voltage, the user must wait until VREQHREADY is set to Ready

|                  |            |          |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW VREQH   |          |       | Request high voltage                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0     | Disable                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1     | Enable                                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

#### 4.7.1.2 VREGRADIO.VREQHREADY

Address offset: 0x508

High voltage on RADIO is ready

|                  |            |          |  |          |   |  |       |  |  |             |                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|--|----------|---|--|-------|--|--|-------------|-------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |  |          |   |  |       |  |  | 31          | 30                                        | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |          |  |          |   |  |       |  |  |             |                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |   |
| Reset 0x00000000 |            |          |  |          |   |  |       |  |  | 0           | 0                                         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |          |  | Value ID |   |  | Value |  |  | Description |                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | R          | READY    |  |          |   |  |       |  |  |             | RADIO is ready to operate on high voltage |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | NotReady |  |          | 0 |  |       |  |  |             | Not ready                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Ready    |  |          | 1 |  |       |  |  |             | Ready                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

## 4.8 RESET - Reset control

A reset in the system is triggered by either a system-level or core-level reset source.

A system-level reset will reset all cores. Power-on reset, brownout reset, and pin reset are examples of a system-level reset. A core-level reset, such as a soft reset or a lockup, will reset either the entire core or only part of it. The different reset sources in the system are illustrated in the following figure.

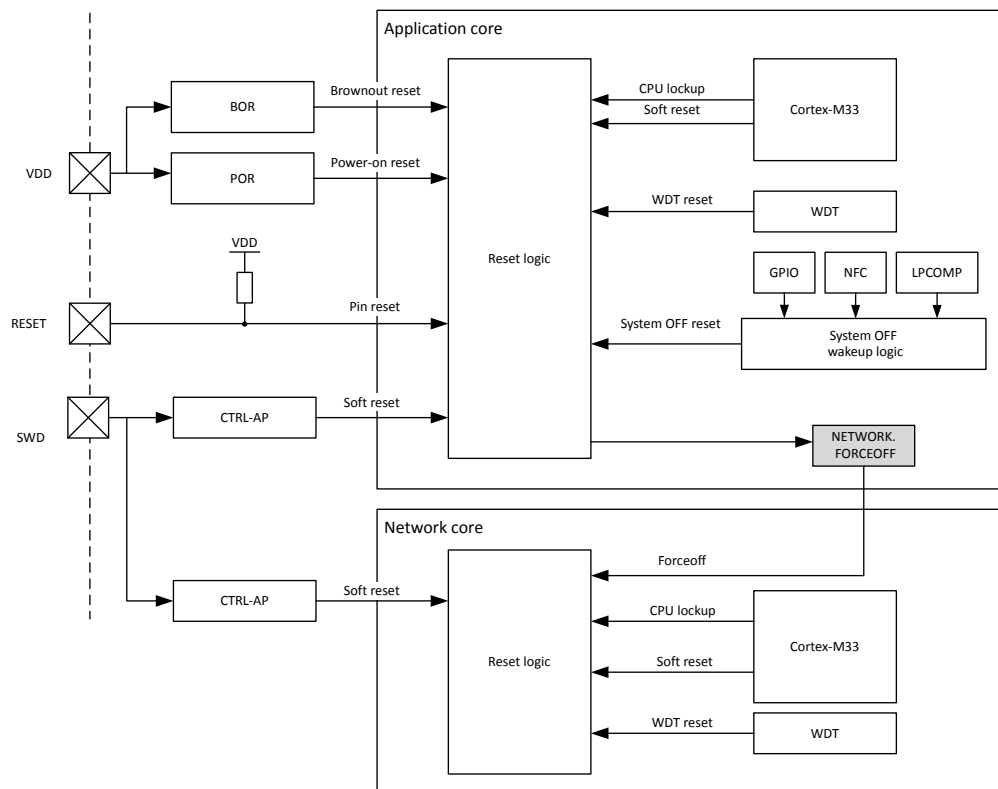


Figure 13: Reset sources

After a system-level reset, the application core will start up on its own and will then start the network core as necessary.

After a reset has occurred, the register [RESETREAS](#) on page 59 can be read to determine which source generated the reset. Each core has its own [RESETREAS](#) register. System-level and application core reset sources are also available in the network core's [RESETREAS](#) register, unless otherwise noted.

### 4.8.1 Power-on reset

The power-on reset (POR) generator initializes the system when the VDD supply voltage is above the power-on threshold. This also applies in high voltage mode, where the VDD supply voltage is provided by the high voltage regulator (VREGH).

The system is held in a reset state until the supply has reached the minimum operating voltage, and the internal voltage regulators have started. After a power-on reset, the application core is started while the network core is held in reset, see [Network force off](#) on page 57.

### 4.8.2 Pin reset

A pin reset is generated when the physical reset pin on the device is asserted.

Similar to a power-on reset, the application core is started after the reset pin is deasserted. The network core is held in reset, see [Network force off](#) on page 57.

The reset pin has an internal pull-up resistor with the same resistance as GPIO pull-ups, see [GPIO — General purpose input/output](#) on page 209.

### 4.8.3 Brownout reset

The brownout reset (BOR) generator puts the system in reset state if the VDD supply voltage drops below the brownout reset threshold. This also applies in high voltage mode, where the VDD supply voltage is provided by the high voltage regulator (VREGH).

Similar to a power-on reset, the application core is started after BOR is deasserted while the network core is held in reset, see [Network force off](#) on page 57.

### 4.8.4 Wakeup from System OFF mode reset

The device is reset when it wakes up from System OFF mode.

Similar to a power-on reset, the application core is started while the network core is held in reset, see [Network force off](#) on page 57.

If the device is in debug interface mode, the debug access port (DAP) is not reset after a wakeup from System OFF. For more information, see [Overview](#) on page 730.

### 4.8.5 Soft reset

Soft reset is generated when the SYSRESETREQ bit of the application interrupt and reset control register (AIRCRR) in the Arm core of the application and network cores is set. For more information, see [ARM documentation](#).

When the application core performs a soft reset, the network core is held in reset, see [Network force off](#) on page 57. A soft reset in the network core will only cause the network core to reset.

A soft reset can also be generated using the [RESET](#) on page 742 register in the associated CTRL-AP.

### 4.8.6 Watchdog timer reset

A watchdog timer (WDT) reset is generated when the watchdog timer times out.

Each core has its own WDT instance. When the application core gets a WDT reset, the network core is held in reset, see [Network force off](#) on page 57. A WDT reset in the network core will only cause the network core to reset. The reset target depends on the core where WDT is instantiated.

**Note:** Because the network core WDT reset is local for the network core, the application core is not aware of WDT timing out in the network core. Notifying the application core is possible. One way is to check the register [RESETREAS](#) on page 59 for WDT flags and report the error through inter-processor communication (IPC).

For more information about WDT, see [WDT — Watchdog timer](#) on page 721. More information about IPC is available in [IPC — Interprocessor communication](#) on page 252.

### 4.8.7 Network force off

The application core can force off the network core, which resets it and switches off its power and clocks.

A FORCEOFF can be issued to the network core by the application core. To force off the network core, use the register [NETWORK.FORCEOFF](#) on page 61.

Application core resets implicitly result in a force off of the network core. The network core will be held in force off until the application core releases the force off signal from the [NETWORK.FORCEOFF](#) register.

### 4.8.8 Retained registers

A retained register is one that retains its value in System OFF and/or Force off mode and when reset, depending on the reset source. See individual peripheral chapters for information about which registers are retained for the various peripherals.

### 4.8.9 Application core reset behavior

Application core reset behavior depends on the reset source.

Any reset in the application core will cause a network core force off, triggering the FORCEOFF reset source in the network core. For more information, see [Network force off](#) on page 57.

In System OFF mode, the watchdog timer is not running and there is no CPU lockup possible. RAM may be fully or partially retained, depending on RAM retention settings in [VMC — Volatile memory controller](#) on page 719.

If the device is in Debug Interface mode, the debug components will not be reset. Additionally, CPU lockup will not generate a reset. See [Overview](#) on page 730 for more information about the different debug components in the system.

Application core reset targets and their reset sources are summarized in the following table.

An 'x' in the table means that the specific module is reset.

| Reset source                      | Reset target |              |       |                |     |            |
|-----------------------------------|--------------|--------------|-------|----------------|-----|------------|
|                                   | CPU          | Network core | Debug | RAM            | WDT | RESETPREAS |
| CPU lockup                        | x            | x            |       |                |     |            |
| Soft reset                        | x            | x            |       |                |     |            |
| Wakeup from System OFF mode reset | x            | x            | x     | x <sup>4</sup> | x   |            |
| Watchdog timer reset              | x            | x            | x     | x              | x   |            |
| Pin reset                         | x            | x            | x     | x              | x   |            |
| Brownout reset                    | x            | x            | x     | x              | x   | x          |
| Power-on reset                    | x            | x            | x     | x              | x   | x          |
| NETWORK.FORCEOFF                  |              | x            |       |                |     |            |

Table 15: Application core reset targets and their reset sources

**Note:** RAM is never reset, but depending on the reset source, its content may be corrupted.

Some retained registers may have a different reset behavior, as shown in the following table.

<sup>4</sup> Depending on RAM retention settings.

An 'x' in the table means that the specific module is reset.

| Reset source                      | Reset target                 |     |      |                         |                |
|-----------------------------------|------------------------------|-----|------|-------------------------|----------------|
|                                   | Regular peripheral registers | SPU | GPIO | REGULATORS, OSCILLATORS | POWER.GPREGRET |
| CPU lockup                        | x                            | x   | x    |                         |                |
| Soft reset                        | x                            | x   | x    |                         |                |
| Wakeup from System OFF mode reset | x                            |     |      |                         |                |
| Watchdog timer reset              | x                            | x   | x    | x                       |                |
| Pin reset                         | x                            | x   | x    | x                       |                |
| Brownout reset                    | x                            | x   | x    | x                       | x              |
| Power-on reset                    | x                            | x   | x    | x                       | x              |

Table 16: Application core reset behavior for retained registers

#### 4.8.10 Network core reset behavior

Network core reset behavior depends on the reset source.

In System OFF mode, or when the network core is held in force-off, the watchdog timer is not running and there is no CPU lockup possible. RAM may be fully or partially retained, depending on RAM retention settings in [VMC — Volatile memory controller](#) on page 719.

If the device is in Debug Interface mode, the debug components will not be reset. Additionally, CPU lockup will not generate a reset. See [Overview](#) on page 730 for more information about the different debug components in the system.

Any reset in the application core will cause a network core force off, triggering the network FORCEOFF reset source in the following table. For more information, see [Network force off](#) on page 57.

An 'x' in the table means that the specific module is reset. Pin reset, brownout reset, and power-on reset are system level reset sources with the network core and application core having the same behavior, see [Application core reset behavior](#) on page 57.

| Reset source                     | Reset target |                |     |           |
|----------------------------------|--------------|----------------|-----|-----------|
|                                  | CPU          | RAM            | WDT | RESETREAS |
| CPU lockup                       | x            |                |     |           |
| Soft reset                       | x            |                |     |           |
| Network FORCEOFF                 | x            | x <sup>5</sup> | x   |           |
| Application Watchdog timer reset | x            | x              | x   |           |
| Local Watchdog timer reset       | x            | x              | x   |           |

Table 17: Network core reset target sources

**Note:** RAM is never reset, but its content may be corrupted depending on the reset source.

Some retained registers may have a different reset behavior, as shown in following table.

<sup>5</sup> Depending on RAM retention settings.

An 'x' in the table means that the specific module is reset. Pin reset, brownout reset, and power-on reset are system level reset sources with the network core and application core having the same behavior, see [Application core reset behavior](#) on page 57.

| Reset source                     | Reset target                 |                |                |
|----------------------------------|------------------------------|----------------|----------------|
|                                  | Regular peripheral registers | GPIO           | POWER.GPREGRET |
| CPU lockup                       | x                            | x <sup>6</sup> |                |
| Soft reset                       | x                            | x <sup>6</sup> |                |
| Network FORCEOFF                 | x                            |                |                |
| Application Watchdog timer reset | x                            | x              |                |
| Local Watchdog timer reset       | x                            | x              |                |

Table 18: Network core reset behavior for retained registers

## 4.8.11 Registers

| Base address | Domain      | Peripheral | Instance   | Secure mapping | DMA security | Description              | Configuration |
|--------------|-------------|------------|------------|----------------|--------------|--------------------------|---------------|
| 0x50005000   | APPLICATION | RESET      | RESET : S  | US             | NA           | Reset control and status |               |
| 0x40005000   |             |            | RESET : NS |                |              |                          |               |
| 0x41005000   | NETWORK     | RESET      | RESET      | NS             | NA           | Reset status             |               |

Table 19: Instances

| Register         | Offset | Security | Description                               |
|------------------|--------|----------|-------------------------------------------|
| RESETRAS         | 0x400  |          | Reset reason                              |
| NETWORK.FORCEOFF | 0x614  |          | Force off power and clock in network core |

Table 20: Register overview

### 4.8.11.1 RESETRAS

Address offset: 0x400

Reset reason

Unless cleared, the RESETRAS register will be cumulative. A field is cleared by writing '1' to it.

| Bit number       |  |  | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         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| ID               |  |  | Q P O N M                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     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| Reset 0x00000000 |  |  | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 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|  |  |  |  |  |  |  |  |  |       |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

<sup>6</sup> MCUSEL settings are kept.

| Bit number       |      |           |             | 31    | 30                                                                                                     | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |
|------------------|------|-----------|-------------|-------|--------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ID               |      |           |             | Q     |                                                                                                        |    |    |    |    |    |    | P  | O  | N  | M  | K  |    |    |    |    |    |    |    | J  | I  | H |   |   |   |   |   |   |   | G | F | E | D | C | B | A |
| Reset 0x00000000 |      |           |             | 0     | 0                                                                                                      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |   |
| ID               | Acce | Field     | Value ID    | Value | Description                                                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| E                | RW   | LOCKUP    | Detected    | 1     | Detected                                                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | NotDetected | 0     | Reset from application CPU lockup detected                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | Detected    | 1     | Not detected                                                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| F                | RW   | OFF       | Detected    | 1     | Detected                                                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | NotDetected | 0     | Reset due to wakeup from System OFF mode when wakeup is triggered by DETECT signal from GPIO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | Detected    | 1     | Not detected                                                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| G                | RW   | LPCOMP    | Detected    | 1     | Detected                                                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | NotDetected | 0     | Reset due to wakeup from System OFF mode when wakeup is triggered by ANADETECT signal from LPCOMP      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | Detected    | 1     | Not detected                                                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| H                | RW   | DIF       | Detected    | 1     | Detected                                                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | NotDetected | 0     | Reset due to wakeup from System OFF mode when wakeup is triggered by entering the debug interface mode |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | Detected    | 1     | Not detected                                                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| I                | RW   | LSREQ     | Detected    | 1     | Detected                                                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | NotDetected | 0     | Reset from network soft reset detected                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | Detected    | 1     | Note: Not available for application core                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| J                | RW   | LLOCKUP   | Detected    | 1     | Detected                                                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | NotDetected | 0     | Reset from network CPU lockup detected                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | Detected    | 1     | Note: Not available for application core                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| K                | RW   | LDOG      | Detected    | 1     | Detected                                                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | NotDetected | 0     | Reset from network watchdog timer detected                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | Detected    | 1     | Note: Not available for application core                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| M                | RW   | MFORCEOFF | Detected    | 1     | Detected                                                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | NotDetected | 0     | Force off reset from application core detected                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | Detected    | 1     | Note: Not available for application core                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| N                | RW   | NFC       | Detected    | 1     | Detected                                                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | NotDetected | 0     | Reset after wakeup from System OFF mode due to NFC field being detected                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | Detected    | 1     | Not detected                                                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| O                | RW   | DOG1      | Detected    | 1     | Detected                                                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | NotDetected | 0     | Reset from application watchdog timer 1 detected                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | Detected    | 1     | Not detected                                                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| P                | RW   | VBUS      | Detected    | 1     | Detected                                                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | NotDetected | 0     | Reset after wakeup from System OFF mode due to VBUS rising into valid range                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | Detected    | 1     | Not detected                                                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |



| Bit number       |            |         |             | 31                                       | 30 | 29 | 28 | 27                                  | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |
|------------------|------------|---------|-------------|------------------------------------------|----|----|----|-------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ID               |            |         |             | Q                                        |    |    |    |                                     |    |    |    |    |    | P  | O  | N  | M  | K  |    |    |    |    | J  | I  | H  |   |   |   |   |   |   |   |   |   | G | F | E | D | C | B | A |
| Reset 0x00000000 |            |         |             | 0                                        | 0  | 0  | 0  | 0                                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |   |   |
| ID               | Acce Field |         | Value ID    | Value                                    |    |    |    | Description                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Q                | RW         | LCTRLAP |             |                                          |    |    |    | Reset from network CTRL-AP detected |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |         |             | Note: Not available for application core |    |    |    |                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |         | NotDetected | 0                                        |    |    |    | Not detected                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |         | Detected    | 1                                        |    |    |    | Detected                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 4.8.11.2 NETWORK.FORCEOFF

Address offset: 0x614

Force off power and clock in network core

Not available for network core

|                  |            |          |       |                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|-------|-------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |       | 31                                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |          |       |                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |
| Reset 0x00000001 |            |          |       | 0                                         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |   |
| ID               | Acce Field | Value ID | Value | Description                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | FORCEOFF |       | Force off power and clock in network core |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Release  | 0     | Release force off signal                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Hold     | 1     | Hold force off signal                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

## 4.9 CLOCK — Clock control

The clock control system can source the system clocks from a range of internal or external high and low frequency oscillators, and distribute them to modules based on the module's individual requirements. Clock distribution is automated and grouped independently by module to limit current consumption in unused branches of the clock tree.

Each core subsystem has its own clock control system that is responsible for requesting resources from the power and clock subsystem.

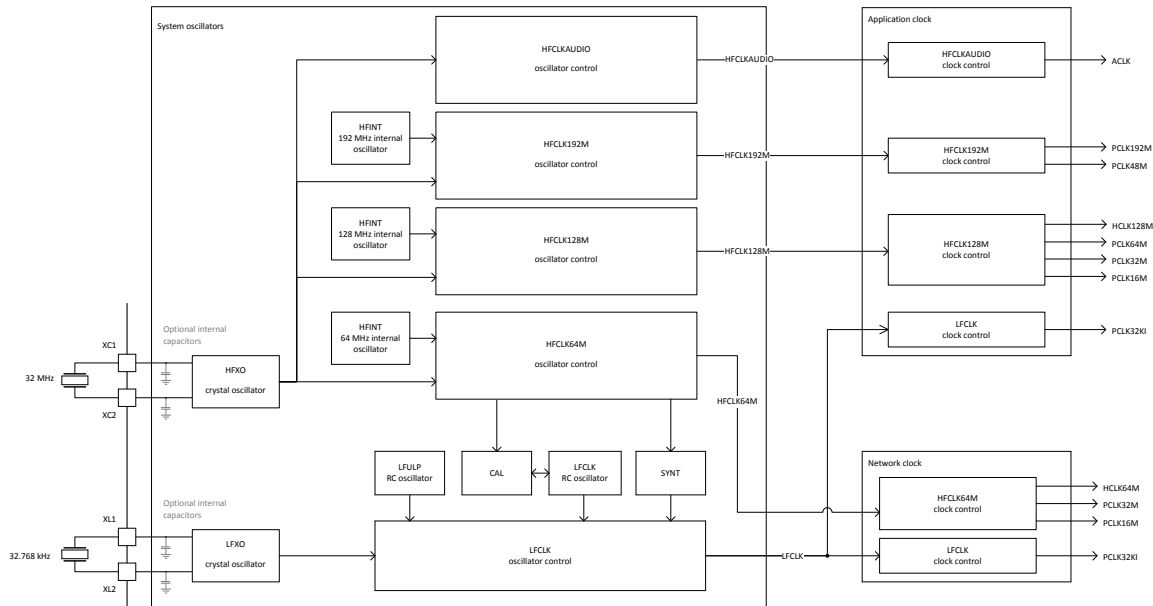


Figure 14: Clock control

The power and clock subsystem secures glitch-free switching from one clock source to another. This applies to all clock sources.

**Note:** Registers [INTEN](#) on page 77, [INTENSET](#) on page 78, and [INTENCLR](#) on page 78 are the same registers (at the same address) as the corresponding registers in POWER.

#### 4.9.1 HFCLK controller

Each core has a number of high frequency clock (HFCLK) control instances. Each instance distributes one or more clocks to the core.

The following table lists the core clocks that are available.

| Core clock | Description                                             |
|------------|---------------------------------------------------------|
| HCLK128M   | Scalable 128 MHz CPU clock for the application core     |
| HCLK64M    | 64 MHz CPU clock for the network core                   |
| PCLK192M   | Scalable 192 MHz clock for QSPI                         |
| PCLK64M    | 64 MHz peripheral clock                                 |
| PCLK48M    | 48 MHz clock for USB                                    |
| PCLK32M    | 32 MHz peripheral clock                                 |
| PCLK16M    | 16 MHz peripheral clock                                 |
| ACLK       | 11.289 MHz or 12.288 MHz tunable audio peripheral clock |

Table 21: Core clocks

The HFCLK clocks sourced from the power and clock subsystem to the HFCLK control instances are the following:

| HFCLK clock | Description         |
|-------------|---------------------|
| HFCLK128M   | 128 MHz HFCLK clock |
| HFCLK64M    | 64 MHz HFCLK clock  |
| HFCLK192M   | 192 MHz HFCLK clock |
| HFCLKAUDIO  | Audio HFCLK clock   |

Table 22: HFCLK clocks for HFCLK control instances

In order to generate the HFCLK clocks, the following HFCLK sources are available:

- 192 MHz/128 MHz/64 MHz internal oscillator (HFINT)
- 32 MHz crystal oscillator (HFXO), optionally using built-in capacitors as described in [OSCILLATORS — Oscillator control](#) on page 88

See [Figure 14: Clock control](#) on page 62 for more information.

CPUs, peripherals, and other system components within a core will automatically request clocks from its corresponding local HFCLK control. The HFCLK control passes the request to the power and clock subsystem and, once the clocks are running, distributes them to the components within the core.

When HFCLK control requests within a core are stopped, the HFCLK control will stop requesting clock from the power and clock subsystem. For example, when the CPU enters sleep or when peripherals have completed their tasks. If there are no HFCLK control requests from any core, the power and clock subsystem will automatically stop the clock.

When the system enters System ON mode, and a HFCLK clock is requested, the relevant HFINT will be used as the HFCLK source. When requests for the clock are stopped, the HFINT will automatically stop.

HFCLK clocks are only available to the HFCLK controllers when the system is in System ON mode.

It is possible to have a HFCLK source running before being started by the relevant clock request (for instance, the HFCLK source is kept running during sleep). This gives shorter start-up time but causes increased power consumption. Starting the HFXO is needed when crystal clock accuracy is required.

The HFCLK source selected in register [HFCLKSRC](#) on page 82 is started by triggering the [HFCLKSTART](#) task.

The source for the HFCLK128M/HFCLK64M clocks can be configured at any time (for instance, when the HFCLK has already been started). The content of the [HFCLKSRC](#) register only takes effect when the [HFCLKSTART](#) task is triggered.

The event [HFCLKSTARTED](#) is generated when the [HFCLKSTART](#) task is triggered, the oscillator is started, and the frequency is stabilized.

The HFCLK source selected in register [HFCLK192MSRC](#) on page 85 is started by triggering the [HFCLK192MSTART](#) task.

The source for the HFCLK192M clock can be configured at any time (for instance, when the HFCLK has already been started). The content of the [HFCLK192MSRC](#) register only takes effect when the [HFCLK192MSTART](#) task is triggered.

The event [HFCLK192MSTARTED](#) is generated when the [HFCLK192MSTART](#) task is triggered, the oscillator is started, and the frequency stabilized.

The HFXO is started by triggering the [HFCLKAUDIOSTART](#) task.

The event [HFCLKAUDIOSTARTED](#) is generated when the [HFCLKAUDIOSTART](#) task is triggered, the oscillator is started, and the frequency stabilized.

It is possible to trigger a new START task after one has already been triggered, and before the corresponding STARTED event is generated. In this case, only one STARTED event will be generated, corresponding to the last triggered START task. Triggering a START task after the STARTED event from a previous triggered START task is generated, will generate a new STARTED event.

Time from a START task to the corresponding STARTED event may differ depending on whether the HFCLK source is already running or in the process of starting. The amount of time before a STARTED event may vary when a different HFCLK source is configured before triggering a new START task.

When the clock control system switches from HFINT source to HFXO source, the HFXO becomes active after a HFXO startup time set in register [HFXOCNT](#) on page 117. The startup time is programmable, enabling the use of different types of crystal oscillators (e.g. standard crystals that may have different startup times).

The HFXO must be selected and started in order to do the following:

- Use RADIO
  - The network domain [HFCLKSTART](#) task is used
- Enable USB D to respond to USB traffic
  - The application domain [HFCLK192MSTART](#) is used
- Set NFCT to activated state
  - The application domain [HFCLKSTART](#) task is used
- Improve SAADC performance by reducing clock jitter
  - The application domain [HFCLKSTART](#) task is used

Each HFCLK control can request the HFXO source independently from one another via the corresponding START task. This ensures that each core and peripheral will have access to a high accuracy clock when needed. Core clocks that originate from the same HFCLK clock will also have the same HFCLK source. This means that parts of the core that have not requested the HFXO may get a clock that is more accurate than expected, but not the other way around.

All cores that have requested a HFCLK source to start by triggering a START task must also request it to stop by triggering the corresponding STOP task (see [HFCLKSTOP](#), [HFCLK192MSTOP](#) and [HFCLKAUDIOSTOP](#) tasks) before the power and clock subsystem will stop it.

HFCLK source(s) will stop when all corresponding STOP tasks have been triggered and there are no requests for HFCLK clock(s) from the system.

Triggering a HFCLK STOP task is required only if the corresponding HFCLK START task has been triggered before. When a HFCLK START task is triggered, it is possible to trigger again the same HFCLK START task without triggering the corresponding HFCLK STOP task in between.

#### 4.9.1.1 Application core frequency scaling

The application core clocks can be scaled from their respective HFCLK clocks.

The application core clock HCLK128M can be scaled from the HFCLK128M clock using the [HFCLKCTRL](#) register.

The HCLK192M clock can be scaled from the HFCLK192M clock using the [HFCLK192MCTRL](#) register.

**Note:** Settings Div1 and Div2 in [HFCLK192MCTRL](#) register will result in increased power consumption.

The ACLK audio clock cannot be scaled from the HFCLKAUDIO clock. Instead, its frequency can be configured in the relevant peripherals. Refer to [Audio oscillator](#) on page 65 for more information on audio clock and related peripherals.

**Note:** It is possible to scale the application core clocks at any time. For instance, when a clock has already been started, without having to stop it first.

#### 4.9.1.2 32 MHz crystal oscillator (HFXO)

The 32 MHz crystal oscillator (HFXO) is controlled by a 32 MHz external crystal, see [OSCILLATORS — Oscillator control](#) on page 88.

#### 4.9.1.3 Audio oscillator

The audio oscillator generates clock frequencies suitable for audio applications.

The audio oscillator has the following features:

- Adjustable frequency with 3.3 ppm resolution in two frequency bands - 11.176 MHz to 11.402 MHz, and 12.165 MHz to 12.411 MHz
- Low jitter, suitable for audio applications
- Always uses the HFXO

The HFCLKAUDIO clock generated by the audio oscillator is suitable for use as the source clock in the I<sup>2</sup>S and PDM audio peripherals. In order to use this clock, it must be selected in the corresponding configuration registers in these peripherals. It is required to trigger the [HFCLKAUDIOSTART](#) task before it is used. To stop the HFCLKAUDIO clock, the [HFCLKAUDIOSTOP](#) task must be triggered. After triggering this task, the oscillator will be kept running as long as a peripheral is using it.

In applications where the audio data is arriving asynchronously to on-chip clocks, the frequency can be adjusted to stay in sync with the sender. The frequency can be configured in register [HFCLKAUDIO.FREQUENCY](#) on page 83 using one of the following equations.

$$f_{out} = \frac{32M}{12} (4 + HFCLKAUDIO.FREQUENCY \cdot 2^{-16})$$

Figure 15: Calculating audio frequency  $f_{out}$  from register value

$$HFCLKAUDIO.FREQUENCY = 2^{16} \left( \frac{12f_{out}}{32M} - 4 \right)$$

Figure 16: Calculating register value from audio frequency  $f_{out}$

The acceptable [HFCLKAUDIO.FREQUENCY](#) register value ranges for the two frequency bands are listed in the following table.

When switching between the two frequency ranges, the peripherals must be stopped.

| Frequency band           | Register value and frequency |                       |                       |
|--------------------------|------------------------------|-----------------------|-----------------------|
|                          | Min                          | Center                | Max                   |
| 11.176 MHz to 11.402 MHz | 12519<br>(11.176 MHz)        | 15298<br>(11.289 MHz) | 16068<br>(11.402 MHz) |
| 12.165 MHz to 12.411 MHz | 36834<br>(12.165 MHz)        | 39854<br>(12.288 MHz) | 42874<br>(12.411 MHz) |

Table 23: HFCLKAUDIO.FREQUENCY register ranges

#### 4.9.1.4 Overriding the automatic HFCLK control system

Overriding the automatic clock control system is possible to ensure a HFCLK clock is started and kept running, even if not requested.

This can be used to avoid associated HFCLK clock start-up times and have the highest clock accuracy after wake-up from sleep.

The register [HFCLKALWAYSRUN](#) on page 84 can override the automatic clock control system for the HFCLK128M/HFCLK64M clocks. This override is initiated by performing the following steps:

1. Set [HFCLKSRC.SRC](#) to select the HFCLK source.
2. Set [HFCLKALWAYSRUN.ALWAYSRUN](#).
3. Trigger the [HFCLKSTART](#) task.

The register [HFCLK192MALWAYSRUN](#) on page 85 can override the automatic clock control system for the HFCLK192M clock. This override is initiated by performing the following steps:

1. Set [HFCLK192MSRC.SRC](#) to select the HFCLK source.
2. Set [HFCLK192MALWAYSRUN.ALWAYSRUN](#).
3. Trigger the [HFCLK192MSTART](#) task.

Registers [HFCLKSRC/HFCLK192MSRC](#) and [HFCLKALWAYSRUN/HFCLK192MALWAYSRUN](#) can be written at any time, but are only activated by the START task.

The register [HFCLKAUDIOALWAYSRUN](#) on page 84 can override the automatic clock control system for the HFCLKAUDIO clock. The override is initiated by performing the following steps:

1. Set [HFCLKAUDIOALWAYSRUN.ALWAYSRUN](#).
2. Trigger the [HFCLKAUDIOSTART](#) task.

**Note:** In this case, the HFCLK source is always the HFXO.

Register [HFCLKAUDIOALWAYSRUN](#) can be written at any time, but is only activated by the START task.

#### 4.9.2 LFCLK controller

Each core has a number of low frequency clock (LFCLK) control instances. Each instance distributes one or more clocks to the core.

The LFCLK control instance in each core distributes the 32.768 kHz PCLK32KI peripheral clock to its corresponding core. The LFCLK clock is sourced from the power and clock subsystem to each LFCLK control instance.

In order to generate the LFCLK clock, the LFCLK controller uses the following LFCLK sources:

- 32.768 kHz RC oscillator (LFRC)
- 32.768 kHz ultra-low power RC oscillator (LFULP)
- 32.768 kHz crystal oscillator (LFXO)
- 32.768 kHz synthesized from HFCLK (LFSYNT)

To see an illustration of the clock sources, see [Figure 14: Clock control](#) on page 62.

The LFCLK controller and all LFCLK sources are switched off in System OFF mode.

When peripherals require the PCLK32KI clock, such as [RTC — Real-time counter](#) on page 488 and [WDT — Watchdog timer](#) on page 721, the LFCLK control will automatically request the LFCLK clock to the power and clock subsystem. The default LFCLK source is the LFRC.

When LFCLK control requests are stopped, LFCLK will stop requesting clock from the power and clock subsystem. If there are no LFCLK control requests from other cores, the power and clock subsystem will automatically stop the LFCLK clock and the LFRC source.

The LFCLK source may also be started by triggering the **LFCLKSTART** task. The LFCLK source is configured by selecting the preferred LFCLK source in register **LFCLKSRC** on page 83. Once selected, the LFCLK source will be started by triggering the **LFCLKSTART** task.

The LFCLK source can be configured at any time (for instance, when the LFCLK has already been started). The content of the **LFCLKSRC** register only takes effect when the **LFCLKSTART** task is triggered.

**Note:** Automatic requests of the LFCLK clock will ignore the value in **LFCLKSRC** and use **LFRC** as source, unless the LFCLK source is started by triggering the **LFCLKSTART** task. In this case, the LFCLK source will correspond to the value in **LFCLKSRC** when the **LFCLKSTART** task was last triggered.

The **LFCLKSTARTED** event will be generated after the **LFCLKSTART** task has been triggered and the LFCLK source has started. Triggering a **LFCLKSTART** task before the **LFCLKSTARTED** event from a previous **LFCLKSTART** task is generated will only generate one **LFCLKSTARTED** event. Triggering a **LFCLKSTART** task after a **LFCLKSTARTED** event is generated will generate a new **LFCLKSTARTED** event.

The LFCLK clock is stopped when nothing requests it, e.g. **RTC — Real-time counter** on page 488 and **WDT — Watchdog timer** on page 721 are stopped, and the **LFCLKSTOP** task is triggered. This must be done for all cores. Triggering the **LFCLKSTOP** task is required only if the **LFCLKSTART** task has been triggered before.

When the **LFCLKSTART** task is triggered, it is possible to trigger a new **LFCLKSTART** task without triggering a **LFCLKSTOP** task in between.

If the **LFXO** is selected as the LFCLK source, the LFCLK clock will initially start running from the **LFRC** while the **LFXO** is starting up, and then automatically switch to using the **LFXO** once this oscillator is running.

Events will be generated in the correct order, even if an LFCLK source that is already started by another LFCLK control instance is requested. The timing of events may differ, depending on whether a LFCLK source is already running or in the process of starting.

If two instances of the LFCLK control system request different LFCLK sources, the power and clock subsystem will secure that the most accurate of the requested LFCLK sources is selected.

If one LFCLK control instance requests a particular LFCLK source to stop when another LFCLK control instance (or a peripheral) requests the same source to run, but at a lower accuracy, the power and clock subsystem will switch to the less accurate source. The following table summarizes the priorities of the LFCLK sources.

| Priority | LFCLK source |
|----------|--------------|
| Highest  | LFSYNT       |
| ...      | LFXO         |
| ...      | LFRC         |
| Lowest   | LFULP        |

Table 24: LFCLK request priority

When switching the LFCLK source, such as from **LFRC** to **LFXO**, up to one LFCLK cycle may be lost.

#### 4.9.2.1 32.768 kHz RC oscillator (LFRC)

An internal 32.768 kHz RC oscillator (**LFRC**) is available as the LFCLK source.

The **LFRC** oscillator is fully embedded in nRF5340 and does not require additional external components.

##### 4.9.2.1.1 Calibrating the 32.768 kHz RC oscillator

To improve accuracy of the **LFRC** oscillator, it can be calibrated using the **HFXO** as a reference oscillator.

The **LFRC** oscillator can be calibrated while it is running. The calibration is started by triggering the **CAL** task which temporarily requests the **HFCLK** with **HFXO** as the source for calibration.

A **DONE** event will be generated when the calibration is finished.

**Note:** Any core changing the LFCLK source will abort calibration without the **DONE** event being generated in the core triggering the **CAL** task.

If **CAL** task is triggered while a calibration routine is already running (i.e. before the **DONE** event is generated), the **CAL** task has no effect and the calibration continues.

All cores can trigger the **CAL** task independently of each other. As a result, each core will receive a corresponding **DONE** event. If the calibration routine is already running (i.e. a core has triggered the **CAL** task), and the **CAL** task is triggered from another core, a **DONE** event is generated in both cores when the calibration of its corresponding LFRC oscillator is complete.

#### 4.9.2.2 32.768 kHz ultra-low power RC oscillator (LFULP)

An internal 32.768 kHz ultra-low power RC oscillator (LFULP) is available as an LFCLK source.

The LFULP oscillator is fully embedded in the SOC and does not require additional external components. Compared to the LFRC, the LFULP uses less power but has decreased accuracy. This oscillator can be used as a coarse, low-precision time reference in applications where low power is the main requirement.

Unlike the LFRC oscillator, the LFULP oscillator cannot be calibrated.

#### 4.9.2.3 32.768 kHz crystal oscillator (LFXO)

For higher LFCLK accuracy (when greater than  $\pm 250$  ppm accuracy is required), the low frequency crystal oscillator (LFXO) must be used.

This clock source requires external components, see [OSCILLATORS — Oscillator control](#) on page 88.

#### 4.9.2.4 32.768 kHz synthesized from HFCLK (LFSYNT)

LFCLK can be synthesized from the HFCLK clock source.

LFSYNTH depends on the HFCLK to run. The accuracy of the LFCLK clock with LFSYNTH as a source assumes the accuracy of the HFCLK. If high accuracy is required, the HFCLK must be generated from the HFXO.

Using the LFSYNT clock removes the requirement for an external 32.768 kHz crystal, but increases average power consumption as the HFCLK will need to be requested in the system.

#### 4.9.2.5 Overriding the automatic LFCLK control system

Overriding the automatic clock control system to ensure the LFCLK clock is started and kept running is possible, even if not requested.

This can be used to avoid associated LFCLK clock start-up times and have the highest clock accuracy after wake-up from sleep.

The register [LFCLKALWAYSRUN](#) on page 84 can override the automatic clock control system. This override is initiated by performing the following steps:

1. Set [LFCLKSRC.SRC](#) to select the LFCLK source.
2. Set [LFCLKALWAYSRUN.ALWAYSRUN](#).
3. Trigger the [LFCLKSTART](#) task.

Registers [LFCLKSRC.SRC](#) and [LFCLKALWAYSRUN.ALWAYSRUN](#) can be written at any time, but are only activated by the [LFCLKSTART](#) task.



## 4.9.3 Registers

| Base address | Domain      | Peripheral | Instance   | Secure mapping | DMA security | Description   | Configuration                |
|--------------|-------------|------------|------------|----------------|--------------|---------------|------------------------------|
| 0x50005000   | APPLICATION | CLOCK      | CLOCK : S  | US             | NA           | Clock control |                              |
| 0x40005000   |             |            | CLOCK : NS |                |              |               |                              |
| 0x41005000   | NETWORK     | CLOCK      | CLOCK      | NS             | NA           | Clock control | HFCLKCTRL reset value is 0x0 |

Table 25: Instances

| Register                  | Offset | Security | Description                                                                                                                                                                                       |
|---------------------------|--------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TASKS_HFCLKSTART          | 0x000  |          | Start HFCLK128M/HFCLK64M source as selected in HFCLKSRC                                                                                                                                           |
| TASKS_HFCLKSTOP           | 0x004  |          | Stop HFCLK128M/HFCLK64M source                                                                                                                                                                    |
| TASKS_LFCLKSTART          | 0x008  |          | Start LFCLK source as selected in LFCLKSRC                                                                                                                                                        |
| TASKS_LFCLKSTOP           | 0x00C  |          | Stop LFCLK source                                                                                                                                                                                 |
| TASKS_CAL                 | 0x010  |          | Start calibration of LFRC oscillator                                                                                                                                                              |
| TASKS_HFCLKAUDIOSTART     | 0x018  |          | Start HFCLKAUDIO source                                                                                                                                                                           |
| TASKS_HFCLKAUDIOSTOP      | 0x01C  |          | Stop HFCLKAUDIO source                                                                                                                                                                            |
| TASKS_HFCLK192MSTART      | 0x020  |          | Start HFCLK192M source as selected in HFCLK192MSRC                                                                                                                                                |
| TASKS_HFCLK192MSTOP       | 0x024  |          | Stop HFCLK192M source                                                                                                                                                                             |
| SUBSCRIBE_HFCLKSTART      | 0x080  |          | Subscribe configuration for task <a href="#">HFCLKSTART</a>                                                                                                                                       |
| SUBSCRIBE_HFCLKSTOP       | 0x084  |          | Subscribe configuration for task <a href="#">HFCLKSTOP</a>                                                                                                                                        |
| SUBSCRIBE_LFCLKSTART      | 0x088  |          | Subscribe configuration for task <a href="#">LFCLKSTART</a>                                                                                                                                       |
| SUBSCRIBE_LFCLKSTOP       | 0x08C  |          | Subscribe configuration for task <a href="#">LFCLKSTOP</a>                                                                                                                                        |
| SUBSCRIBE_CAL             | 0x090  |          | Subscribe configuration for task <a href="#">CAL</a>                                                                                                                                              |
| SUBSCRIBE_HFCLKAUDIOSTART | 0x098  |          | Subscribe configuration for task <a href="#">HFCLKAUDIOSTART</a>                                                                                                                                  |
| SUBSCRIBE_HFCLKAUDIOSTOP  | 0x09C  |          | Subscribe configuration for task <a href="#">HFCLKAUDIOSTOP</a>                                                                                                                                   |
| SUBSCRIBE_HFCLK192MSTART  | 0x0A0  |          | Subscribe configuration for task <a href="#">HFCLK192MSTART</a>                                                                                                                                   |
| SUBSCRIBE_HFCLK192MSTOP   | 0x0A4  |          | Subscribe configuration for task <a href="#">HFCLK192MSTOP</a>                                                                                                                                    |
| EVENTS_HFCLKSTARTED       | 0x100  |          | HFCLK128M/HFCLK64M source started                                                                                                                                                                 |
| EVENTS_LFCLKSTARTED       | 0x104  |          | LFCLK source started                                                                                                                                                                              |
| EVENTS_DONE               | 0x11C  |          | Calibration of LFRC oscillator complete event                                                                                                                                                     |
| EVENTS_HFCLKAUDIOSTARTED  | 0x120  |          | HFCLKAUDIO source started                                                                                                                                                                         |
| EVENTS_HFCLK192MSTARTED   | 0x124  |          | HFCLK192M source started                                                                                                                                                                          |
| PUBLISH_HFCLKSTARTED      | 0x180  |          | Publish configuration for event <a href="#">HFCLKSTARTED</a>                                                                                                                                      |
| PUBLISH_LFCLKSTARTED      | 0x184  |          | Publish configuration for event <a href="#">LFCLKSTARTED</a>                                                                                                                                      |
| PUBLISH_DONE              | 0x19C  |          | Publish configuration for event <a href="#">DONE</a>                                                                                                                                              |
| PUBLISH_HFCLKAUDIOSTARTED | 0x1A0  |          | Publish configuration for event <a href="#">HFCLKAUDIOSTARTED</a>                                                                                                                                 |
| PUBLISH_HFCLK192MSTARTED  | 0x1A4  |          | Publish configuration for event <a href="#">HFCLK192MSTARTED</a>                                                                                                                                  |
| INTEN                     | 0x300  |          | Enable or disable interrupt                                                                                                                                                                       |
| INTENSET                  | 0x304  |          | Enable interrupt                                                                                                                                                                                  |
| INTENCLR                  | 0x308  |          | Disable interrupt                                                                                                                                                                                 |
| INTPEND                   | 0x30C  |          | Pending interrupts                                                                                                                                                                                |
| HFCLKRUN                  | 0x408  |          | Status indicating that HFCLKSTART task has been triggered                                                                                                                                         |
| HFCLKSTAT                 | 0x40C  |          | Status indicating which HFCLK128M/HFCLK64M source is running<br><br>Note: Value of this register in any CLOCK instance reflects status only due to configurations/actions in that CLOCK instance. |
| LFCLKRUN                  | 0x414  |          | Status indicating that LFCLKSTART task has been triggered                                                                                                                                         |
| LFCLKSTAT                 | 0x418  |          | Status indicating which LFCLK source is running<br><br>Note: Value of this register in any CLOCK instance reflects status only due to configurations/actions in that CLOCK instance.              |
| LFCLKSRCCOPY              | 0x41C  |          | Copy of LFCLKSRC register, set when LFCLKSTART task was triggered                                                                                                                                 |

| Register             | Offset | Security | Description                                                                               |
|----------------------|--------|----------|-------------------------------------------------------------------------------------------|
| HFCLKAUDIORUN        | 0x450  |          | Status indicating that HFCLKAUDIOSTART task has been triggered                            |
| HFCLKAUDIOSTAT       | 0x454  |          | Status indicating which HFCLKAUDIO source is running                                      |
| HFCLK192MRUN         | 0x458  |          | Status indicating that HFCLK192MSTART task has been triggered                             |
| HFCLK192MSTAT        | 0x45C  |          | Status indicating which HFCLK192M source is running                                       |
| HFCLKSRC             | 0x514  |          | Clock source for HFCLK128M/HFCLK64M                                                       |
| LFCLKSRC             | 0x518  |          | Clock source for LFCLK                                                                    |
| HFCLKCTRL            | 0x558  |          | HFCLK128M frequency configuration                                                         |
| HFCLKAUDIO.FREQUENCY | 0x55C  |          | Audio PLL frequency in 11.176 MHz - 11.402 MHz or 12.165 MHz - 12.411 MHz frequency bands |
| HFCLKALWAYSRUN       | 0x570  |          | Automatic or manual control of HFCLK128M/HFCLK64M                                         |
| LFCLKALWAYSRUN       | 0x574  |          | Automatic or manual control of LFCLK                                                      |
| HFCLKAUDIOALWAYSRUN  | 0x57C  |          | Automatic or manual control of HFCLKAUDIO                                                 |
| HFCLK192MSRC         | 0x580  |          | Clock source for HFCLK192M                                                                |
| HFCLK192MALWAYSRUN   | 0x584  |          | Automatic or manual control of HFCLK192M                                                  |
| HFCLK192MCTRL        | 0x5B8  |          | HFCLK192M frequency configuration                                                         |

Table 26: Register overview

### 4.9.3.1 TASKS\_HFCLKSTART

Address offset: 0x000

Start HFCLK128M/HFCLK64M source as selected in HFCLKSRC

|                  |             |                  |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
|------------------|-------------|------------------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|
| Bit number       |             |                  |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| ID               |             |                  |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A |
| Reset 0x00000000 |             |                  |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| ID               | Acces Field | Value ID         | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| A                | W           | TASKS_HFCLKSTART |       | Start HFCLK128M/HFCLK64M source as selected in HFCLKSRC                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
|                  |             | Trigger          | 1     | Trigger task                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |

### 4.9.3.2 TASKS\_HFCLKSTOP

Address offset: 0x004

Stop HFCLK128M/HFCLK64M source

|                  |            |                 |          |                                                                                       |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
|------------------|------------|-----------------|----------|---------------------------------------------------------------------------------------|--|--|--|--------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|
| Bit number       |            |                 |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| ID               |            |                 |          |                                                                                       |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A |
| Reset 0x00000000 |            |                 |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| ID               | Acce Field |                 | Value ID | Value                                                                                 |  |  |  | Description                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| A                | W          | TASKS_HFCLKSTOP |          |                                                                                       |  |  |  | Stop HFCLK128M/HFCLK64M source |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
|                  |            | Trigger         |          | 1                                                                                     |  |  |  | Trigger task                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |

### 4.9.3.3 TASKS\_LFCLKSTART

Address offset: 0x008

Start LFCLK source as selected in LFCLKSRC

|                  |            |                  |          |   |       |              |             |                                            |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|------------------|----------|---|-------|--------------|-------------|--------------------------------------------|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                  |          |   |       |              |             |                                            |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |                  |          |   |       |              |             |                                            |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |
| Reset 0x00000000 |            |                  |          |   |       |              |             |                                            |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |                  | Value ID |   | Value |              | Description |                                            |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_LFCLKSTART |          |   |       |              |             | Start LFCLK source as selected in LFCLKSRC |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Trigger          |          | 1 |       | Trigger task |             |                                            |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

#### 4.9.3.4 TASKS\_LFCLKSTOP

Address offset: 0x00C

Stop LFCLK source

|                  |            |                 |          |   |       |                   |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-----------------|----------|---|-------|-------------------|-------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                 |          |   |       |                   |             |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |                 |          |   |       |                   |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | A |   |   |   |   |
| Reset 0x00000000 |            |                 |          |   |       |                   |             |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |                 | Value ID |   | Value |                   | Description |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_LFCLKSTOP |          |   |       | Stop LFCLK source |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Trigger         |          | 1 |       | Trigger task      |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

#### 4.9.3.5 TASKS\_CAL

Address offset: 0x010

Start calibration of LFRC oscillator

Do not calibrate if the clock source is LFULP

|                  |            |           |       |    |    |    |    |    |    |    |    |    |                                               |              |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-----------|-------|----|----|----|----|----|----|----|----|----|-----------------------------------------------|--------------|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |           | 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21                                            | 20           | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |           |       |    |    |    |    |    |    |    |    |    |                                               |              |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |
| Reset 0x00000000 |            |           | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                                             | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID  | Value |    |    |    |    |    |    |    |    |    | Description                                   |              |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_CAL |       |    |    |    |    |    |    |    |    |    | Start calibration of LFRC oscillator          |              |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |           |       |    |    |    |    |    |    |    |    |    | Do not calibrate if the clock source is LFULP |              |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Trigger   | 1     |    |    |    |    |    |    |    |    |    |                                               | Trigger task |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 4.9.3.6 TASKS\_HFCLKAUDIOSTART

Address offset: 0x018

Start HFCLKAUDIO source

|                  |            |                       |  |  |          |   |  |  |       |    |    |    |             |                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-----------------------|--|--|----------|---|--|--|-------|----|----|----|-------------|-------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                       |  |  |          |   |  |  |       | 31 | 30 | 29 | 28          | 27                      | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |                       |  |  |          |   |  |  |       |    |    |    |             |                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |   |
| Reset 0x00000000 |            |                       |  |  |          |   |  |  |       | 0  | 0  | 0  | 0           | 0                       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |                       |  |  | Value ID |   |  |  | Value |    |    |    | Description |                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_HFCLKAUDIOSTART |  |  |          |   |  |  |       |    |    |    |             | Start HFCLKAUDIO source |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Trigger               |  |  |          | 1 |  |  |       |    |    |    |             | Trigger task            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 4.9.3.7 TASKS\_HFCLKAUDIOSTOP

Address offset: 0x01C

Stop HFCLKAUDIO source

|                  |            |                      |          |   |       |              |             |                        |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------------------|----------|---|-------|--------------|-------------|------------------------|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                      |          |   |       |              |             |                        |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |                      |          |   |       |              |             |                        |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |
| Reset 0x00000000 |            |                      |          |   |       |              |             |                        |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |                      | Value ID |   | Value |              | Description |                        |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_HFCLKAUDIOSTOP |          |   |       |              |             | Stop HFCLKAUDIO source |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Trigger              |          | 1 |       | Trigger task |             |                        |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 4.9.3.8 TASKS\_HFCLK192MSTART

Address offset: 0x020

Start HFCLK192M source as selected in HFCLK192MSRC

|                  |            |                      |  |  |          |   |  |  |       |    |    |    |             |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------------------|--|--|----------|---|--|--|-------|----|----|----|-------------|----------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                      |  |  |          |   |  |  |       | 31 | 30 | 29 | 28          | 27                                                 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |                      |  |  |          |   |  |  |       | A  |    |    |             |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |                      |  |  |          |   |  |  |       | 0  | 0  | 0  | 0           | 0                                                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |                      |  |  | Value ID |   |  |  | Value |    |    |    | Description |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_HFCLK192MSTART |  |  |          |   |  |  |       |    |    |    |             | Start HFCLK192M source as selected in HFCLK192MSRC |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Trigger              |  |  |          | 1 |  |  |       |    |    |    |             | Trigger task                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 4.9.3.9 TASKS\_HFCLK192MSTOP

Address offset: 0x024

Stop HFCLK192M source

|                  |            |                     |  |  |          |   |  |  |       |    |    |    |             |                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|---------------------|--|--|----------|---|--|--|-------|----|----|----|-------------|-----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                     |  |  |          |   |  |  |       | 31 | 30 | 29 | 28          | 27                    | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |                     |  |  |          |   |  |  |       |    |    |    |             |                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |
| Reset 0x00000000 |            |                     |  |  |          |   |  |  |       | 0  | 0  | 0  | 0           | 0                     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |                     |  |  | Value ID |   |  |  | Value |    |    |    | Description |                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_HFCLK192MSTOP |  |  |          |   |  |  |       |    |    |    |             | Stop HFCLK192M source |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Trigger             |  |  |          | 1 |  |  |       |    |    |    |             | Trigger task          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 4.9.3.10 SUBSCRIBE\_HFCLKSTART

Address offset: 0x080

Subscribe configuration for task HFCLKSTART

|                  |            |          |  |          |   |  |       |                      |  |             |                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|--|----------|---|--|-------|----------------------|--|-------------|----------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |  |          |   |  |       |                      |  | 31          | 30                                                             | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |          |  |          |   |  |       |                      |  | B           |                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  |    |    |    |   |   |   |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |  |          |   |  |       |                      |  | 0           | 0                                                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |          |  | Value ID |   |  | Value |                      |  | Description |                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | CHIDX    |  |          |   |  |       | [255..0]             |  |             | Channel that task <a href="#">HFCLKSTART</a> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW         | EN       |  |          |   |  |       |                      |  |             |                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled |  |          | 0 |  |       | Disable subscription |  |             |                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  |  |          | 1 |  |       | Enable subscription  |  |             |                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 4.9.3.11 SUBSCRIBE\_HFCLKSTOP

Address offset: 0x084

Subscribe configuration for task HFCLKSTOP

|                  |            |          |          |    |                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|----|---------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          | 31       | 30 | 29                                                            | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |          | B        |    |                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          | 0        | 0  | 0                                                             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce Field | Value ID | Value    |    | Description                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] |    | Channel that task <a href="#">HFCLKSTOP</a> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |    |                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        |    | Disable subscription                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        |    | Enable subscription                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 4.9.3.12 SUBSCRIBE\_LFCLKSTART

Address offset: 0x088

Subscribe configuration for task [LFCLKSTART](#)

|                  |            |  |          |  |          |  |                                                       |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|--|----------|--|-------------------------------------------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          |  |          |  |                                                       |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |  |          |  |          |  |                                                       |  |  | B  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  |    |    |    |   |   |   |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |          |  |          |  |                                                       |  |  | 0  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID |  | Value    |  | Description                                           |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          |  | [255..0] |  | Channel that task <b>LFCLKSTART</b> will subscribe to |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |  |          |  |                                                       |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled |  | 0        |  | Disable subscription                                  |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  |  | 1        |  | Enable subscription                                   |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 4.9.3.13 SUBSCRIBE\_LFCLKSTOP

Address offset: 0x08C

Subscribe configuration for task [LFCLKSTOP](#)

|                  |            |          |                                                                         |    |    |    |                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
|------------------|------------|----------|-------------------------------------------------------------------------|----|----|----|---------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|-----------------|---|---|---|---|---|---|---|--|--|--|--|
| Bit number       |            |          | 31                                                                      | 30 | 29 | 28 | 27                                                            | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |
| ID               |            |          | B                                                                       |    |    |    |                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A A A A A A A A |   |   |   |   |   |   |   |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |    |    |    |                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                   |    |    |    | Description                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                |    |    |    | Channel that task <a href="#">LFCLKSTOP</a> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
| B                | RW EN      |          |                                                                         |    |    |    |                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | Disabled | 0                                                                       |    |    |    | Disable subscription                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | Enabled  | 1                                                                       |    |    |    | Enable subscription                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |

#### 4.9.3.14 SUBSCRIBE\_CAL

Address offset: 0x090

Subscribe configuration for task [CAL](#)

Do not calibrate if the clock source is LFULP

|                  |            |          |                                                                         |    |    |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
|------------------|------------|----------|-------------------------------------------------------------------------|----|----|----|------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|-----------------|---|---|---|---|---|---|---|--|--|--|--|
| Bit number       |            |          | 31                                                                      | 30 | 29 | 28 | 27                                                   | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |
| ID               |            |          | B                                                                       |    |    |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A A A A A A A A |   |   |   |   |   |   |   |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |    |    |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                   |    |    |    | Description                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                |    |    |    | Channel that task <span>CAL</span> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
| B                | RW EN      |          |                                                                         |    |    |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | Disabled | 0                                                                       |    |    |    | Disable subscription                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | Enabled  | 1                                                                       |    |    |    | Enable subscription                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |

## Subscribe configuration for task [HFCLKAUDIOSTART](#)

|                  |            |  |  |  |          |  |  |  |          |    |    |    |                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|--|--|----------|--|--|--|----------|----|----|----|---------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |  |  |          |  |  |  |          | 31 | 30 | 29 | 28                                                                  | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |
| ID               |            |  |  |  |          |  |  |  |          | B  |    |    |                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  |    |    |    |   |   |   |   |   |   | A | A | A | A | A | A | A |   |
| Reset 0x00000000 |            |  |  |  |          |  |  |  |          | 0  | 0  | 0  | 0                                                                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  |  |  | Value ID |  |  |  | Value    |    |    |    | Description                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |  |  |          |  |  |  | [255..0] |    |    |    | Channel that task <a href="#">HFCLKAUDIOSTART</a> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |  |  |          |  |  |  |          |    |    |    |                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  |  |  | Disabled |  |  |  | 0        |    |    |    | Disable subscription                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  |  |  | Enabled  |  |  |  | 1        |    |    |    | Enable subscription                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### Subscribe configuration for task `HFCLKAUDIOSTOP`

|                  |            |  |          |          |    |                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|----------|----|--------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31       | 30 | 29                                                                 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |  |          | B        |    |                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   | A |   |   |   |   |   |   |   |   |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |          | 0        |    |                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID | Value    |    | Description                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          | [255..0] |    | Channel that task <a href="#">HFCLKAUDIOSTOP</a> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |          |    |                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled | 0        |    | Disable subscription                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  | 1        |    | Enable subscription                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

Subscribe configuration for task [HFCLK192MSTART](#)

|            |  |  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     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|------------|--|--|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------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| Bit number |  |  | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               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|                  |            |                     |       |                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|---------------------|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                     |       | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |                     |       | A                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |                     |       | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID            | Value | Description          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | EVENTS_LFCLKSTARTED |       | LFCLK source started |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | NotGenerated        | 0     | Event not generated  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Generated           | 1     | Event generated      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 4.9.3.21 EVENTS\_DONE

Address offset: 0x11C

Calibration of LFRC oscillator complete event

|                  |            |              |       |                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------------|-------|-----------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |              |       | 31                                            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |              |       | A                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |              |       | 0                                             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID     | Value | Description                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | EVENTS_DONE  |       | Calibration of LFRC oscillator complete event |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | NotGenerated | 0     | Event not generated                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Generated    | 1     | Event generated                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

#### 4.9.3.22 EVENTS\_HFCLKAUDIOSTARTED

Address offset: 0x120

HFCLKAUDIO source started

|                  |            |                          |       |                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|------------------|------------|--------------------------|-------|---------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|---|
| Bit number       |            |                          |       | 31                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |   |
| ID               |            |                          |       |                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | A |
| Reset 0x00000000 |            |                          |       | 0                         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |   |
| ID               | Acce Field | Value ID                 | Value | Description               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
| A                | RW         | EVENTS_HFCLKAUDIOSTARTED |       | HFCLKAUDIO source started |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | NotGenerated             | 0     | Event not generated       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | Generated                | 1     | Event generated           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |

#### 4.9.3.23 EVENTS\_HFCLK192MSTARTED

Address offset: 0x124

HFCLK192M source started

|                  |            |                         |       |                          |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-------------------------|-------|--------------------------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                         | 31    | 30                       | 29          | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |                         |       |                          |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |
| Reset 0x00000000 |            |                         | 0     | 0                        | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID                | Value |                          | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | EVENTS_HFCLK192MSTARTED |       | HFCLK192M source started |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | NotGenerated            | 0     | Event not generated      |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Generated               | 1     | Event generated          |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 4.9.3.24 PUBLISH\_HFCLKSTARTED

Address offset: 0x180

Publish configuration for event [HFCLKSTARTED](#)

|                  |            |  |          |          |    |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|----------|----|------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31       | 30 | 29                                                               | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |  |          | B        |    |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   |   |   |   |   |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |          | 0        |    |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID | Value    |    | Description                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          | [255..0] |    | Channel that event <a href="#">HFCLKSTARTED</a> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |          |    |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled | 0        |    | Disable publishing                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  | 1        |    | Enable publishing                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 4.9.3.25 PUBLISH\_LFCLKSTARTED

Address offset: 0x184

Publish configuration for event [LFCLKSTARTED](#)

|                  |            |          |  |          |          |       |                                                         |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|--|----------|----------|-------|---------------------------------------------------------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |  | 31       | 30       | 29    | 28                                                      | 27          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |          |  | B        |          |       |                                                         |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   |   |   |   |   |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |          |  | 0        |          |       |                                                         |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |          |  | Value ID |          | Value |                                                         | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | CHIDX    |  |          | [255..0] |       | Channel that event <b>LFCLKSTARTED</b> will publish to. |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW         | EN       |  |          |          |       |                                                         |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled |  |          | 0        |       | Disable publishing                                      |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  |  |          | 1        |       | Enable publishing                                       |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 4.9.3.26 PUBLISH\_DONE

Address offset: 0x19C





### Enable interrupt

## Disable interrupt

| Bit number       |      |                   | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |
|------------------|------|-------------------|---------------------------------------------------------------------------------------|-------|----------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|-----|--|--|
| ID               |      |                   |                                                                                       |       |                                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | E D C |  |  | B A |  |  |
| Reset 0x00000000 |      |                   | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |       |                                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |
| ID               | Acce | Field             | Value ID                                                                              | Value | Description                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |
| A                | RW   | HFCLKSTARTED      |                                                                                       |       | Write '1' to disable interrupt for event <a href="#">HFCLKSTARTED</a>      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |
|                  |      |                   | Clear                                                                                 | 1     | Disable                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |
|                  |      |                   | Disabled                                                                              | 0     | Read: Disabled                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |
|                  |      |                   | Enabled                                                                               | 1     | Read: Enabled                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |
| B                | RW   | LFCLKSTARTED      |                                                                                       |       | Write '1' to disable interrupt for event <a href="#">LFCLKSTARTED</a>      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |
|                  |      |                   | Clear                                                                                 | 1     | Disable                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |
|                  |      |                   | Disabled                                                                              | 0     | Read: Disabled                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |
|                  |      |                   | Enabled                                                                               | 1     | Read: Enabled                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |
| C                | RW   | DONE              |                                                                                       |       | Write '1' to disable interrupt for event <a href="#">DONE</a>              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |
|                  |      |                   | Clear                                                                                 | 1     | Disable                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |
|                  |      |                   | Disabled                                                                              | 0     | Read: Disabled                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |
|                  |      |                   | Enabled                                                                               | 1     | Read: Enabled                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |
| D                | RW   | HFCLKAUDIOSTARTED |                                                                                       |       | Write '1' to disable interrupt for event <a href="#">HFCLKAUDIOSTARTED</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |
|                  |      |                   | Clear                                                                                 | 1     | Disable                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |
|                  |      |                   | Disabled                                                                              | 0     | Read: Disabled                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |
|                  |      |                   | Enabled                                                                               | 1     | Read: Enabled                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |
| E                | RW   | HFCLK192MSTARTED  |                                                                                       |       | Write '1' to disable interrupt for event <a href="#">HFCLK192MSTARTED</a>  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |
|                  |      |                   | Clear                                                                                 | 1     | Disable                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |
|                  |      |                   | Disabled                                                                              | 0     | Read: Disabled                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |
|                  |      |                   | Enabled                                                                               | 1     | Read: Enabled                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |

### 4.9.3.32 INTPEND

Address offset: 0x30C

Pending interrupts

| Bit number       |      |                   | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |
|------------------|------|-------------------|---------------------------------------------------------------------------------------|-------|------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|-----|--|--|
| ID               |      |                   |                                                                                       |       |                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | E D C |  |  | B A |  |  |
| Reset 0x00000000 |      |                   | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |       |                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |
| ID               | Acce | Field             | Value ID                                                                              | Value | Description                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |
| A                | R    | HFCLKSTARTED      |                                                                                       |       | Read pending status of interrupt for event <a href="#">HFCLKSTARTED</a>      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |
|                  |      |                   | NotPending                                                                            | 0     | Read: Not pending                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |
|                  |      |                   | Pending                                                                               | 1     | Read: Pending                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |
| B                | R    | LFCLKSTARTED      |                                                                                       |       | Read pending status of interrupt for event <a href="#">LFCLKSTARTED</a>      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |
|                  |      |                   | NotPending                                                                            | 0     | Read: Not pending                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |
|                  |      |                   | Pending                                                                               | 1     | Read: Pending                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |
| C                | R    | DONE              |                                                                                       |       | Read pending status of interrupt for event <a href="#">DONE</a>              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |
|                  |      |                   | NotPending                                                                            | 0     | Read: Not pending                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |
|                  |      |                   | Pending                                                                               | 1     | Read: Pending                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |
| D                | R    | HFCLKAUDIOSTARTED |                                                                                       |       | Read pending status of interrupt for event <a href="#">HFCLKAUDIOSTARTED</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |
|                  |      |                   | NotPending                                                                            | 0     | Read: Not pending                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |
|                  |      |                   | Pending                                                                               | 1     | Read: Pending                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |
| E                | R    | HFCLK192MSTARTED  |                                                                                       |       | Read pending status of interrupt for event <a href="#">HFCLK192MSTARTED</a>  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |
|                  |      |                   | NotPending                                                                            | 0     | Read: Not pending                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |
|                  |      |                   | Pending                                                                               | 1     | Read: Pending                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |     |  |  |

### 4.9.3.33 HFCLKRUN

Address offset: 0x408

Status indicating that HFCLKSTART task has been triggered

|                  |      |        |              |                                                                                       |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|--------|--------------|---------------------------------------------------------------------------------------|----------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |        |              | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |        |              | A                                                                                     |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |        |              | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field  | Value ID     | Value                                                                                 | Description                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | R    | STATUS |              |                                                                                       | HFCLKSTART task triggered or not |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |        | NotTriggered | 0                                                                                     | Task not triggered               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |        | Triggered    | 1                                                                                     | Task triggered                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 4.9.3.34 HFCLKSTAT

Address offset: 0x40C

Status indicating which HFCLK128M/HFCLK64M source is running

Note: Value of this register in any CLOCK instance reflects status only due to configurations/actions in that CLOCK instance.

| Bit number       |      |               | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|------------------|------|---------------|---------------------------------------------------------------------------------------|-------|------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|
| ID               |      |               | C                                                                                     |       |                                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  | B |  |  |  |  |  |  |  | A |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |               | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |       |                                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
| ID               | Acce | Field         | Value ID                                                                              | Value | Description                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
| A                | R    | SRC           |                                                                                       |       | Active clock source                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |      |               | HFINT                                                                                 | 0     | Clock source: HFINT - 128 MHz on-chip oscillator                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |      |               | HFXO                                                                                  | 1     | Clock source: HFXO - 128 MHz clock derived from external 32 MHz crystal oscillator |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
| B                | R    | ALWAYSRUNNING |                                                                                       |       | ALWAYSRUN activated                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |      |               | NotRunning                                                                            | 0     | Automatic clock control enabled                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |      |               | Running                                                                               | 1     | Oscillator is always running                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
| C                | R    | STATE         |                                                                                       |       | HFCLK state                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |      |               | NotRunning                                                                            | 0     | HFCLK not running                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |      |               | Running                                                                               | 1     | HFCLK running                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |

### 4.9.3.35 LFCLKRUN

Address offset: 0x414

Status indicating that LFCLKSTART task has been triggered

|                  |      |        |              |                                                                                       |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|--------|--------------|---------------------------------------------------------------------------------------|----------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |        |              | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |        |              | A                                                                                     |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |        |              | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field  | Value ID     | Value                                                                                 | Description                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | R    | STATUS |              |                                                                                       | LFCLKSTART task triggered or not |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |        | NotTriggered | 0                                                                                     | Task not triggered               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |        | Triggered    | 1                                                                                     | Task triggered                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 4.9.3.36 LFCLKSTAT

Address offset: 0x418

Status indicating which LFCLK source is running

Note: Value of this register in any CLOCK instance reflects status only due to configurations/actions in that CLOCK instance.

| Bit number       |      |               | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |
|------------------|------|---------------|---------------------------------------------------------------------------------------|-------|------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|---|--|---|--|
| ID               |      |               | C                                                                                     |       |                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | B |  |  |  | A |  | A |  |
| Reset 0x00000000 |      |               | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |       |                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |
| ID               | Acce | Field         | Value ID                                                                              | Value | Description                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |
| A                | R    | SRC           |                                                                                       |       | Active clock source                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |
|                  |      |               | LFULP                                                                                 | 0     | 32.768 kHz ultra-low power RC oscillator |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |
|                  |      |               | LFRC                                                                                  | 1     | 32.768 kHz RC oscillator                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |
|                  |      |               | LFXO                                                                                  | 2     | 32.768 kHz crystal oscillator            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |
|                  |      |               | LFSYNT                                                                                | 3     | 32.768 kHz synthesized from HFCLK        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |
| B                | R    | ALWAYSRUNNING |                                                                                       |       | ALWAYSRUN activated                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |
|                  |      |               | NotRunning                                                                            | 0     | Automatic clock control enabled          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |
|                  |      |               | Running                                                                               | 1     | Oscillator is always running             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |
| C                | R    | STATE         |                                                                                       |       | LFCLK state                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |
|                  |      |               | NotRunning                                                                            | 0     | LFCLK not running                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |
|                  |      |               | Running                                                                               | 1     | LFCLK running                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |

#### 4.9.3.37 LFCLKSRCCOPY

Address offset: 0x41C

Copy of LFCLKSRC register, set when LFCLKSTART task was triggered

|                  |  |  |  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| Bit number       |  |  |  | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      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| ID               |  |  |  | A A                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        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| Reset 0x00000001 |  |  |  | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 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#### 4.9.3.38 HFCLKAUDIORUN

Address offset: 0x450

Status indicating that HFCLKAUDIOSTART task has been triggered

|                  |      |        |              |                                                                                       |                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
|------------------|------|--------|--------------|---------------------------------------------------------------------------------------|---------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|
| Bit number       |      |        |              | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| ID               |      |        |              |                                                                                       |                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A |
| Reset 0x00000000 |      |        |              | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0           |                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| ID               | Acce | Field  | Value ID     | Value                                                                                 | Description                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| A                | R    | STATUS |              |                                                                                       | HFCLKAUDIOSTART task triggered or not |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
|                  |      |        | NotTriggered | 0                                                                                     | Task not triggered                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
|                  |      |        | Triggered    | 1                                                                                     | Task triggered                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |

#### 4.9.3.39 HFCLKAUDIOSTAT

Address offset: 0x454

Status indicating which HFCLKAUDIO source is running

| Bit number       |            |               | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|---------------|---------------------------------------------------------------------------------------|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |            |               | C                                                                                     |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  | B |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |               | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID      | Value                                                                                 | Description                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | R          | ALWAYSRUNNING |                                                                                       | ALWAYSRUN activated             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | NotRunning    | 0                                                                                     | Automatic clock control enabled |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Running       | 1                                                                                     | Oscillator is always running    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | R          | STATE         |                                                                                       | HFCLKAUDIO state                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | NotRunning    | 0                                                                                     | HFCLKAUDIO not running          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Running       | 1                                                                                     | HFCLKAUDIO running              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

#### 4.9.3.40 HFCLK192MRUN

Address offset: 0x458

Status indicating that HFCLK192MSTART task has been triggered

|                  |            |              |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|--------------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |              |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |              |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |              |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID     | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | R          | STATUS       |       | HFCLK192MSTART task triggered or not                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | NotTriggered | 0     | Task not triggered                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Triggered    | 1     | Task triggered                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

#### 4.9.3.41 HFCLK192MSTAT

Address offset: 0x45C

Status indicating which HFCLK192M source is running

|                  |            |               |                                                                                       |                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |
|------------------|------------|---------------|---------------------------------------------------------------------------------------|----------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|
| Bit number       |            |               | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |
| ID               |            |               | C                                                                                     |                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  | B |  |  |  |  |  |  |  |  |  | A |  |  |  |  |  |
| Reset 0x00000000 |            |               | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |
| ID               | Acce Field | Value ID      | Value                                                                                 | Description                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |
| A                | R          | SRC           |                                                                                       | Active clock source                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |
|                  |            | HFINT         | 0                                                                                     | Clock source: HFINT - on-chip oscillator                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |
|                  |            | HFXO          | 1                                                                                     | Clock source: HFXO - derived from external 32 MHz crystal oscillator |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |
| B                | R          | ALWAYSRUNNING |                                                                                       | ALWAYSRUN activated                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |
|                  |            | NotRunning    | 0                                                                                     | Automatic clock control enabled                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |
|                  |            | Running       | 1                                                                                     | Oscillator is always running                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |
| C                | R          | STATE         |                                                                                       | HFCLK192M state                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |
|                  |            | NotRunning    | 0                                                                                     | HFCLK192M not running                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |
|                  |            | Running       | 1                                                                                     | HFCLK192M running                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |

#### 4.9.3.42 HFCLKSRC

Address offset: 0x514

Clock source for HFCLK128M/HFCLK64M

|                  |            |          |       |                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|------------------|------------|----------|-------|-------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|---|
| Bit number       |            |          |       | 31                                                          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |   |
| ID               |            |          |       |                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  | A |
| Reset 0x00000001 |            |          |       | 0                                                           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |  |  |  |   |
| ID               | Acce Field | Value ID | Value | Description                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
| A                | RW SRC     |          |       | Select which HFCLK source is started by the HFCLKSTART task |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|                  |            | HFINT    | 0     | HFCLKSTART task starts HFINT oscillator                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|                  |            | HFXO     | 1     | HFCLKSTART task starts HFXO oscillator                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |

#### 4.9.3.43 LFCLKSRC

Address offset: 0x518

Clock source for LFCLK

|                  |      |       |        |    |                                                             |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |   |   |
|------------------|------|-------|--------|----|-------------------------------------------------------------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|---|---|
| Bit number       |      |       |        | 31 | 30                                                          | 29          | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |   |   |
| ID               |      |       |        |    |                                                             |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  | A | A |
| Reset 0x00000001 |      |       |        | 0  | 0                                                           | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |  |  |   |   |
| ID               | Acce | Field | Value  | ID | Value                                                       | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |   |   |
| A                | RW   | SRC   |        |    | Select which LFCLK source is started by the LFCLKSTART task |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |   |   |
|                  |      |       | LFULP  | 0  | 32.768 kHz ultra-low power RC oscillator                    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |   |   |
|                  |      |       | LFRC   | 1  | 32.768 kHz RC oscillator                                    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |   |   |
|                  |      |       | LFXO   | 2  | 32.768 kHz crystal oscillator                               |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |   |   |
|                  |      |       | LFSYNT | 3  | 32.768 kHz synthesized from HFCLK                           |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |   |   |

#### 4.9.3.44 HFCLKCTRL

Address offset: 0x558

HFCLK128M frequency configuration

Not present in the CLOCK instance of the network core

|                  |            |      |          |  |       |  |                           |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|------|----------|--|-------|--|---------------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |      |          |  |       |  |                           |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |      |          |  |       |  |                           |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |
| Reset 0x00000001 |            |      |          |  |       |  |                           |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| ID               | Acce Field |      | Value ID |  | Value |  | Description               |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | HCLK |          |  |       |  | High frequency clock HCLK |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |      | Div1     |  | 0     |  | Divide HFCLK by 1         |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |      | Div2     |  | 1     |  | Divide HFCLK by 2         |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

#### 4.9.3.45 HFCLKAUDIO.FREQUENCY

Address offset: 0x55C

Audio PLL frequency in 11.176 MHz - 11.402 MHz or 12.165 MHz - 12.411 MHz frequency bands

Not present in the CLOCK instance of the network core

|                  |            |           |       |    |    |    |    |    |    |    |    |    |                   |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-----------|-------|----|----|----|----|----|----|----|----|----|-------------------|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |           | 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21                | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |           |       |    |    |    |    |    |    |    |    |    |                   |    |    |    |    |    | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00009BAE |            |           | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 1  | 1  | 0  | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |   |
| ID               | Acce Field | Value ID  | Value |    |    |    |    |    |    |    |    |    | Description       |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | FREQUENCY |       |    |    |    |    |    |    |    |    |    | Frequency         |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |           |       |    |    |    |    |    |    |    |    |    | 0: 10.666 MHz     |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |           |       |    |    |    |    |    |    |    |    |    | 65535: 13.333 MHz |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

#### 4.9.3.46 HFCLKALWAYSRUN

Address offset: 0x570

Automatic or manual control of HFCLK128M/HFCLK64M

The AlwaysRun setting will ensure the clock source is always running, independent of the automatic clock request system.

This setting is activated by triggering the HFCLKSTART task.

|                  |            |           |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|-----------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |           |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |           |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |           |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID  | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | R          | ALWAYSRUN |       | Ensure clock is always running                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Automatic | 0     | Use automatic clock control                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | AlwaysRun | 1     | Ensure clock is always running                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

#### 4.9.3.47 LFCLKALWAYSRUN

Address offset: 0x574

Automatic or manual control of LFCLK

The AlwaysRun setting will ensure the clock source is always running, independent of the automatic clock request system.

This setting is activated by triggering the LFCLKSTART task.

|                  |      |           |           |    |       |                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|------------------|------|-----------|-----------|----|-------|--------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|--|
| Bit number       |      |           |           | 31 | 30    | 29                             | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |
| ID               |      |           |           | A  |       |                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| Reset 0x00000000 |      |           |           | 0  | 0     | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |  |
| ID               | Acce | Field     | Value     | ID | Value | Description                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| A                | R    | ALWAYSRUN |           |    |       | Ensure clock is always running |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |      |           | Automatic | 0  |       | Use automatic clock control    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |      |           | AlwaysRun | 1  |       | Ensure clock is always running |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |

#### 4.9.3.48 HFCLKAUDIOALWAYSRUN

Address offset: 0x57C

Automatic or manual control of HFCLKAUDIO

The AlwaysRun setting will ensure the clock source is always running, independent of the automatic clock request system.

This setting is activated by triggering the HFCLKAUDIOSTART task.



|                  |            |           |          |           |       |                                |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-----------|----------|-----------|-------|--------------------------------|-------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |           |          |           |       |                                |             |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |           |          |           |       |                                |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |   |
| Reset 0x00000000 |            |           |          |           |       |                                |             |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |           | Value ID |           | Value |                                | Description |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | R          | ALWAYSRUN |          |           |       | Ensure clock is always running |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |           |          | Automatic | 0     | Use automatic clock control    |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |           |          | AlwaysRun | 1     | Ensure clock is always running |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 4.9.3.49 HFCLK192MSRC

Address offset: 0x580

Clock source for HFCLK192M

|                  |            |          |       |    |                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |
|------------------|------------|----------|-------|----|---------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|---|--|
| Bit number       |            |          | 31    | 30 | 29                                                                  | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |   |  |
| ID               |            |          |       |    |                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  | A |  |
| Reset 0x00000001 |            |          | 0     | 0  | 0                                                                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |  |  |  |   |  |
| ID               | Acce Field | Value ID | Value |    | Description                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |
| A                | RW         | SRC      |       |    | Select which HFCLK192M source is started by the HFCLK192MSTART task |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |
|                  |            |          | HFINT | 0  | HFCLK192MSTART task starts HFINT oscillator                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |
|                  |            |          | HFXO  | 1  | HFCLK192MSTART task starts HFXO oscillator                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |

#### 4.9.3.50 HFCLK192MALWAYSRUN

Address offset: 0x584

Automatic or manual control of HFCLK192M

The AlwaysRun setting will ensure the clock source is always running, independent of the automatic clock request system.

This setting is activated by triggering the HFCLK192MSTART task.

|                  |            |           |       |                                |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-----------|-------|--------------------------------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |           | 31    | 30                             | 29          | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |           |       |                                |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |
| Reset 0x00000000 |            |           | 0     | 0                              | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID  | Value |                                | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | R          | ALWAYSRUN |       | Ensure clock is always running |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Automatic | 0     | Use automatic clock control    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | AlwaysRun | 1     | Ensure clock is always running |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 4.9.3.51 HFCLK192MCTRL

Address offset: 0x5B8

HFCLK192M frequency configuration

|                  |            |          |       |                               |             |                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|-------|-------------------------------|-------------|-----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          | 31    | 30                            | 29          | 28                    | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |          | A     |                               |             |                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000002 |            |          | 0     |                               |             |                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| ID               | Acce Field | Value ID | Value |                               | Description |                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | HCLK192M |       | High frequency clock HCLK192M |             |                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Div1     |       | 0                             |             | Divide HFCLK192M by 1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Div2     |       | 1                             |             | Divide HFCLK192M by 2 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Div4     |       | 2                             |             | Divide HFCLK192M by 4 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

## 4.9.4 Electrical specification

### 4.9.4.1 128 MHz clock source (HFCLK128M)

| Symbol                      | Description                                               | Min. | Typ. | Max. | Units |
|-----------------------------|-----------------------------------------------------------|------|------|------|-------|
| $f_{\text{NOM\_HFCLK128M}}$ | Nominal output frequency                                  |      | 128  |      | MHz   |
| $f_{\text{TOL\_HFINT128M}}$ | Frequency tolerance when running from internal oscillator | ..   | ..   | ..   | %     |
| $f_{\text{TOL\_HFXO128M}}$  | Frequency tolerance when running from crystal oscillator  | ..   | ..   | ..   | %     |

### 4.9.4.2 64 MHz clock source (HFCLK64M)

| Symbol                     | Description                                               | Min. | Typ. | Max. | Units |
|----------------------------|-----------------------------------------------------------|------|------|------|-------|
| $f_{\text{NOM\_HFCLK64M}}$ | Nominal output frequency                                  |      | 64   |      | MHz   |
| $f_{\text{TOL\_HFINT64M}}$ | Frequency tolerance when running from internal oscillator | ..   | ..   | ..   | %     |
| $f_{\text{TOL\_HFXO64M}}$  | Frequency tolerance when running from crystal oscillator  | ..   | ..   | ..   | %     |

### 4.9.4.3 192 MHz clock source (HFCLK192M)

| Symbol                      | Description                                               | Min. | Typ. | Max. | Units |
|-----------------------------|-----------------------------------------------------------|------|------|------|-------|
| $f_{\text{NOM\_HFCLK192M}}$ | Nominal output frequency                                  |      | 192  |      | MHz   |
| $f_{\text{TOL\_HFINT192M}}$ | Frequency tolerance when running from internal oscillator | ..   | ..   | ..   | %     |
| $f_{\text{TOL\_HFXO192M}}$  | Frequency tolerance when running from crystal oscillator  | ..   | ..   | ..   | %     |

### 4.9.4.4 Audio clock source (HFCLKAUDIO)

| Symbol                       | Description                                              | Min. | Typ.                   | Max. | Units |
|------------------------------|----------------------------------------------------------|------|------------------------|------|-------|
| $f_{\text{NOM\_HFCLKAUDIO}}$ | Nominal output frequency                                 |      | 11.289<br>or<br>12.288 |      | MHz   |
| $f_{\text{TOL\_HFXOAUDIO}}$  | Frequency tolerance when running from crystal oscillator | ..   | ..                     | ..   | %     |

### 4.9.4.5 32 MHz crystal oscillator (HFXO)

| Symbol                          | Description                                                                                        | Min. | Typ. | Max. | Units         |
|---------------------------------|----------------------------------------------------------------------------------------------------|------|------|------|---------------|
| $f_{\text{XTAL\_HFXO}}$         | External crystal frequency                                                                         | ..   | ..   | ..   | MHz           |
| $f_{\text{TOL\_HFXO}}$          | Frequency tolerance requirement for 2.4 GHz proprietary radio applications                         | ..   | ..   | ..   | ppm           |
| $f_{\text{TOL\_HFXO\_BLE}}$     | Frequency tolerance requirement, Bluetooth low energy applications, packet length $\leq 200$ bytes | ..   | ..   | ..   | ppm           |
| $f_{\text{TOL\_HFXO\_BLE\_LP}}$ | Frequency tolerance requirement, Bluetooth low energy applications, packet length $> 200$ bytes    | ..   | ..   | ..   | ppm           |
| $C_{\text{L\_HFXO}}$            | Load capacitance                                                                                   | ..   | ..   | ..   | pF            |
| $C_{\text{0\_HFXO}}$            | Shunt capacitance                                                                                  | ..   | ..   | ..   | pF            |
| $R_{\text{S\_HFXO\_7PF}}$       | Equivalent series resistance $3 \text{ pF} < C_0 \leq 7 \text{ pF}$                                | ..   | ..   | ..   | $\Omega$      |
| $R_{\text{S\_HFXO\_3PF}}$       | Equivalent series resistance $C_0 \leq 3 \text{ pF}$                                               | ..   | ..   | ..   | $\Omega$      |
| $P_{\text{D\_HFXO}}$            | Drive level                                                                                        | ..   | ..   | ..   | $\mu\text{W}$ |
| $C_{\text{PIN\_HFXO}}$          | Input capacitance XC1 and XC2                                                                      | ..   | ..   | ..   | pF            |
| $I_{\text{STBY\_X32M}}$         | Core standby current for various crystals                                                          | ..   | ..   | ..   |               |

| Symbol                     | Description                                              | Min. | Typ. | Max. | Units |
|----------------------------|----------------------------------------------------------|------|------|------|-------|
| I <sub>STBY_X32M_X0</sub>  | Epson TSX-3225                                           | ..   | ..   | ..   | μA    |
| I <sub>STBY_X32M_X1</sub>  | Epson FA-20H                                             | ..   | ..   | ..   | μA    |
| I <sub>STBY_X32M_X2</sub>  | Epson FA-128                                             | ..   | ..   | ..   | μA    |
| I <sub>STBY_X32M_X3</sub>  | NDK NX1612AA                                             | ..   | ..   | ..   | μA    |
| I <sub>STBY_X32M_X4</sub>  | NDK NX1210AB                                             | ..   | ..   | ..   | μA    |
| I <sub>START_X32M</sub>    | Average startup current for various crystals, first 1 ms | ..   | ..   | ..   |       |
| I <sub>START_X32M_X0</sub> | Epson TSX-3225                                           | ..   | ..   | ..   | μA    |
| I <sub>START_X32M_X1</sub> | Epson FA-20H                                             | ..   | ..   | ..   | μA    |
| I <sub>START_X32M_X2</sub> | Epson FA-128                                             | ..   | ..   | ..   | μA    |
| I <sub>START_X32M_X3</sub> | NDK NX1612AA                                             | ..   | ..   | ..   | μA    |
| I <sub>START_X32M_X4</sub> | NDK NX1210AB                                             | ..   | ..   | ..   | μA    |
| t <sub>POWER_X32M</sub>    | Power-up time for various crystals                       | ..   | ..   | ..   |       |
| t <sub>POWER_X32M_X0</sub> | Epson TSX-3225                                           | ..   | ..   | ..   | μs    |
| t <sub>POWER_X32M_X1</sub> | Epson FA-20H                                             | ..   | ..   | ..   | μs    |
| t <sub>POWER_X32M_X2</sub> | Epson FA-128                                             | ..   | ..   | ..   | μs    |
| t <sub>POWER_X32M_X3</sub> | NDK NX1612AA                                             | ..   | ..   | ..   | μs    |
| t <sub>POWER_X32M_X4</sub> | NDK NX1210AB                                             | ..   | ..   | ..   | μs    |

#### 4.9.4.6 32.768 kHz crystal oscillator (LFXO)

| Symbol                    | Description                                    | Min. | Typ.   | Max. | Units |
|---------------------------|------------------------------------------------|------|--------|------|-------|
| f <sub>NOM_LFXO</sub>     | Crystal frequency                              |      | 32.768 |      | kHz   |
| f <sub>TOL_LFXO_BLE</sub> | Frequency tolerance requirement for BLE stack  | ..   | ..     | ..   | ppm   |
| f <sub>TOL_LFXO_ANT</sub> | Frequency tolerance requirement for ANT stack  | ..   | ..     | ..   | ppm   |
| C <sub>L_LFXO</sub>       | Load capacitance                               | ..   | ..     | ..   | pF    |
| C <sub>0_LFXO</sub>       | Shunt capacitance                              | ..   | ..     | ..   | pF    |
| R <sub>S_LFXO</sub>       | Equivalent series resistance                   | ..   | ..     | ..   | kΩ    |
| P <sub>D_LFXO</sub>       | Drive level                                    | ..   | ..     | ..   | μW    |
| C <sub>pin</sub>          | Input capacitance on XL1 and XL2 pads          | ..   | ..     | ..   | pF    |
| I <sub>LFXO</sub>         | Run current for 32.768 kHz crystal oscillator  | ..   | ..     | ..   | μA    |
| t <sub>START_LFXO</sub>   | Startup time for 32.768 kHz crystal oscillator | ..   | ..     | ..   | s     |

#### 4.9.4.7 32.768 kHz RC oscillator (LFRC)

| Symbol                    | Description                                        | Min. | Typ.   | Max. | Units |
|---------------------------|----------------------------------------------------|------|--------|------|-------|
| f <sub>NOM_LFRC</sub>     | Nominal frequency                                  |      | 32.768 |      | kHz   |
| f <sub>TOL_LFRC</sub>     | Frequency tolerance, uncalibrated                  | ..   | ..     | ..   | %     |
| f <sub>TOL_CAL_LFRC</sub> | Frequency tolerance after calibration <sup>7</sup> | ..   | ..     | ..   | ppm   |
| I <sub>LFRC</sub>         | Run current                                        | ..   | ..     | ..   | μA    |
| t <sub>START_LFRC</sub>   | Startup time                                       | ..   | ..     | ..   | μs    |

#### 4.9.4.8 32.768 kHz ultra-low power RC oscillator (LFULP)

<sup>7</sup> Constant temperature within ±0.5 °C, calibration performed at least every 8 seconds, averaging interval > 7.5 ms, defined as 3 sigma

| Symbol                    | Description         | Min. | Typ.   | Max. | Units         |
|---------------------------|---------------------|------|--------|------|---------------|
| $f_{\text{NOM\_LFULP}}$   | Nominal frequency   |      | 32.768 |      | kHz           |
| $f_{\text{TOL\_LFULP}}$   | Frequency tolerance | ..   | ..     | ..   | %             |
| $I_{\text{LFULP}}$        | Run current         | ..   | ..     | ..   | $\mu\text{A}$ |
| $t_{\text{START\_LFULP}}$ | Startup time        | ..   | ..     | ..   | $\mu\text{s}$ |

#### 4.9.4.9 Synthesized 32.768 kHz clock (LFSYNT)

| Symbol                   | Description       | Min. | Typ.   | Max. | Units |
|--------------------------|-------------------|------|--------|------|-------|
| $f_{\text{NOM\_LFSYNT}}$ | Nominal frequency |      | 32.768 |      | kHz   |

## 4.10 OSCILLATORS — Oscillator control

The system oscillators are shared between the cores in the system and automatically controlled by the clock control system, see [CLOCK — Clock control](#) on page 61.

The system has the following crystal oscillators:

- High-frequency 32 MHz crystal oscillator (HFXO)
- Low-frequency 32.768 kHz crystal oscillator (LFXO)

The crystal oscillators can be configured to use either built-in or external capacitors.

### 4.10.1 High-frequency (32 MHz) crystal oscillator (HFXO)

The high-frequency crystal oscillator (HFXO) is controlled by a 32 MHz external crystal.

The crystal oscillator is designed for use with an AT-cut quartz crystal in parallel resonant mode, connected between pins XC1 and XC2. To achieve correct oscillation frequency, the load capacitance must match the specification in the crystal data sheet. The following figure shows how the 32 MHz crystal is connected to the high frequency crystal oscillator.

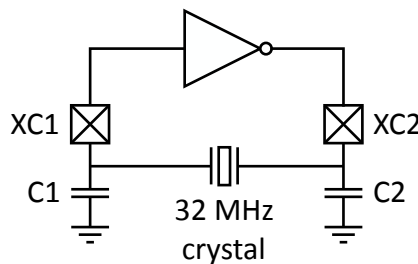


Figure 17: Circuit diagram of the high-frequency crystal oscillator

The load capacitance (CL) is the total capacitance seen by the crystal across its terminals and is calculated by the following equation.

$$CL = \frac{(C1' \cdot C2')}{(C1' + C2')}$$

$$C1' = C1 + C_{pcb1} + C_{pin}$$

$$C2' = C2 + C_{pcb2} + C_{pin}$$

Figure 18: Load capacitance equation

C1 and C2 are ceramic SMD capacitors connected between each crystal terminal and ground. For more information, see [Reference circuitry](#) on page 768.  $C_{pcb1}$  and  $C_{pcb2}$  are stray capacitances on the PCB.  $C_{pin}$  is the pin input capacitance on pins XC1 and XC2. See [table 32 MHz crystal oscillator \(HFXO\)](#) on page 86. The load capacitors C1 and C2 should have the same value.

For reliable operation, the crystal load capacitance, shunt capacitance, equivalent series resistance, and drive level must comply with the specifications in [table 32 MHz crystal oscillator \(HFXO\)](#) on page 86. It is recommended to use a crystal with lower than maximum load capacitance and/or shunt capacitance. A low load capacitance will reduce both startup time and current consumption.

#### 4.10.1.1 Using internal capacitors

Optional internal capacitors ranging from 7.0 pF to 20.0 pF in 0.5 pF steps, are provided on pins XC1 and XC2.

To use these capacitors, in the following equation replace CAPACITANCE with the desired value to find the correct `XOSC32MCAPS.CAPVALUE` field. Then, set `XOSC32MCAPS.ENABLE` to Enabled.

$$CAPVALUE = (1 + FICR \rightarrow XOSC32MTRIM.SLOPE / 16) * (CAPACITANCE * 2 - 14) + FICR \rightarrow XOSC32MTRIM.OFFSET$$

#### 4.10.2 Low-frequency (32.768 kHz) crystal oscillator (LFXO)

For higher LFCLK accuracy (when greater than  $\pm 250$  ppm accuracy is required), the 32.768 kHz crystal oscillator (LFXO) must be used.

To use the LFXO, a 32.768 kHz crystal must be connected between the XL1 and XL2 pins. To achieve correct oscillation frequency, the load capacitance must match the specification in the crystal data sheet.

The LFXO circuitry is illustrated in the following diagram.

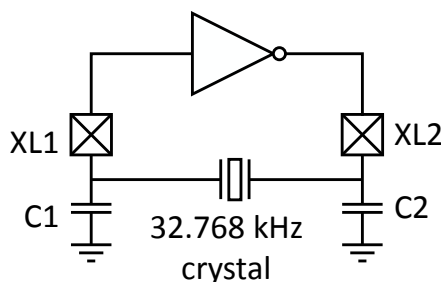


Figure 19: Circuit diagram of the low-frequency crystal oscillator

The load capacitance (CL) is the total capacitance seen by the crystal across its terminals. It is calculated by the following equation.

$$CL = \frac{(C1' \cdot C2')}{(C1' + C2')}$$

$$C1' = C1 + C_{pcb1} + C_{pin}$$

$$C2' = C2 + C_{pcb2} + C_{pin}$$

Figure 20: Load capacitance equation

C1 and C2 are ceramic SMD capacitors connected between each crystal terminal and ground.  $C_{pcb1}$  and  $C_{pcb2}$  are stray capacitances on the PCB.  $C_{pin}$  is the pin input capacitance on the XL1 and XL2 pins (see [32.768 kHz crystal oscillator \(LFXO\)](#) on page 87). The load capacitors C1 and C2 should have the same value.

For more information, see [Reference circuitry](#) on page 768.

#### 4.10.2.1 Using internal capacitors

Optional internal capacitors of 6 pF, 7 pF, and 11 pF are provided on pins XL1 and XL2.

To use these capacitors, select the capacitance in register [XOSC32KI.INTCAP](#).

#### 4.10.3 Low-frequency (32.768 kHz) external source

The 32.768 kHz crystal oscillator (LFXO) is designed to work with external sources.

The following external sources are supported:

- A low swing clock. The signal should be applied to the XL1 pin with the XL2 pin grounded. Set [OSCILLATORS.XOSC32KI.BYPASS](#)=Disabled.
- A rail-to-rail clock. The signal should be applied to the XL1 pin with the XL2 pin left unconnected. Set [OSCILLATORS.XOSC32KI.BYPASS](#)=Enabled.

In order to use an external source, configure [LFCLKSRC.SRC](#)=LFXO.

#### 4.10.4 Registers

| Base address | Domain      | Peripheral  | Instance      | Secure mapping | DMA security | Description              | Configuration |
|--------------|-------------|-------------|---------------|----------------|--------------|--------------------------|---------------|
| 0x50004000   | APPLICATION | OSCILLATORS | OSCILLATORS : | US             | NA           | Oscillator configuration |               |
|              |             |             | S             |                |              |                          |               |
| 0x40004000   |             |             | OSCILLATORS : |                |              |                          |               |
|              |             |             | NS            |                |              |                          |               |

Table 27: Instances

| Register                        | Offset | Security | Description                                                                     | Configuration |
|---------------------------------|--------|----------|---------------------------------------------------------------------------------|---------------|
| <a href="#">XOSC32MCAPS</a>     | 0x5C4  |          | Programmable capacitance of XC1 and XC2                                         | Retained      |
| <a href="#">XOSC32KI.BYPASS</a> | 0x6C0  |          | Enable or disable bypass of LFCLK crystal oscillator with external clock source | Retained      |
| <a href="#">XOSC32KI.INTCAP</a> | 0x6D0  |          | Control usage of internal load capacitors                                       | Retained      |

Table 28: Register overview

##### 4.10.4.1 XOSC32MCAPS ( Retained )

Address offset: 0x5C4

This register is a retained register

Programmable capacitance of XC1 and XC2

|                  |      |          |          |                                                                                       |                                        |                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |
|------------------|------|----------|----------|---------------------------------------------------------------------------------------|----------------------------------------|--------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|---|--|--|--|---|--|--|--|---|--|--|--|
| Bit number       |      |          |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                        |                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |
| ID               |      |          |          |                                                                                       |                                        |                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | B |  |  |  | A |  |  |  | A |  |  |  | A |  |  |  |
| Reset 0x00000000 |      |          |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                   |                                        |                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |
| ID               | Acce | Field    | Value    | ID                                                                                    | Value                                  | Description                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |
| A                | RW   | CAPVALUE |          |                                                                                       |                                        | Value representing capacitance, calculated using provided equation |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |
| B                | RW   | ENABLE   |          |                                                                                       |                                        | Enable on-chip capacitors on XC1 and XC2                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |
|                  |      |          | Disabled | 0                                                                                     | Capacitor disabled (use external caps) |                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |
|                  |      |          | Enabled  | 1                                                                                     | Capacitor enabled                      |                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |

#### 4.10.4.2 XOSC32KI.BYPASS ( Retained )

Address offset: 0x6C0

This register is a retained register

Enable or disable bypass of LFCLK crystal oscillator with external clock source

|                  |      |        |          |    |       |                                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|------------------|------|--------|----------|----|-------|---------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|
| Bit number       |      |        |          | 31 | 30    | 29                                                                              | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |
| ID               |      |        |          |    |       |                                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |  |  |
| Reset 0x00000000 |      |        |          | 0  | 0     | 0                                                                               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |  |  |
| ID               | Acce | Field  | Value    | ID | Value | Description                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
| A                | RW   | BYPASS |          |    |       | Enable or disable bypass of LFCLK crystal oscillator with external clock source |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |        | Disabled | 0  |       | Disable (use with xtal or low-swing external source)                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |        | Enabled  | 1  |       | Enable (use with rail-to-rail external source)                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |

#### 4.10.4.3 XOSC32KI.INTCAP ( Retained )

Address offset: 0x6D0

This register is a retained register

Control usage of internal load capacitors

|                  |            |        |          |   |                                 |                                           |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------|----------|---|---------------------------------|-------------------------------------------|-------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |        |          |   |                                 |                                           |             |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |        |          |   |                                 |                                           |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A | A |   |   |
| Reset 0x00000000 |            |        |          |   |                                 |                                           |             |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |        | Value ID |   | Value                           |                                           | Description |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | INTCAP |          |   |                                 | Control usage of internal load capacitors |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |        | External | 0 | Use external load capacitors    |                                           |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |        | C6PF     | 1 | 6 pF internal load capacitance  |                                           |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |        | C7PF     | 2 | 7 pF internal load capacitance  |                                           |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |        | C11PF    | 3 | 11 pF internal load capacitance |                                           |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

# 5.1 Application core

## 5.1.1 Application core overview

The application core contains a low-power microcontroller with embedded flash memory and a full featured Arm Cortex-M33 processor.

In addition, the application core includes a rich set of peripherals for serial communication, analog interfaces, and cryptographic acceleration. See the following figure for more information. Arrows with white heads indicate signals that share physical pins with other signals, while arrows with black heads are dedicated to one signal.



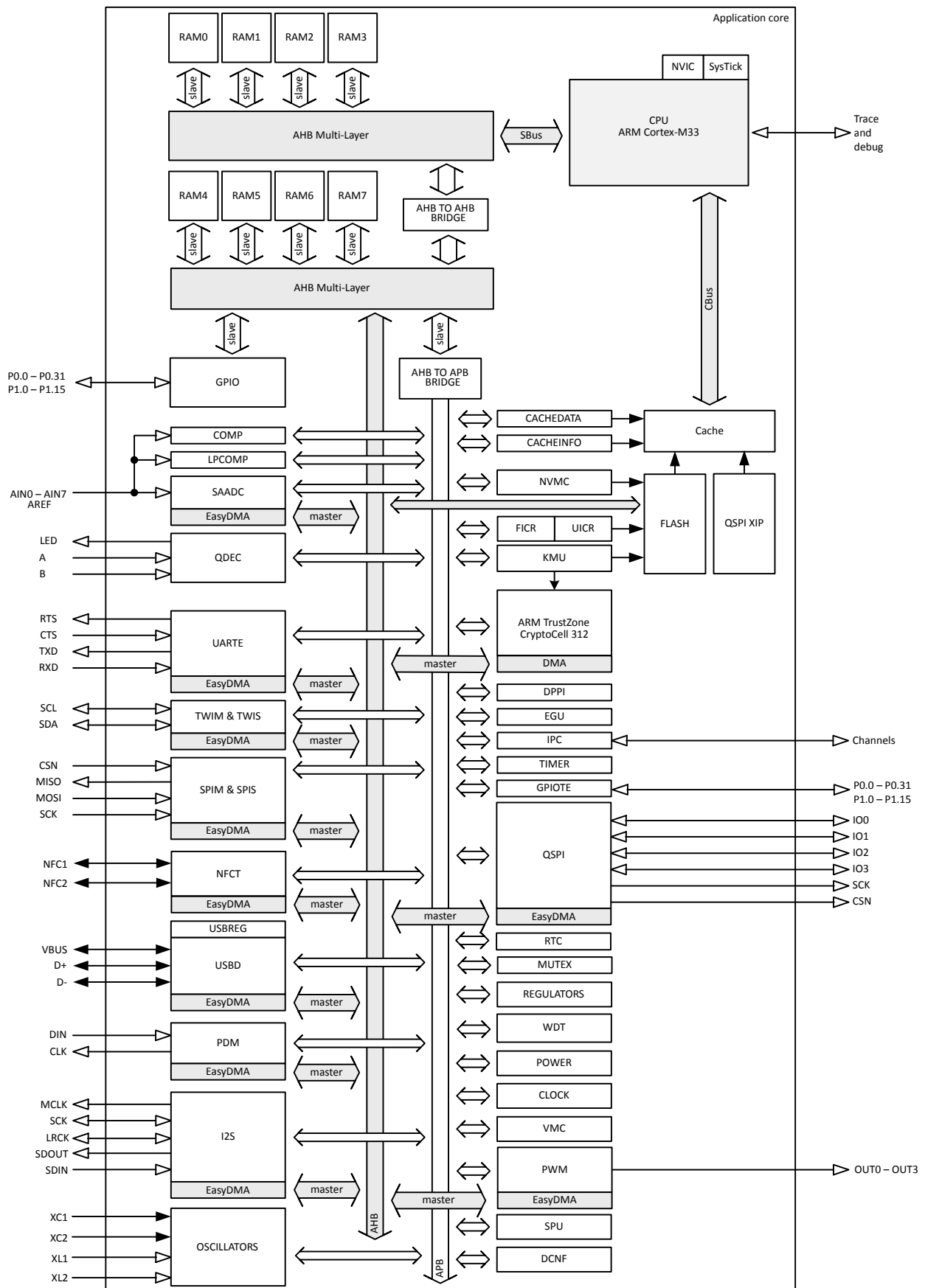


Figure 21: Application core block diagram

## 5.1.2 CPU

The Arm Cortex-M33 processor has a 32-bit instruction set (Thumb-2 technology) that implements a superset of 16- and 32-bit instructions to maximize code density and performance.

This processor implements several features that enable energy-efficient arithmetic and high-performance signal processing including:

- Digital signal processing (DSP) instructions
- Single-cycle multiply and accumulate (MAC) instructions
- Hardware divide
- 8- and 16-bit single instruction multiple data (SIMD) instructions
- Single-precision floating-point unit (FPU)
- Memory Protection Unit (MPU)
- Arm TrustZone for Armv8-M

The [Arm Cortex Microcontroller Software Interface Standard \(CMSIS\)](#) is implemented and available for the application processor.

Real-time execution is highly deterministic in thread mode, to and from sleep modes, and when handling events at configurable priority levels via the Nested Vectored Interrupt Controller (NVIC).

Executing code from internal or external flash will have a wait state penalty. The instruction cache can be enabled to minimize flash wait states when fetching instructions. For more information on cache, see [Cache](#) on page 320. CPU performance parameters including wait states for different configurations, CPU current consumption and efficiency, and processing power and efficiency based on the CoreMark benchmark can be found in .

### 5.1.2.1 Floating point interrupt

The floating point unit (FPU) may generate exceptions, for example, due to overflow or underflow. These exceptions may trigger interrupts when enabled in the FPU peripheral. For more information, see [FPU - Floating point unit \(FPU\) exceptions](#) on page 204.

### 5.1.2.2 Electrical specification

#### 5.1.2.2.1 CPU performance

| Symbol                  | Description                                                           | Min. | Typ. | Max. | Units                    |
|-------------------------|-----------------------------------------------------------------------|------|------|------|--------------------------|
| W <sub>FLASH</sub>      | CPU wait states, running from flash, cache disabled                   | ..   | ..   | ..   |                          |
| W <sub>FLASHCACHE</sub> | CPU wait states, running from flash, cache enabled                    | ..   | ..   | ..   |                          |
| W <sub>RAM</sub>        | CPU wait states, running from RAM                                     | ..   | ..   | ..   |                          |
| CM <sub>FLASH</sub>     | CoreMark <sup>8</sup> , running from flash, cache enabled, HFXO128M   |      | 510  |      | Core <sup>†</sup>        |
| CM <sub>FLASH/MHz</sub> | CoreMark per MHz, running from flash, cache enabled, HFXO128M         |      | 3.9  |      | CoreMark/<br>MHz         |
| CM <sub>FLASH/mA</sub>  | CoreMark per mA, running from flash, cache enabled, DCDC 3V, HFXO128M |      | 65   |      | Core <sup>†</sup><br>mA  |
| CM <sub>FLASH</sub>     | CoreMark <sup>9</sup> , running from flash, cache enabled, HFXO64M    |      | 255  |      | CoreMark                 |
| CM <sub>FLASH/MHz</sub> | CoreMark per MHz, running from flash, cache enabled, HFXO64M          |      | 3.9  |      | Core <sup>†</sup><br>MHz |

<sup>8</sup> Using ARMCLANG compiler

<sup>9</sup> Using ARMCLANG compiler

| Symbol                  | Description                                                             | Min. | Typ. | Max. | Units           |
|-------------------------|-------------------------------------------------------------------------|------|------|------|-----------------|
| CM <sub>FLASH</sub> /mA | CoreMark per mA, running from flash, cache enabled, DCDC<br>3V, HFXO64M |      | 76   |      | CoreMark/<br>mA |

### 5.1.2.3 CPU and support module configuration

The Arm Cortex-M33 processor has a number of CPU options and support modules implemented on the device.

| Option/Module                                                      | Description                         | Implemented   |
|--------------------------------------------------------------------|-------------------------------------|---------------|
| Core options                                                       |                                     |               |
| PRIORITIES                                                         | Priority bits                       | 3             |
| WIC                                                                | Wakeup Interrupt Controller         | NO            |
| Endianness                                                         | Memory system endianness            | Little endian |
| DWT                                                                | Data Watchpoint and Trace           | YES           |
| Modules                                                            |                                     |               |
| MPU_NS                                                             | Number of non-secure MPU regions    | 8             |
| MPU_S                                                              | Number of secure MPU regions        | 8             |
| SAU                                                                | Number of SAU regions               | 0             |
| See <a href="#">SPU</a> for more information about secure regions. |                                     |               |
| FPU                                                                | Floating-point unit                 | YES           |
| DSP                                                                | Digital Signal Processing Extension | YES           |
| Arm TrustZone for Armv8-M                                          | ARMv8-M Security Extensions         | YES           |
| CPIF                                                               | Coprocessor interface               | NO            |
| ETM                                                                | Embedded Trace Macrocell            | YES           |
| ITM                                                                | Instrumentation Trace Macrocell     | YES           |
| MTB                                                                | Micro Trace Buffer                  | NO            |
| CTI                                                                | Cross Trigger Interface             | YES           |
| BPU                                                                | Breakpoint Unit                     | YES           |
| HTM                                                                | AHB Trace Macrocell                 | NO            |

### 5.1.3 Memory

The application core contains flash memory and RAM that can be used for code and data storage.

The following figure shows how the CPU, network core, and peripherals with EasyDMA can access RAM via the AHB multilayer interconnect. The domain configuration (DCNF) registers can block access from external DMA masters, see [DCNF — Domain configuration](#) on page 186.

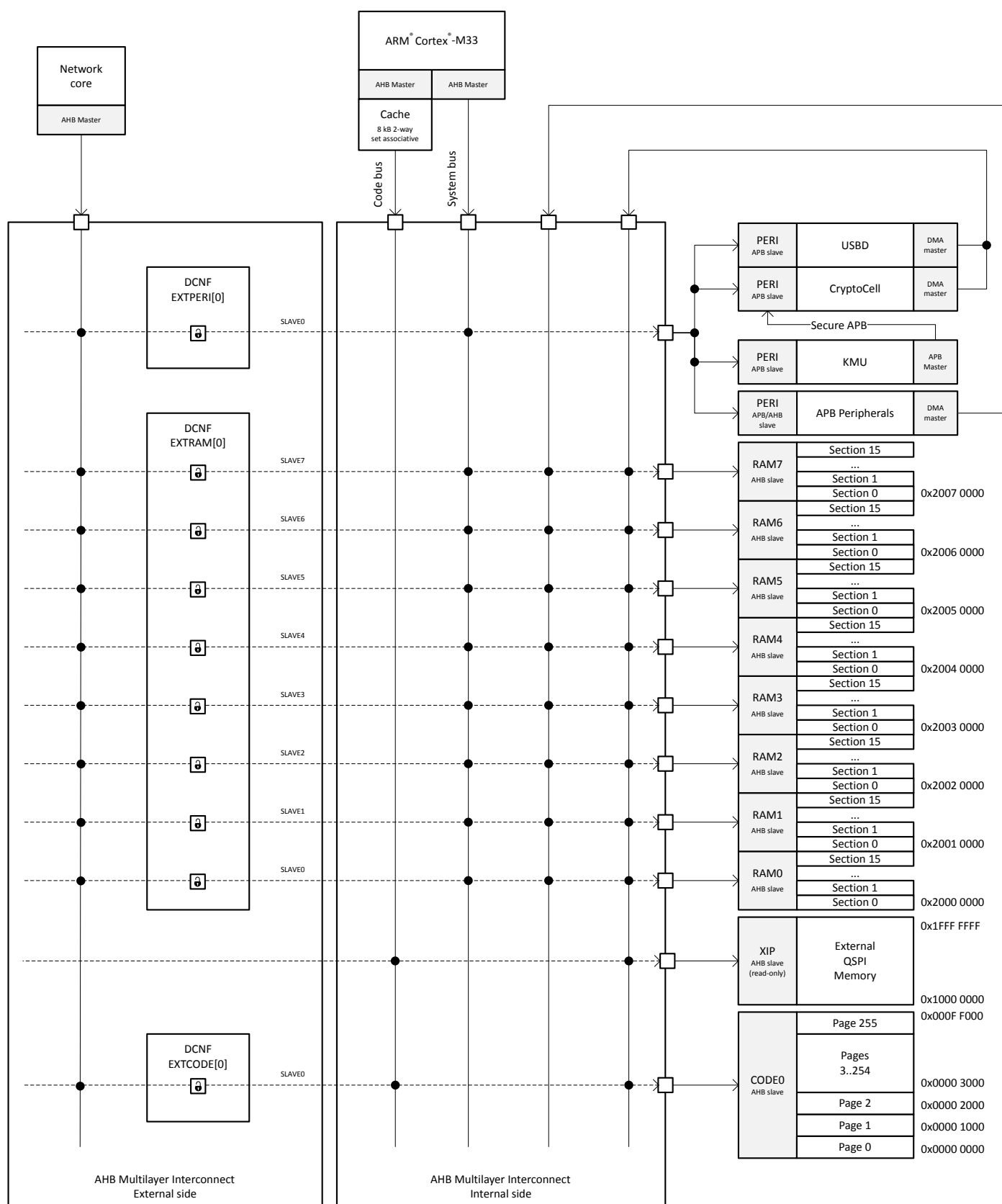


Figure 22: Memory layout

### 5.1.3.1 Peripheral instantiation

The following table describes the abbreviations used in the Instance, Secure mapping, and DMA security columns of the instantiation table.

| Abbreviation | Description                                                                                                                               |
|--------------|-------------------------------------------------------------------------------------------------------------------------------------------|
| NS           | Non-secure - Peripheral is always accessible as a Non-Secure peripheral                                                                   |
| S            | Secure - Peripheral is always accessible as a Secure peripheral                                                                           |
| US           | User Selectable - A Secure or Non-secure attribute for the peripheral is defined in the SPU                                               |
| SPLIT        | Both Secure and Non-secure - The same resource is shared by both secure and non-secure code                                               |
| NA           | Not Applicable - Peripheral has no DMA capability                                                                                         |
| NSA          | NoSeparateAttribute - Peripheral with DMA and DMA transfer has the same security attribute as assigned to the peripheral                  |
| SA           | SeparateAttribute - Peripheral with DMA and DMA transfers can have a different security attribute than the one assigned to the peripheral |

Table 29: Instantiation table abbreviations

The Secure mapping column in the following table defines configuration capabilities for the Arm TrustZone for Armv8-M secure attribute. The DMA security column describes the DMA capabilities of the peripheral.

### 5.1.3.1.1 Instantiation

| ID | Base address             | Peripheral  | Instance                            | Secure mapping | DMA security | Description                                                |
|----|--------------------------|-------------|-------------------------------------|----------------|--------------|------------------------------------------------------------|
| 0  | 0x50000000<br>0x40000000 | DCNF        | DCNF : S<br>DCNF : NS               | US             | NA           | Domain configuration                                       |
| 0  | 0x50000000<br>0x40000000 | FPU         | FPU : S<br>FPU : NS                 | US             | NA           | Floating Point unit interrupt control                      |
| 1  | 0x50001000               | CACHE       | CACHE                               | S              | NA           | Cache                                                      |
| 3  | 0x50003000               | SPU         | SPU                                 | S              | NA           | System protection unit                                     |
| 4  | 0x50004000<br>0x40004000 | OSCILLATORS | OSCILLATORS : S<br>OSCILLATORS : NS | US             | NA           | Oscillator configuration                                   |
| 4  | 0x50004000<br>0x40004000 | REGULATORS  | REGULATORS : S<br>REGULATORS : NS   | US             | NA           | Regulator configuration                                    |
| 5  | 0x50005000<br>0x40005000 | CLOCK       | CLOCK : S<br>CLOCK : NS             | US             | NA           | Clock control                                              |
| 5  | 0x50005000<br>0x40005000 | POWER       | POWER : S<br>POWER : NS             | US             | NA           | Power control                                              |
| 5  | 0x50005000<br>0x40005000 | RESET       | RESET : S<br>RESET : NS             | US             | NA           | Reset control and status                                   |
| 6  | 0x50006000<br>0x40006000 | CTRLAPPERI  | CTRLAP : S<br>CTRLAP : NS           | US             | NSA          | Control access port CPU side                               |
| 8  | 0x50008000<br>0x40008000 | SPIM        | SPIM0 : S<br>SPIM0 : NS             | US             | SA           | SPI master 0                                               |
| 8  | 0x50008000<br>0x40008000 | SPIS        | SPIS0 : S<br>SPIS0 : NS             | US             | SA           | SPI slave 0                                                |
| 8  | 0x50008000<br>0x40008000 | TWIM        | TWIM0 : S<br>TWIM0 : NS             | US             | SA           | Two-wire interface master 0                                |
| 8  | 0x50008000<br>0x40008000 | TWIS        | TWIS0 : S<br>TWIS0 : NS             | US             | SA           | Two-wire interface slave 0                                 |
| 8  | 0x50008000<br>0x40008000 | UARTE       | UARTE0 : S<br>UARTE0 : NS           | US             | SA           | Universal asynchronous receiver/transmitter with EasyDMA 0 |

| ID | Base address             | Peripheral | Instance                  | Secure mapping | DMA security | Description                                                |
|----|--------------------------|------------|---------------------------|----------------|--------------|------------------------------------------------------------|
| 9  | 0x50009000<br>0x40009000 | SPIM       | SPIM1 : S<br>SPIM1 : NS   | US             | SA           | SPI master 1                                               |
| 9  | 0x50009000<br>0x40009000 | SPIS       | SPIS1 : S<br>SPIS1 : NS   | US             | SA           | SPI slave 1                                                |
| 9  | 0x50009000<br>0x40009000 | TWIM       | TWIM1 : S<br>TWIM1 : NS   | US             | SA           | Two-wire interface master 1                                |
| 9  | 0x50009000<br>0x40009000 | TWIS       | TWIS1 : S<br>TWIS1 : NS   | US             | SA           | Two-wire interface slave 1                                 |
| 9  | 0x50009000<br>0x40009000 | UARTE      | UARTE1 : S<br>UARTE1 : NS | US             | SA           | Universal asynchronous receiver/transmitter with EasyDMA 1 |
| 10 | 0x5000A000<br>0x4000A000 | SPIM       | SPIM2 : S<br>SPIM2 : NS   | US             | SA           | SPI master 2 (high-speed)                                  |
| 13 | 0x5000D000               | GPIOE      | GPIOE0                    | S              | NA           | GPIO tasks and events                                      |
| 14 | 0x5000E000<br>0x4000E000 | SAADC      | SAADC : S<br>SAADC : NS   | US             | SA           | Successive approximation analog-to-digital converter       |
| 15 | 0x5000F000<br>0x4000F000 | TIMER      | TIMER0 : S<br>TIMER0 : NS | US             | NA           | Timer 0                                                    |
| 16 | 0x50010000<br>0x40010000 | TIMER      | TIMER1 : S<br>TIMER1 : NS | US             | NA           | Timer 1                                                    |
| 17 | 0x50011000<br>0x40011000 | TIMER      | TIMER2 : S<br>TIMER2 : NS | US             | NA           | Timer 2                                                    |
| 20 | 0x50014000<br>0x40014000 | RTC        | RTC0 : S<br>RTC0 : NS     | US             | NA           | Real time counter 0                                        |
| 21 | 0x50015000<br>0x40015000 | RTC        | RTC1 : S<br>RTC1 : NS     | US             | NA           | Real time counter 1                                        |
| 23 | 0x50017000<br>0x40017000 | DPPI       | DPPI : S<br>DPPI : NS     | SPLIT          | NA           | DPPI controller                                            |
| 24 | 0x50018000<br>0x40018000 | WDT        | WDT0 : S<br>WDT0 : NS     | US             | NA           | Watchdog timer 0                                           |
| 25 | 0x50019000<br>0x40019000 | WDT        | WDT1 : S<br>WDT1 : NS     | US             | NA           | Watchdog timer 1                                           |
| 26 | 0x5001A000<br>0x4001A000 | COMP       | COMP : S<br>COMP : NS     | US             | NA           | Comparator                                                 |
| 26 | 0x5001A000<br>0x4001A000 | LPCOMP     | LPCOMP : S<br>LPCOMP : NS | US             | NA           | Low-power comparator                                       |
| 27 | 0x5001B000<br>0x4001B000 | EGU        | EGU0 : S<br>EGU0 : NS     | US             | NA           | Event generator unit 0                                     |
| 28 | 0x5001C000<br>0x4001C000 | EGU        | EGU1 : S<br>EGU1 : NS     | US             | NA           | Event generator unit 1                                     |
| 29 | 0x5001D000<br>0x4001D000 | EGU        | EGU2 : S<br>EGU2 : NS     | US             | NA           | Event generator unit 2                                     |
| 30 | 0x5001E000<br>0x4001E000 | EGU        | EGU3 : S<br>EGU3 : NS     | US             | NA           | Event generator unit 3                                     |
| 31 | 0x5001F000<br>0x4001F000 | EGU        | EGU4 : S<br>EGU4 : NS     | US             | NA           | Event generator unit 4                                     |
| 32 | 0x50020000<br>0x40020000 | EGU        | EGU5 : S<br>EGU5 : NS     | US             | NA           | Event generator unit 5                                     |
| 33 | 0x50021000<br>0x40021000 | PWM        | PWM0 : S<br>PWM0 : NS     | US             | SA           | Pulse width modulation unit 0                              |
| 34 | 0x50022000<br>0x40022000 | PWM        | PWM1 : S<br>PWM1 : NS     | US             | SA           | Pulse width modulation unit 1                              |
| 35 | 0x50023000<br>0x40023000 | PWM        | PWM2 : S<br>PWM2 : NS     | US             | SA           | Pulse width modulation unit 2                              |

| ID  | Base address             | Peripheral | Instance                                    | Secure mapping | DMA security | Description                                             |
|-----|--------------------------|------------|---------------------------------------------|----------------|--------------|---------------------------------------------------------|
| 38  | 0x50026000<br>0x40026000 | PDM        | PDM0 : S<br>PDM0 : NS                       | US             | SA           | Pulse density modulation (digital microphone) interface |
| 40  | 0x50028000<br>0x40028000 | I2S        | I2S0 : S<br>I2S0 : NS                       | US             | SA           | Inter-IC sound interface                                |
| 42  | 0x5002A000<br>0x4002A000 | IPC        | IPC : S<br>IPC : NS                         | US             | NA           | Interprocessor communication                            |
| 43  | 0x5002B000<br>0x4002B000 | QSPI       | QSPI : S<br>QSPI : NS                       | US             | SA           | External memory (quad serial peripheral) interface      |
| 45  | 0x5002D000<br>0x4002D000 | NFCT       | NFCT : S<br>NFCT : NS                       | US             | SA           | Near field communication tag                            |
| 47  | 0x4002F000               | GPIOTE     | GPIOTE1                                     | NS             | NA           | GPIO tasks and events                                   |
| 48  | 0x50030000<br>0x40030000 | MUTEX      | MUTEX : S<br>MUTEX : NS                     | US             | NA           | Mutual exclusive hardware support                       |
| 51  | 0x50033000<br>0x40033000 | QDEC       | QDEC : S<br>QDEC : NS                       | US             | NA           | Quadrature decoder                                      |
| 54  | 0x50036000<br>0x40036000 | USBBD      | USBBD : S<br>USBBD : NS                     | US             | SA           | Universal serial bus device                             |
| 55  | 0x50037000<br>0x40037000 | USBREG     | USBREGULATOR :<br>S<br>USBREGULATOR :<br>NS | US             | NA           | USB regulator control                                   |
| 57  | 0x50039000<br>0x40039000 | KMU        | KMU : S<br>KMU : NS                         | SPLIT          | NA           | Key management unit                                     |
| 57  | 0x50039000<br>0x40039000 | NVMC       | NVMC : S<br>NVMC : NS                       | SPLIT          | NA           | Non-volatile memory controller                          |
| 66  | 0x50842500<br>0x40842500 | GPIO       | P0 : S<br>P0 : NS                           | SPLIT          | NA           | General purpose input and output, port 0                |
| 66  | 0x50842800<br>0x40842800 | GPIO       | P1 : S<br>P1 : NS                           | SPLIT          | NA           | General purpose input and output, port 1                |
| 68  | 0x50844000               | CRYPTOCELL | CRYPTOCELL                                  | S              | NSA          | CryptoCell subsystem control interface                  |
| 129 | 0x50081000<br>0x40081000 | VMC        | VMC : S<br>VMC : NS                         | US             | NA           | Volatile memory controller                              |
| N/A | 0x00F00000               | CACHEDATA  | CACHEDATA                                   | S              | NA           | Cache data                                              |
| N/A | 0x00F08000               | CACHEINFO  | CACHEINFO                                   | S              | NA           | Cache info                                              |
| N/A | 0x00FF0000               | FICR       | FICR                                        | S              | NA           | Factory information configuration registers             |
| N/A | 0x00FF8000               | UICR       | UICR                                        | S              | NA           | User information configuration registers                |
| N/A | 0xE0042000               | CTI        | CTI                                         | S              | NA           | Cross-trigger interface                                 |
| N/A | 0xE0080000               | TAD        | TAD                                         | S              | NA           | Trace and debug control                                 |

Table 30: Instantiation table

## 5.1.4 Core components

### 5.1.4.1 CACHE — Instruction/data cache

The cache is two-way set associative with a least recently used (LRU) replacement policy. Both instruction and data accesses towards flash memory or XIP code regions are cached.

The cache has the following features:

- 128-bit cache line
- Configurable as a cache or general purpose RAM
- Hit/miss counters per NVM region and access type (instruction or data)

- Readable cache content (for profiling)
  - Data, tag, valid, and most recently used (MRU) bits
  - Can be disabled when not in use
- Manual invalidation and erase support
- Locking cache updates on cache misses

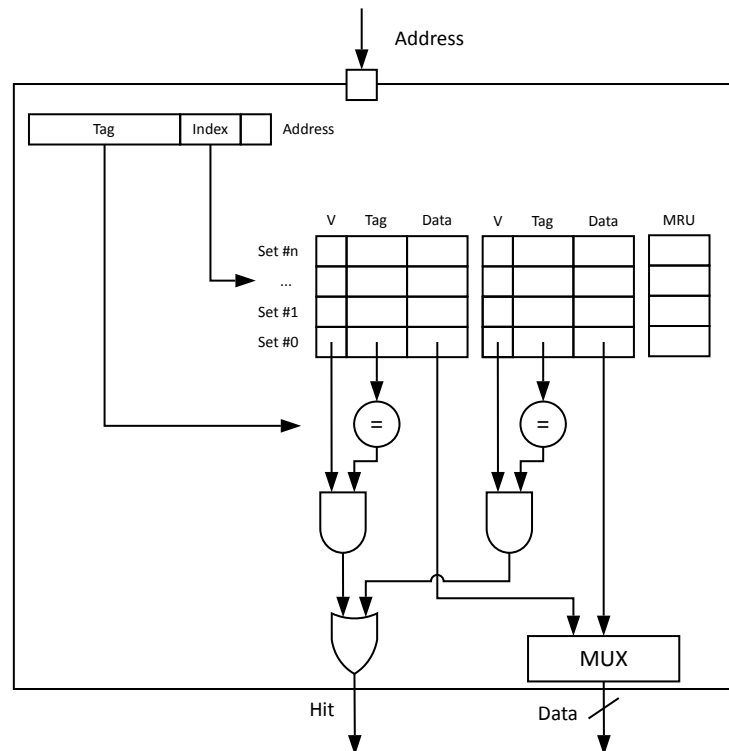


Figure 23: Cache overview

In Cache mode (**MODE**=Cache), instruction and data accesses from the CPU over the code bus towards internal or external flash, are cached. The contents of the cache, i.e. data, tag, valid, and MRU bits, are memory mapped, see [Cache content](#) on page 100. This can be used for performance profiling of code running in the system. Access to the cache content region is read-only by default, but can be blocked by enabling a lock bit in **DEBUGLOCK** on page 105. Preventing cache content updates on cache misses can be enabled through register **DEBUGLOCK** on page 105. When enabled, cache content is not replaced, but kept intact. The cache is still enabled and provides fast instruction and data fetches for cached content.

Access to internal or external flash memory will not be cached when in Ram mode (**MODE**=Ram). Instead, the cache data content, as described in [Cache content](#) on page 100, can be used as read/write RAM.

#### 5.1.4.1.1 Cache content

Cache information is divided into cache info content and cache data content.

Cache info content is organized in memory as show in the following figure.



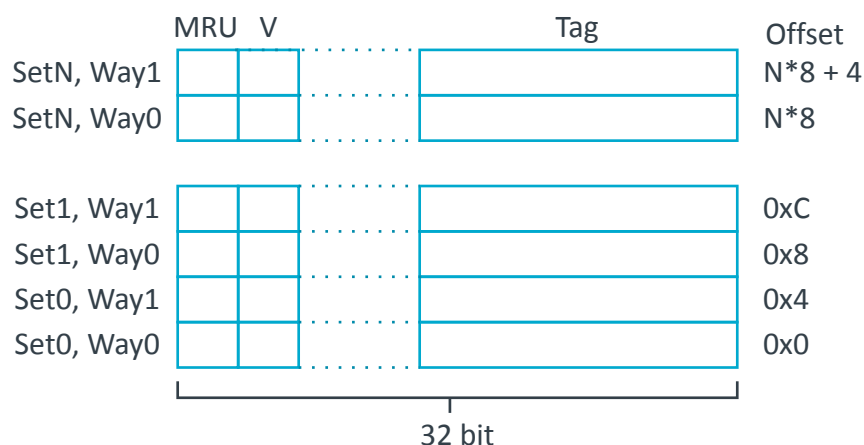


Figure 24: Cache info content

The V field contains the bit that indicates if a cache entry is valid or not. All V fields are cleared when invalidating the cache using register [INVALIDATE](#) on page 104, when disabling the cache using register [ENABLE](#) on page 103, or when changing [MODE](#) from RAM to Cache. The MRU field indicates which way was used most recently in the set. The MRU bit is updated on each fetch from the cache and is used for the cache replacement policy. The Tag field is used to check if an entry in the cache matches the address being fetched.

The following figure shows how the cache data content is organized in memory.

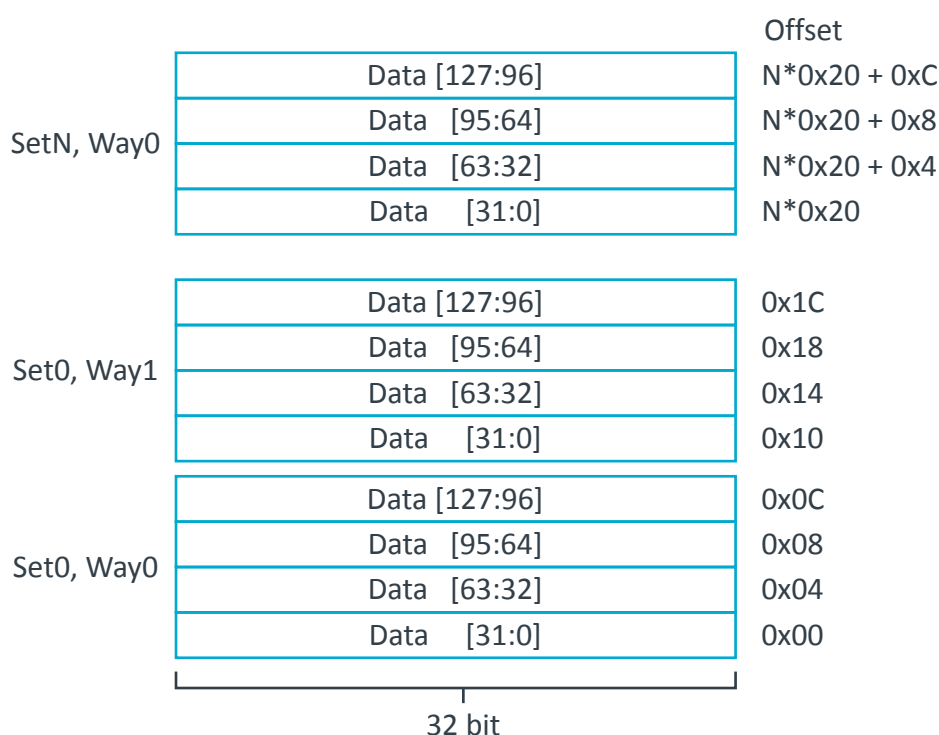


Figure 25: Cache data content

Each set consists of two ways, each containing 128-bits of data. The 128-bit data is available as 4x32-bit words in sequential order. When operating in RAM mode ([MODE](#) = Ram), the data is accessible as general purpose RAM.

The cache info and cache data content are memory mapped in the [CACHEINFO](#) and [CACHEDATA](#) regions. These can be accessed in the [CACHEINFO registers](#) and [CACHEDATA registers](#) respectively.

### 5.1.4.1.2 Profiling

The cache includes profiling counters **IHIT**, **IMISS**, **DHIT**, and **DMISS** for both flash and execute-in-place (XIP).

Cache performance on executed code is indicated by these counters when enabled through **PROFILINGENABLE** on page 104. The counters can be cleared at any time using **PROFILINGCLEAR** on page 104. Writing to this register will clear all profiling counters. After being cleared, the counters will increment at the next instruction, or data fetch, according to the rules in the following table.

| Profiling counter | Description                                                                                      |
|-------------------|--------------------------------------------------------------------------------------------------|
| <b>IHIT</b>       | Increased on a cache hit for instruction fetch                                                   |
| <b>IMISS</b>      | Increased on a cache miss for instruction fetch                                                  |
| <b>DHIT</b>       | Increased on a cache hit for data fetch (i.e. LOAD type instruction targeting the cache region)  |
| <b>DMISS</b>      | Increased on a cache miss for data fetch (i.e. LOAD type instruction targeting the cache region) |

Table 31: Profiling counters

### 5.1.4.1.3 Registers

| Base address | Domain      | Peripheral | Instance | Secure mapping | DMA security | Description | Configuration |
|--------------|-------------|------------|----------|----------------|--------------|-------------|---------------|
| 0x50001000   | APPLICATION | CACHE      | CACHE    | S              | NA           | Cache       |               |

Table 32: Instances

| Register                  | Offset | Security | Description                                                                                                                                                                                       |
|---------------------------|--------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>PROFILING[n].IHIT</b>  | 0x400  |          | Instruction fetch cache hit counter for cache region n, where n=0 means Flash and n=1 means XIP.                                                                                                  |
| <b>PROFILING[n].IMISS</b> | 0x404  |          | Instruction fetch cache miss counter for cache region n, where n=0 means Flash and n=1 means XIP.                                                                                                 |
| <b>PROFILING[n].DHIT</b>  | 0x408  |          | Data fetch cache hit counter for cache region n, where n=0 means Flash and n=1 means XIP.                                                                                                         |
| <b>PROFILING[n].DMISS</b> | 0x40C  |          | Data fetch cache miss counter for cache region n, where n=0 means Flash and n=1 means XIP.                                                                                                        |
| <b>ENABLE</b>             | 0x500  |          | Enable cache                                                                                                                                                                                      |
| <b>INVALIDATE</b>         | 0x504  |          | Invalidate the cache                                                                                                                                                                              |
| <b>ERASE</b>              | 0x508  |          | Erase the cache                                                                                                                                                                                   |
| <b>PROFILINGENABLE</b>    | 0x50C  |          | Enable the profiling counters                                                                                                                                                                     |
| <b>PROFILINGCLEAR</b>     | 0x510  |          | Clear the profiling counters                                                                                                                                                                      |
| <b>MODE</b>               | 0x514  |          | Cache mode.<br><br>Switching from Cache to RAM mode causes the RAM to be cleared.<br><br>Switching from RAM to Cache mode causes the cache to be invalidated.                                     |
| <b>DEBUGLOCK</b>          | 0x518  |          | Lock debug mode<br><br>Ignored in RAM mode.                                                                                                                                                       |
| <b>ERASESTATUS</b>        | 0x51C  |          | Cache erase status                                                                                                                                                                                |
| <b>WRITELOCK</b>          | 0x520  |          | Lock cache updates. Prevents updating of cache content on cache misses, but will continue to lookup instruction/data fetches in content already present in the cache.<br><br>Ignored in RAM mode. |

Table 33: Register overview

#### 5.1.4.1.3.1 PROFILING[n].IHIT (n=0..1)

Address offset:  $0x400 + (n \times 0x20)$

Instruction fetch cache hit counter for cache region n, where n=0 means Flash and n=1 means XIP.

| Bit number       |            | 31       | 30 | 29    | 28 | 27                               | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------|------------|----------|----|-------|----|----------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| ID               |            | A        | A  | A     | A  | A                                | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            | 0        | 0  | 0     | 0  | 0                                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID |    | Value |    | Description                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | R          | HITS     |    |       |    | Number of instruction cache hits |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 5.1.4.1.3.2 PROFILING[n].IMISS (n=0..1)

Address offset:  $0x404 + (n \times 0x20)$

Instruction fetch cache miss counter for cache region n, where n=0 means Flash and n=1 means XIP.

| Bit number       |            | 31       | 30 | 29    | 28 | 27                                 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------|------------|----------|----|-------|----|------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| ID               |            | A        | A  | A     | A  | A                                  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            | 0        | 0  | 0     | 0  | 0                                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID |    | Value |    | Description                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | R          | MISSES   |    |       |    | Number of instruction cache misses |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 5.1.4.1.3.3 PROFILING[n].DHIT (n=0..1)

Address offset:  $0x408 + (n \times 0x20)$

Data fetch cache hit counter for cache region n, where n=0 means Flash and n=1 means XIP.

| Bit number       |            | 31       | 30 | 29    | 28 | 27                        | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------|------------|----------|----|-------|----|---------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| ID               |            | A        | A  | A     | A  | A                         | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            | 0        | 0  | 0     | 0  | 0                         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID |    | Value |    | Description               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | R          | HITS     |    |       |    | Number of data cache hits |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 5.1.4.1.3.4 PROFILING[n].DMISS (n=0..1)

Address offset:  $0x40C + (n \times 0x20)$

Data fetch cache miss counter for cache region n, where n=0 means Flash and n=1 means XIP.

| Bit number       |            | 31       | 30 | 29    | 28 | 27                          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------|------------|----------|----|-------|----|-----------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| ID               |            | A        | A  | A     | A  | A                           | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            | 0        | 0  | 0     | 0  | 0                           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID |    | Value |    | Description                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | R          | MISSES   |    |       |    | Number of data cache misses |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 5.1.4.1.3.5 ENABLE

Address offset: 0x500

Enable cache

|                  |            |        |          |  |       |  |               |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------|----------|--|-------|--|---------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |        |          |  |       |  |               |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |        |          |  |       |  |               |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |
| Reset 0x00000000 |            |        |          |  |       |  |               |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |        | Value ID |  | Value |  | Description   |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | ENABLE |          |  |       |  | Enable cache  |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |        | Disabled |  | 0     |  | Disable cache |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |        | Enabled  |  | 1     |  | Enable cache  |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

#### 5.1.4.1.3.6 INVALIDATE

Address offset: 0x504

Invalidate the cache

|                  |            |            |            |   |       |                      |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|------------|------------|---|-------|----------------------|-------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |            |            |   |       |                      |             |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |            |            |   |       |                      |             |  |  | A  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |            |            |   |       |                      |             |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |            | Value ID   |   | Value |                      | Description |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | INVALIDATE |            |   |       | Invalidate the cache |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |            | Invalidate | 1 |       | Invalidate the cache |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

#### 5.1.4.1.3.7 ERASE

Address offset: 0x508

Erase the cache

|                  |            |       |       |          |  |  |       |  |  |             |                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-------|-------|----------|--|--|-------|--|--|-------------|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |       |       |          |  |  |       |  |  | 31          | 30              | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |       |       |          |  |  |       |  |  |             |                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |   |
| Reset 0x00000000 |            |       |       |          |  |  |       |  |  | 0           | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |       |       | Value ID |  |  | Value |  |  | Description |                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | ERASE |       |          |  |  |       |  |  |             | Erase the cache |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |       | Erase |          |  |  | 1     |  |  | Erase cache |                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 5.1.4.1.3.8 PROFILINGENABLE

Address offset: 0x50C

Enable the profiling counters

|                  |            |         |          |   |       |                   |             |                               |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|---------|----------|---|-------|-------------------|-------------|-------------------------------|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |         |          |   |       |                   |             |                               |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |         |          |   |       |                   |             |                               |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |   |
| Reset 0x00000000 |            |         |          |   |       |                   |             |                               |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |         | Value ID |   | Value |                   | Description |                               |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | ENABLE  |          |   |       |                   |             | Enable the profiling counters |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disable |          | 0 |       | Disable profiling |             |                               |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enable  |          | 1 |       | Enable profiling  |             |                               |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 5.1.4.1.3.9 PROFILINGCLEAR

Address offset: 0x510

Clear the profiling counters

The profiling counters can be cleared at any time. When cleared, all profiling counters will be set to zero, and will increment at the next instruction- or data fetch.



|                  |            |             |                                                                                       |                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|-------------|---------------------------------------------------------------------------------------|-----------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |             | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |             | A                                                                                     |                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |             | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID    | Value                                                                                 | Description                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | ERASESTATUS |                                                                                       | Cache erase status                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Idle        | 0                                                                                     | Erase is not complete or hasn't started |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Finished    | 1                                                                                     | Cache erase is finished                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**Note:** Write 0 to clear.

### 5.1.4.1.3.13 WRITELOCK

Address offset: 0x520

Lock cache updates. Prevents updating of cache content on cache misses, but will continue to lookup instruction/data fetches in content already present in the cache.

Ignored in RAM mode.

|                  |            |           |          |                                                                                       |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|-----------|----------|---------------------------------------------------------------------------------------|------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |           |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |           |          | A                                                                                     |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |           |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                     |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field |           | Value ID | Value                                                                                 | Description            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | WRITELOCK |          |                                                                                       | Lock cache updates     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |           | Unlocked | 0                                                                                     | Cache updates unlocked |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |           | Locked   | 1                                                                                     | Cache updates locked   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 5.1.4.1.4 Registers

| Base address | Domain      | Peripheral | Instance  | Secure mapping | DMA security | Description | Configuration |
|--------------|-------------|------------|-----------|----------------|--------------|-------------|---------------|
| 0x00F08000   | APPLICATION | CACHEINFO  | CACHEINFO | S              | NA           | Cache info  |               |

Table 34: Instances

| Register      | Offset | Security | Description                           |
|---------------|--------|----------|---------------------------------------|
| SET[n].WAY[o] | 0x0    |          | Cache information for SET[n], WAY[o]. |

Table 35: Register overview

#### 5.1.4.1.4.1 SET[n].WAY[o] (n=0..255) (o=0..1)

Address offset:  $0x0 + (n \times 0x8) + (o \times 0x4)$

Cache information for SET[n], WAY[o].

| Base address | Domain      | Peripheral | Instance  | Secure mapping | DMA security | Description | Configuration |
|--------------|-------------|------------|-----------|----------------|--------------|-------------|---------------|
| 0x00F00000   | APPLICATION | CACHEDATA  | CACHEDATA | S              | NA           | Cache data  |               |

| Register            | Offset | Security | Description                                 |
|---------------------|--------|----------|---------------------------------------------|
| SET[n].WAY[o].DATA0 | 0x0    |          | Cache data bits [31:0] of SET[n], WAY[o].   |
| SET[n].WAY[o].DATA1 | 0x4    |          | Cache data bits [63:32] of SET[n], WAY[o].  |
| SET[n].WAY[o].DATA2 | 0x8    |          | Cache data bits [95:64] of SET[n], WAY[o].  |
| SET[n].WAY[o].DATA3 | 0xC    |          | Cache data bits [127:96] of SET[n], WAY[o]. |

Cache data bits [31:0] of SET[n], WAY[o].

Cache data bits [63:32] of SET[n], WAY[o].

Address offset:  $0x8 + (o \times 0x10)$

Cache data bits [95:64] of SET[n], WAY[o].

| Bit number       | 31   | 30    | 29    | 28 | 27    | 26          | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------|------|-------|-------|----|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| ID               | A    | A     | A     | A  | A     | A           | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 | 0    | 0     | 0     | 0  | 0     | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce | Field | Value | ID | Value | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW   | Data  |       |    |       | Data        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 5.1.4.1.5.4 SET[n].WAY[o].DATA3 (o=0..1)

Address offset: 0xC + (o × 0x10)

Cache data bits [127:96] of SET[n], WAY[o].

| Bit number       | 31   | 30    | 29    | 28 | 27    | 26          | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------|------|-------|-------|----|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| ID               | A    | A     | A     | A  | A     | A           | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 | 0    | 0     | 0     | 0  | 0     | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce | Field | Value | ID | Value | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW   | Data  |       |    |       | Data        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 5.1.4.2 FICR — Factory information configuration registers

Factory information configuration registers (FICR) are pre-programmed in factory and cannot be erased by the user. These registers contain chip-specific information and configuration.

#### 5.1.4.2.1 Registers

| Base address | Domain      | Peripheral | Instance | Secure mapping | DMA security | Description                                 | Configuration |
|--------------|-------------|------------|----------|----------------|--------------|---------------------------------------------|---------------|
| 0x00FF0000   | APPLICATION | FICR       | FICR     | S              | NA           | Factory information configuration registers |               |

Table 38: Instances

| Register          | Offset | Security | Description                                                                                                              |
|-------------------|--------|----------|--------------------------------------------------------------------------------------------------------------------------|
| INFO.CONFIGID     | 0x200  |          | Configuration identifier                                                                                                 |
| INFO.DEVICEID[n]  | 0x204  |          | Device identifier                                                                                                        |
| INFO.PART         | 0x20C  |          | Part code                                                                                                                |
| INFO.VARIANT      | 0x210  |          | Part Variant, Hardware version and Production configuration                                                              |
| INFO.PACKAGE      | 0x214  |          | Package option                                                                                                           |
| INFO.RAM          | 0x218  |          | RAM variant                                                                                                              |
| INFO.FLASH        | 0x21C  |          | Flash variant                                                                                                            |
| INFO.CODEPAGESIZE | 0x220  |          | Code memory page size in bytes                                                                                           |
| INFO.CODESIZE     | 0x224  |          | Code memory size                                                                                                         |
| INFO.DEVICETYPE   | 0x228  |          | Device type                                                                                                              |
| TRIMCNF[n].ADDR   | 0x300  |          | Address of the PAR register which will be written                                                                        |
| TRIMCNF[n].DATA   | 0x304  |          | Data                                                                                                                     |
| NFC.TAGHEADER0    | 0x450  |          | Default header for NFC Tag. Software can read these values to populate NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST. |
| NFC.TAGHEADER1    | 0x454  |          | Default header for NFC Tag. Software can read these values to populate NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST. |
| NFC.TAGHEADER2    | 0x458  |          | Default header for NFC Tag. Software can read these values to populate NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST. |



| Register         | Offset | Security | Description                                                                                                              |
|------------------|--------|----------|--------------------------------------------------------------------------------------------------------------------------|
| NFC.TAGHEADER3   | 0x45C  |          | Default header for NFC Tag. Software can read these values to populate NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST. |
| TRNG90B.BYTES    | 0xC00  |          | Amount of bytes for the required entropy bits                                                                            |
| TRNG90B.RCCUTOFF | 0xC04  |          | Repetition counter cutoff                                                                                                |
| TRNG90B.APCUTOFF | 0xC08  |          | Adaptive proportion cutoff                                                                                               |
| TRNG90B.STARTUP  | 0xC0C  |          | Amount of bytes for the startup tests                                                                                    |
| TRNG90B.ROSC1    | 0xC10  |          | Sample count for ring oscillator 1                                                                                       |
| TRNG90B.ROSC2    | 0xC14  |          | Sample count for ring oscillator 2                                                                                       |
| TRNG90B.ROSC3    | 0xC18  |          | Sample count for ring oscillator 3                                                                                       |
| TRNG90B.ROSC4    | 0xC1C  |          | Sample count for ring oscillator 4                                                                                       |
| XOSC32MTRIM      | 0xC20  |          | XOSC32M capacitor selection trim values                                                                                  |

Table 39: Register overview

## 5.1.4.2.1.1 INFO.CONFIGID

Address offset: 0x200

Configuration identifier

|                  |      |       |       |    |       |                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------|-------|-------|----|-------|----------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |      |       |       |    | 31    | 30                               | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |      |       |       |    |       |                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A | A | A |
| Reset 0xFFFFFFFF |      |       |       |    | 1     | 1                                | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |   |
| ID               | Acce | Field | Value | ID | Value | Description                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | R    | HWID  |       |    |       | Identification number for the HW |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

## 5.1.4.2.1.2 INFO.DEVICEID[n] (n=0..1)

Address offset: 0x204 + (n × 0x4)

Device identifier

|                  |      |          |       |    |       |                                                                                                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------|----------|-------|----|-------|----------------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |      |          |       | 31 | 30    | 29                                                                                                                                                 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |      |          |       | A  | A     | A                                                                                                                                                  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0xFFFFFFFF |      |          |       | 1  | 1     | 1                                                                                                                                                  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ID               | Acce | Field    | Value | ID | Value | Description                                                                                                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | R    | DEVICEID |       |    |       | 64 bit unique device identifier                                                                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |          |       |    |       | DEVICEID[0] contains the least significant bits of the device identifier. DEVICEID[1] contains the most significant bits of the device identifier. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

## 5.1.4.2.1.3 INFO.PART

Address offset: 0x20C

Part code

|                  |            |      |          |             |            |    |    |           |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|------|----------|-------------|------------|----|----|-----------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |      |          |             | 31         | 30 | 29 | 28        | 27          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |      |          |             | A          | A  | A  | A         | A           | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |   |
| Reset 0x00005340 |            |      |          |             | 0          | 0  | 0  | 0         | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 1  | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |      | Value ID |             | Value      |    |    |           | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | R          | PART |          |             |            |    |    | Part code |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |      |          | N5340       | 0x5340     |    |    |           | nRF5340     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |      |          | Unspecified | 0xFFFFFFFF |    |    |           | Unspecified |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |



| Bit number       |      |       | 31          | 30 | 29         | 28              | 27            | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------|------|-------|-------------|----|------------|-----------------|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| ID               |      |       | A           | A  | A          | A               | A             | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0xFFFFFFFF |      |       | 1           | 1  | 1          | 1               | 1             | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ID               | Acce | Field | Value ID    |    | Value      |                 | Description   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | R    | FLASH |             |    |            |                 | Flash variant |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |       | K128        |    | 0x80       | 128 kByte FLASH |               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |       | K256        |    | 0x100      | 256 kByte FLASH |               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |       | K512        |    | 0x200      | 512 kByte FLASH |               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |       | K1024       |    | 0x400      | 1 MByte FLASH   |               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |       | K2048       |    | 0x800      | 2 MByte FLASH   |               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |       | Unspecified |    | 0xFFFFFFFF | Unspecified     |               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 5.1.4.2.1.8 INFO.CODEPAGESIZE

Address offset: 0x220

Code memory page size in bytes

|                  |            |              |          |        |       |  |  |  |                                |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------------|----------|--------|-------|--|--|--|--------------------------------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |              |          |        |       |  |  |  |                                | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |              |          |        |       |  |  |  |                                | A           | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A | A |   |
| Reset 0x00001000 |            |              |          |        |       |  |  |  |                                | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |              | Value ID |        | Value |  |  |  |                                | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | R          | CODEPAGESIZE |          |        |       |  |  |  | Code memory page size in bytes |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |              | K4096    | 0x1000 |       |  |  |  | 4 kByte                        |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

#### 5.1.4.2.1.9 INFO.CODESIZE

Address offset: 0x224

Code memory size

| Bit number       |            |          |          |      |       |  |             |                                                    |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
|------------------|------------|----------|----------|------|-------|--|-------------|----------------------------------------------------|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ID               |            |          |          |      |       |  |             |                                                    |  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000100 |            |          |          |      |       |  |             |                                                    |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |          | Value ID |      | Value |  | Description |                                                    |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | R          | CODESIZE |          |      |       |  |             | Code memory size in number of pages                |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |          |          |      |       |  |             | Total code space is: CODEPAGESIZE * CODESIZE bytes |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |          |          | P256 | 256   |  | 256 pages   |                                                    |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 5.1.4.2.1.10 INFO.DEVICETYPE

Address offset: 0x228

Device type

|                  |            |            |          |            |    |    |    |                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|------------|----------|------------|----|----|----|---------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |            |          | 31         | 30 | 29 | 28 | 27                        | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |            |          | A          | A  | A  | A  | A                         | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |            |          | 0          | 0  | 0  | 0  | 0                         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |            | Value ID | Value      |    |    |    | Description               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | R          | DEVICETYPE |          |            |    |    |    | Device type               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |            | Die      | 0x00000000 |    |    |    | Device is an physical DIE |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |            | FPGA     | 0xFFFFFFFF |    |    |    | Device is an FPGA         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 5.1.4.2.1.11 TRIMCNF[n].ADDR (n=0..31)

Address offset:  $0x300 + (n \times 0x8)$

Address of the PAR register which will be written

|                  |            |         |          |         |    |    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|---------|----------|---------|----|----|----|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |         |          | 31      | 30 | 29 | 28 | 27          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |         |          | A       | A  | A  | A  | A           | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0xFFFFFFFF |            |         |          | 1       | 1  | 1  | 1  | 1           | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ID               | Acce Field |         | Value ID | Value   |    |    |    | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | Address |          | Address |    |    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 5.1.4.2.1.12 TRIMCNF[n].DATA (n=0..31)

Address offset:  $0x304 + (n \times 0x8)$

Data

| Bit number       |            |      |          | 31                                       | 30 | 29 | 28 | 27          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------|------------|------|----------|------------------------------------------|----|----|----|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| ID               |            |      |          | A                                        | A  | A  | A  | A           | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0xFFFFFFFF |            |      |          | 1                                        | 1  | 1  | 1  | 1           | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ID               | Acce Field |      | Value ID | Value                                    |    |    |    | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | R          | Data |          | Data to be written into the PAR register |    |    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 5.1.4.2.1.13 NFC.TAGHEADER0

Address offset: 0x450

Default header for NFC Tag. Software can read these values to populate NFCID1\_3RD\_LAST, NFCID1\_2ND\_LAST and NFCID1\_LAST.

|                 |            |       |          |  |       |  |  |  |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|-----------------|------------|-------|----------|--|-------|--|--|--|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number      |            |       |          |  |       |  |  |  | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID              |            |       |          |  |       |  |  |  | D D D D D D D D C C C C C C C C B B B B B B B B A A A A A A A A                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0xFFFFF5F |            |       |          |  |       |  |  |  | 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 0 1 1 1 1 1                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID              | Acce Field |       | Value ID |  | Value |  |  |  | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A               | R          | MFGID |          |  |       |  |  |  | Default Manufacturer ID: Nordic Semiconductor ASA has ICM 0x5F                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B               | R          | UD1   |          |  |       |  |  |  | Unique identifier byte 1                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C               | R          | UD2   |          |  |       |  |  |  | Unique identifier byte 2                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| D               | R          | UD3   |          |  |       |  |  |  | Unique identifier byte 3                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

#### 5.1.4.2.1.14 NFC.TAGHEADER1

Address offset: 0x454

Default header for NFC Tag. Software can read these values to populate NFCID1\_3RD\_LAST, NFCID1\_2ND\_LAST and NFCID1\_LAST.

|                  |      |                |       |    |       |                          |    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------|----------------|-------|----|-------|--------------------------|----|----|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |      |                |       | 31 | 30    | 29                       | 28 | 27 | 26          | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |      |                |       | D  | D     | D                        | D  | D  | D           | D  | C  | C  | C  | C  | C  | C  | C  | B  | B  | B  | B  | B  | B  | B  | B  | B | A | A | A | A | A | A | A | A | A |
| Reset 0xFFFFFFFF |      |                |       | 1  | 1     | 1                        | 1  | 1  | 1           | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ID               | Acce | Field          | Value | ID | Value |                          |    |    | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A-D              | R    | UD[i] (i=4..7) |       |    |       | Unique identifier byte i |    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 5.1.4.2.1.15 NFC.TAGHEADER2

Address offset: 0x458

Default header for NFC Tag. Software can read these values to populate NFCID1\_3RD\_LAST, NFCID1\_2ND\_LAST and NFCID1\_LAST.

|                  |            |                 |          |       |    |                          |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-----------------|----------|-------|----|--------------------------|----|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                 |          | 31    | 30 | 29                       | 28 | 27          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |                 |          | D     | D  | D                        | D  | D           | D  | D  | D  | C  | C  | C  | C  | C  | C  | C  | B  | B  | B  | B  | B  | B  | B  | B | A | A | A | A | A | A | A | A | A |
| Reset 0xFFFFFFFF |            |                 |          | 1     | 1  | 1                        | 1  | 1           | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ID               | Acce Field |                 | Value ID | Value |    |                          |    | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A-D              | R          | UD[i] (i=8..11) |          |       |    | Unique identifier byte i |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 5.1.4.2.1.16 NFC.TAGHEADER3

Address offset: 0x45C

Default header for NFC Tag. Software can read these values to populate NFCID1\_3RD\_LAST, NFCID1\_2ND\_LAST and NFCID1\_LAST.

|                  |            |                  |          |  |                          |       |  |  |  |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|------------------|----------|--|--------------------------|-------|--|--|--|----|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                  |          |  |                          |       |  |  |  | 31 | 30          | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |                  |          |  |                          |       |  |  |  | D  | D           | D  | D  | D  | D  | D  | D  | C  | C  | C  | C  | C  | C  | C  | B  | B  | B  | B  | B  | B  | B  | B | B | A | A | A | A | A | A | A | A | A |   |
| Reset 0xFFFFFFFF |            |                  |          |  |                          |       |  |  |  | 1  | 1           | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ID               | Acce Field |                  | Value ID |  |                          | Value |  |  |  |    | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A-D              | R          | UD[i] (i=12..15) |          |  | Unique identifier byte i |       |  |  |  |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

#### 5.1.4.2.1.17 TRNG90B.BYTES

Address offset: 0xC00

Amount of bytes for the required entropy bits

|                  |            |       |          |  |       |  |  |                                               |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-------|----------|--|-------|--|--|-----------------------------------------------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |       |          |  |       |  |  | 31                                            | 30          | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |       |          |  |       |  |  | A                                             | A           | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A | A |   |
| Reset 0x00000210 |            |       |          |  |       |  |  | 0                                             | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |       | Value ID |  | Value |  |  |                                               | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | R          | BYTES |          |  |       |  |  | Amount of bytes for the required entropy bits |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

#### 5.1.4.2.1.18 TRNG90B.RCCUTOFF

Address offset: 0xC04

Repetition counter cutoff

|                  |            |          |          |       |    |    |    |                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|-------|----|----|----|---------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31    | 30 | 29 | 28 | 27                        | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |          |          | A     | A  | A  | A  | A                         | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0xFFFFFFFF |            |          |          | 1     | 1  | 1  | 1  | 1                         | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ID               | Acce Field |          | Value ID | Value |    |    |    | Description               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | R          | RCCUTOFF |          |       |    |    |    | Repetition counter cutoff |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 5.1.4.2.1.19 TRNG90B.APCUTOFF

Address offset: 0xC08

Adaptive proportion cutoff

|                  |            |          |          |       |    |    |    |                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|-------|----|----|----|----------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31    | 30 | 29 | 28 | 27                         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |          |          | A     | A  | A  | A  | A                          | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0xFFFFFFFF |            |          |          | 1     | 1  | 1  | 1  | 1                          | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ID               | Acce Field |          | Value ID | Value |    |    |    | Description                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | R          | APCUTOFF |          |       |    |    |    | Adaptive proportion cutoff |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 5.1.4.2.1.20 TRNG90B.STARTUP

Address offset: 0xC0C

Amount of bytes for the startup tests

|                  |            |         |          |       |    |    |    |                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|---------|----------|-------|----|----|----|---------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |         |          | 31    | 30 | 29 | 28 | 27                                    | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |         |          | A     | A  | A  | A  | A                                     | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0xFFFFFFFF |            |         |          | 1     | 1  | 1  | 1  | 1                                     | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ID               | Acce Field |         | Value ID | Value |    |    |    | Description                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | R          | STARTUP |          |       |    |    |    | Amount of bytes for the startup tests |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 5.1.4.2.1.21 TRNG90B.ROSC1

Address offset: 0xC10

Sample count for ring oscillator 1

|                  |            |       |          |       |    |    |    |                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-------|----------|-------|----|----|----|------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |       |          | 31    | 30 | 29 | 28 | 27                                 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |       |          | A     | A  | A  | A  | A                                  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0xFFFFFFFF |            |       |          | 1     | 1  | 1  | 1  | 1                                  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ID               | Acce Field |       | Value ID | Value |    |    |    | Description                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | R          | ROSC1 |          |       |    |    |    | Sample count for ring oscillator 1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 5.1.4.2.1.22 TRNG90B.ROSC2

Address offset: 0xC14

Sample count for ring oscillator 2

|                  |            |       |          |                                                                                       |  |  |  |  |  |  |  |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|-------|----------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |       |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |       |          | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A           |  |  |  |  |  |  |  |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0xFFFFFFFF |            |       |          | 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1                   |  |  |  |  |  |  |  |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field |       | Value ID | Value                                                                                 |  |  |  |  |  |  |  | Description                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | R          | ROSC2 |          |                                                                                       |  |  |  |  |  |  |  | Sample count for ring oscillator 2 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

#### 5.1.4.2.1.23 TRNG90B.ROSC3

Address offset: 0xC18

Sample count for ring oscillator 3

|                  |            |       |  |          |  |  |       |  |  |             |                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-------|--|----------|--|--|-------|--|--|-------------|------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |       |  |          |  |  |       |  |  | 31          | 30                                 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |       |  |          |  |  |       |  |  | A           | A                                  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A | A | A |   |
| Reset 0xFFFFFFFF |            |       |  |          |  |  |       |  |  | 1           | 1                                  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ID               | Acce Field |       |  | Value ID |  |  | Value |  |  | Description |                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | R          | ROSC3 |  |          |  |  |       |  |  |             | Sample count for ring oscillator 3 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 5.1.4.2.1.24 TRNG90B.ROSC4

Address offset: 0xC1C

Sample count for ring oscillator 4

|                  |            |       |          |  |       |    |    |    |                                    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-------|----------|--|-------|----|----|----|------------------------------------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |       |          |  | 31    | 30 | 29 | 28 | 27                                 | 26          | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |       |          |  | A     | A  | A  | A  | A                                  | A           | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0xFFFFFFFF |            |       |          |  | 1     | 1  | 1  | 1  | 1                                  | 1           | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ID               | Acce Field |       | Value ID |  | Value |    |    |    |                                    | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | R          | ROSC4 |          |  |       |    |    |    | Sample count for ring oscillator 4 |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 5.1.4.2.1.25 XOSC32MTRIM

Address offset: 0xC20

XOSC32M capacitor selection trim values

To enable the optional internal capacitors on XC1 and XC2 pins, see to the "Using internal capacitors" section of the OSCILLATORS chapter.

|                  |      |        |           |                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |
|------------------|------|--------|-----------|-------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|
| Bit number       |      |        |           |                                           | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |
| ID               |      |        |           |                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   | B | B | B | B | B | A | A | A | A | A |  |
| Reset 0xFFFFFFFF |      |        |           |                                           | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |   |  |
| ID               | Acce | Field  | Value     | ID                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |
| A                | R    | SLOPE  | [-16..15] | Slope trim factor on twos complement form |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |        |           | -16: Minimum slope                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |        |           | 15: Maximum slope                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |
| B                | R    | OFFSET | [31..0]   | Offset trim factor on integer form        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |        |           | 0: Minimum offset                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |        |           | 31: Maximum offset                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |

### 5.1.4.3 UICR — User information configuration registers

The user information configuration registers (UICRs) are non-volatile memory (NVM) registers for configuring user specific settings and storing secure cryptographic keys or OTP values.

The cryptographic key part of the UICR (addresses starting at 0x100 and higher) is handled by the Key Management Unit (KMU), see [KMU — Key management unit](#) on page 258 for more information.

For information on writing registers, see [NVMC — Non-volatile memory controller](#) on page 318 and [Memory](#) on page 18.

#### 5.1.4.3.1 Registers

| Base address | Domain      | Peripheral | Instance | Secure mapping | DMA security | Description                              | Configuration |
|--------------|-------------|------------|----------|----------------|--------------|------------------------------------------|---------------|
| 0x00FF8000   | APPLICATION | UICR       | UICR     | S              | NA           | User information configuration registers |               |

Table 40: Instances

| Register  | Offset | Security | Description            |
|-----------|--------|----------|------------------------|
| APPROTECT | 0x000  |          | Access port protection |

| Register                | Offset | Security | Description                                                                                                                                                                                                                                                                                               |
|-------------------------|--------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| EXTSUPPLY               | 0x00C  |          | Enable external circuitry to be supplied from VDD pin. Applicable in 'High voltage mode' only.                                                                                                                                                                                                            |
| VREGHVOUT               | 0x010  |          | GPIO reference voltage / external output supply voltage in 'High voltage mode'.                                                                                                                                                                                                                           |
| HFXOCNT                 | 0x014  |          | HFXO startup counter                                                                                                                                                                                                                                                                                      |
| SECUREAPPROTECT         | 0x01C  |          | Secure access port protection                                                                                                                                                                                                                                                                             |
| ERASEPROTECT            | 0x020  |          | Erase protection                                                                                                                                                                                                                                                                                          |
| TINSTANCE               | 0x024  |          | SW-DP Target instance                                                                                                                                                                                                                                                                                     |
| NFCPINS                 | 0x028  |          | Setting of pins dedicated to NFC functionality: NFC antenna or GPIO                                                                                                                                                                                                                                       |
| OTP[n]                  | 0x100  |          | One time programmable memory                                                                                                                                                                                                                                                                              |
| KEYSLOT.CONFIG[n].DEST  | 0x400  |          | Destination address where content of the key value registers (KEYSLOT.KEYn.VALUE[0-3]) will be pushed by KMU. Note that this address must match that of a peripherals APB mapped write-only key registers, else the KMU can push this key value into an address range which the CPU can potentially read. |
| KEYSLOT.CONFIG[n].PERM  | 0x404  |          | Define permissions for the key slot. Bits 0-15 and 16-31 can only be written when equal to 0xFFFF.                                                                                                                                                                                                        |
| KEYSLOT.KEY[n].VALUE[o] | 0x800  |          | Define bits [31+o*32:0+o*32] of value assigned to KMU key slot.                                                                                                                                                                                                                                           |

Table 41: Register overview

#### 5.1.4.3.1.1 APPROTECT

Address offset: 0x000

Access port protection

|                  |      |       |             |    |            |                                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|------------------|------|-------|-------------|----|------------|------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|
| Bit number       |      |       |             | 31 | 30         | 29                                                                                 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |
| ID               |      |       |             | A  | A          | A                                                                                  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |  |  |  |
| Reset 0x00000000 |      |       |             | 0  | 0          | 0                                                                                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |
| ID               | Acce | Field | Value       | ID | Value      | Description                                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
| A                | RW   | PALL  |             |    |            | Blocks debugger read/write access to all CPU registers and memory mapped addresses |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |       |             |    |            | Using any value not listed below will yield unexpected results.                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |       | Unprotected |    | 0xFFFFFFFF | Unprotected                                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |       | Protected   |    | 0x00000000 | Protected                                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |

#### 5.1.4.3.1.2 EXTSUPPLY

Address offset: 0x00C

Enable external circuitry to be supplied from VDD pin. Applicable in 'High voltage mode' only.

| Bit number       |            |           |          | 31 | 30                                                           | 29                                                                             | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |  |
|------------------|------------|-----------|----------|----|--------------------------------------------------------------|--------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|--|--|
| ID               |            |           |          | A  |                                                              |                                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |
| Reset 0xFFFFFFFF |            |           |          | 1  | 1                                                            | 1                                                                              | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  |  |  |  |  |
| ID               | Acce Field |           | Value    | ID | Value                                                        | Description                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |
| A                | RW         | EXTSUPPLY |          |    |                                                              | Enable external circuitry to be supplied from VDD pin (output of VREGH stage). |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |
|                  |            |           | Disabled | 1  | No current can be drawn from the VDD pin.                    |                                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |
|                  |            |           | Enabled  | 0  | It is allowed to supply external circuitry from the VDD pin. |                                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |

#### 5.1.4.3.1.3 VREGHVOUT

Address offset: 0x010





## Erase protection

| Bit number       |      |       |             | 31         | 30 | 29 | 28                                                              | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |
|------------------|------|-------|-------------|------------|----|----|-----------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|
| ID               |      |       |             | A          | A  | A  | A                                                               | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |  |  |  |
| Reset 0x00000000 |      |       |             | 0          | 0  | 0  | 0                                                               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |
| ID               | Acce | Field | Value ID    | Value      |    |    | Description                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
| A                | RW   | PALL  |             |            |    |    | Blocks NVMC ERASEALL and CTRLAP ERASEALL functionality.         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |       |             |            |    |    | Using any value not listed below will yield unexpected results. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |       | Unprotected | 0xFFFFFFFF |    |    | Unprotected                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |       | Protected   | 0x00000000 |    |    | Protected                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |

## 5.1.4.3.1.7 TINSTANCE

Address offset: 0x024

SW-DP Target instance

|                  |            |           |                                                                                       |  |  |  |  |  |  |  |                                                                                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|-----------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |           | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |                                                                                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |           | A A A A                                                                               |  |  |  |  |  |  |  |                                                                                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0xFFFFFFFF |            |           | 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1                   |  |  |  |  |  |  |  |                                                                                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID  | Value                                                                                 |  |  |  |  |  |  |  | Description                                                                                                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | TINSTANCE |                                                                                       |  |  |  |  |  |  |  | TINSTANCE bits are negated and used in the SW-DP DLPIDR.TINSTANCE field.<br><br>E.g. 0xF in this field is translated to 0x0 in DLPIDR.TINSTANCE field. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

## 5.1.4.3.1.8 NFCPINS

Address offset: 0x028

Setting of pins dedicated to NFC functionality: NFC antenna or GPIO

When used as NFC antenna pin, the corresponding pin must be controlled by the application core, and the GPIO PIN\_CNF register initialized to its reset value.

|                  |            |          |       |    |                                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |
|------------------|------------|----------|-------|----|----------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|--|--|
| Bit number       |            |          | 31    | 30 | 29                                                                         | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |  |
| ID               |            |          | A     |    |                                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |
| Reset 0xFFFFFFFF |            |          | 1     | 1  | 1                                                                          | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value |    | Description                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |
| A                | RW         | PROTECT  |       |    | Setting of pins dedicated to NFC functionality                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |
|                  |            | Disabled | 0     |    | Operation as GPIO pins. Same protection as normal GPIO pins                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |
|                  |            | NFC      | 1     |    | Operation as NFC antenna pins. Configures the protection for NFC operation |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |

## 5.1.4.3.1.9 OTP[n] (n=0..191)

Address offset: 0x100 + (n × 0x4)

One time programmable memory

| Bit number       |            | 31       | 30 | 29    | 28 | 27                                                           | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------|------------|----------|----|-------|----|--------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| ID               |            | B        | B  | B     | B  | B                                                            | B  | B  | B  | B  | B  | B  | B  | B  | B  | B  | B  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0xFFFFFFFF |            | 1        | 1  | 1     | 1  | 1                                                            | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |   |
| ID               | Acce Field | Value ID |    | Value |    | Description                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW1 LOWER  |          |    |       |    | Lower half word                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |          |    |       |    | <b>Note:</b> Can only be written to a non 0xFFFF value once. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| B                | RW1 UPPER  |          |    |       |    | Upper half word                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |          |    |       |    | <b>Note:</b> Can only be written to a non 0xFFFF value once. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 5.1.4.3.1.10 KEYSLOT.CONFIG[n].DEST (n=0..127)

Address offset:  $0x400 + (n \times 0x8)$

Destination address where content of the key value registers (KEYSLOT.KEYn.VALUE[0-3]) will be pushed by KMU. Note that this address must match that of a peripherals APB mapped write-only key registers, else the KMU can push this key value into an address range which the CPU can potentially read.

Writing/reading this register requires the KMU SELECTKEYSLOT register to be set to n+1.

|                  |             |          |       |    |    |    |                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|-------------|----------|-------|----|----|----|--------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |             |          | 31    | 30 | 29 | 28 | 27                             | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |             |          | A     | A  | A  | A  | A                              | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0xFFFFFFFF |             |          | 1     | 1  | 1  | 1  | 1                              | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ID               | Acces Field | Value ID | Value |    |    |    | Description                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW DEST     |          |       |    |    |    | Secure APB destination address |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 5.1.4.3.1.11 KEYSLOT.CONFIG[n].PERM (n=0..127)

Address offset:  $0x404 + (n \times 0x8)$

Define permissions for the key slot. Bits 0-15 and 16-31 can only be written when equal to 0xFFFF.

Writing/reading this register requires the KMU SELECTKEYSLOT register to be set to n+1.

| Bit number       |      |       | 31       | 30 | 29 | 28                                                                                                                                   | 27 | 26                            | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
|------------------|------|-------|----------|----|----|--------------------------------------------------------------------------------------------------------------------------------------|----|-------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| ID               |      |       | D        |    |    |                                                                                                                                      |    |                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | C | B | A |   |  |
| Reset 0xFFFFFFFF |      |       | 1        | 1  | 1  | 1                                                                                                                                    | 1  | 1                             | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  |
| ID               | Acce | Field | Value    |    | ID | Value                                                                                                                                |    | Description                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| A                | RW   | WRITE |          |    |    |                                                                                                                                      |    | Write permission for key slot |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |       | Disabled |    | 0  | Disable write to the key value registers                                                                                             |    |                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |       | Enabled  |    | 1  | Enable write to the key value registers                                                                                              |    |                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| B                | RW   | READ  |          |    |    |                                                                                                                                      |    | Read permission for key slot  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |       | Disabled |    | 0  | Disable read from key value registers                                                                                                |    |                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |       | Enabled  |    | 1  | Enable read from key value registers                                                                                                 |    |                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| C                | RW   | PUSH  |          |    |    |                                                                                                                                      |    | Push permission for key slot  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |       | Disabled |    | 0  | Disable pushing of key value registers over secure APB, but<br>can be read if field READ is Enabled                                  |    |                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |       | Enabled  |    | 1  | Enable pushing of key value registers over secure APB.<br>Register KEYSLOT.CONFIGn.DEST must contain a valid<br>destination address! |    |                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

|                  |      |       |                                                                                       |  |    |       |  |                                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|-------|---------------------------------------------------------------------------------------|--|----|-------|--|----------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |    |       |  |                                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |       | D C B A                                                                               |  |    |       |  |                                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0xFFFFFFFF |      |       | 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1                       |  |    |       |  |                                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field | Value                                                                                 |  | ID | Value |  | Description                                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| D                | RW   | STATE |                                                                                       |  |    |       |  | Revocation state for the key slot                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       |                                                                                       |  |    |       |  | Note that it is not possible to undo a key revocation by writing the value '1' to this field |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Revoked                                                                               |  | 0  |       |  | Key value registers can no longer be read or pushed                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Active                                                                                |  | 1  |       |  | Key value registers are readable (if enabled) and can be pushed (if enabled)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

#### 5.1.4.3.1.12 KEYSLOT.KEY[n].VALUE[o] (n=0..127) (o=0..3)

Address offset:  $0x800 + (n \times 0x10) + (o \times 0x4)$

Define bits  $[31+o*32:0+o*32]$  of value assigned to KMU key slot.

Writing/reading this register requires the KMU SELECTKEYSLOT register to be set to n+1.

|                  |            |          |       |    |    |    |                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|------------------|------------|----------|-------|----|----|----|----------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|
| Bit number       |            |          | 31    | 30 | 29 | 28 | 27                                                             | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |
| ID               |            |          | A     | A  | A  | A  | A                                                              | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |  |  |  |
| Reset 0xFFFFFFFF |            |          | 1     | 1  | 1  | 1  | 1                                                              | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  |  |  |
| ID               | Acce Field | Value ID | Value |    |    |    | Description                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
| A                | RW         | VALUE    |       |    |    |    | Define bits [31+o*32:0+o*32] of value assigned to KMU key slot |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |

### 5.1.4.4 AHB multilayer

AHB multilayer enables parallel access paths between multiple masters and slaves in a system. Access is resolved using priorities.

Each bus master is connected to a slave device through one or more interconnection matrixes. The bus masters are assigned priorities that are used to resolve access when two (or more) bus masters request access to the same slave device. The following applies when assigning priorities:

- If two (or more) bus masters request access to the same slave device, the master with the highest priority is granted access first.
- Bus masters with lower priority are stalled until the higher priority master has completed its transaction.
- If the higher priority master pauses at any point during its transaction, the lower priority master in queue is temporarily granted access to the slave device until the higher priority master resumes its activity.
- Bus masters that have the same priority are mutually exclusive, and cannot be used concurrently.

Some peripherals, like I2S, do not have a safe stalling mechanism (not able to pause incoming data and no internal data buffering). Being a low priority bus master might cause loss of data for such peripherals upon bus contention. To avoid AHB bus contention when using multiple bus masters, apply one of the following guidelines:

- Avoid situations where more than one bus master is accessing the same slave.
- If more than one bus master is accessing the same slave, make sure that the bus bandwidth is not exhausted.

#### 5.1.4.4.1 AHB multilayer priorities

Each master connected to the AHB multilayer is assigned a default natural priority.

| Bus master name | Natural relative priority | In/Out | Description                                   |
|-----------------|---------------------------|--------|-----------------------------------------------|
| CPU             | Highest priority          | I/O    |                                               |
| QSPI            |                           | I/O    |                                               |
| SERIAL0         |                           | I/O    | Applies to UARTE0, SPIM0, SPIS0, TWIM0, TWIS0 |
| SERIAL1         |                           | I/O    | Applies to UARTE1, SPIM1, SPIS1, TWIM1, TWIS1 |
| SPIM2           |                           | I/O    |                                               |
| SAADC           |                           | I      |                                               |
| PWM             |                           | O      | Applies to PWM0, PWM1, PWM2                   |
| External core   | Lowest priority           | I/O    | Applies to network core                       |

Table 42: AHB bus masters

# 6.1 Network core

## 6.1.1 Network core overview

The network core contains a low-power microcontroller with embedded flash memory and an Arm Cortex-M33 processor.

The network core includes peripherals for efficient implementation of radio protocols such as Bluetooth Low Energy, 802.15.4, and proprietary 2.4 GHz. The following figure provides more information. Arrows with white heads indicate signals that share physical pins with other signals.



## 6.1.2 CPU

The Arm Cortex-M33 processor has a 32-bit instruction set (Thumb-2 technology) that implements a superset of 16- and 32-bit instructions to maximize code density and performance.

This processor implements several features that enable energy-efficient arithmetic and high-performance signal processing including:

- Hardware divide
- 8- and 16-bit single instruction multiple data (SIMD) instructions
- Memory Protection Unit (MPU)

The [Arm Cortex Microcontroller Software Interface Standard \(CMSIS\)](#) is implemented and available for the application processor.

Real-time execution is highly deterministic in thread mode, to and from sleep modes, and when handling events at configurable priority levels via the Nested Vectored Interrupt Controller (NVIC).

Executing code from internal or external flash will have a wait state penalty. The instruction cache can be enabled to minimize flash wait states when fetching instructions. For more information on cache, see [NVMC — Non-volatile memory controller](#) on page 318. CPU performance parameters including mode wait states, CPU current and efficiency, and processing power and efficiency based on the CoreMark benchmark can be found in .

### 6.1.2.1 Electrical specification

#### 6.1.2.1.1 CPU performance

| Symbol                  | Description                                                    | Min. | Typ. | Max. | Units                   |
|-------------------------|----------------------------------------------------------------|------|------|------|-------------------------|
| W <sub>FLASH</sub>      | CPU wait states, running from flash, cache disabled            | ..   | ..   | ..   |                         |
| W <sub>FLASHCACHE</sub> | CPU wait states, running from flash, cache enabled             | ..   | ..   | ..   |                         |
| W <sub>RAM</sub>        | CPU wait states, running from RAM                              | ..   | ..   | ..   |                         |
| CM <sub>FLASH</sub>     | CoreMark <sup>10</sup> , running from flash, cache enabled     |      | 238  |      | Core <sup>®</sup>       |
| CM <sub>FLASH/MHz</sub> | CoreMark per MHz, running from flash, cache enabled            |      | 3.7  |      | CoreMark/<br>MHz        |
| CM <sub>FLASH/mA</sub>  | CoreMark per mA, running from flash, cache enabled, DCDC<br>3V |      | 101  |      | Core <sup>®</sup><br>mA |

### 6.1.2.2 CPU and support module configuration

The Arm Cortex-M33 processor has a number of CPU options and support modules implemented on the device.

<sup>10</sup> Using ARM compiler



| Option/Module     | Description                                   | Implemented                                          |
|-------------------|-----------------------------------------------|------------------------------------------------------|
| Core options      |                                               |                                                      |
| PRIORITIES        | Priority bits                                 | 3                                                    |
| WIC               | Wakeup Interrupt Controller                   | NO                                                   |
| Endianness        | Memory system endianness                      | Little endian                                        |
| DWT               | Data Watchpoint and Trace                     | YES                                                  |
| Modules           |                                               |                                                      |
| MPU_NS            | Number of non-secure MPU regions              | 8                                                    |
| MPU_S             | Number of secure MPU regions                  | 0 (No ARMv8-M Security Extensions)                   |
| SAU               | Number of SAU regions                         | 0 (No Arm TrustZone for Armv8-M Security Extensions) |
| FPU               | Floating-point unit                           | NO                                                   |
| DSP               | Digital Signal Processing Extension           | NO                                                   |
| ARMv8-M TrustZone | Arm TrustZone for Armv8-M Security Extensions | NO                                                   |
| CPIF              | Coprocessor interface                         | NO                                                   |
| ETM               | Embedded Trace Macrocell                      | NO                                                   |
| ITM               | Instrumentation Trace Macrocell               | NO                                                   |
| MTB               | Micro Trace Buffer                            | NO                                                   |
| CTI               | Cross Trigger Interface                       | YES                                                  |
| BPU               | Breakpoint Unit                               | YES                                                  |
| HTM               | AHB Trace Macrocell                           | NO                                                   |

### 6.1.3 Memory

The network core contains flash memory and RAM that can be used for code and data storage.

The following figure shows how the CPU and peripherals with EasyDMA can access RAM via the AHB multilayer interconnect.

The network core can access application core resources (flash, RAM, and peripherals) when granted permission through the application's DCNF and SPU settings. A small portion of the application core RAM is dedicated to the exchange of messages between the application and network cores.

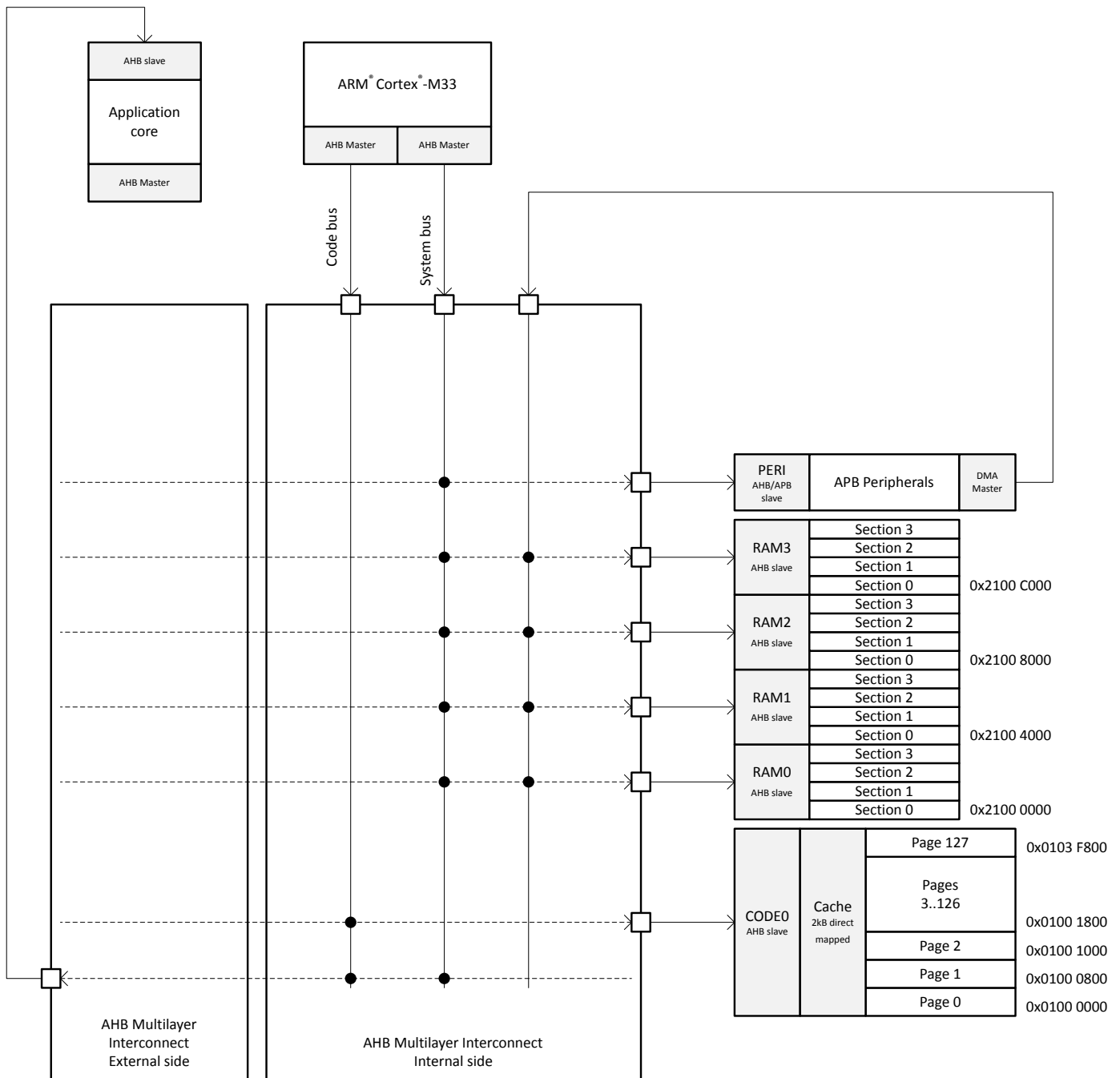


Figure 27: Memory layout

### 6.1.3.1 Peripheral instantiation

The following table describes the abbreviations used in the Instance, Secure mapping, and DMA security columns of the instantiation table.

| Abbreviation | Description                                                                                                                               |
|--------------|-------------------------------------------------------------------------------------------------------------------------------------------|
| NS           | Non-secure - Peripheral is always accessible as a Non-Secure peripheral                                                                   |
| S            | Secure - Peripheral is always accessible as a Secure peripheral                                                                           |
| US           | User Selectable - A Secure or Non-secure attribute for the peripheral is defined in the SPU                                               |
| SPLIT        | Both Secure and Non-secure - The same resource is shared by both secure and non-secure code                                               |
| NA           | Not Applicable - Peripheral has no DMA capability                                                                                         |
| NSA          | NoSeparateAttribute - Peripheral with DMA and DMA transfer has the same security attribute as assigned to the peripheral                  |
| SA           | SeparateAttribute - Peripheral with DMA and DMA transfers can have a different security attribute than the one assigned to the peripheral |

Table 43: Instantiation table abbreviations

The Secure mapping column in the following table defines configuration capabilities for the Arm TrustZone for Armv8-M secure attribute. The DMA security column describes the DMA capabilities of the peripheral.

### 6.1.3.2 Instantiation

| ID | Base address | Peripheral | Instance | Secure mapping | DMA security | Description                                 |
|----|--------------|------------|----------|----------------|--------------|---------------------------------------------|
| 0  | 0x41000000   | DCNF       | DCNF     | NS             | NA           | Domain configuration                        |
| 4  | 0x41004000   | VREQCTRL   | VREQCTRL | NS             | NA           | Voltage request control                     |
| 5  | 0x41005000   | CLOCK      | CLOCK    | NS             | NA           | Clock control                               |
| 5  | 0x41005000   | POWER      | POWER    | NS             | NA           | Power control                               |
| 5  | 0x41005000   | RESET      | RESET    | NS             | NA           | Reset status                                |
| 6  | 0x41006000   | CTRLAPPERI | CTRLAP   | NS             | NA           | Control access port CPU side                |
| 8  | 0x41008000   | RADIO      | RADIO    | NS             | NA           | 2.4 GHz radio                               |
| 9  | 0x41009000   | RNG        | RNG      | NS             | NA           | Random number generator                     |
| 10 | 0x4100A000   | GPIO       | GPIO     | NS             | NA           | GPIO tasks and events                       |
| 11 | 0x4100B000   | WDT        | WDT      | NS             | NA           | Watchdog timer                              |
| 12 | 0x4100C000   | TIMER      | TIMER0   | NS             | NA           | Timer 0                                     |
| 13 | 0x4100D000   | ECB        | ECB      | NS             | NA           | AES ECB mode encryption                     |
| 14 | 0x4100E000   | AAR        | AAR      | NS             | NA           | Accelerated address resolver                |
| 14 | 0x4100E000   | CCM        | CCM      | NS             | NA           | AES CCM mode encryption                     |
| 15 | 0x4100F000   | DPPI       | DPPI     | NS             | NA           | DPPI controller                             |
| 16 | 0x41010000   | TEMP       | TEMP     | NS             | NA           | Temperature sensor                          |
| 17 | 0x41011000   | RTC        | RTC0     | NS             | NA           | Real-time counter 0                         |
| 18 | 0x41012000   | IPC        | IPC      | NS             | NA           | Interprocessor communication                |
| 19 | 0x41013000   | SPIM       | SPIM0    | NS             | NA           | SPI master 0                                |
| 19 | 0x41013000   | SPIS       | SPIS0    | NS             | NA           | SPI slave 0                                 |
| 19 | 0x41013000   | TWIM       | TWIM0    | NS             | NA           | Two-wire interface master 0                 |
| 19 | 0x41013000   | TWIS       | TWIS0    | NS             | NA           | Two-wire interface slave 0                  |
| 19 | 0x41013000   | UARTE      | UARTE0   | NS             | NA           | Universal asynchronous receiver/transmitter |
| 20 | 0x41014000   | EGU        | EGU0     | NS             | NA           | Event generator unit 0                      |
| 22 | 0x41016000   | RTC        | RTC1     | NS             | NA           | Real-time counter 1                         |
| 24 | 0x41018000   | TIMER      | TIMER1   | NS             | NA           | Timer 1                                     |
| 25 | 0x41019000   | TIMER      | TIMER2   | NS             | NA           | Timer 2                                     |
| 26 | 0x4101A000   | SWI        | SWI0     | NS             | NA           | Software interrupt 0                        |
| 27 | 0x4101B000   | SWI        | SWI1     | NS             | NA           | Software interrupt 1                        |

| ID  | Base address | Peripheral | Instance | Secure mapping | DMA security | Description                       |
|-----|--------------|------------|----------|----------------|--------------|-----------------------------------|
| 28  | 0x4101C000   | SWI        | SWI2     | NS             | NA           | Software interrupt 2              |
| 29  | 0x4101D000   | SWI        | SWI3     | NS             | NA           | Software interrupt 3              |
| 128 | 0x41080000   | ACL        | ACL      | NS             | NA           | Access control lists              |
| 128 | 0x41080000   | NVMC       | NVMC     | NS             | NA           | Non-Volatile Memory Controller    |
| 129 | 0x41081000   | VMC        | VMC      | NS             | NA           | Volatile memory controller        |
| 192 | 0x418C0500   | GPIO       | P0       | NS             | NA           | General purpose input and output  |
| 192 | 0x418C0800   | GPIO       | P1       | NS             | NA           | General purpose input and output  |
| N/A | 0x01FF0000   | FICR       | FICR     | NS             | NA           | Factory information configuration |
| N/A | 0x01FF8000   | UICR       | UICR     | NS             | NA           | User information configuration    |
| N/A | 0xE0042000   | CTI        | CTI      | NS             | NA           | Cross-trigger interface           |

Table 44: Instantiation table

## 6.1.4 Core components

### 6.1.4.1 FICR — Factory information configuration registers

Factory information configuration registers (FICR) are pre-programmed in factory and cannot be erased by the user. These registers contain chip-specific information and configuration.

#### 6.1.4.1.1 Registers

| Base address | Domain  | Peripheral | Instance | Secure mapping | DMA security | Description                       | Configuration |
|--------------|---------|------------|----------|----------------|--------------|-----------------------------------|---------------|
| 0x01FF0000   | NETWORK | FICR       | FICR     | NS             | NA           | Factory information configuration |               |

Table 45: Instances

| Register          | Offset | Security | Description                                                 |
|-------------------|--------|----------|-------------------------------------------------------------|
| INFO.CONFIGID     | 0x200  |          | Configuration identifier                                    |
| INFO.DEVICEID[n]  | 0x204  |          | Device identifier                                           |
| INFO.PART         | 0x20C  |          | Part code                                                   |
| INFO.VARIANT      | 0x210  |          | Part Variant, Hardware version and Production configuration |
| INFO.PACKAGE      | 0x214  |          | Package option                                              |
| INFO.RAM          | 0x218  |          | RAM variant                                                 |
| INFO.FLASH        | 0x21C  |          | Flash variant                                               |
| INFO.CODEPAGESIZE | 0x220  |          | Code memory page size in bytes                              |
| INFO.CODESIZE     | 0x224  |          | Code memory size                                            |
| INFO.DEVICETYPE   | 0x228  |          | Device type                                                 |
| ER[n]             | 0x280  |          | Encryption Root, word n                                     |
| IR[n]             | 0x290  |          | Identity Root, word n                                       |
| DEVICEADDRTYPE    | 0x2A0  |          | Device address type                                         |
| DEVICEADDR[n]     | 0x2A4  |          | Device address n                                            |
| TRIMCNF[n].ADDR   | 0x300  |          | Address                                                     |
| TRIMCNF[n].DATA   | 0x304  |          | Data                                                        |

Table 46: Register overview

##### 6.1.4.1.1.1 INFO.CONFIGID

Address offset: 0x200

Configuration identifier

|                  |            |      |          |                                                                                       |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|------|----------|---------------------------------------------------------------------------------------|--|--|--|-------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |      |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |      |          | A A A A A A A A A A A A A A A A A A A A A A A A A A                                   |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0xFFFFFFFF |            |      |          | 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1                       |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field |      | Value ID | Value                                                                                 |  |  |  | Description |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | R          | HWID |          | Identification number for the HW                                                      |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

#### 6.1.4.1.1.2 INFO.DEVICEID[n] (n=0..1)

Address offset: 0x204 + (n × 0x4)

Device identifier

|                  |            |          |       |                                                                                                                                                    |    |    |                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------|----|----|---------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          | 31    | 30                                                                                                                                                 | 29 | 28 | 27                              | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |          | A     | A                                                                                                                                                  | A  | A  | A                               | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0xFFFFFFFF |            |          | 1     | 1                                                                                                                                                  | 1  | 1  | 1                               | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ID               | Acce Field | Value ID | Value |                                                                                                                                                    |    |    | Description                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | R          | DEVICEID |       |                                                                                                                                                    |    |    | 64 bit unique device identifier |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |          |       | DEVICEID[0] contains the least significant bits of the device identifier. DEVICEID[1] contains the most significant bits of the device identifier. |    |    |                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 6.1.4.1.1.3 INFO.PART

Address offset: 0x20C

Part code

|                  |            |             |            |             |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-------------|------------|-------------|----|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |             |            | 31          | 30 | 29          | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |             |            | A           | A  | A           | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00005340 |            |             |            | 0           | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 1  | 0  | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |             | Value ID   | Value       |    | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | R          | PART        |            | Part code   |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | N5340       | 0x5340     | nRF5340     |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Unspecified | 0xFFFFFFFF | Unspecified |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 6.1.4.1.1.4 INFO.VARIANT

Address offset: 0x210

Part Variant, Hardware version and Production configuration

|                  |            |             |            |    |    |    |                                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-------------|------------|----|----|----|-------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |             | 31         | 30 | 29 | 28 | 27                                                                            | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |             | A          | A  | A  | A  | A                                                                             | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0xFFFFFFFF |            |             | 1          | 1  | 1  | 1  | 1                                                                             | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ID               | Acce Field | Value ID    | Value      |    |    |    | Description                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | R          | VARIANT     |            |    |    |    | Part Variant, Hardware version and Production configuration, encoded as ASCII |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | AAAA        | 0x41414141 |    |    |    | AAAA                                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Unspecified | 0xFFFFFFFF |    |    |    | Unspecified                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 6.1.4.1.1.5 INFO.PACKAGE

Address offset: 0x214

Package option

|                  |            |             |            |    |    |    |                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-------------|------------|----|----|----|-------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |             | 31         | 30 | 29 | 28 | 27                | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |             | A          | A  | A  | A  | A                 | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0xFFFFFFFF |            |             | 1          | 1  | 1  | 1  | 1                 | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ID               | Acce Field | Value ID    | Value      |    |    |    | Description       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | R          | PACKAGE     |            |    |    |    | Package option    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | QF          | 0x2000     |    |    |    | QFxx - 94 pin QFN |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Unspecified | 0xFFFFFFFF |    |    |    | Unspecified       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 6.1.4.1.1.6 INFO.RAM

Address offset: 0x218

RAM variant

| Bit number       |      |       | 31          | 30 | 29         | 28            | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------|------|-------|-------------|----|------------|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| ID               |      |       | A           | A  | A          | A             | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0xFFFFFFFF |      |       | 1           | 1  | 1          | 1             | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ID               | Acce | Field | Value       | ID | Value      | Description   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | R    | RAM   |             |    |            | RAM variant   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |       | K16         |    | 0x10       | 16 kByte RAM  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |       | K32         |    | 0x20       | 32 kByte RAM  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |       | K64         |    | 0x40       | 64 kByte RAM  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |       | K128        |    | 0x80       | 128 kByte RAM |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |       | K256        |    | 0x100      | 256 kByte RAM |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |       | K512        |    | 0x200      | 512 kByte RAM |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |       | Unspecified |    | 0xFFFFFFFF | Unspecified   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 6.1.4.1.1.7 INFO.FLASH

Address offset: 0x21C

Flash variant

| Bit number       |            |             | 31         | 30 | 29              | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------|------------|-------------|------------|----|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| ID               |            |             | A          | A  | A               | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0xFFFFFFFF |            |             | 1          | 1  | 1               | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |   |
| ID               | Acce Field | Value ID    | Value      |    | Description     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | R          | FLASH       |            |    | Flash variant   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | K128        | 0x80       |    | 128 kByte FLASH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | K256        | 0x100      |    | 256 kByte FLASH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | K512        | 0x200      |    | 512 kByte FLASH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | K1024       | 0x400      |    | 1 MByte FLASH   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | K2048       | 0x800      |    | 2 MByte FLASH   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Unspecified | 0xFFFFFFFF |    | Unspecified     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 6.1.4.1.1.8 INFO.CODEPAGESIZE

Address offset: 0x220

Code memory page size in bytes

|                  |            |              |          |       |       |       |  |  |             |                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------------|----------|-------|-------|-------|--|--|-------------|--------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |              |          |       |       |       |  |  |             | 31                             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |              |          |       |       |       |  |  |             | A                              | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000800 |            |              |          |       |       |       |  |  |             | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |              | Value ID |       | Value |       |  |  | Description |                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | R          | CODEPAGESIZE |          | K2048 |       | 0x800 |  |  |             | Code memory page size in bytes |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |              |          | K2048 |       | 0x800 |  |  |             | 2 kByte                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

#### 6.1.4.1.1.9 INFO.CODESIZE

Address offset: 0x224

Code memory size

| Bit number       |      |          | 31       | 30   | 29    | 28  | 27                                                 | 26                                  | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------|------|----------|----------|------|-------|-----|----------------------------------------------------|-------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| ID               |      |          | A        | A    | A     | A   | A                                                  | A                                   | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000080 |      |          | 0        | 0    | 0     | 0   | 0                                                  | 0                                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce | Field    | Value ID |      | Value |     | Description                                        |                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | R    | CODESIZE |          | P128 |       | 128 |                                                    | Code memory size in number of pages |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |          |          |      |       |     | Total code space is: CODEPAGESIZE * CODESIZE bytes |                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |          |          | P128 |       | 128 |                                                    | 128 pages                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 6.1.4.1.1.10 INFO.DEVICETYPE

Address offset: 0x228

Device type

|                  |            |            |          |            |    |    |    |                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|------------|----------|------------|----|----|----|---------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |            |          | 31         | 30 | 29 | 28 | 27                        | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |            |          | A          | A  | A  | A  | A                         | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |            |          | 0          | 0  | 0  | 0  | 0                         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |            | Value ID | Value      |    |    |    | Description               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | R          | DEVICETYPE |          |            |    |    |    | Device type               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |            | Die      | 0x00000000 |    |    |    | Device is an physical DIE |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |            | FPGA     | 0xFFFFFFFF |    |    |    | Device is an FPGA         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 6.1.4.1.1.11 ER[n] (n=0..3)

Address offset: 0x280 + (n × 0x4)

Encryption Root, word n

|                  |            |    |  |          |  |  |       |  |  |                         |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----|--|----------|--|--|-------|--|--|-------------------------|----|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |    |  |          |  |  |       |  |  | 31                      | 30 | 29          | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |    |  |          |  |  |       |  |  | A                       | A  | A           | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A | A | A |
| Reset 0xFFFFFFFF |            |    |  |          |  |  |       |  |  | 1                       | 1  | 1           | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ID               | Acce Field |    |  | Value ID |  |  | Value |  |  |                         |    | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | R          | ER |  |          |  |  |       |  |  | Encryption Root, word n |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

#### 6.1.4.1.1.12 IR[n] (n=0..3)

Address offset: 0x290 + (n × 0x4)

Identity Root, word n

|                  |            |    |          |                       |    |    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----|----------|-----------------------|----|----|----|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |    |          | 31                    | 30 | 29 | 28 | 27          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |    |          | A                     | A  | A  | A  | A           | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0xFFFFFFFF |            |    |          | 1                     | 1  | 1  | 1  | 1           | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ID               | Acce Field |    | Value ID | Value                 |    |    |    | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | R          | IR |          | Identity Root, word n |    |    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 6.1.4.1.1.13 DEVICEADDRTYPE

Address offset: 0x2A0

Device address type

|                  |      |                |        |    |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |                     |                |
|------------------|------|----------------|--------|----|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---------------------|----------------|
| Bit number       |      |                |        | 31 | 30    | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |                     |                |
| ID               |      |                |        |    |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |                     |                |
| Reset 0xFFFFFFFF |      |                |        | 1  | 1     | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |                     |                |
| ID               | Acce | Field          | Value  | ID | Value |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   | Description         |                |
| A                | R    | DEVICEADDRTYPE |        |    |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   | Device address type |                |
|                  |      |                | Public |    | 0     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |                     | Public address |
|                  |      |                | Random |    | 1     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |                     | Random address |

#### 6.1.4.1.1.14 DEVICEADDR[n] (n=0..1)

Address offset: 0x2A4 + (n × 0x4)

Device address n

|                  |            |            |       |    |    |    |                                                                                                                                                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|------------|-------|----|----|----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |            | 31    | 30 | 29 | 28 | 27                                                                                                                                                                                           | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |            | A     | A  | A  | A  | A                                                                                                                                                                                            | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0xFFFFFFFF |            |            | 1     | 1  | 1  | 1  | 1                                                                                                                                                                                            | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ID               | Acce Field | Value ID   | Value |    |    |    | Description                                                                                                                                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | R          | DEVICEADDR |       |    |    |    | 48 bit device address                                                                                                                                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |            |       |    |    |    | DEVICEADDR[0] contains the least significant bits of the device address. DEVICEADDR[1] contains the most significant bits of the device address. Only bits [15:0] of DEVICEADDR[1] are used. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 6.1.4.1.1.15 TRIMCNF[n].ADDR (n=0..31)

Address offset: 0x300 + (n × 0x8)

Address

| Bit number       |            |          | 31    | 30 | 29 | 28 | 27          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------|------------|----------|-------|----|----|----|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| ID               |            |          | A     | A  | A  | A  | A           | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0xFFFFFFFF |            |          | 1     | 1  | 1  | 1  | 1           | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ID               | Acce Field | Value ID | Value |    |    |    | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | Address  |       |    |    |    | Address     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 6.1.4.1.1.16 TRIMCNF[n].DATA (n=0..31)

Address offset: 0x304 + (n × 0x8)

Data



|                  |            |      |          |       |    |    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|------|----------|-------|----|----|----|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |      |          | 31    | 30 | 29 | 28 | 27          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |      |          | A     | A  | A  | A  | A           | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0xFFFFFFFF |            |      |          | 1     | 1  | 1  | 1  | 1           | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ID               | Acce Field |      | Value ID | Value |    |    |    | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | R          | Data |          | Data  |    |    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 6.1.4.2 UICR — User information configuration registers

The user information configuration registers (UICRs) are non-volatile memory (NVM) registers for configuring user specific settings.

For information on writing registers, see [NVMC — Non-volatile memory controller](#) on page 318 and [Memory](#) on page 125.

#### 6.1.4.2.1 Registers

| Base address | Domain  | Peripheral | Instance | Secure mapping | DMA security | Description                    | Configuration |
|--------------|---------|------------|----------|----------------|--------------|--------------------------------|---------------|
| 0x01FF8000   | NETWORK | UICR       | UICR     | NS             | NA           | User information configuration |               |

Table 47: Instances

| Register     | Offset | Security | Description                         |
|--------------|--------|----------|-------------------------------------|
| APPROTECT    | 0x000  |          | Access port protection              |
| ERASEPROTECT | 0x004  |          | Erase protection                    |
| NRFFW[n]     | 0x200  |          | Reserved for Nordic firmware design |
| CUSTOMER[n]  | 0x300  |          | Reserved for customer               |

Table 48: Register overview

##### 6.1.4.2.1.1 APPROTECT

Address offset: 0x000

Access port protection

|                  |      |       |             |            |    |    |    |                                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------|-------|-------------|------------|----|----|----|------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |      |       |             | 31         | 30 | 29 | 28 | 27                                                                                 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |      |       |             | A          | A  | A  | A  | A                                                                                  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |      |       |             | 0          | 0  | 0  | 0  | 0                                                                                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce | Field | Value ID    | Value      |    |    |    | Description                                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW   | PALL  |             |            |    |    |    | Blocks debugger read/write access to all CPU registers and memory mapped addresses |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |       |             |            |    |    |    | Any value except for the enumerations will yield unexpected results.               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |       | Unprotected | 0xFFFFFFFF |    |    |    | Unprotected                                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |       | Protected   | 0x00000000 |    |    |    | Protected                                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

##### 6.1.4.2.1.2 ERASEPROTECT

Address offset: 0x004

Erase protection

| Bit number       |            |             | 31         | 30 | 29 | 28                                                                   | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |
|------------------|------------|-------------|------------|----|----|----------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|--|
| ID               |            |             | A          | A  | A  | A                                                                    | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |  |  |  |  |
| Reset 0x00000000 |            |             | 0          | 0  | 0  | 0                                                                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |  |
| ID               | Acce Field | Value ID    | Value      |    |    | Description                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| A                | RW         | PALL        |            |    |    | Blocks NVMC ERASEALL and CTRLAP ERASEALL functionality.              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            |             |            |    |    | Any value except for the enumerations will yield unexpected results. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | Unprotected | 0xFFFFFFFF |    |    | Unprotected                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | Protected   | 0x00000000 |    |    | Protected                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |

#### 6.1.4.2.1.3 NRFFW[n] (n=0..31)

Address offset: 0x200 + (n × 0x4)

Reserved for Nordic firmware design

| Bit number       |            |          | 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21                                  | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------|------------|----------|-------|----|----|----|----|----|----|----|----|----|-------------------------------------|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| ID               |            |          | A     | A  | A  | A  | A  | A  | A  | A  | A  | A  | A                                   | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0xFFFFFFFF |            |          | 1     | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1                                   | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |   |
| ID               | Acce Field | Value ID | Value |    |    |    |    |    |    |    |    |    | Description                         |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | NRFFW    |       |    |    |    |    |    |    |    |    |    | Reserved for Nordic firmware design |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 6.1.4.2.1.4 CUSTOMER[n] (n=0..31)

Address offset: 0x300 + (n × 0x4)

Reserved for customer

|                  |            |          |          |                       |    |    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|-----------------------|----|----|----|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                    | 30 | 29 | 28 | 27          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |          |          | A                     | A  | A  | A  | A           | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0xFFFFFFFF |            |          |          | 1                     | 1  | 1  | 1  | 1           | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ID               | Acce Field |          | Value ID | Value                 |    |    |    | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | CUSTOMER |          | Reserved for customer |    |    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 6.1.4.3 AHB multilayer

AHB multilayer enables parallel access paths between multiple masters and slaves in a system. Access is resolved using priorities.

Each bus master is connected to a slave device through one or more interconnection matrixes. The bus masters are assigned priorities that are used to resolve access when two (or more) bus masters request access to the same slave device. The following applies when assigning priorities:

- If two (or more) bus masters request access to the same slave device, the master with the highest priority is granted access first.
- Bus masters with lower priority are stalled until the higher priority master has completed its transaction.
- If the higher priority master pauses at any point during its transaction, the lower priority master in queue is temporarily granted access to the slave device until the higher priority master resumes its activity.
- Bus masters that have the same priority are mutually exclusive, and cannot be used concurrently.

Some peripherals, like RADIO, do not have a safe stalling mechanism (not able to pause incoming data and no internal data buffering). Being a low priority bus master might cause loss of data for such peripherals upon bus contention. To avoid AHB bus contention when using multiple bus masters, apply one of the following guidelines:

- Avoid situations where more than one bus master is accessing the same slave.
- If more than one bus master is accessing the same slave, make sure that the bus bandwidth is not exhausted.

#### 6.1.4.3.1 AHB multilayer priorities

Each master connected to the AHB multilayer is assigned a default natural priority.

| Bus master name                | Natural relative priority | In/Out | Description                          |
|--------------------------------|---------------------------|--------|--------------------------------------|
| CPU                            | Highest priority          | I/O    |                                      |
| RADIO                          |                           | I/O    |                                      |
| CCM/ECB/AAR                    |                           | I/O    | Same priority and mutually exclusive |
| UARTE0/SPIM0/SPIS0/TWIM0/TWIS0 | Lowest priority           | I/O    | Same priority and mutually exclusive |

Table 49: AHB bus masters

# 7.1 Peripherals

## 7.1.1 Instantiation

The nRF5340 has two cores. Each core has its own peripherals that are part of that core, listed in their instantiation tables: [Instantiation](#) on page 97 for the application core, and [Instantiation](#) on page 127 for the network core. As seen in the memory map [Memory](#) on page 18, the application core peripherals are accessible from the network core, but the application core cannot access the network core peripherals.

If instances of a peripheral has differing configurations, this is noted in the configuration column of the peripheral's instantiation table. E.g. some of the TIMER instances have more capture and compare channels implemented than others, as listed in [Registers](#) on page 603.

## 7.1.2 Peripheral interface

Peripherals are controlled by the CPU through configuration registers, as well as task and event registers. Task registers are inputs, enabling the CPU and other peripherals to initiate a functionality. Event registers are outputs, enabling a peripheral to trigger tasks in other peripherals and/or the CPU by tying events to CPU interrupts.

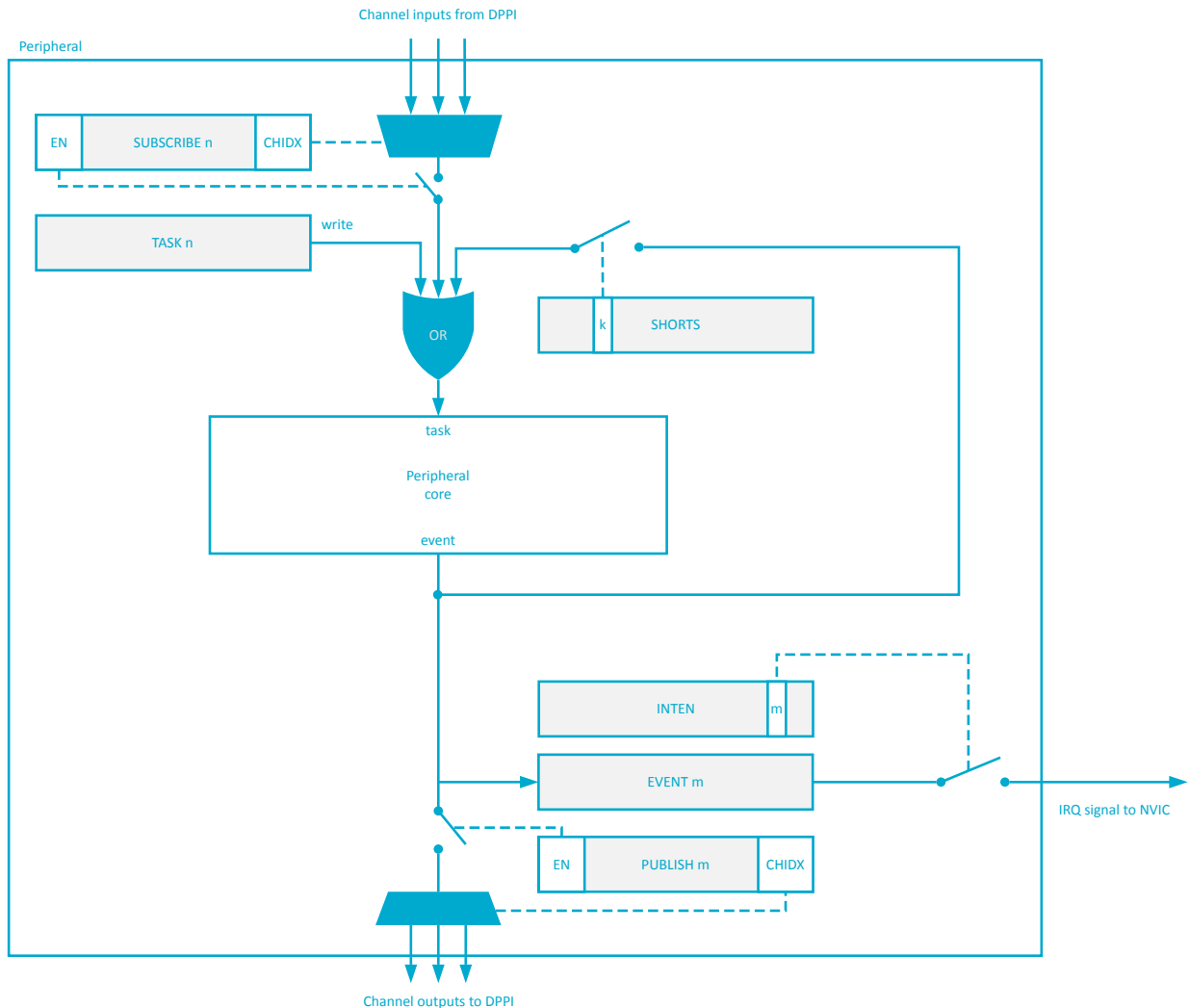


Figure 28: Peripheral interface

The distributed programmable peripheral interconnect (DPPI) feature enables peripherals to connect events to tasks without CPU intervention.

**Note:** For more information on DPPI and the DPPI channels, see [DPPI - Distributed programmable peripheral interconnect](#) on page 188.

### 7.1.2.1 Peripheral ID

Every peripheral is assigned a fixed block of 0x1000 bytes of address space, which is equal to 1024 x 32 bit registers.

See [Instantiation](#) on page 136 for more information about which peripherals are available and where they are located in the address map.

There is a direct relationship between peripheral ID and base address. For example, a peripheral with base address 0x40000000 is assigned ID=0, a peripheral with base address 0x40001000 is assigned ID=1, and a peripheral with base address 0x4001F000 is assigned ID=31.

Peripherals may share the same ID, which may impose one or more of the following limitations:

- Shared registers or common resources
- Limited availability due to mutually exclusive operation; only one peripheral in use at a time

- Enforced peripheral behavior when switching between peripherals (disable the first peripheral before enabling the second)

### 7.1.2.2 Peripherals with shared ID

In general (with the exception of ID 0), peripherals sharing an ID and base address may not be used simultaneously. Only one peripheral can be enabled at a given ID.

When switching between two peripherals sharing an ID, the following should be performed to prevent unwanted behavior:

1. Disable the previously used peripheral.
2. Disable any publish/subscribe connection to the DPPI system for the peripheral that is being disabled.
3. Clear all bits in the INTEN register, i.e. `INTENCLR = 0xFFFFFFFF`.
4. Explicitly configure the peripheral being enabled. Do not rely on inherited configuration from the disabled peripheral.
5. Enable the now configured peripheral.

For a list of which peripherals that share an ID see [Instantiation](#) on page 136.

### 7.1.2.3 Peripheral registers

Most peripherals feature an ENABLE register. Unless otherwise specified, the peripheral registers must be configured before enabling the peripheral.

PSEL registers need to be set before a peripheral is enabled or started. Updating PSEL registers while the peripheral is running has no effect. In order to connect a peripheral to a different GPIO, the peripheral must be disabled, the PSEL register updated, and the peripheral re-enabled. It takes four CPU cycles between the PSEL register update and the connection between a peripheral and a GPIO becoming effective.

**Note:** Note that the peripheral must be enabled before tasks and events can be used.

Most of the register values are lost during System OFF or when a reset is triggered. Some registers will retain their values in System OFF or for some specific reset sources. These registers are marked as retained in the register description for a given peripheral. For more information on their behavior, see chapter [RESET - Reset control](#) on page 55.

### 7.1.2.4 Bit set and clear

Registers with multiple single-bit bit fields may implement the set-and-clear pattern. This pattern enables firmware to set and clear individual bits in a register without having to perform a read-modify-write operation on the main register.

This pattern is implemented using three consecutive addresses in the register map, where the main register is followed by dedicated SET and CLR registers (in that exact order).

In the main register, the SET register sets individual bits and the CLR register clears them. Writing '1' to a bit in the SET or CLR register will set or clear the same bit in the main register respectively. Writing '0' to a bit in the SET or CLR register has no effect. Reading the SET or CLR register returns the value of the main register.

**Note:** The main register may not be visible and therefore not directly accessible in all cases.

### 7.1.2.5 Tasks

Tasks are used to trigger actions in a peripheral, such as to start a particular behavior. A peripheral can implement multiple tasks with each task having a separate register in that peripheral's task register group.

A task is triggered when firmware writes '1' to the task register, or when the peripheral itself or another peripheral toggles the corresponding task signal. See the figure [Figure 28: Peripheral interface](#) on page 137.

### 7.1.2.6 Events

Events are used to notify peripherals and the CPU about events that have happened, for example a state change in a peripheral. A peripheral may generate multiple events, where each event has a separate register in that peripheral's event register group.

An event is generated when the peripheral itself toggles the corresponding event signal, and the event register is updated to reflect that the event has been generated, see figure [Figure 28: Peripheral interface](#) on page 137. An event register is cleared when a '0' is written to it by firmware. Events can be generated by the peripheral even when the event register is set to '1'.

### 7.1.2.7 Publish and subscribe

Events and tasks from different peripherals can be connected together through the DPPI system using the PUBLISH and SUBSCRIBE registers in each peripheral. See [Figure 28: Peripheral interface](#) on page 137.

An event can be published onto a DPPI channel by configuring the event's PUBLISH register. Similarly, a task can subscribe to a DPPI channel by configuring the task's SUBSCRIBE register.

See [DPPI - Distributed programmable peripheral interconnect](#) on page 188 for details.

### 7.1.2.8 Shortcuts

A shortcut is a direct connection between an event and a task within the same peripheral. If a shortcut is enabled, the associated task is automatically triggered when its associated event is generated.

Using shortcuts is equivalent to making the connection outside the peripheral and through the DPPI. However, the propagation delay when using shortcuts is usually shorter than the propagation delay through the DPPI.

Shortcuts are predefined, which means that their connections cannot be configured by firmware. Each shortcut can be individually enabled or disabled through the shortcut register, one bit per shortcut, giving a maximum of 32 shortcuts for each peripheral.

### 7.1.2.9 Interrupts

All peripherals support interrupts which are generated by events.

A peripheral only occupies one interrupt, and the interrupt number follows the peripheral ID. For example, the peripheral with ID=4 is connected to interrupt number 4 in the nested vectored interrupt controller (NVIC).

Using registers INTEN, INTENSET, and INTENCLR, every event generated by a peripheral can be configured to generate that peripheral's interrupt. Multiple events can be enabled to generate interrupts simultaneously. To resolve the correct interrupt source, the event registers in the event group of peripheral registers will indicate the source.

Some peripherals implement only INTENSET and INTENCLR registers, and the INTEN register is not available on those peripherals. See the individual peripheral chapters for details. In all cases, reading back the INTENSET or INTENCLR register returns the same information as in INTEN.

Each event implemented in the peripheral is associated with a specific bit position in the INTEN, INTENSET, and INTENCLR registers.

The relationship between tasks, events, shortcuts, and interrupts is illustrated in figure [Figure 28: Peripheral interface](#) on page 137.

#### 7.1.2.9.1 Interrupt clearing and disabling

Interrupts should always be cleared by writing '0' to the corresponding EVENT register.

Until cleared, interrupts will immediately be re-triggered and cause software interrupt service routines to be executed repeatedly.

Because the clearing of the EVENT register may take a number of CPU clock cycles, the program should perform a read from the EVENT register that has been cleared before exiting the interrupt service routine. This will ensure that the EVENT clearing has taken place before the interrupt service routine is exited. Care should be taken to ensure that the compiler does not remove the read operation as an optimization.

Similarly, when disabling an interrupt inside an interrupt service routine, the program should perform a read from the INTEN or INTENCLR registers to ensure that the interrupt is disabled before exiting the interrupt service routine.

#### 7.1.2.10 Secure/non-secure peripherals

For some peripherals, the security configuration can change from secure to non-secure, or vice versa. Care must be taken when changing the security configuration of a peripheral, to prevent security information leakage and ensure correct operation.

The following sequence should be followed, where applicable, when configuring and changing the security settings of a peripheral in the [SPU — System protection unit](#) on page 568:

1. Stop peripheral operation
2. Disable the peripheral
3. Remove pin connections
4. Disable DPPI connections
5. Clear sensitive registers (e.g. writing back default values)
6. Change peripheral security setting in the [SPU — System protection unit](#) on page 568
7. Re-enable the peripheral

### 7.1.3 EasyDMA

EasyDMA is a module implemented by some peripherals to gain direct access to Data RAM.

EasyDMA is an AHB bus master similar to CPU and is connected to the AHB multilayer interconnect for direct access to Data RAM. EasyDMA is not able to access flash.

A peripheral can implement multiple EasyDMA instances to provide dedicated channels. For example, for reading and writing of data between the peripheral and RAM. This concept is illustrated in [Figure 29: EasyDMA example](#) on page 141.



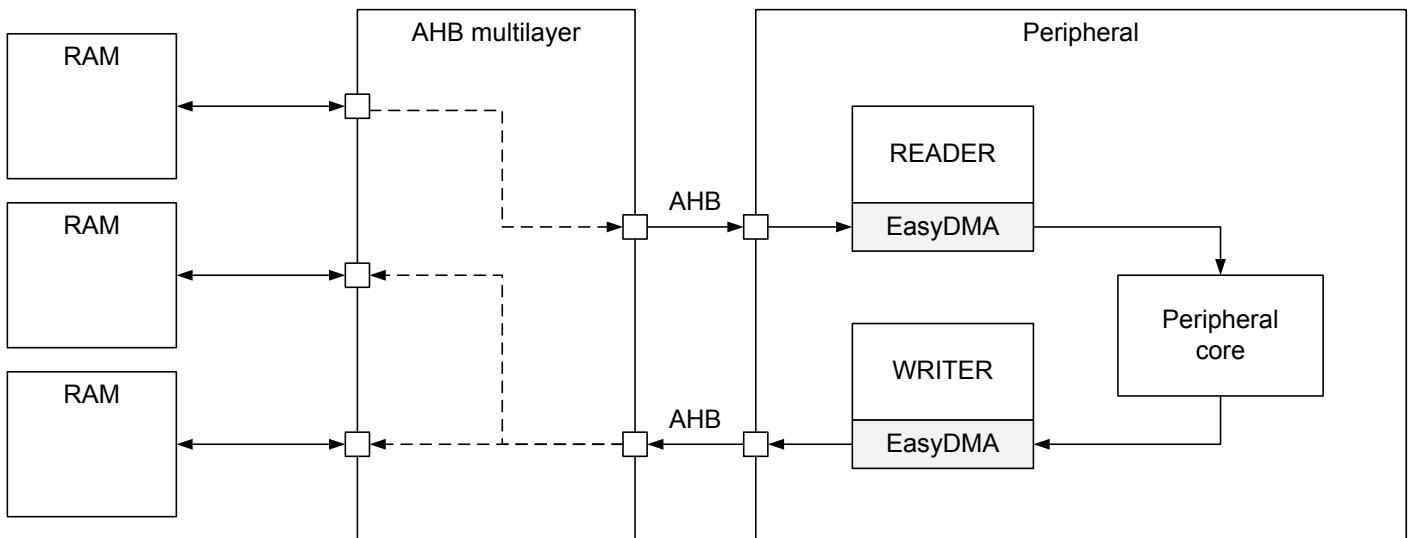


Figure 29: EasyDMA example

An EasyDMA channel is implemented in the following way, but some variations may occur:

```

READERBUFFER_SIZE 5
WRITERBUFFER_SIZE 6

uint8_t readerBuffer[READERBUFFER_SIZE] __at__ 0x20000000;
uint8_t writerBuffer[WRITERBUFFER_SIZE] __at__ 0x20000005;

// Configuring the READER channel
MYPERIPHERAL->READER.MAXCNT = READERBUFFER_SIZE;
MYPERIPHERAL->READER.PTR = &readerBuffer;

// Configure the WRITER channel
MYPERIPHERAL->WRITER.MAXCNT = WRITERBUFFER_SIZE;
MYPERIPHERAL->WRITER.PTR = &writerBuffer;

```

This example shows a peripheral called MYPERIPHERAL that implements two EasyDMA channels - one for reading called READER, and one for writing called WRITER. When the peripheral is started, it is assumed that the peripheral will:

- Read 5 bytes from the readerBuffer located in RAM at address 0x20000000.
- Process the data.
- Write no more than 6 bytes back to the writerBuffer located in RAM at address 0x20000005.

The memory layout of these buffers is illustrated in [Figure 30: EasyDMA memory layout](#) on page 141.

|            |                 |                 |                 |                 |
|------------|-----------------|-----------------|-----------------|-----------------|
| 0x20000000 | readerBuffer[0] | readerBuffer[1] | readerBuffer[2] | readerBuffer[3] |
| 0x20000004 | readerBuffer[4] | writerBuffer[0] | writerBuffer[1] | writerBuffer[2] |
| 0x20000008 | writerBuffer[3] | writerBuffer[4] | writerBuffer[5] |                 |

Figure 30: EasyDMA memory layout

The WRITER.MAXCNT register should not be specified larger than the actual size of the buffer (writerBuffer). Otherwise, the channel would overflow the writerBuffer.

Once an EasyDMA transfer is completed, the AMOUNT register can be read by the CPU to see how many bytes were transferred. For example, CPU can read MYPERIPHERAL->WRITER.AMOUNT register to see how many bytes WRITER wrote to RAM.

Note that the PTR register of a READER or WRITER must point to a valid memory region before use. The reset value of a PTR register is not guaranteed to point to valid memory. See [Memory](#) on page 18 for more information about the different memory regions and EasyDMA connectivity.

### 7.1.3.1 EasyDMA error handling

Some errors may occur during DMA handling.

If READER.PTR or WRITER.PTR is not pointing to a valid memory region, an EasyDMA transfer may result in a HardFault or RAM corruption. See [Memory](#) on page 18 for more information about the different memory regions.

If several AHB bus masters try to access the same AHB slave at the same time, AHB bus congestion might occur. An EasyDMA channel is an AHB master. Depending on the peripheral, the peripheral may either stall and wait for access to be granted, or lose data.

### 7.1.3.2 EasyDMA array list

EasyDMA is able to operate in Array List mode.

The Array List mode is implemented in channels where the LIST register is available.

The array list does not provide a mechanism to explicitly specify where the next item in the list is located. Instead, it assumes that the list is organized as a linear array where items are located one after the other in RAM.

The EasyDMA Array List can be implemented by using the data structure ArrayList\_type as illustrated in the code example below using a READER EasyDMA channel as an example:

```
#define BUFFER_SIZE 4

typedef struct ArrayList
{
    uint8_t buffer[BUFFER_SIZE];
} ArrayList_type;

ArrayList_type ReaderList[3] __at__ 0x20000000;

MYPERIPHERAL->READER.MAXCNT = BUFFER_SIZE;
MYPERIPHERAL->READER.PTR = &ReaderList;
MYPERIPHERAL->READER.LIST = MYPERIPHERAL_READER_LIST_ArrayList;
```

The data structure only includes a buffer with size equal to the size of READER.MAXCNT register. EasyDMA uses the READER.MAXCNT register to determine when the buffer is full.

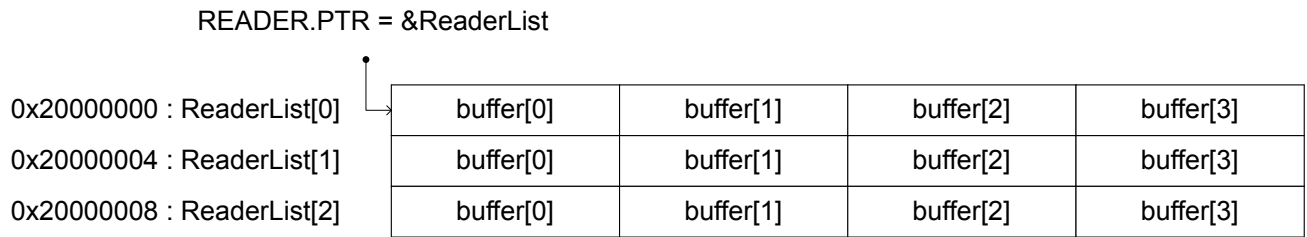


Figure 31: EasyDMA array list

### 7.1.4 ACL — Access control lists

The Access control lists (ACL) peripheral is designed to assign and enforce access permissions to different regions of the on-chip flash memory map.

Flash memory regions can be assigned individual ACL permission schemes. The following registers are involved:

- PERM register, where the permissions are configured.
- ADDR register, where the word-aligned start address for the flash page is defined.
- SIZE register, where the size of the region the permissions are applied to is determined.

**Important:** The size of the region in bytes is restricted to a multiple of the flash page size, and the maximum region size is limited to the flash size. See [Memory](#) on page 18 for more information.

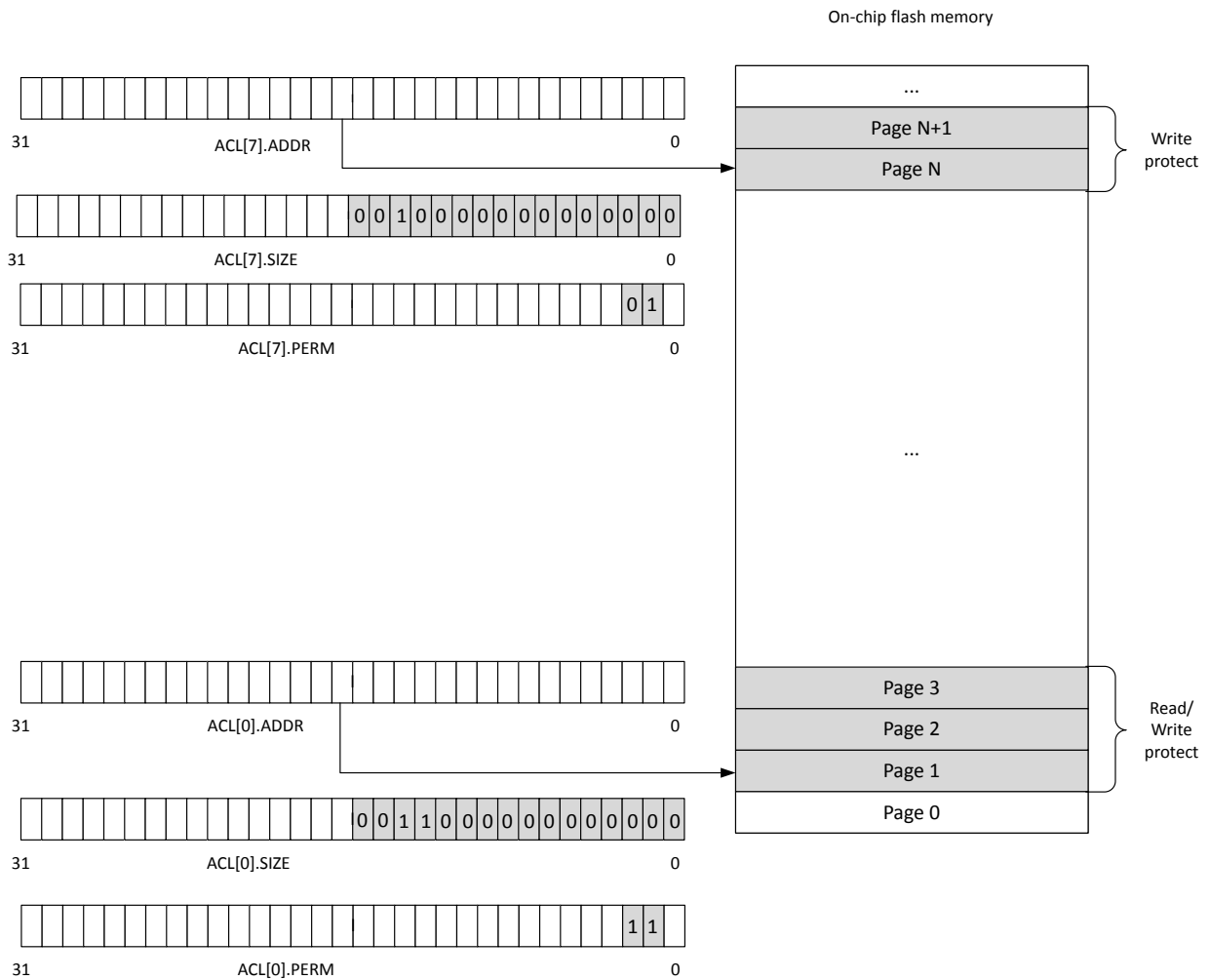


Figure 32: Protected regions of on-chip flash memory

There are four defined ACL permission schemes, with different combinations of read/write permissions:

| Read | Write | Protection description                                                 |
|------|-------|------------------------------------------------------------------------|
| 0    | 0     | No protection. Entire region can be executed, read, written or erased. |
| 0    | 1     | Region can be executed and read, but not written or erased.            |
| 1    | 0     | Region can be written and erased, but not executed or read.            |
| 1    | 1     | Region is locked for all access until next reset.                      |

Table 50: Permission schemes

**Important:** If a permission violation to a protected region is detected by the ACL peripheral, the request is blocked and a Bus Fault exception is triggered.

Access control to a configured region is enforced by the hardware two CPU clock cycles after the ADDR, SIZE, and PERM registers for an ACL instance have been successfully written. The protection is only enforced if a valid start address of the flash page boundary is written into the ADDR register, and the values of the SIZE and PERM registers are not zero.

The ADDR, SIZE, and PERM registers can only be written once. All ACL configuration registers are cleared on reset (by resetting the device from any reset source), which is also the only way of clearing the configuration registers. To ensure that the desired permission schemes are always enforced by the ACL peripheral, the device boot sequence must perform the necessary configuration.

Debugger read access to a read-protected region will be Read-As-Zero (RAZ), while debugger write access to a write-protected region will be Write-Ignored (WI).

### 7.1.4.1 Registers

| Base address | Domain  | Peripheral | Instance | Secure mapping | DMA security | Description          | Configuration                                          |
|--------------|---------|------------|----------|----------------|--------------|----------------------|--------------------------------------------------------|
| 0x41080000   | NETWORK | ACL        | ACL      | NS             | NA           | Access control lists | This ACL can only protect network core's local memory. |

Table 51: Instances

| Register       | Offset | Security | Description                                                                                  |
|----------------|--------|----------|----------------------------------------------------------------------------------------------|
| ACL[n].ADDR    | 0x800  |          | Configure the word-aligned start address of region n to protect                              |
| ACL[n].SIZE    | 0x804  |          | Size of region to protect counting from address ACL[n].ADDR. Write '0' as no effect.         |
| ACL[n].PERM    | 0x808  |          | Access permissions for region n as defined by start address ACL[n].ADDR and size ACL[n].SIZE |
| ACL[n].UNUSED0 | 0x80C  |          | Reserved                                                                                     |

Table 52: Register overview

#### 7.1.4.1.1 ACL[n].ADDR (n=0..7)

Address offset:  $0x800 + (n \times 0x10)$

Configure the word-aligned start address of region n to protect

This register can only be written once.

|                  |            |  |          |       |    |    |    |                                                                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|-------|----|----|----|----------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31    | 30 | 29 | 28 | 27                                                                                                       | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |  |          | A     | A  | A  | A  | A                                                                                                        | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |          | 0     | 0  | 0  | 0  | 0                                                                                                        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID | Value |    |    |    | Description                                                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW1 ADDR   |  |          |       |    |    |    | Valid word-aligned start address of region n to protect.<br>Address must point to a flash page boundary. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 7.1.4.1.2 ACL[n].SIZE (n=0..7)

Address offset:  $0x804 + (n \times 0x10)$

Size of region to protect counting from address ACL[n].ADDR. Write '0' as no effect.

This register can only be written once.

|                  |            |  |          |       |    |    |    |                                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|-------|----|----|----|-----------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31    | 30 | 29 | 28 | 27                                                                          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |  |          | A     | A  | A  | A  | A                                                                           | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |          | 0     | 0  | 0  | 0  | 0                                                                           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID | Value |    |    |    | Description                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW1 SIZE   |  |          |       |    |    |    | Size of flash region n in bytes. Must be a multiple of the flash page size. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 7.1.4.1.3 ACL[n].PERM (n=0..7)

Address offset:  $0x808 + (n \times 0x10)$

Access permissions for region n as defined by start address ACL[n].ADDR and size ACL[n].SIZE

This register can only be written once.

| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |            |          | C B                                                                                   |                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW1 WRITE  |          |                                                                                       | Configure write and erase permissions for region n. Write '0' has no effect. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enable   | 0                                                                                     | Allow write and erase instructions to region n                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disable  | 1                                                                                     | Block write and erase instructions to region n                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW1 READ   |          |                                                                                       | Configure read permissions for region n. Write '0' has no effect.            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enable   | 0                                                                                     | Allow read instructions to region n                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disable  | 1                                                                                     | Block read instructions to region n                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

## 7.1.5 AAR — Accelerated address resolver

Accelerated address resolver is a cryptographic support function for implementing the Resolvable Private Address Resolution Procedure described in the *Bluetooth Core specification v4.0*. Resolvable Private Address generation should be achieved using ECB and is not supported by AAR.

The procedure allows two devices that share a secret key to generate and resolve a hash based on their device address. The AAR block enables real-time address resolution on incoming packets when configured as described in this chapter. This allows real-time packet filtering (whitelisting) using a list of known shared keys (Identity Resolving Keys (IRK) in *Bluetooth*).

### 7.1.5.1 Shared resources

The AAR shares the same AES module as the ECB and CCM peripherals. The ECB will always have the lowest priority. If there is a sharing conflict during encryption, the ECB operation will be aborted and an `ERRORECB` event will be generated in the ECB peripheral.

Additionally, the AAR shares registers and other resources with the peripherals that have the same ID as the AAR. See [Peripherals with shared ID](#) on page 138 for more information.

### 7.1.5.2 EasyDMA

The AAR implements EasyDMA for reading and writing to the RAM. The EasyDMA will have finished accessing the RAM when the `END`, `RESOLVED`, and `NOTRESOLVED` events are generated.

If the `IRKPTR` on page 153, `ADDRPTR` on page 153, and the `SCRATCHPTR` on page 153 is not pointing to the Data RAM region, an EasyDMA transfer may result in a `HardFault` or RAM corruption. See [Memory](#) on page 18 for more information about the different memory regions.

### 7.1.5.3 Resolving a resolvable address

As per *Bluetooth* specification, a private resolvable address is composed of six bytes.

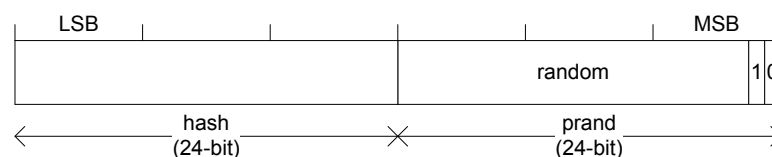


Figure 33: Resolvable address

To resolve an address the register [ADDRPTR](#) on page 153 must point to the start of the packet. The resolver is started by triggering the START task. A RESOLVED event is generated when the AAR manages to resolve the address using one of the Identity Resolving Keys (IRK) found in the IRK data structure. The AAR will use the IRK specified in the register IRK0 to IRK15 starting from IRK0. The register [NIRK](#) on page 152 specifies how many IRKs should be used. The AAR module will generate a NOTRESOLVED event if it is not able to resolve the address using the specified list of IRKs.

The AAR will go through the list of available IRKs in the IRK data structure and for each IRK try to resolve the address according to the Resolvable Private Address Resolution Procedure described in the *Bluetooth Core specification v4.0 [Vol 3]* chapter 10.8.2.3. The time it takes to resolve an address varies due to the location in the list of the resolvable address. The resolution time will also be affected by RAM accesses performed by other peripherals and the CPU. See the [Electrical specifications](#) for more information about resolution time.

The AAR only compares the received address to those programmed in the module without checking the address type.

The AAR will stop as soon as it has managed to resolve the address, or after trying to resolve the address using NIRK number of IRKs from the IRK data structure. The AAR will generate an END event after it has stopped.

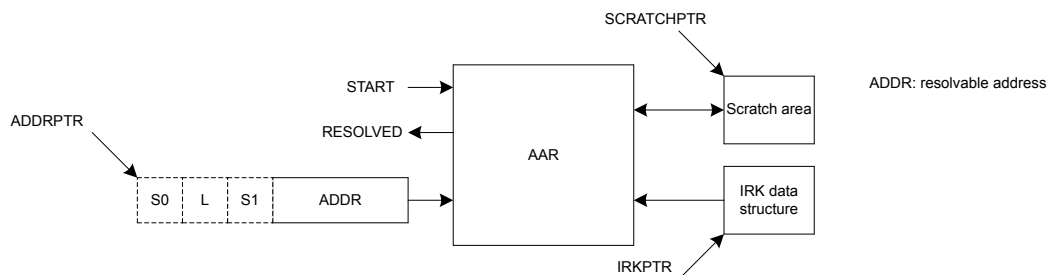


Figure 34: Address resolution with packet preloaded into RAM

#### 7.1.5.4 Use case example for chaining RADIO packet reception with address resolution using AAR

The AAR may be started as soon as the 6 bytes required by the AAR have been received by the RADIO and stored in RAM. The ADDRPTR pointer must point to the start of packet.

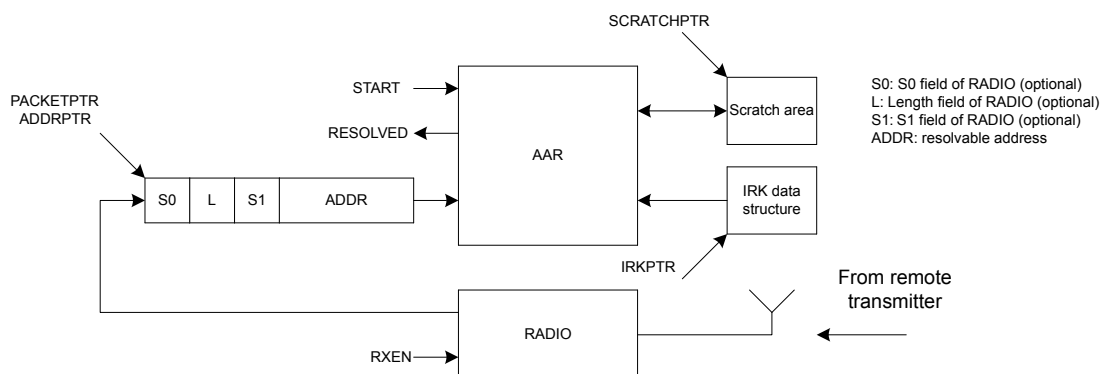


Figure 35: Address resolution with packet loaded into RAM by the RADIO

#### 7.1.5.5 IRK data structure

The IRK data structure is located in RAM at the memory location specified by the IRKPTR register.

| Property | Address offset | Description               |
|----------|----------------|---------------------------|
| IRK0     | 0              | IRK number 0 (16 - byte)  |
| IRK1     | 16             | IRK number 1 (16 - byte)  |
| ..       | ..             | ..                        |
| IRK15    | 240            | IRK number 15 (16 - byte) |

Table 53: IRK data structure overview

### 7.1.5.6 Registers

| Base address | Domain  | Peripheral | Instance | Secure mapping | DMA security | Description                  | Configuration |
|--------------|---------|------------|----------|----------------|--------------|------------------------------|---------------|
| 0x4100E000   | NETWORK | AAR        | AAR      | NS             | NA           | Accelerated address resolver |               |

Table 54: Instances

| Register            | Offset | Security | Description                                                                 |
|---------------------|--------|----------|-----------------------------------------------------------------------------|
| TASKS_START         | 0x000  |          | Start resolving addresses based on IRKs specified in the IRK data structure |
| TASKS_STOP          | 0x008  |          | Stop resolving addresses                                                    |
| SUBSCRIBE_START     | 0x080  |          | Subscribe configuration for task <b>START</b>                               |
| SUBSCRIBE_STOP      | 0x088  |          | Subscribe configuration for task <b>STOP</b>                                |
| EVENTS_END          | 0x100  |          | Address resolution procedure complete                                       |
| EVENTS_RESOLVED     | 0x104  |          | Address resolved                                                            |
| EVENTS_NOTRESOLVED  | 0x108  |          | Address not resolved                                                        |
| PUBLISH_END         | 0x180  |          | Publish configuration for event <b>END</b>                                  |
| PUBLISH_RESOLVED    | 0x184  |          | Publish configuration for event <b>RESOLVED</b>                             |
| PUBLISH_NOTRESOLVED | 0x188  |          | Publish configuration for event <b>NOTRESOLVED</b>                          |
| INTENSET            | 0x304  |          | Enable interrupt                                                            |
| INTENCLR            | 0x308  |          | Disable interrupt                                                           |
| STATUS              | 0x400  |          | Resolution status                                                           |
| ENABLE              | 0x500  |          | Enable AAR                                                                  |
| NIRK                | 0x504  |          | Number of IRKs                                                              |
| IRKPTR              | 0x508  |          | Pointer to IRK data structure                                               |
| ADDRPTR             | 0x510  |          | Pointer to the resolvable address                                           |
| SCRATCHPTR          | 0x514  |          | Pointer to data area used for temporary storage                             |

Table 55: Register overview

#### 7.1.5.6.1 TASKS\_START

Address offset: 0x000

Start resolving addresses based on IRKs specified in the IRK data structure

|                  |            |             |       |    |                                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |
|------------------|------------|-------------|-------|----|-----------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|--|--|
| Bit number       |            |             | 31    | 30 | 29                                                                          | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |  |
| ID               |            |             | A     |    |                                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |
| Reset 0x00000000 |            |             | 0     | 0  | 0                                                                           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |  |  |
| ID               | Acce Field | Value ID    | Value |    | Description                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |
| A                | W          | TASKS_START |       |    | Start resolving addresses based on IRKs specified in the IRK data structure |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |
|                  |            | Trigger     | 1     |    | Trigger task                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |



### 7.1.5.6.2 TASKS\_STOP

Address offset: 0x008

Stop resolving addresses

| Bit number       |             | 31         | 30 | 29    | 28 | 27                       | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------|-------------|------------|----|-------|----|--------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| ID               |             |            |    |       |    |                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | A |
| Reset 0x00000000 |             | 0          | 0  | 0     | 0  | 0                        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acces Field | Value ID   |    | Value |    | Description              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | W           | TASKS_STOP |    |       |    | Stop resolving addresses |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |             | Trigger    |    | 1     |    | Trigger task             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.5.6.3 SUBSCRIBE\_START

Address offset: 0x080

Subscribe configuration for task **START**

| Bit number       |             | 31       | 30       | 29       | 28 | 27                                               | 26                   | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------|-------------|----------|----------|----------|----|--------------------------------------------------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| ID               |             | B        |          |          |    |                                                  |                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | A |
| Reset 0x00000000 |             | 0        | 0        | 0        | 0  | 0                                                | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acces Field | Value ID |          | Value    |    | Description                                      |                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW          | CHIDX    |          | [255..0] |    | Channel that task <b>START</b> will subscribe to |                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| B                | RW          | EN       | Disabled |          | 0  |                                                  | Disable subscription |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |             |          | Enabled  |          | 1  |                                                  | Enable subscription  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.5.6.4 SUBSCRIBE\_STOP

Address offset: 0x088

Subscribe configuration for task **STOP**

| Bit number       |             | 31       | 30       | 29       | 28 | 27                                              | 26                   | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------|-------------|----------|----------|----------|----|-------------------------------------------------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| ID               |             | B        |          |          |    |                                                 |                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | A |
| Reset 0x00000000 |             | 0        | 0        | 0        | 0  | 0                                               | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acces Field | Value ID |          | Value    |    | Description                                     |                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW          | CHIDX    |          | [255..0] |    | Channel that task <b>STOP</b> will subscribe to |                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| B                | RW          | EN       | Disabled |          | 0  |                                                 | Disable subscription |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |             |          | Enabled  |          | 1  |                                                 | Enable subscription  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.5.6.5 EVENTS\_END

Address offset: 0x100

Address resolution procedure complete

|                  |            |              |          |   |       |                                       |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------------|----------|---|-------|---------------------------------------|-------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |              |          |   |       |                                       |             |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |              |          |   |       |                                       |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |   |
| Reset 0x00000000 |            |              |          |   |       |                                       |             |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |              | Value ID |   | Value |                                       | Description |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | EVENTS_END   |          |   |       | Address resolution procedure complete |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | NotGenerated |          | 0 |       | Event not generated                   |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Generated    |          | 1 |       | Event generated                       |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.5.6.6 EVENTS\_RESOLVED

Address offset: 0x104

Address resolved

|                  |            |                 |       |                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-----------------|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                 |       | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |                 |       |                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |
| Reset 0x00000000 |            |                 |       | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID        | Value | Description         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | EVENTS_RESOLVED |       | Address resolved    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | NotGenerated    | 0     | Event not generated |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Generated       | 1     | Event generated     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.5.6.7 EVENTS\_NOTRESOLVED

Address offset: 0x108

Address not resolved

|                  |            |                    |       |                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|------------------|------------|--------------------|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|---|
| Bit number       |            |                    |       | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |   |
| ID               |            |                    |       |                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  | A |
| Reset 0x00000000 |            |                    |       | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |   |
| ID               | Acce Field | Value ID           | Value | Description          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
| A                | RW         | EVENTS_NOTRESOLVED |       | Address not resolved |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|                  |            | NotGenerated       | 0     | Event not generated  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|                  |            | Generated          | 1     | Event generated      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |

#### 7.1.5.6.8 PUBLISH\_END

Address offset: 0x180

Publish configuration for event [END](#)

|                  |            |          |          |                    |    |                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|--------------------|----|------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                 | 30 | 29                                             | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |          |          | B                  |    |                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   |   |   |   |   |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |          |          | 0                  |    |                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |          | Value ID | Value              |    | Description                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | CHIDX    |          | [255..0]           |    | Channel that event <b>END</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW         | EN       |          |                    |    |                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        | Disable publishing |    |                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        | Enable publishing  |    |                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.5.6.9 PUBLISH\_RESOLVED

Address offset: 0x184

Publish configuration for event [RESOLVED](#)

|                  |            |  |          |          |    |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|----------|----|-----------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31       | 30 | 29                                                  | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |  |          | B        |    |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   |   |   |   |   |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |          | 0        |    |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID | Value    |    | Description                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          | [255..0] |    | Channel that event <b>RESOLVED</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |          |    |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled | 0        |    | Disable publishing                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  | 1        |    | Enable publishing                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.5.6.10 PUBLISH\_NOTRESOLVED

Address offset: 0x188

Publish configuration for event **NOTRESOLVED**

|            |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| Bit number |  |  |  |  |  |  |  |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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Address offset: 0x304

Enable interrupt

|                  |      |             |          |                                                                         |                |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------|-------------|----------|-------------------------------------------------------------------------|----------------|------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |      |             |          | 31                                                                      | 30             | 29                                                               | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |      |             |          |                                                                         |                |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | C | B | A |
| Reset 0x00000000 |      |             |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |                |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| D                | Acce | Field       | Value    | ID                                                                      | Value          | Description                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW   | END         |          |                                                                         |                | Write '1' to enable interrupt for event <span>END</span>         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |             | Set      | 1                                                                       | Enable         |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |             | Disabled | 0                                                                       | Read: Disabled |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |             | Enabled  | 1                                                                       | Read: Enabled  |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW   | RESOLVED    |          |                                                                         |                | Write '1' to enable interrupt for event <span>RESOLVED</span>    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |             | Set      | 1                                                                       | Enable         |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |             | Disabled | 0                                                                       | Read: Disabled |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |             | Enabled  | 1                                                                       | Read: Enabled  |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| C                | RW   | NOTRESOLVED |          |                                                                         |                | Write '1' to enable interrupt for event <span>NOTRESOLVED</span> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |             | Set      | 1                                                                       | Enable         |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |             | Disabled | 0                                                                       | Read: Disabled |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |             | Enabled  | 1                                                                       | Read: Enabled  |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.5.6.12 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number       |                |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|----------------|----------|---------------------------------------------------------------------------------------|------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |                |          | C B A                                                                                 |                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |                |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field     | Value ID | Value                                                                                 | Description                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW END         |          |                                                                                       | Write '1' to disable interrupt for event END         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                | Clear    | 1                                                                                     | Disable                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                | Disabled | 0                                                                                     | Read: Disabled                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                | Enabled  | 1                                                                                     | Read: Enabled                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW RESOLVED    |          |                                                                                       | Write '1' to disable interrupt for event RESOLVED    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                | Clear    | 1                                                                                     | Disable                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                | Disabled | 0                                                                                     | Read: Disabled                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                | Enabled  | 1                                                                                     | Read: Enabled                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW NOTRESOLVED |          |                                                                                       | Write '1' to disable interrupt for event NOTRESOLVED |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                | Clear    | 1                                                                                     | Disable                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                | Disabled | 0                                                                                     | Read: Disabled                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                | Enabled  | 1                                                                                     | Read: Enabled                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.5.6.13 STATUS

Address offset: 0x400

Resolution status

|                  |            |          |         |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          |         | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          |         | A A A A                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          |         | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value   | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | R STATUS   |          | [0..15] | The IRK that was used last time an address was resolved                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.5.6.14 ENABLE

Address offset: 0x500

Enable AAR

|                  |      |        |          |                                                                                       |                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|--------|----------|---------------------------------------------------------------------------------------|-----------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |        |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |        |          | A A                                                                                   |                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |        |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field  | Value ID | Value                                                                                 | Description           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW   | ENABLE |          |                                                                                       | Enable or disable AAR |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |        | Disabled | 0                                                                                     | Disable               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |        | Enabled  | 3                                                                                     | Enable                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.5.6.15 NIRK

Address offset: 0x504

Number of IRKs

|                  |  |  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               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| Bit number       |  |  | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         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| ID               |  |  | A A A A A                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     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| Reset 0x00000001 |  |  | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 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0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.5.6.16 IRKPTR

Address offset: 0x508

Pointer to IRK data structure

|                  |            |  |          |                                   |    |    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|-----------------------------------|----|----|----|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31                                | 30 | 29 | 28 | 27          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |  |          | A                                 | A  | A  | A  | A           | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |          | 0                                 | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID | Value                             |    |    |    | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW IRKPTR  |  |          | Pointer to the IRK data structure |    |    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.5.6.17 ADDRPTR

Address offset: 0x510

Pointer to the resolvable address

|                  |            |         |          |                                             |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|---------|----------|---------------------------------------------|----|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |         |          | 31                                          | 30 | 29          | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |         |          | A                                           | A  | A           | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |         |          | 0                                           | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |         | Value ID | Value                                       |    | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | ADDRPTR |          | Pointer to the resolvable address (6-bytes) |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.5.6.18 SCRATCHPTR

Address offset: 0x514

Pointer to data area used for temporary storage

|                  |            |  |            |       |    |    |                                                                                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|------------|-------|----|----|---------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |            | 31    | 30 | 29 | 28                                                                                                                        | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |  |            | A     | A  | A  | A                                                                                                                         | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |            | 0     | 0  | 0  | 0                                                                                                                         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID   | Value |    |    | Description                                                                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW         |  | SCRATCHPTR |       |    |    | Pointer to a scratch data area used for temporary storage during resolution. A space of minimum 3 bytes must be reserved. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

## 7.1.5.7 Electrical specification

### 7.1.5.7.1 AAR Electrical Specification

| Symbol      | Description                                                                                                                                                                               | Min. | Typ. | Max. | Units   |
|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|---------|
| $t_{AAR}$   | Address resolution time per IRK. Total time for several IRKs is given as $(1 \mu s + n * t_{AAR})$ , where n is the number of IRKs. (Given priority to the actual destination RAM block). | ..   | ..   | ..   | $\mu s$ |
| $t_{AAR,8}$ | Time for address resolution of 8 IRKs. (Given priority to the actual destination RAM block).                                                                                              | ..   | ..   | ..   | $\mu s$ |

## 7.1.6 CCM — AES CCM mode encryption

Counter with cipher block chaining - message authentication code (CCM) mode is an authenticated encryption algorithm designed to provide both authentication and confidentiality during data transfer.

AES CCM combines counter (CTR) mode encryption and cipher block chaining - message authentication code (CBC-MAC) authentication. The CCM terminology message authentication code (MAC) is called message integrity check (MIC) in *Bluetooth* terminology, and also in this document.

The CCM block generates an encrypted keystream that is applied to input data using the XOR operation, and generates the 4-byte MIC field in one operation. The CCM and the radio can be configured to work synchronously. The CCM will encrypt in time for transmission, and decrypt after receiving bytes into memory from the radio. All operations can complete within the packet receive (RX) or transmit (TX) time.

The CCM on this device is implemented according to *Bluetooth* requirements and the algorithm as defined in IETF [RFC3610](#), and depends on the AES-128 block cipher. A description of the CCM algorithm can also be found in [NIST Special Publication 800-38C](#). The *Bluetooth* specification describes the configuration of the counter mode blocks and the encryption blocks to implement compliant encryption for *Bluetooth* low energy.

The CCM block uses EasyDMA to load the key and the counter mode blocks (including the nonce required), and to read/write plain text and cipher text.

Three operations are supported:

- keystream generation
- packet encryption
- packet decryption

All operations are done in compliance with the *Bluetooth* specification.<sup>11</sup>

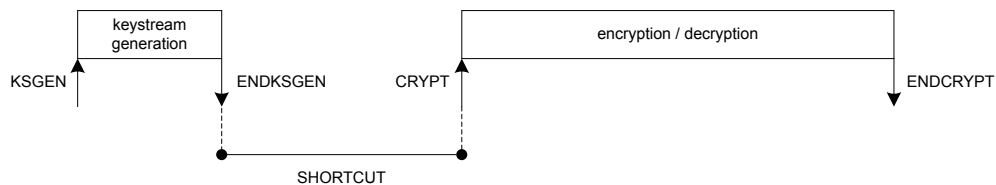


Figure 36: Keystream generation, followed by encryption or decryption. The shortcut is optional.

### 7.1.6.1 Shared resources

The CCM shares the same AES module as the ECB and AAR peripherals. The ECB will always have the lowest priority. If there is a sharing conflict during encryption, the ECB operation will be aborted and an `ERRORECB` event will be generated in the ECB peripheral.

Additionally, the CCM shares registers and other resources with other peripherals that have the same ID as the CCM. See [Peripherals with shared ID](#) on page 138 for more information.

### 7.1.6.2 Keystream generation

A new keystream needs to be generated before a new packet encryption or packet decryption operation can be started.

A keystream is generated by triggering the KSGEN task, and an `ENDKSGEN` event will be generated when the keystream has been generated.

Keystream generation, packet encryption, and packet decryption operations utilize the configuration specified in the data structure pointed to by `CNFPTR` on page 166. It is necessary to configure this pointer and its underlying data structure, and the register `MODE` on page 165, before the KSGEN task is triggered.

The keystream will be stored in the AES CCM's temporary memory area, specified by the `SCRATCHPTR` on page 167, where it will be used in subsequent encryption and decryption operations.

<sup>11</sup> *Bluetooth* AES CCM 128-bit block encryption, see *Bluetooth Core specification* version 4.0.

For default length packets (MODE.LENGTH = Default), the size of the generated keystream is 27 bytes. When using extended length packets (MODE.LENGTH = Extended), register [MAXPACKETSIZE](#) on page 167 specifies the length of the keystream to be generated. The length of the generated keystream must be greater than or equal to the length of the subsequent packet payload to be encrypted or decrypted. The maximum length of the keystream in extended mode is 251 bytes, which means that the maximum packet payload size is 251 bytes.

If a shortcut is used between ENDKSGEN event and CRYPT task, pointers [INPTR](#) on page 166 and [OUTPTR](#) on page 166 must also be configured before the KSGEN task is triggered.

### 7.1.6.3 Encryption

During packet encryption, the AES CCM will read the unencrypted packet located in RAM at the address specified by the INPTR pointer, encrypt the packet, and append a four byte long message integrity check (MIC) field to the packet.

The packet header (S0) and payload are included in the MIC generation. Bits in the packet header can be masked away by configuring register [HEADERMASK](#) on page 168.

Encryption is started by triggering the CRYPT task, by setting the register [MODE](#) on page 165 to [Encryption](#). An ENDCRYPT event will be generated when packet encryption is completed.

The AES CCM will also modify the length field of the packet to adjust for the appended MIC field, that is, add four bytes to the length, and store the resulting packet back into RAM at the address specified by the pointer [OUTPTR](#) on page 166.

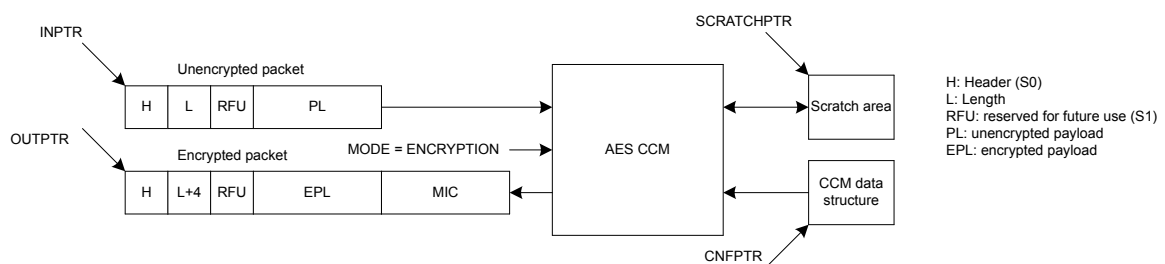


Figure 37: Encryption

Empty packets (length field is set to 0) will not be encrypted, but instead moved unmodified through the AES CCM.

The CCM supports different widths of the length field in the data structure for encrypted packets. This is configured in register [MODE](#) on page 165.

### 7.1.6.4 Decryption

During packet decryption, the AES CCM will read the encrypted packet located in RAM at the address specified by the INPTR pointer, decrypt the packet, authenticate the packet's MIC field, and generate the appropriate MIC status.

The packet header (S0) and payload are included in the MIC authentication. Bits in the packet header can be masked away by configuring register [HEADERMASK](#) on page 168.

Decryption is started by triggering the CRYPT task, by setting the register [MODE](#) on page 165 to [Decryption](#). An ENDCRYPT event will be generated when packet decryption is completed.

The AES CCM will also modify the length field of the packet to adjust for the MIC field, that is, subtract four bytes from the length, and then store the decrypted packet into RAM at the address specified by the pointer [OUTPTR](#) on page 166 pointer.

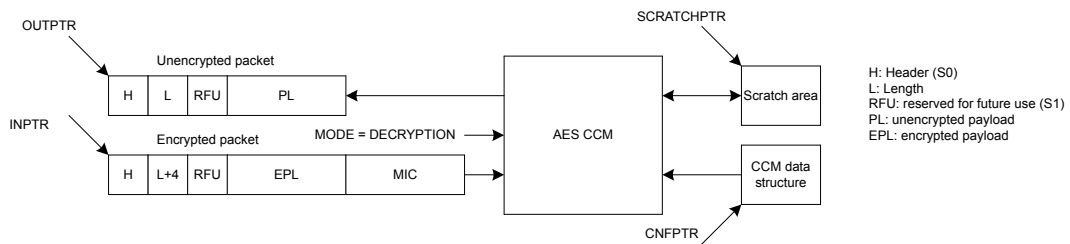


Figure 38: Decryption

The CCM is only able to decrypt packet payloads that are at least 5 bytes long, 1 byte or more encrypted payload (EPL) and 4 bytes of MIC. The CCM will therefore generate a MIC error for packets where the length field is set to 1, 2, 3 or 4. Empty packets (length field is set to 0) will not be decrypted, but instead moved unmodified through the AES CCM. These packets will always pass the MIC check.

The CCM supports different widths of the length field in the data structure for decrypted packets. This is configured in register [MODE](#) on page 165.

### 7.1.6.5 AES CCM and radio concurrent operation

The CCM module is able to encrypt/decrypt data synchronously to data being transmitted or received on the radio.

In order for the CCM module to run synchronously with the radio, the data rate setting in register [MODE](#) on page 165 needs to match the radio data rate. Settings in this register apply whenever either the KSGEN or the CRYPT task is triggered.

The data rate setting of the register [MODE](#) on page 165 can also be overridden on-the-fly, during an ongoing encrypt/decrypt operation, by the contents of the register [RATEOVERRIDE](#) on page 167. The data rate setting in this register applies whenever the RATEOVERRIDE task is triggered. This feature can be useful in cases where the radio data rate is changed during an ongoing packet transaction.

### 7.1.6.6 Encrypting packets on-the-fly in radio transmit mode

When the AES CCM is encrypting a packet on-the-fly, at the same time as the radio is transmitting it, the radio must read the encrypted packet from the same memory location the AES CCM is writing to.

The pointer [OUTPTR](#) on page 166 in the AES CCM must therefore point to the same memory location as the [PACKETPTR](#) pointer in the radio.

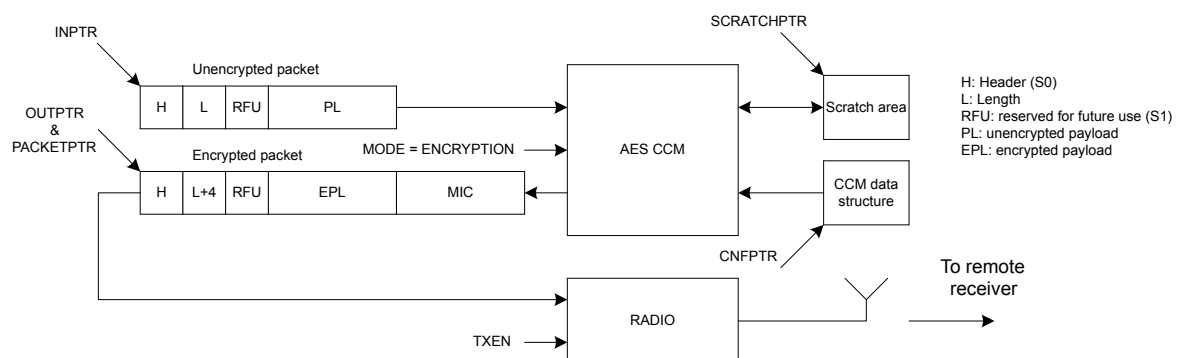


Figure 39: Configuration of on-the-fly encryption

In order to match the radio's timing, the KSGEN task must be triggered early enough to allow the keystream generation to complete before the encryption of the packet starts.

For short packets ([MODE.LENGTH](#) = Default), the KSGEN task must be triggered no later than when the radio START task is triggered. In addition, the shortcut between the ENDKSGEN event and the CRYPT task



must be enabled. This use case, using a programmable peripheral interconnect (PPI) connection between the READY event in the radio and the KSGEN task in the AES CCM, is illustrated in figure below.

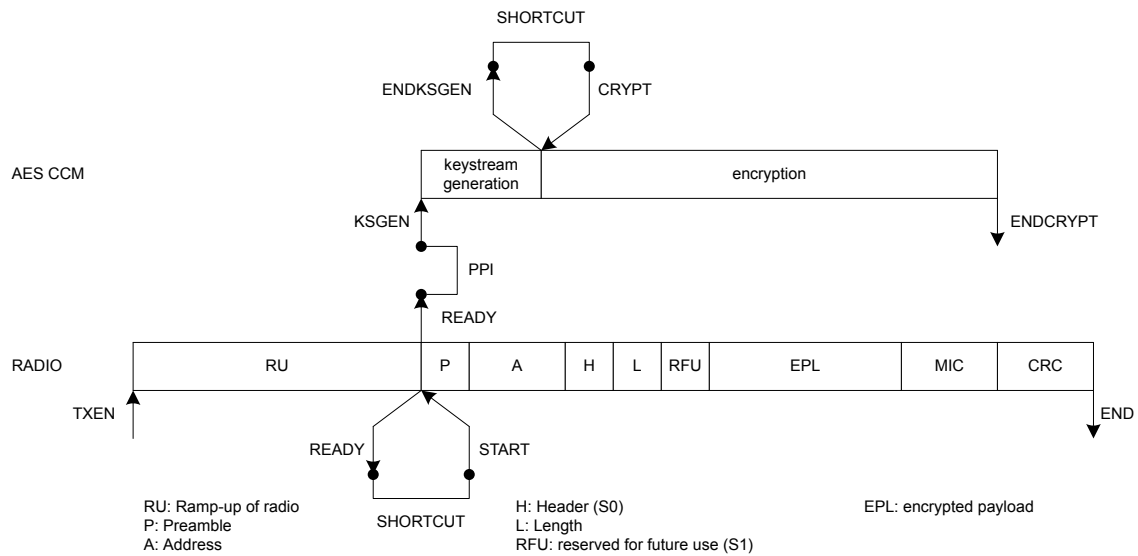


Figure 40: On-the-fly encryption of short packets (MODE.LENGTH = Default), using a PPI connection

For long packets (MODE.LENGTH = Extended), the keystream generation will need to be started even earlier, for example at the time when the TXEN task in the radio is triggered.

**Note:** See [Timing specification](#) on page 168 for information about the time needed for generating a keystream.

### 7.1.6.7 Decrypting packets on-the-fly in radio receive mode

When the AES CCM is decrypting a packet on-the-fly, at the same time as the radio is receiving it, the AES CCM must read the encrypted packet from the same memory location that the radio is writing to.

The pointer [INPTR](#) on page 166 in the AES CCM must therefore point to the same memory location as the [PACKETPTR](#) pointer in the radio.

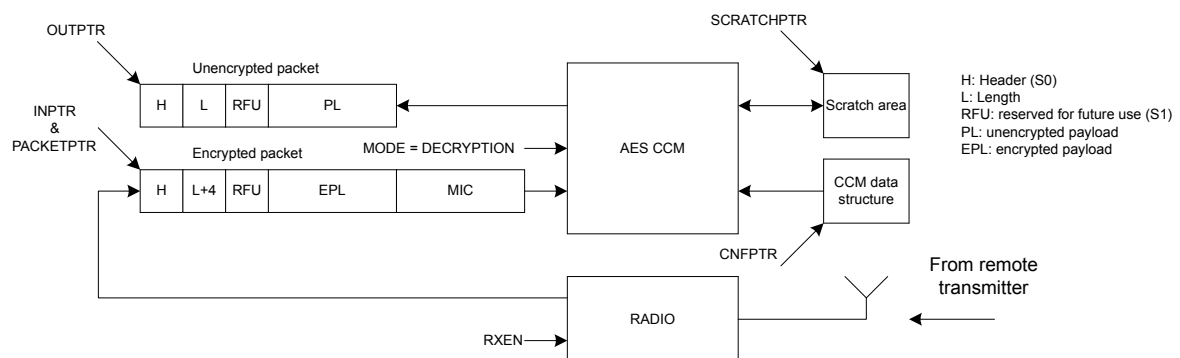


Figure 41: Configuration of on-the-fly decryption

In order to match the radio's timing, the KSGEN task must be triggered early enough to allow the keystream generation to complete before the decryption of the packet starts.

For short packets (MODE.LENGTH = Default), the KSGEN task must be triggered no later than when the START task in the radio is triggered. In addition, the CRYPT task must not be triggered earlier than when the ADDRESS event is generated by the radio. If the CRYPT task is triggered exactly at the same time as the ADDRESS event is generated by the radio, the AES CCM will guarantee that the decryption is completed no

later than when the END event in the radio is generated. This use case, using a PPI connection between the ADDRESS event in the radio and the CRYPT task in the AES CCM, is illustrated in figure below.

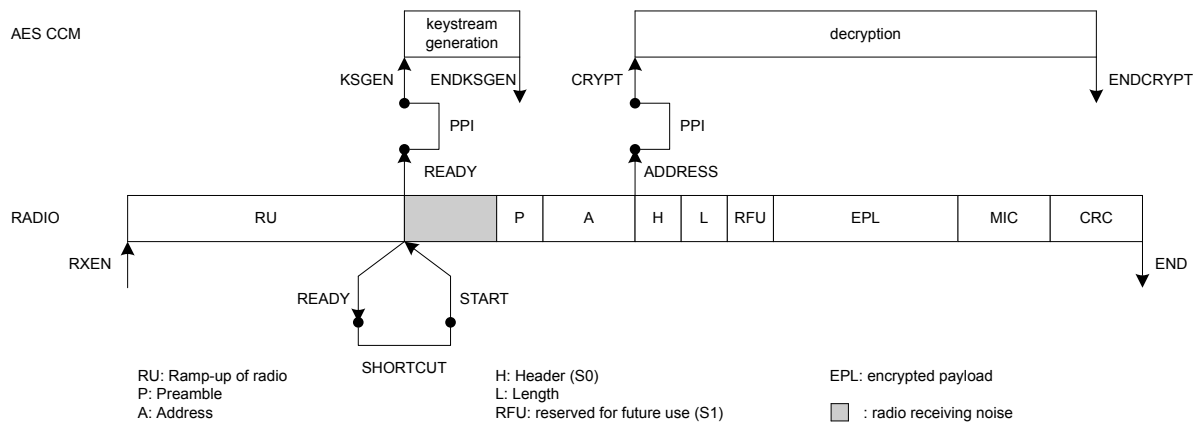


Figure 42: On-the-fly decryption of short packets (MODE.LENGTH = Default), using a PPI connection

The KSGEN task is triggered from the READY event in the radio, through a PPI connection.

For long packets (MODE.LENGTH = Extended), the keystream generation will need to be started even earlier, for example at the time when the RXEN task in the radio is triggered.

**Note:** See [Timing specification](#) on page 168 for information about the time needed for generating a keystream.

### 7.1.6.8 CCM data structure

The CCM data structure is located in data RAM, at the memory location specified by the CNFPTR pointer register.

| Property | Address offset | Description                                                                                                                   |
|----------|----------------|-------------------------------------------------------------------------------------------------------------------------------|
| KEY      | 0              | 16-byte AES key.                                                                                                              |
| PKTCTR   | 16             | Octet0 (least significant octet (LSO)) of packet. counter                                                                     |
|          | 17             | Octet1 of packet counter.                                                                                                     |
|          | 18             | Octet2 of packet counter.                                                                                                     |
|          | 19             | Octet3 of packet counter.                                                                                                     |
|          | 20             | Bit 6 – bit 0: Octet4 (7 most significant bits of packet counter, with bit 6 being the most significant bit). Bit 7: Ignored. |
|          | 21             | Ignored.                                                                                                                      |
|          | 22             | Ignored.                                                                                                                      |
|          | 23             | Ignored.                                                                                                                      |
|          | 24             | Bit 0: Direction bit. Bit 7 – bit 1: Zero padded.                                                                             |
| IV       | 25             | 8-byte initialization vector (IV). Octet0 (LSO) of IV, Octet1 of IV, ..., Octet7 (MSO) of IV.                                 |

Table 56: CCM data structure overview

The NONCE vector (as specified by the *Bluetooth* Core Specification) will be generated by hardware based on the information specified in the CCM data structure.

| Property | Address offset | Description                            |
|----------|----------------|----------------------------------------|
| HEADER   | 0              | Packet header                          |
| LENGTH   | 1              | Number of bytes in unencrypted payload |
| RFU      | 2              | Reserved for future use                |
| PAYLOAD  | 3              | Unencrypted payload                    |

Table 57: Data structure for unencrypted packet

| Property                                                                                     | Address offset     | Description                                                  |
|----------------------------------------------------------------------------------------------|--------------------|--------------------------------------------------------------|
| HEADER                                                                                       | 0                  | Packet header                                                |
| LENGTH                                                                                       | 1                  | Number of bytes in encrypted payload including length of MIC |
| <b>Note:</b> LENGTH will be 0 for empty packets since the MIC is not added to empty packets. |                    |                                                              |
| RFU                                                                                          | 2                  | Reserved for future use                                      |
| PAYLOAD                                                                                      | 3                  | Encrypted payload                                            |
| MIC                                                                                          | 3 + payload length | ENCRYPT: 4-byte encrypted MIC                                |
| <b>Note:</b> MIC is not added to empty packets.                                              |                    |                                                              |

Table 58: Data structure for encrypted packet

### 7.1.6.9 EasyDMA and ERROR event

The CCM implements an EasyDMA mechanism for reading from and writing to RAM.

In cases where the CPU and other EasyDMA enabled peripherals are accessing the same RAM block at the same time, a high level of bus collisions may cause operation that is too slow for correct on-the-fly encryption. In this case, the ERROR event will be generated.

EasyDMA will have finished accessing the RAM when the ENDKSGEN and ENDCRYPT events are generated.

If the pointers CNFPTR, SCRATCHPTR, INPTR and the OUTPTR are not pointing to the data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See [Memory](#) on page 18 for more information about the different memory regions.

### 7.1.6.10 Registers

| Base address | Domain  | Peripheral | Instance | Secure mapping | DMA security | Description             | Configuration |
|--------------|---------|------------|----------|----------------|--------------|-------------------------|---------------|
| 0x4100E000   | NETWORK | CCM        | CCM      | NS             | NA           | AES CCM mode encryption |               |

Table 59: Instances

| Register               | Offset | Security | Description                                                                                                                     |
|------------------------|--------|----------|---------------------------------------------------------------------------------------------------------------------------------|
| TASKS_KSGEN            | 0x000  |          | Start generation of keystream. This operation will stop by itself when completed.                                               |
| TASKS_CRYPT            | 0x004  |          | Start encryption/decryption. This operation will stop by itself when completed.                                                 |
| TASKS_STOP             | 0x008  |          | Stop encryption/decryption                                                                                                      |
| TASKS_RATEOVERRIDE     | 0x00C  |          | Override DATARATE setting in MODE register with the contents of the RATEOVERRIDE register for any ongoing encryption/decryption |
| SUBSCRIBE_KSGEN        | 0x080  |          | Subscribe configuration for task KSGEN                                                                                          |
| SUBSCRIBE_CRYPT        | 0x084  |          | Subscribe configuration for task CRYPT                                                                                          |
| SUBSCRIBE_STOP         | 0x088  |          | Subscribe configuration for task STOP                                                                                           |
| SUBSCRIBE_RATEOVERRIDE | 0x08C  |          | Subscribe configuration for task RATEOVERRIDE                                                                                   |
| EVENTS_ENDKSGEN        | 0x100  |          | Keystream generation complete                                                                                                   |

| Register         | Offset | Security | Description                                                                                         |
|------------------|--------|----------|-----------------------------------------------------------------------------------------------------|
| EVENTS_ENDCRYPT  | 0x104  |          | Encrypt/decrypt complete                                                                            |
| EVENTS_ERROR     | 0x108  |          | CCM error event <span style="float: right;">Deprecated</span>                                       |
| PUBLISH_ENDKSGEN | 0x180  |          | Publish configuration for event <a href="#">ENDKSGEN</a>                                            |
| PUBLISH_ENDCRYPT | 0x184  |          | Publish configuration for event <a href="#">ENDCRYPT</a>                                            |
| PUBLISH_ERROR    | 0x188  |          | Publish configuration for event <a href="#">ERROR</a> <span style="float: right;">Deprecated</span> |
| SHORTS           | 0x200  |          | Shortcuts between local events and tasks                                                            |
| INTENSET         | 0x304  |          | Enable interrupt                                                                                    |
| INTENCLR         | 0x308  |          | Disable interrupt                                                                                   |
| MICSTATUS        | 0x400  |          | MIC check result                                                                                    |
| ENABLE           | 0x500  |          | Enable                                                                                              |
| MODE             | 0x504  |          | Operation mode                                                                                      |
| CNFPTR           | 0x508  |          | Pointer to data structure holding the AES key and the NONCE vector                                  |
| INPTR            | 0x50C  |          | Input pointer                                                                                       |
| OUTPTR           | 0x510  |          | Output pointer                                                                                      |
| SCRATCHPTR       | 0x514  |          | Pointer to data area used for temporary storage                                                     |
| MAXPACKETSIZE    | 0x518  |          | Length of keystream generated when MODE.LENGTH = Extended                                           |
| RATEOVERRIDE     | 0x51C  |          | Data rate override setting.                                                                         |
| HEADERMASK       | 0x520  |          | Header (S0) mask.                                                                                   |

Table 60: Register overview

### 7.1.6.10.1 TASKS\_KSGEN

Address offset: 0x000

Start generation of keystream. This operation will stop by itself when completed.

|                  |            |             |                                                                                       |   |       |                                                                                   |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|-------------|---------------------------------------------------------------------------------------|---|-------|-----------------------------------------------------------------------------------|-------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |             | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |   |       |                                                                                   |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |             | A                                                                                     |   |       |                                                                                   |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |             | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |   |       |                                                                                   |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field |             | Value ID                                                                              |   | Value |                                                                                   | Description |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W          | TASKS_KSGEN |                                                                                       |   |       | Start generation of keystream. This operation will stop by itself when completed. |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Trigger     |                                                                                       | 1 |       | Trigger task                                                                      |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.6.10.2 TASKS\_CRYPT

Address offset: 0x004

Start encryption/decryption. This operation will stop by itself when completed.

|                  |            |             |                                                                                       |  |                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|-------------|---------------------------------------------------------------------------------------|--|---------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |             | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |             | A                                                                                     |  |                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |             | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |  |                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID    | Value                                                                                 |  | Description                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W          | TASKS_CRYPT |                                                                                       |  | Start encryption/decryption. This operation will stop by itself when completed. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Trigger     | 1                                                                                     |  | Trigger task                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.6.10.3 TASKS\_STOP

Address offset: 0x008

Stop encryption/decryption

|                  |            |            |          |   |       |  |             |                            |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|------------|----------|---|-------|--|-------------|----------------------------|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |            |          |   |       |  |             |                            |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |            |          |   |       |  |             |                            |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |   |
| Reset 0x00000000 |            |            |          |   |       |  |             |                            |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |            | Value ID |   | Value |  | Description |                            |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_STOP |          |   |       |  |             | Stop encryption/decryption |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Trigger    |          | 1 |       |  |             | Trigger task               |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.6.10.4 TASKS\_RATEOVERRIDE

Address offset: 0x00C

Override DATARATE setting in MODE register with the contents of the RATEOVERRIDE register for any ongoing encryption/decryption

|                  |      |                    |                                                                                       |    |       |                                                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|--------------------|---------------------------------------------------------------------------------------|----|-------|---------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |                    | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |    |       |                                                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |                    | A                                                                                     |    |       |                                                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |                    | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |    |       |                                                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field              | Value                                                                                 | ID | Value | Description                                                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W    | TASKS_RATEOVERRIDE |                                                                                       |    |       | Override DATARATE setting in MODE register with the contents of the RATEOVERRIDE register for any ongoing encryption/decryption |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                    | Trigger                                                                               | 1  |       | Trigger task                                                                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

#### 7.1.6.10.5 SUBSCRIBE\_KSGEN

Address offset: 0x080

Subscribe configuration for task **KSGEN**

|                  |            |          |          |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|----------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          |          | B A A A A A A A                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value    | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0] | Channel that task <span style="color: #0070C0;">KSGEN</span> will subscribe to        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW EN      |          |          |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0        | Disable subscription                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1        | Enable subscription                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

#### 7.1.6.10.6 SUBSCRIBE\_CRYPT

Address offset: 0x084

Subscribe configuration for task **CRYPT**

|                  |            |       |          |                                                                         |                      |                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-------|----------|-------------------------------------------------------------------------|----------------------|--------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |       |          | 31                                                                      | 30                   | 29                                                     | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |       |          | B                                                                       |                      |                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |       |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |                      |                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field |       | Value ID | Value                                                                   |                      | Description                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | CHIDX |          | [255..0]                                                                |                      | Channel that task <span>CRYPT</span> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW         | EN    |          |                                                                         |                      |                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |       | Disabled | 0                                                                       | Disable subscription |                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |       | Enabled  | 1                                                                       | Enable subscription  |                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |



|                  |            |                 |       |                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|------------------|------------|-----------------|-------|--------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|---|
| Bit number       |            |                 |       | 31                       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |   |
| ID               |            |                 |       |                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | A |
| Reset 0x00000000 |            |                 |       | 0                        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |   |
| ID               | Acce Field | Value ID        | Value | Description              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
| A                | RW         | EVENTS_ENDCRYPT |       | Encrypt/decrypt complete |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | NotGenerated    | 0     | Event not generated      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | Generated       | 1     | Event generated          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |

#### 7.1.6.10.11 EVENTS\_ERROR ( Deprecated )

Address offset: 0x108

CCM error event

|                  |            |              |       |                                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |            |
|------------------|------------|--------------|-------|---------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|------------|
| Bit number       |            |              |       | 31                                                                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |            |
| ID               |            |              |       | A                                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |            |
| Reset 0x00000000 |            |              |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |            |
| ID               | Acce Field | Value ID     | Value | Description                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |            |
| A                | RW         | EVENTS_ERROR |       | CCM error event                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  | Deprecated |
|                  |            | NotGenerated | 0     | Event not generated                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |            |
|                  |            | Generated    | 1     | Event generated                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |            |

Deprecated

#### 7.1.6.10.12 PUBLISH\_ENDKSGEN

Address offset: 0x180

Publish configuration for event [ENDKSGEN](#)

|                  |            |  |  |          |    |          |    |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|--|----------|----|----------|----|-----------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |  | 31       | 30 | 29       | 28 | 27                                                  | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |  |  | B        |    |          |    |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   |   |   |   |   |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |  | 0        |    |          |    |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  |  | Value ID |    | Value    |    | Description                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |  |          |    | [255..0] |    | Channel that event <b>ENDKSGEN</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |  |          |    |          |    |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  |  | Disabled |    | 0        |    | Disable publishing                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  |  | Enabled  |    | 1        |    | Enable publishing                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.6.10.13 PUBLISH\_ENDCRYPT

Address offset: 0x184

Publish configuration for event [ENDCRYPT](#)

|                  |            |  |  |          |    |          |    |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|--|----------|----|----------|----|-----------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |  | 31       | 30 | 29       | 28 | 27                                                  | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |  |  | B        |    |          |    |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   |   |   |   |   |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |  | 0        |    |          |    |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  |  | Value ID |    | Value    |    | Description                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |  |          |    | [255..0] |    | Channel that event <b>ENDCRYPT</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |  |          |    |          |    |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  |  | Disabled |    | 0        |    | Disable publishing                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  |  | Enabled  |    | 1        |    | Enable publishing                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.6.10.14 PUBLISH\_ERROR ( Deprecated )

Address offset: 0x188

Publish configuration for event **ERROR**

|                  |      |          |                                                                                       |    |       |                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------|----------|---------------------------------------------------------------------------------------|----|-------|-----------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |      |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |    |       |                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |      |          | B                                                                                     |    |       |                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |    |       |                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce | Field    | Value                                                                                 | ID | Value | Description                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW   | CHIDX    | [255..0]                                                                              |    |       | Channel that event <a href="#">ERROR</a> will publish to. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW   | EN       |                                                                                       |    |       |                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      | Disabled | 0                                                                                     |    |       | Disable publishing                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      | Enabled  | 1                                                                                     |    |       | Enable publishing                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

### 7.1.6.10.15 SHORTS

Address offset: 0x200

## Shortcuts between local events and tasks

|                  |            |                |          |       |                                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------------|----------|-------|--------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                |          |       | 31                                                                       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |                |          |       | A                                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |                |          |       | 0                                                                        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |                | Value ID | Value | Description                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | ENDKSGEN_CRYPT |          |       | Shortcut between event <span>ENDKSGEN</span> and task <span>CRYPT</span> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled       |          | 0     | Disable shortcut                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled        |          | 1     | Enable shortcut                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.6.10.16 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number       |      |          |          | 31 | 30                                                               | 29          | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
|------------------|------|----------|----------|----|------------------------------------------------------------------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ID               |      |          |          |    |                                                                  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | C | B | A |
| Reset 0x00000000 |      |          |          | 0  | 0                                                                | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |
| ID               | Acce | Field    | Value    | ID | Value                                                            | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW   | ENDKSGEN |          |    | Write '1' to enable interrupt for event <a href="#">ENDKSGEN</a> |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |          | Set      | 1  | Enable                                                           |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |          | Disabled | 0  | Read: Disabled                                                   |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |          | Enabled  | 1  | Read: Enabled                                                    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW   | ENDCRYPT |          |    | Write '1' to enable interrupt for event <a href="#">ENDCRYPT</a> |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |          | Set      | 1  | Enable                                                           |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |          | Disabled | 0  | Read: Disabled                                                   |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |          | Enabled  | 1  | Read: Enabled                                                    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| C                | RW   | ERROR    |          |    | Write '1' to enable interrupt for event <a href="#">ERROR</a>    | Deprecated  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |          | Set      | 1  | Enable                                                           |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |          | Disabled | 0  | Read: Disabled                                                   |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |          | Enabled  | 1  | Read: Enabled                                                    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.6.10.17 INTENCLR

Address offset: 0x308

## Disable interrupt



| Bit number       |      |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                |       |                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|----------|---------------------------------------------------------------------------------------|----------------|-------|----------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |      |          | C B A                                                                                 |                |       |                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                         |                |       |                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field    | Value                                                                                 | ID             | Value | Description                                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW   | ENDKSGEN |                                                                                       |                |       | Write '1' to disable interrupt for event <a href="#">ENDKSGEN</a>                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Clear    | 1                                                                                     | Disable        |       |                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Disabled | 0                                                                                     | Read: Disabled |       |                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Enabled  | 1                                                                                     | Read: Enabled  |       |                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW   | ENDCRYPT |                                                                                       |                |       | Write '1' to disable interrupt for event <a href="#">ENDCRYPT</a>                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Clear    | 1                                                                                     | Disable        |       |                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Disabled | 0                                                                                     | Read: Disabled |       |                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Enabled  | 1                                                                                     | Read: Enabled  |       |                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW   | ERROR    |                                                                                       |                |       | Write '1' to disable interrupt for event <a href="#">ERROR</a> <span>Deprecated</span> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Clear    | 1                                                                                     | Disable        |       |                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Disabled | 0                                                                                     | Read: Disabled |       |                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Enabled  | 1                                                                                     | Read: Enabled  |       |                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

#### 7.1.6.10.18 MICSTATUS

Address offset: 0x400

## MIC check result

|                  |      |           |             |    |                  |                                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|------------------|------|-----------|-------------|----|------------------|--------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|--|
| Bit number       |      |           |             | 31 | 30               | 29                                                                             | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |
| ID               |      |           |             | A  |                  |                                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| Reset 0x00000000 |      |           |             | 0  | 0                | 0                                                                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |  |
| ID               | Acce | Field     | Value       | ID | Value            | Description                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| A                | R    | MICSTATUS |             |    |                  | The result of the MIC check performed during the previous decryption operation |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |      |           | CheckFailed | 0  | MIC check failed |                                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |      |           | CheckPassed | 1  | MIC check passed |                                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |

### 7.1.6.10.19 ENABLE

Address offset: 0x500

Enable

|                  |            |        |          |       |    |                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |  |
|------------------|------------|--------|----------|-------|----|-----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|---|--|
| Bit number       |            |        |          | 31    | 30 | 29                    | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |   |  |
| ID               |            |        |          | A     |    |                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | A |  |
| Reset 0x00000000 |            |        |          | 0     | 0  | 0                     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |   |  |
| ID               | Acce Field |        | Value ID | Value |    | Description           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |  |
| A                | RW         | ENABLE |          |       |    | Enable or disable CCM |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |  |
|                  |            |        | Disabled | 0     |    | Disable               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |  |
|                  |            |        | Enabled  | 2     |    | Enable                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |  |

#### 7.1.6.10.20 MODE

Address offset: 0x504

### Operation mode

| Bit number       |      |          | 31                                                                    | 30    | 29                                                                                                                                                                      | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |
|------------------|------|----------|-----------------------------------------------------------------------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|
| ID               |      |          | C                                                                     |       |                                                                                                                                                                         |    |    |    |    |    |    |    | B  |    | B  |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |  |  |  |
| Reset 0x00000001 |      |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 |       |                                                                                                                                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
| ID               | Acce | Field    | Value ID                                                              | Value | Description                                                                                                                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
| A                | RW   | MODE     |                                                                       |       | The mode of operation to be used. Settings in this register apply whenever either the KSGEN task or the CRYPT task is triggered.                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |          | Encryption                                                            | 0     | AES CCM packet encryption mode                                                                                                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |          | Decryption                                                            | 1     | AES CCM packet decryption mode                                                                                                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |          |                                                                       |       |                                                                                                                                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
| B                | RW   | DATARATE |                                                                       |       | Radio data rate that the CCM shall run synchronous with                                                                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |          | 1Mbit                                                                 | 0     | 1 Mbps                                                                                                                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |          | 2Mbit                                                                 | 1     | 2 Mbps                                                                                                                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |          | 125Kbps                                                               | 2     | 125 Kbps                                                                                                                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |          | 500Kbps                                                               | 3     | 500 Kbps                                                                                                                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
| C                | RW   | LENGTH   |                                                                       |       | Packet length configuration                                                                                                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |          | Default                                                               | 0     | Default length. Effective length of LENGTH field in encrypted/decrypted packet is 5 bits. A keystream for packet payloads up to 27 bytes will be generated.             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |          | Extended                                                              | 1     | Extended length. Effective length of LENGTH field in encrypted/decrypted packet is 8 bits. A keystream for packet payloads up to MAXPACKETSIZE bytes will be generated. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |

#### 7.1.6.10.21 CNFPTR

Address offset: 0x508

Pointer to data structure holding the AES key and the NONCE vector

|                  |            |  |          |       |    |    |    |                                                                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|-------|----|----|----|--------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31    | 30 | 29 | 28 | 27                                                                                                                 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |  |          | A     | A  | A  | A  | A                                                                                                                  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |          | 0     | 0  | 0  | 0  | 0                                                                                                                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID | Value |    |    |    | Description                                                                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW         |  | CNFPTR   |       |    |    |    | Pointer to the data structure holding the AES key and the CCM NONCE vector (see table CCM data structure overview) |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 7.1.6.10.22 INPTR

Address offset: 0x50C

Input pointer

|                  |            |          |       |    |    |    |               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|-------|----|----|----|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          | 31    | 30 | 29 | 28 | 27            | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |          | A     | A  | A  | A  | A             | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          | 0     | 0  | 0  | 0  | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID | Value |    |    |    | Description   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | INPTR    |       |    |    |    | Input pointer |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 7.1.6.10.23 OUTPTR

Address offset: 0x510

Output pointer

|                  |            |  |          |       |    |    |    |                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|-------|----|----|----|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31    | 30 | 29 | 28 | 27             | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |  |          | A     | A  | A  | A  | A              | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |          | 0     | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID | Value |    |    |    | Description    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW         |  | OUTPTR   |       |    |    |    | Output pointer |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 7.1.6.10.24 SCRATCHPTR

Address offset: 0x514

Pointer to data area used for temporary storage

| Bit number       |      |            | 31    | 30 | 29    | 28                                                                                                                                                                                                                                                                                                                                                                                                                               | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |
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| ID               |      |            |       | A  | A     | A                                                                                                                                                                                                                                                                                                                                                                                                                                | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |  |  |  |  |
| Reset 0x00000000 |      |            | 0     | 0  | 0     | 0                                                                                                                                                                                                                                                                                                                                                                                                                                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |  |
| ID               | Acce | Field      | Value | ID | Value | Description                                                                                                                                                                                                                                                                                                                                                                                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| A                | RW   | SCRATCHPTR |       |    |       | <p>Pointer to a scratch data area used for temporary storage during keystream generation, MIC generation and encryption/decryption.</p> <p>The scratch area is used for temporary storage of data during keystream generation and encryption.</p> <p>When MODE.LENGTH = Default, a space of 43 bytes is required for this temporary storage. When MODE.LENGTH = Extended, a space of (16 + MAXPACKETSIZE) bytes is required.</p> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |

#### 7.1.6.10.25 MAXPACKETSIZE

Address offset: 0x518

Length of keystream generated when MODE.LENGTH = Extended

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#### 7.1.6.10.26 RATEOVERRIDE

Address offset: 0x51C

Data rate override setting.

Override value to be used instead of the setting of MODE.DATARATE. This override value applies when the RATEOVERRIDE task is triggered.

|                  |            |  |              |  |       |  |                            |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|--------------|--|-------|--|----------------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |              |  |       |  |                            |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |  |              |  |       |  |                            |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A | A |   |   |
| Reset 0x00000000 |            |  |              |  |       |  |                            |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID     |  | Value |  | Description                |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         |  | RATEOVERRIDE |  |       |  | Data rate override setting |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | 1Mbit        |  | 0     |  | 1 Mbps                     |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | 2Mbit        |  | 1     |  | 2 Mbps                     |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | 125Kbps      |  | 2     |  | 125 Kbps                   |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | 500Kbps      |  | 3     |  | 500 Kbps                   |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.6.10.27 HEADERMASK

Address offset: 0x520

Header (S0) mask.

Bitmask for packet header (S0) before MIC generation/authentication.

|                  |            |  |            |       |                  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|------------|-------|------------------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |            | 31    | 30               | 29          | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |  |            |       |                  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A | A | A | A | A | A | A | A | A |
| Reset 0x000000E3 |            |  |            | 0     | 0                | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |   |
| ID               | Acce Field |  | Value ID   | Value |                  | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         |  | HEADERMASK |       | Header (S0) mask |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.6.11 Electrical specification

#### 7.1.6.11.1 Timing specification

| Symbol            | Description                                                                           | Min. | Typ. | Max. | Units         |
|-------------------|---------------------------------------------------------------------------------------|------|------|------|---------------|
| $t_{\text{ngen}}$ | Time needed for keystream generation (given priority access to destination RAM block) | ..   | ..   | ..   | $\mu\text{s}$ |

## 7.1.7 COMP — Comparator

The comparator (COMP) compares an input voltage (VIN+) against a second input voltage (VIN-). VIN+ can be derived from an analog input pin (AIN0-AIN7). VIN- can be derived from multiple sources depending on the operation mode of the comparator.

Main features of the comparator are:

- Input range from 0 V to VDD
- Single-ended mode
  - Fully flexible hysteresis using a 64-level reference ladder
- Differential mode
  - Configurable hysteresis
- Reference inputs (VREF):
  - VDD
  - External reference from AIN0 to AIN7 (between 0 V and VDD)
  - Internal references 1.2 V, 1.8 V and 2.4 V
- Three speed/power consumption modes: low-power, normal and high-speed
- Single-pin capacitive sensor support

- Event generation on output changes
  - UP event on  $V_{IN-} > V_{IN+}$
  - DOWN event on  $V_{IN-} < V_{IN+}$
  - CROSS event on  $V_{IN+}$  and  $V_{IN-}$  crossing
  - READY event on core and internal reference (if used) ready

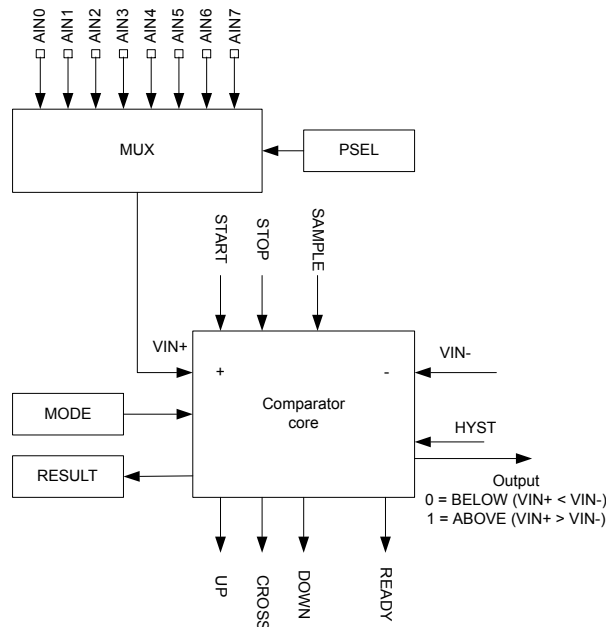


Figure 43: Comparator overview

Once enabled (using the [ENABLE](#) register), the comparator is started by triggering the START task and stopped by triggering the STOP task. The comparator will generate a READY event to indicate when it is ready for use and the output is correct. The delay between START and READY is  $t_{INT\_REF,START}$  if an internal reference is selected, or  $t_{COMP,START}$  if an external reference is used. When the COMP module is started, events will be generated every time  $V_{IN+}$  crosses  $V_{IN-}$ .

## Operation modes

The comparator can be configured to operate in two main operation modes, differential mode and single-ended mode. See the [MODE](#) register for more information. In both operation modes, the comparator can operate in different speed and power consumption modes (low-power, normal and high-speed). High-speed mode will consume more power compared to low-power mode, and low-power mode will result in slower response time compared to high-speed mode.

Use the [PSEL](#) register to select any of the AIN0-AIN7 pins as  $V_{IN+}$  input, regardless of the operation mode selected for the comparator. The source of  $V_{IN-}$  depends on which operation mode is used:

- Differential mode: Derived directly from AIN0 to AIN7
- Single-ended mode: Derived from VREF. VREF can be derived from VDD, AIN0-AIN7 or internal 1.2 V, 1.8 V and 2.4 V references.

The selected analog pins will be acquired by the comparator once it is enabled.

An optional hysteresis on  $V_{IN+}$  and  $V_{IN-}$  can be enabled when the module is used in differential mode through the [HYST](#) register. In single-ended mode, VUP and VDOWN thresholds can be set to implement a hysteresis using the reference ladder (see [Figure 46: Comparator in single-ended mode](#) on page 172). This hysteresis is in the order of magnitude of  $V_{DIFFHYST}$ , and shall prevent noise on the signal to create unwanted events. See [Figure 47: Hysteresis example where  \$V\_{IN+}\$  starts below VUP](#) on page 172 for illustration of the effect of an active hysteresis on a noisy input signal.

An upward crossing will generate an UP event and a downward crossing will generate a DOWN event. The CROSS event will be generated every time there is a crossing, independent of direction.

The immediate value of the comparator can be sampled to [RESULT](#) register by triggering the SAMPLE task.

## ISOURCE

A selectable current can be applied (ISOURCE register) on the currently selected AINx line. Enabling the block creates a feedback path around the comparator, forming a relaxation oscillator. The circuit will sink current from VIN+ when the comparator output is high, and source current into VIN+ when the comparator output is low. The frequency of the oscillator is dependent on the capacitance at the analog input pin, the reference voltages and the value of the current source. In this mode, only a capacitive sensor needs to be attached between the analog input pin and ground. With a selected current of 10 µA, VUP-VDOWN equal to 1 V, and an external capacity of typically 10 pF, the resulting oscillation frequency is around 500 kHz.

The frequency of the oscillator can be calculated as

$$f_{\_OSC} = I\_SOURCE / (2C \cdot (VUP - VDOWN) )$$

### 7.1.7.1 Shared resources

The COMP shares analog resources with SAADC. While it is possible to use the SAADC at the same time as the COMP, selecting the same analog input pin for both modules is not supported.

Additionally, COMP shares registers and other resources with other peripherals that have the same ID as the COMP. See [Peripherals with shared ID](#) on page 138 for more information.

The COMP peripheral shall not be disabled (by writing to the ENABLE register) before the peripheral has been stopped. Failing to do so may result in unpredictable behavior.

### 7.1.7.2 Differential mode

In differential mode, the reference input VIN- is derived directly from one of the AINx pins.

Before enabling the comparator via the [ENABLE](#) register, the following registers must be configured for the differential mode:

- [PSEL](#)
- [MODE](#)
- [EXTREFSEL](#)

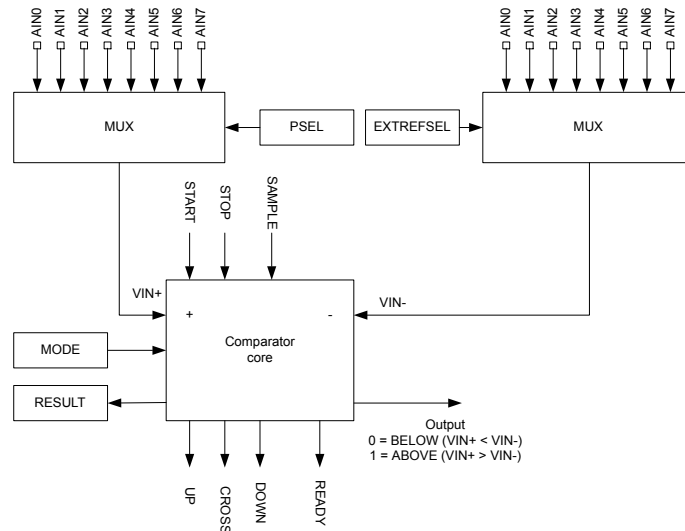


Figure 44: Comparator in differential mode

**Note:** Depending on the device, not all the analog inputs may be available for each MUX. See definitions for [PSEL](#) and [EXTREFSEL](#) for more information about which analog pins are available on a particular device.

When [HYST](#) register is turned on while in this mode, the output of the comparator (and associated events) will change from ABOVE to BELOW whenever  $V_{IN+}$  becomes lower than  $V_{IN-} - (V_{DIFFHYST} / 2)$ . It will also change from BELOW to ABOVE whenever  $V_{IN+}$  becomes higher than  $V_{IN-} + (V_{DIFFHYST} / 2)$ . This behavior is illustrated in [Figure 45: Hysteresis enabled in differential mode](#) on page 171.

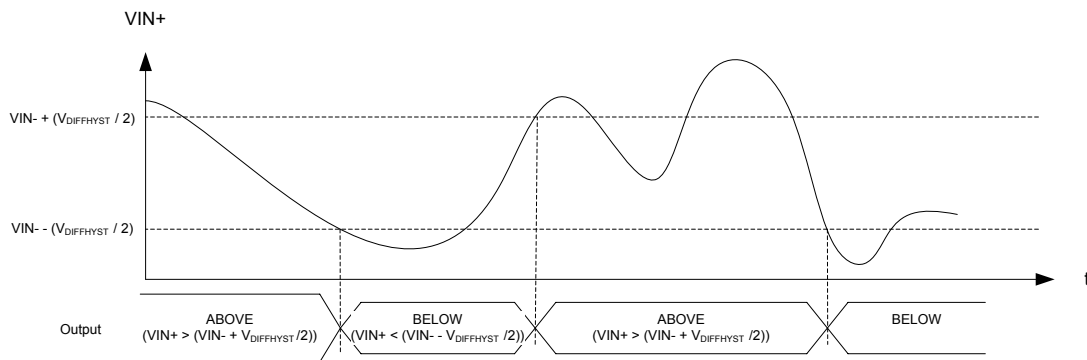


Figure 45: Hysteresis enabled in differential mode

### 7.1.7.3 Single-ended mode

In single-ended mode,  $V_{IN-}$  is derived from the reference ladder.

Before enabling the comparator via the [ENABLE](#) register, the following registers must be configured for the single-ended mode:

- [PSEL](#)
- [MODE](#)
- [REFSEL](#)
- [EXTREFSEL](#)
- [TH](#)

The reference ladder uses the reference voltage ( $V_{REF}$ ) to derive two new voltage references,  $V_{UP}$  and  $V_{DOWN}$ .  $V_{UP}$  and  $V_{DOWN}$  are configured using  $TH_{UP}$  and  $TH_{DOWN}$  respectively in the [TH](#) register.  $V_{REF}$

can be derived from any of the available reference sources, configured using the [EXTREFSEL](#) and [REFSEL](#) registers as illustrated in [Figure 46: Comparator in single-ended mode](#) on page 172. When AREF is selected in the [REFSEL](#) register, the [EXTREFSEL](#) register is used to select one of the AIN0-AIN7 analog input pins as reference input. The selected analog pins will be acquired by the comparator once it is enabled.

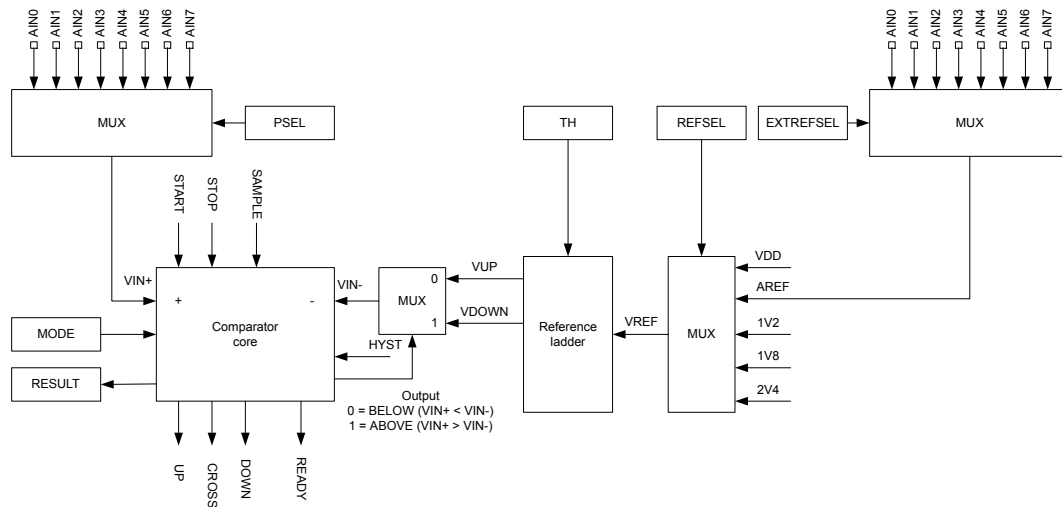


Figure 46: Comparator in single-ended mode

**Note:** Depending on the device, not all the analog inputs may be available for each MUX. See definitions for [PSEL](#) and [EXTREFSEL](#) for more information about which analog pins are available on a particular device.

When the comparator core detects that  $VIN+ > VIN-$ , i.e. ABOVE as per the [RESULT](#) register,  $VIN-$  will switch to  $VDOWN$ . When  $VIN+$  falls below  $VIN-$  again,  $VIN-$  will be switched back to  $VUP$ . By specifying  $VUP$  larger than  $VDOWN$ , a hysteresis can be generated as illustrated in [Figure 47: Hysteresis example where  \$VIN+\$  starts below  \$VUP\$](#)  on page 172 and [Figure 48: Hysteresis example where  \$VIN+\$  starts above  \$VUP\$](#)  on page 173.

Writing to [HYST](#) has no effect in single-ended mode, and the content of this register is ignored.

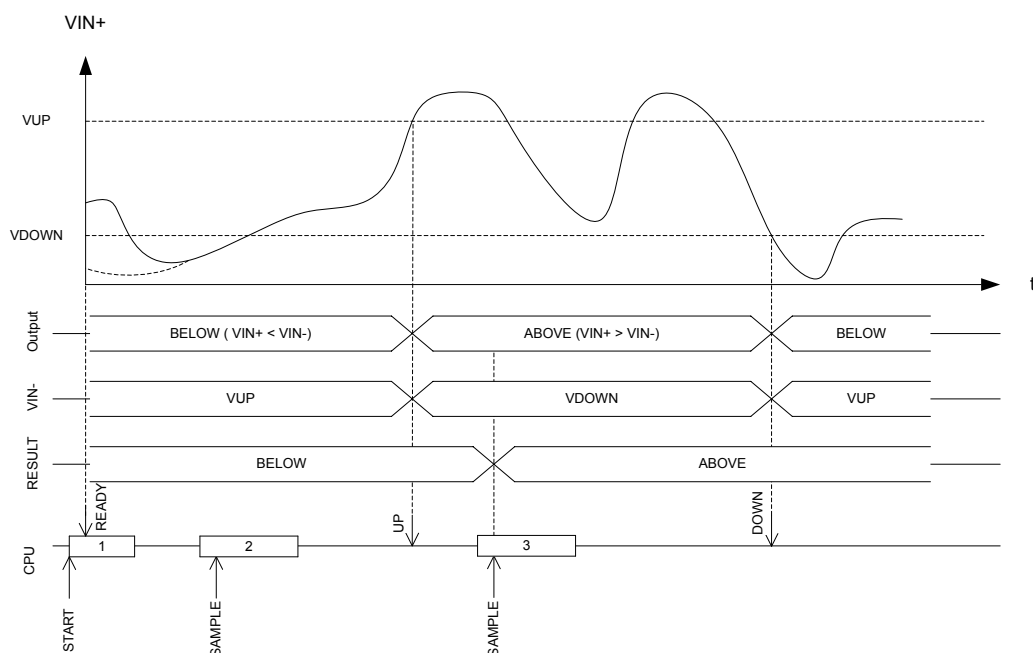


Figure 47: Hysteresis example where  $VIN+$  starts below  $VUP$



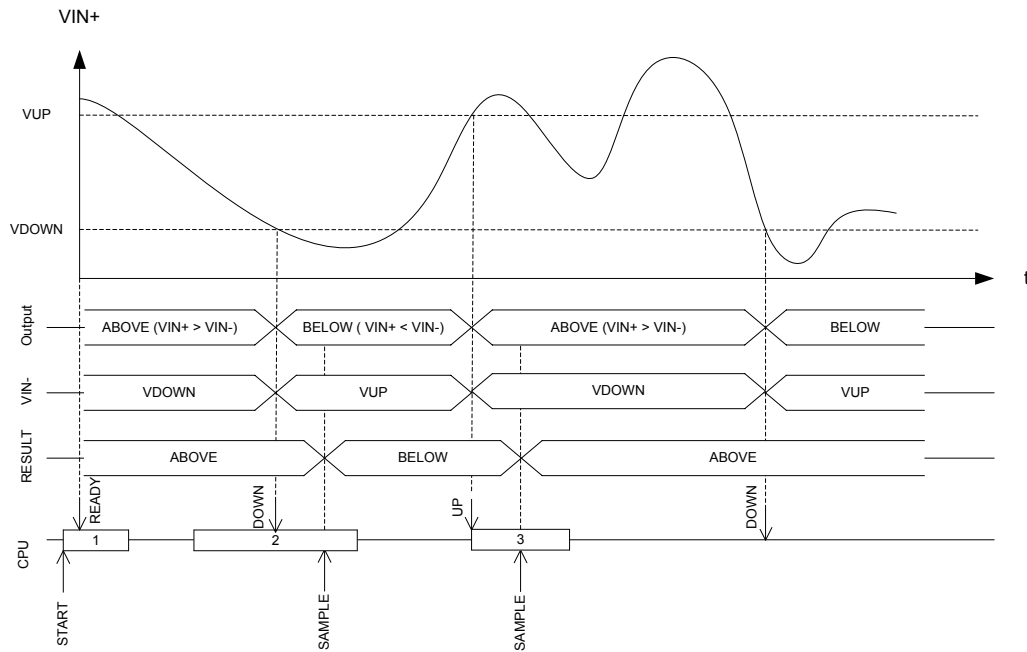


Figure 48: Hysteresis example where VIN+ starts above VUP

### 7.1.7.4 Registers

| Base address | Domain      | Peripheral | Instance  | Secure mapping | DMA security | Description | Configuration |
|--------------|-------------|------------|-----------|----------------|--------------|-------------|---------------|
| 0x5001A000   | APPLICATION | COMP       | COMP : S  | US             | NA           | Comparator  |               |
| 0x4001A000   |             |            | COMP : NS |                |              |             |               |

Table 61: Instances

| Register         | Offset | Security | Description                                             |
|------------------|--------|----------|---------------------------------------------------------|
| TASKS_START      | 0x000  |          | Start comparator                                        |
| TASKS_STOP       | 0x004  |          | Stop comparator                                         |
| TASKS_SAMPLE     | 0x008  |          | Sample comparator value                                 |
| SUBSCRIBE_START  | 0x080  |          | Subscribe configuration for task <a href="#">START</a>  |
| SUBSCRIBE_STOP   | 0x084  |          | Subscribe configuration for task <a href="#">STOP</a>   |
| SUBSCRIBE_SAMPLE | 0x088  |          | Subscribe configuration for task <a href="#">SAMPLE</a> |
| EVENTS_READY     | 0x100  |          | COMP is ready and output is valid                       |
| EVENTS_DOWN      | 0x104  |          | Downward crossing                                       |
| EVENTS_UP        | 0x108  |          | Upward crossing                                         |
| EVENTS_CROSS     | 0x10C  |          | Downward or upward crossing                             |
| PUBLISH_READY    | 0x180  |          | Publish configuration for event <a href="#">READY</a>   |
| PUBLISH_DOWN     | 0x184  |          | Publish configuration for event <a href="#">DOWN</a>    |
| PUBLISH_UP       | 0x188  |          | Publish configuration for event <a href="#">UP</a>      |
| PUBLISH_CROSS    | 0x18C  |          | Publish configuration for event <a href="#">CROSS</a>   |
| SHORTS           | 0x200  |          | Shortcuts between local events and tasks                |
| INTEN            | 0x300  |          | Enable or disable interrupt                             |
| INTENSET         | 0x304  |          | Enable interrupt                                        |
| INTENCLR         | 0x308  |          | Disable interrupt                                       |
| RESULT           | 0x400  |          | Compare result                                          |
| ENABLE           | 0x500  |          | COMP enable                                             |
| PSEL             | 0x504  |          | Pin select                                              |
| REFSEL           | 0x508  |          | Reference source select for single-ended mode           |

| Register  | Offset | Security | Description                                 |
|-----------|--------|----------|---------------------------------------------|
| EXTREFSEL | 0x50C  |          | External reference select                   |
| TH        | 0x530  |          | Threshold configuration for hysteresis unit |
| MODE      | 0x534  |          | Mode configuration                          |
| HYST      | 0x538  |          | Comparator hysteresis enable                |
| ISOURCE   | 0x53C  |          | Current source select on analog input       |

Table 62: Register overview

#### 7.1.7.4.1 TASKS\_START

Address offset: 0x000

Start comparator

|                  |            |             |          |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|-------------|----------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |             |          |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |             |          |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |             |          |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field |             | Value ID | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W          | TASKS_START |          |       | Start comparator                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |             | Trigger  | 1     | Trigger task                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

#### 7.1.7.4.2 TASKS\_STOP

Address offset: 0x004

Stop comparator

|                  |              |  |          |       |                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|--------------|--|----------|-------|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |              |  |          |       | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |              |  |          |       |                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |
| Reset 0x00000000 |              |  |          |       | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field   |  | Value ID | Value | Description     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | W TASKS_STOP |  |          |       | Stop comparator |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |              |  | Trigger  | 1     | Trigger task    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.7.4.3 TASKS\_SAMPLE

Address offset: 0x008

Sample comparator value

|                  |                |  |          |       |                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|----------------|--|----------|-------|-------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |                |  |          |       | 31                      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |                |  |          |       |                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |
| Reset 0x00000000 |                |  |          |       | 0                       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field     |  | Value ID | Value | Description             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | W TASKS_SAMPLE |  |          |       | Sample comparator value |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |                |  | Trigger  | 1     | Trigger task            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.7.4.4 SUBSCRIBE\_START

Address offset: 0x080

Subscribe configuration for task **START**

|                  |            |          |          |    |                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|----|--------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          | 31       | 30 | 29                                                     | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |          | B        |    |                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   | A | A | A | A | A | A |
| Reset 0x00000000 |            |          | 0        | 0  | 0                                                      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce Field | Value ID | Value    |    | Description                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] |    | Channel that task <span>START</span> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |    |                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        |    | Disable subscription                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        |    | Enable subscription                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.7.4.5 SUBSCRIBE\_STOP

Address offset: 0x084

Subscribe configuration for task **STOP**

|                  |            |  |          |  |          |  |                                                 |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|--|----------|--|-------------------------------------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          |  |          |  |                                                 |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |
| ID               |            |  |          |  |          |  |                                                 |  |  | B  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  |    |    |    |   |   |   |   |   |   | A | A | A | A | A | A | A |   |
| Reset 0x00000000 |            |  |          |  |          |  |                                                 |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID |  | Value    |  | Description                                     |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          |  | [255..0] |  | Channel that task <b>STOP</b> will subscribe to |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |  |          |  |                                                 |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled |  | 0        |  | Disable subscription                            |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  |  | 1        |  | Enable subscription                             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.7.4.6 SUBSCRIBE\_SAMPLE

Address offset: 0x088

Subscribe configuration for task **SAMPLE**

|                  |            |  |          |          |    |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|----------|----|---------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31       | 30 | 29                                                | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |
| ID               |            |  |          | B        |    |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |          | 0        | 0  | 0                                                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |   |
| ID               | Acce Field |  | Value ID | Value    |    | Description                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          | [255..0] |    | Channel that task <b>SAMPLE</b> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |          |    |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled | 0        |    | Disable subscription                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  | 1        |    | Enable subscription                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.7.4.7 EVENTS\_READY

Address offset: 0x100

COMP is ready and output is valid

|                  |                 |              |       |                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|-----------------|--------------|-------|-----------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |                 |              |       | 31                                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |                 |              |       |                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |
| Reset 0x00000000 |                 |              |       | 0                                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |
| ID               | Acce Field      | Value ID     | Value | Description                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW EVENTS_READY |              |       | COMP is ready and output is valid |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |                 | NotGenerated | 0     | Event not generated               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |                 | Generated    | 1     | Event generated                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.7.4.8 EVENTS\_DOWN

Address offset: 0x104

Downward crossing

|                  |            |              |       |                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|------------------|------------|--------------|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|---|
| Bit number       |            |              |       | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |   |
| ID               |            |              |       |                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  | A |
| Reset 0x00000000 |            |              |       | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |   |
| ID               | Acce Field | Value ID     | Value | Description         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
| A                | RW         | EVENTS_DOWN  |       | Downward crossing   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|                  |            | NotGenerated | 0     | Event not generated |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|                  |            | Generated    | 1     | Event generated     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |

### 7.1.7.4.9 EVENTS\_UP

Address offset: 0x108

Upward crossing

|                  |            |  |              |  |       |  |                     |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|--------------|--|-------|--|---------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |              |  |       |  |                     |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |  |              |  |       |  |                     |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |
| Reset 0x00000000 |            |  |              |  |       |  |                     |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID     |  | Value |  | Description         |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         |  | EVENTS_UP    |  |       |  | Upward crossing     |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | NotGenerated |  | 0     |  | Event not generated |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Generated    |  | 1     |  | Event generated     |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.7.4.10 EVENTS\_CROSS

Address offset: 0x10C

Downward or upward crossing

|                  |            |              |       |                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------------|-------|-----------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |              |       | 31                          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |              |       |                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |
| Reset 0x00000000 |            |              |       | 0                           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |
| ID               | Acce Field | Value ID     | Value | Description                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | EVENTS_CROSS |       | Downward or upward crossing |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | NotGenerated | 0     | Event not generated         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Generated    | 1     | Event generated             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.7.4.11 PUBLISH\_READY

Address offset: 0x180

Publish configuration for event [READY](#)

|                  |            |          |          |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|--------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                                               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |          |          | B                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   |   |   |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |          |          | 0                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID | Value    | Description                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] | Channel that event <b>READY</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        | Disable publishing                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        | Enable publishing                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.7.4.12 PUBLISH\_DOWN

Address offset: 0x184

Publish configuration for event **DOWN**

|                  |            |  |          |          |    |                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|----------|----|-------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31       | 30 | 29                                              | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |  |          | B        |    |                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   |   |   |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |          | 0        |    |                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID | Value    |    | Description                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          | [255..0] |    | Channel that event <b>DOWN</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |          |    |                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled | 0        |    | Disable publishing                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  | 1        |    | Enable publishing                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.7.4.13 PUBLISH\_UP

Address offset: 0x188

Publish configuration for event **UP**

|                  |            |  |          |          |                    |                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|----------|--------------------|----------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31       | 30                 | 29                                     | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |  |          | B        |                    |                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |          | 0        | 0                  | 0                                      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce Field |  | Value ID | Value    |                    | Description                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          | [255..0] |                    | Channel that event UP will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |          |                    |                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled | 0        | Disable publishing |                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  | 1        | Enable publishing  |                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.7.4.14 PUBLISH\_CROSS

Address offset: 0x18C

Publish configuration for event **CROSS**

|                  |            |  |          |          |    |                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|----------|----|-------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31       | 30 | 29                                        | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |  |          | B        |    |                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   |   |   |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |          | 0        |    |                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID | Value    |    | Description                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          | [255..0] |    | Channel that event CROSS will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |          |    |                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled | 0        |    | Disable publishing                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  | 1        |    | Enable publishing                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.7.4.15 SHORTS

Address offset: 0x200

Shortcuts between local events and tasks

| Bit number       |      |              | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|--------------|---------------------------------------------------------------------------------------|-------|------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |      |              | E D C B A                                                                             |       |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |              | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |       |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field        | Value ID                                                                              | Value | Description                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW   | READY_SAMPLE |                                                                                       |       | Shortcut between event <span>READY</span> and task <span>SAMPLE</span> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |              | Disabled                                                                              | 0     | Disable shortcut                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |              | Enabled                                                                               | 1     | Enable shortcut                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW   | READY_STOP   |                                                                                       |       | Shortcut between event <span>READY</span> and task <span>STOP</span>   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |              | Disabled                                                                              | 0     | Disable shortcut                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |              | Enabled                                                                               | 1     | Enable shortcut                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW   | DOWN_STOP    |                                                                                       |       | Shortcut between event <span>DOWN</span> and task <span>STOP</span>    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |              | Disabled                                                                              | 0     | Disable shortcut                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |              | Enabled                                                                               | 1     | Enable shortcut                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| D                | RW   | UP_STOP      |                                                                                       |       | Shortcut between event <span>UP</span> and task <span>STOP</span>      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |              | Disabled                                                                              | 0     | Disable shortcut                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |              | Enabled                                                                               | 1     | Enable shortcut                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| E                | RW   | CROSS_STOP   |                                                                                       |       | Shortcut between event <span>CROSS</span> and task <span>STOP</span>   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |              | Disabled                                                                              | 0     | Disable shortcut                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |              | Enabled                                                                               | 1     | Enable shortcut                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.7.4.16 INTEN

Address offset: 0x300

Enable or disable interrupt

| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|----------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |            |          | D C B A                                                                               |                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| D                | Acce Field | Value ID | Value                                                                                 | Description                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW READY   |          |                                                                                       | Enable or disable interrupt for event <span>READY</span> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Disable                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Enable                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW DOWN    |          |                                                                                       | Enable or disable interrupt for event <span>DOWN</span>  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Disable                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Enable                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW UP      |          |                                                                                       | Enable or disable interrupt for event <span>UP</span>    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Disable                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Enable                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| D                | RW CROSS   |          |                                                                                       | Enable or disable interrupt for event <span>CROSS</span> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Disable                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Enable                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.7.4.17 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number       |      |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|-------|---------------------------------------------------------------------------------------|-------|------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |      |       | D C B A                                                                               |       |                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |       |                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field | Value ID                                                                              | Value | Description                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW   | READY |                                                                                       |       | Write '1' to enable interrupt for event <span>READY</span> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Set                                                                                   | 1     | Enable                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Disabled                                                                              | 0     | Read: Disabled                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Enabled                                                                               | 1     | Read: Enabled                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW   | DOWN  |                                                                                       |       | Write '1' to enable interrupt for event <span>DOWN</span>  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Set                                                                                   | 1     | Enable                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Disabled                                                                              | 0     | Read: Disabled                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Enabled                                                                               | 1     | Read: Enabled                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW   | UP    |                                                                                       |       | Write '1' to enable interrupt for event <span>UP</span>    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Set                                                                                   | 1     | Enable                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Disabled                                                                              | 0     | Read: Disabled                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Enabled                                                                               | 1     | Read: Enabled                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| D                | RW   | CROSS |                                                                                       |       | Write '1' to enable interrupt for event <span>CROSS</span> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Set                                                                                   | 1     | Enable                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Disabled                                                                              | 0     | Read: Disabled                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Enabled                                                                               | 1     | Read: Enabled                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

#### 7.1.7.4.18 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number       |      |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|-------|---------------------------------------------------------------------------------------|-------|-------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |      |       | D C B A                                                                               |       |                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |       |                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field | Value ID                                                                              | Value | Description                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW   | READY |                                                                                       |       | Write '1' to disable interrupt for event <span>READY</span> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Clear                                                                                 | 1     | Disable                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Disabled                                                                              | 0     | Read: Disabled                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Enabled                                                                               | 1     | Read: Enabled                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW   | DOWN  |                                                                                       |       | Write '1' to disable interrupt for event <span>DOWN</span>  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Clear                                                                                 | 1     | Disable                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Disabled                                                                              | 0     | Read: Disabled                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Enabled                                                                               | 1     | Read: Enabled                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW   | UP    |                                                                                       |       | Write '1' to disable interrupt for event <span>UP</span>    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Clear                                                                                 | 1     | Disable                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Disabled                                                                              | 0     | Read: Disabled                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Enabled                                                                               | 1     | Read: Enabled                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| D                | RW   | CROSS |                                                                                       |       | Write '1' to disable interrupt for event <span>CROSS</span> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Clear                                                                                 | 1     | Disable                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Disabled                                                                              | 0     | Read: Disabled                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Enabled                                                                               | 1     | Read: Enabled                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

#### 7.1.7.4.19 RESULT

Address offset: 0x400

Compare result

|                  |            |        |          |       |    |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|------------------|------------|--------|----------|-------|----|-----------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|---|
| Bit number       |            |        |          | 31    | 30 | 29                                                  | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |   |
| ID               |            |        |          |       |    |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | A |
| Reset 0x00000000 |            |        |          | 0     | 0  | 0                                                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |   |
| ID               | Acce Field |        | Value ID | Value |    | Description                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
| A                | R          | RESULT |          |       |    | Result of last compare. Decision point SAMPLE task. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            |        | Below    | 0     |    | Input voltage is below the threshold (VIN+ < VIN-)  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            |        | Above    | 1     |    | Input voltage is above the threshold (VIN+ > VIN-)  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |

#### 7.1.7.4.20 ENABLE

Address offset: 0x500

COMP enable

|                  |            |  |          |  |       |  |                        |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|--|-------|--|------------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          |  |       |  |                        |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |  |          |  |       |  |                        |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | A | A |   |   |   |   |   |
| Reset 0x00000000 |            |  |          |  |       |  |                        |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID |  | Value |  | Description            |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         |  | ENABLE   |  |       |  | Enable or disable COMP |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled |  | 0     |  | Disable                |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  |  | 2     |  | Enable                 |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.7.4.21 PSEL

Address offset: 0x504

Pin select

|                  |      |       |              |    |       |                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------|-------|--------------|----|-------|-------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |      |       |              | 31 | 30    | 29                            | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |      |       |              |    |       |                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A | A | A |
| Reset 0x00000000 |      |       |              | 0  | 0     | 0                             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce | Field | Value        | ID | Value | Description                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW   | PSEL  |              |    |       | Analog pin select             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |       | AnalogInput0 |    | 0     | AIN0 selected as analog input |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |       | AnalogInput1 |    | 1     | AIN1 selected as analog input |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |       | AnalogInput2 |    | 2     | AIN2 selected as analog input |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |       | AnalogInput3 |    | 3     | AIN3 selected as analog input |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |       | AnalogInput4 |    | 4     | AIN4 selected as analog input |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |       | AnalogInput5 |    | 5     | AIN5 selected as analog input |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |       | AnalogInput6 |    | 6     | AIN6 selected as analog input |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |       | AnalogInput7 |    | 7     | AIN7 selected as analog input |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.7.4.22 REFSEL

Address offset: 0x508

Reference source select for single-ended mode



| Bit number       |            |          | 31    | 30 | 29                                                    | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |  |
|------------------|------------|----------|-------|----|-------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|--|
| ID               |            |          |       |    |                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | A | A | A |  |
| Reset 0x00000004 |            |          | 0     | 0  | 0                                                     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |   |   |  |
| ID               | Acce Field | Value ID | Value |    | Description                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |
| A                | RW         | REFSEL   |       |    | Reference select                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | Int1V2   | 0     |    | VREF = internal 1.2 V reference (VDD >= 1.7 V)        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | Int1V8   | 1     |    | VREF = internal 1.8 V reference (VDD >= VREF + 0.2 V) |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | Int2V4   | 2     |    | VREF = internal 2.4 V reference (VDD >= VREF + 0.2 V) |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | VDD      | 4     |    | VREF = VDD                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | ARef     | 5     |    | VREF = AREF                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |

#### 7.1.7.4.23 EXTREFSEL

Address offset: 0x50C

External reference select

| Bit number       |            |                  | 31    | 30                                    | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |  |
|------------------|------------|------------------|-------|---------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|--|
| ID               |            |                  |       |                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A | A | A |  |  |  |
| Reset 0x00000000 |            |                  | 0     | 0                                     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |  |  |  |
| ID               | Acce Field | Value ID         | Value | Description                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
| A                | RW         | EXTREFSEL        |       | External analog reference select      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            | AnalogReference0 | 0     | Use AIN0 as external analog reference |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            | AnalogReference1 | 1     | Use AIN1 as external analog reference |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            | AnalogReference2 | 2     | Use AIN2 as external analog reference |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            | AnalogReference3 | 3     | Use AIN3 as external analog reference |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            | AnalogReference4 | 4     | Use AIN4 as external analog reference |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            | AnalogReference5 | 5     | Use AIN5 as external analog reference |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            | AnalogReference6 | 6     | Use AIN6 as external analog reference |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            | AnalogReference7 | 7     | Use AIN7 as external analog reference |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |

#### 7.1.7.4.24 TH

Address offset: 0x530

Threshold configuration for hysteresis unit

|                  |            |          |        |                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|--------|----------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |        | 31                         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |
| ID               |            |          |        |                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | B  | B  | B  | B  | B | B |   |   |   |   |   |   |   |   |   |   | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |        | 0                          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |   |   |   |
| ID               | Acce Field | Value ID | Value  | Description                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW THDOWN  |          | [63:0] | VDOWN = (THDOWN+1)/64*VREF |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW THUP    |          | [63:0] | VUP = (THUP+1)/64*VREF     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.7.4.25 MODE

Address offset: 0x534

Mode configuration



| Symbol               | Description                                                     | Min. | Typ. | Max. | Units   |
|----------------------|-----------------------------------------------------------------|------|------|------|---------|
| $V_{VDD-VREF}$       | Required difference between VDD and a selected VREF, VDD > VREF | ..   | ..   | ..   | V       |
| $t_{INT\_REF,START}$ | Startup time for the internal bandgap reference                 | ..   | ..   | ..   | $\mu$ S |
| $E_{INT\_REF}$       | Internal bandgap reference error                                | ..   | ..   | ..   | %       |
| $V_{INPUTOFFSET}$    | Input offset                                                    | ..   | ..   | ..   | mV      |
| $t_{COMP,START}$     | Startup time for the comparator core                            | ..   | ..   | ..   | $\mu$ S |

## 7.1.8 CRYPTOCELL — ARM TrustZone CryptoCell 312

ARM TrustZone CryptoCell 312 (CRYPTOCELL) is a security subsystem which provides root of trust (RoT) and cryptographic services for a device.

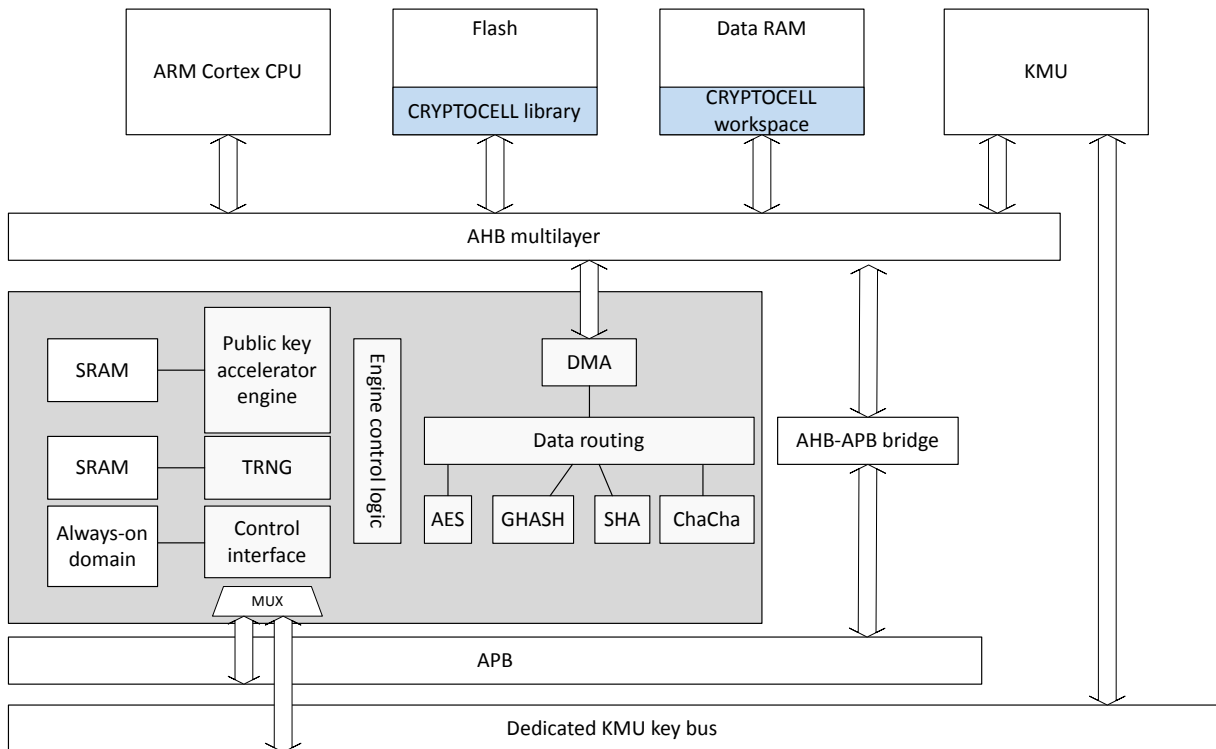


Figure 49: Block diagram for CRYPTOCELL

The following cryptographic features are provided:

- True random number generator (TRNG) compliant with NIST 800-90B, AIS-31, and FIPS 140-2
- Pseudorandom number generator (PRNG) using underlying AES engine compliant with NIST 800-90A
- RSA public key cryptography
  - Up to 3072-bit key size
  - PKCS#1 v2.1/v1.5
  - Optional CRT support
- Elliptic curve cryptography (ECC)
  - NIST FIPS 186-4 recommended curves using pseudorandom parameters, up to 521 bits:
    - Prime field: P-192, P-224, P-256, P-384, P-521
  - SEC 2 recommended curves using pseudorandom parameters, up to 521 bits:
    - Prime field: secp160r1, secp192r1, secp224r1, secp256r1, secp384r1, secp521r1
  - Koblitz curves using fixed parameters, up to 256 bits:

- Prime field: secp160k1, secp192k1, secp224k1, secp256k1
- Edwards/Montgomery curves:
  - Ed25519, Curve25519
- ECDH/ECDSA support
- Secure remote password protocol (SRP)
  - Up to 3072-bit operations
- Hashing functions
  - SHA-1, SHA-2 up to 256 bits
  - Keyed-hash message authentication code (HMAC)
- AES symmetric encryption
  - General purpose AES engine (encrypt/decrypt, sign/verify)
  - Supported key size: 128 and 256 bits
  - Supported encryption modes: ECB, CBC, CMAC/CBC-MAC, CTR, CCM/CCM\*, GCM
- ChaCha20/Poly1305 symmetric encryption
  - Supported key size: 128 and 256 bits
  - Authenticated encryption with associated data (AEAD) mode

### 7.1.8.1 Usage

The CRYPTOCELL state is controlled via a register interface. The cryptographic functions of CRYPTOCELL are accessible by using a software library provided in the device SDK, not directly via a register interface.

To enable CRYPTOCELL, use register [ENABLE](#) on page 186.

**WARNING:** Keeping the CRYPTOCELL subsystem enabled will prevent the device from reaching the System ON, All Idle state.

### 7.1.8.2 Direct memory access (DMA)

The CRYPTOCELL features a direct access memory (DMA) to allow cryptographic operations on memory mapped regions without involving the CPU.

The maximum DMA transaction size is limited to  $2^{16}-1$  bytes. See [Memory](#) on page 18 for information about what memories are accessible through the CRYPTOCELL DMA.

The CRYPTOCELL DMA can configure the security setting used for bus transactions.

Any data stored in memory type(s) not accessible by the CRYPTOCELL DMA engine must be copied to a memory type accessible by the direct memory before it can be processed by the CRYPTOCELL subsystem.

### 7.1.8.3 Standards

ARM TrustZone CryptoCell 312 (CRYPTOCELL) is compliant with the following protocol specifications and standards.

| Algorithm family | Identification code    | Document title                                                                                                                                                                                     |
|------------------|------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TRNG             | NIST SP 800-90B        | <i>Recommendation for the Entropy Sources Used for Random Bit Generation</i>                                                                                                                       |
|                  | AIS-31                 | <i>A proposal for: Functionality classes and evaluation methodology for physical random number generators</i>                                                                                      |
|                  | FIPS 140-2             | <i>Security Requirements for Cryptographic Modules</i>                                                                                                                                             |
| PRNG             | NIST SP 800-90A        | <i>Recommendation for Random Number Generation Using Deterministic Random Bit Generators</i>                                                                                                       |
| Stream cipher    | Chacha                 | <i>ChaCha, a variant of Salsa20</i> , Daniel J. Bernstein, January 28th 2008                                                                                                                       |
| MAC              | Poly1305               | <i>The Poly1305-AES message-authentication code</i> , Daniel J. Bernstein                                                                                                                          |
|                  |                        | <i>Cryptography in NaCl</i> , Daniel J. Bernstein                                                                                                                                                  |
| Key agreement    | SRP                    | <i>The Secure Remote Password Protocol</i> , Thomas Wu, November 11th 1997                                                                                                                         |
| Key derivation   | NIST SP 800-108        | <i>Recommendation for Key Derivation Using Pseudorandom Functions</i> . Compliant with section 5.1                                                                                                 |
| AES              | FIPS-197               | <i>Advanced Encryption Standard (AES)</i> . Compliant with 128-bit and 256-bit key size only                                                                                                       |
|                  | NIST SP 800-38A        | <i>Recommendation for Block Cipher Modes of Operation - Methods and Techniques</i> . Compliant with sections 6.1, 6.2, 6.4, and 6.5.                                                               |
|                  | NIST SP 800-38B        | <i>Recommendation for Block Cipher Modes of Operation: The CMAC Mode for Authentication</i>                                                                                                        |
|                  | NIST SP 800-38C        | <i>Recommendation for Block Cipher Modes of Operation: The CCM Mode for Authentication and Confidentiality</i>                                                                                     |
|                  | ISO/IEC 9797-1         | AES CBC-MAC per ISO/IEC 9797-1 MAC algorithm 1                                                                                                                                                     |
|                  | IEEE 802.15.4-2011     | <i>IEEE Standard for Local and metropolitan area networks - Part 15.4: Low-Rate Wireless Personal Area Networks (LR-WPANs)</i> , Annex B.4: <i>Specification of generic CCM* mode of operation</i> |
| Hash             | FIPS 180-3             | Secure Hash Standard (SHA1, SHA-224, SHA-256)                                                                                                                                                      |
|                  | RFC2104                | <i>HMAC: Keyed-Hashing for Message Authentication</i>                                                                                                                                              |
| RSA              | PKCS#1                 | <i>Public-Key Cryptography Standards (PKCS) #1: RSA Cryptography Specifications v1.5/2.1</i>                                                                                                       |
| Diffie-Hellman   | ANSI X9.42             | <i>Public Key Cryptography for the Financial Services Industry: Agreement of Symmetric Keys Using Discrete Logarithm Cryptography</i>                                                              |
|                  | PKCS#3                 | <i>Diffie-Hellman Key-Agreement Standard</i>                                                                                                                                                       |
| ECC              | ANSI X9.63             | <i>Public Key Cryptography for the Financial Services Industry - Key Agreement and Key Transport Using Elliptic Curve Cryptography</i>                                                             |
|                  | IEEE 1363              | <i>Standard Specifications for Public-Key Cryptography</i>                                                                                                                                         |
|                  | ANSI X9.62             | <i>Public Key Cryptography For The Financial Services Industry: The Elliptic Curve Digital Signature Algorithm (ECDSA)</i>                                                                         |
|                  | Ed25519                | Edwards-curve, <i>Ed25519: high-speed high-security signatures</i> , Daniel J. Bernstein, Niels Duif, Tanja Lange, Peter Schwabe, and Bo-Yin Yang                                                  |
|                  | Curve25519             | Montgomery curve, <i>Curve25519: new Diffie-Hellman speed records</i> , Daniel J. Bernstein                                                                                                        |
|                  | FIPS 186-4             | <i>Digital Signature Standard (DSS)</i> . Compliant with sections 5.1, 6.2, 6.3, 6.4, B.1.2, B.2.2, B.3.6, B.4.2, C.3.1, C.3.3, C.3.5, C.9, and D.1.2.                                             |
|                  | SEC 2                  | <i>Recommended Elliptic Curve Domain Parameters</i> , Certicom Research                                                                                                                            |
|                  | NIST SP 800-56A rev. 2 | <i>Recommendation for Pair-Wise Key Establishment Schemes Using Discrete Logarithm Cryptography</i>                                                                                                |

Table 63: CRYPTOCELL cryptography standards

### 7.1.8.4 Registers

| Base address | Domain      | Peripheral | Instance   | Secure mapping | DMA security | Description                            | Configuration |
|--------------|-------------|------------|------------|----------------|--------------|----------------------------------------|---------------|
| 0x50844000   | APPLICATION | CRYPTOCELL | CRYPTOCELL | S              | NSA          | CryptoCell subsystem control interface |               |

Table 64: Instances

| Register | Offset | Security | Description                  |
|----------|--------|----------|------------------------------|
| ENABLE   | 0x500  |          | Enable CRYPTOCELL subsystem. |

Table 65: Register overview

### 7.1.8.4.1 ENABLE

Address offset: 0x500

Enable CRYPTOCELL subsystem.

|                  |      |        |          |    |    |       |    |                                                                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------|--------|----------|----|----|-------|----|---------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |      |        | 31       | 30 | 29 | 28    | 27 | 26                                                                                                            | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |      |        |          |    |    |       |    |                                                                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | A |
| Reset 0x00000000 |      |        | 0        | 0  | 0  | 0     | 0  | 0                                                                                                             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce | Field  | Value    |    | ID | Value |    | Description                                                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW   | ENABLE |          |    |    |       |    | Enable or disable the CRYPTOCELL subsystem.                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |        | Disabled |    |    | 0     |    | CRYPTOCELL subsystem disabled.                                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |        | Enabled  |    |    | 1     |    | CRYPTOCELL subsystem enabled.                                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |        |          |    |    |       |    | When enabled, the CRYPTOCELL subsystem can be initialized and controlled through the CryptoCell firmware API. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

## 7.1.9 DCNF — Domain configuration

The domain configuration (DCNF) module provides a way to identify the CPU by its CPU ID in the device (CPUID). It also provides protection of the AHB multilayer interconnect (AMLI).

To provide for the AMLI protection, the DCNF contains configuration registers that can be used to block some paths from the AHB masters to their respective AHB slaves in the AMLI.

For an illustration of how the AHB masters and slaves are connected through the AMLI, see [Memory](#) on page 18.

### 7.1.9.1 Protection

The DCNF protection involves blocking of paths from AHB masters in an external core to the AHB slaves in the local core's AMLI. This way, the local core's internal resources can be blocked from masters in an external core. A set of configuration registers is used to control this behavior.

See [Memory](#) on page 18 to get an overview of the AMLI.

The DCNF configuration registers that are enabling the DCNF protection are listed below.

- [EXTPERI\[n\].PROTECT](#)
- [EXTRAM\[n\].PROTECT](#)
- [EXTCODE\[n\].PROTECT](#)

An attempt to access the blocked resources will trigger a BusFault or a HardFault exception, depending on the value of the BUSFAULTENA bit in the ARM Cortex-M33 SHCSR (system handler control and state register), described in the *ARM Cortex-M33 Devices Generic User Guide*.

### RAM protection

The protection of RAM regions is configured through the SLAVE-bits of the corresponding master ports' register [EXTRAM\[n\].PROTECT](#).

### Peripheral protection

The protection of peripheral memory regions is configured through the SLAVE-bits of the corresponding master ports' register [EXTPERI\[n\].PROTECT](#).

## Code protection

The protection of code memory regions is configured through the SLAVE-bits of the corresponding master ports' register `EXTCODE[0].PROTECT`.

### 7.1.9.2 Registers

| Base address | Domain      | Peripheral | Instance  | Secure mapping | DMA security | Description          | Configuration                                                                                                                                       |
|--------------|-------------|------------|-----------|----------------|--------------|----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x50000000   | APPLICATION | DCNF       | DCNF : S  | US             | NA           | Domain configuration | CPUID value is 0x00000000                                                                                                                           |
| 0x40000000   |             |            | DCNF : NS |                |              |                      |                                                                                                                                                     |
| 0x41000000   | NETWORK     | DCNF       | DCNF      | NS             | NA           | Domain configuration | Registers<br>EXTPERI[n].PROTECT,<br>EXTRAM[n].PROTECT and<br>EXTCODE[n].PROTECT not<br>available for network core.<br><br>CPUID value is 0x00000001 |

Table 66: Instances

| Register           | Offset | Security | Description                                                         |
|--------------------|--------|----------|---------------------------------------------------------------------|
| CPUID              | 0x420  |          | CPU ID of this subsystem                                            |
| EXTPERI[n].PROTECT | 0x440  |          | Control access for master connected to AMLI master port EXTPERI[n]  |
| EXTRAM[n].PROTECT  | 0x460  |          | Control access from master connected to AMLI master port EXTRAM[n]  |
| EXTCODE[n].PROTECT | 0x480  |          | Control access from master connected to AMLI master port EXTCODE[n] |

Table 67: Register overview

#### 7.1.9.2.1 CPUID

Address offset: 0x420

CPU ID of this subsystem

|                  |            |       |  |          |        |  |       |  |  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-------|--|----------|--------|--|-------|--|--|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |       |  |          |        |  |       |  |  | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |       |  |          |        |  |       |  |  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  | A  | A  | A  | A | A | A | A |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |       |  |          |        |  |       |  |  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |       |  | Value ID |        |  | Value |  |  | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | R          | CPUID |  |          | CPU ID |  |       |  |  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.9.2.2 EXTPERI[n].PROTECT (n=0..0)

Address offset: 0x440 + (n × 0x4)

Control access for master connected to AMLI master port EXTPERI[n]

|                  |            |  |                   |  |       |  |                                                |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|-------------------|--|-------|--|------------------------------------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |                   |  |       |  |                                                |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |  |                   |  |       |  |                                                |  |  | A  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |                   |  |       |  |                                                |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID          |  | Value |  | Description                                    |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A-A              | RW         |  | SLAVE[i] (i=0..0) |  |       |  | Control access to slave i of master EXTPERI[n] |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Allowed           |  | 0     |  | Access to slave is allowed                     |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Blocked           |  | 1     |  | Access to slave is blocked                     |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.9.2.3 EXTRAM[n].PROTECT (n=0..0)

Address offset: 0x460 + (n × 0x4)

Control access from master connected to AMLI master port EXTRAM[n]

|                  |      |                   |          |  |       |  |                            |                                               |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------|-------------------|----------|--|-------|--|----------------------------|-----------------------------------------------|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |      |                   |          |  |       |  |                            |                                               |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |      |                   |          |  |       |  |                            |                                               |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | H  | G  | F | E | D | C | B | A |   |   |   |   |   |   |   |
| Reset 0x00000000 |      |                   |          |  |       |  |                            |                                               |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce | Field             | Value ID |  | Value |  | Description                |                                               |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A-H              | RW   | SLAVE[i] (i=0..7) |          |  |       |  |                            | Control access to slave i of master EXTRAM[n] |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |                   | Allowed  |  | 0     |  | Access to slave is allowed |                                               |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |                   | Blocked  |  | 1     |  | Access to slave is blocked |                                               |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.9.2.4 EXTCODE[n].PROTECT (n=0..0)

Address offset: 0x480 + (n × 0x4)

Control access from master connected to AMLI master port EXTCODE[n]

|                  |            |                   |       |                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-------------------|-------|------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                   |       | 31                                             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |                   |       |                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |
| Reset 0x00000000 |            |                   |       | 0                                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID          | Value | Description                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A-A              | RW         | SLAVE[i] (i=0..0) |       | Control access to slave i of master EXTCODE[n] |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Allowed           | 0     | Access to slave is allowed                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Blocked           | 1     | Access to slave is blocked                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

## 7.1.10 DPPI - Distributed programmable peripheral interconnect

The distributed programmable peripheral interconnect (DPPI) enables peripherals to interact autonomously with each other by using tasks and events, without any intervention from the CPU. DPPI allows precise synchronization between peripherals when real-time application constraints exist, and eliminates the need for CPU involvement to implement behavior which can be predefined using the DPPI.

**Note:** Read [Peripheral interface](#) on page 136 to get familiarized with tasks, events, publish/subscribe, interrupts and other concepts.

The DPPI has the following features:

- Peripheral tasks can subscribe to channels
- Peripheral events can be published on channels
- Publish/subscribe pattern enabling multiple connection options that include the following:
  - One-to-one
  - One-to-many
  - Many-to-one
  - Many-to-many

The DPPI consists of several PPIBus modules, which are connected to a fixed number of DPPI channels and a DPPI configuration (DPPIC).



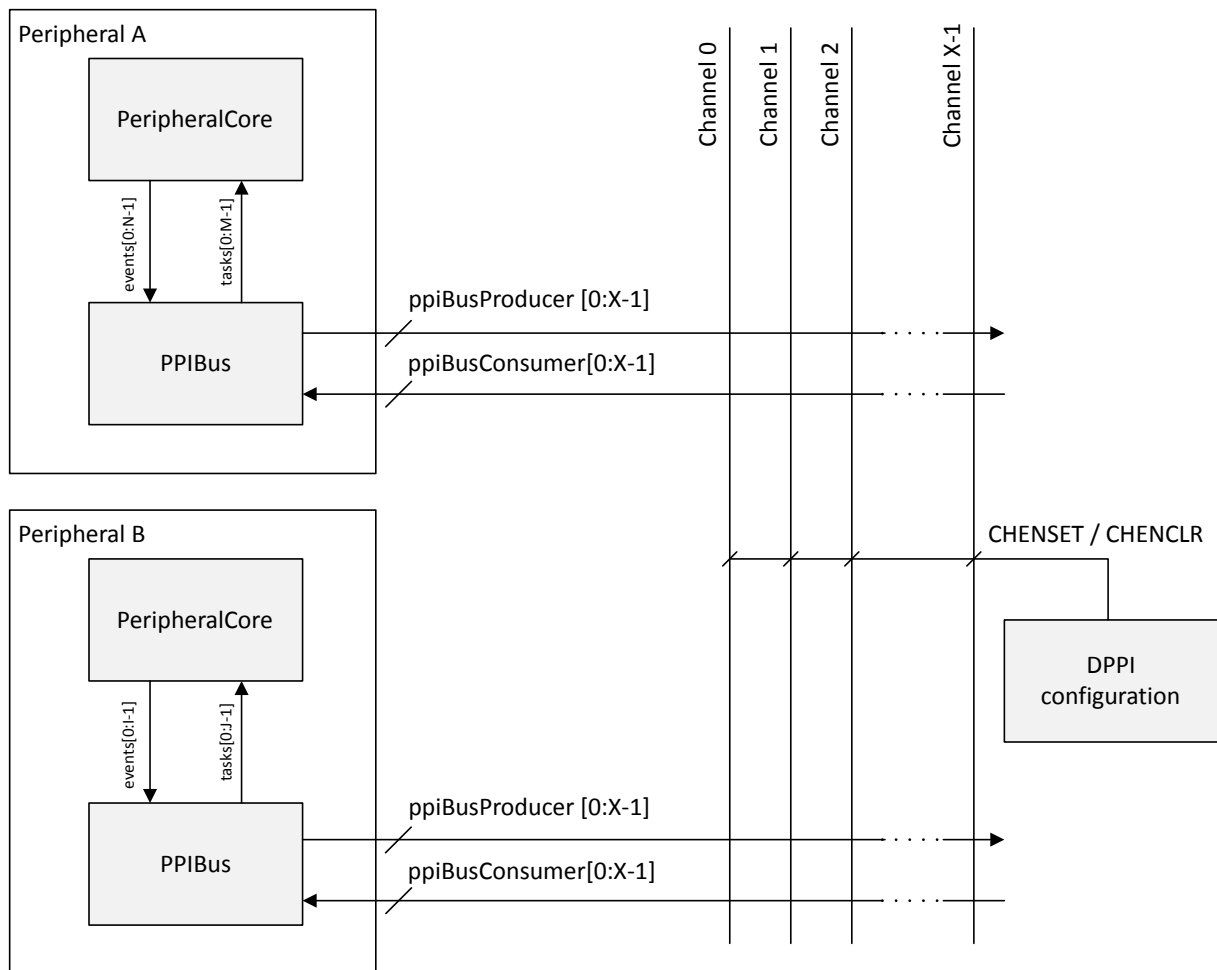


Figure 50: DPPI overview

### 7.1.10.1 Subscribing to and publishing on channels

The PPIBus can route peripheral events onto the channels (publishing), or route events from the channels into peripheral tasks (subscribing).

All peripherals include:

- One subscribe register per task
- One publish register per event

Publish and subscribe registers use a channel index field to determine the channel to which the event is published or tasks subscribed. In addition, there is an enable bit for the subscribe and publish registers that needs to be enabled before the subscription or publishing takes effect.

Writing non-existing channel index (CHIDX) numbers into a peripheral's publish or subscribe registers will yield unexpected results.

One event can trigger multiple tasks by subscribing different tasks to the same channel. Similarly, one task can be triggered by multiple events by publishing different events to the same channel. For advanced use cases, multiple events and multiple tasks can connect to the same channel forming a many-to-many connection. If multiple events are published on the same channel at the same time, the events are merged and only one event is routed through the DPPI.

How peripheral events are routed onto different channels based on publish registers is illustrated in the following figure.

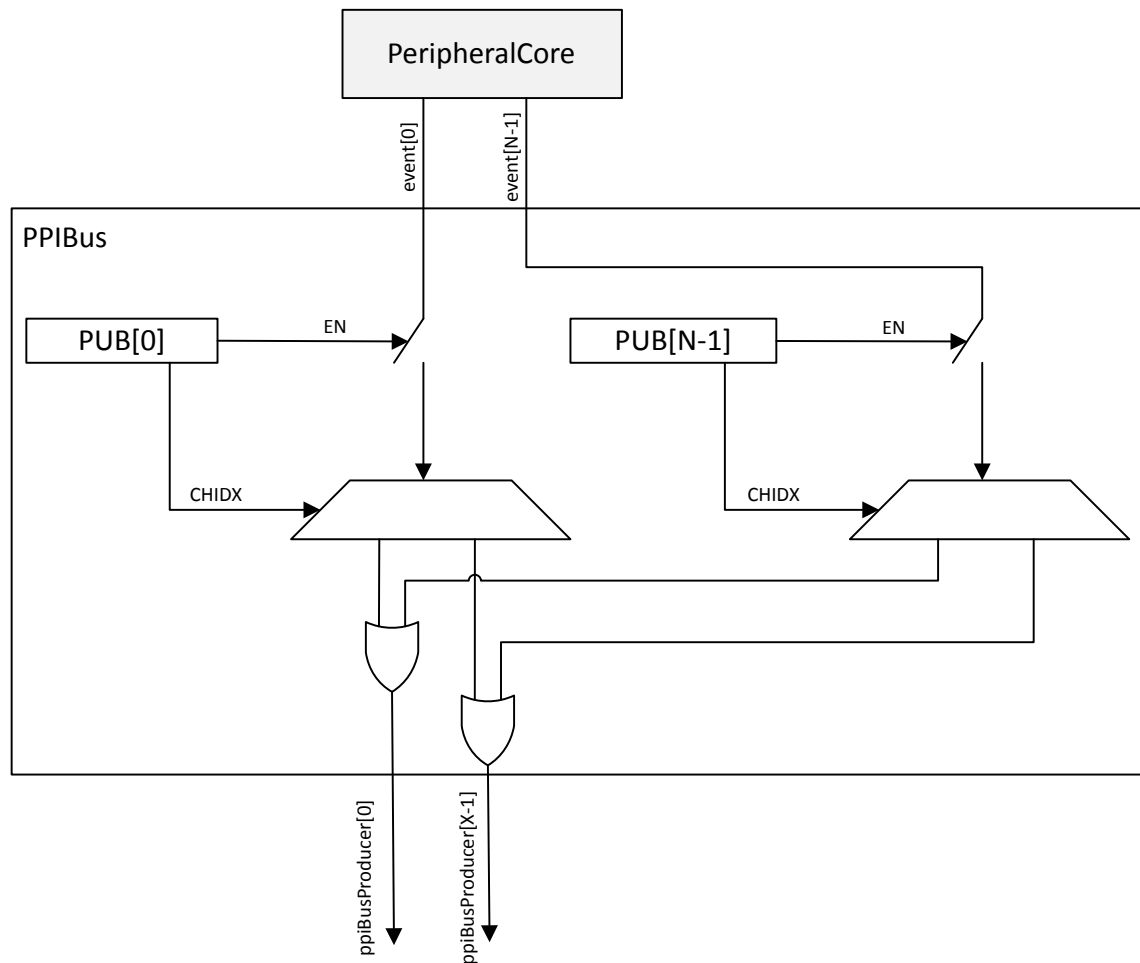


Figure 51: DPPI events flow

How peripheral tasks are triggered from different channels based on subscribe registers is illustrated in the following figure.

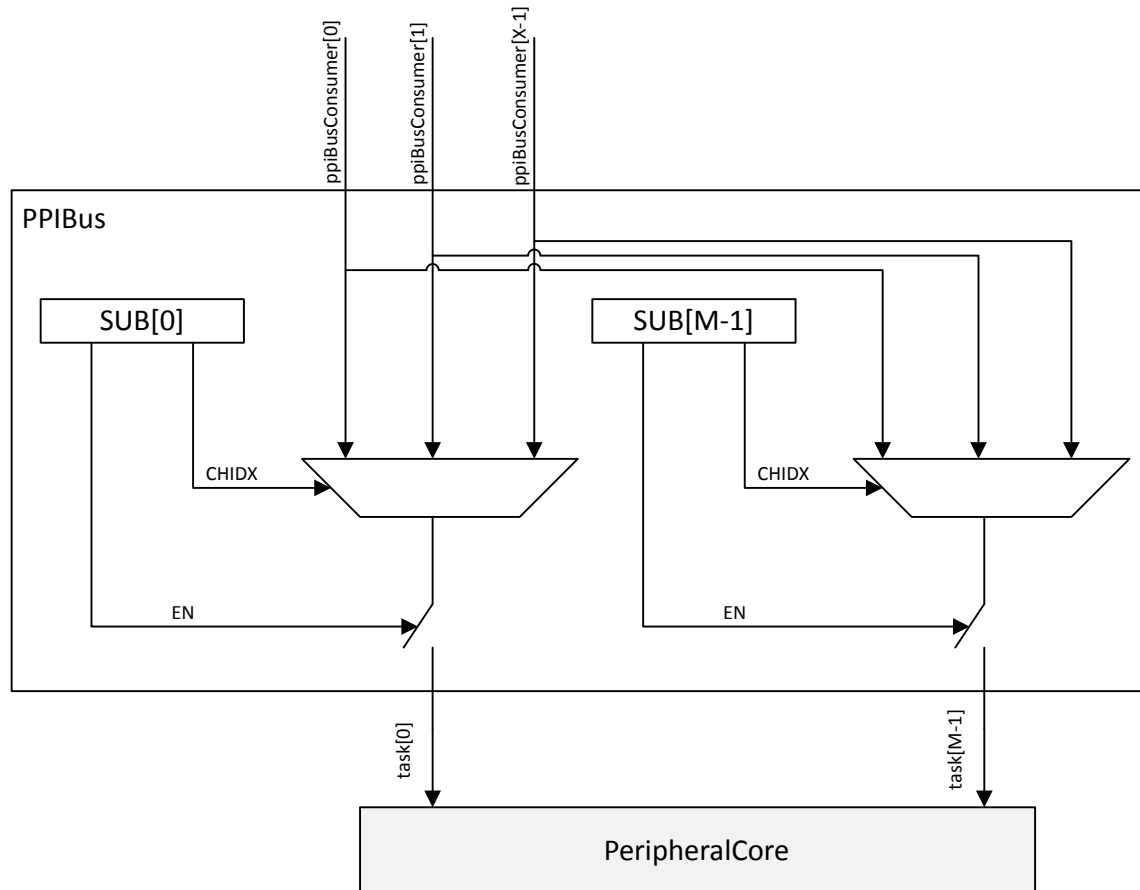


Figure 52: DPPI tasks flow

### 7.1.10.2 DPPI configuration (DPPIC)

Enabling and disabling of channels globally is handled through the DPPI configuration (DPPIC). Connection (connect/disconnect) between a channel and a peripheral is handled locally by the PPIBus.

There are two ways of enabling and disabling global channels using the DPPI configuration:

- Enable or disable channels individually using registers CHEN, CHENSET, and CHENCLR
- Enable or disable channels in channel groups using the groups' tasks ENABLE and DISABLE. It needs to be defined which channels belong to which channel groups before these tasks are triggered.

**Note:** ENABLE tasks are prioritized over DISABLE tasks. When a channel belongs to two or more groups, for example group m and n, and the tasks CHG[m].EN and CHG[n].DIS occur simultaneously (m and n can be equal or different), the CHG[m].EN task on that channel is prioritized.

The DPPI configuration tasks (for example CHG[0].EN) can be triggered through DPPI like any other task, which means they can be linked to a DPPI channel through the subscribe registers.

In order to write to CHG[x], the corresponding CHG[x].EN and CHG[x].DIS subscribe registers must be disabled. Writes to CHG[x] are ignored if any of the two subscribe registers are enabled.

### 7.1.10.3 Connection examples

DPPI offers several connection options. Examples are given for how to create one-to-one and many-to-many connections.

## One-to-one connection

This example shows how to create a one-to-one connection between TIMER compare register and SAADC start task.

The channel configuration is set up first. TIMER0 will publish its COMPARE0 event on channel 0, and SAADC will subscribe its START task to events on the same channel. After that, the channel is enabled through the DPPIC.

```
NRF_TIMER0->PUBLISH_COMPARE0 = (DPPI_PUB_CHIDX_Ch0) |
                                (DPPI_PUB_EN_Msk);
NRF_SAADC->SUBSCRIBE_START    = (DPPI_SUB_CHIDX_Ch0) |
                                (DPPI_SUB_EN_Msk);

NRF_DPPIC->CHENSET = (DPPI_CHENSET_CH0_Set << DPPI_CHENSET_CH0_Pos);
```

## Many-to-many connection

The example shows how to create a many-to-many connection, showcasing the DPPIC's channel group functionality.

A channel group that includes only channel 0 is set up first. Then the GPIOTE and TIMER0 configure their IN0 and COMPARE0 events respectively to be published on channel 0, while the SAADC configures its START task to subscribe to events on channel 0. Through DPPIC, the CHG0 DISABLE task is configured to subscribe to events on channel 0. After an event is received on channel 0 it will be disabled. Finally, channel 0 is enabled using the DPPIC task to enable a channel group.

```
NRF_DPPIC->CHG[0] = (DPPI_CHG_CH0_Included << PPI_CHG_CH0_Pos);

NRF_GPIOTE->PUBLISH_IN0      = (DPPI_PUB_CHIDX_Ch0) |
                                (DPPI_PUB_EN_Msk);
NRF_TIMER0->PUBLISH_COMPARE0 = (DPPI_PUB_CHIDX_Ch0) |
                                (DPPI_PUB_EN_Msk);
NRF_SAADC->SUBSCRIBE_START    = (DPPI_SUB_CHIDX_Ch0) |
                                (DPPI_SUB_EN_Msk);
NRF_DPPIC->SUBSCRIBE_CHG[0].DIS = (DPPI_SUB_CHIDX_Ch0) |
                                (DPPI_SUB_EN_Msk);

NRF_DPPIC->TASK_CHG[0].EN = 1;
```

### 7.1.10.4 Special considerations for a system implementing TrustZone for Cortex-M processors

DPPI is implemented with split security, meaning it handles both secure and non-secure accesses. In a system implementing the TrustZone for Cortex-M technology, DPPI channels can be defined as secure or non-secure using the SPU.

A peripheral configured as non-secure will only be able to subscribe to or publish on non-secure DPPI channels. A peripheral configured as secure will be able to access all DPPI channels. DPPI handles both secure and non-secure accesses, but behaves differently depending on the access type:

- A non-secure peripheral access can only configure and control the DPPI channels defined as non-secure in the SPU.DPPI.PERM[] register(s)

- A secure peripheral access can control all the DPPI channels, independently of the SPU.DPPI.PERM[] register(s)

A group of channels can be created, making it possible to simultaneously enable or disable all channels within the group. The security attribute of a group of channels (secure or non-secure) is defined as follows:

- If all channels (enabled or not) within a group are non-secure, then the group is considered non-secure
- If at least one of the channels (enabled or not) within the group is secure, then the group is considered secure

A non-secure access to a DPPI register, or a bit field, controlling a channel marked as secure in SPU.DPPI[].PERM register(s) will be ignored. Write accesses will have no effect, and read accesses will always return a zero value.

No exceptions are triggered when non-secure accesses target a register or a bit field controlling a secure channel. For example, if the bit  $i$  is set in the SPU.DPPI[0].PERM register (declaring DPPI channel  $i$  as secure), then:

- Non-secure write accesses to registers CHEN, CHENSET, and CHENCLR cannot write bit  $i$  of these registers
- Non-secure write accesses to TASK\_CHG[j].EN and TASK\_CHG[j].DIS registers are ignored if the channel group  $j$  contains at least one channel defined as secure (it can be the channel  $i$  itself or any channel declared as secure)
- Non-secure read accesses to registers CHEN, CHENSET, and CHENCLR always read 0 for the bit at position  $i$

For the channel configuration registers (CHG[]), access from non-secure code is only possible if the included channels are all non-secure, whether the channels are enabled or not. If a CHG[g] register included one or more secure channel(s), then the group  $g$  is considered as secure, and only secure transfers can read to or write from CHG[g]. A non-secure write access is ignored, and a non-secure read access returns 0.

The DPPI can subscribe to secure and non-secure channels through the SUBSCRIBE\_CHG[] registers, in order to trigger the task for enabling or disabling groups of channels. An event from a non-secure channel will be ignored if the group subscribing to this channel is secure. An event from a secure channel can trigger both secure and non-secure tasks.

### 7.1.10.5 Registers

| Base address | Domain      | Peripheral | Instance   | Secure mapping | DMA security | Description     | Configuration                            |
|--------------|-------------|------------|------------|----------------|--------------|-----------------|------------------------------------------|
| 0x50017000   | APPLICATION | DPPIC      | DPPIC : S  | SPLIT          | NA           | DPPI controller | Application core                         |
| 0x40017000   |             |            | DPPIC : NS |                |              |                 | implements 32 DPPI channels              |
| 0x4100F000   | NETWORK     | DPPIC      | DPPIC      | NS             | NA           | DPPI controller | Network core implements 16 DPPI channels |

Table 68: Instances

| Register             | Offset | Security | Description                                                                                                |
|----------------------|--------|----------|------------------------------------------------------------------------------------------------------------|
| TASKS_CHG[n].EN      | 0x000  |          | Enable channel group n                                                                                     |
| TASKS_CHG[n].DIS     | 0x004  |          | Disable channel group n                                                                                    |
| SUBSCRIBE_CHG[n].EN  | 0x080  |          | Subscribe configuration for task CHG[n].EN                                                                 |
| SUBSCRIBE_CHG[n].DIS | 0x084  |          | Subscribe configuration for task CHG[n].DIS                                                                |
| CHEN                 | 0x500  |          | Channel enable register                                                                                    |
| CHENSET              | 0x504  |          | Channel enable set register                                                                                |
| CHENCLR              | 0x508  |          | Channel enable clear register                                                                              |
| CHG[n]               | 0x800  |          | Channel group n                                                                                            |
|                      |        |          | Note: Writes to this register are ignored if either SUBSCRIBE_CHG[n].EN or SUBSCRIBE_CHG[n].DIS is enabled |

Table 69: Register overview

### 7.1.10.5.1 TASKS\_CHG[n].EN (n=0..5)

Address offset: 0x000 + (n × 0x8)

Enable channel group n

|                  |            |    |          |                                                                                       |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
|------------------|------------|----|----------|---------------------------------------------------------------------------------------|------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|
| Bit number       |            |    |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| ID               |            |    |          |                                                                                       |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A |
| Reset 0x00000000 |            |    |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0             |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| ID               | Acce Field |    | Value ID | Value                                                                                 | Description            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| A                | W          | EN |          |                                                                                       | Enable channel group n |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
|                  |            |    | Trigger  | 1                                                                                     | Trigger task           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |

### 7.1.10.5.2 TASKS\_CHG[n].DIS (n=0..5)

Address offset: 0x004 + (n × 0x8)

Disable channel group n

|                  |            |     |          |                                                                                       |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|-----|----------|---------------------------------------------------------------------------------------|-------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |     |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |     |          | A                                                                                     |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |     |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                   |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field |     | Value ID | Value                                                                                 | Description             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W          | DIS |          |                                                                                       | Disable channel group n |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |     | Trigger  | 1                                                                                     | Trigger task            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.10.5.3 SUBSCRIBE\_CHG[n].EN (n=0..5)

Address offset: 0x080 + (n × 0x8)

Subscribe configuration for task CHG[n].EN

|                  |            |          |                                                                                       |                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|---------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |          | B                                                                                     |                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                              | Channel that task <a href="#">CHG[n].EN</a> will subscribe to |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |                                                                                       |                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Disable subscription                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Enable subscription                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

### Subscribe configuration for task CHG[n].DIS

|                  |      |          |          |                                                                         |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |                                                |             |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|----------|----------|-------------------------------------------------------------------------|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|------------------------------------------------|-------------|--|--|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |          |          | 31                                                                      | 30    | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                |             |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |          |          | B                                                                       |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A |   |   |   | A                                              |             |  |  | A |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |          |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |                                                |             |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field    | Value    | ID                                                                      | Value |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |                                                | Description |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW   | CHIDX    | [255..0] |                                                                         |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | Channel that task CHG[n].DIS will subscribe to |             |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW   | EN       |          |                                                                         |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |                                                |             |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Disabled | 0        | Disable subscription                                                    |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |                                                |             |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Enabled  | 1        | Enable subscription                                                     |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |                                                |             |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

## Channel enable register

|                  |      |          |           |    |       |                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------|----------|-----------|----|-------|-----------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |      |          |           | 31 | 30    | 29                          | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |      |          |           | f  | e     | d                           | c  | b  | a  | Z  | Y  | X  | W  | V  | U  | T  | S  | R  | Q  | P  | O  | N  | M  | L  | K  | J | I | H | G | F | E | D | C | B | A |
| Reset 0x00000000 |      |          |           | 0  | 0     | 0                           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce | Field    | Value     | ID | Value | Description                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A-f              | RW   | CH[i]    | (i=0..31) |    |       | Enable or disable channel i |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      | Disabled |           | 0  |       | Disable channel             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      | Enabled  |           | 1  |       | Enable channel              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

Read: Reads value of CH{i} field in CHEN register

|                  |      |                 |       |    |       |                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------|-----------------|-------|----|-------|---------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |      |                 |       | 31 | 30    | 29                                                      | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |      |                 |       | f  | e     | d                                                       | c  | b  | a  | Z  | Y  | X  | W  | V  | U  | T  | S  | R  | Q  | P  | O  | N  | M  | L  | K  | J | I | H | G | F | E | D | C | B | A |
| Reset 0x00000000 |      |                 |       | 0  | 0     | 0                                                       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce | Field           | Value | ID | Value | Description                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A-f              | RW   | CH[i] (i=0..31) |       |    |       | Channel i enable set register. Writing 0 has no effect. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      | Disabled        | 0     |    |       | Read: Channel disabled                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      | Enabled         | 1     |    |       | Read: Channel enabled                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      | Set             | 1     |    |       | Write: Enable channel                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

Read: Reads value of CH{i} field in CHEN register

|                  |            |                 |       |    |                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-----------------|-------|----|-----------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                 | 31    | 30 | 29                                                        | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |                 | f     | e  | d                                                         | c  | b  | a  | Z  | Y  | X  | W  | V  | U  | T  | S  | R  | Q  | P  | O  | N  | M  | L  | K  | J | I | H | G | F | E | D | C | B | A |
| Reset 0x00000000 |            |                 | 0     | 0  | 0                                                         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID        | Value |    | Description                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A-f              | RW         | CH[i] (i=0..31) |       |    | Channel i enable clear register. Writing 0 has no effect. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled        | 0     |    | Read: Channel disabled                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled         | 1     |    | Read: Channel enabled                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Clear           | 1     |    | Write: Disable channel                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 7.1.10.5.8 CHG[n] (n=0..5)

Address offset: 0x800 + (n × 0x4)

Channel group n

Note: Writes to this register are ignored if either SUBSCRIBE\_CHG[n].EN or SUBSCRIBE\_CHG[n].DIS is enabled

|                  |            |                 |       |    |                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-----------------|-------|----|------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                 | 31    | 30 | 29                           | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |                 | f     | e  | d                            | c  | b  | a  | Z  | Y  | X  | W  | V  | U  | T  | S  | R  | Q  | P  | O  | N  | M  | L  | K  | J | I | H | G | F | E | D | C | B | A |
| Reset 0x00000000 |            |                 | 0     | 0  | 0                            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID        | Value |    | Description                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A-f              | RW         | CH[i] (i=0..31) |       |    | Include or exclude channel i |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Excluded        | 0     |    | Exclude                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Included        | 1     |    | Include                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.11 ECB — AES electronic codebook mode encryption

The AES electronic codebook mode encryption (ECB) can be used for a range of cryptographic functions like hash generation, digital signatures, and keystream generation for data encryption/decryption. The ECB encryption block supports 128 bit AES encryption (encryption only, not decryption).

AES ECB operates with EasyDMA access to system Data RAM for in-place operations on cleartext and ciphertext during encryption. ECB uses the same AES core as the CCM and AAR blocks and is an asynchronous operation which may not complete if the AES core is busy.

AES ECB features:

- 128 bit AES encryption
- Supports standard AES ECB block encryption
- Memory pointer support
- DMA data transfer

AES ECB performs a 128 bit AES block encrypt. At the STARTECB task, data and key is loaded into the algorithm by EasyDMA. When output data has been written back to memory, the ENDECB event is triggered.

AES ECB can be stopped by triggering the STOPECB task.

#### 7.1.11.1 Shared resources

The ECB, CCM, and AAR share the same AES module. The ECB will always have lowest priority and if there is a sharing conflict during encryption, the ECB operation will be aborted and an ERRORECB event will be generated.



### 7.1.11.2 EasyDMA

The ECB implements an EasyDMA mechanism for reading and writing to the Data RAM. This DMA cannot access the program memory or any other parts of the memory area except RAM.

If the ECBDATAPTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See [Memory](#) on page 18 for more information about the different memory regions.

The EasyDMA will have finished accessing the Data RAM when the ENDECB or ERRORECB is generated.

### 7.1.11.3 ECB data structure

Input to the block encrypt and output from the block encrypt are stored in the same data structure. ECBDATAPTR should point to this data structure before STARTECB is initiated.

| Property   | Address offset | Description                         |
|------------|----------------|-------------------------------------|
| KEY        | 0              | 16 byte AES key                     |
| CLEARTEXT  | 16             | 16 byte AES cleartext input block   |
| CIPHERTEXT | 32             | 16 byte AES ciphertext output block |

Table 70: ECB data structure overview

### 7.1.11.4 Registers

| Base address | Domain  | Peripheral | Instance | Secure mapping | DMA security | Description             | Configuration |
|--------------|---------|------------|----------|----------------|--------------|-------------------------|---------------|
| 0x4100D000   | NETWORK | ECB        | ECB      | NS             | NA           | AES ECB mode encryption |               |

Table 71: Instances

| Register           | Offset | Security | Description                                                                            |
|--------------------|--------|----------|----------------------------------------------------------------------------------------|
| TASKS_STARTECB     | 0x000  |          | Start ECB block encrypt                                                                |
| TASKS_STOPECB      | 0x004  |          | Abort a possible executing ECB operation                                               |
| SUBSCRIBE_STARTECB | 0x080  |          | Subscribe configuration for task <a href="#">STARTECB</a>                              |
| SUBSCRIBE_STOPECB  | 0x084  |          | Subscribe configuration for task <a href="#">STOPECB</a>                               |
| EVENTS_ENDECB      | 0x100  |          | ECB block encrypt complete                                                             |
| EVENTS_ERRORECB    | 0x104  |          | ECB block encrypt aborted because of a <a href="#">STOPECB</a> task or due to an error |
| PUBLISH_ENDECB     | 0x180  |          | Publish configuration for event <a href="#">ENDECB</a>                                 |
| PUBLISH_ERRORECB   | 0x184  |          | Publish configuration for event <a href="#">ERRORECB</a>                               |
| INTENSET           | 0x304  |          | Enable interrupt                                                                       |
| INTENCLR           | 0x308  |          | Disable interrupt                                                                      |
| ECBDATAPTR         | 0x504  |          | ECB block encrypt memory pointers                                                      |

Table 72: Register overview

#### 7.1.11.4.1 TASKS\_STARTECB

Address offset: 0x000

Start ECB block encrypt

If a crypto operation is already running in the AES core, the STARTECB task will not start a new encryption and an ERRORECB event will be triggered

| Bit number       |      |                |          | 31      | 30 | 29                                                                                                                                                  | 28 | 27           | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |  |
|------------------|------|----------------|----------|---------|----|-----------------------------------------------------------------------------------------------------------------------------------------------------|----|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|--|
| ID               |      |                |          |         |    |                                                                                                                                                     |    |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |  |  |  |
| Reset 0x00000000 |      |                |          | 0       | 0  | 0                                                                                                                                                   | 0  | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |
| ID               | Acce | Field          | Value ID | Value   |    | Description                                                                                                                                         |    |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
| A                | W    | TASKS_STARTECB |          |         |    | Start ECB block encrypt                                                                                                                             |    |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |                |          |         |    | If a crypto operation is already running in the AES core, the STARTECB task will not start a new encryption and an ERRORECB event will be triggered |    |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |                |          | Trigger |    | 1                                                                                                                                                   |    | Trigger task |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |

#### 7.1.11.4.2 TASKS\_STOPECB

Address offset: 0x004

Abort a possible executing ECB operation

If a running ECB operation is aborted by STOPECB, the ERRORECB event is triggered.

|                  |      |               |       |                                                                                       |              |                                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|---------------|-------|---------------------------------------------------------------------------------------|--------------|------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |               |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |              |                                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |               |       | A                                                                                     |              |                                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |               |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |              |                                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field         | Value | ID                                                                                    | Value        | Description                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W    | TASKS_STOPECB |       |                                                                                       |              | Abort a possible executing ECB operation                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               |       |                                                                                       |              | If a running ECB operation is aborted by STOPECB, the ERRORECB event is triggered. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Trigger          |      |               |       | 1                                                                                     | Trigger task |                                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

#### 7.1.11.4.3 SUBSCRIBE\_STARTECB

Address offset: 0x080

Subscribe configuration for task [STARTECB](#)

If a crypto operation is already running in the AES core, the STARTECB task will not start a new encryption and an ERRORECB event will be triggered

|                  |            |  |  |          |  |  |          |  |  |                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|--|----------|--|--|----------|--|--|--------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |  |          |  |  |          |  |  | 31                                                           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |  |  |          |  |  |          |  |  | B                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  |    |    |    |   |   |   |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |  |          |  |  |          |  |  | 0                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  |  | Value ID |  |  | Value    |  |  | Description                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |  |          |  |  | [255..0] |  |  | Channel that task <a href="#">STARTECB</a> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |  |          |  |  |          |  |  |                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  |  | Disabled |  |  | 0        |  |  | Disable subscription                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  |  | Enabled  |  |  | 1        |  |  | Enable subscription                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.11.4.4 SUBSCRIBE\_STOPECB

Address offset: 0x084

Subscribe configuration for task [STOPECB](#)

If a running ECB operation is aborted by STOPECB, the ERRORECB event is triggered.

|                  |            |          |                                                                                       |                      |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|----------------------|----------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                      |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |          | B                                                                                     |                      |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |                      |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 |                      | Description                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                              |                      | Channel that task <b>STOPECB</b> will subscribe to |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |                                                                                       |                      |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Disable subscription |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Enable subscription  |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

#### 7.1.11.4.5 EVENTS\_ENDECB

Address offset: 0x100

ECB block encrypt complete

|                  |                  |              |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------------|--------------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |                  |              |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |                  |              |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |                  |              |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field       | Value ID     | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW EVENTS_ENDECB |              |       | ECB block encrypt complete                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                  | NotGenerated | 0     | Event not generated                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                  | Generated    | 1     | Event generated                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

#### 7.1.11.4.6 EVENTS\_ERRORECB

Address offset: 0x104

ECB block encrypt aborted because of a STOPECB task or due to an error

|                  |            |                 |                                                                                       |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|-----------------|---------------------------------------------------------------------------------------|------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |                 | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |                 | A                                                                                     |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |                 | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID        | Value                                                                                 | Description                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | EVENTS_ERRORECB |                                                                                       | ECB block encrypt aborted because of a STOPECB task or due to an error |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | NotGenerated    | 0                                                                                     | Event not generated                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Generated       | 1                                                                                     | Event generated                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

#### 7.1.11.4.7 PUBLISH\_ENDECB

Address offset: 0x180

Publish configuration for event **ENDECB**

|                  |            |          |                                                                                       |                    |                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|--------------------|---------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                    |                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |          | B                                                                                     |                    |                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                    |                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 |                    | Description                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                              |                    | Channel that event <b>ENDECB</b> will publish to. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |                                                                                       |                    |                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Disable publishing |                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Enable publishing  |                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |



### 7.1.11.4.11 ECBDATAPTR

Address offset: 0x504

ECB block encrypt memory pointers

|                  |      |            |       |    |       |                                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------|------------|-------|----|-------|-----------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |      |            |       | 31 | 30    | 29                                                                          | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |      |            |       | A  | A     | A                                                                           | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |      |            |       | 0  | 0     | 0                                                                           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce | Field      | Value | ID | Value | Description                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW   | ECBDATAPTR |       |    |       | Pointer to the ECB data structure (see Table 1 ECB data structure overview) |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

## 7.1.11.5 Electrical specification

### 7.1.11.5.1 ECB Electrical Specification

| Symbol           | Description                             | Min. | Typ. | Max. | Units |
|------------------|-----------------------------------------|------|------|------|-------|
| t <sub>ECB</sub> | Run time per 16 byte block in all modes | ..   | ..   | ..   | µs    |

## 7.1.12 EGU — Event generator unit

Event generator unit (EGU) provides support for interlayer signaling. This means providing support for atomic triggering of both CPU execution and hardware tasks, from both firmware (by CPU) and hardware (by PPI). This feature can, for instance, be used for triggering CPU execution at a lower priority execution from a higher priority execution, or to handle a peripheral's interrupt service routine (ISR) execution at a lower priority for some of its events. However, triggering any priority from any priority is possible.

Listed here are the main EGU features:

- Software-enabled interrupt triggering
- Separate interrupt vectors for every EGU instance
- Up to 16 separate event flags per interrupt for multiplexing

Each instance of EGU implements a set of tasks which can individually be triggered to generate the corresponding event, for example, the corresponding event for TASKS\_TRIGGER[n] is EVENTS\_TRIGGERED[n]. See [Table 73: Instances](#) on page 202 for a list of EGU instances.

### 7.1.12.1 Registers

| Base address | Domain      | Peripheral | Instance  | Secure mapping | DMA security | Description            | Configuration |
|--------------|-------------|------------|-----------|----------------|--------------|------------------------|---------------|
| 0x5001B000   | APPLICATION | EGU        | EGU0 : S  | US             | NA           | Event generator unit 0 |               |
| 0x4001B000   |             |            | EGU0 : NS |                |              |                        |               |
| 0x5001C000   | APPLICATION | EGU        | EGU1 : S  | US             | NA           | Event generator unit 1 |               |
| 0x4001C000   |             |            | EGU1 : NS |                |              |                        |               |
| 0x5001D000   | APPLICATION | EGU        | EGU2 : S  | US             | NA           | Event generator unit 2 |               |
| 0x4001D000   |             |            | EGU2 : NS |                |              |                        |               |
| 0x5001E000   | APPLICATION | EGU        | EGU3 : S  | US             | NA           | Event generator unit 3 |               |
| 0x4001E000   |             |            | EGU3 : NS |                |              |                        |               |
| 0x5001F000   | APPLICATION | EGU        | EGU4 : S  | US             | NA           | Event generator unit 4 |               |
| 0x4001F000   |             |            | EGU4 : NS |                |              |                        |               |
| 0x50020000   | APPLICATION | EGU        | EGU5 : S  | US             | NA           | Event generator unit 5 |               |
| 0x40020000   |             |            | EGU5 : NS |                |              |                        |               |
| 0x41014000   | NETWORK     | EGU        | EGU0      | NS             | NA           | Event generator unit 0 |               |

Table 73: Instances

| Register             | Offset | Security | Description                                                              |
|----------------------|--------|----------|--------------------------------------------------------------------------|
| TASKS_TRIGGER[n]     | 0x000  |          | Trigger n for triggering the corresponding TRIGGERED[n] event            |
| SUBSCRIBE_TRIGGER[n] | 0x080  |          | Subscribe configuration for task TRIGGER[n]                              |
| EVENTS_TRIGGERED[n]  | 0x100  |          | Event number n generated by triggering the corresponding TRIGGER[n] task |
| PUBLISH_TRIGGERED[n] | 0x180  |          | Publish configuration for event TRIGGERED[n]                             |
| INTEN                | 0x300  |          | Enable or disable interrupt                                              |
| INTENSET             | 0x304  |          | Enable interrupt                                                         |
| INTENCLR             | 0x308  |          | Disable interrupt                                                        |

Table 74: Register overview

#### 7.1.12.1.1 TASKS\_TRIGGER[n] (n=0..15)

Address offset: 0x000 + (n × 0x4)

Trigger n for triggering the corresponding TRIGGERED[n] event

| Bit number       |      | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                               |
|------------------|------|---------------------------------------------------------------------------------------|---------------------------------------------------------------|
| ID               |      | A                                                                                     |                                                               |
| Reset 0x00000000 |      | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                               |
| ID               | Acce | Field                                                                                 | Description                                                   |
| A                | W    | TASKS_TRIGGER                                                                         | Trigger n for triggering the corresponding TRIGGERED[n] event |
|                  |      | Trigger                                                                               | 1<br>Trigger task                                             |

#### 7.1.12.1.2 SUBSCRIBE\_TRIGGER[n] (n=0..15)

Address offset: 0x080 + (n × 0x4)

Subscribe configuration for task TRIGGER[n]

|                  |            |  |          |  |          |  |  |  |                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|--|----------|--|--|--|-------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          |  |          |  |  |  |                                                       | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |
| ID               |            |  |          |  |          |  |  |  |                                                       | B  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  |    |    |    |   |   |   |   |   |   | A | A | A | A | A | A | A |   |
| Reset 0x00000000 |            |  |          |  |          |  |  |  |                                                       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID |  | Value    |  |  |  | Description                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          |  | [255..0] |  |  |  | Channel that task <b>TRIGGER[n]</b> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |  |          |  |  |  |                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled |  | 0        |  |  |  | Disable subscription                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  |  | 1        |  |  |  | Enable subscription                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.12.1.3 EVENTS\_TRIGGERED[n] (n=0..15)

Address offset:  $0x100 + (n \times 0x4)$

Event number n generated by triggering the corresponding **TRIGGER[n]** task

|                  |            |  |                  |  |              |   |                                                                          |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|------------------|--|--------------|---|--------------------------------------------------------------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |                  |  |              |   |                                                                          |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |  |                  |  |              |   |                                                                          |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |   |
| Reset 0x00000000 |            |  |                  |  |              |   |                                                                          |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID         |  | Value        |   | Description                                                              |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         |  | EVENTS_TRIGGERED |  |              |   | Event number n generated by triggering the corresponding TRIGGER[n] task |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  |                  |  | NotGenerated | 0 | Event not generated                                                      |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  |                  |  | Generated    | 1 | Event generated                                                          |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.12.1.4 PUBLISH\_TRIGGERED[n] (n=0..15)

Address offset:  $0x180 + (n \times 0x4)$

Publish configuration for event **TRIGGERED[n]**

|                  |            |          |          |                                                                         |    |                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
|------------------|------------|----------|----------|-------------------------------------------------------------------------|----|---------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|-----------------|---|---|---|---|---|---|---|--|--|--|--|
| Bit number       |            |          |          | 31                                                                      | 30 | 29                                                      | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |
| ID               |            |          |          | B                                                                       |    |                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A A A A A A A A |   |   |   |   |   |   |   |  |  |  |  |
| Reset 0x00000000 |            |          |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |    |                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
| ID               | Acce Field |          | Value ID | Value                                                                   |    | Description                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
| A                | RW CHIDX   |          |          | [255..0]                                                                |    | Channel that event <b>TRIGGERED[n]</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
| B                | RW EN      |          |          |                                                                         |    |                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | Disabled |          | 0                                                                       |    | Disable publishing                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | Enabled  |          | 1                                                                       |    | Enable publishing                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |

#### 7.1.12.1.5 INTEN

Address offset: 0x300

Enable or disable interrupt

|                  |            |                        |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|------------------------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |                        |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |                        |       | P O N M L K J I H G F E D C B A                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |                        |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID               | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A-P              | RW         | TRIGGERED[i] (i=0..15) |       | Enable or disable interrupt for event <span>TRIGGERED[i]</span>                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled               | 0     | Disable                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled                | 1     | Enable                                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.12.1.6 INTENSET

Address offset: 0x304

Enable interrupt

|                  |      |                        |          |       |                                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|------------------|------|------------------------|----------|-------|----------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|
| Bit number       |      |                        |          | 31    | 30                                                                   | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |
| ID               |      |                        |          |       |                                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    | P  | O  | N  | M  | L  | K  | J | I | H | G | F | E | D | C | B | A |  |  |  |
| Reset 0x00000000 |      |                        |          | 0     | 0                                                                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |
| ID               | Acce | Field                  | Value ID | Value | Description                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
| A-P              | RW   | TRIGGERED[i] (i=0..15) |          |       | Write '1' to enable interrupt for event <a href="#">TRIGGERED[i]</a> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |                        | Set      | 1     | Enable                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |                        | Disabled | 0     | Read: Disabled                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |                        | Enabled  | 1     | Read: Enabled                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |

### 7.1.12.1.7 INTENCLR

Address offset: 0x308

Disable interrupt

|                  |      |                        |          |    |                |                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------|------------------------|----------|----|----------------|-------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |      |                        |          | 31 | 30             | 29                                                    | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |      |                        |          |    |                |                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    | P  | O  | N  | M  | L  | K  | J | I | H | G | F | E | D | C | B | A |
| Reset 0x00000000 |      |                        |          | 0  | 0              | 0                                                     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce | Field                  | Value    | ID | Value          | Description                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A-P              | RW   | TRIGGERED[i] (i=0..15) |          |    |                | Write '1' to disable interrupt for event TRIGGERED[i] |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |                        | Clear    | 1  | Disable        |                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |                        | Disabled | 0  | Read: Disabled |                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |                        | Enabled  | 1  | Read: Enabled  |                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

## 7.1.12.2 Electrical specification

### 7.1.12.2.1 EGU Electrical Specification

| Symbol               | Description                                                                   | Min. | Typ. | Max. | Units  |
|----------------------|-------------------------------------------------------------------------------|------|------|------|--------|
| t <sub>EGU,EVT</sub> | Latency between setting an EGU event flag and the system setting an interrupt | ..   | ..   | ..   | cycles |

## 7.1.13 FPU - Floating point unit (FPU) exceptions

The ARM Cortex-M33 has FPU signals that indicate mathematical errors that cause floating-point exceptions.

The FPU signals are routed to the following event registers:

- FPUIOC: INVALIDOPERATION
- FPUIDC: DENORMALINPUT
- FPUOFC: OVERFLOW
- FPUUFC: UNDERFLOW
- FPUDZC: DIVIDEBYZERO
- FPUIXC: INEXACT



To clear the FPU exception source, write a 0 to the ARM Cortex-M33 FPSCR (floating-point status control register), as described in the *ARM Cortex-M33 Devices Generic User Guide*.

### 7.1.13.1 Registers

| Base address | Domain      | Peripheral | Instance | Secure mapping | DMA security | Description         | Configuration |
|--------------|-------------|------------|----------|----------------|--------------|---------------------|---------------|
| 0x50000000   | APPLICATION | FPU        | FPU : S  | US             | NA           | Floating Point unit |               |
| 0x40000000   |             |            | FPU : NS |                |              | interrupt control   |               |

Table 75: Instances

| Register                | Offset | Security | Description                                                                                        |
|-------------------------|--------|----------|----------------------------------------------------------------------------------------------------|
| EVENTS_INVALIDOPERATION | 0x100  |          | An FPUIOC exception triggered by an invalid operation has occurred in the FPU                      |
| EVENTS_DIVIDEBYZERO     | 0x104  |          | An FPUDZC exception triggered by a floating-point divide-by-zero operation has occurred in the FPU |
| EVENTS_OVERFLOW         | 0x108  |          | An FPUOFC exception triggered by a floating-point overflow has occurred in the FPU                 |
| EVENTS_UNDERFLOW        | 0x10C  |          | An FPUUFC exception triggered by a floating-point underflow has occurred in the FPU                |
| EVENTS_INEXACT          | 0x110  |          | An FPUIXC exception triggered by an inexact floating-point operation has occurred in the FPU       |
| EVENTS_DENORMALINPUT    | 0x114  |          | An FPUIDC exception triggered by a denormal floating-point input has occurred in the FPU           |
| INTEN                   | 0x300  |          | Enable or disable interrupt                                                                        |
| INTENSET                | 0x304  |          | Enable interrupt                                                                                   |
| INTENCLR                | 0x308  |          | Disable interrupt                                                                                  |

Table 76: Register overview

#### 7.1.13.1.1 EVENTS\_INVALIDOPERATION

Address offset: 0x100

An FPUIOC exception triggered by an invalid operation has occurred in the FPU

|                  |      |                         |              |                                                                                       |                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|-------------------------|--------------|---------------------------------------------------------------------------------------|-------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |                         |              | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |                         |              | A                                                                                     |                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |                         |              | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field                   | Value ID     | Value                                                                                 | Description                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW   | EVENTS_INVALIDOPERATION |              |                                                                                       | An FPUIOC exception triggered by an invalid operation has occurred in the FPU |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                         | NotGenerated | 0                                                                                     | Event not generated                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                         | Generated    | 1                                                                                     | Event generated                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

#### 7.1.13.1.2 EVENTS\_DIVIDEBYZERO

Address offset: 0x104

An FPUDZC exception triggered by a floating-point divide-by-zero operation has occurred in the FPU

| Bit number       |      |                     |              | 31    | 30                                                                                                 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |   |
|------------------|------|---------------------|--------------|-------|----------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|---|
| ID               |      |                     |              |       |                                                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | A |
| Reset 0x00000000 |      |                     |              | 0     | 0                                                                                                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |   |
| ID               | Acce | Field               | Value ID     | Value | Description                                                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
| A                | RW   | EVENTS_DIVIDEBYZERO |              |       | An FPUDZC exception triggered by a floating-point divide-by-zero operation has occurred in the FPU |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |      |                     | NotGenerated | 0     | Event not generated                                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |      |                     | Generated    | 1     | Event generated                                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |

### 7.1.13.1.3 EVENTS\_OVERFLOW

Address offset: 0x108

An FPU OFC exception triggered by a floating-point overflow has occurred in the FPU

|                  |            |                 |       |                                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|------------------|------------|-----------------|-------|------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|---|
| Bit number       |            |                 |       | 31                                                                                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |   |
| ID               |            |                 |       |                                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  | A |
| Reset 0x00000000 |            |                 |       | 0                                                                                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |   |
| ID               | Acce Field | Value ID        | Value | Description                                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
| A                | RW         | EVENTS_OVERFLOW |       | An FPUOFC exception triggered by a floating-point overflow has occurred in the FPU |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|                  |            | NotGenerated    | 0     | Event not generated                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|                  |            | Generated       | 1     | Event generated                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |

### 7.1.13.1.4 EVENTS\_UNDERFLOW

Address offset: 0x10C

An FPU UFC exception triggered by a floating-point underflow has occurred in the FPU

|                  |      |                  |              |    |                     |                                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|------------------|------|------------------|--------------|----|---------------------|-------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|--|
| Bit number       |      |                  |              | 31 | 30                  | 29                                                                                  | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |  |
| ID               |      |                  |              | A  |                     |                                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
| Reset 0x00000000 |      |                  |              | 0  | 0                   | 0                                                                                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |
| ID               | Acce | Field            | Value        | ID | Value               | Description                                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
| A                | RW   | EVENTS_UNDERFLOW |              |    |                     | An FPUUFC exception triggered by a floating-point underflow has occurred in the FPU |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |                  | NotGenerated | 0  | Event not generated |                                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |                  | Generated    | 1  | Event generated     |                                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |

### 7.1.13.1.5 EVENTS\_INEXACT

Address offset: 0x110

An FPU IXC exception triggered by an inexact floating-point operation has occurred in the FPU

|                  |            |                |       |                                                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|------------------|------------|----------------|-------|----------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|
| Bit number       |            |                |       | 31                                                                                           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |
| ID               |            |                |       | A                                                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
| Reset 0x00000000 |            |                |       | 0                                                                                            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |
| ID               | Acce Field | Value ID       | Value | Description                                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
| A                | RW         | EVENTS_INEXACT |       | An FPUIXC exception triggered by an inexact floating-point operation has occurred in the FPU |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            | NotGenerated   | 0     | Event not generated                                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            | Generated      | 1     | Event generated                                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |

### 7.1.13.1.6 EVENTS\_DENORMALINPUT

Address offset: 0x114

An FPUIDC exception triggered by a denormal floating-point input has occurred in the FPU

|                  |            |                      |       |                                                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|------------------|------------|----------------------|-------|------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|---|
| Bit number       |            |                      | 31    | 30                                                                                       | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |   |
| ID               |            |                      |       |                                                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  | A |
| Reset 0x00000000 |            |                      | 0     | 0                                                                                        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |   |
| ID               | Acce Field | Value ID             | Value | Description                                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
| A                | RW         | EVENTS_DENORMALINPUT |       | An FPUIDC exception triggered by a denormal floating-point input has occurred in the FPU |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|                  |            | NotGenerated         | 0     | Event not generated                                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|                  |            | Generated            | 1     | Event generated                                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |

### 7.1.13.1.7 INTEN

Address offset: 0x300

Enable or disable interrupt

|                  |      |                  |          |                                                                                       |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|------------------|----------|---------------------------------------------------------------------------------------|------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |                  |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |                  |          | F E D C B A                                                                           |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |                  |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field            | Value ID | Value                                                                                 | Description                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW   | INVALIDOPERATION |          |                                                                                       | Enable or disable interrupt for event <a href="#">INVALIDOPERATION</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                  | Disabled | 0                                                                                     | Disable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                  | Enabled  | 1                                                                                     | Enable                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW   | DIVIDEBYZERO     |          |                                                                                       | Enable or disable interrupt for event <a href="#">DIVIDEBYZERO</a>     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                  | Disabled | 0                                                                                     | Disable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                  | Enabled  | 1                                                                                     | Enable                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW   | OVERFLOW         |          |                                                                                       | Enable or disable interrupt for event <a href="#">OVERFLOW</a>         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                  | Disabled | 0                                                                                     | Disable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                  | Enabled  | 1                                                                                     | Enable                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| D                | RW   | UNDERFLOW        |          |                                                                                       | Enable or disable interrupt for event <a href="#">UNDERFLOW</a>        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                  | Disabled | 0                                                                                     | Disable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                  | Enabled  | 1                                                                                     | Enable                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| E                | RW   | INEXACT          |          |                                                                                       | Enable or disable interrupt for event <a href="#">INEXACT</a>          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                  | Disabled | 0                                                                                     | Disable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                  | Enabled  | 1                                                                                     | Enable                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| F                | RW   | DENORMALINPUT    |          |                                                                                       | Enable or disable interrupt for event <a href="#">DENORMALINPUT</a>    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                  | Disabled | 0                                                                                     | Disable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                  | Enabled  | 1                                                                                     | Enable                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.13.1.8 INTENSET

Address offset: 0x304

Enable interrupt

|                  |            |  |                  |  |       |  |                                                                          |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|------------------|--|-------|--|--------------------------------------------------------------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |                  |  |       |  |                                                                          |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |  |                  |  |       |  |                                                                          |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | F  | E  | D | C | B | A |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |                  |  |       |  |                                                                          |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID         |  | Value |  | Description                                                              |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         |  | INVALIDOPERATION |  |       |  | Write '1' to enable interrupt for event <a href="#">INVALIDOPERATION</a> |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

| Bit number       |                  |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------------|----------|---------------------------------------------------------------------------------------|-----------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |                  |          | F E D C B A                                                                           |                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |                  |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field       | Value ID | Value                                                                                 | Description                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                  | Set      | 1                                                                                     | Enable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                  | Disabled | 0                                                                                     | Read: Disabled                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                  | Enabled  | 1                                                                                     | Read: Enabled                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                  |          |                                                                                       |                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW DIVIDEBYZERO  |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">DIVIDEBYZERO</a>  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                  | Set      | 1                                                                                     | Enable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                  | Disabled | 0                                                                                     | Read: Disabled                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                  | Enabled  | 1                                                                                     | Read: Enabled                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                  |          |                                                                                       |                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW OVERFLOW      |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">OVERFLOW</a>      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                  | Set      | 1                                                                                     | Enable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                  | Disabled | 0                                                                                     | Read: Disabled                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                  | Enabled  | 1                                                                                     | Read: Enabled                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                  |          |                                                                                       |                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| D                | RW UNDERFLOW     |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">UNDERFLOW</a>     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                  | Set      | 1                                                                                     | Enable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                  | Disabled | 0                                                                                     | Read: Disabled                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                  | Enabled  | 1                                                                                     | Read: Enabled                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                  |          |                                                                                       |                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| E                | RW INEXACT       |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">INEXACT</a>       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                  | Set      | 1                                                                                     | Enable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                  | Disabled | 0                                                                                     | Read: Disabled                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                  | Enabled  | 1                                                                                     | Read: Enabled                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                  |          |                                                                                       |                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| F                | RW DENORMALINPUT |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">DENORMALINPUT</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                  | Set      | 1                                                                                     | Enable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                  | Disabled | 0                                                                                     | Read: Disabled                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                  | Enabled  | 1                                                                                     | Read: Enabled                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                  |          |                                                                                       |                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.13.1.9 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number       |      |                  | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                |       |                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|------------------|---------------------------------------------------------------------------------------|----------------|-------|---------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |      |                  | F E D C B A                                                                           |                |       |                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |                  | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                |       |                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field            | Value                                                                                 | ID             | Value | Description                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW   | INVALIDOPERATION |                                                                                       |                |       | Write '1' to disable interrupt for event <a href="#">INVALIDOPERATION</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Clear            | 1                                                                                     | Disable        |       |                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Disabled         | 0                                                                                     | Read: Disabled |       |                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Enabled          | 1                                                                                     | Read: Enabled  |       |                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW   | DIVIDEBYZERO     |                                                                                       |                |       | Write '1' to disable interrupt for event <a href="#">DIVIDEBYZERO</a>     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Clear            | 1                                                                                     | Disable        |       |                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Disabled         | 0                                                                                     | Read: Disabled |       |                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Enabled          | 1                                                                                     | Read: Enabled  |       |                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW   | OVERFLOW         |                                                                                       |                |       | Write '1' to disable interrupt for event <a href="#">OVERFLOW</a>         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Clear            | 1                                                                                     | Disable        |       |                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Disabled         | 0                                                                                     | Read: Disabled |       |                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Enabled          | 1                                                                                     | Read: Enabled  |       |                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| D                | RW   | UNDERFLOW        |                                                                                       |                |       | Write '1' to disable interrupt for event <a href="#">UNDERFLOW</a>        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Clear            | 1                                                                                     | Disable        |       |                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Disabled         | 0                                                                                     | Read: Disabled |       |                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Enabled          | 1                                                                                     | Read: Enabled  |       |                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

| Bit number       |      |               |          | 31          | 30             | 29                                                                     | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |
|------------------|------|---------------|----------|-------------|----------------|------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|
| ID               |      |               |          | F E D C B A |                |                                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
| Reset 0x00000000 |      |               |          | 0           | 0              | 0                                                                      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |
| ID               | Acce | Field         | Value    | ID          | Value          | Description                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
| E                | RW   | INEXACT       |          |             |                | Write '1' to disable interrupt for event <a href="#">INEXACT</a>       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |               | Clear    | 1           | Disable        |                                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |               | Disabled | 0           | Read: Disabled |                                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |               | Enabled  | 1           | Read: Enabled  |                                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
| F                | RW   | DENORMALINPUT |          |             |                | Write '1' to disable interrupt for event <a href="#">DENORMALINPUT</a> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |               | Clear    | 1           | Disable        |                                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |               | Disabled | 0           | Read: Disabled |                                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |               | Enabled  | 1           | Read: Enabled  |                                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |

## 7.1.14 GPIO — General purpose input/output

The general purpose input/output pins (GPIOs) are grouped as one or more ports with each port having up to 32 GPIOs.

The number of ports and GPIOs per port may vary with product variant and package. Refer to [Registers](#) on page 215 and [Pin assignments](#) on page 764 for more information about the number of GPIOs that are supported.

GPIO has the following user-configurable features:

- Up to 32 GPIO pins per GPIO port
- Configurable output drive strength
- Internal pull-up and pull-down resistors
- Wake-up from high or low level triggers on all pins
- Trigger interrupt on state changes on any pin
- All pins can be used by the PPI task/event system
- One or more GPIO outputs can be controlled through PPI and GPIOTE channels
- All pins can be individually mapped to interface blocks for layout flexibility
- GPIO state changes captured on SENSE signal can be stored by LATCH register
- Pin sharing in multi-MCU system
- Support for secure and non-secure attributes for pins in conjunction with the system protection unit ([SPU — System protection unit](#) on page 568)

[Figure 53: GPIO port and the GPIO pin details](#) on page 210 illustrates the GPIO port containing 32 individual pins, where `PIN0` is illustrated in more detail as a reference. All signals on the left side in the illustration are used by other peripherals in the system and therefore not directly available to the CPU.

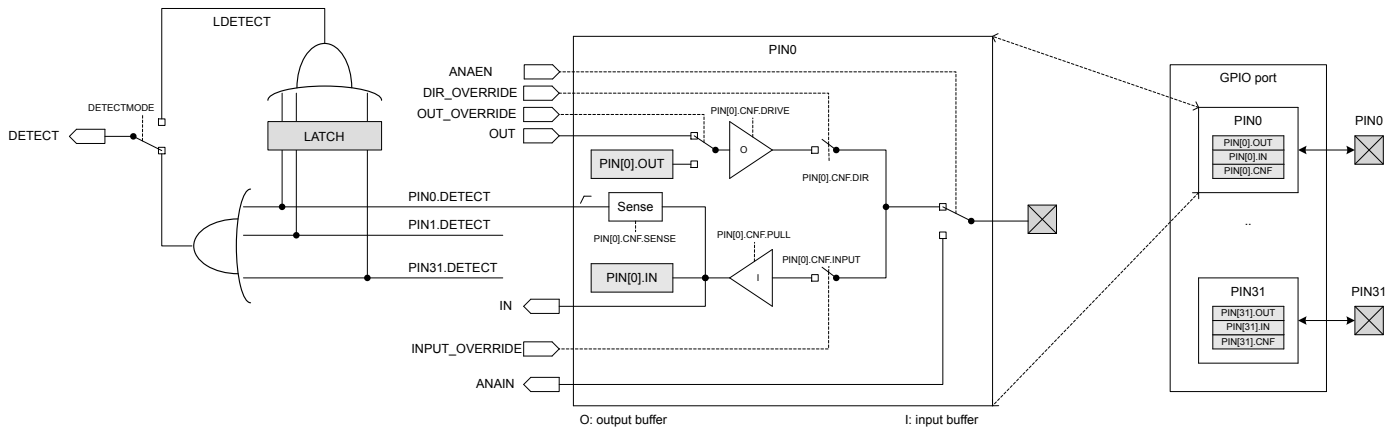


Figure 53: GPIO port and the GPIO pin details

#### 7.1.14.1 Assigning pins to MCUs and Subsystems

In a system implementing multiple MCUs, some pins of the system can be allocated among other MCUs and Subsystems than the Application MCU.

The pins accessible by each MCU are listed in [Table 77: Instances](#) on page 215.

Pins can be assigned to the following MCUs and Subsystems:

- Application MCU
- Network MCU
- Peripheral with dedicated pins
- Trace and Debug Subsystem

**Note:** Unless specified otherwise, the term Subsystem is used as a generic term for referring to a MCU, Peripheral or Subsystem.

The GPIO peripheral instantiated in the Application MCU will control which pin(s) another Subsystem can access. By default, all pins are assigned to the Application MCU. Pins can be assigned to a different Subsystem than the Application MCU by using the MCUSEL bitfield in the `PIN_CNF[]` register as shown in [Figure 54: Pin allocation in multiple-MCU systems](#) on page 211. If a pin is allocated to a Subsystem that can not access it, the pin stays under control of the Application MCU GPIO peripheral.

When a pin  $p$  is assigned to another Subsystem,

- for the GPIO peripheral instantiated in the Application MCU:
  - all write operations to bitfields or registers related to this pin will be ignored, except for the LATCH register and the `PIN_CNF[p].MCUSEL`, `PIN_CNF[p].SENSE` bitfields.
  - read operation will return 0 for the bitfields or the registers associated to this pin, except for LATCH, `PIN_CNF[p].MCUSEL` and `PIN_CNF[p].SENSE` bitfields.
- if the Subsystem is another MCU, for the GPIO peripherals instantiated in this MCU:
  - write operations will update the internal registers of the GPIO peripheral independently of the content of the `PIN_CNF[p].MCUSEL` bitfield of the Application MCU's GPIO peripheral.
  - the pin state will only be affected if this pin has been assigned to this MCU. Pins not assigned to this MCU will be read as zero in this MCU.
- if the Subsystem is a Peripheral with dedicated pins or the Trace and Debug Subsystem, for the pins assigned to this Subsystem:
  - the pin state will only be affected if this pin has been assigned to this Subsystem

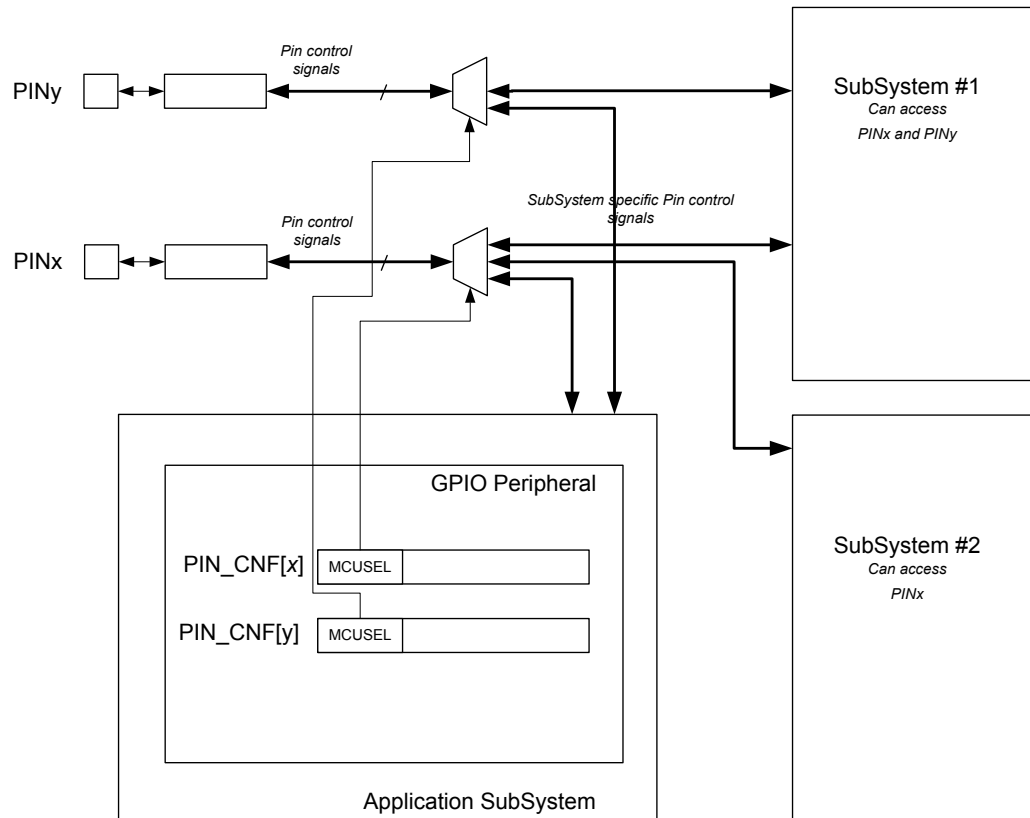


Figure 54: Pin allocation in multiple-MCU systems

As explained before, only the Application MCU can assign pins. GPIO peripherals instantiated in other MCUs than the Application MCU don't have the `PIN_CNF[]`.MCUSEL bitfield.

Changing the MCUSEL bitfield for a pin may induce glitches, therefore it is recommended that peripherals using this pin are disabled before updating MCUSEL.

#### 7.1.14.2 Pin configuration

The GPIO port peripheral implements up to 32 pins, `PIN0` through `PIN31`. Each of these pins can be individually configured in the `PIN_CNF[n]` registers ( $n=0..31$ ).

**Note:** Refer to [Assigning pins to MCUs and Subsystems](#) on page 210 for pin assignment and corresponding effect of read and write operations of GPIO registers

The following parameters can be configured through these registers:

- Direction
- Drive strength
- Enabling of pull-up and pull-down resistors
- Pin sensing
- Input buffer disconnect
- Analog input (for selected pins)

**Note:** All write-capable registers are retained registers. See [POWER — Power control](#) on page 36 chapter for more information about retained registers.

The input buffer of a GPIO pin can be disconnected from the pin to enable power savings when the pin is not used as an input, see [Figure 53: GPIO port and the GPIO pin details](#) on page 210. Inputs must be

connected to get a valid input value in the [IN](#) register, and for the sense mechanism to get access to the pin.

Other peripherals in the system can connect to GPIO pins and override their output value and configuration, or read their analog or digital input value. See [Figure 53: GPIO port and the GPIO pin details](#) on page 210.

Selected pins also support analog input signals, see ANAIN in [Figure 53: GPIO port and the GPIO pin details](#) on page 210. The assignment of the analog pins can be found in [Pin assignments](#) on page 764.

The following delays should be taken into considerations:

- There is 2 CPU clock cycles delay from the GPIO pad to the [IN](#) register
- The GPIO pad must be low (or high depending on the SENSE polarity) for 3 CPU clock cycles after DETECT has gone high in order to generate a new DETECT signal

**Note:** When a pin is configured as digital input, care has been taken to minimize increased current consumption when the input voltage is between  $V_{IL}$  and  $V_{IH}$ . However, it is a good practice to ensure that the external circuitry does not drive that pin to levels between  $V_{IL}$  and  $V_{IH}$  for a long period of time.

### 7.1.14.3 Pin sense mechanism

Pins sensitivity can be individually configured, through the SENSE field in the PIN\_CNF[n] register, to detect either a high level or a low level on their input.

**Note:** Refer to [Assigning pins to MCUs and Subsystems](#) on page 210 for pin assignment and corresponding effect of read and write operations of GPIO registers

When the correct level is detected on any such configured pin, the sense mechanism will set the DETECT signal high. Each pin has a separate DETECT signal. Default behavior, defined by the DETECTMODE register, is that the DETECT signals from all pins in the GPIO port are combined into one common DETECT signal that is routed throughout the system, which then can be utilized by other peripherals. This mechanism is functional in both System ON and System OFF modes.

DETECTMODE and DETECTMODE\_SEC are provided to handle secure and non-secure pins. DETECTMODE\_SEC register is available to control the behavior associated to pin marked as secure, while the DETECTMODE register is restricted to pin marked as non-secure. Please refer to [GPIO security](#) on page 213 for more details.

Make sure that a pin is in a level that cannot trigger the sense mechanism before enabling it. The DETECT signal will go high immediately if the SENSE condition configured in the PIN\_CNF registers is met when the sense mechanism is enabled. This will trigger a PORT event if the DETECT signal was low before enabling the sense mechanism.

The DETECT signal is also used by power and clock management system to exit from System OFF mode, and by GPIOTE to generate the PORT event. In addition GPIOTE\_SEC is used for PORT event related to secure pins). See [POWER — Power control](#) on page 36 and [GPIOTE — GPIO tasks and events](#) on page 220 for more information about how the DETECT signal is used.

When a pin's PINx.DETECT signal goes high, a flag will be set in the [LATCH](#) register. For example, when the PIN0.DETECT signal goes high, bit 0 in the [LATCH](#) register will be set to '1'. If the CPU performs a clear operation on a bit in the [LATCH](#) register when the associated PINx.DETECT signal is high, the bit in the [LATCH](#) register will not be cleared. The [LATCH](#) register will only be cleared if the CPU explicitly clears it by writing a '1' to the bit that shall be cleared, i.e. the [LATCH](#) register will not be affected by a PINx.DETECT signal being set low.

The LDETECT signal will be set high when one or more bits in the [LATCH](#) register are '1'. The LDETECT signal will be set low when all bits in the [LATCH](#) register are successfully cleared to '0'.



If one or more bits in the **LATCH** register are '1' after the CPU has performed a clear operation on the **LATCH** registers, a rising edge will be generated on the LDETECT signal. This is illustrated in [Figure 55: DETECT signal behavior](#) on page 213.

**Note:** The CPU can read the **LATCH** register at any time to check if a SENSE condition has been met on one or more of the the GPIO pins, even if that condition is no longer met at the time the CPU queries the **LATCH** register. This mechanism will work even if the LDETECT signal is not used as the DETECT signal.

The LDETECT signal is by default not connected to the GPIO port's DETECT signal, but via the DETECTMODE register it is possible to change from default behavior to DETECT signal being derived directly from the LDETECT signal instead. See [Figure 53: GPIO port and the GPIO pin details](#) on page 210. [Figure 55: DETECT signal behavior](#) on page 213 illustrates the DETECT signal behavior for these two alternatives.

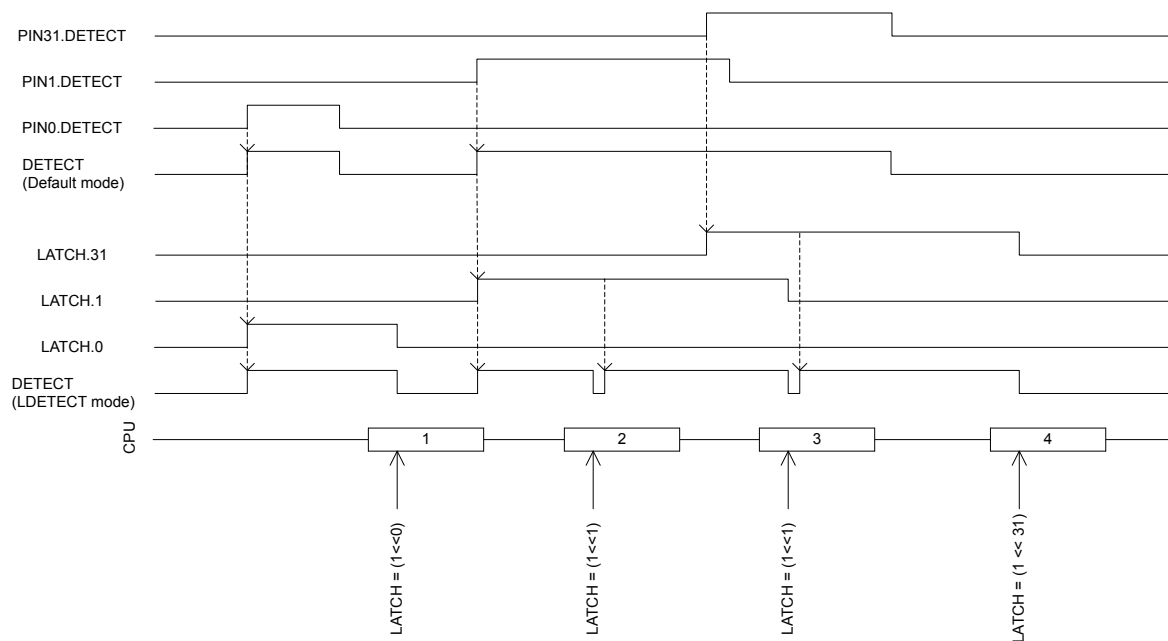


Figure 55: DETECT signal behavior

#### 7.1.14.4 GPIO security

The general purpose input/output peripheral (GPIO) is implemented as a "split-security" peripheral. If marked as non-secure, it can be access by both secure and non-secure accesses but will behave differently depending of the access type.

**Note:** Refer to [Assigning pins to MCUs and Subsystems](#) on page 210 for pin assignment and corresponding effect of read and write operations of GPIO registers

A non-secure peripheral access will only be able to configure and control pins defined as non-secure in the system protection unit (SPU) GPIOPORT.PERM[] register(s).

A non-secure access to a register or a bitfield controlling a pin marked as secure in GPIO.PERM[] register(s) will be ignored:

- write accesses will have no effect
- read accesses will always return a zero value

No exception is triggered when a non-secure access targets a register or bitfield controlling a secure pin.

For example, if the bit  $i$  is set in the SPU.GPIO.PERM[0] register (declaring Pin P0. $i$  as secure), then

- non-secure write accesses to OUT, OUTSET, OUTCLR, DIR, DIRSET, DIRCLR and LATCH registers will not be able to write to bit  $i$  of those registers
- non-secure write accesses to registers PIN[ $i$ ].OUT and PIN\_CNF[ $i$ ] will be ignored
- non-secure read accesses to registers OUT, OUTSET, OUTCLR, IN, DIR, DIRSET, DIRCLR and LATCH will always read a 0 for the bit at position  $i$
- non-secure read accesses to registers PIN[ $i$ ].OUT, PIN[ $i$ ].IN and PIN\_CNF[ $i$ ] will always return 0

The GPIO.DETECTMODE and GPIO.DETECTMODE\_SEC registers are handled differently than the other registers mentioned before. When accessed by a secure access, the DETECTMODE\_SEC register controls the source for the DETECT\_SEC signal for the pins marked as secure. When accessed by a non-secure access, the DETECTMODE\_SEC is read as zero and write accesses are ignored. The GPIO.DETECTMODE register controls the source for the DETECT\_NSEC signal for the pins defined as non-secure.

The DETECT\_NSEC signal is routed to the GPIOTE peripheral, allowing generation of events and interrupts from pins marked as non-secure. The DETECT\_SEC signal is routed to the GPIOTESEC peripheral, allowing generation of events and interrupts from pins marked as secure. [Figure 56: Principle of direct pin access](#) on page 214 illustrates how the DETECT\_NSEC and DETECT\_SEC signals are generated from the GPIO PIN[ $i$ ].DETECT signals.

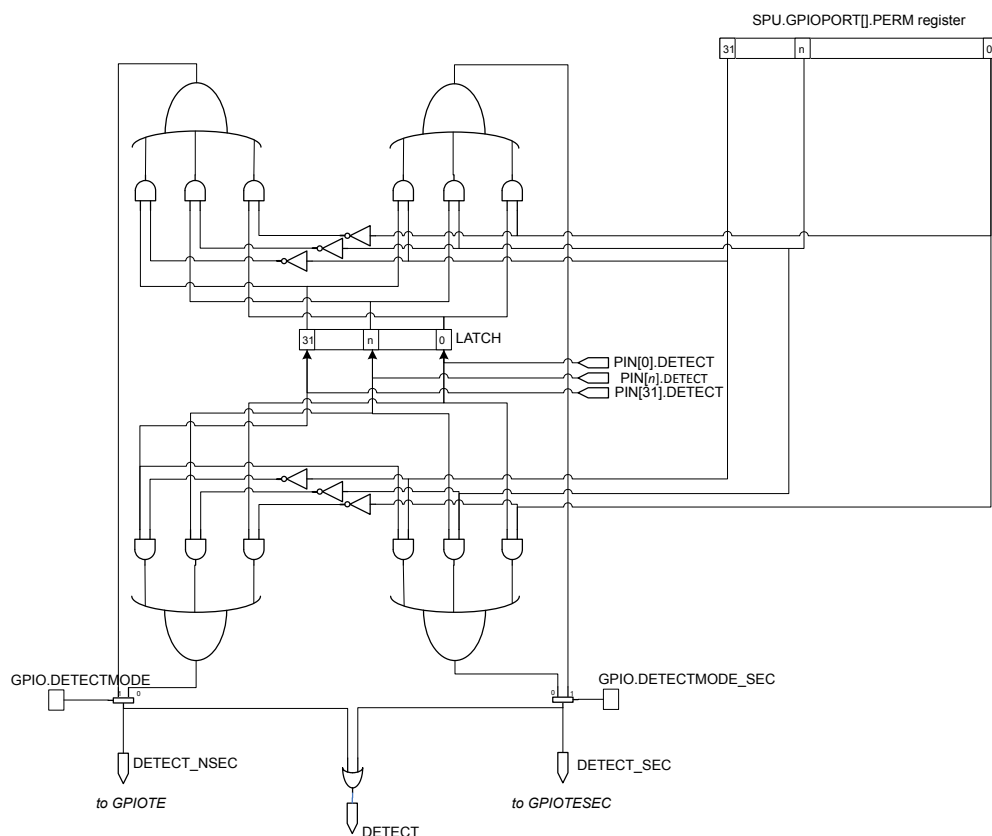


Figure 56: Principle of direct pin access

### 7.1.14.5 Registers

| Base address | Domain      | Peripheral | Instance | Secure mapping | DMA security | Description                              | Configuration              |
|--------------|-------------|------------|----------|----------------|--------------|------------------------------------------|----------------------------|
| 0x50842500   | APPLICATION | GPIO       | P0 : S   | SPLIT          | NA           | General purpose input and output, port 0 | P0.00 to P0.31 implemented |
| 0x40842500   |             |            | P0 : NS  |                |              |                                          |                            |
| 0x50842800   | APPLICATION | GPIO       | P1 : S   | SPLIT          | NA           | General purpose input and output, port 1 | P1.00 to P1.16 implemented |
| 0x40842800   |             |            | P1 : NS  |                |              |                                          |                            |
| 0x418C0500   | NETWORK     | GPIO       | P0       | NS             | NA           | General purpose input and output         | P0.00 to P0.31 implemented |
| 0x418C0800   | NETWORK     | GPIO       | P1       | NS             | NA           | General purpose input and output         | P1.00 to P1.16 implemented |

Table 77: Instances

| Register       | Offset | Security | Description                                                                                               |          |
|----------------|--------|----------|-----------------------------------------------------------------------------------------------------------|----------|
| OUT            | 0x004  |          | Write GPIO port                                                                                           | Retained |
| OUTSET         | 0x008  |          | Set individual bits in GPIO port                                                                          |          |
| OUTCLR         | 0x00C  |          | Clear individual bits in GPIO port                                                                        |          |
| IN             | 0x010  |          | Read GPIO port                                                                                            |          |
| DIR            | 0x014  |          | Direction of GPIO pins                                                                                    | Retained |
| DIRSET         | 0x018  |          | DIR set register                                                                                          |          |
| DIRCLR         | 0x01C  |          | DIR clear register                                                                                        |          |
| LATCH          | 0x020  |          | Latch register indicating what GPIO pins that have met the criteria set in the PIN_CNF[n].SENSE registers | Retained |
| DETECTMODE     | 0x024  |          | Select between default DETECT signal behavior and LDETECT mode (For non-secure pin only)                  | Retained |
| DETECTMODE_SEC | 0x028  |          | Select between default DETECT signal behavior and LDETECT mode (For secure pin only)                      | Retained |
| PIN_CNF[n]     | 0x200  |          | Configuration of GPIO pins                                                                                | Retained |

Table 78: Register overview

#### 7.1.14.5.1 OUT ( Retained )

Address offset: 0x004

This register is a retained register

Write GPIO port

|                  |            |                  |                                                                                       |                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|------------------|---------------------------------------------------------------------------------------|--------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |                  | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |                  | f e d c b a Z Y X W V U T S R Q P O N M L K J I H G F E D C B A                       |                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |                  | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID         | Value                                                                                 | Description        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A-f              | RW         | PIN[i] (i=0..31) |                                                                                       | Pin i              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Low              | 0                                                                                     | Pin driver is low  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | High             | 1                                                                                     | Pin driver is high |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

#### 7.1.14.5.2 OUTSET

Address offset: 0x008

Set individual bits in GPIO port

Read: reads value of OUT register.

|                  |            |                  |       |    |                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|------------------|-------|----|---------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                  | 31    | 30 | 29                                                                  | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |                  | f     | e  | d                                                                   | c  | b  | a  | Z  | Y  | X  | W  | V  | U  | T  | S  | R  | Q  | P  | O  | N  | M  | L  | K  | J | I | H | G | F | E | D | C | B | A |
| Reset 0x00000000 |            |                  | 0     | 0  | 0                                                                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID         | Value |    | Description                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A-f              | RW         | PIN[i] (i=0..31) |       |    | Pin i                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Low              | 0     |    | Read: pin driver is low                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | High             | 1     |    | Read: pin driver is high                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Set              | 1     |    | Write: writing a '1' sets the pin high; writing a '0' has no effect |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.14.5.3 OUTCLR

Address offset: 0x00C

Clear individual bits in GPIO port

Read: reads value of OUT register.

|                  |            |                  |          |       |  |                                                                    |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|------------------|----------|-------|--|--------------------------------------------------------------------|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                  |          |       |  |                                                                    |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |                  |          |       |  |                                                                    |  | f  | e  | d  | c  | b  | a  | Z  | Y  | X  | W  | V  | U  | T  | S  | R  | Q  | P  | O  | N  | M  | L  | K  | J | I | H | G | F | E | D | C | B | A |   |
| Reset 0x00000000 |            |                  |          |       |  |                                                                    |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |                  | Value ID | Value |  | Description                                                        |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A-f              | RW         | PIN[i] (i=0..31) |          |       |  | Pin i                                                              |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Low              |          | 0     |  | Read: pin driver is low                                            |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | High             |          | 1     |  | Read: pin driver is high                                           |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Clear            |          | 1     |  | Write: writing a '1' sets the pin low; writing a '0' has no effect |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.14.5.4 IN

Address offset: 0x010

Read GPIO port

|                  |            |                  |          |   |       |  |             |                   |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|------------------|----------|---|-------|--|-------------|-------------------|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                  |          |   |       |  |             |                   |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |                  |          |   |       |  |             |                   |  | f  | e  | d  | c  | b  | a  | Z  | Y  | X  | W  | V  | U  | T  | S  | R  | Q  | P  | O  | N  | M  | L  | K  | J | I | H | G | F | E | D | C | B | A |   |   |   |
| Reset 0x00000000 |            |                  |          |   |       |  |             |                   |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |                  | Value ID |   | Value |  | Description |                   |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A-f              | R          | PIN[i] (i=0..31) |          |   |       |  |             | Pin i             |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |                  | Low      | 0 |       |  |             | Pin input is low  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |                  | High     | 1 |       |  |             | Pin input is high |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.14.5.5 DIR ( Retained )

Address offset: 0x014

This register is a retained register

Direction of GPIO pins

|                  |            |                  |          |        |       |   |             |                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|------------------|----------|--------|-------|---|-------------|-------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                  |          |        |       |   |             | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |                  |          |        |       |   |             | f                 | e  | d  | c  | b  | a  | Z  | Y  | X  | W  | V  | U  | T  | S  | R  | Q  | P  | O  | N  | M  | L  | K  | J | I | H | G | F | E | D | C | B | A |   |
| Reset 0x00000000 |            |                  |          |        |       |   |             | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |                  | Value ID |        | Value |   | Description |                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A-f              | RW         | PIN[i] (i=0..31) |          |        |       |   |             |                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |                  |          | Input  |       | 0 |             | Pin set as input  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |                  |          | Output |       | 1 |             | Pin set as output |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.14.5.6 DIRSET

Address offset: 0x018

DIR set register

Read: reads value of DIR register.

|                  |            |                  |          |       |  |                                                                      |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|------------------|----------|-------|--|----------------------------------------------------------------------|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                  |          |       |  |                                                                      |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |                  |          |       |  |                                                                      |  | f  | e  | d  | c  | b  | a  | Z  | Y  | X  | W  | V  | U  | T  | S  | R  | Q  | P  | O  | N  | M  | L  | K  | J | I | H | G | F | E | D | C | B | A |   |
| Reset 0x00000000 |            |                  |          |       |  |                                                                      |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |                  | Value ID | Value |  | Description                                                          |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A-f              | RW         | PIN[i] (i=0..31) |          |       |  | Set as output pin i                                                  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Input            |          | 0     |  | Read: pin set as input                                               |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Output           |          | 1     |  | Read: pin set as output                                              |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Set              |          | 1     |  | Write: writing a '1' sets pin to output; writing a '0' has no effect |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.14.5.7 DIRCLR

Address offset: 0x01C

DIR clear register

Read: reads value of DIR register.

|                  |            |                  |          |       |  |                                                                     |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|------------------|----------|-------|--|---------------------------------------------------------------------|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                  |          |       |  |                                                                     |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |                  |          |       |  |                                                                     |  | f  | e  | d  | c  | b  | a  | Z  | Y  | X  | W  | V  | U  | T  | S  | R  | Q  | P  | O  | N  | M  | L  | K  | J | I | H | G | F | E | D | C | B | A |   |
| Reset 0x00000000 |            |                  |          |       |  |                                                                     |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |                  | Value ID | Value |  | Description                                                         |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A-f              | RW         | PIN[i] (i=0..31) |          |       |  | Set as input pin i                                                  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |                  | Input    | 0     |  | Read: pin set as input                                              |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |                  | Output   | 1     |  | Read: pin set as output                                             |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |                  | Clear    | 1     |  | Write: writing a '1' sets pin to input; writing a '0' has no effect |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.14.5.8 LATCH ( Retained )

Address offset: 0x020

This register is a retained register

Latch register indicating what GPIO pins that have met the criteria set in the PIN\_CNF[n].SENSE registers

|                  |      |                  |            |       |                                                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|------------------|------|------------------|------------|-------|---------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|
| Bit number       |      |                  |            | 31    | 30                                                                                          | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |
| ID               |      |                  |            | f     | e                                                                                           | d  | c  | b  | a  | Z  | Y  | X  | W  | V  | U  | T  | S  | R  | Q  | P  | O  | N  | M  | L  | K  | J | I | H | G | F | E | D | C | B | A |  |  |  |
| Reset 0x00000000 |      |                  |            | 0     | 0                                                                                           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |
| ID               | Acce | Field            | Value ID   | Value | Description                                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
| A-f              | RW   | PIN[i] (i=0..31) |            |       | Status on whether PINi has met criteria set in PIN_CNFi.SENSE register. Write '1' to clear. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |                  | NotLatched | 0     | Criteria has not been met                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |                  | Latched    | 1     | Criteria has been met                                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |

#### 7.1.14.5.9 DETECTMODE ( Retained )

Address offset: 0x024

This register is a retained register

Select between default DETECT signal behavior and LDETECT mode (For non-secure pin only)

|                  |      |            |          |                                                                         |                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|------------------|------|------------|----------|-------------------------------------------------------------------------|----------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|--|
| Bit number       |      |            |          | 31                                                                      | 30                                                             | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |
| ID               |      |            |          | A                                                                       |                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| Reset 0x00000000 |      |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| ID               | Acce | Field      | Value ID | Value                                                                   | Description                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| A                | RW   | DETECTMODE |          |                                                                         | Select between default DETECT signal behavior and LDETECT mode |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |      |            | Default  | 0                                                                       | DETECT directly connected to PIN DETECT signals                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |      |            | LDETECT  | 1                                                                       | Use the latched LDETECT behavior                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |

#### 7.1.14.5.10 DETECTMODE\_SEC ( Retained )

Address offset: 0x028

This register is a retained register

Select between default DETECT signal behavior and LDETECT mode (For secure pin only)

|                  |      |            |          |                                                                         |    |                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|------------------|------|------------|----------|-------------------------------------------------------------------------|----|----------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|--|
| Bit number       |      |            |          | 31                                                                      | 30 | 29                                                             | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |
| ID               |      |            |          | A                                                                       |    |                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| Reset 0x00000000 |      |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |    |                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| ID               | Acce | Field      | Value ID | Value                                                                   |    | Description                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| A                | RW   | DETECTMODE |          |                                                                         |    | Select between default DETECT signal behavior and LDETECT mode |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |      |            | Default  | 0                                                                       |    | DETECT directly connected to PIN DETECT signals                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |      |            | LDETECT  | 1                                                                       |    | Use the latched LDETECT behavior                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |

#### 7.1.14.5.11 PIN\_CNFi[n] (n=0..31) ( Retained )

Address offset: 0x200 + (n × 0x4)

This register is a retained register

Configuration of GPIO pins

| Bit number       |            |     |          |  |       |  |  |  |  | 31                                                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |  |   |   |   |   |
|------------------|------------|-----|----------|--|-------|--|--|--|--|-------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|---|---|---|---|
| ID               |            |     |          |  |       |  |  |  |  | G                                                     | G  | G  |    |    |    |    |    |    |    |    |    |    | E  | E  |    |    |    |    |    |    |    |   |   |   | D | D | D | D |   |   |   |   |   |   |   |   |   |  | C | C | B | A |
| Reset 0x00000002 |            |     |          |  |       |  |  |  |  | 0                                                     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |  |   |   |   |   |
| ID               | Acce Field |     | Value ID |  | Value |  |  |  |  | Description                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |
| A                | RW         | DIR |          |  |       |  |  |  |  | Pin direction. Same physical register as DIR register |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |

| Bit number       |            |            | 31    | 30 | 29                                                                             | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |  |
|------------------|------------|------------|-------|----|--------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|--|
| ID               |            |            | G     |    |                                                                                | G  | G  |    |    |    |    |    |    |    |    |    |    |    | E  |    | E  | D  |    |    |   | D | D | D | C |   |   |   | C | B | A |  |  |  |
| Reset 0x00000002 |            |            | 0     | 0  | 0                                                                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |  |  |  |
| ID               | Acce Field | Value ID   | Value |    | Description                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
| B                | RW INPUT   | Input      | 0     |    | Configure pin as an input pin                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            | Output     | 1     |    | Configure pin as an output pin                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            | Connect    | 0     |    | Connect input buffer                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            | Disconnect | 1     |    | Disconnect input buffer                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
| C                | RW PULL    |            |       |    | Pull configuration                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            | Disabled   | 0     |    | No pull                                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            | Pulldown   | 1     |    | Pull down on pin                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            | Pullup     | 3     |    | Pull up on pin                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
| D                | RW DRIVE   |            |       |    | Drive configuration                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            | S0S1       | 0     |    | Standard '0', standard '1'                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            | H0S1       | 1     |    | High drive '0', standard '1'                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            | S0H1       | 2     |    | Standard '0', high drive '1'                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            | H0H1       | 3     |    | High drive '0', high 'drive '1''                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            | D0S1       | 4     |    | Disconnect '0', standard '1' (normally used for wired-or connections)          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            | D0H1       | 5     |    | Disconnect '0', high drive '1' (normally used for wired-or connections)        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            | S0D1       | 6     |    | Standard '0', disconnect '1' (normally used for wired-and connections)         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            | H0D1       | 7     |    | High drive '0', disconnect '1' (normally used for wired-and connections)       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            | E0S1       | 9     |    | Extra high drive '0', standard '1'                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            | S0E1       | 10    |    | Standard '0', extra high drive '1'                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            | E0E1       | 11    |    | Extra high drive '0', extra high drive '1'                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            | D0E1       | 13    |    | Disconnect '0', extra high drive '1' (normally used for wired-or connections)  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            | E0D1       | 15    |    | Extra high drive '0', disconnect '1' (normally used for wired-and connections) |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
| E                | RW SENSE   |            |       |    | Pin sensing mechanism                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            | Disabled   | 0     |    | Disabled                                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            | High       | 2     |    | Sense for high level                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            | Low        | 3     |    | Sense for low level                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
| G                | RW MCUSEL  |            |       |    | Select which MCU/Subsystem controls this pin                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            |            |       |    | Note: this field is only accessible from secure code.                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            | AppMCU     | 0x0   |    | Application MCU                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            | NetworkMCU | 0x1   |    | Network MCU                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            | Peripheral | 0x3   |    | Peripheral with dedicated pins                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            | TND        | 0x7   |    | Trace and Debug Subsystem                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |

#### 7.1.14.6 Electrical specification

#### 7.1.14.6.1 GPIO Electrical Specification

| Symbol              | Description                                           | Min. | Typ. | Max. | Units |
|---------------------|-------------------------------------------------------|------|------|------|-------|
| V <sub>IH</sub>     | Input high voltage                                    | ..   | ..   | ..   | V     |
| V <sub>IL</sub>     | Input low voltage                                     | ..   | ..   | ..   | V     |
| V <sub>OH,SD</sub>  | Output high voltage, standard drive, 0.5 mA, VDD ≥1.7 | ..   | ..   | ..   | V     |
| V <sub>OH,HDH</sub> | Output high voltage, high drive, 5 mA, VDD ≥= 2.7 V   | ..   | ..   | ..   | V     |

| Symbol                | Description                                                          | Min. | Typ. | Max. | Units |
|-----------------------|----------------------------------------------------------------------|------|------|------|-------|
| V <sub>OH,HDL</sub>   | Output high voltage, high drive, 3 mA, VDD ≥ 1.7 V                   | ..   | ..   | ..   | V     |
| V <sub>OL,SD</sub>    | Output low voltage, standard drive, 0.5 mA, VDD ≥ 1.7                | ..   | ..   | ..   | V     |
| V <sub>OL,HDH</sub>   | Output low voltage, high drive, 5 mA, VDD ≥ 2.7 V                    | ..   | ..   | ..   | V     |
| V <sub>OL,HDL</sub>   | Output low voltage, high drive, 3 mA, VDD ≥ 1.7 V                    | ..   | ..   | ..   | V     |
| I <sub>OL,SD</sub>    | Current at VSS+0.4 V, output set low, standard drive, VDD ≥ 1.7      | ..   | ..   | ..   | mA    |
| I <sub>OL,HDH</sub>   | Current at VSS+0.4 V, output set low, high drive, VDD ≥ 2.7 V        | ..   | ..   | ..   | mA    |
| I <sub>OL,HDL</sub>   | Current at VSS+0.4 V, output set low, high drive, VDD ≥ 1.7 V        | ..   | ..   | ..   | mA    |
| I <sub>OH,SD</sub>    | Current at VDD-0.4 V, output set high, standard drive, VDD ≥ 1.7     | ..   | ..   | ..   | mA    |
| I <sub>OH,HDH</sub>   | Current at VDD-0.4 V, output set high, high drive, VDD ≥ 2.7 V       | ..   | ..   | ..   | mA    |
| I <sub>OH,HDL</sub>   | Current at VDD-0.4 V, output set high, high drive, VDD ≥ 1.7 V       | ..   | ..   | ..   | mA    |
| t <sub>RF,15pF</sub>  | Rise/fall time, standard drive mode, 10-90%, 15 pF load <sup>1</sup> | ..   | ..   | ..   | ns    |
| t <sub>RF,25pF</sub>  | Rise/fall time, standard drive mode, 10-90%, 25 pF load <sup>1</sup> | ..   | ..   | ..   | ns    |
| t <sub>RF,50pF</sub>  | Rise/fall time, standard drive mode, 10-90%, 50 pF load <sup>1</sup> | ..   | ..   | ..   | ns    |
| t <sub>HRF,15pF</sub> | Rise/Fall time, high drive mode, 10-90%, 15 pF load <sup>1</sup>     | ..   | ..   | ..   | ns    |
| t <sub>HRF,25pF</sub> | Rise/Fall time, high drive mode, 10-90%, 25 pF load <sup>1</sup>     | ..   | ..   | ..   | ns    |
| t <sub>HRF,50pF</sub> | Rise/Fall time, high drive mode, 10-90%, 50 pF load <sup>1</sup>     | ..   | ..   | ..   | ns    |
| R <sub>PU</sub>       | Pull-up resistance                                                   | ..   | ..   | ..   | kΩ    |
| R <sub>PD</sub>       | Pull-down resistance                                                 | ..   | ..   | ..   | kΩ    |
| C <sub>PAD</sub>      | Pad capacitance                                                      | ..   | ..   | ..   | pF    |
| C <sub>PAD_NFC</sub>  | Pad capacitance on NFC pads                                          | ..   | ..   | ..   | pF    |
| I <sub>NFC_LEAK</sub> | Leakage current between NFC pads when driven to different states     | ..   | ..   | ..   | μA    |

### 7.1.15 GPIOTE — GPIO tasks and events

The GPIO tasks and events (GPIOTE) module provides functionality for accessing GPIO pins using tasks and events. Each GPIOTE channel can be assigned to one pin.

A GPIOTE block enables GPIOs to generate events on pin state change which can be used to carry out tasks through the PPI system. A GPIO can also be driven to change state on system events using the PPI system. Tasks and events are briefly introduced in [Peripheral interface](#) on page 136, and GPIO is described in more detail in [GPIO — General purpose input/output](#) on page 209.

Low power detection of pin state changes is possible when in System ON or System OFF.

| Instance | Number of GPIOTE channels |
|----------|---------------------------|
| GPIOTE   | 8                         |

Table 79: GPIOTE properties

Up to three tasks can be used in each GPIOTE channel for performing write operations to a pin. Two tasks are fixed (SET and CLR), and one (OUT) is configurable to perform following operations:

- Set
- Clear

<sup>1</sup> Rise and fall times based on simulations



- Toggle

An event can be generated in each GPIOTE channel from one of the following input conditions:

- Rising edge
- Falling edge
- Any change

### 7.1.15.1 Pin events and tasks

The GPIOTE module has a number of tasks and events that can be configured to operate on individual GPIO pins.

The secure instance of the GPIOTE peripheral is able to operate on all GPIO pins configured in `GPIOTE.CONFIG[n].PSEL`.

The non-secure instance of the GPIOTE peripheral is able to operate only on non-secure GPIO pins. The field `GPIOTE.CONFIG[n].PSEL` can only select a non-secure pin.

The tasks `SET[n]`, `CLR[n]`, and `OUT[n]` can write to individual pins, and events `IN[n]` can be generated from input changes of individual pins.

The SET task will set the pin selected in `GPIOTE.CONFIG[n].PSEL` to high. The CLR task will set the pin low.

The effect of the OUT task on the pin is configurable in `CONFIG[n].POLARITY`. It can set the pin high, set it low, or toggle it.

Tasks and events are configured using the `CONFIG[n]` registers. One `CONFIG[n]` register is associated with a set of `SET[n]`, `CLR[n]`, and `OUT[n]` tasks and `IN[n]` events.

As long as a `SET[n]`, `CLR[n]`, and `OUT[n]` task or an `IN[n]` event is configured to control pin `n`, the pin's output value will only be updated by the GPIOTE module. The pin's output value, as specified in the GPIO, will therefore be ignored as long as the pin is controlled by GPIOTE. Attempting to write to the pin as a normal GPIO pin will have no effect. When the GPIOTE is disconnected from a pin, the associated pin gets the output and configuration values specified in the GPIO module, see `MODE` field in `CONFIG[n]` register.

When conflicting tasks are triggered simultaneously (i.e. during the same clock cycle) in one channel, the priority of the tasks is as described in the following table.

| Priority | Task |
|----------|------|
| 1        | OUT  |
| 2        | CLR  |
| 3        | SET  |

Table 80: Task priorities

When setting the `CONFIG[n]` registers, `MODE=Disabled` does not have the same effect as `MODE=Task` and `POLARITY=None`. In the latter case, a CLR or SET task occurring at the exact same time as OUT will end up with no change on the pin, based on the priorities described in the table above.

When a GPIOTE channel is configured to operate on a pin as a task, the initial value of that pin is configured in the `OUTINIT` field of `CONFIG[n]`.

### 7.1.15.2 Port event

PORT is an event that can be generated from multiple input pins using the GPIO DETECT signal.

The event will be generated on the rising edge of the DETECT signal. See [GPIO — General purpose input/output](#) on page 209 for more information about the DETECT signal.

There are two DETECT signals that come from the [GPIO](#) peripheral. The secure DETECT\_SEC, for the secure instance of the GPIOTE peripheral, and the non-secure DETECT\_NONSEC, for the non-secure instance of the GPIOTE peripheral.

The GPIO DETECT signal will not wake the system up again if the system is put into System ON IDLE while the DETECT signal is high. Make sure to clear all DETECT sources before entering sleep. If the LATCH register is used as a source, a new rising edge will be generated on DETECT if any bit in LATCH is still high after clearing all or part of the register. This could occur if one of the PINx.DETECT signals is still high, for example. See [Pin sense mechanism](#) on page 212 for more information.

Setting the system to System OFF while DETECT is high will cause a wakeup from System OFF reset.

This feature is always enabled even if the peripheral itself appears to be IDLE, meaning no clocks or other power intensive infrastructure have to be requested to keep this feature enabled. This feature can therefore be used to wake up the CPU from a WFI or WFE type sleep in System ON when all peripherals and the CPU are idle, meaning the lowest power consumption in System ON mode.

In order to prevent spurious interrupts from the PORT event while configuring the sources, the following must be performed:

1. Disable interrupts on the PORT event (through INTENCLR.PORT).
2. Configure the sources (PIN\_CNF[n].SENSE).
3. Clear any potential event that could have occurred during configuration (write '0' to EVENTS\_PORT).
4. Enable interrupts (through INTENSET.PORT).

### 7.1.15.3 Tasks and events pin configuration

Each GPIOTE channel is associated with one physical GPIO pin through the CONFIG.PSEL field.

When Event mode is selected in CONFIG.MODE, the pin specified by CONFIG.PSEL will be configured as an input, overriding the DIR setting in GPIO. Similarly, when Task mode is selected in CONFIG.MODE, the pin specified by CONFIG.PSEL will be configured as an output overriding the DIR setting and OUT value in GPIO. When Disabled is selected in CONFIG.MODE, the pin specified by CONFIG.PSEL will use its configuration from the PIN[n].CNF registers in GPIO. CONFIG.MODE must be disabled in order to be able to change the value of the PSEL field.

**Note:** A pin can only be assigned to one GPIOTE channel at a time. Failing to do so may result in unpredictable behavior.

### 7.1.15.4 Registers

| Base address | Domain      | Peripheral | Instance | Secure mapping | DMA security | Description           | Configuration |
|--------------|-------------|------------|----------|----------------|--------------|-----------------------|---------------|
| 0x5000D000   | APPLICATION | GPIOTE     | GPIOTE0  | S              | NA           | GPIO tasks and events |               |
| 0x4002F000   | APPLICATION | GPIOTE     | GPIOTE1  | NS             | NA           | GPIO tasks and events |               |
| 0x4100A000   | NETWORK     | GPIOTE     | GPIOTE   | NS             | NA           | GPIO tasks and events |               |

Table 81: Instances

| Register         | Offset | Security | Description                                                                                             |
|------------------|--------|----------|---------------------------------------------------------------------------------------------------------|
| TASKS_OUT[n]     | 0x000  |          | Task for writing to pin specified in CONFIG[n].PSEL. Action on pin is configured in CONFIG[n].POLARITY. |
| TASKS_SET[n]     | 0x030  |          | Task for writing to pin specified in CONFIG[n].PSEL. Action on pin is to set it high.                   |
| TASKS_CLR[n]     | 0x060  |          | Task for writing to pin specified in CONFIG[n].PSEL. Action on pin is to set it low.                    |
| SUBSCRIBE_OUT[n] | 0x080  |          | Subscribe configuration for task OUT[n]                                                                 |
| SUBSCRIBE_SET[n] | 0x0B0  |          | Subscribe configuration for task SET[n]                                                                 |
| SUBSCRIBE_CLR[n] | 0x0E0  |          | Subscribe configuration for task CLR[n]                                                                 |

| Register      | Offset | Security | Description                                                                |
|---------------|--------|----------|----------------------------------------------------------------------------|
| EVENTS_IN[n]  | 0x100  |          | Event generated from pin specified in CONFIG[n].PSEL                       |
| EVENTS_PORT   | 0x17C  |          | Event generated from multiple input GPIO pins with SENSE mechanism enabled |
| PUBLISH_IN[n] | 0x180  |          | Publish configuration for event IN[n]                                      |
| PUBLISH_PORT  | 0x1FC  |          | Publish configuration for event PORT                                       |
| INTENSET      | 0x304  |          | Enable interrupt                                                           |
| INTENCLR      | 0x308  |          | Disable interrupt                                                          |
| CONFIG[n]     | 0x510  |          | Configuration for OUT[n], SET[n], and CLR[n] tasks and IN[n] event         |

Table 82: Register overview

#### 7.1.15.4.1 TASKS\_OUT[n] (n=0..7)

Address offset:  $0x000 + (n \times 0x4)$

Task for writing to pin specified in CONFIG[n].PSEL. Action on pin is configured in CONFIG[n].POLARITY.

|                  |            |           |          |   |       |              |             |                                                                                                         |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-----------|----------|---|-------|--------------|-------------|---------------------------------------------------------------------------------------------------------|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |           |          |   |       |              |             |                                                                                                         |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |           |          |   |       |              |             |                                                                                                         |  | A  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |           |          |   |       |              |             |                                                                                                         |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |           | Value ID |   | Value |              | Description |                                                                                                         |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_OUT |          |   |       |              |             | Task for writing to pin specified in CONFIG[n].PSEL. Action on pin is configured in CONFIG[n].POLARITY. |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Trigger   |          | 1 |       | Trigger task |             |                                                                                                         |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.15.4.2 TASKS\_SET[n] (n=0..7)

Address offset:  $0x030 + (n \times 0x4)$

Task for writing to pin specified in CONFIG[n].PSEL. Action on pin is to set it high.

|                  |            |           |          |   |       |              |             |                                                                                       |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-----------|----------|---|-------|--------------|-------------|---------------------------------------------------------------------------------------|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |           |          |   |       |              |             |                                                                                       |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |           |          |   |       |              |             |                                                                                       |  | A  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |           |          |   |       |              |             |                                                                                       |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |           | Value ID |   | Value |              | Description |                                                                                       |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_SET |          |   |       |              |             | Task for writing to pin specified in CONFIG[n].PSEL. Action on pin is to set it high. |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |           | Trigger  | 1 |       | Trigger task |             |                                                                                       |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.15.4.3 TASKS\_CLR[n] (n=0..7)

Address offset:  $0x060 + (n \times 0x4)$

Task for writing to pin specified in CONFIG[n].PSEL. Action on pin is to set it low.

|                  |            |           |  |          |   |  |       |              |  |             |                                                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-----------|--|----------|---|--|-------|--------------|--|-------------|--------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |           |  |          |   |  |       |              |  | 31          | 30                                                                                   | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |           |  |          |   |  |       |              |  | A           |                                                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |           |  |          |   |  |       |              |  | 0           | 0                                                                                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |           |  | Value ID |   |  | Value |              |  | Description |                                                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_CLR |  |          |   |  |       |              |  |             | Task for writing to pin specified in CONFIG[n].PSEL. Action on pin is to set it low. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |           |  | Trigger  | 1 |  |       | Trigger task |  |             |                                                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.15.4.4 SUBSCRIBE OUT[n] (n=0..7)

Address offset:  $0x080 + (n \times 0x4)$

## Subscribe configuration for task OUT[n]

|                  |            |          |                                                                                       |  |  |  |                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|--|--|--|--------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |          | B                                                                                     |  |  |  |                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |  |  |  |                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 |  |  |  | Description                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                              |  |  |  | Channel that task OUT[n] will subscribe to |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |                                                                                       |  |  |  |                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     |  |  |  | Disable subscription                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     |  |  |  | Enable subscription                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

## 7.1.15.4.5 SUBSCRIBE\_SET[n] (n=0..7)

Address offset: 0x0B0 + (n × 0x4)

Subscribe configuration for task SET[n]

|                  |            |          |          |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|----------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |          |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |          |          | B                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value    | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0] | Channel that task SET[n] will subscribe to                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |          |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0        | Disable subscription                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1        | Enable subscription                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

## 7.1.15.4.6 SUBSCRIBE\_CLR[n] (n=0..7)

Address offset: 0x0E0 + (n × 0x4)

Subscribe configuration for task CLR[n]

| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|--------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| ID               |            |          | B                                                                                     |                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                              | Channel that task CLR[n] will subscribe to |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |                                                                                       |                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Disable subscription                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Enable subscription                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

## 7.1.15.4.7 EVENTS\_IN[n] (n=0..7)

Address offset: 0x100 + (n × 0x4)

Event generated from pin specified in CONFIG[n].PSEL

|                  |            |              |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|--------------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |              |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |              |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |              |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID     | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | EVENTS_IN    |       | Event generated from pin specified in CONFIG[n].PSEL                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | NotGenerated | 0     | Event not generated                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Generated    | 1     | Event generated                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.15.4.8 EVENTS\_PORT

Address offset: 0x17C

Event generated from multiple input GPIO pins with SENSE mechanism enabled

|                  |            |              |       |    |                                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|------------------|------------|--------------|-------|----|----------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| Bit number       |            |              | 31    | 30 | 29                                                                         | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| ID               |            |              | A     |    |                                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| Reset 0x00000000 |            |              | 0     | 0  | 0                                                                          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |
| ID               | Acce Field | Value ID     | Value |    | Description                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| A                | RW         | EVENTS_PORT  |       |    | Event generated from multiple input GPIO pins with SENSE mechanism enabled |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | NotGenerated | 0     |    | Event not generated                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | Generated    | 1     |    | Event generated                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

### 7.1.15.4.9 PUBLISH\_IN[n] (n=0..7)

Address offset: 0x180 + (n × 0x4)

Publish configuration for event IN[n]

|                  |            |       |          |          |    |                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-------|----------|----------|----|-------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |       |          | 31       | 30 | 29                                        | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |       |          | B        |    |                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |       |          | 0        | 0  | 0                                         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce Field |       | Value ID | Value    |    | Description                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | CHIDX |          | [255..0] |    | Channel that event IN[n] will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW         | EN    |          |          |    |                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |       | Disabled | 0        |    | Disable publishing                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |       | Enabled  | 1        |    | Enable publishing                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.15.4.10 PUBLISH\_PORT

Address offset: 0x1FC

Publish configuration for event PORT

|                  |            |          |          |    |                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|----|-------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          | 31       | 30 | 29                                              | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |          | B        |    |                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          | 0        | 0  | 0                                               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce Field | Value ID | Value    |    | Description                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | CHIDX    | [255..0] |    | Channel that event <b>PORT</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW         | EN       |          |    |                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        |    | Disable publishing                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        |    | Enable publishing                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.15.4.11 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number       |            |                | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------------|---------------------------------------------------------------------------------------|---------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| ID               |            |                | I                                                                                     |                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | H G F E D C B A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |                | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID       | Value                                                                                 | Description                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A-H              | RW         | IN[i] (i=0..7) |                                                                                       | Write '1' to enable interrupt for event <a href="#">IN[i]</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Set            | 1                                                                                     | Enable                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled       | 0                                                                                     | Read: Disabled                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled        | 1                                                                                     | Read: Enabled                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| I                | RW         | PORT           |                                                                                       | Write '1' to enable interrupt for event <a href="#">PORT</a>  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Set            | 1                                                                                     | Enable                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled       | 0                                                                                     | Read: Disabled                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled        | 1                                                                                     | Read: Enabled                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

#### 7.1.15.4.12 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number       |            |                | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------------|---------------------------------------------------------------------------------------|----------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| ID               |            |                | I                                                                                     |                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | H G F E D C B A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |                | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID       | Value                                                                                 | Description                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A-H              | RW         | IN[i] (i=0..7) |                                                                                       | Write '1' to disable interrupt for event <a href="#">IN[i]</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Clear          | 1                                                                                     | Disable                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled       | 0                                                                                     | Read: Disabled                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled        | 1                                                                                     | Read: Enabled                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| I                | RW         | PORT           |                                                                                       | Write '1' to disable interrupt for event <a href="#">PORT</a>  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Clear          | 1                                                                                     | Disable                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled       | 0                                                                                     | Read: Disabled                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled        | 1                                                                                     | Read: Enabled                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

#### 7.1.15.4.13 CONFIG[n] (n=0..7)

Address offset: 0x510 + (n × 0x4)

Configuration for OUT[n], SET[n], and CLR[n] tasks and IN[n] event

| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |         |  |  |  |     |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----|--|---------|--|--|--|-----|--|--|--|--|--|--|--|--|--|
| ID               |            |          | E                                                                                     |                                                                                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  | D D |  | C B B B |  |  |  | A A |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |         |  |  |  |     |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                                                                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |         |  |  |  |     |  |  |  |  |  |  |  |  |  |
| A                | RW         | MODE     |                                                                                       | Mode                                                                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |         |  |  |  |     |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Disabled. Pin specified by PSEL will not be acquired by the GPIOTE module.                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |         |  |  |  |     |  |  |  |  |  |  |  |  |  |
|                  |            | Event    | 1                                                                                     | Event mode                                                                                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |         |  |  |  |     |  |  |  |  |  |  |  |  |  |
|                  |            |          |                                                                                       | The pin specified by PSEL will be configured as an input and the IN[n] event will be generated if operation specified in POLARITY occurs on the pin. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |         |  |  |  |     |  |  |  |  |  |  |  |  |  |

| Bit number       |      |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |    |       |                                                                                                                                                                                                                                                                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|----------|---------------------------------------------------------------------------------------|----|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |      |          | E D D C B B B B A A                                                                   |    |       |                                                                                                                                                                                                                                                                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |    |       |                                                                                                                                                                                                                                                                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field    | Value                                                                                 | ID | Value | Description                                                                                                                                                                                                                                                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Task     | 3                                                                                     |    |       | Task mode                                                                                                                                                                                                                                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |          |                                                                                       |    |       | The GPIO specified by PSEL will be configured as an output and triggering the SET[n], CLR[n] or OUT[n] task will perform the operation specified by POLARITY on the pin. When enabled as a task the GPIOTE module will acquire the pin and the pin can no longer be written as a regular output pin from the GPIO module. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW   | PSEL     | [0..31]                                                                               |    |       | GPIO number associated with SET[n], CLR[n], and OUT[n] tasks and IN[n] event                                                                                                                                                                                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW   | PORT     | [0..1]                                                                                |    |       | Port number                                                                                                                                                                                                                                                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| D                | RW   | POLARITY |                                                                                       |    |       | When In task mode: Operation to be performed on output when OUT[n] task is triggered. When In event mode: Operation on input that shall trigger IN[n] event.                                                                                                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | None     | 0                                                                                     |    |       | Task mode: No effect on pin from OUT[n] task. Event mode: no IN[n] event generated on pin activity.                                                                                                                                                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | LoToHi   | 1                                                                                     |    |       | Task mode: Set pin from OUT[n] task. Event mode: Generate IN[n] event when rising edge on pin.                                                                                                                                                                                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | HiToLo   | 2                                                                                     |    |       | Task mode: Clear pin from OUT[n] task. Event mode: Generate IN[n] event when falling edge on pin.                                                                                                                                                                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Toggle   | 3                                                                                     |    |       | Task mode: Toggle pin from OUT[n]. Event mode: Generate IN[n] when any change on pin.                                                                                                                                                                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| E                | RW   | OUTINIT  |                                                                                       |    |       | When in task mode: Initial value of the output when the GPIOTE channel is configured. When in event mode: No effect.                                                                                                                                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Low      | 0                                                                                     |    |       | Task mode: Initial value of pin before task triggering is low                                                                                                                                                                                                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | High     | 1                                                                                     |    |       | Task mode: Initial value of pin before task triggering is high                                                                                                                                                                                                                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

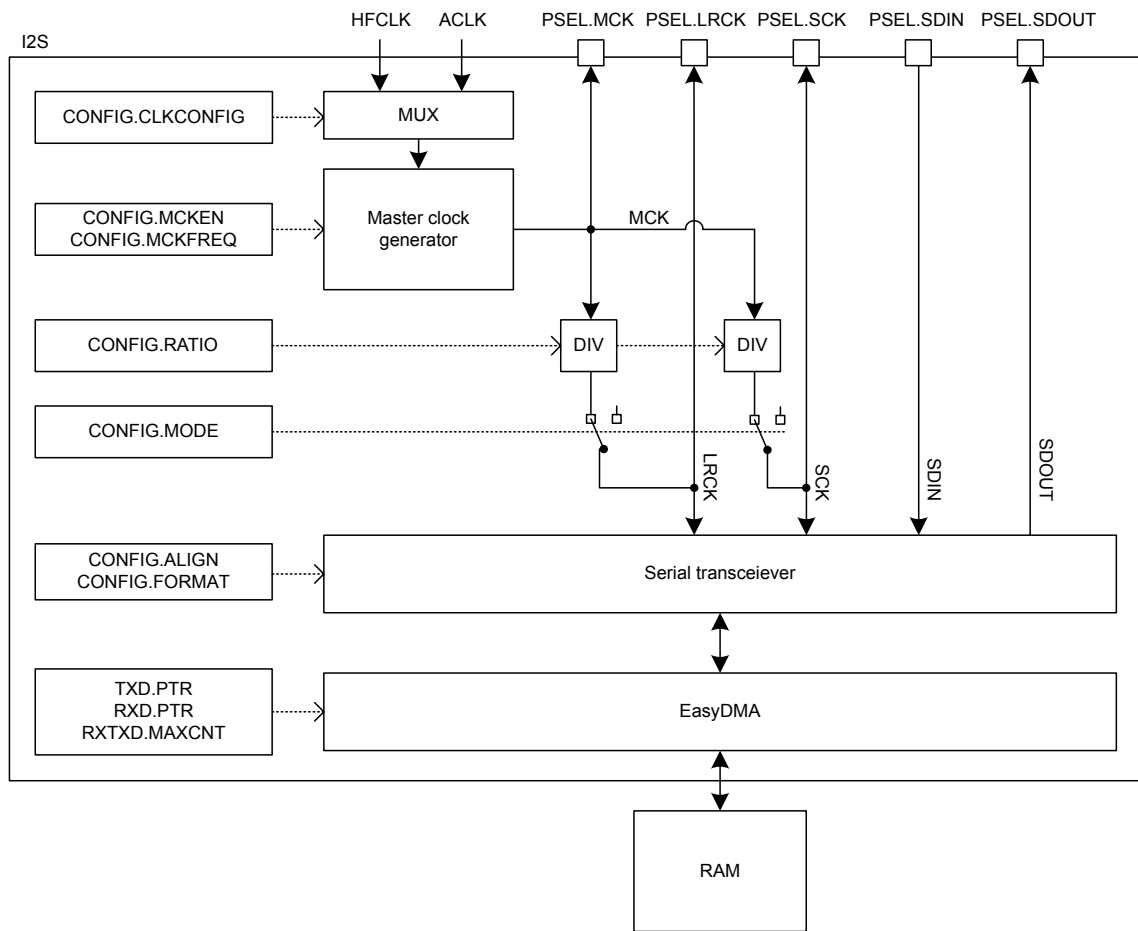
### 7.1.15.5 Electrical specification

## 7.1.16 I<sup>2</sup>S — Inter-IC sound interface

The I<sup>2</sup>S (Inter-IC Sound) module, supports the original two-channel I<sup>2</sup>S format, and left- or right-aligned formats. It implements EasyDMA for sample transfer directly to and from RAM without CPU intervention.

The I<sup>2</sup>S peripheral has the following main features:

- Master and Slave mode
- Simultaneous bidirectional (TX and RX) audio streaming
- Original I<sup>2</sup>S and left- or right-aligned format
- 32, 24, 16 and 8-bit sample widths
- Separate sample and word widths
- Low-jitter master clock generator
- Various sample rates

Figure 57: I<sup>2</sup>S master

### 7.1.16.1 Mode

The I<sup>2</sup>S protocol specification defines two modes of operation, Master and Slave.

The I<sup>2</sup>S mode decides which of the two sides (master or slave) shall provide the clock signals LRCK and SCK, and these signals are always supplied by the master to the slave.

### 7.1.16.2 Transmitting and receiving

The I<sup>2</sup>S module supports both transmission (TX) and reception (RX) of serial data. In both cases the serial data is shifted synchronously to the clock signals SCK and LRCK.

TX data is written to the SDOUT pin on the falling edge of SCK, and RX data is read from the SDIN pin on the rising edge of SCK. The most significant bit (MSB) is always transmitted first.

TX and RX are available in both Master and Slave modes and can be enabled/disabled independently in the [CONFIG.TXEN](#) on page 245 and [CONFIG.RXEN](#) on page 245.

Transmission and/or reception is started by triggering the [START](#) task. With transmission enabled in [CONFIG.TXEN](#), the [TXPTRUPD](#) event will be generated for every number of transmitted data words given by [RXTXD.MAXCNT](#) on page 250. Each data word contains one or more samples. The [TXPTRUPD](#) event is generated just before [MAXCNT](#) number of data words have been transmitted. Similarly, with reception enabled in [CONFIG.RXEN](#), the [RXPTRUPD](#) event will be generated for every received data word given by [RXTXD.MAXCNT](#) on page 250. The [RXPTRUPD](#) event is generated just after [MAXCNT](#) number of data bytes have been received.



The **FRAMESTART** event is generated synchronously to the active LRCK edge at the beginning of a frame after transmitting **RXTXD.MAXCNT** data words. The initial **FRAMESTART** event is generated at the first active edge of LRCK after the **START** task has been triggered.

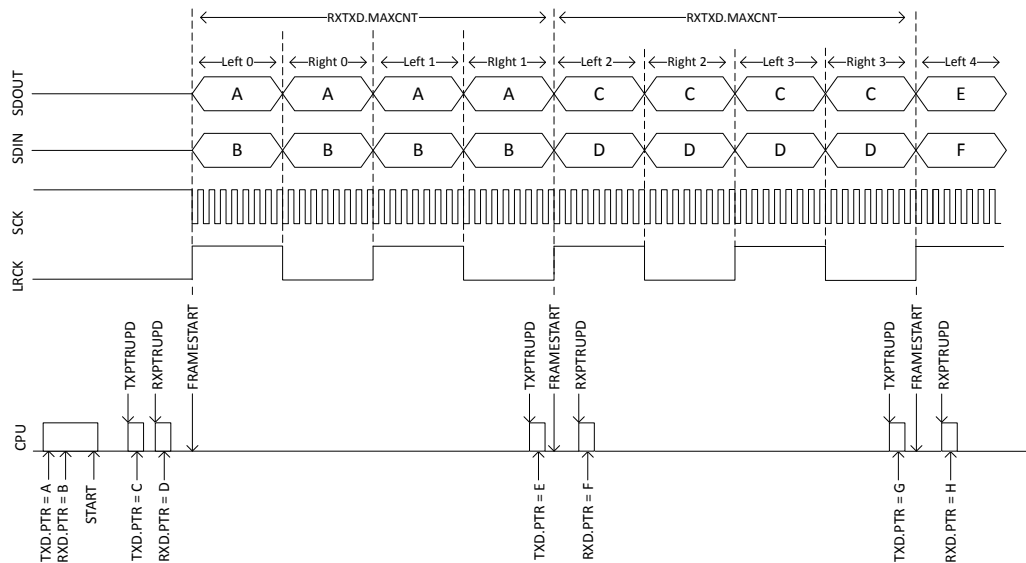


Figure 58: Transmitting and receiving. *CONFIG.FORMAT = Aligned, CONFIG.SWIDTH = 8Bit, CONFIG.CHANNELS = Stereo, RXTXD.MAXCNT = 1*

### 7.1.16.3 Left right clock (LRCK)

The left right clock (LRCK), often referred to as word clock, sample clock, or word select in I<sup>2</sup>S context, is the clock defining the frames in serial bitstreams sent and received on SDOUT and SDIN, respectively.

In I2S format, each frame contains one left and/or right sample pair. The left sample is transferred during the low half period of LRCK, followed by the right sample being transferred during the high half period of LRCK.

In Aligned format, each frame contains one left and/or right sample pair. The left sample is transferred during the high half period of LRCK, followed by the right sample being transferred during the low half period of LRCK.

For mono, the frame will contain only zeros for the unused half period of LRCK.

Consequently, the LRCK frequency is equivalent to the audio sample rate.

When operating in Master mode, the LRCK is generated from the MCK, and the frequency of LRCK is then given as:

$$\text{LRCK} = \text{MCK} / \text{CONFIG.RATIO}$$

LRCK always toggles around the falling edge of the serial clock SCK.

### 7.1.16.4 Serial clock (SCK)

The serial clock (SCK), often referred to as the serial bit clock, pulses once for each data bit being transferred on the serial data lines SDIN and SDOUT.

When operating in Master mode, the SCK is generated from the MCK, and the frequency of SCK is then given as:

$$\text{SCK} = 2 * \text{LRCK} * \text{CONFIG.SWIDTH}$$

The falling edge of the SCK falls on the toggling edge of LRCK.

When operating in Slave mode, SCK is provided by the external I<sup>2</sup>S master.

### 7.1.16.5 Master clock (MCK)

The master clock (MCK) is the clock from which LRCK and SCK are derived when operating in Master mode.

The master clock generator always needs to be enabled when in Master mode, but the generator can also be enabled when in Slave mode. Enabling the generator when in Slave mode can be useful in the case where the external master is not able to generate its own master clock.

MCK is generated from the clock source selected in the [CONFIG.CLKCONFIG](#) and [CONFIG.MCKFREQ](#) registers.

The following equation can be used to calculate the value of [CONFIG.MCKFREQ](#) for given MCK and clock source frequency:

$$MCKFREQ = 4096 \cdot \left\lceil \frac{f_{MCK} \cdot 1048576}{f_{source} + \frac{f_{MCK}}{2}} \right\rceil$$

Figure 59: MCK clock frequency equation

The parameter  $f_{MCK}$  is the requested MCK clock frequency in Hz, and  $f_{source}$  is the frequency of the selected clock source in Hz. Because of rounding errors, an accurate MCK clock may not be achievable. The equation does not take into account the maximum register value of [CONFIG.MCKFREQ](#) on page 246.

The actual MCK frequency can be calculated using the equation below.

$$f_{actual} = \frac{f_{source}}{\left\lceil \frac{1048576 \cdot 4096}{MCKFREQ} \right\rceil}$$

Figure 60: Actual MCK clock frequency

The clock error can be calculated using the equation below. The error  $e$  is the percentage difference from the requested  $f_{MCK}$  frequency.

$$e = 100 \cdot \frac{f_{actual} - f_{MCK}}{f_{MCK}} = 100 \cdot \frac{\frac{f_{source}}{\left\lceil \frac{1048576 \cdot 4096}{MCKFREQ} \right\rceil} - f_{MCK}}{f_{MCK}}$$

Figure 61: MCK frequency error equation

The master clock generator does not add any jitter to the clock source chosen.

The master clock generator is enabled/disabled using [CONFIG.MCKEN](#) on page 246, and the generator is started or stopped by the [START](#) or [STOP](#) tasks respectively.

The MCK frequency can be adjusted on-the-fly:

- For PCLK32M, by using [MCKFREQ](#)
- For ACLK, by adjusting the audio clock source, see [CLOCK — Clock control](#) on page 61.

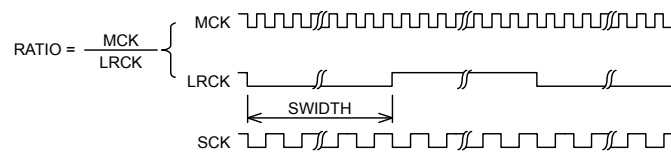
In Master mode, the LRCK and the SCK frequencies are closely related as both are derived from MCK and set indirectly through [CONFIG.RATIO](#) on page 247 and [CONFIG.SWIDTH](#) on page 248.

When configuring these registers, the user is responsible for fulfilling the following requirements:

1. The SCK frequency can never exceed the MCK frequency.
2. The MCK/LRCK ratio shall be a multiple of  $2 \cdot \text{CONFIG.SWIDTH}$ .

The MCK signal can be routed to an output pin (specified in [PSEL.MCK](#)) to supply external I<sup>2</sup>S devices that require the MCK to be supplied from the outside.

When operating in Slave mode, the I<sup>2</sup>S module does not use the MCK and the MCK generator does not need to be enabled.

Figure 62: Relation between *RATIO*, *MCK* and *LRCK*

#### 7.1.16.5.1 Clock source selection

The clock source for the master clock generator can be selected in the register [CONFIG.CLKCONFIG](#) on page 249. Choose one of the following clocks as the clock source:

- 32 MHz peripheral clock (PCLK32M), synchronous to HFCLK.
- Audio PLL clock (ACLK) with configurable frequency.

To improve the master clock accuracy and jitter performance, it is recommended (but not mandatory) that the source is running off the HFXO instead of the HFINT oscillator. See [CLOCK — Clock control](#) on page 61 for more information about starting HFXO for the relevant clock source.

The master clock generator can be bypassed so the MCK clock is derived directly from the input source. This can be configured in the BYPASS field of register [CONFIG.CLKCONFIG](#) on page 249.

#### 7.1.16.5.2 Configuration examples

Table 83: Configuration examples for [CLKCONFIG = PCLK32M](#) on page 231 and Table 84: Configuration examples for [CLKCONFIG = ACLK](#) on page 232 show some configuration examples for popular sample rates, using both the 32 MHz master clock and the Audio PLL clock source.

| Source frequency [Hz] | Requested LRCK [Hz] | Requested RATIO | Requested MCK [Hz] | MCKFREQ   | MCK [Hz] | LRCK [Hz] | LRCK error [%] |
|-----------------------|---------------------|-----------------|--------------------|-----------|----------|-----------|----------------|
| 32000000              | 16000               | 32              | 512000             | 68173824  | 507936   | 15873     | -0.8           |
| 32000000              | 16000               | 64              | 1024000            | 135274496 | 1032258  | 16129     | 0.8            |
| 32000000              | 16000               | 256             | 4096000            | 516685824 | 4000000  | 15625     | -2.3           |
| 32000000              | 32000               | 32              | 1024000            | 135274496 | 1032258  | 32258     | 0.8            |
| 32000000              | 32000               | 64              | 2048000            | 266350592 | 2000000  | 31250     | -2.3           |
| 32000000              | 32000               | 256             | 8192000            | 974741504 | 8000000  | 31250     | -2.3           |
| 32000000              | 44100               | 32              | 1411200            | 185319424 | 1391304  | 43478     | -1.4           |
| 32000000              | 44100               | 64              | 2822400            | 362815488 | 2909090  | 45455     | 3.1            |
| 32000000              | 48000               | 32              | 1536000            | 201326592 | 1523809  | 47619     | -0.8           |
| 32000000              | 48000               | 64              | 3072000            | 393428992 | 3200000  | 50000     | 4.2            |
| 32000000              | 96000               | 32              | 3072000            | 393428992 | 3200000  | 100000    | 4.2            |
| 32000000              | 96000               | 64              | 6144000            | 752402432 | 6400000  | 100000    | 4.2            |

Table 83: Configuration examples for *CLKCONFIG = PCLK32M*

| Source frequency [Hz] | Requested LRCK [Hz] | RATIO | Requested MCK [Hz] | MCKFREQ   | MCK [Hz] | LRCK [Hz] | LRCK error [%] |
|-----------------------|---------------------|-------|--------------------|-----------|----------|-----------|----------------|
| 11289600              | 44100               | 32    | 1411200            | 505286656 | 1411200  | 44100     | 0              |
| 11289600              | 44100               | 64    | 2822400            | 954433536 | 2822400  | 44100     | 0              |
| 12288000              | 16000               | 32    | 510000             | 175304704 | 512000   | 16000     | 0              |
| 12288000              | 16000               | 64    | 1024000            | 343597056 | 1024000  | 16000     | 0              |
| 12288000              | 32000               | 32    | 1024000            | 343597056 | 1024000  | 32000     | 0              |
| 12288000              | 32000               | 64    | 2048000            | 660762624 | 2048000  | 32000     | 0              |
| 12288000              | 48000               | 32    | 1536000            | 505286656 | 1536000  | 48000     | 0              |
| 12288000              | 48000               | 64    | 3072000            | 954433536 | 3072000  | 48000     | 0              |
| 12288000              | 96000               | 32    | 3072000            | 954433536 | 3072000  | 96000     | 0              |

Table 84: Configuration examples for CLKCONFIG = ACLK

### 7.1.16.6 Width, alignment and format

The register `CONFIG.SWIDTH` on page 248 defines the sample width of the data read and written to memory, as well as the number of SCK clock cycles per half-frame. Figure [Figure 63: Aligned format, with CONFIG.SWIDTH configured to 16 bit samples in a 16 bit half-frame](#) on page 232 illustrates a configuration with identical sample and half-frame widths. The number of SCK pulses matches the number of sample bits. Figure [Figure 64: Aligned format, with CONFIG.SWIDTH configured to 16-bit samples in a 24-bit half-frame](#) on page 232 illustrates a configuration with greater half-frame width than sample width. The number of SCK pulses are greater than the number of sample bits, with the sample being left-aligned in the half-frame.

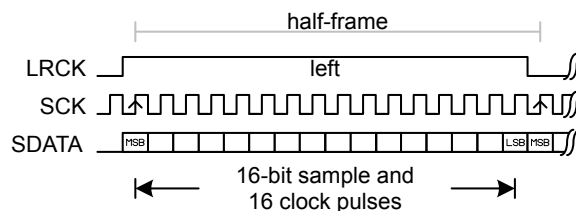


Figure 63: Aligned format, with CONFIG.SWIDTH configured to 16 bit samples in a 16 bit half-frame

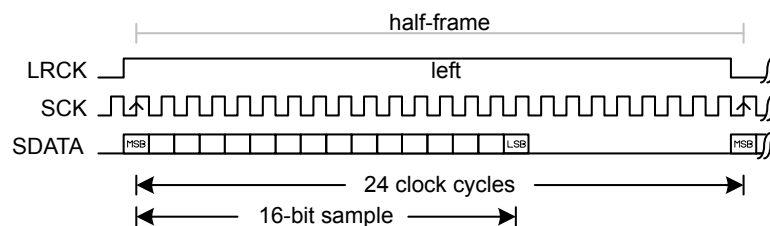


Figure 64: Aligned format, with CONFIG.SWIDTH configured to 16-bit samples in a 24-bit half-frame

The register `CONFIG.FORMAT` on page 248 is used to choose whether a word shall be aligned on the LRCK edge, or be delayed one bit period after this edge:

- When using Aligned format, the first bit in a half-frame gets sampled on the first rising edge of SCK following a LRCK edge, as illustrated in [Figure 65: Aligned format. Identical sample width and half-frame width. Left sample on high level of LRCK](#) on page 233. The left sample is transferred during the high half period of LRCK.
- When using I<sup>2</sup>S format, the first bit in a half-frame (containing one left or right sample) gets sampled on the second rising edge of the SCK after a LRCK edge, as illustrated in [Figure 66: I<sup>2</sup>S format. Identical](#)

sample width and half-frame width. Left sample on low level of LRCK on page 233. The left sample is transferred during the low half period of LRCK.

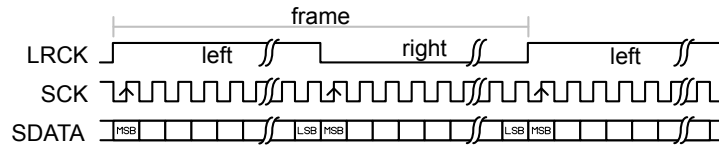


Figure 65: Aligned format. Identical sample width and half-frame width. Left sample on high level of LRCK

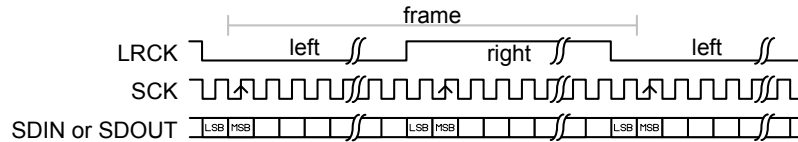


Figure 66: I<sup>2</sup>S format. Identical sample width and half-frame width. Left sample on low level of LRCK

If the half-frame width differs from the sample width, the sample value can be either right or left-aligned inside a half-frame, as specified in [CONFIG.ALIGN](#) on page 248

- When using left-alignment, each half-frame starts with the MSB of the sample value, as illustrated by [Figure 67: CONFIG.ALIGN set to left justified](#) on page 233.
- When using right-alignment, each half-frame ends with the LSB of the sample value. This is illustrated in [Figure 68: CONFIG.ALIGN set to right justified](#) on page 233.

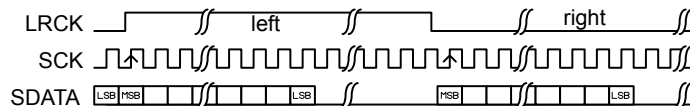


Figure 67: CONFIG.ALIGN set to left justified

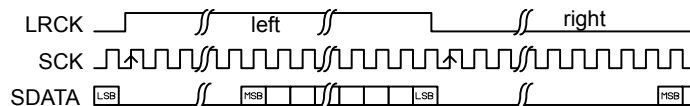


Figure 68: CONFIG.ALIGN set to right justified

## Slave mode considerations

In Slave mode, the sample width does not need to equal the half-frame width, or even frame size. This means that there can be extra or fewer SCK pulses per half-frame than what the sample and half-frame widths specified in [CONFIG.SWIDTH](#) on page 248 require.

In cases where **left-alignment** is used, and the number of SCK pulses per half-frame is **higher** than the configured width, the following will apply:

- For data received on SDIN, all bits after the least significant bit (LSB) of the word value will be discarded.
- For data sent on SDOUT, all bits after the LSB of the word value will be 0.

In cases where **left-alignment** is used, and the number of SCK pulses per frame is **lower** than the word width, the following will apply:

- Data sent and received on SDOUT and SDIN will be truncated with the LSBs being removed first.

In cases where **right-alignment** is used, and the number of SCK pulses per frame is **higher** than the configured width, the following will apply:

- For data received on SDIN, all bits before the MSB of the word value will be discarded.

- For data sent on SDOUT, all bits after the LSB of the word value will be 0 (same behavior as for left-alignment).

In cases where **right-alignment** is used, and the number of SCK pulses per frame is **lower** than the configured width, the following will apply:

- Data received on SDIN will be sign-extended to the same number of bits as the sample width before being written to memory.
- Data sent on SDOUT will be truncated with the LSBs being removed first (same behavior as for left-alignment).

### 7.1.16.7 EasyDMA

The I<sup>2</sup>S module implements EasyDMA for accessing internal Data RAM without CPU intervention.

The source and destination pointers for the TX and RX data are configured in [TXD.PTR](#) on page 249 and [RXD.PTR](#) on page 249. The memory pointed to by these pointers will only be read or written when TX or RX are enabled in [CONFIG.TXEN](#) on page 245, and [CONFIG.RXEN](#) on page 245.

The addresses written to the pointer registers [TXD.PTR](#) on page 249 and [RXD.PTR](#) on page 249 are double-buffered in hardware. These double buffers are updated for every number of transmitted data words given by [RXTXD.MAXCNT](#) on page 250 read from/written to memory. The events TXPTRUPD and RXPTRUPD are generated whenever the TXD.PTR and RXD.PTR are transferred to these double buffers.

If [TXD.PTR](#) on page 249 is not pointing to the Data RAM region when transmission is enabled, or [RXD.PTR](#) on page 249 is not pointing to the Data RAM region when reception is enabled, an EasyDMA transfer may result in a HardFault and/or memory corruption. See [Memory](#) on page 18 for more information about the different memory regions.

Due to the nature of I<sup>2</sup>S, where the number of transmitted samples always equals the number of received samples (at least when both TX and RX are enabled), one common register [RXTXD.MAXCNT](#) on page 250 is used for specifying the sizes of these two memory buffers. The size of the buffers is specified in a number of 32-bit words. Such a 32-bit memory word can either contain one 32-bit sample, one right-aligned 24-bit sample sign extended to 32-bit, two 16-bit samples or four 8-bit samples.

In Stereo mode ([CONFIG.CHANNELS](#) on page 248=Stereo), the samples are stored as left and right sample pairs in memory. [Figure 69: Memory mapping for 8-bit stereo](#). [CONFIG.SWIDTH = 8Bit](#), [CONFIG.CHANNELS = Stereo](#). on page 235, [Figure 71: Memory mapping for 16-bit stereo](#). [CONFIG.SWIDTH = 16Bit](#), [CONFIG.CHANNELS = Stereo](#). on page 235 and [Figure 73: Memory mapping for 24-bit stereo](#). [CONFIG.SWIDTH = 24Bit](#), [CONFIG.CHANNELS = Stereo](#). on page 236 show how the samples are mapped to memory in this mode. The mapping is valid for both RX and TX.

In Mono mode ([CONFIG.CHANNELS](#) on page 248=Left or Right), RX sample from only one channel in the frame is stored in memory, the other channel sample is ignored. [Figure 70: Memory mapping for 8-bit mono](#). [CONFIG.SWIDTH = 8Bit](#), [CONFIG.CHANNELS = Left](#). on page 235, [Figure 72: Memory mapping for 16-bit mono, left channel only](#). [CONFIG.SWIDTH = 16Bit](#), [CONFIG.CHANNELS = Left](#). on page 235 and [Figure 74: Memory mapping for 24-bit mono, left channel only](#). [CONFIG.SWIDTH = 24Bit](#), [CONFIG.CHANNELS = Left](#). on page 236 show how RX samples are mapped to memory in this mode. For TX, the same outgoing sample read from memory is transmitted on both left and right in a frame, resulting in a mono output stream.

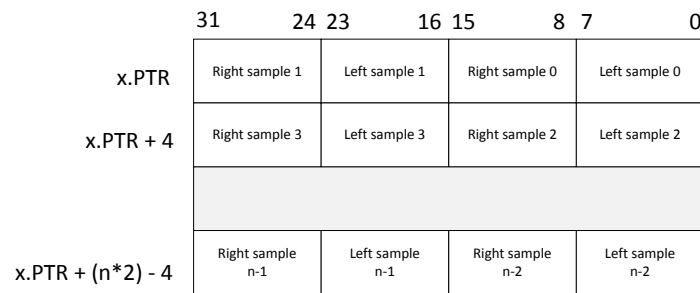


Figure 69: Memory mapping for 8-bit stereo. CONFIG.SWIDTH = 8Bit, CONFIG.CHANNELS = Stereo.

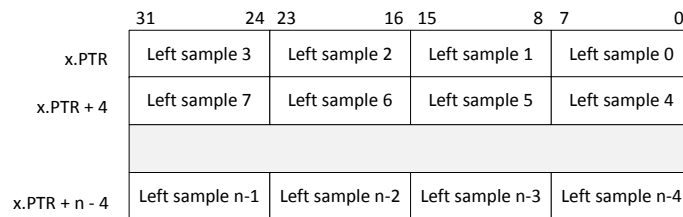


Figure 70: Memory mapping for 8-bit mono. CONFIG.SWIDTH = 8Bit, CONFIG.CHANNELS = Left.

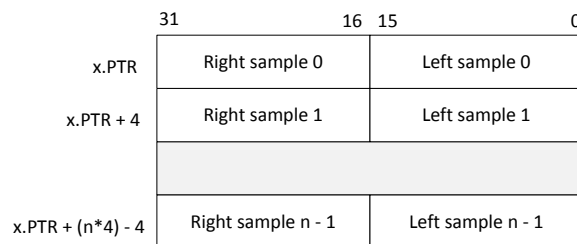


Figure 71: Memory mapping for 16-bit stereo. CONFIG.SWIDTH = 16Bit, CONFIG.CHANNELS = Stereo.

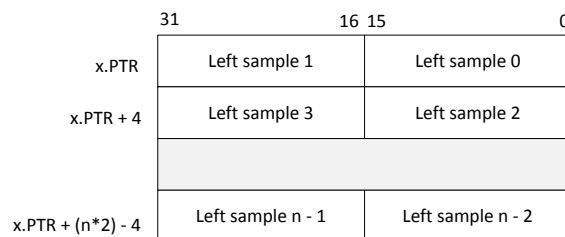


Figure 72: Memory mapping for 16-bit mono, left channel only. CONFIG.SWIDTH = 16Bit, CONFIG.CHANNELS = Left.

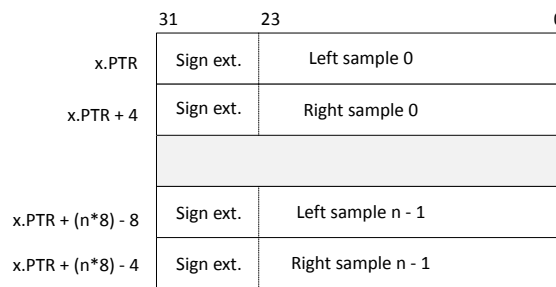


Figure 73: Memory mapping for 24-bit stereo. *CONFIG.SWIDTH = 24Bit, CONFIG.CHANNELS = Stereo.*

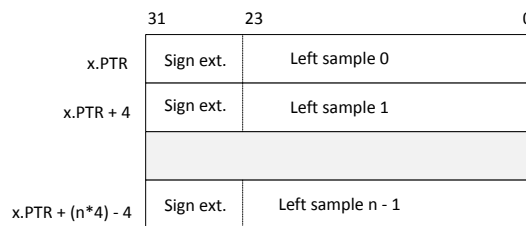


Figure 74: Memory mapping for 24-bit mono, left channel only. *CONFIG.SWIDTH = 24Bit, CONFIG.CHANNELS = Left.*

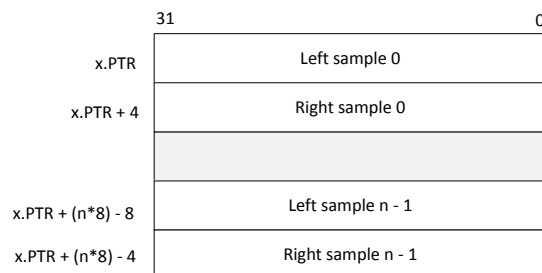


Figure 75: Memory mapping for 32-bit stereo. *CONFIG.SWIDTH = 32Bit, CONFIG.CHANNELS = Stereo.*

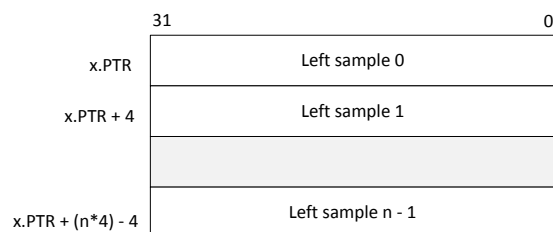


Figure 76: Memory mapping for 32-bit mono, left channel only. *CONFIG.SWIDTH = 32Bit, CONFIG.CHANNELS = Left.*

### 7.1.16.8 Module operation

Described here is a typical operating procedure for the I<sup>2</sup>S module.



## 1. Configure the I<sup>2</sup>S module using the CONFIG registers

```
// Enable reception
NRF_I2S->CONFIG.RXEN = (I2S_CONFIG_RXEN_RXEN_Enabled <<
                        I2S_CONFIG_RXEN_RXEN_Pos);

// Enable transmission
NRF_I2S->CONFIG.TXEN = (I2S_CONFIG_TXEN_TXEN_Enabled <<
                        I2S_CONFIG_TXEN_TXEN_Pos);

// Enable MCK generator
NRF_I2S->CONFIG.MCKEN = (I2S_CONFIG_MCKEN_MCKEN_Enabled <<
                        I2S_CONFIG_MCKEN_MCKEN_Pos);

// MCKFREQ = 4 MHz
NRF_I2S->CONFIG.MCKFREQ = I2S_CONFIG_MCKFREQ_MCKFREQ_32MDIV8 <<
                        I2S_CONFIG_MCKFREQ_MCKFREQ_Pos;

// Ratio = 256
NRF_I2S->CONFIG.RATIO = I2S_CONFIG_RATIO_RATIO_256X <<
                        I2S_CONFIG_RATIO_RATIO_Pos;

// MCKFREQ = 4 MHz and Ratio = 256 gives sample rate = 15.625 ks/s
// Sample width = 16 bit
NRF_I2S->CONFIG.SWIDTH = I2S_CONFIG_SWIDTH_SWIDTH_16Bit <<
                        I2S_CONFIG_SWIDTH_SWIDTH_Pos;

// Alignment = Left
NRF_I2S->CONFIG.ALIGN = I2S_CONFIG_ALIGN_ALIGN_Left <<
                        I2S_CONFIG_ALIGN_ALIGN_Pos;

// Format = I2S
NRF_I2S->CONFIG.FORMAT = I2S_CONFIG_FORMAT_FORMAT_I2S <<
                        I2S_CONFIG_FORMAT_FORMAT_Pos;

// Use stereo
NRF_I2S->CONFIG.CHANNELS = I2S_CONFIG_CHANNELS_CHANNELS_Stereo <<
                        I2S_CONFIG_CHANNELS_CHANNELS_Pos;
```

## 2. Map IO pins using the PINSEL registers

```
// MCK routed to pin 0
NRF_I2S->PSEL.MCK = (0 << I2S_PSEL_MCK_PIN_Pos) |
                    (I2S_PSEL_MCK_CONNECT_Connected <<
                     I2S_PSEL_MCK_CONNECT_Pos);

// SCK routed to pin 1
NRF_I2S->PSEL.SCK = (1 << I2S_PSEL_SCK_PIN_Pos) |
                    (I2S_PSEL_SCK_CONNECT_Connected <<
                     I2S_PSEL_SCK_CONNECT_Pos);

// LRCK routed to pin 2
NRF_I2S->PSEL.LRCK = (2 << I2S_PSEL_LRCK_PIN_Pos) |
                     (I2S_PSEL_LRCK_CONNECT_Connected <<
                      I2S_PSEL_LRCK_CONNECT_Pos);

// SDOUT routed to pin 3
NRF_I2S->PSEL.SDOUT = (3 << I2S_PSEL_SDOUT_PIN_Pos) |
                      (I2S_PSEL_SDOUT_CONNECT_Connected <<
                       I2S_PSEL_SDOUT_CONNECT_Pos);

// SDIN routed on pin 4
NRF_I2S->PSEL.SDIN = (4 << I2S_PSEL_SDIN_PIN_Pos) |
                     (I2S_PSEL_SDIN_CONNECT_Connected <<
                      I2S_PSEL_SDIN_CONNECT_Pos);
```

### 3. Configure TX and RX data pointers using the TXD, RXD and RXTXD registers

```
NRF_I2S->TXD.PTR = my_tx_buf;
NRF_I2S->RXD.PTR = my_rx_buf;
NRF_I2S->TXD.MAXCNT = MY_BUF_SIZE;
```

### 4. Enable the I<sup>2</sup>S module using the ENABLE register

```
NRF_I2S->ENABLE = 1;
```

### 5. Start audio streaming using the START task

```
NRF_I2S->TASKS_START = 1;
```

### 6. Handle received and transmitted data when receiving the TXPTRUPD and RXPTRUPD events

```
if (NRF_I2S->EVENTS_TXPTRUPD != 0)
{
    NRF_I2S->TXD.PTR = my_next_tx_buf;
    NRF_I2S->EVENTS_TXPTRUPD = 0;
}

if (NRF_I2S->EVENTS_RXPTRUPD != 0)
{
    NRF_I2S->RXD.PTR = my_next_rx_buf;
    NRF_I2S->EVENTS_RXPTRUPD = 0;
}
```

#### 7.1.16.9 Pin configuration

The MCK, SCK, LRCK, SDIN and SDOUT signals associated with the I<sup>2</sup>S module are mapped to physical pins according to the pin numbers specified in the PSEL.x registers.

These pins are acquired whenever the I<sup>2</sup>S module is enabled through the register [ENABLE](#) on page 245.

When a pin is acquired by the I<sup>2</sup>S module, the direction of the pin (input or output) will be configured automatically, and any pin direction setting done in the GPIO module will be overridden. The directions for the various I<sup>2</sup>S pins are shown below in [Table 85: GPIO configuration before enabling peripheral \(Master mode\)](#) on page 238 and [Table 86: GPIO configuration before enabling peripheral \(Slave mode\)](#) on page 239.

To secure correct signal levels on the pins in System OFF mode, and when the I<sup>2</sup>S module is disabled, these pins must be configured in the GPIO peripheral directly.

| I <sup>2</sup> S signal | I <sup>2</sup> S pin       | Direction | Output value   | Comment |
|-------------------------|----------------------------|-----------|----------------|---------|
| MCK                     | As specified in PSEL.MCK   | Output    | 0              |         |
| LRCK                    | As specified in PSEL.LRCK  | Output    | 0              |         |
| SCK                     | As specified in PSEL.SCK   | Output    | 0              |         |
| SDIN                    | As specified in PSEL.SDIN  | Input     | Not applicable |         |
| SDOUT                   | As specified in PSEL.SDOUT | Output    | 0              |         |

Table 85: GPIO configuration before enabling peripheral (Master mode)

| I <sup>2</sup> S signal | I <sup>2</sup> S pin       | Direction | Output value   | Comment |
|-------------------------|----------------------------|-----------|----------------|---------|
| MCK                     | As specified in PSEL.MCK   | Output    | 0              |         |
| LRCK                    | As specified in PSEL.LRCK  | Input     | Not applicable |         |
| SCK                     | As specified in PSEL.SCK   | Input     | Not applicable |         |
| SDIN                    | As specified in PSEL.SDIN  | Input     | Not applicable |         |
| SDOUT                   | As specified in PSEL.SDOUT | Output    | 0              |         |

Table 86: GPIO configuration before enabling peripheral (Slave mode)

### 7.1.16.10 Registers

| Base address | Domain      | Peripheral | Instance  | Secure mapping | DMA security | Description              | Configuration |
|--------------|-------------|------------|-----------|----------------|--------------|--------------------------|---------------|
| 0x50028000   | APPLICATION | I2S        | I2S0 : S  | US             | SA           | Inter-IC sound interface |               |
| 0x40028000   |             |            | I2S0 : NS |                |              |                          |               |

Table 87: Instances

| Register           | Offset | Security | Description                                                                                                                                                                                                  |
|--------------------|--------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TASKS_START        | 0x000  |          | Starts continuous I2S transfer. Also starts MCK generator when this is enabled                                                                                                                               |
| TASKS_STOP         | 0x004  |          | Stops I2S transfer. Also stops MCK generator. Triggering this task will cause the event STOPPED to be generated.                                                                                             |
| SUBSCRIBE_START    | 0x080  |          | Subscribe configuration for task START                                                                                                                                                                       |
| SUBSCRIBE_STOP     | 0x084  |          | Subscribe configuration for task STOP                                                                                                                                                                        |
| EVENTS_RXPTRUPD    | 0x104  |          | The RXD.PTR register has been copied to internal double-buffers. When the I2S module is started and RX is enabled, this event will be generated for every RXTXD.MAXCNT words received on the SDIN pin.       |
| EVENTS_STOPPED     | 0x108  |          | I2S transfer stopped.                                                                                                                                                                                        |
| EVENTS_TXPTRUPD    | 0x114  |          | The TDX.PTR register has been copied to internal double-buffers. When the I2S module is started and TX is enabled, this event will be generated for every RXTXD.MAXCNT words that are sent on the SDOUT pin. |
| EVENTS_FRAMESTART  | 0x11C  |          | Frame start event, generated on the active edge of LRCK                                                                                                                                                      |
| PUBLISH_RXPTRUPD   | 0x184  |          | Publish configuration for event RXPTRUPD                                                                                                                                                                     |
| PUBLISH_STOPPED    | 0x188  |          | Publish configuration for event STOPPED                                                                                                                                                                      |
| PUBLISH_TXPTRUPD   | 0x194  |          | Publish configuration for event TXPTRUPD                                                                                                                                                                     |
| PUBLISH_FRAMESTART | 0x19C  |          | Publish configuration for event FRAMESTART                                                                                                                                                                   |
| INTEN              | 0x300  |          | Enable or disable interrupt                                                                                                                                                                                  |
| INTENSET           | 0x304  |          | Enable interrupt                                                                                                                                                                                             |
| INTENCLR           | 0x308  |          | Disable interrupt                                                                                                                                                                                            |
| ENABLE             | 0x500  |          | Enable I2S module                                                                                                                                                                                            |
| CONFIG.MODE        | 0x504  |          | I2S mode                                                                                                                                                                                                     |
| CONFIG.RXEN        | 0x508  |          | Reception (RX) enable                                                                                                                                                                                        |
| CONFIG.TXEN        | 0x50C  |          | Transmission (TX) enable                                                                                                                                                                                     |
| CONFIG.MCKEN       | 0x510  |          | Master clock generator enable                                                                                                                                                                                |
| CONFIG.MCKFREQ     | 0x514  |          | I2S clock generator control                                                                                                                                                                                  |
| CONFIG.RATIO       | 0x518  |          | MCK / LRCK ratio                                                                                                                                                                                             |
| CONFIG.SWIDTH      | 0x51C  |          | Sample width                                                                                                                                                                                                 |
| CONFIG.ALIGN       | 0x520  |          | Alignment of sample within a frame                                                                                                                                                                           |
| CONFIG.FORMAT      | 0x524  |          | Frame format                                                                                                                                                                                                 |
| CONFIG.CHANNELS    | 0x528  |          | Enable channels                                                                                                                                                                                              |
| CONFIG.CLKCONFIG   | 0x52C  |          | Clock source selection for the I2S module                                                                                                                                                                    |
| RXD.PTR            | 0x538  |          | Receive buffer RAM start address.                                                                                                                                                                            |
| TXD.PTR            | 0x540  |          | Transmit buffer RAM start address                                                                                                                                                                            |
| RXTXD.MAXCNT       | 0x550  |          | Size of RXD and TXD buffers                                                                                                                                                                                  |

| Register   | Offset | Security | Description                 |
|------------|--------|----------|-----------------------------|
| PSEL.MCK   | 0x560  |          | Pin select for MCK signal   |
| PSEL.SCK   | 0x564  |          | Pin select for SCK signal   |
| PSEL.LRCK  | 0x568  |          | Pin select for LRCK signal  |
| PSEL.SDIN  | 0x56C  |          | Pin select for SDIN signal  |
| PSEL.SDOUT | 0x570  |          | Pin select for SDOUT signal |

Table 88: Register overview

### 7.1.16.10.1 TASKS\_START

Address offset: 0x000

Starts continuous I2S transfer. Also starts MCK generator when this is enabled

|                  |      |             |       |                                                                                       |       |                                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|-------------|-------|---------------------------------------------------------------------------------------|-------|--------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |             |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |             |       | A                                                                                     |       |                                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |             |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                   |       |                                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field       | Value | ID                                                                                    | Value | Description                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W    | TASKS_START |       |                                                                                       |       | Starts continuous I2S transfer. Also starts MCK generator when this is enabled |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Trigger     |       | 1                                                                                     |       | Trigger task                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.16.10.2 TASKS\_STOP

Address offset: 0x004

Stops I2S transfer. Also stops MCK generator. Triggering this task will cause the event **STOPPED** to be generated.

|                  |            |            |       |                                                                                                                  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |
|------------------|------------|------------|-------|------------------------------------------------------------------------------------------------------------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|--|--|
| Bit number       |            |            | 31    | 30                                                                                                               | 29           | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |  |
| ID               |            |            | A     |                                                                                                                  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |
| Reset 0x00000000 |            |            | 0     | 0                                                                                                                | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |  |  |
| ID               | Acce Field | Value ID   | Value |                                                                                                                  | Description  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |
| A                | W          | TASKS_STOP |       | Stops I2S transfer. Also stops MCK generator. Triggering this task will cause the event STOPPED to be generated. |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |
|                  |            | Trigger    | 1     |                                                                                                                  | Trigger task |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |

### 7.1.16.10.3 SUBSCRIBE\_START

Address offset: 0x080

Subscribe configuration for task **START**

|                  |            |          |          |    |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|----|--------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          | 31       | 30 | 29                                               | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |          | B        |    |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |          | 0        |    |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID | Value    |    | Description                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | CHIDX    | [255..0] |    | Channel that task <b>START</b> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW         | EN       |          |    |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        |    | Disable subscription                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        |    | Enable subscription                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.16.10.4 SUBSCRIBE\_STOP

Address offset: 0x084



| Bit number       |            |                 | 31    | 30                                                                                                                                                                                                           | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
|------------------|------------|-----------------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| ID               |            |                 |       |                                                                                                                                                                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |
| Reset 0x00000000 |            |                 | 0     | 0                                                                                                                                                                                                            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |
| ID               | Acce Field | Value ID        | Value | Description                                                                                                                                                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | EVENTS_TXPTRUPD |       | The TDX.PTR register has been copied to internal double-buffers. When the I2S module is started and TX is enabled, this event will be generated for every RXTXD.MAXCNT words that are sent on the SDOUT pin. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | NotGenerated    | 0     | Event not generated                                                                                                                                                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Generated       | 1     | Event generated                                                                                                                                                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.16.10.8 EVENTS\_FRAMESTART

Address offset: 0x11C

Frame start event, generated on the active edge of LRCK

|                  |            |                   |       |                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|------------------|------------|-------------------|-------|---------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|---|
| Bit number       |            |                   |       | 31                                                      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |   |
| ID               |            |                   |       |                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  | A |
| Reset 0x00000000 |            |                   |       | 0                                                       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |   |
| ID               | Acce Field | Value ID          | Value | Description                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
| A                | RW         | EVENTS_FRAMESTART |       | Frame start event, generated on the active edge of LRCK |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|                  |            | NotGenerated      | 0     | Event not generated                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|                  |            | Generated         | 1     | Event generated                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |

### 7.1.16.10.9 PUBLISH\_RXPTRUPD

Address offset: 0x184

Publish configuration for event RXPTRUPD

|                  |            |  |  |          |  |  |          |  |  |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|--|----------|--|--|----------|--|--|-----------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |  |          |  |  |          |  |  | 31                                                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |
| ID               |            |  |  |          |  |  |          |  |  | B                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  |    |    |    |   |   |   |   |   |   | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |  |          |  |  |          |  |  | 0                                                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |
| ID               | Acce Field |  |  | Value ID |  |  | Value    |  |  | Description                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |  |          |  |  | [255..0] |  |  | Channel that event <b>RXPTRUPD</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |  |          |  |  |          |  |  |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  |  | Disabled |  |  | 0        |  |  | Disable publishing                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  |  | Enabled  |  |  | 1        |  |  | Enable publishing                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.16.10.10 PUBLISH\_STOPPED

Address offset: 0x188

Publish configuration for event STOPPED

|                  |            |  |  |          |    |       |    |                                             |    |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|--|----------|----|-------|----|---------------------------------------------|----|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |  | 31       | 30 | 29    | 28 | 27                                          | 26 | 25                 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |  |  | B        |    |       |    |                                             |    |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   |   |   |   |   |   |   |   | A | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |  | 0        |    |       |    |                                             |    |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  |  | Value ID |    | Value |    |                                             |    | Description        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |  | [255..0] |    |       |    | Channel that event STOPPED will publish to. |    |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |  |          |    |       |    |                                             |    |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  |  | Disabled |    | 0     |    |                                             |    | Disable publishing |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  |  | Enabled  |    | 1     |    |                                             |    | Enable publishing  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.16.10.11 PUBLISH\_TXPTRUPD

Address offset: 0x194

Publish configuration for event **TXPTRUPD**

|                  |            |          |                                                                                       |  |                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|--|-----------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |          | B                                                                                     |  |                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |  |                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 |  | Description                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                              |  | Channel that event <b>TXPTRUPD</b> will publish to. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |                                                                                       |  |                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     |  | Disable publishing                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     |  | Enable publishing                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

### 7.1.16.10.12 PUBLISH\_FRAMESTART

Address offset: 0x19C

Publish configuration for event **FRAMESTART**

|                  |            |          |                                                                                       |                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|-------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |          | B                                                                                     |                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0           |                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                              | Channel that event <b>FRAMESTART</b> will publish to. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |                                                                                       |                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Disable publishing                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Enable publishing                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

### 7.1.16.10.13 INTEN

Address offset: 0x300

Enable or disable interrupt

| Bit number       |            |            | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |   |  |   |  |   |  |
|------------------|------------|------------|---------------------------------------------------------------------------------------|------------------------------------------------------------------|-------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|--|---|--|---|--|---|--|
| ID               |            |            |                                                                                       |                                                                  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | H |  | F |  | C |  | B |  |
| Reset 0x00000000 |            |            | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |   |  |   |  |   |  |
| ID               | Acce Field | Value ID   | Value                                                                                 |                                                                  | Description |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |   |  |   |  |   |  |
| B                | RW         | RXPTRUPD   |                                                                                       | Enable or disable interrupt for event <a href="#">RXPTRUPD</a>   |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |   |  |   |  |   |  |
|                  |            | Disabled   | 0                                                                                     | Disable                                                          |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |   |  |   |  |   |  |
|                  |            | Enabled    | 1                                                                                     | Enable                                                           |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |   |  |   |  |   |  |
| C                | RW         | STOPPED    |                                                                                       | Enable or disable interrupt for event <a href="#">STOPPED</a>    |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |   |  |   |  |   |  |
|                  |            | Disabled   | 0                                                                                     | Disable                                                          |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |   |  |   |  |   |  |
|                  |            | Enabled    | 1                                                                                     | Enable                                                           |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |   |  |   |  |   |  |
| F                | RW         | TXPTRUPD   |                                                                                       | Enable or disable interrupt for event <a href="#">TXPTRUPD</a>   |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |   |  |   |  |   |  |
|                  |            | Disabled   | 0                                                                                     | Disable                                                          |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |   |  |   |  |   |  |
|                  |            | Enabled    | 1                                                                                     | Enable                                                           |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |   |  |   |  |   |  |
| H                | RW         | FRAMESTART |                                                                                       | Enable or disable interrupt for event <a href="#">FRAMESTART</a> |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |   |  |   |  |   |  |
|                  |            | Disabled   | 0                                                                                     | Disable                                                          |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |   |  |   |  |   |  |
|                  |            | Enabled    | 1                                                                                     | Enable                                                           |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |   |  |   |  |   |  |

### 7.1.16.10.14 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number       |               |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |  |  |  |  |
|------------------|---------------|----------|---------------------------------------------------------------------------------------|--------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|---|---|---|--|--|--|--|
| ID               |               |          |                                                                                       |                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | H | F | C | B |  |  |  |  |
| Reset 0x00000000 |               |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |  |  |  |  |
| ID               | Acce Field    | Value ID | Value                                                                                 | Description                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |  |  |  |  |
| B                | RW RXPTRUPD   |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">RXPTRUPD</a>   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |  |  |  |  |
|                  |               | Set      | 1                                                                                     | Enable                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |  |  |  |  |
|                  |               | Disabled | 0                                                                                     | Read: Disabled                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |  |  |  |  |
|                  |               | Enabled  | 1                                                                                     | Read: Enabled                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |  |  |  |  |
| C                | RW STOPPED    |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">STOPPED</a>    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |  |  |  |  |
|                  |               | Set      | 1                                                                                     | Enable                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |  |  |  |  |
|                  |               | Disabled | 0                                                                                     | Read: Disabled                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |  |  |  |  |
|                  |               | Enabled  | 1                                                                                     | Read: Enabled                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |  |  |  |  |
| F                | RW TXPTRUPD   |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">TXPTRUPD</a>   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |  |  |  |  |
|                  |               | Set      | 1                                                                                     | Enable                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |  |  |  |  |
|                  |               | Disabled | 0                                                                                     | Read: Disabled                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |  |  |  |  |
|                  |               | Enabled  | 1                                                                                     | Read: Enabled                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |  |  |  |  |
| H                | RW FRAMESTART |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">FRAMESTART</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |  |  |  |  |
|                  |               | Set      | 1                                                                                     | Enable                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |  |  |  |  |
|                  |               | Disabled | 0                                                                                     | Read: Disabled                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |  |  |  |  |
|                  |               | Enabled  | 1                                                                                     | Read: Enabled                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |  |  |  |  |

### 7.1.16.10.15 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number       |      |            | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |
|------------------|------|------------|---------------------------------------------------------------------------------------|-------|---------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|---|---|---|
| ID               |      |            |                                                                                       |       |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | H | F | C | B |
| Reset 0x00000000 |      |            | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |       |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |
| ID               | Acce | Field      | Value ID                                                                              | Value | Description                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |
| B                | RW   | RXPTRUPD   |                                                                                       |       | Write '1' to disable interrupt for event <a href="#">RXPTRUPD</a>   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |
|                  |      |            | Clear                                                                                 | 1     | Disable                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |
|                  |      |            | Disabled                                                                              | 0     | Read: Disabled                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |
|                  |      |            | Enabled                                                                               | 1     | Read: Enabled                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |
| C                | RW   | STOPPED    |                                                                                       |       | Write '1' to disable interrupt for event <a href="#">STOPPED</a>    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |
|                  |      |            | Clear                                                                                 | 1     | Disable                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |
|                  |      |            | Disabled                                                                              | 0     | Read: Disabled                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |
|                  |      |            | Enabled                                                                               | 1     | Read: Enabled                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |
| F                | RW   | TXPTRUPD   |                                                                                       |       | Write '1' to disable interrupt for event <a href="#">TXPTRUPD</a>   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |
|                  |      |            | Clear                                                                                 | 1     | Disable                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |
|                  |      |            | Disabled                                                                              | 0     | Read: Disabled                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |
|                  |      |            | Enabled                                                                               | 1     | Read: Enabled                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |
| H                | RW   | FRAMESTART |                                                                                       |       | Write '1' to disable interrupt for event <a href="#">FRAMESTART</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |
|                  |      |            | Clear                                                                                 | 1     | Disable                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |
|                  |      |            | Disabled                                                                              | 0     | Read: Disabled                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |
|                  |      |            | Enabled                                                                               | 1     | Read: Enabled                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |



### 7.1.16.10.16 ENABLE

Address offset: 0x500

Enable I2S module

|                  |            |          |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW ENABLE  |          |       | Enable I2S module                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0     | Disable                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1     | Enable                                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.16.10.17 CONFIG.MODE

Address offset: 0x504

I2S mode

|                  |            |          |                                                                                       |                                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          | A                                                                                     |                                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |                                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW MODE    |          |                                                                                       | I2S mode                                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Master   | 0                                                                                     | Master mode. SCK and LRCK generated from internal master<br>clkck (MCK) and output on pins defined by PSEL.xxx. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Slave    | 1                                                                                     | Slave mode. SCK and LRCK generated by external master<br>and received on pins defined by PSEL.xxx               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.16.10.18 CONFIG.RXEN

Address offset: 0x508

Reception (RX) enable

|                  |            |          |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW RXEN    |          |       | Reception (RX) enable                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0     | Reception disabled and now data will be written to the RXD.PTR address.               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1     | Reception enabled.                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.16.10.19 CONFIG.TXEN

Address offset: 0x50C

Transmission (TX) enable

|                  |            |          |       |                                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|------------------|------------|----------|-------|------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|--|
| Bit number       |            |          | 31    | 30                                                                           | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |
| ID               |            |          | A     |                                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| Reset 0x00000001 |            |          | 0     | 0                                                                            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |  |  |  |  |
| ID               | Acce Field | Value ID | Value | Description                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| A                | RW         | TXEN     |       | Transmission (TX) enable                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | Disabled | 0     | Transmission disabled and now data will be read from the<br>RXD.TXD address. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | Enabled  | 1     | Transmission enabled.                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |

### 7.1.16.10.20 CONFIG.MCKEN

Address offset: 0x510

Master clock generator enable

|                  |            |          |          |    |                                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |
|------------------|------------|----------|----------|----|--------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|--|--|
| Bit number       |            |          | 31       | 30 | 29                                                                             | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |  |
| ID               |            |          | A        |    |                                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |
| Reset 0x00000001 |            |          | 0        | 0  | 0                                                                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value    |    | Description                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |
| A                | RW         | MCKEN    |          |    | Master clock generator enable                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |
|                  |            |          | Disabled | 0  | Master clock generator disabled and PSEL.MCK not connected(available as GPIO). |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |
|                  |            |          | Enabled  | 1  | Master clock generator running and MCK output on PSEL.MCK.                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |

### 7.1.16.10.21 CONFIG.MCKFREQ

Address offset: 0x514

I2S clock generator control

| Bit number       |            |                                   | 31       | 30         | 29                                                                                        | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |
|------------------|------------|-----------------------------------|----------|------------|-------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|--|
| ID               |            |                                   | A        | A          | A                                                                                         | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |  |  |  |  |
| Reset 0x20000000 |            |                                   | 0        | 0          | 1                                                                                         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |  |
| ID               | Acce       | Field                             | Value ID | Value      | Description                                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| A                | RW         | MCKFREQ                           |          |            | I2S MCK frequency configuration                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            |                                   |          |            | NOTE: Enumerations are deprecated, use MCKFREQ equation.                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            |                                   |          |            | NOTE: The 12 least significant bits of the register are ignored and shall be set to zero. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            |                                   | 32MDIV2  | 0x80000000 | 32 MHz / 2 = 16.0 MHz                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            |                                   |          |            | Deprecated, use MCKFREQ equation.                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            |                                   | 32MDIV3  | 0x50000000 | 32 MHz / 3 = 10.6666667 MHz                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            |                                   |          |            | Deprecated, use MCKFREQ equation.                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            |                                   | 32MDIV4  | 0x40000000 | 32 MHz / 4 = 8.0 MHz                                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            |                                   |          |            | Deprecated, use MCKFREQ equation.                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            |                                   | 32MDIV5  | 0x30000000 | 32 MHz / 5 = 6.4 MHz                                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            |                                   |          |            | Deprecated, use MCKFREQ equation.                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| 32MDIV6          | 0x28000000 | 32 MHz / 6 = 5.3333333 MHz        |          |            |                                                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | Deprecated, use MCKFREQ equation. |          |            |                                                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| 32MDIV8          | 0x20000000 | 32 MHz / 8 = 4.0 MHz              |          |            |                                                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | Deprecated, use MCKFREQ equation. |          |            |                                                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |

| Bit number       |            |           | 31         | 30 | 29 | 28                                | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |
|------------------|------------|-----------|------------|----|----|-----------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|--|
| ID               |            |           | A          | A  | A  | A                                 | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |  |  |  |  |
| Reset 0x20000000 |            |           | 0          | 0  | 1  | 0                                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |  |
| ID               | Acce Field | Value ID  | Value      |    |    | Description                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | 32MDIV10  | 0x18000000 |    |    | 32 MHz / 10 = 3.2 MHz             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            |           |            |    |    | Deprecated, use MCKFREQ equation. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | 32MDIV11  | 0x16000000 |    |    | 32 MHz / 11 = 2.9090909 MHz       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            |           |            |    |    | Deprecated, use MCKFREQ equation. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | 32MDIV15  | 0x11000000 |    |    | 32 MHz / 15 = 2.1333333 MHz       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            |           |            |    |    | Deprecated, use MCKFREQ equation. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | 32MDIV16  | 0x10000000 |    |    | 32 MHz / 16 = 2.0 MHz             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            |           |            |    |    | Deprecated, use MCKFREQ equation. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | 32MDIV21  | 0x0C000000 |    |    | 32 MHz / 21 = 1.5238095           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            |           |            |    |    | Deprecated, use MCKFREQ equation. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | 32MDIV23  | 0x0B000000 |    |    | 32 MHz / 23 = 1.3913043 MHz       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            |           |            |    |    | Deprecated, use MCKFREQ equation. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | 32MDIV30  | 0x08800000 |    |    | 32 MHz / 30 = 1.0666667 MHz       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            |           |            |    |    | Deprecated, use MCKFREQ equation. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | 32MDIV31  | 0x08400000 |    |    | 32 MHz / 31 = 1.0322581 MHz       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            |           |            |    |    | Deprecated, use MCKFREQ equation. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | 32MDIV32  | 0x08000000 |    |    | 32 MHz / 32 = 1.0 MHz             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            |           |            |    |    | Deprecated, use MCKFREQ equation. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | 32MDIV42  | 0x06000000 |    |    | 32 MHz / 42 = 0.7619048 MHz       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            |           |            |    |    | Deprecated, use MCKFREQ equation. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | 32MDIV63  | 0x04100000 |    |    | 32 MHz / 63 = 0.5079365 MHz       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            |           |            |    |    | Deprecated, use MCKFREQ equation. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | 32MDIV125 | 0x020C0000 |    |    | 32 MHz / 125 = 0.256 MHz          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            |           |            |    |    | Deprecated, use MCKFREQ equation. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |

### 7.1.16.10.22 CONFIG.RATIO

Address offset: 0x518

MCK / LRCK ratio

| Bit number       |            |          | 31    | 30               | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |
|------------------|------------|----------|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ID               |            |          |       |                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A | A | A | A |
| Reset 0x00000006 |            |          | 0     | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |   |   |   |
| ID               | Acce Field | Value ID | Value | Description      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | RATIO    |       | MCK / LRCK ratio |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | 32X      | 0     | LRCK = MCK / 32  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | 48X      | 1     | LRCK = MCK / 48  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | 64X      | 2     | LRCK = MCK / 64  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | 96X      | 3     | LRCK = MCK / 96  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | 128X     | 4     | LRCK = MCK / 128 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | 192X     | 5     | LRCK = MCK / 192 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | 256X     | 6     | LRCK = MCK / 256 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | 384X     | 7     | LRCK = MCK / 384 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | 512X     | 8     | LRCK = MCK / 512 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

Sample width

#### 7.1.16.10.24 CONFIG.ALIGN

## Alignment of sample within a frame

#### 7.1.16.10.25 CONFIG.FORMAT

## Frame format

#### 7.1.16.10.26 CONFIG.CHANNELS

## Enable channels

|                  |             |          |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|-------------|----------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |             |          |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |             |          |       | A A                                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |             |          |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field  | Value ID | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW CHANNELS |          |       | Enable channels                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |             | Stereo   | 0     | Stereo.                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |             | Left     | 1     | Left only.                                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |             | Right    | 2     | Right only.                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.16.10.27 CONFIG.CLKCONFIG

Address offset: 0x52C

Clock source selection for the I2S module

| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |            |          | B A                                                                                   |                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | CLKSRC   |                                                                                       | Clock source selection                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | PCLK32M  | 0                                                                                     | 32MHz peripheral clock                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | ACLK     | 1                                                                                     | Audio PLL clock                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW         | BYPASS   |                                                                                       | Bypass clock generator. MCK will be equal to source input. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |          |                                                                                       | If bypass is enabled the MCKFREQ setting has no effect.    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disable  | 0                                                                                     | Disable bypass                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enable   | 1                                                                                     | Enable bypass                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.16.10.28 RXD.PTR

Address offset: 0x538

Receive buffer RAM start address.

| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                                                                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |            |          | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A                   |                                                                                                                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                                                                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                                                                                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW PTR     |          |                                                                                       | Receive buffer Data RAM start address. When receiving, words containing samples will be written to this address.<br><br>This address is a word aligned Data RAM address. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**Note:** See the memory chapter for details about which memories are available for EasyDMA.

### 7.1.16.10.29 TXD.PTR

Address offset: 0x540

Transmit buffer RAM start address

|                  |            |  |          |       |    |                                                                                                                                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|------------------|------------|--|----------|-------|----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|
| Bit number       |            |  |          | 31    | 30 | 29                                                                                                                                                                             | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |
| ID               |            |  |          | A     | A  | A                                                                                                                                                                              | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |  |  |  |
| Reset 0x00000000 |            |  |          | 0     | 0  | 0                                                                                                                                                                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |
| ID               | Acce Field |  | Value ID | Value |    | Description                                                                                                                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
| A                | RW PTR     |  |          |       |    | Transmit buffer Data RAM start address. When transmitting, words containing samples will be fetched from this address.<br><br>This address is a word aligned Data RAM address. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |

**Note:** See the memory chapter for details about which memories are available for EasyDMA.

### 7.1.16.10.30 RXTXD.MAXCNT

Address offset: 0x550

Size of RXD and TXD buffers

|                  |            |  |          |       |    |    |    |                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|-------|----|----|----|-------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31    | 30 | 29 | 28 | 27                                                    | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |  |          |       |    |    |    |                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |          | 0     | 0  | 0  | 0  | 0                                                     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field |  | Value ID | Value |    |    |    | Description                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW MAXCNT  |  |          |       |    |    |    | Size of RXD and TXD buffers in number of 32 bit words |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.16.10.31 PSEL.MCK

Address offset: 0x560

Pin select for MCK signal

|                  |            |              |         |    |    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------------|---------|----|----|----|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |              | 31      | 30 | 29 | 28 | 27          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |              | C       |    |    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | B |   |   |   |   |   |   |   |   |   |   |   | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0xFFFFFFFF |            |              | 1       |    |    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ID               | Acce Field | Value ID     | Value   |    |    |    | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW PIN     |              | [0..31] |    |    |    | Pin number  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW PORT    |              | [0..1]  |    |    |    | Port number |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| C                | RW CONNECT |              |         |    |    |    | Connection  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disconnected | 1       |    |    |    | Disconnect  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Connected    | 0       |    |    |    | Connect     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.16.10.32 PSEL.SCK

Address offset: 0x564

Pin select for SCK signal

|                  |      |         |              |    |         |    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |
|------------------|------|---------|--------------|----|---------|----|----|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|--|
| Bit number       |      |         |              | 31 | 30      | 29 | 28 | 27          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |  |
| ID               |      |         |              | C  |         |    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | B |   |   |   |   | A | A | A | A | A |  |
| Reset 0xFFFFFFFF |      |         |              | 1  | 1       | 1  | 1  | 1           | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |   |   |  |
| ID               | Acce | Field   | Value        | ID | Value   |    |    | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |
| A                | RW   | PIN     |              |    | [0..31] |    |    | Pin number  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |
| B                | RW   | PORT    |              |    | [0..1]  |    |    | Port number |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |
| C                | RW   | CONNECT |              |    |         |    |    | Connection  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |         | Disconnected |    | 1       |    |    | Disconnect  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |         | Connected    |    | 0       |    |    | Connect     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |

## Pin select for LRCK signal

|                  |      |              |         |    |    |       |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------|--------------|---------|----|----|-------|----|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |      |              | 31      | 30 | 29 | 28    | 27 | 26          | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |      |              | C       |    |    |       |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Reset 0xFFFFFFFF |      |              | 1       |    |    |       |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce | Field        | Value   |    | ID | Value |    | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW   | PIN          | [0..31] |    |    |       |    | Pin number  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| B                | RW   | PORT         | [0..1]  |    |    |       |    | Port number |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| C                | RW   | CONNECT      |         |    |    |       |    | Connection  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      | Disconnected | 1       |    |    |       |    | Disconnect  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      | Connected    | 0       |    |    |       |    | Connect     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

Address offset: 0x56C

### Pin select for SDIN signal

|                  |      |              |            |             |       |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------|--------------|------------|-------------|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |      |              |            | 31          | 30    | 29          | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |
| ID               |      |              |            | C           |       |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | B |   |   |   | A | A | A | A | A |
| Reset 0xFFFFFFFF |      |              |            | 1           | 1     | 1           | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |   |   |   |   |   |
| ID               | Acce | Field        | Value      | ID          | Value | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW   | PIN          | [0..31]    | Pin number  |       |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW   | PORT         | [0..1]     | Port number |       |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| C                | RW   | CONNECT      | Connection |             |       |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      | Disconnected | 1          | Disconnect  |       |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      | Connected    | 0          | Connect     |       |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

Address offset: 0x570

### Pin select for SDOUT signal

|                 |      |              |       |    |         |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|-----------------|------|--------------|-------|----|---------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|
| Bit number      |      |              |       | 31 | 30      | 29          | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |
| ID              |      |              |       | C  |         |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | B |   |   |   | A | A | A | A | A |  |  |
| Reset 0xFFFFFFF |      |              |       | 1  | 1       | 1           | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |   |  |  |
| ID              | Acce | Field        | Value | ID | Value   | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
| A               | RW   | PIN          |       |    | [0..31] | Pin number  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
| B               | RW   | PORT         |       |    | [0..1]  | Port number |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
| C               | RW   | CONNECT      |       |    |         | Connection  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                 |      | Disconnected | 1     |    |         | Disconnect  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                 |      | Connected    | 0     |    |         | Connect     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |

## 7.1.16.11 Electrical specification

### 7.1.16.11.1 I2S timing specification

| Symbol          | Description                        | Min. | Typ. | Max. | Units |
|-----------------|------------------------------------|------|------|------|-------|
| $t_{S\_SDIN}$   | SDIN setup time before SCK rising  | ..   | ..   | ..   | ns    |
| $t_{H\_SDIN}$   | SDIN hold time after SCK rising    | ..   | ..   | ..   | ns    |
| $t_{S\_SDOUT}$  | SDOUT setup time after SCK falling | ..   | ..   | ..   | ns    |
| $t_{H\_SDOUT}$  | SDOUT hold time before SCK falling | ..   | ..   | ..   | ns    |
| $t_{SCK\_LRCK}$ | SCLK falling to LRCK edge          | ..   | ..   | ..   | ns    |
| $f_{MCK}$       | MCK frequency                      | ..   | ..   | ..   | kHz   |
| $f_{LRCK}$      | LRCK frequency                     | ..   | ..   | ..   | kHz   |
| $f_{SCK}$       | SCK frequency                      | ..   | ..   | ..   | kHz   |
| $DC_{CK}$       | Clock duty cycle (MCK, LRCK, SCK)  | ..   | ..   | ..   | %     |

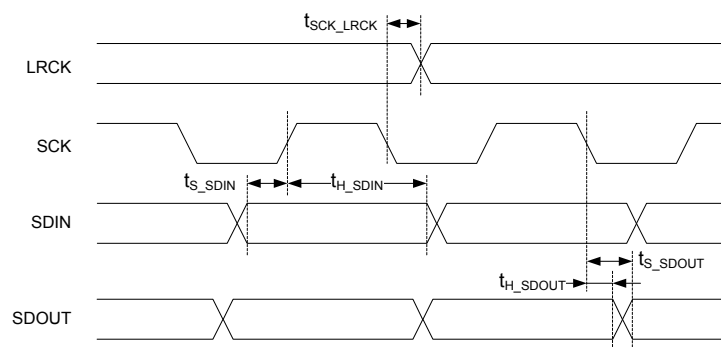


Figure 77: I2S timing diagram

## 7.1.17 IPC — Interprocessor communication

The interprocessor communication (IPC) peripheral is used to send and receive events between MCUs in the system.



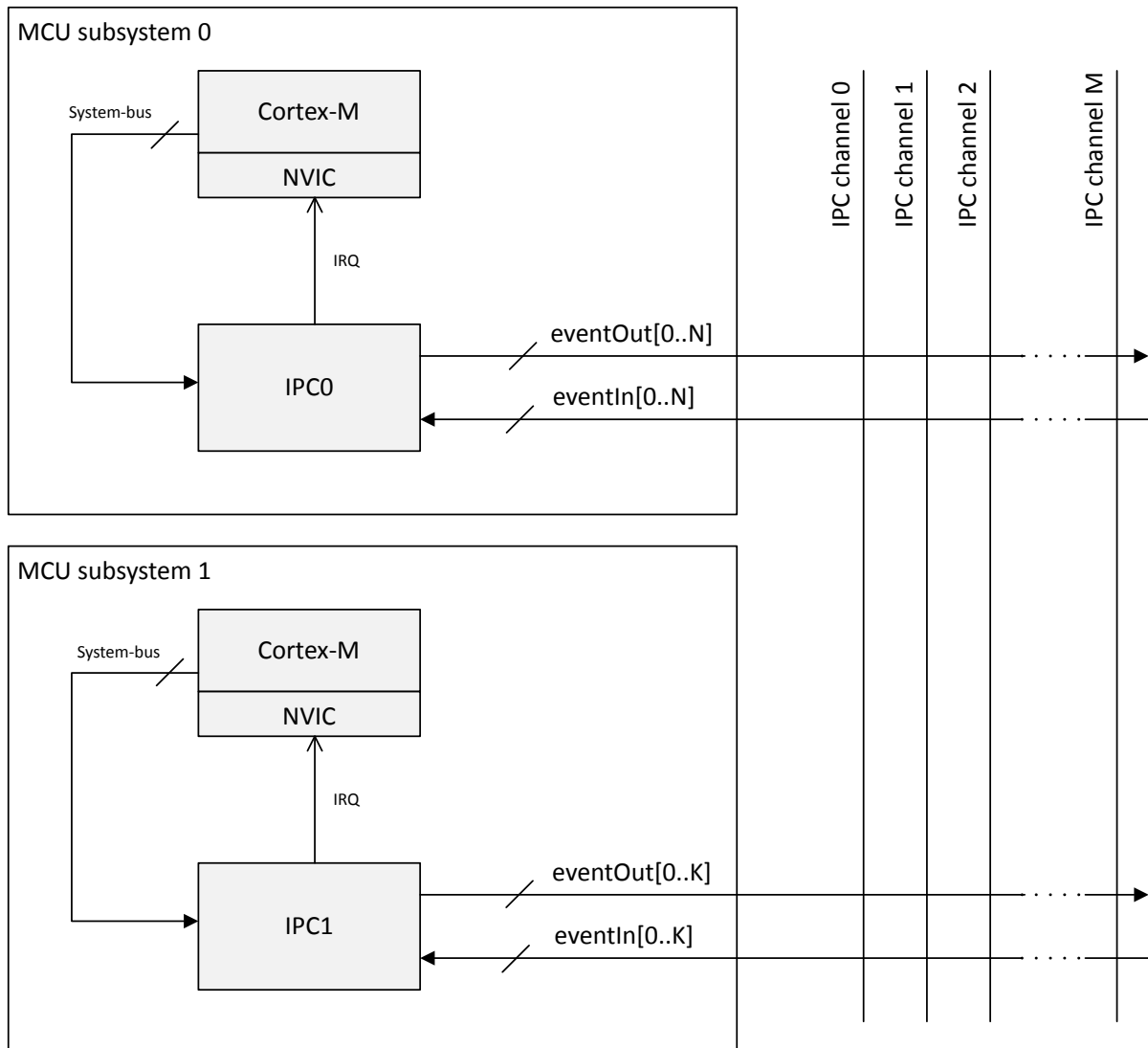


Figure 78: IPC block diagram

## Functional description

Figure 78: IPC block diagram on page 253 illustrates the interprocessor communication (IPC) peripheral. In a multi-MCU system, each MCU has one dedicated IPC peripheral. The IPC peripheral can be used to send and receive events to and from other IPC peripherals. An instance of the IPC peripheral can have multiple SEND tasks and RECEIVE events. A single SEND task can be configured to signal an event on one or more IPC channels, and a RECEIVE event can be configured to listen on one or more IPC channels. The IPC channels that are triggered in a SEND task can be configured through the `SEND_CNF` registers, and the IPC channels that trigger a RECEIVE event are configured through the `RECEIVE_CNF` registers. The figure below illustrates how the `SEND_CNF` and `RECEIVE_CNF` registers work. Both the SEND task and the RECEIVE event can be connected to all IPC channels.

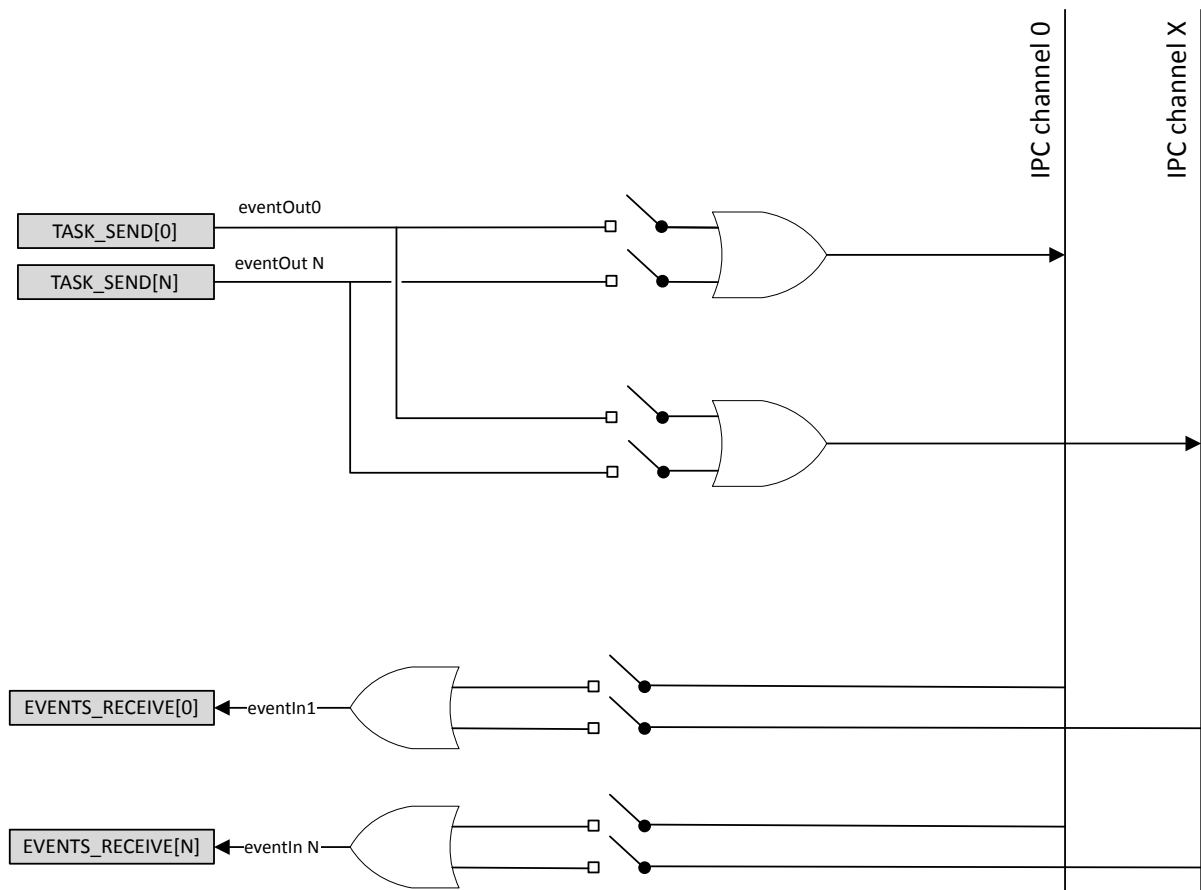


Figure 79: IPC registers *SEND\_CNF* and *RECEIVE\_CNF*

A SEND task can be viewed as broadcasting events onto one or more IPC channels, and a RECEIVE event can be seen as subscribing to a subset of IPC channels. It is possible for multiple IPCs to trigger events onto the same channel at the same time. When two or more events on the same channel occur within  $t_{IPC}$ , the events may be merged into a single event seen from the IPC receiver. One of the events can therefore be lost. To prevent this, the user must ensure that events on the same IPC channel do not occur within  $t_{IPC}$  of each other. When implementing firmware data structures, such as queues or mailboxes, this can be done by using one channel for acknowledgements.

An IPC event often does not contain any data itself, it is used to signal other MCUs that something has occurred. Data can be shared through shared memory, for example in the form of a software implemented mailbox, or command/event queues. It is up to software to assign a logical functionality to an IPC channel. For instance, one IPC channel can be used to signal that a command is ready to be executed, and any processor in the system can subscribe to that particular channel and decode/execute the command.

## General purpose memory

The **GP**MEM registers can be used freely to store information. These registers are accessed like any other of the IPC peripheral's registers.

### 7.1.17.1 IPC and PPI connections

The IPC SEND tasks and RECEIVE events can be connected through PPI channels. This makes it possible to relay events from peripherals in one MCU to another, without CPU involvement.

Figure below illustrates a timer COMPARE event that is relayed from one MCU to IPC using PPI, then back into a timer CAPTURE event in another MCU.

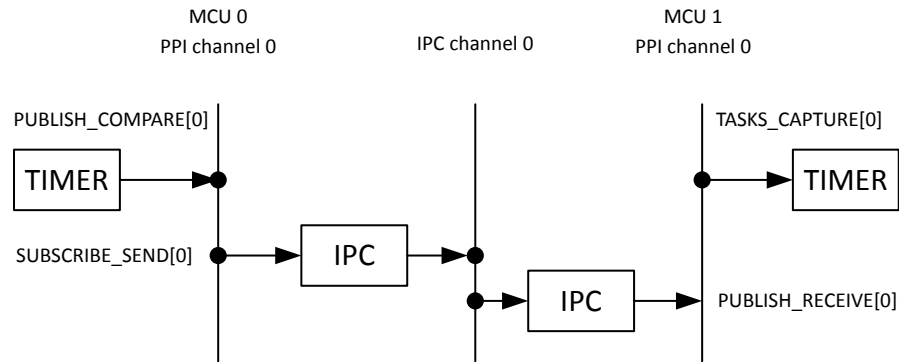


Figure 80: Example of PPI and IPC connections

### 7.1.17.2 Registers

| Base address | Domain      | Peripheral | Instance | Secure mapping | DMA security | Description                  | Configuration |
|--------------|-------------|------------|----------|----------------|--------------|------------------------------|---------------|
| 0x5002A000   | APPLICATION | IPC        | IPC : S  | US             | NA           | Interprocessor communication |               |
| 0x4002A000   |             |            | IPC : NS |                |              |                              |               |
| 0x41012000   | NETWORK     | IPC        | IPC      | NS             | NA           | Interprocessor communication |               |

Table 89: Instances

| Register           | Offset | Security | Description                                                                 |
|--------------------|--------|----------|-----------------------------------------------------------------------------|
| TASKS_SEND[n]      | 0x000  |          | Trigger events on IPC channel enabled in SEND_CNF[n]                        |
| SUBSCRIBE_SEND[n]  | 0x080  |          | Subscribe configuration for task SEND[n]                                    |
| EVENTS_RECEIVE[n]  | 0x100  |          | Event received on one or more of the enabled IPC channels in RECEIVE_CNF[n] |
| PUBLISH_RECEIVE[n] | 0x180  |          | Publish configuration for event RECEIVE[n]                                  |
| INTEN              | 0x300  |          | Enable or disable interrupt                                                 |
| INTENSET           | 0x304  |          | Enable interrupt                                                            |
| INTENCLR           | 0x308  |          | Disable interrupt                                                           |
| INTPEND            | 0x30C  |          | Pending interrupts                                                          |
| SEND_CNF[n]        | 0x510  |          | Send event configuration for TASKS_SEND[n]                                  |
| RECEIVE_CNF[n]     | 0x590  |          | Receive event configuration for EVENTS_RECEIVE[n]                           |
| GPMEM[n]           | 0x610  |          | General purpose memory                                                      |

Table 90: Register overview

#### 7.1.17.2.1 TASKS\_SEND[n] (n=0..15)

Address offset: 0x000 + (n × 0x4)

Trigger events on IPC channel enabled in SEND\_CNF[n]

|                  |            |            |          |                                                                                       |  |  |  |                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|------------|----------|---------------------------------------------------------------------------------------|--|--|--|------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |            |          | A                                                                                     |  |  |  |                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |  |  |  |                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field |            | Value ID | Value                                                                                 |  |  |  | Description                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W          | TASKS_SEND |          |                                                                                       |  |  |  | Trigger events on IPC channel enabled in SEND_CNF[n] |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |            | Trigger  | 1                                                                                     |  |  |  | Trigger task                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.17.2.2 SUBSCRIBE\_SEND[n] (n=0..15)

Address offset:  $0x080 + (n \times 0x4)$

Subscribe configuration for task `SEND[n]`

|                  |            |          |                                                                                       |                      |                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|----------------------|----------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                      |                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |          | B                                                                                     |                      |                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |                      |                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 |                      | Description                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                              |                      | Channel that task <span>SEND[n]</span> will subscribe to |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |                                                                                       |                      |                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Disable subscription |                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Enable subscription  |                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

### 7.1.17.2.3 EVENTS\_RECEIVE[n] (n=0..15)

Address offset:  $0x100 + (n \times 0x4)$

Event received on one or more of the enabled IPC channels in `RECEIVE_CNF[n]`

|                  |                   |              |                                                                                       |                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|-------------------|--------------|---------------------------------------------------------------------------------------|-----------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |                   |              | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |                   |              | A                                                                                     |                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |                   |              | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field        | Value ID     | Value                                                                                 | Description                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW EVENTS_RECEIVE |              |                                                                                       | Event received on one or more of the enabled IPC channels in RECEIVE_CNF[n] |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                   | NotGenerated | 0                                                                                     | Event not generated                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                   | Generated    | 1                                                                                     | Event generated                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.17.2.4 PUBLISH\_RECEIVE[n] (n=0..15)

Address offset:  $0x180 + (n \times 0x4)$

Publish configuration for event `RECEIVE[n]`

|                  |            |          |                                                                                       |  |  |  |                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|--|--|--|-------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |          | B                                                                                     |  |  |  |                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |  |  |  |                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 |  |  |  | Description                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                              |  |  |  | Channel that event <span>RECEIVE[n]</span> will publish to. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |                                                                                       |  |  |  |                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     |  |  |  | Disable publishing                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     |  |  |  | Enable publishing                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

### 7.1.17.2.5 INTEN

Address offset:  $0x300$

Enable or disable interrupt

|                  |      |                      |          |                                                                                       |         |                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------|----------------------|----------|---------------------------------------------------------------------------------------|---------|------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |      |                      |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |         |                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |      |                      |          |                                                                                       |         |                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  | P | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| Reset 0x00000000 |      |                      |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |         |                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce | Field                | Value    | ID                                                                                    | Value   | Description                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A-P              | RW   | RECEIVE[i] (i=0..15) |          |                                                                                       |         | Enable or disable interrupt for event <a href="#">RECEIVE[i]</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |                      | Disabled | 0                                                                                     | Disable |                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |                      | Enabled  | 1                                                                                     | Enable  |                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.17.2.6 INTENSET

Address offset: 0x304

## Enable interrupt

|                  |            |                      |          |   |                |                                                                    |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------------------|----------|---|----------------|--------------------------------------------------------------------|-------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                      |          |   |                |                                                                    |             |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |                      |          |   |                |                                                                    |             |  |  |    |    |    |    |    |    |    |    |    |    | P  | O  | N  | M  | L  | K  | J  | I  | H  | G  | F  | E  | D | C | B | A |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |                      |          |   |                |                                                                    |             |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |                      | Value ID |   | Value          |                                                                    | Description |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A-P              | RW         | RECEIVE[i] (i=0..15) |          |   |                | Write '1' to enable interrupt for event <a href="#">RECEIVE[i]</a> |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |                      | Set      | 1 | Enable         |                                                                    |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |                      | Disabled | 0 | Read: Disabled |                                                                    |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |                      | Enabled  | 1 | Read: Enabled  |                                                                    |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.17.2.7 INTENCLR

Address offset: 0x308

## Disable interrupt

|                  |      |                      |       |                                                                                       |       |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|----------------------|-------|---------------------------------------------------------------------------------------|-------|---------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |                      |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |                      |       | P O N M L K J I H G F E D C B A                                                       |       |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |                      |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                   |       |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field                | Value | ID                                                                                    | Value | Description                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A-P              | RW   | RECEIVE[i] (i=0..15) |       |                                                                                       |       | Write '1' to disable interrupt for event <a href="#">RECEIVE[i]</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Clear                | 1     |                                                                                       |       | Disable                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Disabled             | 0     |                                                                                       |       | Read: Disabled                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Enabled              | 1     |                                                                                       |       | Read: Enabled                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

#### 7.1.17.2.8 INTPEND

Address offset: 0x30C

## Pending interrupts

|                  |      |                      |            |    |                   |                                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------|----------------------|------------|----|-------------------|-----------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |      |                      |            |    | 31                | 30                                                                    | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |      |                      |            |    |                   |                                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    | P  | O  | N  | M  | L  | K  | J | I | H | G | F | E | D | C | B | A |
| Reset 0x00000000 |      |                      |            |    | 0                 | 0                                                                     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce | Field                | Value      | ID | Value             | Description                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A-P              | R    | RECEIVE[i] (i=0..15) |            |    |                   | Read pending status of interrupt for event <a href="#">RECEIVE[i]</a> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |                      | NotPending | 0  | Read: Not pending |                                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |                      | Pending    | 1  | Read: Pending     |                                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 7.1.17.2.9 SEND CNF[n] (n=0..15)

Address offset:  $0x510 + (n \times 0x4)$

## Send event configuration for TASKS\_SEND[n]

|                  |                      |          |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|----------------------|----------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |                      |          |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |                      |          |       | P O N M L K J I H G F E D C B A                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |                      |          |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field           | Value ID | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A-P              | RW CHEN[i] (i=0..15) |          |       | Enable broadcasting on IPC channel i                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                      | Disable  | 0     | Disable broadcast                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                      | Enable   | 1     | Enable broadcast                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

## 7.1.17.2.10 RECEIVE\_CNF[n] (n=0..15)

Address offset: 0x590 + (n × 0x4)

Receive event configuration for EVENTS\_RECEIVE[n]

|                  |                      |          |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|----------------------|----------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |                      |          |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |                      |          |       | P O N M L K J I H G F E D C B A                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |                      |          |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field           | Value ID | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A-P              | RW CHEN[i] (i=0..15) |          |       | Enable subscription to IPC channel i                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                      | Disable  | 0     | Disable events                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                      | Enable   | 1     | Enable events                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

## 7.1.17.2.11 GPMEM[n] (n=0..1)

Address offset: 0x610 + (n × 0x4)

General purpose memory

Retained only in System ON mode

| Bit number       |             |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|-------------|----------|---------------------------------------------------------------------------------------|--|--|--|------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |             |          | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A                   |  |  |  |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |             |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |  |  |  |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acces Field | Value ID | Value                                                                                 |  |  |  | Description            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW          | GPMEM    |                                                                                       |  |  |  | General purpose memory |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

## 7.1.17.3 Electrical specification

## 7.1.17.3.1 IPC Electrical Specification

| Symbol           | Description                                        | Min. | Typ. | Max. | Units |
|------------------|----------------------------------------------------|------|------|------|-------|
| t <sub>IPC</sub> | Minimum IPC event spacing before events are merged | ..   | ..   | ..   | µs    |

## 7.1.18 KMU — Key management unit

The key management unit (KMU) enforces access policies to a subset region of user information configuration register (UICR). This subset region is used for storing cryptographic key values inside the key slots, which the CPU has no access to.

In total there are 128 key slots available, where each key slot can store one 128-bit key value together with an access policy and a destination address for the key value. Multiple key slots can be combined in order

to support key sizes larger than 128 bits. The access policy of a key slot governs if and how a key value can be used, while the destination address determines where in the memory map the KMU pushes the key value upon a request from the CPU.

Key slots can be configured to be pushed directly into write-only key registers in cryptographic accelerators, like e.g. CryptoCell, without exposing the key value itself to the CPU. This enables the CPU to use the key values stored inside the key slots for cryptographic operations without being exposed to the key value.

Access to the KMU, and the key slots in the UICR, is only allowed from secure mode.

### 7.1.18.1 Functional view

From a functional view the UICR is divided into two different regions, one-time programmable (OTP) memory and key storage.

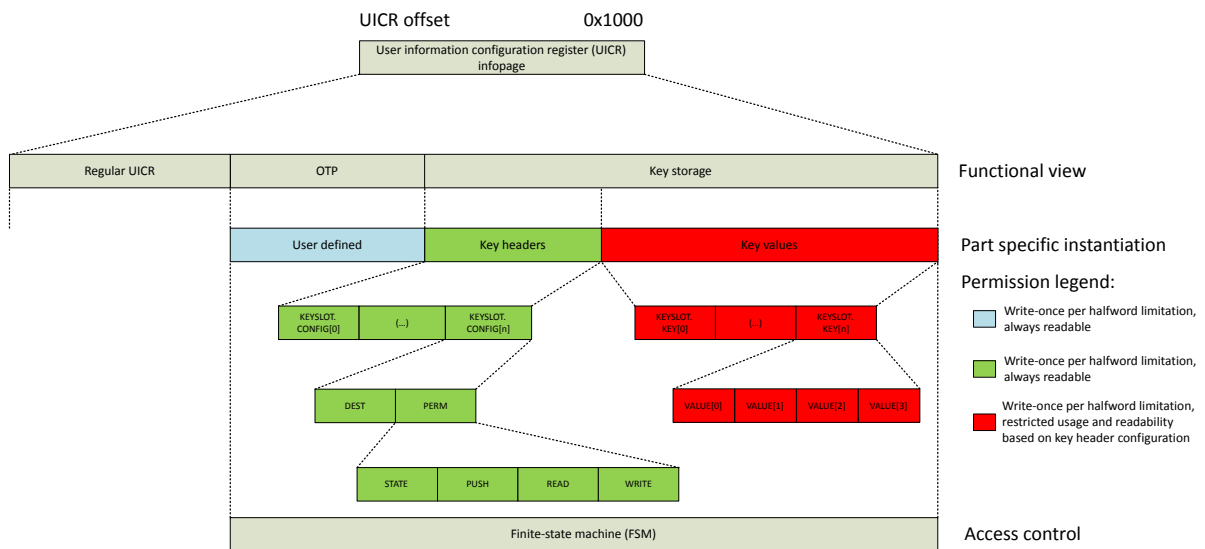


Figure 81: Memory map overview

## OTP

One-time programmable (OTP) memory is typically used for holding values that are written once, and then never to be changed again throughout the product lifetime. The OTP region of UICR is emulated by placing a write-once per halfword limitation on registers defined here.

## Key storage

The key storage region contains multiple key slots, where each slot consists of a key header and an associated key value. The key value is limited to 128 bits. Any key size greater than 128 bits must be divided and distributed over multiple key slot instances.

Key headers are allocated an address range of 0x400 in the UICR memory map, allowing a total of 128 keys to be addressable inside the key storage region.

**Note:** The use of the key storage region in UICR should be limited to keys with a certain life span, and not per-session derived keys where the CPU is involved in the key exchange.

### 7.1.18.2 Access control

Access control to the underlying UICR infopage in flash is enforced by a hardware finite-state machine (FSM). The FSM can allow or block transactions, depending both on the security of the transaction (secure or non-secure) and on the type of register being written and/or read.

| Access type | Key headers | Key values |
|-------------|-------------|------------|
| Read        | Allowed     | Restricted |
| Write       | Restricted  | Restricted |

Table 91: Access control

Any restricted access requires an explicit key slot selection through the KMU register interface. Any illegal access to restricted key slot registers will be blocked and word `0xDEADDEAD` will be returned on the AHB.

The OTP region has individual access control behavior, while access control to the key storage region is configured on a per key slot basis. The KMU FSM operates on only one key slot instance at a time, and the permissions and the usage restriction for a key value associated with a key slot can be configured individually.

**Note:** Even if the KMU can be configured as non-secure, all non-secure transactions will be blocked.

### 7.1.18.3 Protecting the UICR content

The UICR content can be protected against device-internal NVMC.ERASEALL requests, in addition to device-external ERASEALL requests, through the CTRL-AP interface. This feature is useful if the firmware designers want to prevent the OTP region from being erased.

Since enabling this step will permanently disable erase for the UICR, the procedure requires an implementation defined 32-bit word to be written into the UICR's ERASEPROTECT register.

In case of a field return handling, it is still possible to erase the UICR even if the ERASEPROTECT is set. If this functionality is desired, the secure boot code must implement a secure communication channel over the CTRL-AP mailbox interface. Upon successful authentication of the external party, the secure boot code can temporarily re-enable the CTRL-AP ERASEALL functionality.

### 7.1.18.4 Usage

This section describes the specific KMU and UICR behavior in more detail, to help the reader get a better overview of KMU's features and the intended usage.

#### 7.1.18.4.1 OTP

The OTP region of the UICR contains a user-defined static configuration of the device. The KMU emulates the OTP functionality by placing a write-once per halfword limitation of registers defined in this region, i.e. only halfwords containing all '1's can be written.

An OTP write transaction must consist of a full 32-bit word. Both halfwords can either be written simultaneously or one at a time. The KMU FSM will block any write to a halfword in the OTP region, if the initial value of this halfword is not `0xFFFF`. When writing halfwords one at a time, the non-active halfword must be masked as `0xFFFF`, otherwise the request will be blocked. For example, writing `0x1234XXXX` to an OTP destination address which already contains the value `0xFFFFAABB`, must be configured as `0x1234FFFF`. The OTP destination address will contain the value `0x1234AABB` after both write transactions have been processed.

The KMU will also only allow secure AHB write transactions into the OTP region of the UICR. Any AHB write transaction to this region that does not satisfy the above requirements will be ignored, and the `STATUS.BLOCKED` register will be set to '1'.

#### 7.1.18.4.2 Key storage

The key storage region of the UICR can contain multiple keys of different type, including symmetrical keys, hashes, public/private key pairs and other device secrets. One of the key features of the KMU, is that these



device secrets can be installed and made available for use in cryptographic operations without revealing the actual secret values.

Keys in this region will typically have a certain life span. The region is not designed to be used for per-session derived keys where the non-secure side (i.e. application) is participating in the key exchange.

All key storage is done through the concept of multiple key slots, where each key slot instance consists of one key header and an associated key value. Each key header supports the configuration of usage permissions and an optional secure destination address.

The key header secure destination address option enables the KMU to push the associated key value over a dedicated secure APB to a pre-configured secure location within the memory map. Such locations typically include a write-only key register of the hardware cryptographic accelerator, allowing the KMU to distribute keys within the system without compromising the key values.

One key slot instance can store a key value of maximum 128 bits. If a key size exceeds this limit, the key value itself must be split over multiple key slot instances.

The following usage and read permissions scheme is applicable for each key slot:

| State          | Push            | Read            | Write           | Description                                                                                                                       |
|----------------|-----------------|-----------------|-----------------|-----------------------------------------------------------------------------------------------------------------------------------|
| Active (1)     | Enabled<br>(1)  | Enabled<br>(1)  | Enabled<br>(1)  | Default flash erase value. Key slot cannot be pushed, write is enabled.                                                           |
| Active (1)     | Enabled<br>(1)  | Enabled<br>(1)  | Disabled<br>(0) | Key slot is active, push is enabled. Key slot VALUE registers can be read, but write is disabled.                                 |
| Active (1)     | Enabled<br>(1)  | Disabled<br>(0) | Disabled<br>(0) | Key slot is active, push is enabled. Read and write to key slot VALUE registers are disabled.                                     |
| Active (1)     | Disabled<br>(0) | Enabled<br>(1)  | Disabled<br>(0) | Key slot is active, push is disabled. Key slot VALUE registers can be read, but write is disabled.                                |
| Revoked<br>(0) | -               | -               | -               | Key slot is revoked and key value is set to zero. Cannot be read or pushed over secure APB regardless of the permission settings. |

Table 92: Valid key slot permission schemes

#### 7.1.18.4.2.1 Selecting a key slot

The KMU FSM is designed to process only one key slot at a time, effectively operating as a memory protection unit for the key storage region. Whenever a key slot is selected, the KMU will allow access to writing, reading, and/or pushing the associated key value according to the selected slot configuration.

A key slot must be selected prior to use, by writing the key slot ID into the KMU SELECTKEYSLOT register. Because the reset value of this register is 0x00000000, there is no key slot associated with ID=0 and no slot is selected by default. All key slots are addressed using IDs from 1 to 128.

SELECTED status is set when a key slot is selected, and a read or write access to that keyslot occurs.

BLOCKED status is set when any illegal access to key slot registers is detected.

When the use of the particular key slot is stopped, the key slot selection in SELECTKEYSLOT must be set back to '0'.

By default, all KMU key slots will consist of a 128-bit key value of '1's, where the key headers have no secure destination address, or any usage and read restrictions.

#### 7.1.18.4.2.2 Writing to a key slot

Writing a key slot into UICR is a five-step process.

1. Select which key slot the KMU shall operate on by writing the desired key slot ID into KMU->SELECTKEYSLOT. The selected key slot must be empty in order to add a new entry to UICR.
2. If the key value shall be pushable over secure APB, the destination address of the recipient must be configured in register KEYSLOT.CONFIG[ID-1].DEST.

3. Write the 128-bit key value into KEYSLOT.KEY[ID-1].VALUE[0-3].
4. Write the desired key slot permissions into KEYSLOT.CONFIG[ID-1].PERM, including any applicable usage restrictions.
5. Select key slot 0.

In case the total key size is greater than 128 bits, the key value itself must be split into 128-bit segments and written to multiple key slot instances. Steps 1 through 5 above must be repeated for the entire key size.

**Note:** If a key slot is configured as readable, and KEYSLOT.CONFIG[ID-1].DEST is not to be used, it is recommended to disable the push bit in KEYSLOT.CONFIG[ID-1].PERM when configuring key slot permissions.

**Note:** A key value distributed over multiple key slots should use the same key slot configuration in its key headers, but the secure destination address for each key slot instance must be incremented by 4 words (128 bits) for each key slot instance spanned.

**Note:** Write to flash must be enabled in NVMC->CONFIG prior to writing keys to flash, and subsequently disabled once writing is complete.

Steps 1 through 5 above will be blocked if any of the following violations are detected:

- No key slot selected
- Non-empty key slot selected
- NVM destination address not empty
- AHB write to KEYSLOT.KEY[ID-1].VALUE[0-3] registers not belonging to selected key slot

#### 7.1.18.4.2.3 Reading a key value

Key slots that are configured as readable can have their key value read directly from the UICR memory map by the CPU.

Readable keys are typically used during the secure boot sequence, where the CPU is involved in falsifying or verifying the integrity of the system. Since the CPU is involved in this decision process, it makes little sense not to trust the CPU having access to the actual key value but ultimately trust the decision of the integrity check. Another use-case for readable keys is if the key type in question does not have a HW peripheral in the platform that is able to accept such keys over secure APB.

Reading a key value from the UICR is a three-step process:

1. Select the key slot which the KMU shall operate on by writing the desired key slot ID into KMU->SELECTKEYSLOT.
2. If STATE and READ permission requirements are fulfilled as defined in KEYSLOT.CONFIG[ID-1].PERM, the key value can be read from region KEYSLOT.KEY[ID-1].VALUE[0-3] for selected key slot.
3. Select key slot 0.

Step 2 will be blocked and word 0xDEADDEAD will be returned on AHB if any of the following violations are detected:

- No key slot selected
- Key slot not configured as readable
- Key slot is revoked
- AHB read to KEYSLOT.KEY[ID-1].VALUE[0-3] registers not belonging to selected key slot

#### 7.1.18.4.2.4 Push over secure APB

Key slots that are configured as non-readable cannot be read by the CPU regardless of the mode the system is in, and must be pushed over secure APB in order to use the key value for cryptographic operations.

The secure APB destination address is set in the key slot configuration DEST register. Such destination addresses are typically write-only key registers in a hardware cryptographic accelerators memory map. The secure APB allows key slots to be utilized by the software side, without exposing the key value itself.

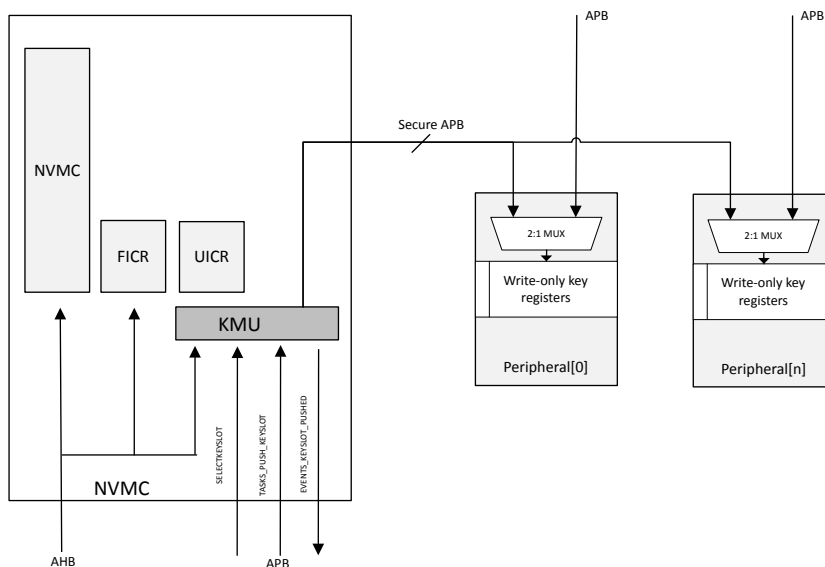


Figure 82: Tasks and events pattern for key slots

Pushing a key slot over secure APB is a four-step process:

1. Select the key slot on which the KMU shall operate by writing the desired key slot ID into KMU->SELECTKEYSLOT.
2. Start TASKS\_PUSH\_KEYSLLOT to initiate a secure APB transaction, writing the 128-bit key value associated with the selected key slot into address defined in KEYSLOT.CONFIG[ID-1].DEST.
3. After completing the secure APB transaction, the 128-bit key value is ready for use by the peripheral and EVENTS\_KEYSLLOT\_PUSHED is triggered.
4. Select key slot 0.

**Note:** If a key value is distributed over multiple key slots due to its key size, exceeding the maximum 128-bit key value limitation, then each distributed key slot must be pushed individually in order to transfer the entire key value over secure APB.

Step 3 will trigger other events than EVENTS\_KEYSLLOT\_PUSHED if the following violations are detected:

- EVENTS\_KEYSLLOT\_ERROR:
  - If no key slot is selected
  - If a key slot has no destination address configured
  - If when pushing a key slot, flash or peripheral returns an error
  - If pushing a key slot when push permissions are disabled
  - If attempting to push a key slot with default permissions
- EVENTS\_KEYSLLOT\_REVOKED if a key slot is marked as revoked in its key header configuration

#### 7.1.18.4.2.5 Revoking the key slots

All key slots within the key storage area can be marked as revoked.

To revoke any key slots, write to the STATE field in the KEYSLOT.CONFIG[ID-1].PERM register. The following rules apply to keys that have been revoked:

1. Key slots that have the PUSH field enabled in PERM register can no longer be pushed. If a revoked key slot is selected and task TASKS\_PUSH\_KEYSLLOT is started, the event EVENTS\_KEYSLLOT\_REVOKED is triggered.
2. Key slots that have the READ field enabled in PERM register can no longer be read. Any read operation to a revoked key value will return word 0xDEADDEAD.
3. Previously pushed key values stored in a peripheral write-only key register are not affected by key revocation. If secure code wants to enforce that a revoked key is no longer usable by a peripheral for cryptographic operations, the secure code should disable or reset the peripheral in question.

**Note:** If a key slot is revoked, the KMU will automatically zeroize the associated VALUE registers.

#### 7.1.18.4.3 STATUS register

The KMU uses a STATUS register to indicate its status of operation. The SELECTED bit will be asserted whenever the currently selected key slot is successfully read from or written to.

All read or write operations to other key slots than what is currently selected in KMU->SELECTKEYSLOT will assert the BLOCKED bit. The BLOCKED bit will also be asserted if the KMU fails to select a key slot, or if a request has been blocked due to an access violation. Normal operation using the KMU should never trigger the BLOCKED bit. If this bit is triggered during the development phase, it indicates that the code is using the KMU incorrectly.

The STATUS register is reset every time register SELECTKEYSLOT is written.

#### 7.1.18.5 Registers

| Base address | Domain      | Peripheral | Instance | Secure mapping | DMA security | Description         | Configuration |
|--------------|-------------|------------|----------|----------------|--------------|---------------------|---------------|
| 0x50039000   | APPLICATION | KMU        | KMU : S  | SPLIT          | NA           | Key management unit |               |
| 0x40039000   |             |            | KMU : NS |                |              |                     |               |

Table 93: Instances

| Register                | Offset | Security | Description                                                                                       |
|-------------------------|--------|----------|---------------------------------------------------------------------------------------------------|
| TASKS_PUSH_KEYSLLOT     | 0x0000 |          | Push a key slot over secure APB                                                                   |
| EVENTS_KEYSLLOT_PUSHED  | 0x100  |          | Key slot successfully pushed over secure APB                                                      |
| EVENTS_KEYSLLOT_REVOKED | 0x104  |          | Key slot has been revoked and cannot be tasked for selection                                      |
| EVENTS_KEYSLLOT_ERROR   | 0x108  |          | No key slot selected, no destination address defined, or error during push operation              |
| INTEN                   | 0x300  |          | Enable or disable interrupt                                                                       |
| INTENSET                | 0x304  |          | Enable interrupt                                                                                  |
| INTENCLR                | 0x308  |          | Disable interrupt                                                                                 |
| INTPEND                 | 0x30C  |          | Pending interrupts                                                                                |
| STATUS                  | 0x40C  |          | Status bits for KMU operation                                                                     |
| SELECTKEYSLOT           | 0x500  |          | Select key slot to be read over AHB or pushed over secure APB when TASKS_PUSH_KEYSLLOT is started |

Table 94: Register overview



|                  |            |  |  |                       |  |  |       |  |  |                                                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|--|-----------------------|--|--|-------|--|--|--------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |  |                       |  |  |       |  |  | 31                                                                                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |  |  |                       |  |  |       |  |  | A                                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |  |                       |  |  |       |  |  | 0                                                                                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  |  | Value ID              |  |  | Value |  |  | Description                                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         |  |  | EVENTS_KEYSLLOT_ERROR |  |  |       |  |  | No key slot selected, no destination address defined, or error during push operation |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  |  | NotGenerated          |  |  | 0     |  |  | Event not generated                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  |  | Generated             |  |  | 1     |  |  | Event generated                                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.18.5.5 INTEN

Address offset: 0x300

Enable or disable interrupt

| Bit number       |      |                 |          | 31    | 30                                                                    | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
|------------------|------|-----------------|----------|-------|-----------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ID               |      |                 |          |       |                                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | C | B | A |
| Reset 0x00000000 |      |                 |          | 0     | 0                                                                     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |
| ID               | Acce | Field           | Value ID | Value | Description                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW   | KEYSLOT_PUSHED  |          |       | Enable or disable interrupt for event <a href="#">KEYSLOT_PUSHED</a>  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |                 | Disabled | 0     | Disable                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |                 | Enabled  | 1     | Enable                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW   | KEYSLOT_REVOKED |          |       | Enable or disable interrupt for event <a href="#">KEYSLOT_REVOKED</a> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |                 | Disabled | 0     | Disable                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |                 | Enabled  | 1     | Enable                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| C                | RW   | KEYSLOT_ERROR   |          |       | Enable or disable interrupt for event <a href="#">KEYSLOT_ERROR</a>   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |                 | Disabled | 0     | Disable                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |                 | Enabled  | 1     | Enable                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.18.5.6 INTENSET

Address offset: 0x304

Enable interrupt

|                  |            |                                                                                       |       |                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|---------------------------------------------------------------------------------------|-------|-------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            | C B A                                                                                 |       |                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |       |                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID                                                                              | Value | Description                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | KEYSLOT_PUSHED                                                                        |       | Write '1' to enable interrupt for event <a href="#">KEYSLOT_PUSHED</a>  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Set                                                                                   | 1     | Enable                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled                                                                              | 0     | Read: Disabled                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled                                                                               | 1     | Read: Enabled                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW         | KEYSLOT_REVOKED                                                                       |       | Write '1' to enable interrupt for event <a href="#">KEYSLOT_REVOKED</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Set                                                                                   | 1     | Enable                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled                                                                              | 0     | Read: Disabled                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled                                                                               | 1     | Read: Enabled                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW         | KEYSLOT_ERROR                                                                         |       | Write '1' to enable interrupt for event <a href="#">KEYSLOT_ERROR</a>   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Set                                                                                   | 1     | Enable                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled                                                                              | 0     | Read: Disabled                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled                                                                               | 1     | Read: Enabled                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.18.5.7 INTENCLR

Address offset: 0x308

## Disable interrupt

| Bit number       |                    |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|--------------------|----------|---------------------------------------------------------------------------------------|--------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |                    |          | C B A                                                                                 |                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |                    |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field         | Value ID | Value                                                                                 | Description                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW KEYSLOT_PUSHED  |          |                                                                                       | Write '1' to disable interrupt for event <a href="#">KEYSLOT_PUSHED</a>  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                    | Clear    | 1                                                                                     | Disable                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                    | Disabled | 0                                                                                     | Read: Disabled                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                    | Enabled  | 1                                                                                     | Read: Enabled                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW KEYSLOT_REVOKED |          |                                                                                       | Write '1' to disable interrupt for event <a href="#">KEYSLOT_REVOKED</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                    | Clear    | 1                                                                                     | Disable                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                    | Disabled | 0                                                                                     | Read: Disabled                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                    | Enabled  | 1                                                                                     | Read: Enabled                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW KEYSLOT_ERROR   |          |                                                                                       | Write '1' to disable interrupt for event <a href="#">KEYSLOT_ERROR</a>   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                    | Clear    | 1                                                                                     | Disable                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                    | Disabled | 0                                                                                     | Read: Disabled                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                    | Enabled  | 1                                                                                     | Read: Enabled                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

## 7.1.18.5.8 INTPEND

Address offset: 0x30C

Pending interrupts

| Bit number       |            |                 | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                               |                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|-----------------|---------------------------------------------------------------------------------------|-------------------------------------------------------------------------------|-------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |            |                 | C B A                                                                                 |                                                                               |                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |                 | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                               |                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID        | Value                                                                                 | Description                                                                   |                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | R          | KEYSLOT_PUSHED  |                                                                                       | Read pending status of interrupt for event<br><a href="#">KEYSLOT_PUSHED</a>  |                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |                 | NotPending                                                                            | 0                                                                             | Read: Not pending |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |                 | Pending                                                                               | 1                                                                             | Read: Pending     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | R          | KEYSLOT_REVOKED |                                                                                       | Read pending status of interrupt for event<br><a href="#">KEYSLOT_REVOKED</a> |                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |                 | NotPending                                                                            | 0                                                                             | Read: Not pending |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |                 | Pending                                                                               | 1                                                                             | Read: Pending     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | R          | KEYSLOT_ERROR   |                                                                                       | Read pending status of interrupt for event <a href="#">KEYSLOT_ERROR</a>      |                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |                 | NotPending                                                                            | 0                                                                             | Read: Not pending |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |                 | Pending                                                                               | 1                                                                             | Read: Pending     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

## 7.1.18.5.9 STATUS

Address offset: 0x40C

Status bits for KMU operation

This register is reset and re-written by the KMU whenever SELECTKEYSLOT is written

| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|----------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |            |          |                                                                                       |                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | R          | SELECTED |                                                                                       | Key slot ID successfully selected by the KMU |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | No key slot ID selected by KMU               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Key slot ID successfully selected by KMU     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | R          | BLOCKED  |                                                                                       | Violation status                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | No access violation detected                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Access violation detected and blocked        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.18.5.10 SELECTKEYSLOT

Address offset: 0x500

Select key slot to be read over AHB or pushed over secure APB when TASKS\_PUSH\_KEYSLLOT is started

|                  |            |          |                                                                                       |                                                                                                                                                                                                                                                                                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                                                                                                                                                                                                                                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          | A A A A A A A A                                                                       |                                                                                                                                                                                                                                                                                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                                                                                                                                                                                                                                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                                                                                                                                                                                                                                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | ID       |                                                                                       | <p>Select key slot ID to be read over AHB, or pushed over secure APB, when TASKS_PUSH_KEYSLLOT is started.</p> <p>NOTE: ID=0 is not a valid key slot ID. The 0 ID should be used when the KMU is idle or not in use.</p> <p>NOTE: Index N in UICR-&gt;KEYSLOT.KEY[N] and UICR-&gt;KEYSLOT.CONFIG[N] corresponds to KMU key slot ID=N+1.</p> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

## 7.1.19 LPCOMP — Low-power comparator

Low-power comparator (LPCOMP) compares an input voltage against a reference voltage.

Listed here are the main features of LPCOMP:

- 0 - VDD input range
- Ultra-low power
- Eight input options (**AIN0** to **AIN7**)
- Reference voltage options:
  - Two external analog reference inputs, or
  - 15-level internal reference ladder (VDD/16)
- Optional hysteresis enable on input
- Can be used as a wakeup source from System OFF mode

In System ON, the LPCOMP can generate separate events on rising and falling edges of a signal, or sample the current state of the pin as being above or below the selected reference. The block can be configured to use any of the analog inputs on the device. Additionally, the low-power comparator can be used as an analog wakeup source from System OFF or System ON. The comparator threshold can be programmed to a range of fractions of the supply voltage.

**Note:** LPCOMP cannot be used (STARTed) at the same time as COMP. Only one comparator can be used at a time.



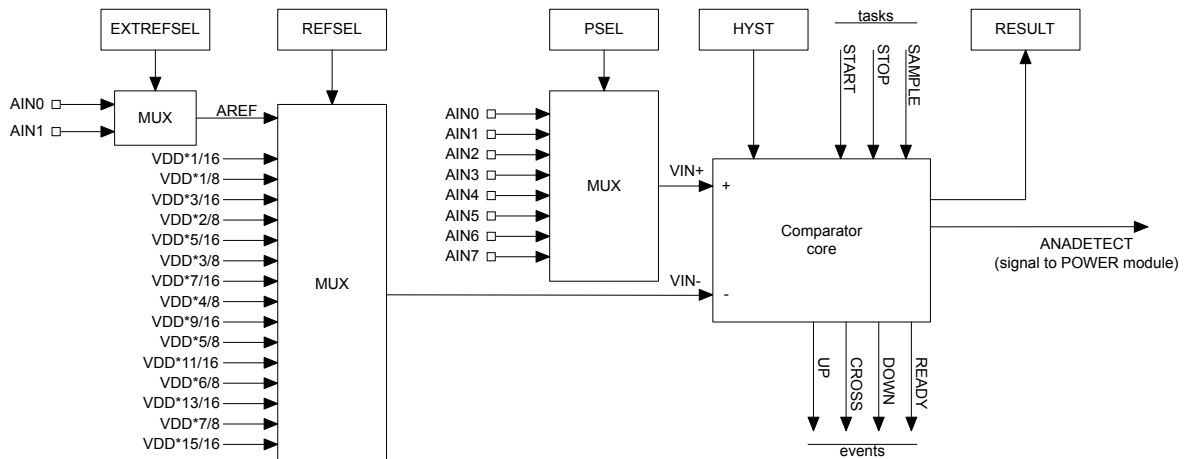


Figure 83: Low-power comparator

The wakeup comparator (LPCOMP) compares an input voltage ( $V_{IN+}$ ), which comes from an analog input pin selected via the PSEL register, against a reference voltage ( $V_{IN-}$ ) selected via registers REFSEL on page 277 and EXTREFSEL.

The PSEL, REFSEL, and EXTREFSEL registers must be configured before the LPCOMP is enabled through the ENABLE register.

The HYST register allows enabling an optional hysteresis in the comparator core. This hysteresis shall prevent noise on the signal to create unwanted events. Figure below illustrates the effect of an active hysteresis on a noisy input signal. It is disabled by default, and shall be configured before enabling LPCOMP as well.

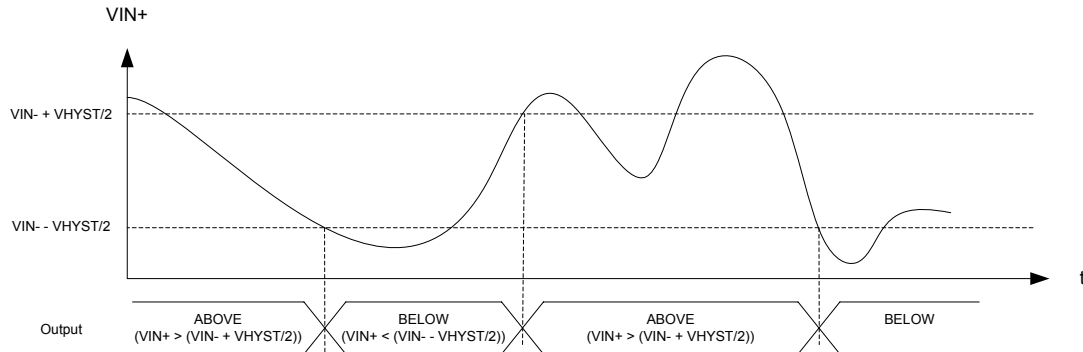


Figure 84: Effect of hysteresis on a noisy input signal

The LPCOMP is started by triggering the START task. After a startup time of  $t_{LPCOMP,STARTUP}$ , the LPCOMP will generate a READY event to indicate that the comparator is ready to use and the output of the LPCOMP is correct. The LPCOMP will generate events every time  $V_{IN+}$  crosses  $V_{IN-}$ . More specifically, every time  $V_{IN+}$  rises above  $V_{IN-}$  (upward crossing) an UP event is generated along with a CROSS event. Every time  $V_{IN+}$  falls below  $V_{IN-}$  (downward crossing), a DOWN event is generated along with a CROSS event. When hysteresis is enabled, the upward crossing level becomes  $(V_{IN-} + VHYST/2)$ , and the downward crossing level becomes  $(V_{IN-} - VHYST/2)$ .

The LPCOMP is stopped by triggering the STOP task.

LPCOMP will be operational in both System ON and System OFF mode when it is enabled through the ENABLE register. See [POWER — Power control](#) on page 36 for more information about power modes. Note that it is not allowed to go to System OFF when a READY event is pending to be generated.

All LPCOMP registers, including ENABLE, are classified as retained registers when the LPCOMP is enabled. However, when the device wakes up from System OFF, all LPCOMP registers will be reset.

The LPCOMP can wake up the system from System OFF by asserting the ANADETECT signal. The ANADETECT signal can be derived from any of the event sources that generate the UP, DOWN and CROSS events. In case of wakeup from System OFF, no events will be generated, only the ANADETECT signal. See the ANADETECT register ([ANADETECT](#) on page 278) for more information on how to configure the ANADETECT signal.

The immediate value of the LPCOMP can be sampled to [RESULT](#) on page 276 by triggering the SAMPLE task.

See [RESETREAS](#) on page 59 for more information on how to detect a wakeup from LPCOMP.

### 7.1.19.1 Shared resources

The LPCOMP shares analog resources with SAADC. While it is possible to use the SAADC at the same time as the LPCOMP, selecting the same analog input pin for both modules is not supported.

Additionally, LPCOMP shares registers and other resources with other peripherals that have the same ID as the LPCOMP. See [Peripherals with shared ID](#) on page 138 for more information.

The LPCOMP peripheral shall not be disabled (by writing to the ENABLE register) before the peripheral has been stopped. Failing to do so may result in unpredictable behavior.

### 7.1.19.2 Pin configuration

You can use the LPCOMP.PSEL register to select one of the analog input pins, **AIN0** through **AIN7**, as the analog input pin for the LPCOMP.

See [GPIO — General purpose input/output](#) on page 209 for more information about the pins. Similarly, you can use [EXTREFSEL](#) on page 277 to select one of the analog reference input pins, **AIN0** and **AIN1**, as input for AREF in case AREF is selected in [EXTREFSEL](#) on page 277. The selected analog pins will be acquired by the LPCOMP when it is enabled through [ENABLE](#) on page 276.

### 7.1.19.3 Registers

| Base address | Domain      | Peripheral | Instance    | Secure mapping | DMA security | Description          | Configuration |
|--------------|-------------|------------|-------------|----------------|--------------|----------------------|---------------|
| 0x5001A000   | APPLICATION | LPCOMP     | LPCOMP : S  | US             | NA           | Low-power comparator |               |
| 0x4001A000   |             |            | LPCOMP : NS |                |              |                      |               |

Table 95: Instances

| Register                         | Offset | Security | Description                                             |
|----------------------------------|--------|----------|---------------------------------------------------------|
| <a href="#">TASKS_START</a>      | 0x000  |          | Start comparator                                        |
| <a href="#">TASKS_STOP</a>       | 0x004  |          | Stop comparator                                         |
| <a href="#">TASKS_SAMPLE</a>     | 0x008  |          | Sample comparator value                                 |
| <a href="#">SUBSCRIBE_START</a>  | 0x080  |          | Subscribe configuration for task <a href="#">START</a>  |
| <a href="#">SUBSCRIBE_STOP</a>   | 0x084  |          | Subscribe configuration for task <a href="#">STOP</a>   |
| <a href="#">SUBSCRIBE_SAMPLE</a> | 0x088  |          | Subscribe configuration for task <a href="#">SAMPLE</a> |
| <a href="#">EVENTS_READY</a>     | 0x100  |          | LPCOMP is ready and output is valid                     |
| <a href="#">EVENTS_DOWN</a>      | 0x104  |          | Downward crossing                                       |
| <a href="#">EVENTS_UP</a>        | 0x108  |          | Upward crossing                                         |
| <a href="#">EVENTS_CROSS</a>     | 0x10C  |          | Downward or upward crossing                             |
| <a href="#">PUBLISH_READY</a>    | 0x180  |          | Publish configuration for event <a href="#">READY</a>   |
| <a href="#">PUBLISH_DOWN</a>     | 0x184  |          | Publish configuration for event <a href="#">DOWN</a>    |
| <a href="#">PUBLISH_UP</a>       | 0x188  |          | Publish configuration for event <a href="#">UP</a>      |
| <a href="#">PUBLISH_CROSS</a>    | 0x18C  |          | Publish configuration for event <a href="#">CROSS</a>   |
| <a href="#">SHORTS</a>           | 0x200  |          | Shortcuts between local events and tasks                |
| <a href="#">INTENSET</a>         | 0x304  |          | Enable interrupt                                        |

| Register  | Offset | Security | Description                  |
|-----------|--------|----------|------------------------------|
| INTENCLR  | 0x308  |          | Disable interrupt            |
| RESULT    | 0x400  |          | Compare result               |
| ENABLE    | 0x500  |          | Enable LPCOMP                |
| PSEL      | 0x504  |          | Input pin select             |
| REFSEL    | 0x508  |          | Reference select             |
| EXTREFSEL | 0x50C  |          | External reference select    |
| ANADETECT | 0x520  |          | Analog detect configuration  |
| HYST      | 0x538  |          | Comparator hysteresis enable |

Table 96: Register overview

### 7.1.19.3.1 TASKS\_START

Address offset: 0x000

Start comparator

|                  |               |          |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|---------------|----------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |               |          |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |               |          |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |               |          |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field    | Value ID | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W TASKS_START |          |       | Start comparator                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |               | Trigger  | 1     | Trigger task                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.19.3.2 TASKS\_STOP

Address offset: 0x004

Stop comparator

|                  |              |          |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|--------------|----------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |              |          |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |              |          |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |              |          |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field   | Value ID | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W TASKS_STOP |          |       | Stop comparator                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Trigger  | 1     | Trigger task                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.19.3.3 TASKS\_SAMPLE

Address offset: 0x008

Sample comparator value

|                  |                |          |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|----------------|----------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |                |          |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |                |          |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |                |          |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field     | Value ID | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W TASKS_SAMPLE |          |       | Sample comparator value                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                | Trigger  | 1     | Trigger task                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.19.3.4 SUBSCRIBE\_START

Address offset: 0x080

Subscribe configuration for task **START**

|                  |            |          |                                                                                       |                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|--------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |          | B                                                                                     |                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                              | Channel that task <b>START</b> will subscribe to |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |                                                                                       |                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Disable subscription                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Enable subscription                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

### 7.1.19.3.5 SUBSCRIBE\_STOP

Address offset: 0x084

Subscribe configuration for task **STOP**

|                  |            |          |          |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|----------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |          |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |          |          | B                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value    | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0] | Channel that task <b>STOP</b> will subscribe to                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |          |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0        | Disable subscription                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1        | Enable subscription                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

### 7.1.19.3.6 SUBSCRIBE\_SAMPLE

Address offset: 0x088

Subscribe configuration for task **SAMPLE**

|                  |            |  |          |                                                                                       |  |                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|--|----------|---------------------------------------------------------------------------------------|--|---------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |  |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |  |          | B                                                                                     |  |                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |  |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |  |                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field |  | Value ID | Value                                                                                 |  | Description                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |  |          | [255..0]                                                                              |  | Channel that task <b>SAMPLE</b> will subscribe to |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |  |          |                                                                                       |  |                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            |  | Disabled | 0                                                                                     |  | Disable subscription                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            |  | Enabled  | 1                                                                                     |  | Enable subscription                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

### 7.1.19.3.7 EVENTS\_READY

Address offset: 0x100

LPCOMP is ready and output is valid

|                  |                 |              |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|-----------------|--------------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |                 |              |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |                 |              |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |                 |              |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field      | Value ID     | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW EVENTS_READY |              |       | LPCOMP is ready and output is valid                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                 | NotGenerated | 0     | Event not generated                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                 | Generated    | 1     | Event generated                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.19.3.8 EVENTS\_DOWN

Address offset: 0x104

Downward crossing

|                  |      |             |              |    |       |                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|------------------|------|-------------|--------------|----|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|---|
| Bit number       |      |             |              | 31 | 30    | 29                  | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |   |
| ID               |      |             |              |    |       |                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  | A |
| Reset 0x00000000 |      |             |              | 0  | 0     | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |   |
| ID               | Acce | Field       | Value        | ID | Value | Description         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
| A                | RW   | EVENTS_DOWN |              |    |       | Downward crossing   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|                  |      |             | NotGenerated | 0  |       | Event not generated |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|                  |      |             | Generated    | 1  |       | Event generated     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |

### 7.1.19.3.9 EVENTS\_UP

Address offset: 0x108

Upward crossing

|                  |            |           |          |              |       |                 |                     |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-----------|----------|--------------|-------|-----------------|---------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |           |          |              |       |                 |                     |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |           |          |              |       |                 |                     |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |
| Reset 0x00000000 |            |           |          |              |       |                 |                     |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |           | Value ID |              | Value |                 | Description         |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | EVENTS_UP |          |              |       | Upward crossing |                     |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |           |          | NotGenerated |       | 0               | Event not generated |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |           |          | Generated    |       | 1               | Event generated     |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.19.3.10 EVENTS\_CROSS

Address offset: 0x10C

Downward or upward crossing

|                  |            |              |       |                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------------|-------|-----------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |              |       | 31                          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |              |       |                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |
| Reset 0x00000000 |            |              |       | 0                           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID     | Value | Description                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | EVENTS_CROSS |       | Downward or upward crossing |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | NotGenerated | 0     | Event not generated         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Generated    | 1     | Event generated             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.19.3.11 PUBLISH\_READY

Address offset: 0x180

Publish configuration for event [READY](#)

|                  |            |          |          |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|--------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                                               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |          |          | B                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |          | 0                                                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce Field | Value ID | Value    | Description                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] | Channel that event <b>READY</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        | Disable publishing                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        | Enable publishing                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.19.3.12 PUBLISH\_DOWN

Address offset: 0x184

Publish configuration for event **DOWN**

|                  |            |          |          |                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|-------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |          |          | B                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |          | 0                                               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce Field | Value ID | Value    | Description                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] | Channel that event <b>DOWN</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        | Disable publishing                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        | Enable publishing                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.19.3.13 PUBLISH\_UP

Address offset: 0x188

Publish configuration for event **UP**

|                  |            |  |          |                                                                         |    |                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|-------------------------------------------------------------------------|----|----------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31                                                                      | 30 | 29                                     | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |  |          | B                                                                       |    |                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |    |                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field |  | Value ID | Value                                                                   |    | Description                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          | [255..0]                                                                |    | Channel that event UP will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |                                                                         |    |                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled | 0                                                                       |    | Disable publishing                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  | 1                                                                       |    | Enable publishing                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.19.3.14 PUBLISH\_CROSS

Address offset: 0x18C

Publish configuration for event **CROSS**

|                  |            |          |          |                                                                         |    |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|-------------------------------------------------------------------------|----|--------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                                                                      | 30 | 29                                               | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |          |          | B                                                                       |    |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |    |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field |          | Value ID | Value                                                                   |    | Description                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          |          | [255..0]                                                                |    | Channel that event <b>CROSS</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |                                                                         |    |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled |          | 0                                                                       |    | Disable publishing                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  |          | 1                                                                       |    | Enable publishing                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.19.3.15 SHORTS

Address offset: 0x200

Shortcuts between local events and tasks

| Bit number       |      |              | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|--------------|---------------------------------------------------------------------------------------|-------|------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |      |              | E D C B A                                                                             |       |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |              | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |       |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field        | Value ID                                                                              | Value | Description                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW   | READY_SAMPLE |                                                                                       |       | Shortcut between event <span>READY</span> and task <span>SAMPLE</span> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |              | Disabled                                                                              | 0     | Disable shortcut                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |              | Enabled                                                                               | 1     | Enable shortcut                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW   | READY_STOP   |                                                                                       |       | Shortcut between event <span>READY</span> and task <span>STOP</span>   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |              | Disabled                                                                              | 0     | Disable shortcut                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |              | Enabled                                                                               | 1     | Enable shortcut                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW   | DOWN_STOP    |                                                                                       |       | Shortcut between event <span>DOWN</span> and task <span>STOP</span>    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |              | Disabled                                                                              | 0     | Disable shortcut                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |              | Enabled                                                                               | 1     | Enable shortcut                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| D                | RW   | UP_STOP      |                                                                                       |       | Shortcut between event <span>UP</span> and task <span>STOP</span>      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |              | Disabled                                                                              | 0     | Disable shortcut                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |              | Enabled                                                                               | 1     | Enable shortcut                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| E                | RW   | CROSS_STOP   |                                                                                       |       | Shortcut between event <span>CROSS</span> and task <span>STOP</span>   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |              | Disabled                                                                              | 0     | Disable shortcut                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |              | Enabled                                                                               | 1     | Enable shortcut                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.19.3.16 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number       |      |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|-------|---------------------------------------------------------------------------------------|-------|------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |      |       | D C B A                                                                               |       |                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |       |                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field | Value ID                                                                              | Value | Description                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW   | READY |                                                                                       |       | Write '1' to enable interrupt for event <span>READY</span> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Set                                                                                   | 1     | Enable                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Disabled                                                                              | 0     | Read: Disabled                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Enabled                                                                               | 1     | Read: Enabled                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW   | DOWN  |                                                                                       |       | Write '1' to enable interrupt for event <span>DOWN</span>  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Set                                                                                   | 1     | Enable                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Disabled                                                                              | 0     | Read: Disabled                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Enabled                                                                               | 1     | Read: Enabled                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW   | UP    |                                                                                       |       | Write '1' to enable interrupt for event <span>UP</span>    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Set                                                                                   | 1     | Enable                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Disabled                                                                              | 0     | Read: Disabled                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Enabled                                                                               | 1     | Read: Enabled                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| D                | RW   | CROSS |                                                                                       |       | Write '1' to enable interrupt for event <span>CROSS</span> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Set                                                                                   | 1     | Enable                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Disabled                                                                              | 0     | Read: Disabled                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Enabled                                                                               | 1     | Read: Enabled                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.19.3.17 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number       |      |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|-------|---------------------------------------------------------------------------------------|-------|-------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |      |       | D C B A                                                                               |       |                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                   |       |                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field | Value ID                                                                              | Value | Description                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW   | READY |                                                                                       |       | Write '1' to disable interrupt for event <span>READY</span> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Clear                                                                                 | 1     | Disable                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Disabled                                                                              | 0     | Read: Disabled                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Enabled                                                                               | 1     | Read: Enabled                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW   | DOWN  |                                                                                       |       | Write '1' to disable interrupt for event <span>DOWN</span>  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Clear                                                                                 | 1     | Disable                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Disabled                                                                              | 0     | Read: Disabled                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Enabled                                                                               | 1     | Read: Enabled                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW   | UP    |                                                                                       |       | Write '1' to disable interrupt for event <span>UP</span>    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Clear                                                                                 | 1     | Disable                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Disabled                                                                              | 0     | Read: Disabled                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Enabled                                                                               | 1     | Read: Enabled                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| D                | RW   | CROSS |                                                                                       |       | Write '1' to disable interrupt for event <span>CROSS</span> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Clear                                                                                 | 1     | Disable                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Disabled                                                                              | 0     | Read: Disabled                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Enabled                                                                               | 1     | Read: Enabled                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.19.3.18 RESULT

Address offset: 0x400

Compare result

|                  |            |          |                                                                                       |                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|--------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          | A                                                                                     |                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | R          | RESULT   |                                                                                       | Result of last compare. Decision point SAMPLE task.          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Below    | 0                                                                                     | Input voltage is below the reference threshold (VIN+ < VIN-) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Above    | 1                                                                                     | Input voltage is above the reference threshold (VIN+ > VIN-) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.19.3.19 ENABLE

Address offset: 0x500

Enable LPCOMP

|                  |      |        |          |                                                                                       |                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|--------|----------|---------------------------------------------------------------------------------------|--------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |        |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |        |          | A A                                                                                   |                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |        |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field  | Value ID | Value                                                                                 | Description              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW   | ENABLE |          |                                                                                       | Enable or disable LPCOMP |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |        | Disabled | 0                                                                                     | Disable                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |        | Enabled  | 1                                                                                     | Enable                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |



### 7.1.19.3.20 PSEL

Address offset: 0x504

Input pin select

| Bit number       |      |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|-------|---------------------------------------------------------------------------------------|-------|-------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |      |       | A A A                                                                                 |       |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |       |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field | Value ID                                                                              | Value | Description                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW   | PSEL  |                                                                                       |       | Analog pin select             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | AnalogInput0                                                                          | 0     | AIN0 selected as analog input |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | AnalogInput1                                                                          | 1     | AIN1 selected as analog input |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | AnalogInput2                                                                          | 2     | AIN2 selected as analog input |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | AnalogInput3                                                                          | 3     | AIN3 selected as analog input |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | AnalogInput4                                                                          | 4     | AIN4 selected as analog input |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | AnalogInput5                                                                          | 5     | AIN5 selected as analog input |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | AnalogInput6                                                                          | 6     | AIN6 selected as analog input |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | AnalogInput7                                                                          | 7     | AIN7 selected as analog input |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.19.3.21 REFSEL

Address offset: 0x508

Reference select

|                  |      |        |             |                                                                                       |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|--------|-------------|---------------------------------------------------------------------------------------|------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |        |             | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |        |             | A A A A                                                                               |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000004 |      |        |             | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0                 |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field  | Value ID    | Value                                                                                 | Description                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW   | REFSEL |             |                                                                                       | Reference select                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |        | Ref1_8Vdd   | 0                                                                                     | VDD * 1/8 selected as reference    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |        | Ref2_8Vdd   | 1                                                                                     | VDD * 2/8 selected as reference    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |        | Ref3_8Vdd   | 2                                                                                     | VDD * 3/8 selected as reference    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |        | Ref4_8Vdd   | 3                                                                                     | VDD * 4/8 selected as reference    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |        | Ref5_8Vdd   | 4                                                                                     | VDD * 5/8 selected as reference    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |        | Ref6_8Vdd   | 5                                                                                     | VDD * 6/8 selected as reference    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |        | Ref7_8Vdd   | 6                                                                                     | VDD * 7/8 selected as reference    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |        | ARef        | 7                                                                                     | External analog reference selected |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |        | Ref1_16Vdd  | 8                                                                                     | VDD * 1/16 selected as reference   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |        | Ref3_16Vdd  | 9                                                                                     | VDD * 3/16 selected as reference   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |        | Ref5_16Vdd  | 10                                                                                    | VDD * 5/16 selected as reference   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |        | Ref7_16Vdd  | 11                                                                                    | VDD * 7/16 selected as reference   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |        | Ref9_16Vdd  | 12                                                                                    | VDD * 9/16 selected as reference   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |        | Ref11_16Vdd | 13                                                                                    | VDD * 11/16 selected as reference  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |        | Ref13_16Vdd | 14                                                                                    | VDD * 13/16 selected as reference  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |        | Ref15_16Vdd | 15                                                                                    | VDD * 15/16 selected as reference  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.19.3.22 EXTREFSEL

Address offset: 0x50C

External reference select

|                  |            |           |          |                  |       |                                  |                                       |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-----------|----------|------------------|-------|----------------------------------|---------------------------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |           |          |                  |       |                                  |                                       |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |           |          |                  |       |                                  |                                       |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |   |
| Reset 0x00000000 |            |           |          |                  |       |                                  |                                       |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |           | Value ID |                  | Value |                                  | Description                           |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | EXTREFSEL |          |                  |       | External analog reference select |                                       |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |           |          | AnalogReference0 |       | 0                                | Use AIN0 as external analog reference |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |           |          | AnalogReference1 |       | 1                                | Use AIN1 as external analog reference |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.19.3.23 ANADETECT

Address offset: 0x520

Analog detect configuration

|                  |            |           |          |       |    |                                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-----------|----------|-------|----|----------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |           |          | 31    | 30 | 29                                                                         | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |           |          |       |    |                                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A | A |
| Reset 0x00000000 |            |           |          | 0     | 0  | 0                                                                          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |
| ID               | Acce Field |           | Value ID | Value |    | Description                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | ANADETECT |          |       |    | Analog detect configuration                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Cross     |          | 0     |    | Generate ANADETECT on crossing, both upward crossing and downward crossing |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Up        |          | 1     |    | Generate ANADETECT on upward crossing only                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Down      |          | 2     |    | Generate ANADETECT on downward crossing only                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.19.3.24 HYST

Address offset: 0x538

Comparator hysteresis enable

|                  |            |      |          |       |    |                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|------------------|------------|------|----------|-------|----|--------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|---|
| Bit number       |            |      |          | 31    | 30 | 29                             | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |   |
| ID               |            |      |          |       |    |                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | A |
| Reset 0x00000000 |            |      |          | 0     | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |   |
| ID               | Acce Field |      | Value ID | Value |    | Description                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
| A                | RW         | HYST |          |       |    | Comparator hysteresis enable   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            |      | Disabled | 0     |    | Comparator hysteresis disabled |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            |      | Enabled  | 1     |    | Comparator hysteresis enabled  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |

## 7.1.19.4 Electrical specification

### 7.1.19.4.1 LPCOMP Electrical Specification

| Symbol         | Description                                                                          | Min. | Typ. | Max. | Units   |
|----------------|--------------------------------------------------------------------------------------|------|------|------|---------|
| $t_{LPCANDET}$ | Time from VIN crossing ( $\geq 50$ mV above threshold) to ANADETECT signal generated | ..   | ..   | ..   | $\mu$ s |
| $V_{INOFFSET}$ | Input offset including reference ladder error                                        | ..   | ..   | ..   | mV      |
| $V_{HYST}$     | Optional hysteresis                                                                  | ..   | ..   | ..   | mV      |
| $t_{STARTUP}$  | Startup time for LPCOMP                                                              | ..   | ..   | ..   | $\mu$ s |

## 7.1.20 MUTEX — Mutual exclusive peripheral

The MUTEX peripheral uses mutual exclusion to support locking a resource that is shared between different CPUs in the system. The shared resource can only be used by one of these cores during the duration that it is locked.

The MUTEX peripheral includes several mutex registers. Each mutex register contains one bit which indicates if it is in a locked or unlocked state. Reading or writing to a mutex register may impact its state.

When a mutex is read, the following conditions apply:

- If the state is locked, the MUTEX[i] state is unchanged (remains in a locked state) and returns a value equal to 1.
- If the state is unlocked, the MUTEX[i] state changes to the locked state and returns a value equal to 0.

When writing '0' to a mutex, the following occurs:

- If the state is unlocked, the MUTEX[i] state is unchanged (remains in unlocked state) and the store is ignored.
- If the state is locked, the MUTEX[i] state changes to the unlocked state.

**Note:** Faults are not managed by the peripheral. If a mutex is locked and a fault occurs, it is the responsibility of the fault handler to release the mutex. If a fault handler is not managing the mutex release, the mutex will stay locked.

The following figure illustrates the mutex state transitions.

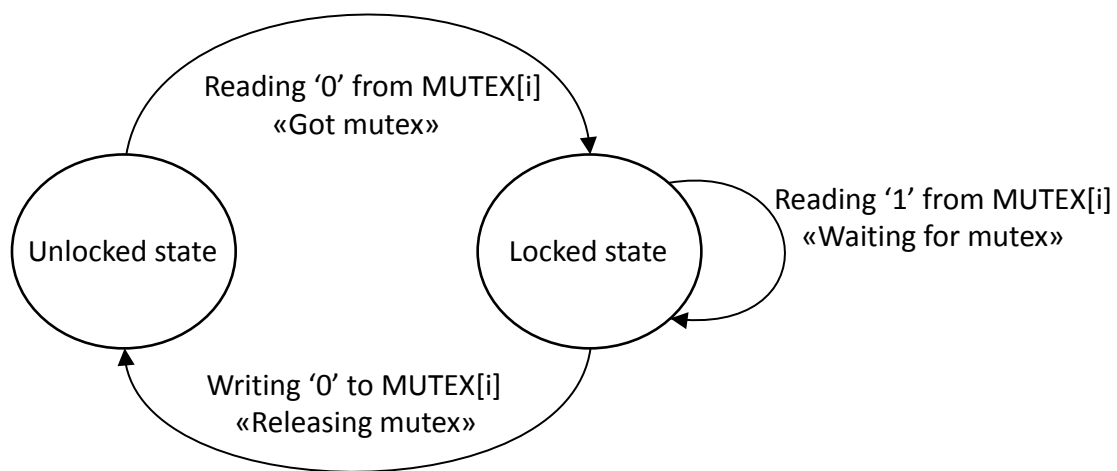


Figure 85: MUTEX - state transitions

The following code is an example of how a mutex can be used by two different CPUs:

```
// CPU0 Polling the MUX[0] register
while (NRF_MUX->MUX[0]){ // Read MUX[0]
    // If a 0 is read, the mutex will lock
    // If a 1 is read, polling will continue
}
// CPU0 working on shared data related to the mutex
...
NRF_MUX->MUX[0] = 0; // Release the mutex
```

```
// CPU1 Polling the MUX[0] register
while (NRF_MUX->MUX[0]){ // Read MUX[0]
    // If a 0 is read, the mutex will lock
    // If a 1 is read, polling will continue
}
// CPU1 working on shared data related to the mutex
...
NRF_MUX->MUX[0] = 0; // Release the mutex
```

Only one CPU can access the mutex at a time, meaning the mutex must be released before being accessed by the another CPU. If the load operation occurs at the same time, a bus arbitration mechanism will ensure only one CPU gets the mutex.

### 7.1.20.1 Registers

| Base address | Domain      | Peripheral | Instance     | Secure mapping | DMA security | Description                       | Configuration |
|--------------|-------------|------------|--------------|----------------|--------------|-----------------------------------|---------------|
| 0x50030000   | APPLICATION | MUTEX      | MUTEX : S    | US             | NA           | Mutual exclusive hardware support |               |
| 0x40030000   |             |            | MUTEX : NS   |                |              |                                   |               |
| 0x50030000   | NETWORK     | MUTEX      | APPMUTEX : S | US             | NA           | Mutex control                     |               |
| 0x40030000   |             |            | APPMUTEX :   |                |              |                                   |               |
|              |             |            | NS           |                |              |                                   |               |

Table 97: Instances

| Register | Offset | Security | Description    |
|----------|--------|----------|----------------|
| MUX[n]   | 0x400  |          | Mutex register |

Table 98: Register overview

#### 7.1.20.1.1 MUX[n] (n=0..15)

Address offset:  $0x400 + (n \times 0x4)$

Mutex register

|                  |            |  |          |       |    |                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |
|------------------|------------|--|----------|-------|----|------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|
| Bit number       |            |  |          | 31    | 30 | 29                           | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |
| ID               |            |  |          |       |    |                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |  |
| Reset 0x00000000 |            |  |          | 0     | 0  | 0                            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |
| ID               | Acce Field |  | Value ID | Value |    | Description                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |
| A                | RW MUTEX   |  |          |       |    | Mutex register n             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |            |  | Unlocked | 0     |    | Mutex n is in unlocked state |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |            |  | Locked   | 1     |    | Mutex n is in locked state   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |

## 7.1.21 NFCT — Near field communication tag

The NFCT peripheral is an implementation of an NFC Forum compliant listening device NFC-A.

With appropriate software, the NFCT peripheral can be used as the listening device NFC-A as specified by the [NFC Forum](#).

Listed here are the main features for the NFCT peripheral:

- NFC-A listen mode operation
  - 13.56 MHz input frequency
  - Bit rate 106 kbps
- Wake-on-field low power field detection (SENSE) mode
- Frame assemble and disassemble for the NFC-A frames specified by the NFC Forum
- Programmable frame timing controller
- Integrated automatic collision resolution, cyclic redundancy check (CRC), and parity functions

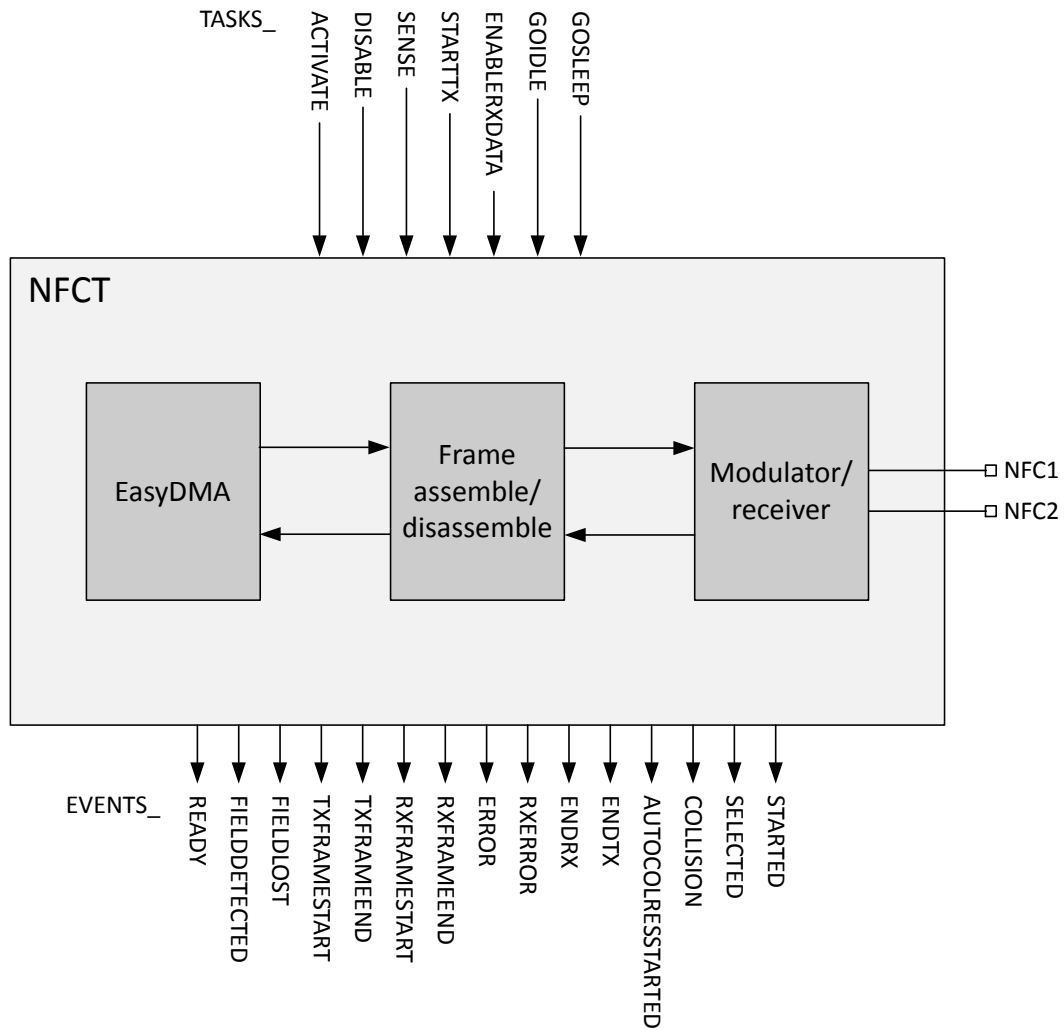


Figure 86: NFCT block diagram

#### 7.1.21.1 Overview

The NFCT peripheral contains a 13.56 MHz AM receiver and a 13.56 MHz load modulator with 106 kbps data rate as defined by the NFC Forum.

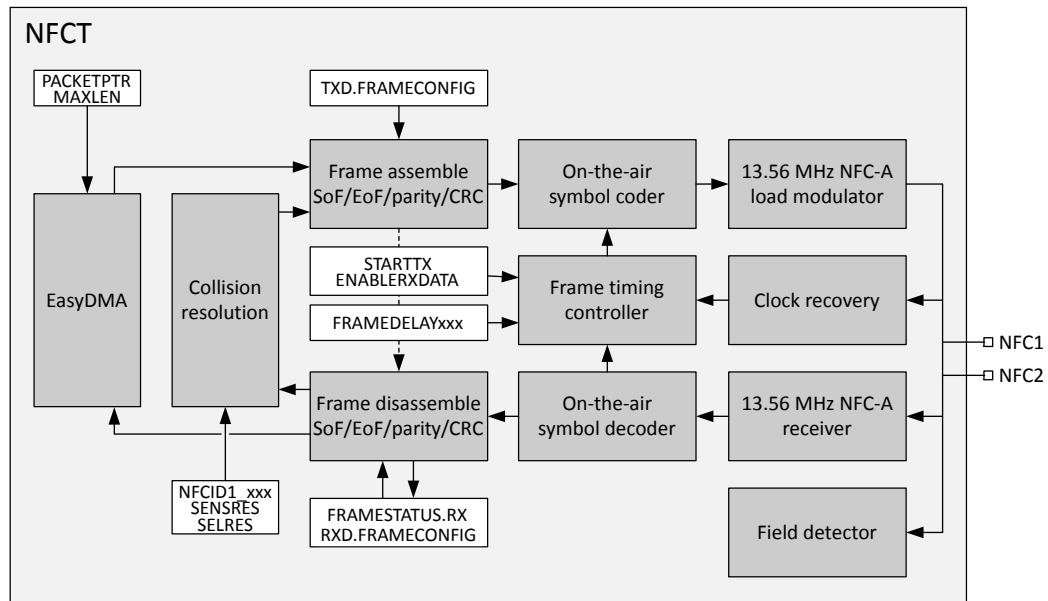


Figure 87: NFCT overview

When transmitting, the frame data will be transferred directly from RAM and transmitted with configurable frame type and delay timing. The system will be notified by an event whenever a complete frame is received or sent. The received frames will be automatically disassembled and the data part of the frame transferred to RAM.

The NFCT peripheral also supports the collision detection and resolution ("anticollision") as defined by the NFC Forum.

Wake-on-field is supported in SENSE mode while the device is either in System OFF or System ON mode. When the antenna enters an NFC field, an event will be triggered notifying the system to activate the NFCT functionality for incoming frames. In System ON, if the energy detected at the antenna increases beyond a threshold value, the module will generate a **FIELDDETECTED** event. When the strength of the field no longer supports NFC communication, the module will generate a **FIELDLOST** event. For the Low Power Field Detect threshold values, refer to **NFCT Electrical Specification** on page 317.

In System OFF, the NFCT Low Power Field Detect function can wake the system up through a reset. See **RESETREAS** on page 59 for more information on how to detect a wakeup from NFCT.

If the system is put into System OFF mode while a field is already present, the NFCT Low Power Field Detect function will wake the system up right away and generate a reset.

**Important:** As a consequence of a reset, NFCT is disabled, and therefore the reset handler will have to activate NFCT again and set it up properly.

The HFXO must be running before the NFCT peripheral goes into ACTIVATED state. Note that the NFCT peripheral calibration is automatically done on **ACTIVATE** task. The HFXO can be turned off when the NFCT peripheral goes into SENSE mode. The shortcut **FIELDDETECTED\_ACTIVATE** can be used when the HFXO is already running while in SENSE mode.

Outgoing data will be collected from RAM with the EasyDMA function and assembled according to the **TXD.FRAMECONFIG** on page 313 register. Incoming data will be disassembled according to the **RXD.FRAMECONFIG** register and the data section in the frame will be written to RAM via the EasyDMA function.

The NFCT peripheral includes a frame timing controller that can be used to accurately control the inter-frame delay between the incoming frame and a corresponding outgoing frame. It also includes optional CRC functionality.

### 7.1.21.2 Operating states

Tasks and events are used to control the operating state of the peripheral. The module can change state by triggering a task, or when specific operations are finalized. Events and tasks allow software to keep track of and change the current state.

See [Figure 86: NFCT block diagram](#) on page 282 and [Figure 88: NFCT state diagram, automatic collision resolution enabled](#) on page 284 for more information. See *NFC Forum, NFC Activity Technical Specification* for description on NFCT operating states.

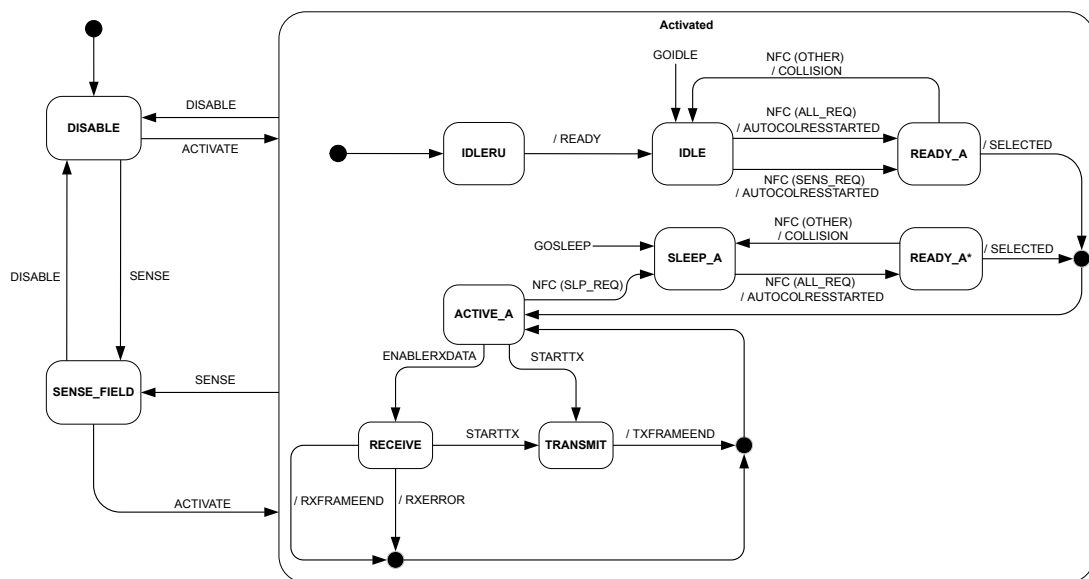


Figure 88: NFCT state diagram, automatic collision resolution enabled

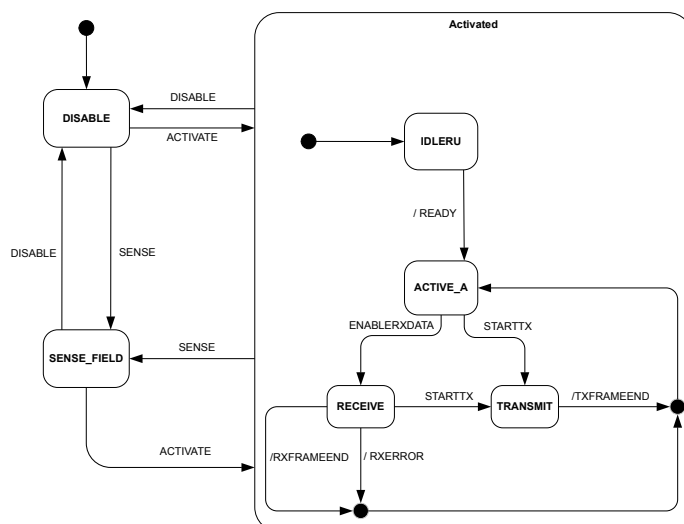


Figure 89: NFCT state diagram, automatic collision resolution disabled



**Important:**

- FIELDLOST event is not generated in SENSE mode.
- Sending SENSE task while field is still present does not generate **FIELDDETECTED** event.
- If the FIELDDETECTED event is cleared before sending the **ACTIVATE** task, then the FIELDDETECTED event shows up again after sending the ACTIVATE task. The shortcut FIELDDETECTED\_ACTIVATE can be used to avoid this condition.

### 7.1.21.3 Pin configuration

NFCT uses two pins to connect the antenna and these pins are shared with GPIOs.

The PROTECT field in the NFCPINS register in UICR defines the usage of these pins and their protection level against excessive voltages. The content of the NFCPINS register is reloaded at every reset. See [Pin assignments](#) on page 764 for the pins used by the NFCT peripheral.

When NFCPINS.PROTECT=NFC, a protection circuit will be enabled on the dedicated pins, preventing the chip from being damaged in the presence of a strong NFC field. The protection circuit will short the two pins together if voltage difference exceeds approximately 2V. The GPIO function on those pins will also be disabled.

When NFCPINS.PROTECT=Disabled, the device will not be protected against strong NFC field damages caught by a connected NFCT antenna, and the NFCT peripheral will not operate as expected, as it will never leave the DISABLE state.

The pins dedicated to the NFCT antenna function will have some limitation when the pins are configured for normal GPIO operation. The pin capacitance will be higher on those (refer to  $C_{PAD\_NFC}$  in the Electrical Specification of [GPIO — General purpose input/output](#) on page 209), and some increased leakage current between the two pins is to be expected if they are used in GPIO mode, and are driven to different logical values. To save power, the two pins should always be set to the same logical value whenever entering one of the device power saving modes. For details, refer to  $I_{NFC\_LEAK}$  in the Electrical Specification of [GPIO — General purpose input/output](#) on page 209.

### 7.1.21.4 EasyDMA

The NFCT peripheral implements EasyDMA for reading and writing of data packets from and to the Data RAM.

The NFCT EasyDMA utilizes a pointer called [PACKETPTR](#) on page 312 for receiving and transmitting packets.

The NFCT peripheral uses EasyDMA to read or write RAM, but not both at the same time. The event **RXFRAMESTART** indicates that the EasyDMA has started writing to the RAM for a receive frame and the event **RXFRAMEEND** indicates that the EasyDMA has completed writing to the RAM. Similarly, the event **TXFRAMESTART** indicates that the EasyDMA has started reading from the RAM for a transmit frame and the event **TXFRAMEEND** indicates that the EasyDMA has completed reading from the RAM. If a transmit and a receive operation is issued at the same time, the transmit operation would be prioritized.

Starting a transmit operation while the EasyDMA is writing a receive frame to the RAM will result in unpredictable behavior. Starting an EasyDMA operation when there is an ongoing EasyDMA operation may result in unpredictable behavior. It is recommended to wait for the TXFRAMEEND or RXFRAMEEND event for the ongoing transmit or receive before starting a new receive or transmit operation.

The **MAXLEN** on page 313 register determines the maximum number of bytes that can be read from or written to the RAM. This feature can be used to ensure that the NFCT peripheral does not overwrite, or read beyond, the RAM assigned to a packet. Note that if the **RXD.AMOUNT** or **TXD.AMOUNT** register indicates longer data packets than set in MAXLEN, the frames sent to or received from the physical layer

will be incomplete. In that situation, in RX, the **OVERRUN** bit in the **FRAMESTATUS.RX** register will be set and an **RXERROR** event will be triggered.

**Important:** The **RXD.AMOUNT** and **TXD.AMOUNT** define a frame length in bytes and bits excluding start of frame (SoF), end of frame (EoF), and parity, but including CRC for **RXD.AMOUNT** only. Make sure to take potential additional bits into account when setting **MAXLEN**.

Only sending task **ENABLERXDATA** ensures that a new value in **PACKETPTR** pointing to the RX buffer in Data RAM is taken into account.

If **PACKETPTR** is not pointing to the Data RAM region, an EasyDMA transfer may result in a hard fault or RAM corruption. For more information about the different memory regions, see Chapter **Memory** on page 18.

The NFCT peripherals normally do alternative receive and transmit frames. Therefore, to prepare for the next frame, the **PACKETPTR**, **MAXLEN**, **TXD.FRAMECONFIG** and **TXD.AMOUNT** can be updated while the receive is in progress, and, similarly, the **PACKETPTR**, **MAXLEN** and **RXD.FRAMECONFIG** can be updated while the transmit is in progress. They can be updated and prepared for the next NFC frame immediately after the **STARTED** event of the current frame has been received. Updating the **TXD.FRAMECONFIG** and **TXD.AMOUNT** during the current transmit frame or updating **RXD.FRAMECONFIG** during current receive frame may cause unpredictable behaviour.

In accordance with *NFC Forum, NFC Digital Protocol Technical Specification*, the least significant bit (LSB) from the least significant byte (LSByte) is sent on air first. The bytes are stored in increasing order, starting at the lowest address in the EasyDMA buffer in RAM.

### 7.1.21.5 Frame assembler

The NFCT peripheral implements a frame assembler in hardware.

When the NFCT peripheral is in the **ACTIVE\_A** state, the software can decide to enter RX or TX mode. For RX, see **Frame disassembler** on page 287. For TX, the software must indicate the address of the source buffer in Data RAM and its size through programming the **PACKETPTR** and **MAXLEN** registers respectively, then issuing a **STARTTX** task.

**MAXLEN** must be set so that it matches the size of the frame to be sent.

The **STARTED** event indicates that the **PACKETPTR** and **MAXLEN** registers have been captured by the frame assembler EasyDMA.

When asserting the **STARTTX** task, the frame assembler module will start reading **TXD.AMOUNT.TXDATABYTES** bytes (plus one additional byte if **TXD.AMOUNT.TXDATABITS** > 0) from the RAM position set by the **PACKETPTR**.

The NFCT peripheral transmits the data as read from RAM, adding framing and the CRC calculated on the fly if set in **TXD.FRAMECONFIG**. The NFCT peripheral will take  $(8 * \text{TXD.AMOUNT.TXDATABYTES} + \text{TXD.AMOUNT.TXDATABITS})$  bits and assemble a frame according to the settings in **TXD.FRAMECONFIG**. Both short frames, standard frames, and bit-oriented SDD frames as specified in the *NFC Forum, NFC Digital Protocol Technical Specification* can be assembled by the correct setting of the **TXD.FRAMECONFIG** register.

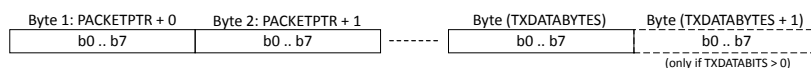
The bytes will be transmitted on air in the same order as they are read from RAM with a rising bit order within each byte, least significant bit (LSB) first. That is, b0 will be transmitted on air before b1, and so on. The bits read from RAM will be coded into symbols as defined in the *NFC Forum, NFC Digital Protocol Technical Specification*.

**Important:** Some NFC Forum documents, such as *NFC Forum*, *NFC Digital Protocol Technical Specification*, define bit numbering in a byte from b1 (LSB) to b8 (most significant bit (MSB)), while most other technical documents from the NFC Forum, and also the Nordic Semiconductor documentation, traditionally number them from b0 to b7. The present document uses the b0–b7 numbering scheme. Be aware of this when comparing the *NFC Forum*, *NFC Digital Protocol Technical Specification* to others.

The frame assembler can be configured in TXD.FRAMECONFIG to add SoF symbol, calculate and add parity bits, and calculate and add CRC to the data read from RAM when assembling the frame. The total frame will then be longer than what is defined by TXD.AMOUNT.TXDATABYTES. TXDATABITS. DISCARDMODE will select if the first bits in the first byte read from RAM or the last bits in the last byte read from RAM will be discarded if TXD.AMOUNT.TXDATABITS are not equal to zero. Note that if TXD.FRAMECONFIG.PARITY = Parity and TXD.FRAMECONFIG.DISCARDMODE=DiscardStart, a parity bit will be included after the non-complete first byte. No parity will be added after a non-complete last byte.

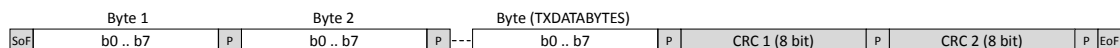
The frame assemble operation is illustrated in [Figure 90: Frame assemble illustration](#) on page 287 for different settings in TXD.FRAMECONFIG. All shaded bit fields are added by the frame assembler. Some of these bits are optional and appearances are configured in TXD.FRAMECONFIG. Note that the frames illustrated do not necessarily comply with the NFC specification. The figure is only to illustrate the behavior of the NFCT peripheral.

#### Data from RAM



#### Frame on air

PARITY = Parity  
TXDATABITS = 0  
CRCMODETX = CRC16TX



PARITY = Parity  
TXDATABITS = 4  
CRCMODETX = NoCRCTX  
DISCARDMODE = DiscardStart



PARITY = Parity  
TXDATABITS = 0  
CRCMODETX = NoCRCTX



Figure 90: Frame assemble illustration

The accurate timing for transmitting the frame on air is set using the frame timing controller settings.

### 7.1.21.6 Frame disassembler

The NFCT peripheral implements a frame disassembler in hardware.

When the NFCT peripheral is in the ACTIVE\_A state, the software can decide to enter RX or TX mode. For TX, see [Frame assembler](#) on page 286. For RX, the software must indicate the address and size of the destination buffer in Data RAM through programming the [PACKETPTR](#) and [MAXLEN](#) registers before issuing an [ENABLERXDATA](#) task.

The [STARTED](#) event indicates that the [PACKETPTR](#) and [MAXLEN](#) registers have been captured by the frame disassembler EasyDMA.

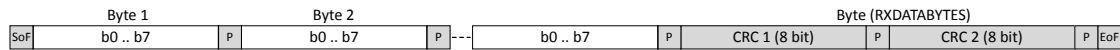
When an incoming frame starts, the [RXFRAMESTART](#) event will get issued and data will be written to the buffer in Data RAM. The frame disassembler will verify and remove any parity bits, start of frame (SoF) and

end of frame (EoF) symbols on the fly based on [RXD.FRAMECONFIG](#) register configuration. It will, however, verify and transfer the CRC bytes into RAM, if the CRC is enabled through [RXD.FRAMECONFIG](#).

When an EoF symbol is detected, the NFCT peripheral will assert the [RXFRAMEEND](#) event and write the [RXD.AMOUNT](#) register to indicate numbers of received bytes and bits in the data packet. The module does not interpret the content of the data received from the remote NFC device, except for SoF, EoF, parity, and CRC checking, as described above. The frame disassemble operation is illustrated below.

#### Frame on air

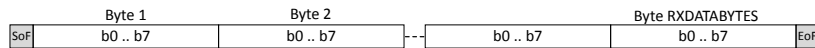
PARITY = Parity  
RXDATABITS = 0  
CRCMODERX = CRC16RX



PARITY = Parity  
CRCMODERX = NoCRCTR  
RXDATABITS = 4



PARITY = NoParity  
CRCMODERX = NoCRCRX  
RXDATABITS = 0



#### Data to RAM

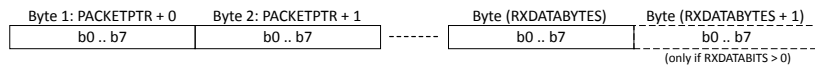


Figure 91: Frame disassemble illustration

Per NFC specification, the time between EoF to the next SoF can be as short as 86  $\mu$ s, and therefore care must be taken that PACKETPTR and MAXLEN are ready and ENABLERXDATA is issued on time after the end of previous frame. The use of a PPI shortcut from [TXFRAMEEND](#) to ENABLERXDATA is recommended.

### 7.1.21.7 Frame timing controller

The NFCT peripheral includes a frame timing controller that continuously keeps track of the number of the 13.56 MHz RF carrier clock periods since the end of the EoF of the last received frame.

The NFCT peripheral can be programmed to send a responding frame within a time window or at an exact count of RF carrier periods. In case of [FRAMEDELAYMODE](#) = Window, a [STARTTX](#) task triggered before the frame timing controller counter is equal to [FRAMEDELAYMIN](#) will force the transmission to halt until the counter is equal to [FRAMEDELAYMIN](#). If the counter is within [FRAMEDELAYMIN](#) and [FRAMEDELAYMAX](#) when the [STARTTX](#) task is triggered, the NFCT peripheral will start the transmission straight away. In case of [FRAMEDELAYMODE](#) = ExactVal, a [STARTTX](#) task triggered before the frame delay counter is equal to [FRAMEDELAYMAX](#) will halt the actual transmission start until the counter is equal to [FRAMEDELAYMAX](#).

In case of [FRAMEDELAYMODE](#) = WindowGrid, the behaviour is similar to the [FRAMEDELAYMODE](#) = Window, but the actual transmission between [FRAMEDELAYMIN](#) and [FRAMEDELAYMAX](#) starts on a bit grid as defined for NFC-A Listen frames (slot duration of 128 RF carrier periods).

An [ERROR](#) event (with [FRAMEDELAYTIMEOUT](#) cause in [ERRORSTATUS](#)) will be asserted if the frame timing controller counter reaches [FRAMEDELAYMAX](#) without any [STARTTX](#) task triggered. This may happen even when the response is not required as per *NFC Forum, NFC Digital Protocol Technical Specification*. Any commands handled by the automatic collision resolution that don't involve a response being generated may also result in an [ERROR](#) event (with [FRAMEDELAYTIMEOUT](#) cause in [ERRORSTATUS](#)). The [FRAMEDELAYMIN](#) and [FRAMEDELAYMAX](#) values shall only be updated before the [STARTTX](#) task is triggered. Failing to do so may cause unpredictable behaviour.

The frame timing controller operation is illustrated in [Figure 92: Frame timing controller \(FRAMEDELAYMODE=Window\)](#) on page 289. The frame timing controller automatically adjusts the frame timing counter based on the last received data bit according to NFC-A technology in the *NFC Forum, NFC Digital Protocol Technical Specification*.

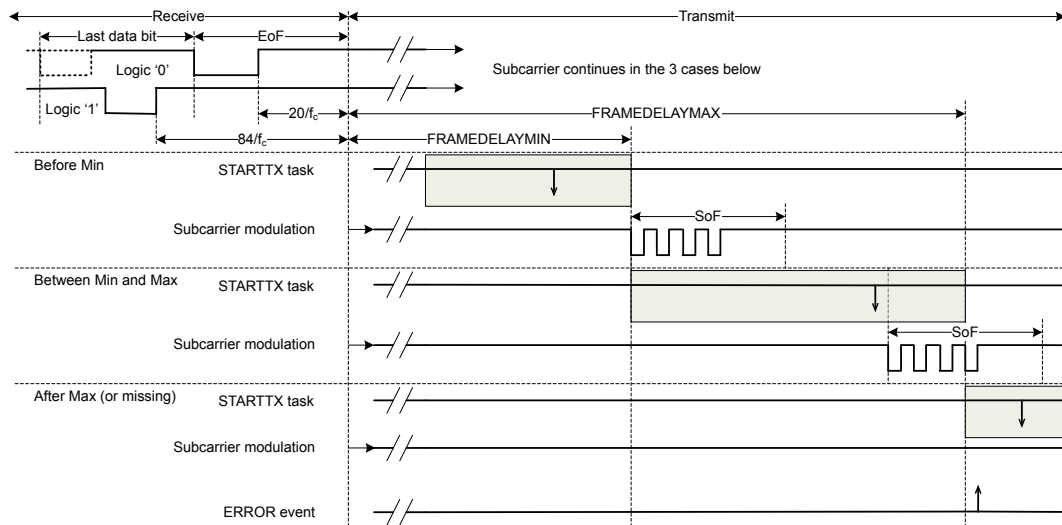


Figure 92: Frame timing controller (FRAMEDELAYMODE=Window)

### 7.1.21.8 Collision resolution

The NFCT peripheral implements an automatic collision resolution function as defined by the NFC Forum.

Automatic collision resolution is enabled by default, and it is recommended that the feature is used since it is power efficient and reduces the complexity of software handling the collision resolution sequence. This feature can be disabled through the MODE field in the [AUTOCOLRESCONFIG](#) register. When the automatic collision resolution is disabled, all commands will be sent over EasyDMA as defined in frame disassembler.

The [SENSRES](#) and [SELRES](#) registers need to be programmed upfront in order for the collision resolution to behave correctly. Depending on the NFCIDSIZE field in SENSRES, the following registers also need to be programmed upfront:

- NFCID1\_LAST if NFCID1SIZE=NFCID1Single (ID = 4 bytes);
- NFCID1\_2ND\_LAST and NFCID1\_LAST if NFCID1SIZE=NFCID1Double (ID = 7 bytes);
- NFCID1\_3RD\_LAST, NFCID1\_2ND\_LAST and NFCID1\_LAST if NFCID1SIZE=NFCID1Triple (ID = 10 bytes);

A pre-defined set of registers, NFC.TAGHEADER0..3, containing a valid NFCID1 value, is available in FICR and can be used by software to populate the NFCID1\_3RD\_LAST, NFCID1\_2ND\_LAST, and NFCID1\_LAST registers.

[Table 99: NFCID1 byte allocation \(top sent first on air\)](#) on page 290 explains the position of the ID bytes in NFCID1\_3RD\_LAST, NFCID1\_2ND\_LAST, and NFCID1\_LAST, depending on the ID size, and as compared to the definition used in the *NFC Forum, NFC Digital Protocol Technical Specification*.

| ID = 4 bytes | ID = 7 bytes        | ID = 10 bytes       |
|--------------|---------------------|---------------------|
| NFCID1_Q     |                     | nfcid1 <sub>0</sub> |
| NFCID1_R     |                     | nfcid1 <sub>1</sub> |
| NFCID1_S     |                     | nfcid1 <sub>2</sub> |
| NFCID1_T     | nfcid1 <sub>0</sub> | nfcid1 <sub>3</sub> |
| NFCID1_U     | nfcid1 <sub>1</sub> | nfcid1 <sub>4</sub> |
| NFCID1_V     | nfcid1 <sub>2</sub> | nfcid1 <sub>5</sub> |
| NFCID1_W     | nfcid1 <sub>0</sub> | nfcid1 <sub>6</sub> |
| NFCID1_X     | nfcid1 <sub>1</sub> | nfcid1 <sub>7</sub> |
| NFCID1_Y     | nfcid1 <sub>2</sub> | nfcid1 <sub>8</sub> |
| NFCID1_Z     | nfcid1 <sub>3</sub> | nfcid1 <sub>9</sub> |

Table 99: NFCID1 byte allocation (top sent first on air)

The hardware implementation can handle the states from IDLE to ACTIVE\_A automatically as defined in the *NFC Forum, NFC Activity Technical Specification*, and the other states are to be handled by software. The software keeps track of the state through events. The collision resolution will trigger an **AUTOCOLRESSTARTED** event when it has started. Reaching the ACTIVE\_A state is indicated by the **SELECTED** event.

If collision resolution fails, a **COLLISION** event is triggered. Note that errors occurring during automatic collision resolution may also cause **ERROR** and/or **RXERROR** events to be generated. Other events may also get generated. It is recommended that the software ignores any event except COLLISION, SELECTED and FIELDLOST during automatic collision resolution. Software shall also make sure that any unwanted SHORT or PPI shortcut is disabled during automatic collision resolution.

The automatic collision resolution will be restarted, if the packets are received with CRC or parity errors while in ACTIVE\_A state. The automatic collision resolution feature can be disabled while in ACTIVE\_A state to avoid this.

The SLP\_REQ is automatically handled by the NFCT peripheral when the automatic collision resolution is enabled. However, this results in an ERROR event (with FRAMEDELAYTIMEOUT cause in ERRORSTATUS) since the SLP\_REQ has no response. This error must be ignored until the SELECTED event is triggered and this error should be cleared by the software when the SELECTED event is triggered.

### 7.1.21.9 Antenna interface

In ACTIVATED state, an amplitude regulator will adjust the voltage swing on the antenna pins to a value that is within the  $V_{\text{swing}}$  limit.

Refer to **NFCT Electrical Specification** on page 317.

### 7.1.21.10 NFCT antenna recommendations

The NFCT antenna coil must be connected differential between **NFC1** and **NFC2** pins of the device.

Two external capacitors should be used to tune the resonance of the antenna circuit to 13.56 MHz.

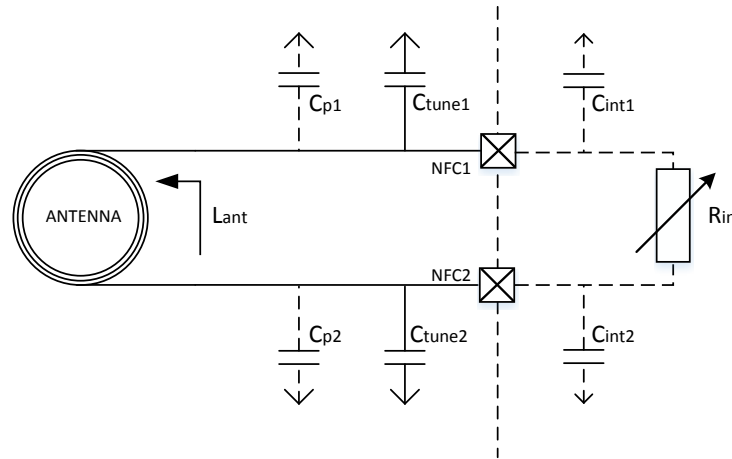


Figure 93: NFCT antenna recommendations

The required tuning capacitor value is given by the below equations:

$$C'_{tune} = \frac{1}{(2\pi \cdot 13.56 \text{ MHz})^2 \cdot L_{ant}} \quad \text{where } C'_{tune} = \frac{1}{2} \cdot (C_p + C_{int} + C_{tune})$$

$$\text{and } C_{tune1} = C_{tune2} = C_{tune} \quad C_{p1} = C_{p2} = C_p \quad C_{int1} = C_{int2} = C_{int}$$

$$C_{tune} = \frac{2}{(2\pi \cdot 13.56 \text{ MHz})^2 \cdot L_{ant}} - C_p - C_{int}$$

An antenna inductance of  $L_{ant} = 2 \mu\text{H}$  will give tuning capacitors in the range of 130 pF on each pin. The total capacitance on **NFC1** and **NFC2** must be matched.

#### 7.1.21.11 Battery protection

If the antenna is exposed to a strong NFC field, current may flow in the opposite direction on the supply due to parasitic diodes and ESD structures.

If the battery used does not tolerate return current, a series diode must be placed between the battery and the device in order to protect the battery.

#### 7.1.21.12 References

NFC Forum, NFC Analog Specification version 1.0, [www.nfc-forum.org](http://www.nfc-forum.org)

NFC Forum, NFC Digital Protocol Technical Specification version 1.1, [www.nfc-forum.org](http://www.nfc-forum.org)

NFC Forum, NFC Activity Technical Specification version 1.1, [www.nfc-forum.org](http://www.nfc-forum.org)

## 7.1.21.13 Registers

| Base address | Domain      | Peripheral | Instance  | Secure mapping | DMA security | Description                  | Configuration |
|--------------|-------------|------------|-----------|----------------|--------------|------------------------------|---------------|
| 0x5002D000   | APPLICATION | NFCT       | NFCT : S  | US             | SA           | Near field communication tag |               |
| 0x4002D000   |             |            | NFCT : NS |                |              |                              |               |

Table 100: Instances

| Register               | Offset | Security | Description                                                                                                        |
|------------------------|--------|----------|--------------------------------------------------------------------------------------------------------------------|
| TASKS_ACTIVATE         | 0x000  |          | Activate NFCT peripheral for incoming and outgoing frames, change state to activated                               |
| TASKS_DISABLE          | 0x004  |          | Disable NFCT peripheral                                                                                            |
| TASKS_SENSE            | 0x008  |          | Enable NFC sense field mode, change state to sense mode                                                            |
| TASKS_STARTTX          | 0x00C  |          | Start transmission of an outgoing frame, change state to transmit                                                  |
| TASKS_ENABLERXDATA     | 0x01C  |          | Initializes the EasyDMA for receive.                                                                               |
| TASKS_GOIDLE           | 0x024  |          | Force state machine to IDLE state                                                                                  |
| TASKS_GOSLEEP          | 0x028  |          | Force state machine to SLEEP_A state                                                                               |
| SUBSCRIBE_ACTIVATE     | 0x080  |          | Subscribe configuration for task <a href="#">ACTIVATE</a>                                                          |
| SUBSCRIBE_DISABLE      | 0x084  |          | Subscribe configuration for task <a href="#">DISABLE</a>                                                           |
| SUBSCRIBE_SENSE        | 0x088  |          | Subscribe configuration for task <a href="#">SENSE</a>                                                             |
| SUBSCRIBE_STARTTX      | 0x08C  |          | Subscribe configuration for task <a href="#">STARTTX</a>                                                           |
| SUBSCRIBE_ENABLERXDATA | 0x09C  |          | Subscribe configuration for task <a href="#">ENABLERXDATA</a>                                                      |
| SUBSCRIBE_GOIDLE       | 0x0A4  |          | Subscribe configuration for task <a href="#">GOIDLE</a>                                                            |
| SUBSCRIBE_GOSLEEP      | 0x0A8  |          | Subscribe configuration for task <a href="#">GOSLEEP</a>                                                           |
| EVENTS_READY           | 0x100  |          | The NFCT peripheral is ready to receive and send frames                                                            |
| EVENTS_FIELDDETECTED   | 0x104  |          | Remote NFC field detected                                                                                          |
| EVENTS_FIELDLOST       | 0x108  |          | Remote NFC field lost                                                                                              |
| EVENTS_TXFRAMESTART    | 0x10C  |          | Marks the start of the first symbol of a transmitted frame                                                         |
| EVENTS_TXFRAMEEND      | 0x110  |          | Marks the end of the last transmitted on-air symbol of a frame                                                     |
| EVENTS_RXFRAMESTART    | 0x114  |          | Marks the end of the first symbol of a received frame                                                              |
| EVENTS_RXFRAMEEND      | 0x118  |          | Received data has been checked (CRC, parity) and transferred to RAM, and EasyDMA has ended accessing the RX buffer |
| EVENTS_ERROR           | 0x11C  |          | NFC error reported. The ERRORSTATUS register contains details on the source of the error.                          |
| EVENTS_RXERROR         | 0x128  |          | NFC RX frame error reported. The FRAMESTATUS.RX register contains details on the source of the error.              |
| EVENTS_ENDRX           | 0x12C  |          | RX buffer (as defined by PACKETPTR and MAXLEN) in Data RAM full.                                                   |
| EVENTS_ENDTX           | 0x130  |          | Transmission of data in RAM has ended, and EasyDMA has ended accessing the TX buffer                               |
| EVENTS_AUTOCOLRESSTAR  | 0x138  |          | Auto collision resolution process has started                                                                      |
| EVENTS_COLLISION       | 0x148  |          | NFC auto collision resolution error reported.                                                                      |
| EVENTS_SELECTED        | 0x14C  |          | NFC auto collision resolution successfully completed                                                               |
| EVENTS_STARTED         | 0x150  |          | EasyDMA is ready to receive or send frames.                                                                        |
| PUBLISH_READY          | 0x180  |          | Publish configuration for event <a href="#">READY</a>                                                              |
| PUBLISH_FIELDDETECTED  | 0x184  |          | Publish configuration for event <a href="#">FIELDDETECTED</a>                                                      |
| PUBLISH_FIELDLOST      | 0x188  |          | Publish configuration for event <a href="#">FIELDLOST</a>                                                          |
| PUBLISH_TXFRAMESTART   | 0x18C  |          | Publish configuration for event <a href="#">TXFRAMESTART</a>                                                       |
| PUBLISH_TXFRAMEEND     | 0x190  |          | Publish configuration for event <a href="#">TXFRAMEEND</a>                                                         |
| PUBLISH_RXFRAMESTART   | 0x194  |          | Publish configuration for event <a href="#">RXFRAMESTART</a>                                                       |
| PUBLISH_RXFRAMEEND     | 0x198  |          | Publish configuration for event <a href="#">RXFRAMEEND</a>                                                         |
| PUBLISH_ERROR          | 0x19C  |          | Publish configuration for event <a href="#">ERROR</a>                                                              |
| PUBLISH_RXERROR        | 0x1A8  |          | Publish configuration for event <a href="#">RXERROR</a>                                                            |
| PUBLISH_ENDRX          | 0x1AC  |          | Publish configuration for event <a href="#">ENDRX</a>                                                              |



| Register                | Offset | Security | Description                                                                                                         |
|-------------------------|--------|----------|---------------------------------------------------------------------------------------------------------------------|
| PUBLISH_ENDTX           | 0x1B0  |          | Publish configuration for event <a href="#">ENDTX</a>                                                               |
| PUBLISH_AUTOCOLRESSTART | 0x1B8  |          | Publish configuration for event <a href="#">AUTOCOLRESSTARTED</a>                                                   |
| PUBLISH_COLLISION       | 0x1C8  |          | Publish configuration for event <a href="#">COLLISION</a>                                                           |
| PUBLISH_SELECTED        | 0x1CC  |          | Publish configuration for event <a href="#">SELECTED</a>                                                            |
| PUBLISH_STARTED         | 0x1D0  |          | Publish configuration for event <a href="#">STARTED</a>                                                             |
| SHORTS                  | 0x200  |          | Shortcuts between local events and tasks                                                                            |
| INTEN                   | 0x300  |          | Enable or disable interrupt                                                                                         |
| INTENSET                | 0x304  |          | Enable interrupt                                                                                                    |
| INTENCLR                | 0x308  |          | Disable interrupt                                                                                                   |
| ERRORSTATUS             | 0x404  |          | NFC Error Status register                                                                                           |
| FRAMESTATUS.RX          | 0x40C  |          | Result of last incoming frame                                                                                       |
| NFCTAGSTATE             | 0x410  |          | NfcTag state register                                                                                               |
| SLEEPSTATE              | 0x420  |          | Sleep state during automatic collision resolution                                                                   |
| FIELDPRESENT            | 0x43C  |          | Indicates the presence or not of a valid field                                                                      |
| FRAMEDELAYMIN           | 0x504  |          | Minimum frame delay                                                                                                 |
| FRAMEDELAYMAX           | 0x508  |          | Maximum frame delay                                                                                                 |
| FRAMEDELAYMODE          | 0x50C  |          | Configuration register for the Frame Delay Timer                                                                    |
| PACKETPTR               | 0x510  |          | Packet pointer for TXD and RXD data storage in Data RAM                                                             |
| MAXLEN                  | 0x514  |          | Size of the RAM buffer allocated to TXD and RXD data storage each                                                   |
| TXD.FRAMECONFIG         | 0x518  |          | Configuration of outgoing frames                                                                                    |
| TXD.AMOUNT              | 0x51C  |          | Size of outgoing frame                                                                                              |
| RXD.FRAMECONFIG         | 0x520  |          | Configuration of incoming frames                                                                                    |
| RXD.AMOUNT              | 0x524  |          | Size of last incoming frame                                                                                         |
| MODULATIONCTRL          | 0x52C  |          | Enables the modulation output to a GPIO pin which can be connected to a second external antenna.                    |
| MODULATIONPSEL          | 0x538  |          | Pin select for Modulation control.                                                                                  |
| NFCID1_LAST             | 0x590  |          | Last NFCID1 part (4, 7 or 10 bytes ID)                                                                              |
| NFCID1_2ND_LAST         | 0x594  |          | Second last NFCID1 part (7 or 10 bytes ID)                                                                          |
| NFCID1_3RD_LAST         | 0x598  |          | Third last NFCID1 part (10 bytes ID)                                                                                |
| AUTOCOLRESCONFIG        | 0x59C  |          | Controls the auto collision resolution function. This setting must be done before the NFCT peripheral is activated. |
| SENSRES                 | 0x5A0  |          | NFC-A SENS_RES auto-response settings                                                                               |
| SELRES                  | 0x5A4  |          | NFC-A SEL_RES auto-response settings                                                                                |

Table 101: Register overview

### 7.1.21.13.1 TASKS\_ACTIVATE

Address offset: 0x000

Activate NFCT peripheral for incoming and outgoing frames, change state to activated

|                  |            |                |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |                |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |                |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |                |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID       | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W          | TASKS_ACTIVATE |       | Activate NFCT peripheral for incoming and outgoing frames, change state to activated  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Trigger        | 1     | Trigger task                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.21.13.2 TASKS\_DISABLE

Address offset: 0x004

Disable NFCT peripheral

|                  |            |               |          |   |       |              |             |                         |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|---------------|----------|---|-------|--------------|-------------|-------------------------|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |               |          |   |       |              |             |                         |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |               |          |   |       |              |             |                         |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |   |
| Reset 0x00000000 |            |               |          |   |       |              |             |                         |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |               | Value ID |   | Value |              | Description |                         |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_DISABLE |          |   |       |              |             | Disable NFCT peripheral |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Trigger       |          | 1 |       | Trigger task |             |                         |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.21.13.3 TASKS\_SENSE

Address offset: 0x008

Enable NFC sense field mode, change state to sense mode

|                  |            |             |          |   |       |              |             |                                                         |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-------------|----------|---|-------|--------------|-------------|---------------------------------------------------------|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |             |          |   |       |              |             |                                                         |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |             |          |   |       |              |             |                                                         |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |
| Reset 0x00000000 |            |             |          |   |       |              |             |                                                         |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |             | Value ID |   | Value |              | Description |                                                         |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_SENSE |          |   |       |              |             | Enable NFC sense field mode, change state to sense mode |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Trigger     |          | 1 |       | Trigger task |             |                                                         |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.21.13.4 TASKS\_STARTTX

Address offset: 0x00C

Start transmission of an outgoing frame, change state to transmit

|                  |      |               |       |                                                                                       |       |                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|---------------|-------|---------------------------------------------------------------------------------------|-------|-------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |               |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |               |       | A                                                                                     |       |                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |               |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |       |                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field         | Value | ID                                                                                    | Value | Description                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W    | TASKS_STARTTX |       |                                                                                       |       | Start transmission of an outgoing frame, change state to transmit |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Trigger       | 1     |                                                                                       |       | Trigger task                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.21.13.5 TASKS\_ENABLERXDATA

Address offset: 0x01C

Initializes the EasyDMA for receive.

|                  |            |                                                                                       |  |       |  |                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|---------------------------------------------------------------------------------------|--|-------|--|--------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |       |  |                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            | A                                                                                     |  |       |  |                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |  |       |  |                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID                                                                              |  | Value |  | Description                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W          | TASKS_ENABLERXDATA                                                                    |  | 1     |  | Initializes the EasyDMA for receive. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Trigger                                                                               |  | 1     |  | Trigger task                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.21.13.6 TASKS\_GOIDLE

Address offset: 0x024

Force state machine to IDLE state

|                  |            |              |          |         |       |  |              |                                   |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------------|----------|---------|-------|--|--------------|-----------------------------------|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |              |          |         |       |  |              |                                   |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |              |          |         |       |  |              |                                   |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |   |
| Reset 0x00000000 |            |              |          |         |       |  |              |                                   |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |              | Value ID |         | Value |  | Description  |                                   |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_GOIDLE |          |         |       |  |              | Force state machine to IDLE state |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |              |          | Trigger | 1     |  | Trigger task |                                   |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.21.13.7 TASKS\_GOSLEEP

Address offset: 0x028

Force state machine to SLEEP\_A state

|                  |            |               |  |          |   |  |       |  |  |             |                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|---------------|--|----------|---|--|-------|--|--|-------------|--------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |               |  |          |   |  |       |  |  | 31          | 30                                   | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |               |  |          |   |  |       |  |  |             |                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |   |
| Reset 0x00000000 |            |               |  |          |   |  |       |  |  | 0           | 0                                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |               |  | Value ID |   |  | Value |  |  | Description |                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_GOSLEEP |  |          |   |  |       |  |  |             | Force state machine to SLEEP_A state |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Trigger       |  |          | 1 |  |       |  |  |             | Trigger task                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.21.13.8 SUBSCRIBE\_ACTIVATE

Address offset: 0x080

Subscribe configuration for task [ACTIVATE](#)

|                  |      |       |          |                                                                                       |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|-------|----------|---------------------------------------------------------------------------------------|----------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|-----------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |       |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |       |          | B                                                                                     |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |       |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field | Value    | ID                                                                                    | Value                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  | Description                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW   | CHIDX |          |                                                                                       | [255..0]             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  | Channel that task <span>ACTIVATE</span> will subscribe to |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW   | EN    |          |                                                                                       |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Disabled | 0                                                                                     | Disable subscription |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Enabled  | 1                                                                                     | Enable subscription  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.21.13.9 SUBSCRIBE\_DISABLE

Address offset: 0x084

Subscribe configuration for task [DISABLE](#)

|                  |            |          |          |    |                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|----|----------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          | 31       | 30 | 29                                                       | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |          | B        |    |                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |          | 0        |    |                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID | Value    |    | Description                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | CHIDX    | [255..0] |    | Channel that task <span>DISABLE</span> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW         | EN       |          |    |                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        |    | Disable subscription                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        |    | Enable subscription                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.21.13.10 SUBSCRIBE\_SENSE

Address offset: 0x088

Subscribe configuration for task [SENSE](#)

|                  |      |       |          |    |                      |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
|------------------|------|-------|----------|----|----------------------|--------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|--|
| Bit number       |      |       |          | 31 | 30                   | 29                                               | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |  |
| ID               |      |       |          | B  |                      |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   | A | A | A | A | A | A |  |
| Reset 0x00000000 |      |       |          | 0  | 0                    | 0                                                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |  |
| ID               | Acce | Field | Value    | ID | Value                | Description                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| A                | RW   | CHIDX |          |    | [255..0]             | Channel that task <b>SENSE</b> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| B                | RW   | EN    |          |    |                      |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |       | Disabled | 0  | Disable subscription |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |       | Enabled  | 1  | Enable subscription  |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |  |

### 7.1.21.13.11 SUBSCRIBE\_STARTTX

Address offset: 0x08C

Subscribe configuration for task **STARTTX**

|                  |            |          |          |   |       |                      |             |                                                    |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|---|-------|----------------------|-------------|----------------------------------------------------|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          |   |       |                      |             |                                                    |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |          |          |   |       |                      |             |                                                    |  | B  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  | A  | A | A | A | A | A | A |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |          |          |   |       |                      |             |                                                    |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |          | Value ID |   | Value |                      | Description |                                                    |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | CHIDX    |          |   |       | [255..0]             |             | Channel that task <b>STARTTX</b> will subscribe to |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW         | EN       |          |   |       |                      |             |                                                    |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled |          | 0 |       | Disable subscription |             |                                                    |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  |          | 1 |       | Enable subscription  |             |                                                    |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.21.13.12 SUBSCRIBE\_ENABLERXDATA

Address offset: 0x09C

Subscribe configuration for task **ENABLERXDATA**

|                  |            |       |          |          |                      |                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-------|----------|----------|----------------------|---------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |       |          | 31       | 30                   | 29                                                      | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |       |          | B        |                      |                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   | A | A | A | A | A | A |
| Reset 0x00000000 |            |       |          | 0        | 0                    | 0                                                       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce Field |       | Value ID | Value    |                      | Description                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | CHIDX |          | [255..0] |                      | Channel that task <b>ENABLERXDATA</b> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW         | EN    |          |          |                      |                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |       | Disabled | 0        | Disable subscription |                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |       | Enabled  | 1        | Enable subscription  |                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.21.13.13 SUBSCRIBE\_GOIDLE

Address offset: 0x0A4

Subscribe configuration for task **GOIDLE**

|                  |            |          |          |                                                                         |    |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|-------------------------------------------------------------------------|----|---------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                                                                      | 30 | 29                                                | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |          |          | B                                                                       |    |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |    |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field |          | Value ID | Value                                                                   |    | Description                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | CHIDX    |          | [255..0]                                                                |    | Channel that task <b>GOIDLE</b> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW         | EN       |          |                                                                         |    |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        | Disable subscription                                                    |    |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        | Enable subscription                                                     |    |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.21.13.14 SUBSCRIBE\_GOSLEEP

Address offset: 0x0A8

Subscribe configuration for task **GOSLEEP**

|                  |            |          |                                                                                       |                      |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|----------------------|----------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                      |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |          | B                                                                                     |                      |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                   |                      |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 |                      | Description                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                              |                      | Channel that task <b>GOSLEEP</b> will subscribe to |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |                                                                                       |                      |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Disable subscription |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Enable subscription  |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

### 7.1.21.13.15 EVENTS\_READY

Address offset: 0x100

The NFCT peripheral is ready to receive and send frames

|                  |                 |              |                                                                                       |                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|-----------------|--------------|---------------------------------------------------------------------------------------|---------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |                 |              | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |                 |              | A                                                                                     |                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |                 |              | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field      | Value ID     | Value                                                                                 | Description                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW EVENTS_READY |              |                                                                                       | The NFCT peripheral is ready to receive and send frames |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                 | NotGenerated | 0                                                                                     | Event not generated                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                 | Generated    | 1                                                                                     | Event generated                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.21.13.16 EVENTS\_FIELDDETECTED

Address offset: 0x104

Remote NFC field detected

|                  |            |                      |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------------------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |                      |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |                      |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |                      |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID             | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | EVENTS_FIELDDETECTED |       | Remote NFC field detected                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | NotGenerated         | 0     | Event not generated                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Generated            | 1     | Event generated                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.21.13.17 EVENTS\_FIELDLOST

Address offset: 0x108

Remote NFC field lost

|                  |            |                  |       |                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|------------------|-------|-----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                  |       | 31                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |                  |       |                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |
| Reset 0x00000000 |            |                  |       | 0                     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |
| ID               | Acce Field | Value ID         | Value | Description           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | EVENTS_FIELDLOST |       | Remote NFC field lost |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | NotGenerated     | 0     | Event not generated   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Generated        | 1     | Event generated       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.21.13.18 EVENTS\_TXFRAMESTART

Address offset: 0x10C

Marks the start of the first symbol of a transmitted frame

|                  |            |                     |       |    |                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|------------------|------------|---------------------|-------|----|------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| Bit number       |            |                     | 31    | 30 | 29                                                         | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| ID               |            |                     |       |    |                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | A |  |
| Reset 0x00000000 |            |                     | 0     | 0  | 0                                                          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |
| ID               | Acce Field | Value ID            | Value |    | Description                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| A                | RW         | EVENTS_TXFRAMESTART |       |    | Marks the start of the first symbol of a transmitted frame |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | NotGenerated        | 0     |    | Event not generated                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | Generated           | 1     |    | Event generated                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

### 7.1.21.13.19 EVENTS\_TXFRAMEEND

Address offset: 0x110

Marks the end of the last transmitted on-air symbol of a frame

|                  |            |                   |       |    |                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|------------------|------------|-------------------|-------|----|----------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| Bit number       |            |                   | 31    | 30 | 29                                                             | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| ID               |            |                   | A     |    |                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| Reset 0x00000000 |            |                   | 0     | 0  | 0                                                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |
| ID               | Acce Field | Value ID          | Value |    | Description                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| A                | RW         | EVENTS_TXFRAMEEND |       |    | Marks the end of the last transmitted on-air symbol of a frame |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | NotGenerated      | 0     |    | Event not generated                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | Generated         | 1     |    | Event generated                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

### 7.1.21.13.20 EVENTS\_RXFRAMESTART

Address offset: 0x114

Marks the end of the first symbol of a received frame

|                  |            |                     |       |                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|---------------------|-------|-------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                     |       | 31                                                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |                     |       | A                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |                     |       | 0                                                     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID            | Value | Description                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | EVENTS_RXFRAMESTART |       | Marks the end of the first symbol of a received frame |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | NotGenerated        | 0     | Event not generated                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Generated           | 1     | Event generated                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.21.13.21 EVENTS\_RXFRAMEEND

Address offset: 0x118

Received data has been checked (CRC, parity) and transferred to RAM, and EasyDMA has ended accessing the RX buffer

|                  |            |  |                   |  |       |  |                                                                                                                    |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|-------------------|--|-------|--|--------------------------------------------------------------------------------------------------------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |                   |  |       |  |                                                                                                                    |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |  |                   |  |       |  |                                                                                                                    |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |
| Reset 0x00000000 |            |  |                   |  |       |  |                                                                                                                    |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID          |  | Value |  | Description                                                                                                        |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         |  | EVENTS_RXFRAMEEND |  |       |  | Received data has been checked (CRC, parity) and transferred to RAM, and EasyDMA has ended accessing the RX buffer |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | NotGenerated      |  | 0     |  | Event not generated                                                                                                |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Generated         |  | 1     |  | Event generated                                                                                                    |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.21.13.22 EVENTS\_ERROR

Address offset: 0x11C

NFC error reported. The ERRORSTATUS register contains details on the source of the error.

|                  |      |              |              |                                                                         |                                                                                           |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|------------------|------|--------------|--------------|-------------------------------------------------------------------------|-------------------------------------------------------------------------------------------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|--|
| Bit number       |      |              |              | 31                                                                      | 30                                                                                        | 29          | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |
| ID               |      |              |              | A                                                                       |                                                                                           |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| Reset 0x00000000 |      |              |              | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |                                                                                           |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| ID               | Acce | Field        | Value        | ID                                                                      | Value                                                                                     | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| A                | RW   | EVENTS_ERROR |              |                                                                         | NFC error reported. The ERRORSTATUS register contains details on the source of the error. |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |      |              | NotGenerated | 0                                                                       | Event not generated                                                                       |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |      |              | Generated    | 1                                                                       | Event generated                                                                           |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |

### 7.1.21.13.23 EVENTS\_RXERROR

Address offset: 0x128

NFC RX frame error reported. The FRAMESTATUS.RX register contains details on the source of the error.

|                  |            |                |       |                                                                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|------------------|------------|----------------|-------|-------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|--|
| Bit number       |            |                | 31    | 30                                                                                                    | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |
| ID               |            |                | A     |                                                                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| Reset 0x00000000 |            |                | 0     | 0                                                                                                     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |  |
| ID               | Acce Field | Value ID       | Value | Description                                                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| A                | RW         | EVENTS_RXERROR |       | NFC RX frame error reported. The FRAMESTATUS.RX register contains details on the source of the error. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | NotGenerated   | 0     | Event not generated                                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | Generated      | 1     | Event generated                                                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |

### 7.1.21.13.24 EVENTS\_ENDRX

Address offset: 0x12C

RX buffer (as defined by PACKETPTR and MAXLEN) in Data RAM full.

|                  |            |  |              |  |       |  |                                                                  |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|--------------|--|-------|--|------------------------------------------------------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |              |  |       |  |                                                                  |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |  |              |  |       |  |                                                                  |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |   |
| Reset 0x00000000 |            |  |              |  |       |  |                                                                  |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID     |  | Value |  | Description                                                      |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         |  | EVENTS_ENDRX |  |       |  | RX buffer (as defined by PACKETPTR and MAXLEN) in Data RAM full. |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | NotGenerated |  | 0     |  | Event not generated                                              |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Generated    |  | 1     |  | Event generated                                                  |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.21.13.25 EVENTS\_ENDTX

Address offset: 0x130

Transmission of data in RAM has ended, and EasyDMA has ended accessing the TX buffer

|                  |            |  |              |  |       |  |                                                                                      |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|--------------|--|-------|--|--------------------------------------------------------------------------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |              |  |       |  |                                                                                      |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |  |              |  |       |  |                                                                                      |  |  | A  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |              |  |       |  |                                                                                      |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID     |  | Value |  | Description                                                                          |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         |  | EVENTS_ENDTX |  |       |  | Transmission of data in RAM has ended, and EasyDMA has ended accessing the TX buffer |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | NotGenerated |  | 0     |  | Event not generated                                                                  |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Generated    |  | 1     |  | Event generated                                                                      |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.21.13.26 EVENTS\_AUTOCOLRESSTARTED

Address offset: 0x138

Auto collision resolution process has started

|                  |      |                          |              |    |                                               |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|------------------|------|--------------------------|--------------|----|-----------------------------------------------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|---|
| Bit number       |      |                          |              | 31 | 30                                            | 29          | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |   |
| ID               |      |                          |              |    |                                               |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | A |
| Reset 0x00000000 |      |                          |              | 0  | 0                                             | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |   |
| ID               | Acce | Field                    | Value        | ID | Value                                         | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
| A                | RW   | EVENTS_AUTOCOLRESSTARTED |              |    | Auto collision resolution process has started |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |      |                          | NotGenerated | 0  | Event not generated                           |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |      |                          | Generated    | 1  | Event generated                               |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |

### 7.1.21.13.27 EVENTS\_COLLISION

Address offset: 0x148

NFC auto collision resolution error reported.

|                  |            |                  |       |                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|------------------|-------|-----------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                  |       | 31                                            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |                  |       | A                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |                  |       | 0                                             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID         | Value | Description                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | EVENTS_COLLISION |       | NFC auto collision resolution error reported. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | NotGenerated     | 0     | Event not generated                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Generated        | 1     | Event generated                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |



### 7.1.21.13.28 EVENTS\_SELECTED

Address offset: 0x14C

NFC auto collision resolution successfully completed

|                  |            |                 |       |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|------------------|------------|-----------------|-------|------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|---|
| Bit number       |            |                 |       | 31                                                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |   |
| ID               |            |                 |       |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  | A |
| Reset 0x00000000 |            |                 |       | 0                                                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |   |
| ID               | Acce Field | Value ID        | Value | Description                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
| A                | RW         | EVENTS_SELECTED |       | NFC auto collision resolution successfully completed |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|                  |            | NotGenerated    | 0     | Event not generated                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|                  |            | Generated       | 1     | Event generated                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |

### 7.1.21.13.29 EVENTS\_STARTED

Address offset: 0x150

EasyDMA is ready to receive or send frames.

|                  |                   |              |       |                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|------------------|-------------------|--------------|-------|---------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|---|
| Bit number       |                   |              |       | 31                                          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |   |
| ID               |                   |              |       |                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  | A |
| Reset 0x00000000 |                   |              |       | 0                                           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |   |
| ID               | Acce Field        | Value ID     | Value | Description                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
| A                | RW EVENTS_STARTED |              |       | EasyDMA is ready to receive or send frames. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|                  |                   | NotGenerated | 0     | Event not generated                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|                  |                   | Generated    | 1     | Event generated                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |

### 7.1.21.13.30 PUBLISH\_READY

Address offset: 0x180

Publish configuration for event [READY](#)

|                  |            |          |          |                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|--------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                                                     | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |          |          | B                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |          | 0                                                      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce Field | Value ID | Value    | Description                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] | Channel that event <span>READY</span> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        | Disable publishing                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        | Enable publishing                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.21.13.31 PUBLISH\_FIELDDETECTED

Address offset: 0x184

Publish configuration for event [FIELDDETECTED](#)

|                  |            |          |          |                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|----------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                                                       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |          |          | B                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |          | 0                                                        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |
| ID               | Acce Field | Value ID | Value    | Description                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] | Channel that event <b>FIELDDETECTED</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        | Disable publishing                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        | Enable publishing                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.21.13.32 PUBLISH\_FIELDLOST

Address offset: 0x188

Publish configuration for event **FIELDLOST**

|                  |            |          |          |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                                                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |          |          | B                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |          | 0                                                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |
| ID               | Acce Field | Value ID | Value    | Description                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] | Channel that event <b>FIELDLOST</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        | Disable publishing                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        | Enable publishing                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.21.13.33 PUBLISH\_TXFRAMESTART

Address offset: 0x18C

Publish configuration for event **TXFRAMESTART**

|                  |            |  |          |          |    |                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|----------|----|---------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31       | 30 | 29                                                      | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |  |          | B        |    |                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |          | 0        | 0  | 0                                                       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce Field |  | Value ID | Value    |    | Description                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          | [255..0] |    | Channel that event <b>TXFRAMESTART</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |          |    |                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled | 0        |    | Disable publishing                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  | 1        |    | Enable publishing                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.21.13.34 PUBLISH\_TXFRAMEEND

Address offset: 0x190

Publish configuration for event **TXFRAMEEND**

|                  |            |  |          |  |          |  |                                                       |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|--|----------|--|-------------------------------------------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          |  |          |  |                                                       |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |
| ID               |            |  |          |  |          |  |                                                       |  |  | B  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  |    |    |    |   |   |   |   |   |   | A | A | A | A | A | A | A |   |
| Reset 0x00000000 |            |  |          |  |          |  |                                                       |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID |  | Value    |  | Description                                           |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          |  | [255..0] |  | Channel that event <b>TXFRAMEEND</b> will publish to. |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |  |          |  |                                                       |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled |  | 0        |  | Disable publishing                                    |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  |  | 1        |  | Enable publishing                                     |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |



|                  |            |          |          |                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|----------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                                                       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |          |          | B                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |          | 0                                                        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce Field | Value ID | Value    | Description                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] | Channel that event <span>RXERROR</span> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        | Disable publishing                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        | Enable publishing                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.21.13.39 PUBLISH\_ENDRX

Address offset: 0x1AC

Publish configuration for event **ENDRX**

|                  |            |  |          |          |    |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|----------|----|--------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31       | 30 | 29                                               | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |  |          | B        |    |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   |   |   |   |   |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |          | 0        |    |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID | Value    |    | Description                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          | [255..0] |    | Channel that event <b>ENDRX</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |          |    |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled | 0        |    | Disable publishing                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  | 1        |    | Enable publishing                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.21.13.40 PUBLISH\_ENDTX

Address offset: 0x1B0

Publish configuration for event **ENDTX**

|                  |            |          |          |                                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|-------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                                                                      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |          |          | B                                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field | Value ID | Value    | Description                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] | Channel that event <b>ENDTX</b> will publish to.                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |                                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        | Disable publishing                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        | Enable publishing                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.21.13.41 PUBLISH\_AUTOCOLRESSTARTED

Address offset: 0x1B8

Publish configuration for event **AUTOCOLRESSTARTED**

|                  |            |  |          |          |                    |                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|----------|--------------------|-------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31       | 30                 | 29                                                    | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |  |          | B        |                    |                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   |   |   |   |   |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |          | 0        |                    |                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID | Value    |                    | Description                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          | [255..0] |                    | Channel that event AUTOCOLRESSTARTED will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |          |                    |                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled | 0        | Disable publishing |                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  | 1        | Enable publishing  |                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |



| Bit number       |      |                         | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |   |  |   |  |
|------------------|------|-------------------------|---------------------------------------------------------------------------------------|-------|-----------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|--|---|--|---|--|
| ID               |      |                         |                                                                                       |       |                                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | F |  | B |  | A |  |
| Reset 0x00000000 |      |                         | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |       |                                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |   |  |   |  |
| ID               | Acce | Field                   | Value ID                                                                              | Value | Description                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |   |  |   |  |
| A                | RW   | FIELDDETECTED_ACTIVATE  |                                                                                       |       | Shortcut between event <a href="#">FIELDDETECTED</a> and task <a href="#">ACTIVATE</a>  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |   |  |   |  |
|                  |      |                         | Disabled                                                                              | 0     | Disable shortcut                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |   |  |   |  |
|                  |      |                         | Enabled                                                                               | 1     | Enable shortcut                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |   |  |   |  |
| B                | RW   | FIELDLOST_SENSE         |                                                                                       |       | Shortcut between event <a href="#">FIELDLOST</a> and task <a href="#">SENSE</a>         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |   |  |   |  |
|                  |      |                         | Disabled                                                                              | 0     | Disable shortcut                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |   |  |   |  |
|                  |      |                         | Enabled                                                                               | 1     | Enable shortcut                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |   |  |   |  |
| F                | RW   | TXFRAMEEND_ENABLERXDATA |                                                                                       |       | Shortcut between event <a href="#">TXFRAMEEND</a> and task <a href="#">ENABLERXDATA</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |   |  |   |  |
|                  |      |                         | Disabled                                                                              | 0     | Disable shortcut                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |   |  |   |  |
|                  |      |                         | Enabled                                                                               | 1     | Enable shortcut                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |   |  |   |  |

### 7.1.21.13.46 INTEN

Address offset: 0x300

Enable or disable interrupt

| Bit number       |      |               |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |         |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |       |  |  |                 |  |  |  |  |  |  |  |  |  |
|------------------|------|---------------|----------|---------------------------------------------------------------------------------------|---------|---------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|---|--|--|-------|--|--|-----------------|--|--|--|--|--|--|--|--|--|
| ID               |      |               |          | T S R                                                                                 |         |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  | N |  |  | M L K |  |  | H G F E D C B A |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |               |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |         |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |       |  |  |                 |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field         | Value    | ID                                                                                    | Value   | Description                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |       |  |  |                 |  |  |  |  |  |  |  |  |  |
| A                | RW   | READY         |          |                                                                                       |         | Enable or disable interrupt for event <a href="#">READY</a>         |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |       |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |               | Disabled | 0                                                                                     | Disable |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |       |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |               | Enabled  | 1                                                                                     | Enable  |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |       |  |  |                 |  |  |  |  |  |  |  |  |  |
| B                | RW   | FIELDDETECTED |          |                                                                                       |         | Enable or disable interrupt for event <a href="#">FIELDDETECTED</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |       |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |               | Disabled | 0                                                                                     | Disable |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |       |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |               | Enabled  | 1                                                                                     | Enable  |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |       |  |  |                 |  |  |  |  |  |  |  |  |  |
| C                | RW   | FIELDLOST     |          |                                                                                       |         | Enable or disable interrupt for event <a href="#">FIELDLOST</a>     |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |       |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |               | Disabled | 0                                                                                     | Disable |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |       |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |               | Enabled  | 1                                                                                     | Enable  |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |       |  |  |                 |  |  |  |  |  |  |  |  |  |
| D                | RW   | TXFRAMESTART  |          |                                                                                       |         | Enable or disable interrupt for event <a href="#">TXFRAMESTART</a>  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |       |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |               | Disabled | 0                                                                                     | Disable |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |       |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |               | Enabled  | 1                                                                                     | Enable  |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |       |  |  |                 |  |  |  |  |  |  |  |  |  |
| E                | RW   | TXFRAMEEND    |          |                                                                                       |         | Enable or disable interrupt for event <a href="#">TXFRAMEEND</a>    |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |       |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |               | Disabled | 0                                                                                     | Disable |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |       |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |               | Enabled  | 1                                                                                     | Enable  |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |       |  |  |                 |  |  |  |  |  |  |  |  |  |
| F                | RW   | RXFRAMESTART  |          |                                                                                       |         | Enable or disable interrupt for event <a href="#">RXFRAMESTART</a>  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |       |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |               | Disabled | 0                                                                                     | Disable |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |       |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |               | Enabled  | 1                                                                                     | Enable  |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |       |  |  |                 |  |  |  |  |  |  |  |  |  |
| G                | RW   | RXFRAMEEND    |          |                                                                                       |         | Enable or disable interrupt for event <a href="#">RXFRAMEEND</a>    |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |       |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |               | Disabled | 0                                                                                     | Disable |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |       |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |               | Enabled  | 1                                                                                     | Enable  |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |       |  |  |                 |  |  |  |  |  |  |  |  |  |
| H                | RW   | ERROR         |          |                                                                                       |         | Enable or disable interrupt for event <a href="#">ERROR</a>         |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |       |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |               | Disabled | 0                                                                                     | Disable |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |       |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |               | Enabled  | 1                                                                                     | Enable  |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |       |  |  |                 |  |  |  |  |  |  |  |  |  |
| K                | RW   | RXERROR       |          |                                                                                       |         | Enable or disable interrupt for event <a href="#">RXERROR</a>       |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |       |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |               | Disabled | 0                                                                                     | Disable |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |       |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |               | Enabled  | 1                                                                                     | Enable  |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |       |  |  |                 |  |  |  |  |  |  |  |  |  |
| L                | RW   | ENDRX         |          |                                                                                       |         | Enable or disable interrupt for event <a href="#">ENDRX</a>         |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |       |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |               | Disabled | 0                                                                                     | Disable |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |       |  |  |                 |  |  |  |  |  |  |  |  |  |

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### 7.1.21.13.47 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number       |      |               | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------|---------------|---------------------------------------------------------------------------------------|-------|-----------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|-------|--|--|--|-----------------|--|--|--|--|--|--|--|
| ID               |      |               | T S R                                                                                 |       |                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  | N |  |  |  | M L K |  |  |  | H G F E D C B A |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |               | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |       |                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce | Field         | Value ID                                                                              | Value | Description                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW   | READY         |                                                                                       |       | Write '1' to enable interrupt for event <a href="#">READY</a>         |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |               | Set                                                                                   | 1     | Enable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |               | Disabled                                                                              | 0     | Read: Disabled                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |               | Enabled                                                                               | 1     | Read: Enabled                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW   | FIELDDETECTED |                                                                                       |       | Write '1' to enable interrupt for event <a href="#">FIELDDETECTED</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |               | Set                                                                                   | 1     | Enable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |               | Disabled                                                                              | 0     | Read: Disabled                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |               | Enabled                                                                               | 1     | Read: Enabled                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
| C                | RW   | FIELDLOST     |                                                                                       |       | Write '1' to enable interrupt for event <a href="#">FIELDLOST</a>     |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |               | Set                                                                                   | 1     | Enable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |               | Disabled                                                                              | 0     | Read: Disabled                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |               | Enabled                                                                               | 1     | Read: Enabled                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
| D                | RW   | TXFRAMESTART  |                                                                                       |       | Write '1' to enable interrupt for event <a href="#">TXFRAMESTART</a>  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |               | Set                                                                                   | 1     | Enable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |               | Disabled                                                                              | 0     | Read: Disabled                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |               | Enabled                                                                               | 1     | Read: Enabled                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
| E                | RW   | TXFRAMEEND    |                                                                                       |       | Write '1' to enable interrupt for event <a href="#">TXFRAMEEND</a>    |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |               | Set                                                                                   | 1     | Enable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |               | Disabled                                                                              | 0     | Read: Disabled                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |               | Enabled                                                                               | 1     | Read: Enabled                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
| F                | RW   | RXFRAMESTART  |                                                                                       |       | Write '1' to enable interrupt for event <a href="#">RXFRAMESTART</a>  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |               | Set                                                                                   | 1     | Enable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |               | Disabled                                                                              | 0     | Read: Disabled                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |

| Bit number       |                      |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|----------------------|----------|---------------------------------------------------------------------------------------|---------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |                      |          | T S R                                                                                 |                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  | N M L K H G F E D C B A |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |                      |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field           | Value ID | Value                                                                                 | Description                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                      | Enabled  | 1                                                                                     | Read: Enabled                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| G                | RW RXFRAMEEND        |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">RXFRAMEEND</a>        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                      | Set      | 1                                                                                     | Enable                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                      | Disabled | 0                                                                                     | Read: Disabled                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                      | Enabled  | 1                                                                                     | Read: Enabled                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| H                | RW ERROR             |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">ERROR</a>             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                      | Set      | 1                                                                                     | Enable                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                      | Disabled | 0                                                                                     | Read: Disabled                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                      | Enabled  | 1                                                                                     | Read: Enabled                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| K                | RW RXERROR           |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">RXERROR</a>           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                      | Set      | 1                                                                                     | Enable                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                      | Disabled | 0                                                                                     | Read: Disabled                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                      | Enabled  | 1                                                                                     | Read: Enabled                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| L                | RW ENDRX             |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">ENDRX</a>             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                      | Set      | 1                                                                                     | Enable                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                      | Disabled | 0                                                                                     | Read: Disabled                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                      | Enabled  | 1                                                                                     | Read: Enabled                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| M                | RW ENDTX             |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">ENDTX</a>             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                      | Set      | 1                                                                                     | Enable                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                      | Disabled | 0                                                                                     | Read: Disabled                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                      | Enabled  | 1                                                                                     | Read: Enabled                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| N                | RW AUTOCOLRESSTARTED |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">AUTOCOLRESSTARTED</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                      | Set      | 1                                                                                     | Enable                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                      | Disabled | 0                                                                                     | Read: Disabled                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                      | Enabled  | 1                                                                                     | Read: Enabled                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| R                | RW COLLISION         |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">COLLISION</a>         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                      | Set      | 1                                                                                     | Enable                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                      | Disabled | 0                                                                                     | Read: Disabled                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                      | Enabled  | 1                                                                                     | Read: Enabled                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| S                | RW SELECTED          |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">SELECTED</a>          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                      | Set      | 1                                                                                     | Enable                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                      | Disabled | 0                                                                                     | Read: Disabled                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                      | Enabled  | 1                                                                                     | Read: Enabled                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| T                | RW STARTED           |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">STARTED</a>           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                      | Set      | 1                                                                                     | Enable                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                      | Disabled | 0                                                                                     | Read: Disabled                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                      | Enabled  | 1                                                                                     | Read: Enabled                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.21.13.48 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number       |  |  |  | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      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| Reset 0x00000000 |  |  |  | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 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 |   |  |   |  |



| Bit number       |      |                   |               | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                            |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------|-------------------|---------------|---------------------------------------------------------------------------------------|----------------------------------------------------------------------------|------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|--|-------|--|--|--|-----------------|--|--|--|--|--|--|--|
| ID               |      |                   |               | T S R                                                                                 |                                                                            |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  | N |  |  |  |  | M L K |  |  |  | H G F E D C B A |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |                   |               | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                            |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce | Field             | Value ID      | Value                                                                                 | Description                                                                |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |                   | Clear         | 1                                                                                     | Disable                                                                    |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |                   | Disabled      | 0                                                                                     | Read: Disabled                                                             |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |                   | Enabled       | 1                                                                                     | Read: Enabled                                                              |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  | B    | RW                | FIELDDETECTED |                                                                                       |                                                                            | Write '1' to disable interrupt for event <a href="#">FIELDDETECTED</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
| Clear            |      |                   |               | 1                                                                                     | Disable                                                                    |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
| Disabled         |      |                   |               | 0                                                                                     | Read: Disabled                                                             |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
| Enabled          |      |                   |               | 1                                                                                     | Read: Enabled                                                              |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
| C                | RW   | FIELDLOST         |               |                                                                                       | Write '1' to disable interrupt for event <a href="#">FIELDLOST</a>         |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |                   | Clear         | 1                                                                                     | Disable                                                                    |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |                   | Disabled      | 0                                                                                     | Read: Disabled                                                             |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |                   | Enabled       | 1                                                                                     | Read: Enabled                                                              |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
| D                | RW   | TXFRAMESTART      |               |                                                                                       | Write '1' to disable interrupt for event <a href="#">TXFRAMESTART</a>      |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |                   | Clear         | 1                                                                                     | Disable                                                                    |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |                   | Disabled      | 0                                                                                     | Read: Disabled                                                             |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |                   | Enabled       | 1                                                                                     | Read: Enabled                                                              |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
| E                | RW   | TXFRAMEEND        |               |                                                                                       | Write '1' to disable interrupt for event <a href="#">TXFRAMEEND</a>        |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |                   | Clear         | 1                                                                                     | Disable                                                                    |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |                   | Disabled      | 0                                                                                     | Read: Disabled                                                             |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |                   | Enabled       | 1                                                                                     | Read: Enabled                                                              |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
| F                | RW   | RXFRAMESTART      |               |                                                                                       | Write '1' to disable interrupt for event <a href="#">RXFRAMESTART</a>      |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |                   | Clear         | 1                                                                                     | Disable                                                                    |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |                   | Disabled      | 0                                                                                     | Read: Disabled                                                             |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |                   | Enabled       | 1                                                                                     | Read: Enabled                                                              |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
| G                | RW   | RXFRAMEEND        |               |                                                                                       | Write '1' to disable interrupt for event <a href="#">RXFRAMEEND</a>        |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |                   | Clear         | 1                                                                                     | Disable                                                                    |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |                   | Disabled      | 0                                                                                     | Read: Disabled                                                             |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |                   | Enabled       | 1                                                                                     | Read: Enabled                                                              |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
| H                | RW   | ERROR             |               |                                                                                       | Write '1' to disable interrupt for event <a href="#">ERROR</a>             |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |                   | Clear         | 1                                                                                     | Disable                                                                    |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |                   | Disabled      | 0                                                                                     | Read: Disabled                                                             |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |                   | Enabled       | 1                                                                                     | Read: Enabled                                                              |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
| K                | RW   | RXERROR           |               |                                                                                       | Write '1' to disable interrupt for event <a href="#">RXERROR</a>           |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |                   | Clear         | 1                                                                                     | Disable                                                                    |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |                   | Disabled      | 0                                                                                     | Read: Disabled                                                             |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |                   | Enabled       | 1                                                                                     | Read: Enabled                                                              |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
| L                | RW   | ENDRX             |               |                                                                                       | Write '1' to disable interrupt for event <a href="#">ENDRX</a>             |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |                   | Clear         | 1                                                                                     | Disable                                                                    |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |                   | Disabled      | 0                                                                                     | Read: Disabled                                                             |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |                   | Enabled       | 1                                                                                     | Read: Enabled                                                              |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
| M                | RW   | ENDTX             |               |                                                                                       | Write '1' to disable interrupt for event <a href="#">ENDTX</a>             |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |                   | Clear         | 1                                                                                     | Disable                                                                    |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |                   | Disabled      | 0                                                                                     | Read: Disabled                                                             |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |                   | Enabled       | 1                                                                                     | Read: Enabled                                                              |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
| N                | RW   | AUTOCOLRESSTARTED |               |                                                                                       | Write '1' to disable interrupt for event <a href="#">AUTOCOLRESSTARTED</a> |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |                   | Clear         | 1                                                                                     | Disable                                                                    |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |                   | Disabled      | 0                                                                                     | Read: Disabled                                                             |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |                   | Enabled       | 1                                                                                     | Read: Enabled                                                              |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
| R                | RW   | COLLISION         |               |                                                                                       | Write '1' to disable interrupt for event <a href="#">COLLISION</a>         |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |                   | Clear         | 1                                                                                     | Disable                                                                    |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |       |  |  |  |                 |  |  |  |  |  |  |  |

| Bit number       |            |          | 31    | 30       | 29             | 28 | 27                                                                | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |  |  |
|------------------|------------|----------|-------|----------|----------------|----|-------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|--|--|
| ID               |            |          |       |          |                |    |                                                                   |    |    |    |    |    | T  | S  | R  |    |    |    | N  |    |    |    | M  | L  | K |   |   |   | H | G | F | E | D | C | B | A |  |  |
| Reset 0x00000000 |            |          | 0     | 0        | 0              | 0  | 0                                                                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |  |  |
| ID               | Acce Field | Value ID | Value |          | Description    |    |                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            | Disabled | 0     |          | Read: Disabled |    |                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            | Enabled  | 1     |          | Read: Enabled  |    |                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            | S        | RW    | SELECTED |                |    | Write '1' to disable interrupt for event <a href="#">SELECTED</a> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            | Clear    | 1     |          | Disable        |    |                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            | Disabled | 0     |          | Read: Disabled |    |                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            | Enabled  | 1     |          | Read: Enabled  |    |                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            | T        | RW    | STARTED  |                |    | Write '1' to disable interrupt for event <a href="#">STARTED</a>  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            | Clear    | 1     |          | Disable        |    |                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            | Disabled | 0     |          | Read: Disabled |    |                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            | Enabled  | 1     |          | Read: Enabled  |    |                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |

### 7.1.21.13.49 ERRORSTATUS

Address offset: 0x404

NFC Error Status register

Write a bit to '1' to clear it. Writing '0' has no effect.

|                  |            |                   |       |    |    |    |                                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-------------------|-------|----|----|----|---------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                   | 31    | 30 | 29 | 28 | 27                                                                              | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |                   |       |    |    |    |                                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |
| Reset 0x00000000 |            |                   | 0     | 0  | 0  | 0  | 0                                                                               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |
| ID               | Acce Field | Value ID          | Value |    |    |    | Description                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | FRAMEDELAYTIMEOUT |       |    |    |    | No STARTTX task triggered before expiration of the time set<br>in FRAMEDELAYMAX |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.21.13.50 FRAMESTATUS.RX

Address offset: 0x40C

Result of last incoming frame

Write a bit to '1' to clear it. Writing '0' has no effect.

|                  |      |              |                                                                                       |             |       |                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|--------------|---------------------------------------------------------------------------------------|-------------|-------|-----------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |              | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |             |       |                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |              | C B A                                                                                 |             |       |                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |              | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |             |       |                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field        | Value                                                                                 | ID          | Value | Description                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW   | CRCERROR     |                                                                                       |             |       | No valid end of frame (EoF) detected    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |              |                                                                                       | CRCCorrect  | 0     | Valid CRC detected                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |              |                                                                                       | CRCError    | 1     | CRC received does not match local check |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW   | PARITYSTATUS |                                                                                       |             |       | Parity status of received frame         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |              |                                                                                       | ParityOK    | 0     | Frame received with parity OK           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |              |                                                                                       | ParityError | 1     | Frame received with parity error        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW   | OVERRUN      |                                                                                       |             |       | Overrun detected                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |              |                                                                                       | NoOverrun   | 0     | No overrun detected                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |              |                                                                                       | Overrun     | 1     | Overrun error                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.21.13.51 NFCTAGSTATE

Address offset: 0x410

NfcTag state register

| Bit number       |            |             | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|-------------|---------------------------------------------------------------------------------------|-------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |            |             | A A A                                                                                 |                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |             | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID    | Value                                                                                 | Description       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | R          | NFCTAGSTATE |                                                                                       | NfcTag state      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled    | 0                                                                                     | Disabled or sense |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | RampUp      | 2                                                                                     | RampUp            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Idle        | 3                                                                                     | Idle              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Receive     | 4                                                                                     | Receive           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | FrameDelay  | 5                                                                                     | FrameDelay        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Transmit    | 6                                                                                     | Transmit          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.21.13.52 SLEEPSTATE

Address offset: 0x420

Sleep state during automatic collision resolution

|                  |            |            |                                                                                       |                                                                                                                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|------------|---------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |            | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                                                                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |            | A                                                                                     |                                                                                                                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |            | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |                                                                                                                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID   | Value                                                                                 | Description                                                                                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | R          | SLEEPSTATE |                                                                                       | Reflects the sleep state during automatic collision resolution. Set to IDLE by a GOIDLE task. Set to SLEEP_A when a valid SLEEP_REQ frame is received or by a GOSLEEP task. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Idle       | 0                                                                                     | State is IDLE.                                                                                                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | SleepA     | 1                                                                                     | State is SLEEP_A.                                                                                                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.21.13.53 FIELDPRESENT

Address offset: 0x43C

Indicates the presence or not of a valid field

|                  |      |              |                                                                                       |       |                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|--------------|---------------------------------------------------------------------------------------|-------|-------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |              | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |              | B A                                                                                   |       |                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |              | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |       |                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field        | Value ID                                                                              | Value | Description                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | R    | FIELDPRESENT |                                                                                       |       | Indicates if a valid field is present. Available only in the activated state. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |              | NoField                                                                               | 0     | No valid field detected                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |              | FieldPresent                                                                          | 1     | Valid field detected                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | R    | LOCKDETECT   |                                                                                       |       | Indicates if the low level has locked to the field                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |              | NotLocked                                                                             | 0     | Not locked to field                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |              | Locked                                                                                | 1     | Locked to field                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.21.13.54 FRAMEDELAYMIN

Address offset: 0x504

Minimum frame delay

|                  |            |  |               |       |    |    |    |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|---------------|-------|----|----|----|---------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |               | 31    | 30 | 29 | 28 | 27                                                | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |  |               |       |    |    |    |                                                   |    |    |    |    |    |    |    |    |    |    |    | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000480 |            |  |               | 0     | 0  | 0  | 0  | 0                                                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |
| ID               | Acce Field |  | Value ID      | Value |    |    |    | Description                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         |  | FRAMEDELAYMIN |       |    |    |    | Minimum frame delay in number of 13.56 MHz clocks |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.21.13.55 FRAMEDELAYMAX

Address offset: 0x508

Maximum frame delay

|                  |            |  |               |  |       |  |  |  |  |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|---------------|--|-------|--|--|--|--|---------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |               |  |       |  |  |  |  | 31                                                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |
| ID               |            |  |               |  |       |  |  |  |  | A                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  | A  | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00001000 |            |  |               |  |       |  |  |  |  | 0                                                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |   |   |
| ID               | Acce Field |  | Value ID      |  | Value |  |  |  |  | Description                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         |  | FRAMEDELAYMAX |  |       |  |  |  |  | Maximum frame delay in number of 13.56 MHz clocks |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.21.13.56 FRAMEDELAYMODE

Address offset: 0x50C

Configuration register for the Frame Delay Timer

|                  |      |                |       |    |                                                                                                           |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|------------------|------|----------------|-------|----|-----------------------------------------------------------------------------------------------------------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|---|
| Bit number       |      |                | 31    | 30 | 29                                                                                                        | 28          | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |   |
| ID               |      |                | A     |    |                                                                                                           |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  | A |
| Reset 0x00000001 |      |                | 0     | 0  | 0                                                                                                         | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |  |  |  |   |
| ID               | Acce | Field          | Value | ID | Value                                                                                                     | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
| A                | RW   | FRAMEDELAYMODE |       |    | Configuration register for the Frame Delay Timer                                                          |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|                  |      | FreeRun        | 0     |    | Transmission is independent of frame timer and will start when the STARTTX task is triggered. No timeout. |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|                  |      | Window         | 1     |    | Frame is transmitted between FRAMEDELAYMIN and FRAMEDELAYMAX                                              |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|                  |      | ExactVal       | 2     |    | Frame is transmitted exactly at FRAMEDELAYMAX                                                             |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|                  |      | WindowGrid     | 3     |    | Frame is transmitted on a bit grid between FRAMEDELAYMIN and FRAMEDELAYMAX                                |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |

### 7.1.21.13.57 PACKETPTR

Address offset: 0x510

Packet pointer for TXD and RXD data storage in Data RAM

|                  |            |  |          |       |    |    |    |                                                                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|-------|----|----|----|-------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31    | 30 | 29 | 28 | 27                                                                                                          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |  |          | A     | A  | A  | A  | A                                                                                                           | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |          | 0     | 0  | 0  | 0  | 0                                                                                                           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID | Value |    |    |    | Description                                                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW PTR     |  |          |       |    |    |    | Packet pointer for TXD and RXD data storage in Data RAM.<br><br>This address is a byte-aligned RAM address. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

**Note:** See the memory chapter for details about which memories are available for EasyDMA.

### 7.1.21.13.58 MAXLEN

Address offset: 0x514

Size of the RAM buffer allocated to TXD and RXD data storage each

|                  |      |        |       |    |          |    |                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------|--------|-------|----|----------|----|-------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |      |        |       | 31 | 30       | 29 | 28                                                                | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |      |        |       |    |          |    |                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |      |        |       | 0  | 0        | 0  | 0                                                                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |
| ID               | Acce | Field  | Value | ID | Value    |    | Description                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW   | MAXLEN |       |    | [0..257] |    | Size of the RAM buffer allocated to TXD and RXD data storage each |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.21.13.59 TXD.FRAMECONFIG

Address offset: 0x518

Configuration of outgoing frames

| Bit number       |      |             |              | 31    | 30                                                                                          | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |
|------------------|------|-------------|--------------|-------|---------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ID               |      |             |              |       |                                                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | D | C | B | A |
| Reset 0x00000017 |      |             |              | 0     | 0                                                                                           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |   |   |   |
| ID               | Acce | Field       | Value ID     | Value | Description                                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW   | PARITY      |              |       | Indicates if parity is added to the frame                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |             | NoParity     | 0     | Parity is not added to TX frames                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |             | Parity       | 1     | Parity is added to TX frames                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW   | DISCARDMODE |              |       | Discarding unused bits at start or end of a frame                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |             | DiscardEnd   | 0     | Unused bits are discarded at end of frame (EoF)                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |             | DiscardStart | 1     | Unused bits are discarded at start of frame (SoF)                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| C                | RW   | SOF         |              |       | Adding SoF or not in TX frames                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |             | NoSoF        | 0     | SoF symbol not added                                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |             | SoF          | 1     | SoF symbol added                                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| D                | RW   | CRCMODETX   |              |       | CRC mode for outgoing frames                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |             | NoCRCTX      | 0     | CRC is not added to the frame                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |             | CRC16TX      | 1     | 16 bit CRC added to the frame based on all the data read from RAM that is used in the frame |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.21.13.60 TXD.AMOUNT

Address offset: 0x51C

Size of outgoing frame

|                  |      |             |          |          |                                                                                                                                                                                                                                                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------|-------------|----------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |      |             |          | 31       | 30                                                                                                                                                                                                                                                                                               | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |
| ID               |      |             |          |          |                                                                                                                                                                                                                                                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   | B | B | B | B | B | B | B | B | B | A | A | A | A |
| Reset 0x00000000 |      |             |          | 0        | 0                                                                                                                                                                                                                                                                                                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce | Field       | Value ID | Value    | Description                                                                                                                                                                                                                                                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW   | TXDATABITS  |          | [0..7]   | Number of bits in the last or first byte read from RAM that shall be included in the frame (excluding parity bit).<br><br>The DISCARDMODE field in FRAMECONFIG.TX selects if unused bits is discarded at the start or at the end of a frame. A value of 0 data bytes and 0 data bits is invalid. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW   | TXDATABYTES |          | [0..257] | Number of complete bytes that shall be included in the frame, excluding CRC, parity and framing                                                                                                                                                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |





### 7.1.21.13.67 NFCID1\_3RD\_LAST

Address offset: 0x598

Third last NFCID1 part (10 bytes ID)

|                  |      |          |       |    |       |               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|------------------|------|----------|-------|----|-------|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|
| Bit number       |      |          |       | 31 | 30    | 29            | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |
| ID               |      |          |       |    |       |               |    |    |    |    |    |    |    | C  | C  | C  | C  | C  | C  | C  | B  | B  | B  | B  | B  | B | B | A | A | A | A | A | A | A |   |  |  |  |
| Reset 0x00000000 |      |          |       | 0  | 0     | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |
| ID               | Acce | Field    | Value | ID | Value | Description   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
| A                | RW   | NFCID1_S |       |    |       | NFCID1 byte S |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
| B                | RW   | NFCID1_R |       |    |       | NFCID1 byte R |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
| C                | RW   | NFCID1_Q |       |    |       | NFCID1 byte Q |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |

### 7.1.21.13.68 AUTOCOLRESCONFIG

Address offset: 0x59C

Controls the auto collision resolution function. This setting must be done before the NFCT peripheral is activated.

When modifying this register bit 1 must be written to '1'.

|                  |            |  |          |       |    |                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |   |  |
|------------------|------------|--|----------|-------|----|--------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|---|--|
| Bit number       |            |  |          | 31    | 30 | 29                                         | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |   |  |
| ID               |            |  |          |       |    |                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  | A |  |
| Reset 0x00000002 |            |  |          | 0     | 0  | 0                                          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |  |  |   |  |
| ID               | Acce Field |  | Value ID | Value |    | Description                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |   |  |
| A                | RW         |  | MODE     |       |    | Enables/disables auto collision resolution |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |   |  |
|                  |            |  | Enabled  | 0     |    | Auto collision resolution enabled          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |   |  |
|                  |            |  | Disabled | 1     |    | Auto collision resolution disabled         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |   |  |

### 7.1.21.13.69 SENSRES

Address offset: 0x5A0

NFC-A SENS\_RES auto-response settings

| Bit number       |            |              | 31                                                                    | 30                                                                                                                                        | 29                                   | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
|------------------|------------|--------------|-----------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| ID               |            |              | E E E E D D D D C C B A A A A A                                       |                                                                                                                                           |                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| Reset 0x00000001 |            |              | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 |                                                                                                                                           |                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| ID               | Acce Field | Value ID     | Value                                                                 | Description                                                                                                                               |                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| A                | RW         | BITFRAMESDD  |                                                                       | Bit frame SDD as defined by the b5:b1 of byte 1 in<br>SENS_RES response in the NFC Forum, NFC Digital Protocol<br>Technical Specification |                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | SDD00000     | 0                                                                     | SDD pattern 00000                                                                                                                         |                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | SDD00001     | 1                                                                     | SDD pattern 00001                                                                                                                         |                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | SDD00010     | 2                                                                     | SDD pattern 00010                                                                                                                         |                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | SDD00100     | 4                                                                     | SDD pattern 00100                                                                                                                         |                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | SDD01000     | 8                                                                     | SDD pattern 01000                                                                                                                         |                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | SDD10000     | 16                                                                    | SDD pattern 10000                                                                                                                         |                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | B            | RW                                                                    | RFU5                                                                                                                                      | Reserved for future use. Shall be 0. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| C                | RW         | NFCIDSIZE    |                                                                       | NFCID1 size. This value is used by the auto collision<br>resolution engine.                                                               |                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | NFCID1Single | 0                                                                     | NFCID1 size: single (4 bytes)                                                                                                             |                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | NFCID1Double | 1                                                                     | NFCID1 size: double (7 bytes)                                                                                                             |                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |



|                  |      |                |  |              |    |                                                                                                                                                  |    |                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------|----------------|--|--------------|----|--------------------------------------------------------------------------------------------------------------------------------------------------|----|--------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |      |                |  | 31           | 30 | 29                                                                                                                                               | 28 | 27                             | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |      |                |  |              |    |                                                                                                                                                  |    |                                |    |    |    |    |    |    |    |    |    |    |    | E  | E  | E  | E  | D  | D  | D | C | C | B | A | A | A | A | A | A | A | A |
| Reset 0x00000001 |      |                |  | 0            | 0  | 0                                                                                                                                                | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |   |
| ID               | Acce | Field          |  | Value ID     |    | Value                                                                                                                                            |    | Description                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |                |  | NFCID1Triple |    | 2                                                                                                                                                |    | NFCID1 size: triple (10 bytes) |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| D                | RW   | PLATFORMCONFIG |  |              |    | Tag platform configuration as defined by the b4:b1 of byte 2 in SENS_RES response in the NFC Forum, NFC Digital Protocol Technical Specification |    |                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| E                | RW   | RFU74          |  |              |    | Reserved for future use. Shall be 0.                                                                                                             |    |                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.21.13.70 SELRES

Address offset: 0x5A4

NFC-A SEL\_RES auto-response settings

|                  |      |          |       |                                                                                       |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                                                                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|----------|-------|---------------------------------------------------------------------------------------|-------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |          |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                                                                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |          |       | E D D C C B A A                                                                       |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                                                                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |          |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                                                                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field    | Value | ID                                                                                    | Value |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Description                                                                                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW   | RFU10    |       |                                                                                       |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reserved for future use. Shall be 0.                                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW   | CASCADE  |       |                                                                                       |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Cascade as defined by the b3 of SEL_RES response in the NFC Forum, NFC Digital Protocol Technical Specification (controlled by hardware, shall be 0) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW   | RFU43    |       |                                                                                       |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reserved for future use. Shall be 0.                                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| D                | RW   | PROTOCOL |       |                                                                                       |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Protocol as defined by the b7:b6 of SEL_RES response in the NFC Forum, NFC Digital Protocol Technical Specification                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| E                | RW   | RFU7     |       |                                                                                       |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reserved for future use. Shall be 0.                                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

## 7.1.21.14 Electrical specification

### 7.1.21.14.1 NFCT Electrical Specification

| Symbol      | Description                                                               | Min. | Typ. | Max. | Units |
|-------------|---------------------------------------------------------------------------|------|------|------|-------|
| $f_c$       | Frequency of operation                                                    | ..   | ..   | ..   | MHz   |
| $C_{MI}$    | Carrier modulation index                                                  | ..   | ..   | ..   | %     |
| DR          | Data Rate                                                                 | ..   | ..   | ..   | kbps  |
| $V_{sense}$ | Peak differential Field detect threshold level on NFC1-NFC2 <sup>12</sup> | ..   | ..   | ..   | Vp    |
| $I_{max}$   | Maximum input current on NFCT pins                                        | ..   | ..   | ..   | mA    |

### 7.1.21.14.2 NFCT Timing Parameters

| Symbol         | Description                                                                                 | Min. | Typ. | Max. | Units |
|----------------|---------------------------------------------------------------------------------------------|------|------|------|-------|
| $t_{activate}$ | Time from task_ACTIVATE in SENSE or DISABLE state to ACTIVATE_A or IDLE state <sup>13</sup> | ..   | ..   | ..   | μs    |
| $t_{sense}$    | Time from remote field is present in SENSE mode to FIELDDETECTED event is asserted          | ..   | ..   | ..   | μs    |

<sup>12</sup> Input is high impedance in sense mode

<sup>13</sup> Does not account for voltage supply and oscillator startup times

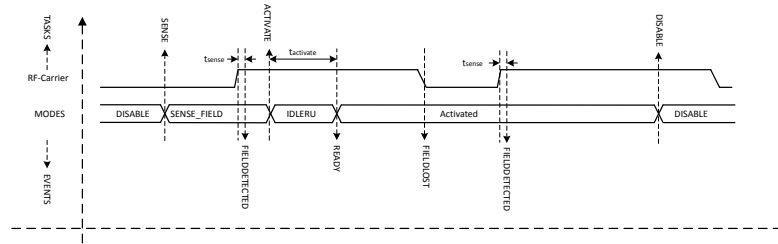


Figure 94: NFCT timing parameters (Shortcuts for FIELDDETECTED and FIELDLOST are disabled)

## 7.1.22 NVMC — Non-volatile memory controller

The non-volatile memory controller (NVMC) is used for writing and erasing of the internal flash memory and the user information configuration register (UICR).

The NVMC is a split security peripheral. This means that when the NVMC is configured as non-secure, only a subset of the registers is available from the non-secure code. See [SPU — System protection unit](#) on page 568 and [Registers](#) on page 321 for more details.

When the NVMC is configured to be a secure peripheral, only secure code has access.

Before a write can be performed, the NVMC must be enabled for writing in CONFIG.WEN. Similarly, before an erase can be performed, the NVMC must be enabled for erasing in CONFIG.EEN, see [CONFIG](#) on page 322. The user must make sure that writing and erasing are not enabled at the same time. Failing to do so may result in unpredictable behavior.

### 7.1.22.1 Writing to flash

When writing is enabled, in CONFIG register for secure region, or in CONFIGNS register for non-secure region, flash is written by writing a full 32-bit word to a word-aligned address in flash.

Secure code has access to both secure and non-secure regions, by using the appropriate configuration of CONFIG and CONFIGNS registers. Non-secure code, in contrast, has access to non-secure regions only. Thus, non-secure code only needs CONFIGNS.

The NVMC is only able to write '0' to erased bits in flash, that is bits set to '1'. It cannot write a bit back to '1'.

As illustrated in [Memory](#) on page 18, flash is divided into multiple pages. The same address in flash can only be written  $n_{\text{WRITE}}$  number of times before a page erase must be performed.

Only full 32-bit words can be written to flash using the NVMC interface. To write less than 32 bits to flash, write the data as a word, and set all the bits that should remain unchanged in the word to '1'. Note that the restriction about the number of writes (see above) still applies in this case.

The time it takes to write a word to flash is specified by  $t_{\text{WRITE}}$ . If CPU executes code from flash while the NVMC is writing to flash, the CPU will be stalled.

Only word-aligned writes are allowed. Byte or half-word-aligned writes will result in a bus fault.

### 7.1.22.2 Erasing a secure page in flash

When secure region erase is enabled (in CONFIG register), a flash page can be erased by writing 0xFFFFFFFF into the first 32-bit word in a flash page.

Page erase is only applicable to the code area in the flash and does not work with UICR.

After erasing a flash page, all bits in the page are set to '1'. The time it takes to erase a page is specified by  $t_{\text{ERASEPAGE}}$ . The CPU is stalled if the CPU executes code from the flash while the NVMC performs the erase operation.

See [Partial erase of a page in flash](#) for information on splitting the erase time in smaller chunks.

### 7.1.22.3 Erasing a non-secure page in flash

When non-secure region erase is enabled, a non-secure flash page can be erased by writing 0xFFFFFFFF into the first 32-bit word of the flash page.

Page erase is only applicable to the code area in the flash and does not work with UICR.

After erasing a flash page, all bits in the page are set to '1'. The time it takes to erase a page is specified by  $t_{\text{ERASEPAGE}}$ . The CPU is stalled if the CPU executes code from the flash while the NVMC performs the erase operation.

### 7.1.22.4 Writing to user information configuration registers (UICR)

User information configuration registers (UICR) are written in the same way as flash. After UICR has been written, the new UICR configuration will only take effect after a reset.

UICR is only accessible by secure code. Any write from non-secure code will be faulted. In order to lock the chip after uploading non-secure code, non-secure debugger needs to use the WRITEUICRNS register inside the NVMC in order to set APPROTECT (APPROTECT will be written to 0x00000000).

UICR can only be written  $n_{\text{WRITE}}$  number of times before an erase must be performed using [ERASEALL](#).

The time it takes to write a word to the UICR is specified by  $t_{\text{WRITE}}$ . The CPU is stalled if the CPU executes code from the flash while the NVMC is writing to the UICR.

### 7.1.22.5 Erase all

When erase is enabled, the whole flash and UICR can be erased in one operation by using the [ERASEALL](#) register. [ERASEALL](#) will not erase the factory information configuration registers (FICR).

This functionality can be blocked by some configuration of the UICR protection bits, see the table [Table 102: NVMC protection \(1 - Enabled, 0 - Disabled, X - Don't care\)](#) on page 320.

The time it takes to perform an [ERASEALL](#) on page 322 command is specified by  $t_{\text{ERASEALL}}$ . The CPU is stalled if the CPU executes code from the flash while the NVMC performs the erase operation.

### 7.1.22.6 NVMC protection mechanisms

This chapter describes the different protection mechanisms for the non-volatile memory.

#### 7.1.22.6.1 NVMC blocking

UICR integrity is assured through use of multiple levels of protection. UICR protection bits can be configured to allow or block certain operations.

The table below shows the different status of UICR protection bits, and which operations are allowed or blocked.

| UICR protection bit status |           |              | NVMC protection     |                  |
|----------------------------|-----------|--------------|---------------------|------------------|
| SECUREAPPROTECT            | APPROTECT | ERASEPROTECT | CTRL-AP<br>ERASEALL | NVMC<br>ERASEALL |
| 0                          | 0         | 0            | Available           | Available        |
| 1                          | X         | 0            | Available           | Blocked          |
| X                          | 1         | 0            | Available           | Blocked          |
| X                          | X         | 1            | Blocked             | Blocked          |

Table 102: NVMC protection (1 - Enabled, 0 - Disabled, X - Don't care)

**Note:** Erase can still be performed through CTRL-AP, regardless of the above settings. See [CTRL-AP - Control access port](#) on page 739 for more information.

## Uploading code with secure debugging blocked

Non-secure code can program non-secure flash regions. In order to perform these operations, the NVMC has the following non-secure registers: CONFIGS, READY and READYNEXT.

Register [CONFIGS](#) on page 323 works as the CONFIG register but it is used only for non-secure transactions. Both page erase and writing inside the flash require a write transaction (see [Erasing a secure page in flash](#) on page 318 or [Erasing a non-secure page in flash](#) on page 319). Because of this, the [SPU — System protection unit](#) on page 568 will guarantee that the non-secure code cannot write inside a secure page, since the transaction will never reach the NVMC controller.

### 7.1.22.6.2 NVMC power failure protection

NVMC power failure protection is possible through use of power-fail comparator that is monitoring power supply.

If the power-fail comparator is enabled, and the power supply voltage is below  $V_{POF}$  threshold, the power-fail comparator will prevent the NVMC from performing erase or write operations in non-volatile memory (NVM).

If a power failure warning is present at the start of an NVM write or erase operation, the NVMC will block the operation and a bus error will be signalled. If a power failure warning occurs during an ongoing NVM write operation, the NVMC will try to finish the operation. And if the power failure warning persists, consecutive NVM write operations will be blocked by the NVMC, and a bus error will be signalled.

### 7.1.22.7 Cache

An instruction cache (I-Cache) can be enabled for the ICODE bus in the NVMC.

See [Memory](#) on page 18 for the location of flash.

A cache hit is an instruction fetch from the cache, and it has a 0 wait-state delay. The number of wait-states for a cache miss, where the instruction is not available in the cache and needs to be fetched from flash, depends on the processor frequency, see CPU parameter `W_FLASHCACHE`.

Enabling the cache can increase the CPU performance, and reduce power consumption by reducing the number of wait cycles and the number of flash accesses. This will depend on the cache hit rate. Cache draws current when enabled. If the reduction in average current due to reduced flash accesses is larger than the cache power requirement, the average current to execute the program code will be reduced.

When disabled, the cache does not draw current and its content is not retained.

It is possible to enable cache profiling to analyze the performance of the cache for your program using the register `ICACHECNF`. When profiling is enabled, registers `IHIT` and `IMISS` are incremented for every instruction cache hit or miss respectively.

## 7.1.22.8 Registers

| Base address             | Domain      | Peripheral | Instance              | Secure mapping | DMA security | Description                    | Configuration                                     |
|--------------------------|-------------|------------|-----------------------|----------------|--------------|--------------------------------|---------------------------------------------------|
| 0x50039000<br>0x40039000 | APPLICATION | NVMC       | NVMC : S<br>NVMC : NS | SPLIT          | NA           | Non-volatile memory controller | ICACHECNF, IHIT and IMISS registers not supported |
| 0x41080000               | NETWORK     | NVMC       | NVMC                  | NS             | NA           | Non-Volatile Memory Controller | CONFIGNS and WRITEUICRNS not supported.           |

Table 103: Instances

| Register            | Offset | Security | Description                                       |
|---------------------|--------|----------|---------------------------------------------------|
| READY               | 0x400  | NS       | Ready flag                                        |
| READYNEXT           | 0x408  | NS       | Ready flag                                        |
| CONFIG              | 0x504  | S        | Configuration register                            |
| ERASEALL            | 0x50C  | S        | Register for erasing all non-volatile user memory |
| ERASEPAGEPARTIALCFG | 0x51C  | S        | Register for partial erase configuration          |
| ICACHECNF           | 0x540  | S        | I-code cache configuration register               |
| IHIT                | 0x548  | S        | I-code cache hit counter                          |
| IMISS               | 0x54C  | S        | I-code cache miss counter                         |
| CONFIGNS            | 0x584  | NS       |                                                   |
| WRITEUICRNS         | 0x588  | NS       | Non-secure APPROTECT enable register              |

Table 104: Register overview

### 7.1.22.8.1 READY

Address offset: 0x400

Ready flag

|                  |      |       |       |                                                                                       |       |                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|-------|-------|---------------------------------------------------------------------------------------|-------|--------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |       |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |       |       | A                                                                                     |       |                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000001 |      |       |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1             |       |                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field | Value | ID                                                                                    | Value | Description                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | R    | READY |       |                                                                                       |       | NVMC is ready or busy                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Busy  | 0                                                                                     |       | NVMC is busy (on-going write or erase operation) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Ready | 1                                                                                     |       | NVMC is ready                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.22.8.2 READYNEXT

Address offset: 0x408

Ready flag

|                  |      |           |       |                                                                                       |       |                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|-----------|-------|---------------------------------------------------------------------------------------|-------|----------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |           |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |           |       | A                                                                                     |       |                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000001 |      |           |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1             |       |                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field     | Value | ID                                                                                    | Value | Description                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | R    | READYNEXT |       |                                                                                       |       | NVMC can accept a new write operation  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Busy  |                                                                                       | 0     | NVMC cannot accept any write operation |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Ready |                                                                                       | 1     | NVMC is ready                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |



## I-code cache configuration register

| Bit number       |      |             |          | 31 | 30                                            | 29                     | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |  |
|------------------|------|-------------|----------|----|-----------------------------------------------|------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|--|
| ID               |      |             |          |    |                                               |                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | B |   |   |   |   |   |   |   | A |  |  |  |
| Reset 0x00000000 |      |             |          | 0  | 0                                             | 0                      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |
| ID               | Acce | Field       | Value    | ID | Value                                         | Description            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
| A                | RW   | CACHEEN     |          |    |                                               | Cache enable           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |             | Disabled | 0  | Disable cache. Invalidates all cache entries. |                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |             | Enabled  | 1  | Enable cache                                  |                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
| B                | RW   | CACHEPROFEN |          |    |                                               | Cache profiling enable |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |             | Disabled | 0  | Disable cache profiling                       |                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |             | Enabled  | 1  | Enable cache profiling                        |                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |

#### 7.1.22.8.7 IHIT

Address offset: 0x548

I-code cache hit counter

|                  |      |       |       |    |       |    |                     |                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------|-------|-------|----|-------|----|---------------------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |      |       |       | 31 | 30    | 29 | 28                  | 27                   | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |      |       |       | A  | A     | A  | A                   | A                    | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |      |       |       | 0  | 0     | 0  | 0                   | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce | Field | Value | ID | Value |    |                     | Description          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW   | HITS  |       |    |       |    |                     | Number of cache hits |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |       |       |    |       |    | Write zero to clear |                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 7.1.22.8.8 IMISS

Address offset: 0x54C

I-code cache miss counter

|                  |            |          |       |                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|-------|------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |       | 31                     | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |          |       | A                      | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |       | 0                      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID | Value | Description            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | MISSES   |       | Number of cache misses |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |          |       | Write zero to clear    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 7.1.22.8.9 CONFIGS

Address offset: 0x584

This register is one hot

| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                                                                                                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |            |          |                                                                                       |                                                                                                                                                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                                                                                                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                                                                                                                                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | WEN      |                                                                                       | <p>Program memory access mode. It is strongly recommended to only activate erase and write modes when they are actively used.</p> <p>Enabling write or erase will invalidate the cache and keep it invalidated.</p> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Ren      | 0                                                                                     | Read only access                                                                                                                                                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Wen      | 1                                                                                     | Write enabled                                                                                                                                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Een      | 2                                                                                     | Erase enabled                                                                                                                                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.22.8.10 WRITEUICRNS

Address offset: 0x588

Non-secure APPROTECT enable register

| Bit number       |      |       |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|-------|----------|---------------------------------------------------------------------------------------|-------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |      |       |          | B B B B B B B B B B B B B B B B B B B B B B B B B B B B B B A                         |                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |       |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field | Value ID | Value                                                                                 | Description                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W    | SET   |          |                                                                                       | Allow non-secure code to set APPROTECT                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Set      | 1                                                                                     | Set value                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | W    | KEY   |          |                                                                                       | Key to write in order to validate the write operation |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Keyvalid | 0xAFBE5A7                                                                             | Key value                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

## 7.1.22.9 Electrical specification

### 7.1.22.9.1 Flash programming

| Symbol                       | Description                                               | Min. | Typ. | Max. | Units   |
|------------------------------|-----------------------------------------------------------|------|------|------|---------|
| $n_{WRITE}$                  | Number of times a 32-bit word can be written before erase | ..   | ..   | ..   |         |
| $n_{ENDURANCE}$              | Erase cycles per page                                     | ..   | ..   | ..   |         |
| $t_{WRITE}$                  | Time to write one 32-bit word                             | ..   | ..   | ..   | $\mu s$ |
| $t_{ERASEPAGE}$              | Time to erase one page                                    | ..   | ..   | ..   | ms      |
| $t_{ERASEALL}$               | Time to erase all flash                                   | ..   | ..   | ..   | ms      |
| $t_{ERASEPAGEPARTIAL,setup}$ | Setup time for one partial erase                          | ..   | ..   | ..   | ms      |

### 7.1.22.9.2 Cache size

| Symbol                           | Description       | Min. | Typ. | Max. | Units |
|----------------------------------|-------------------|------|------|------|-------|
| Size <sub>I<sub>CODE</sub></sub> | I-Code cache size | ..   | ..   | ..   | Bytes |

## 7.1.23 PDM — Pulse density modulation interface

The pulse density modulation (PDM) module enables input of pulse density modulated signals from external audio frontends, for example, digital microphones. The PDM module generates the PDM clock and supports single-channel or dual-channel (left and right) data input. Data is transferred directly to RAM buffers using EasyDMA.



Listed here are the main features for PDM:

- Up to two PDM microphones configured as a left/right pair using the same data input
- 16 kHz output sample rate, 16-bit samples
- EasyDMA support for sample buffering
- HW decimation filters
- Selectable ratio of 64 or 80 between PDM\_CLK and output sample rate

The PDM module illustrated below is interfacing up to two digital microphones with the PDM interface. EasyDMA is implemented to relieve the real-time requirements associated with controlling of the PDM slave from a low priority CPU execution context. It also includes all the necessary digital filter elements to produce pulse code modulation (PCM) samples. The PDM module allows continuous audio streaming.

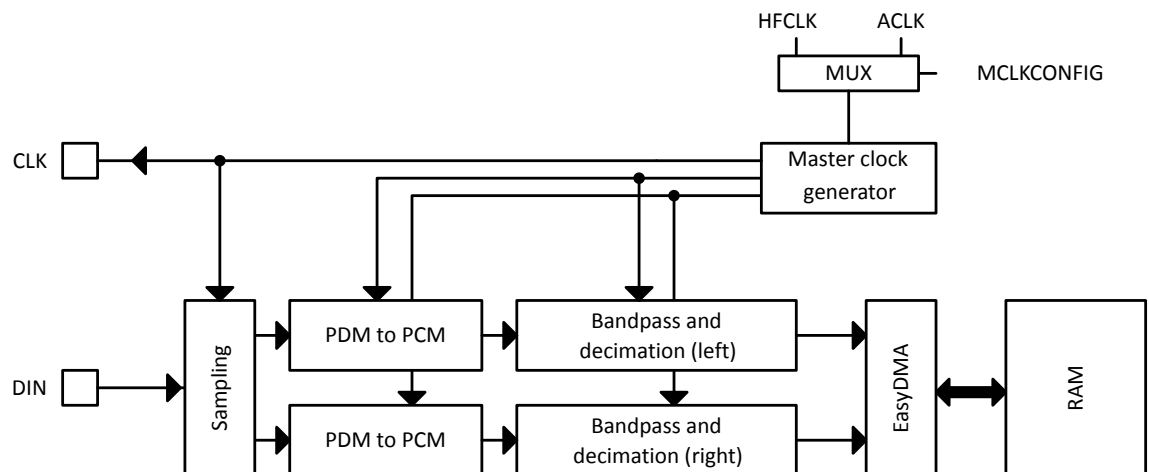


Figure 95: PDM module

### 7.1.23.1 Master clock source selection

The master clock source can be configured in register [MCLKCONFIG](#) on page 337. Choose one of the following as the master clock source:

- 32 MHz peripheral clock (PCLK32M), synchronous to HFCLK.
- Audio PLL clock (ACLK) with configurable frequency.

The peripheral must be stopped before selecting the master clock source. The use of the STOP task and the STOPPED event is described in [Module operation](#) on page 326.

To improve the master clock accuracy and jitter performance, it is recommended (but not mandatory) that the source is running off the HFXO instead of the HFINT oscillator. See [CLOCK — Clock control](#) on page 61 for more information about starting HFXO for the relevant clock source.

### 7.1.23.2 Master clock generator

The master clock generator's PDMCLKCTRL register allows adjusting the PDM clock's frequency.

The master clock generator does not add any jitter to the HFCLK source chosen. It is recommended (but not mandatory) to use the Xtal as HFCLK source.

The following equation can be used to calculate the value of the PDMCLKCTRL register for a given PDM clock- and master clock source frequency:

$$PDMCLKCTRL = 4096 \cdot \left\lfloor \frac{f_{pdm} \cdot 1048576}{f_{source} + \frac{f_{pdm}}{2}} \right\rfloor$$

Figure 96: PDM clock frequency equation

Where  $f_{\text{pdm}}$  is the requested PDM clock frequency in Hz, and  $f_{\text{source}}$  is the master clock generator source in Hz. Because of rounding errors, an accurate PDM clock may not be achievable. The actual PDM frequency can be calculated using the equation below.

$$f_{\text{actual}} = \frac{f_{\text{source}}}{\left\lfloor \frac{1048576 \cdot 4096}{\text{PDMCLKCTRL}} \right\rfloor}$$

Figure 97: Actual PDM frequency

The clock error can be calculated using the equation below. The error  $e$  is the percentage difference from the requested  $f_{\text{pdm}}$  frequency.

$$e = 100 \cdot \frac{f_{\text{actual}} - f_{\text{pdm}}}{f_{\text{pdm}}} = 100 \cdot \frac{\frac{f_{\text{source}}}{\left\lfloor \frac{1048576 \cdot 4096}{\text{PDMCLKCTRL}} \right\rfloor} - f_{\text{pdm}}}{f_{\text{pdm}}}$$

Figure 98: PDM frequency error equation

The PDM frequency can be adjusted on-the-fly:

- For PCLK32M, by using PDMCLKCTRL
- For ACLK, by adjusting the audio clock source, see [CLOCK — Clock control](#) on page 61.

| Requested PDM frequency $f_{\text{pdm}}$ [Hz] | $f_{\text{source}}$ [Hz] | RATIO | PDMCLKCTRL | Actual PDM frequency $f_{\text{actual}}$ [Hz] | Sample frequency [Hz] | Error [%] |
|-----------------------------------------------|--------------------------|-------|------------|-----------------------------------------------|-----------------------|-----------|
| 1024000                                       | 32000000 (PCLK32M)       | 64    | 135274496  | 1032258.1                                     | 16129.0               | 0.81      |
| 1280000                                       | 32000000 (PCLK32M)       | 80    | 168427520  | 1280000                                       | 16000                 | 0         |
| 1024000                                       | 12288000 (ACLK)          | 64    | 343597056  | 1024000                                       | 16000                 | 0         |

Table 105: Configuration examples

### 7.1.23.3 Module operation

By default, bits from the left PDM microphone are sampled on PDM\_CLK falling edge, and bits for the right are sampled on the rising edge of PDM\_CLK, resulting in two bitstreams. Each bitstream is fed into a digital filter which converts the PDM stream into 16-bit PCM samples, then filters and down-samples them to reach the appropriate sample rate.

The EDGE field in the MODE register allows swapping left and right, so that left will be sampled on rising edge, and right on falling.

The PDM module uses EasyDMA to store the samples coming out from the filters into one buffer in RAM. Depending on the mode chosen in the OPERATION field in the MODE register, memory either contains alternating left and right 16-bit samples (Stereo), or only left 16-bit samples (Mono). To ensure continuous PDM sampling, it is up to the application to update the EasyDMA destination address pointer as the previous buffer is filled.

The continuous transfer can be started or stopped by sending the START and STOP tasks. STOP becomes effective after the current frame has finished transferring, which will generate the STOPPED event. The STOPPED event indicates that all activity in the module is finished, and that the data is available in RAM (EasyDMA has finished transferring as well). Attempting to restart before receiving the STOPPED event may result in unpredictable behavior.

### 7.1.23.4 Decimation filter

In order to convert the incoming data stream into PCM audio samples, a decimation filter is included in the PDM interface module.

The input of the filter is the two-channel PDM serial stream (with left channel on clock high, right channel on clock low). Depending on the **RATIO** selected, its output is  $2 \times 16$ -bit PCM samples at a sample rate either 64 times or 80 times (depending on the **RATIO** register) lower than the PDM clock rate.

The filter stage of each channel is followed by a digital volume control, to attenuate or amplify the output samples in a range of -20 dB to +20 dB around the default (reset) setting, defined by  $G_{PDM, default}$ . The gain is controlled by the **GAINL** and **GAINR** registers.

As an example, if the goal is to achieve 2500 RMS output samples (16-bit) with a 1 kHz 90 dBA signal into a -26 dBFS sensitivity PDM microphone, do the following:

- Sum the PDM module's default gain ( $G_{PDM, default}$ ) and the gain introduced by the microphone and acoustic path of his implementation (an attenuation would translate into a negative gain)
- Adjust **GAINL** and **GAINR** by the above summed amount. Assuming that only the PDM module influences the gain, **GAINL** and **GAINR** must be set to  $-G_{PDM, default}$  dB to achieve the requirement.

With  $G_{PDM, default}=3.2$  dB, and as **GAINL** and **GAINR** are expressed in 0.5 dB steps, the closest value to program would be 3.0 dB, which can be calculated as:

```
GAINL = GAINR = (DefaultGain - (2 * 3))
```

Remember to check that the resulting values programmed into **GAINL** and **GAINR** fall within **MinGain** and **MaxGain**.

### 7.1.23.5 EasyDMA

Samples will be written directly to RAM, and EasyDMA must be configured accordingly.

The address pointer for the EasyDMA channel is set in **SAMPLE.PTR** register. If the destination address set in **SAMPLE.PTR** is not pointing to the Data RAM region, an EasyDMA transfer may result in a **HardFault** or RAM corruption. See [Memory](#) on page 18 for more information about the different memory regions.

DMA supports Stereo (Left+Right 16-bit samples) and Mono (Left only) data transfer, depending on the setting in the **OPERATION** field in the **MODE** register. The samples are stored little endian.

| MODE.OPERATION | Bits per sample | Result stored per RAM word | Physical RAM allocated (32-bit words) | Result boundary indexes in RAM | Note    |
|----------------|-----------------|----------------------------|---------------------------------------|--------------------------------|---------|
| Stereo         | 32 (2x16)       | L+R                        | $\text{ceil}(\text{SAMPLE.MAXCNT}/2)$ | $R0=[31:16]; L0=[15:0]$        | Default |
| Mono           | 16              | 2xL                        | $\text{ceil}(\text{SAMPLE.MAXCNT}/2)$ | $L1=[31:16]; L0=[15:0]$        |         |

Table 106: DMA sample storage

The destination buffer in RAM consists of one block, the size of which is set in **SAMPLE.MAXCNT** register. Format is number of 16-bit samples. The physical RAM allocated is always:

```
(RAM allocation, in bytes) = SAMPLE.MAXCNT * 2;
```

(but the mapping of the samples depends on **MODE.OPERATION**).

If **OPERATION**=Stereo, RAM will contain a succession of left and right samples.

If **OPERATION**=Mono, RAM will contain a succession of left only samples.

For a given value of `SAMPLE.MAXCNT`, the buffer in RAM can contain half the stereo sampling time as compared to the mono sampling time.

The PDM acquisition can be started by the `START` task, after the `SAMPLE.PTR` and `SAMPLE.MAXCNT` registers have been written. When starting the module, it will take some time for the filters to start outputting valid data. Transients from the PDM microphone itself may also occur. The first few samples (typically around 50) might hence contain invalid values or transients. It is therefore advised to discard the first few samples after a PDM start.

As soon as the `STARTED` event is received, the firmware can write the next `SAMPLE.PTR` value (this register is double-buffered), to ensure continuous operation.

When the buffer in RAM is filled with samples, an `END` event is triggered. The firmware can start processing the data in the buffer. Meanwhile, the PDM module starts acquiring data into the new buffer pointed to by `SAMPLE.PTR`, and sends a new `STARTED` event, so that the firmware can update `SAMPLE.PTR` to the next buffer address.

### 7.1.23.6 Hardware example

PDM can be configured with a single microphone (mono), or with two microphones.

When a single microphone is used, connect the microphone clock to `CLK`, and data to `DIN`.

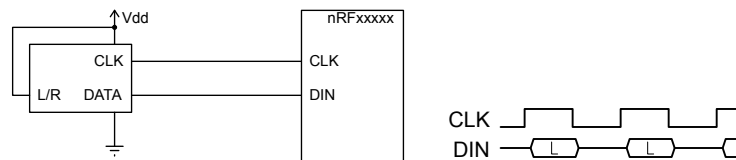


Figure 99: Example of a single PDM microphone, wired as left

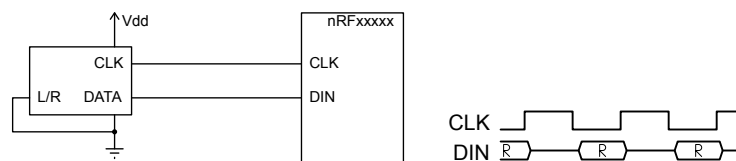


Figure 100: Example of a single PDM microphone, wired as right

Note that in a single-microphone (mono) configuration, depending on the microphone's implementation, either the left or the right channel (sampled at falling or rising CLK edge respectively) will contain reliable data.

If two microphones are used, one of them has to be set as left, the other as right (L/R pin tied high or to GND on the respective microphone). It is strongly recommended to use two microphones of exactly the same brand and type so that their timings in left and right operation match.

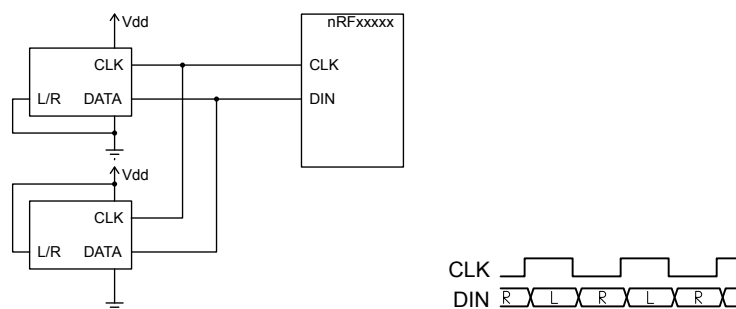


Figure 101: Example of two PDM microphones

### 7.1.23.7 Pin configuration

The CLK and DIN signals associated to the PDM module are mapped to physical pins according to the configuration specified in the PSEL.CLK and PSEL.DIN registers respectively. If the CONNECT field in any PSEL register is set to Disconnected, the associated PDM module signal will not be connected to the required physical pins, and will not operate properly.

The PSEL.CLK and PSEL.DIN registers and their configurations are only used as long as the PDM module is enabled, and retained only as long as the device is in System ON mode. See [POWER — Power control](#) on page 36 for more information about power modes. When the peripheral is disabled, the pins will behave as regular GPIOs, and use the configuration in their respective OUT bit field and PIN\_CNF[n] register.

To ensure correct behavior in the PDM module, the pins used by the PDM module must be configured in the GPIO peripheral as described in [Table 107: GPIO configuration before enabling peripheral](#) on page 329 before enabling the PDM module. This is to ensure that the pins used by the PDM module are driven correctly if the PDM module itself is temporarily disabled or the device temporarily enters System OFF. This configuration must be retained in the GPIO for the selected I/Os as long as the PDM module is supposed to be connected to an external PDM circuit.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

| PDM signal | PDM pin                  | Direction | Output value   | Comment |
|------------|--------------------------|-----------|----------------|---------|
| CLK        | As specified in PSEL.CLK | Output    | 0              |         |
| DIN        | As specified in PSEL.DIN | Input     | Not applicable |         |

Table 107: GPIO configuration before enabling peripheral

### 7.1.23.8 Registers

| Base address | Domain      | Peripheral | Instance  | Secure mapping | DMA security | Description                    | Configuration |
|--------------|-------------|------------|-----------|----------------|--------------|--------------------------------|---------------|
| 0x50026000   | APPLICATION | PDM        | PDM0 : S  | US             | SA           | Pulse density modulation       |               |
| 0x40026000   |             |            | PDM0 : NS |                |              | (digital microphone) interface |               |

Table 108: Instances

| Register        | Offset | Security | Description                                                                                                                         |
|-----------------|--------|----------|-------------------------------------------------------------------------------------------------------------------------------------|
| TASKS_START     | 0x000  |          | Starts continuous PDM transfer                                                                                                      |
| TASKS_STOP      | 0x004  |          | Stops PDM transfer                                                                                                                  |
| SUBSCRIBE_START | 0x080  |          | Subscribe configuration for task <a href="#">START</a>                                                                              |
| SUBSCRIBE_STOP  | 0x084  |          | Subscribe configuration for task <a href="#">STOP</a>                                                                               |
| EVENTS_STARTED  | 0x100  |          | PDM transfer has started                                                                                                            |
| EVENTS_STOPPED  | 0x104  |          | PDM transfer has finished                                                                                                           |
| EVENTS_END      | 0x108  |          | The PDM has written the last sample specified by SAMPLE.MAXCNT (or the last sample after a STOP task has been received) to Data RAM |
| PUBLISH_STARTED | 0x180  |          | Publish configuration for event <a href="#">STARTED</a>                                                                             |
| PUBLISH_STOPPED | 0x184  |          | Publish configuration for event <a href="#">STOPPED</a>                                                                             |
| PUBLISH_END     | 0x188  |          | Publish configuration for event <a href="#">END</a>                                                                                 |
| INTEN           | 0x300  |          | Enable or disable interrupt                                                                                                         |
| INTENSET        | 0x304  |          | Enable interrupt                                                                                                                    |
| INTENCLR        | 0x308  |          | Disable interrupt                                                                                                                   |
| ENABLE          | 0x500  |          | PDM module enable register                                                                                                          |
| PDMCLKCTRL      | 0x504  |          | PDM clock generator control                                                                                                         |
| MODE            | 0x508  |          | Defines the routing of the connected PDM microphones' signals                                                                       |

| Register      | Offset | Security | Description                                                                              |
|---------------|--------|----------|------------------------------------------------------------------------------------------|
| GAINL         | 0x518  |          | Left output gain adjustment                                                              |
| GAINR         | 0x51C  |          | Right output gain adjustment                                                             |
| RATIO         | 0x520  |          | Selects the ratio between PDM_CLK and output sample rate. Change PDMCLKCTRL accordingly. |
| PSEL.CLK      | 0x540  |          | Pin number configuration for PDM CLK signal                                              |
| PSEL.DIN      | 0x544  |          | Pin number configuration for PDM DIN signal                                              |
| MCLKCONFIG    | 0x54C  |          | Master clock generator configuration                                                     |
| SAMPLE.PTR    | 0x560  |          | RAM address pointer to write samples to with EasyDMA                                     |
| SAMPLE.MAXCNT | 0x564  |          | Number of samples to allocate memory for in EasyDMA mode                                 |

Table 109: Register overview

### 7.1.23.8.1 TASKS\_START

Address offset: 0x000

Starts continuous PDM transfer

|                  |            |             |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
|------------------|------------|-------------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|
| Bit number       |            |             |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| ID               |            |             |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A |
| Reset 0x00000000 |            |             |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| ID               | Acce Field | Value ID    | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| A                | W          | TASKS_START |       | Starts continuous PDM transfer                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
|                  |            | Trigger     | 1     | Trigger task                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |

### 7.1.23.8.2 TASKS\_STOP

Address offset: 0x004

Stops PDM transfer

|                  |            |            |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|------------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |            |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |            |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |            |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID   | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W          | TASKS_STOP |       | Stops PDM transfer                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Trigger    | 1     | Trigger task                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.23.8.3 SUBSCRIBE\_START

Address offset: 0x080

Subscribe configuration for task [START](#)

|                  |            |  |          |                                                                                       |  |                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|--|----------|---------------------------------------------------------------------------------------|--|--------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |  |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |  |          | B                                                                                     |  |                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |  |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0           |  |                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field |  | Value ID | Value                                                                                 |  | Description                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |  |          | [255..0]                                                                              |  | Channel that task <span>START</span> will subscribe to |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |  |          |                                                                                       |  |                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            |  | Disabled | 0                                                                                     |  | Disable subscription                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            |  | Enabled  | 1                                                                                     |  | Enable subscription                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

### 7.1.23.8.4 SUBSCRIBE\_STOP

Address offset: 0x084

Subscribe configuration for task **STOP**

|                  |            |          |                                                                                       |                      |                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|----------------------|-------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                      |                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |          | B                                                                                     |                      |                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |                      |                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 |                      | Description                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                              |                      | Channel that task <b>STOP</b> will subscribe to |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |                                                                                       |                      |                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Disable subscription |                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Enable subscription  |                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

### 7.1.23.8.5 EVENTS\_STARTED

Address offset: 0x100

PDM transfer has started

|                  |                   |              |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|-------------------|--------------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |                   |              |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |                   |              |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |                   |              |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field        | Value ID     | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW EVENTS_STARTED |              |       | PDM transfer has started                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                   | NotGenerated | 0     | Event not generated                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                   | Generated    | 1     | Event generated                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.23.8.6 EVENTS\_STOPPED

Address offset: 0x104

PDM transfer has finished

|                  |            |                |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |                |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |                |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |                |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID       | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | EVENTS_STOPPED |       | PDM transfer has finished                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | NotGenerated   | 0     | Event not generated                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Generated      | 1     | Event generated                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.23.8.7 EVENTS\_END

Address offset: 0x108

The PDM has written the last sample specified by **SAMPLE.MAXCNT** (or the last sample after a **STOP** task has been received) to Data RAM

|                  |            |              |       |    |                                                                                                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|------------------|------------|--------------|-------|----|---------------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| Bit number       |            |              | 31    | 30 | 29                                                                                                                                                | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| ID               |            |              | A     |    |                                                                                                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| Reset 0x00000000 |            |              | 0     | 0  | 0                                                                                                                                                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |
| ID               | Acce Field | Value ID     | Value |    | Description                                                                                                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| A                | RW         | EVENTS_END   |       |    | The PDM has written the last sample specified by<br><br>SAMPLE.MAXCNT (or the last sample after a STOP task has<br><br>been received) to Data RAM |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | NotGenerated | 0     |    | Event not generated                                                                                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | Generated    | 1     |    | Event generated                                                                                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

### 7.1.23.8.8 PUBLISH\_STARTED

Address offset: 0x180

Publish configuration for event **STARTED**

|                  |            |          |          |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|----------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                                                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |          |          | B                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |          | 0                                                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |
| ID               | Acce Field | Value ID | Value    | Description                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] | Channel that event <b>STARTED</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        | Disable publishing                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        | Enable publishing                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.23.8.9 PUBLISH\_STOPPED

Address offset: 0x184

Publish configuration for event **STOPPED**

|                  |            |       |          |          |       |          |  |  |  |             |                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-------|----------|----------|-------|----------|--|--|--|-------------|---------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |       |          |          |       |          |  |  |  | 31          | 30                                          | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |
| ID               |            |       |          |          |       |          |  |  |  | B           |                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  |    |   |   |   |   |   |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |       |          |          |       |          |  |  |  | 0           | 0                                           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |       | Value ID |          | Value |          |  |  |  | Description |                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | CHIDX |          |          |       | [255..0] |  |  |  |             | Channel that event STOPPED will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW         | EN    |          |          |       |          |  |  |  |             |                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |       |          | Disabled |       | 0        |  |  |  |             | Disable publishing                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |       |          | Enabled  |       | 1        |  |  |  |             | Enable publishing                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.23.8.10 PUBLISH\_END

Address offset: 0x188

Publish configuration for event **END**

|                  |      |       |          |    |          |                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------|-------|----------|----|----------|------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |      |       |          | 31 | 30       | 29                                             | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |      |       |          | B  |          |                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |      |       |          | 0  | 0        | 0                                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |
| ID               | Acce | Field | Value    | ID | Value    | Description                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW   | CHIDX |          |    | [255..0] | Channel that event <b>END</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW   | EN    |          |    |          |                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |       | Disabled |    | 0        | Disable publishing                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |       | Enabled  |    | 1        | Enable publishing                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |



### 7.1.23.8.11 INTEN

Address offset: 0x300

Enable or disable interrupt

| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|---------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |            |          | C B A                                                                                 |                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | STARTED  |                                                                                       | Enable or disable interrupt for event <a href="#">STARTED</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Disable                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Enable                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW         | STOPPED  |                                                                                       | Enable or disable interrupt for event <a href="#">STOPPED</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Disable                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Enable                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW         | END      |                                                                                       | Enable or disable interrupt for event <a href="#">END</a>     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Disable                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Enable                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.23.8.12 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|-----------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |            |          | C B A                                                                                 |                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| D                | Acce Field | Value ID | Value                                                                                 | Description                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW STARTED |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">STARTED</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Set      | 1                                                                                     | Enable                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Read: Disabled                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Read: Enabled                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW STOPPED |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">STOPPED</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Set      | 1                                                                                     | Enable                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Read: Disabled                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Read: Enabled                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW END     |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">END</a>     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Set      | 1                                                                                     | Enable                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Read: Disabled                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Read: Enabled                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.23.8.13 INTENCLR

Address offset: 0x308

Disable interrupt

|                  |            |          |                                                                                       |                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          | C B A                                                                                 |                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW STARTED |          |                                                                                       | Write '1' to disable interrupt for event <a href="#">STARTED</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Clear    | 1                                                                                     | Disable                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|--------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |            |          | C B A                                                                                 |                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW STOPPED | Disabled | 0                                                                                     | Read: Disabled                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Read: Enabled                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |          |                                                                                       | Write '1' to disable interrupt for event STOPPED |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Clear    | 1                                                                                     | Disable                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Read: Disabled                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW END     | Enabled  | 1                                                                                     | Read: Enabled                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |          |                                                                                       | Write '1' to disable interrupt for event END     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Clear    | 1                                                                                     | Disable                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Read: Disabled                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Read: Enabled                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

#### 7.1.23.8.14 ENABLE

Address offset: 0x500

## PDM module enable register

|                  |            |        |          |                                                                                       |  |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|--------|----------|---------------------------------------------------------------------------------------|--|------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |        |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |        |          | A                                                                                     |  |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |        |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                   |  |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field |        | Value ID | Value                                                                                 |  | Description                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | ENABLE |          |                                                                                       |  | Enable or disable PDM module |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |        | Disabled | 0                                                                                     |  | Disable                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |        | Enabled  | 1                                                                                     |  | Enable                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

#### 7.1.23.8.15 PDMCLKCTRL

Address offset: 0x504

## PDM clock generator control

| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |                                                                                                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|--|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |            |          | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A                           |  |                                                                                                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x08400000 |            |          | 0 0 0 0 1 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |  |                                                                                                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 |  | Description                                                                                                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | FREQ     |                                                                                       |  | PDM_CLK frequency configuration.                                                                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |          |                                                                                       |  | Enumerations are deprecated, use PDMCLKCTRL equation to find the register value. The 12 least significant bits of the register are ignored and shall be set to zero. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | 1000K    | 0x08000000                                                                            |  | PDM_CLK = 32 MHz / 32 = 1.000 MHz                                                                                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Default  | 0x08400000                                                                            |  | PDM_CLK = 32 MHz / 31 = 1.032 MHz. Nominal clock for RATIO=Ratio64.                                                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | 1067K    | 0x08800000                                                                            |  | PDM_CLK = 32 MHz / 30 = 1.067 MHz                                                                                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | 1231K    | 0x09800000                                                                            |  | PDM_CLK = 32 MHz / 26 = 1.231 MHz                                                                                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | 1280K    | 0x0A000000                                                                            |  | PDM_CLK = 32 MHz / 25 = 1.280 MHz. Nominal clock for RATIO=Ratio80.                                                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | 1333K    | 0x0A800000                                                                            |  | PDM_CLK = 32 MHz / 24 = 1.333 MHz                                                                                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

#### 7.1.23.8.16 MODE

Address offset: 0x508

Defines the routing of the connected PDM microphones' signals

| Bit number       |              |             | 31    | 30                                                                                             | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------|--------------|-------------|-------|------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| ID               |              |             |       |                                                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | B | A |
| Reset 0x00000000 |              |             | 0     | 0                                                                                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field   | Value ID    | Value | Description                                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW OPERATION |             |       | Mono or stereo operation                                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |              | Stereo      | 0     | Sample and store one pair (left + right) of 16-bit samples per RAM word R=[31:16]; L=[15:0]    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |              | Mono        | 1     | Sample and store two successive left samples (16 bits each) per RAM word L1=[31:16]; L0=[15:0] |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| B                | RW EDGE      |             |       | Defines on which PDM_CLK edge left (or mono) is sampled                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |              | LeftFalling | 0     | Left (or mono) is sampled on falling edge of PDM_CLK                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |              | LeftRising  | 1     | Left (or mono) is sampled on rising edge of PDM_CLK                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.23.8.17 GAINL

Address offset: 0x518

Left output gain adjustment

| Bit number       |             |          | 31                               | 30                                                                                                       | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
|------------------|-------------|----------|----------------------------------|----------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ID               |             |          |                                  |                                                                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000028 |             |          | 0                                | 0                                                                                                        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |   |   |
| ID               | Acce Field  | Value ID | Value                            | Description                                                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW          | GAINL    |                                  | Left output gain adjustment, in 0.5 dB steps, around the default module gain (see electrical parameters) |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |             |          |                                  | 0x00 -20 dB gain adjust                                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |             |          |                                  | 0x01 -19.5 dB gain adjust                                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |             |          |                                  | (...)                                                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |             |          |                                  | 0x27 -0.5 dB gain adjust                                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |             |          |                                  | 0x28 0 dB gain adjust                                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |             |          |                                  | 0x29 +0.5 dB gain adjust                                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |             |          |                                  | (...)                                                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |             |          |                                  | 0x4F +19.5 dB gain adjust                                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |             |          |                                  | 0x50 +20 dB gain adjust                                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  | MinGain     | 0x00     | -20 dB gain adjustment (minimum) |                                                                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  | DefaultGain | 0x28     | 0 dB gain adjustment             |                                                                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  | MaxGain     | 0x50     | +20 dB gain adjustment (maximum) |                                                                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.23.8.18 GAINR

Address offset: 0x51C

Right output gain adjustment

| Bit number |  |  | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 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### 7.1.23.8.19 RATIO

Address offset: 0x520

Selects the ratio between PDM\_CLK and output sample rate. Change PDMCLKCTRL accordingly.

|                  |            |          |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| Bit number       |            |          |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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|                  |            | Ratio64  | 0     | Ratio of 64                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Ratio80  | 1     | Ratio of 80                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.23.8.20 PSEL.CLK

Address offset: 0x540

Pin number configuration for PDM CLK signal

|                  |            |              |                                                                                       |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| ID               | Acce Field | Value ID     | Value                                                                                 | Description |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW PIN     |              | [0..31]                                                                               | Pin number  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW PORT    |              | [0..1]                                                                                | Port number |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW CONNECT |              |                                                                                       | Connection  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disconnected | 1                                                                                     | Disconnect  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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Address offset: 0x544

Pin number configuration for PDM DIN signal

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### 7.1.23.8.22 MCLKCONFIG

Address offset: 0x54C

Master clock generator configuration

| Bit number       |             | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                               |
|------------------|-------------|---------------------------------------------------------------------------------------|-------------------------------|
| ID               |             | A                                                                                     |                               |
| Reset 0x00000000 |             | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                               |
| ID               | Acces Field | Value ID                                                                              | Description                   |
| A                | RW SRC      |                                                                                       | Master clock source selection |
|                  |             | PCLK32M                                                                               | 32 MHz peripheral clock       |
|                  |             | ACLK                                                                                  | Audio PLL clock               |

### 7.1.23.8.23 SAMPLE.PTR

Address offset: 0x560

RAM address pointer to write samples to with EasyDMA

| Bit number       |              | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                          |
|------------------|--------------|---------------------------------------------------------------------------------------|------------------------------------------|
| ID               |              | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A                           |                                          |
| Reset 0x00000000 |              | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                          |
| ID               | Acces Field  | Value ID                                                                              | Description                              |
| A                | RW SAMPLEPTR |                                                                                       | Address to write PDM samples to over DMA |

**Note:** See the memory chapter for details about which memories are available for EasyDMA.

### 7.1.23.8.24 SAMPLE.MAXCNT

Address offset: 0x564

Number of samples to allocate memory for in EasyDMA mode

| Bit number       |             | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                   |
|------------------|-------------|---------------------------------------------------------------------------------------|---------------------------------------------------|
| ID               |             | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A                           |                                                   |
| Reset 0x00000000 |             | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                   |
| ID               | Acces Field | Value ID                                                                              | Description                                       |
| A                | RW BUFFSIZE |                                                                                       | Length of DMA RAM allocation in number of samples |

## 7.1.23.9 Electrical specification

### 7.1.23.9.1 PDM Electrical Specification

| Symbol                  | Description                                                                                          | Min. | Typ. | Max. | Units |
|-------------------------|------------------------------------------------------------------------------------------------------|------|------|------|-------|
| $f_{\text{PDM,CLK},64}$ | PDM clock speed. PDMCLKCTRL = Default (Setting needed for 16 MHz sample frequency @ RATIO = Ratio64) | ..   | ..   | ..   | MHz   |
| $f_{\text{PDM,CLK},80}$ | PDM clock speed. PDMCLKCTRL = 1280K (Setting needed for 16 MHz sample frequency @ RATIO = Ratio80)   | ..   | ..   | ..   | MHz   |
| $t_{\text{PDM,JITTER}}$ | Jitter in PDM clock output                                                                           | ..   | ..   | ..   | ns    |
| $T_{\text{dPDM,CLK}}$   | PDM clock duty cycle                                                                                 | ..   | ..   | ..   | %     |
| $t_{\text{PDM,DATA}}$   | Decimation filter delay                                                                              | ..   | ..   | ..   | ms    |

| Symbol            | Description                                             | Min. | Typ. | Max. | Units |
|-------------------|---------------------------------------------------------|------|------|------|-------|
| $t_{PDM,cv}$      | Allowed clock edge to data valid                        | ..   | ..   | ..   | ns    |
| $t_{PDM,ci}$      | Allowed (other) clock edge to data invalid              | ..   | ..   | ..   | ns    |
| $t_{PDM,s}$       | Data setup time at $f_{PDM,CLK}=1.024$ MHz or 1.280 MHz | ..   | ..   | ..   | ns    |
| $t_{PDM,h}$       | Data hold time at $f_{PDM,CLK}=1.024$ MHz or 1.280 MHz  | ..   | ..   | ..   | ns    |
| $G_{PDM,default}$ | Default (reset) absolute gain of the PDM module         | ..   | ..   | ..   | dB    |

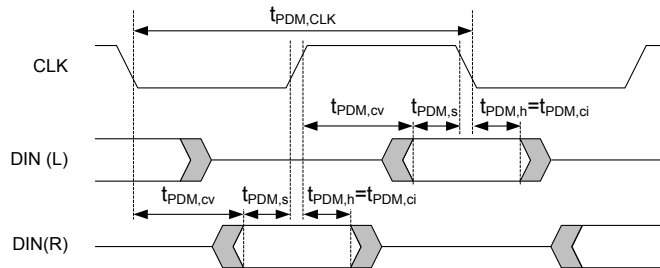


Figure 102: PDM timing diagram

## 7.1.24 PWM — Pulse width modulation

The pulse with modulation (PWM) module enables the generation of pulse width modulated signals on GPIO. The module implements an up or up-and-down counter with four PWM channels that drive assigned GPIOs.

The following are the main features of a PWM module:

- Programmable PWM frequency
- Up to four PWM channels with individual polarity and duty cycle values
- Edge or center-aligned pulses across PWM channels
- Multiple duty cycle arrays (sequences) defined in RAM
- Autonomous and glitch-free update of duty cycle values directly from memory through EasyDMA (no CPU involvement)
- Change of polarity, duty cycle, and base frequency possibly on every PWM period
- RAM sequences can be repeated or connected into loops

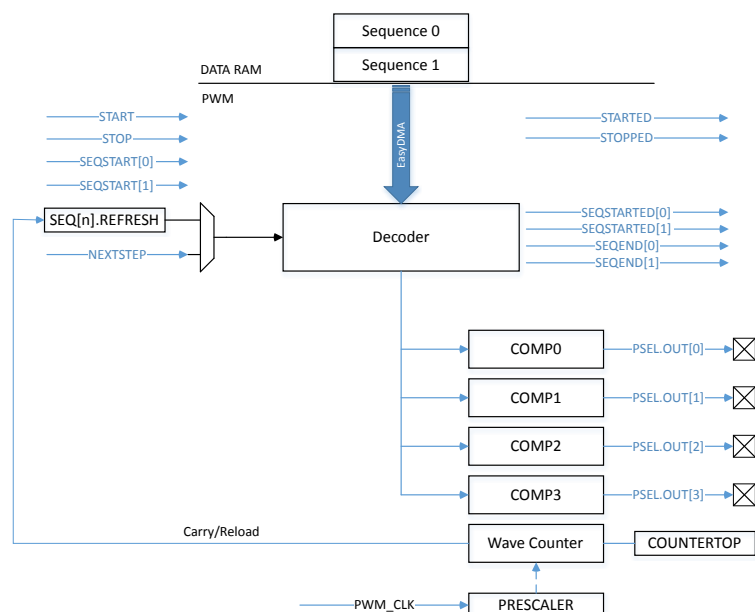


Figure 103: PWM module

### 7.1.24.1 Wave counter

The wave counter is responsible for generating the pulses at a duty cycle that depends on the compare values, and at a frequency that depends on COUNTERTOP.

There is one common 15-bit counter with four compare channels. Thus, all four channels will share the same period (PWM frequency), but can have individual duty cycle and polarity. The polarity is set by a value read from RAM (see figure [Figure 106: Decoder memory access modes](#) on page 342). Whether the counter counts up, or up and down, is controlled by the MODE register.

The timer top value is controlled by the COUNTERTOP register. This register value, in conjunction with the selected PRESCALER of the PWM\_CLK, will result in a given PWM period. A COUNTERTOP value smaller than the compare setting will result in a state where no PWM edges are generated. OUT[n] is held high, given that the polarity is set to FallingEdge. All compare registers are internal and can only be configured through decoder presented later. COUNTERTOP can be safely written at any time.

Sampling follows the START task. If DECODER.LOAD=WaveForm, the register value is ignored and taken from RAM instead (see section [Decoder with EasyDMA](#) on page 342 for more details). If DECODER.LOAD is anything else than the WaveForm, it is sampled following a STARTSEQ[n] task and when loading a new value from RAM during a sequence playback.

The following figure shows the counter operating in up mode (MODE=PWM\_MODE\_Up), with three PWM channels with the same frequency but different duty cycle:

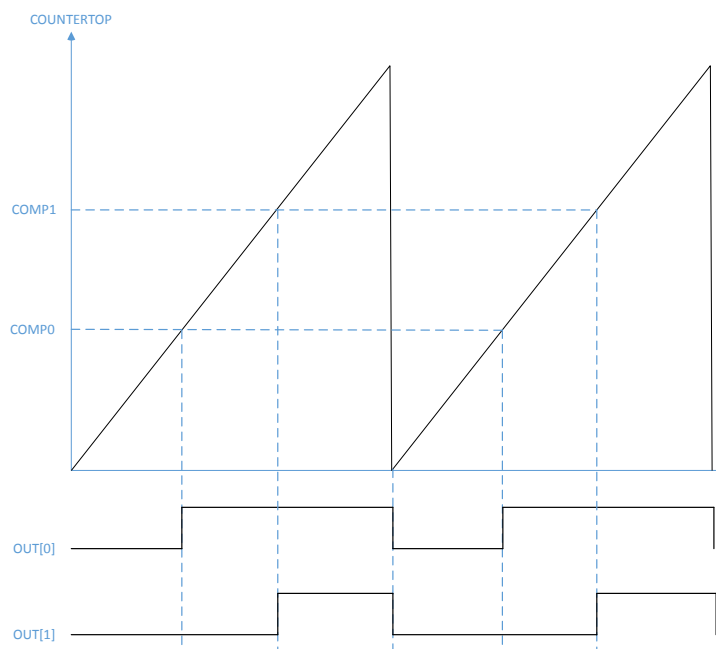


Figure 104: PWM counter in up mode example - FallingEdge polarity

The counter is automatically reset to zero when COUNTERTOP is reached and OUT[n] will invert. OUT[n] is held low if the compare value is 0 and held high if set to COUNTERTOP, given that the polarity is set to

**FallingEdge.** Counter running in up mode results in pulse widths that are edge-aligned. The following is the code for the counter in up mode example:

```
uint16_t pwm_seq[4] = {PWM_CH0_DUTY, PWM_CH1_DUTY, PWM_CH2_DUTY, PWM_CH3_DUTY};
NRF_PWM0->PSEL.OUT[0] = (first_pin << PWM_PSEL_OUT_PIN_Pos) |
                        (PWM_PSEL_OUT_CONNECT_Connected <<
                         PWM_PSEL_OUT_CONNECT_Pos);
NRF_PWM0->PSEL.OUT[1] = (second_pin << PWM_PSEL_OUT_PIN_Pos) |
                        (PWM_PSEL_OUT_CONNECT_Connected <<
                         PWM_PSEL_OUT_CONNECT_Pos);
NRF_PWM0->ENABLE      = (PWM_ENABLE_ENABLE_Enabled << PWM_ENABLE_ENABLE_Pos);
NRF_PWM0->MODE        = (PWM_MODE_UPDOWN_Up << PWM_MODE_UPDOWN_Pos);
NRF_PWM0->PRESCALER   = (PWM_PRESCALER_PRESCALER_DIV_1 <<
                         PWM_PRESCALER_PRESCALER_Pos);
NRF_PWM0->COUNTERTOP  = (16000 << PWM_COUNTERTOP_COUNTERTOP_Pos); //1 msec
NRF_PWM0->LOOP        = (PWM_LOOP_CNT_Disabled << PWM_LOOP_CNT_Pos);
NRF_PWM0->DECODER     = (PWM_DECODER_LOAD_Individual << PWM_DECODER_LOAD_Pos) |
                        (PWM_DECODER_MODE_RefreshCount << PWM_DECODER_MODE_Pos);
NRF_PWM0->SEQ[0].PTR  = ((uint32_t)(pwm_seq) << PWM_SEQ_PTR_PTR_Pos);
NRF_PWM0->SEQ[0].CNT  = ((sizeof(pwm_seq) / sizeof(uint16_t)) <<
                         PWM_SEQ_CNT_CNT_Pos);
NRF_PWM0->SEQ[0].REFRESH = 0;
NRF_PWM0->SEQ[0].ENDDELAY = 0;
NRF_PWM0->TASKS_SEQSTART[0] = 1;
```

When the counter is running in up mode, the following formula can be used to compute the PWM period and the step size:

PWM period:  $T_{PWM(Up)} = T_{PWM\_CLK} * COUNTERTOP$

Step width/Resolution:  $T_{steps} = T_{PWM\_CLK}$

The following figure shows the counter operating in up-and-down mode (MODE=PWM\_MODE\_UpAndDown), with two PWM channels with the same frequency but different duty cycle and output polarity:



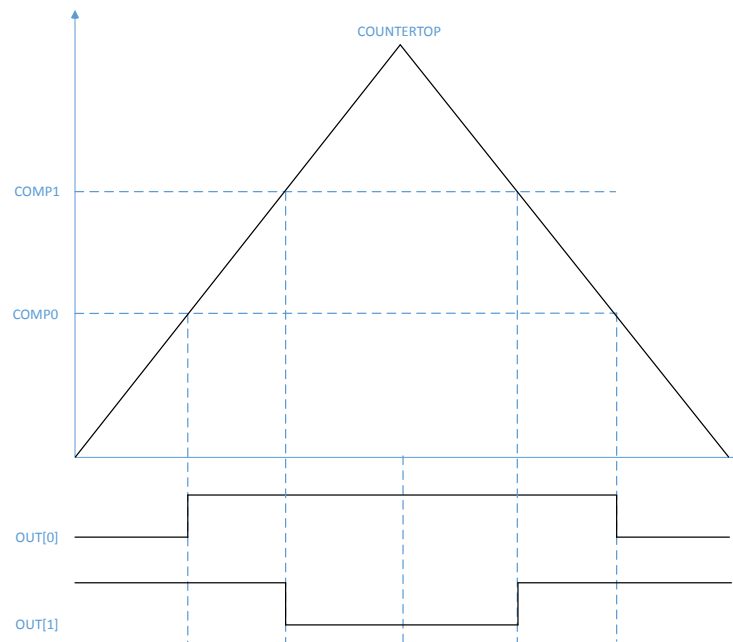


Figure 105: PWM counter in up-and-down mode example

The counter starts decrementing to zero when COUNTERTOP is reached and will invert the OUT[n] when compare value is hit for the second time. This results in a set of pulses that are center-aligned. The following is the code for the counter in up-and-down mode example:

```
uint16_t pwm_seq[4] = {PWM_CH0_DUTY, PWM_CH1_DUTY, PWM_CH2_DUTY, PWM_CH3_DUTY};
NRF_PWM0->PSEL.OUT[0] = (first_pin << PWM_PSEL_OUT_PIN_Pos) |
    (PWM_PSEL_OUT_CONNECT_Connected <<
        PWM_PSEL_OUT_CONNECT_Pos);
NRF_PWM0->PSEL.OUT[1] = (second_pin << PWM_PSEL_OUT_PIN_Pos) |
    (PWM_PSEL_OUT_CONNECT_Connected <<
        PWM_PSEL_OUT_CONNECT_Pos);
NRF_PWM0->ENABLE = (PWM_ENABLE_ENABLE_Enabled << PWM_ENABLE_ENABLE_Pos);
NRF_PWM0->MODE = (PWM_MODE_UPDOWN_UpAndDown << PWM_MODE_UPDOWN_Pos);
NRF_PWM0->PRESCALER = (PWM_PRESCALER_PRESCALER_DIV_1 <<
    PWM_PRESCALER_PRESCALER_Pos);
NRF_PWM0->COUNTERTOP = (16000 << PWM_COUNTERTOP_COUNTERTOP_Pos); //1 msec
NRF_PWM0->LOOP = (PWM_LOOP_CNT_Disabled << PWM_LOOP_CNT_Pos);
NRF_PWM0->DECODER = (PWM_DECODER_LOAD_Individual << PWM_DECODER_LOAD_Pos) |
    (PWM_DECODER_MODE_RefreshCount << PWM_DECODER_MODE_Pos);
NRF_PWM0->SEQ[0].PTR = ((uint32_t)(pwm_seq) << PWM_SEQ_PTR_PTR_Pos);
NRF_PWM0->SEQ[0].CNT = ((sizeof(pwm_seq) / sizeof(uint16_t)) <<
    PWM_SEQ_CNT_CNT_Pos);
NRF_PWM0->SEQ[0].REFRESH = 0;
NRF_PWM0->SEQ[0].ENDDELAY = 0;
NRF_PWM0->TASKS_SEQSTART[0] = 1;
```

When the counter is running in up-and-down mode, the following formula can be used to compute the PWM period and the step size:

$$T_{\text{PWM(Up And Down)}} = T_{\text{PWM\_CLK}} * 2 * \text{COUNTERTOP}$$

$$\text{Step width/Resolution: } T_{\text{steps}} = T_{\text{PWM\_CLK}} * 2$$

PWM parameters are organized into a sequence containing at least one half word (16 bit). Its most significant bit[15] denotes the polarity of the OUT[n] while bit[14:0] is the 15-bit compare value.

|                  |    |          |             |                                                                                       |                                             |                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|----|----------|-------------|---------------------------------------------------------------------------------------|---------------------------------------------|----------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |    |          |             | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                             |                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Id               |    |          |             |                                                                                       |                                             |                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  | B A A A A A A A A A A A A A A A A A |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |    |          |             | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0               |                                             |                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Id               | RW | Field    | Value Id    | Value                                                                                 |                                             | Description                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW | COMPARE  |             |                                                                                       |                                             | Duty cycle setting - value loaded to internal compare register |  |  |  |  |  |  |  |  |  |  |  |  |  |                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW | POLARITY |             |                                                                                       |                                             | Edge polarity of GPIO.                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |    |          | RisingEdge  | 0                                                                                     | First edge within the PWM period is rising  |                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |    |          | FallingEdge | 1                                                                                     | First edge within the PWM period is falling |                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

The diagram illustrates three different decoder load configurations, each showing a vertical stack of components (P, O, L) and their connections to comparators (COMP0, COMP1, COMP2, COMP3) or a counter (COUNTERTOP).

**DECODER.LOAD=Common**

SEQ[n].PTR

Increasing Data RAM address

Each component (P, O, L) is connected to a single output line, which is then connected to a single output line (COMP0, COMP1, COMP2, COMP3). This configuration is labeled "Common".

**DECODER.LOAD=Grouped**

Each component (P, O, L) is connected to a single output line, which is then connected to a single output line (COMP0, COMP1, COMP2, COMP3). This configuration is labeled "Grouped".

**DECODER.LOAD=Single**

Each component (P, O, L) is connected to a single output line, which is then connected to a single output line (COMP0, COMP1, COMP2, COMP3). This configuration is labeled "Single".

**DECODER.LOAD=WaveForm**

Each component (P, O, L) is connected to a single output line, which is then connected to a single output line (COMP0, COMP1, COMP2, COUNTERTOP). This configuration is labeled "WaveForm".

A special mode of operation is available when `DECODER.LOAD` is set to `WaveForm`. In this mode, up to three PWM channels can be enabled - `OUT[0]` to `OUT[2]`. In RAM, four values are loaded at a time: the first, second and third location are used to load the values, and the fourth RAM location is used to load the `COUNTERTOP` register. This way one can have up to three PWM channels with a frequency base that changes on a per PWM period basis. This mode of operation is useful for arbitrary wave form generation in applications, such as LED lighting.

The register `SEQ[n].REFRESH=N` (one per sequence  $n=0$  or  $1$ ) will instruct a new RAM stored pulse width value on every  $(N+1)^{\text{th}}$  PWM period. Setting the register to zero will result in a new duty cycle update every PWM period, as long as the minimum PWM period is observed.

Note that registers `SEQ[n].REFRESH` and `SEQ[n].ENDDELAY` are ignored when `DECODER.MODE=NextStep`. The next value is loaded upon every received `NEXTSTEP` task.

`SEQ[n].PTR` is the pointer used to fetch `COMPARE` values from RAM. If the `SEQ[n].PTR` is not pointing to a RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See [Memory](#) on page 18 for more information about the different memory regions. After the `SEQ[n].PTR` is set to the desired RAM location, the `SEQ[n].CNT` register must be set to number of 16-bit half words in the sequence. It is important to observe that the Grouped mode requires one half word per group, while the Single mode requires one half word per channel, thus increasing the RAM size occupation. If PWM generation is not running when the `SEQSTART[n]` task is triggered, the task will load the first value from RAM and then start the PWM generation. A `SEQSTARTED[n]` event is generated as soon as the EasyDMA has read the first PWM parameter from RAM and the wave counter has started executing it. When `LOOP.CNT=0`, sequence  $n=0$  or  $1$  is played back once. After the last value in the sequence has been loaded and started executing, a `SEQEND[n]` event is generated. The PWM generation will then continue with the last loaded value. The following figure illustrates an example of such simple playback:

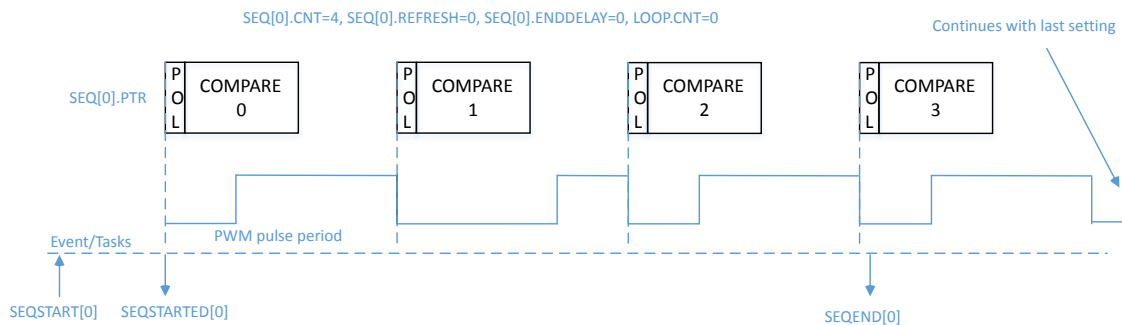


Figure 107: Simple sequence example

Figure depicts the source code used for configuration and timing details in a sequence where only sequence 0 is used and only run once with a new PWM duty cycle for each period.

```

NRF_PWM0->PSEL.OUT[0] = (first_pin << PWM_PSEL_OUT_PIN_Pos) |
                        (PWM_PSEL_OUT_CONNECT_Connected <<
                          PWM_PSEL_OUT_CONNECT_Pos);
NRF_PWM0->ENABLE       = (PWM_ENABLE_ENABLE_Enabled << PWM_ENABLE_ENABLE_Pos);
NRF_PWM0->MODE         = (PWM_MODE_UPDOWN_Up << PWM_MODE_UPDOWN_Pos);
NRF_PWM0->PRESCALER    = (PWM_PRESCALER_PRESCALER_DIV_1 <<
                          PWM_PRESCALER_PRESCALER_Pos);
NRF_PWM0->COUNTERTOP   = (16000 << PWM_COUNTERTOP_COUNTERTOP_Pos); //1 msec
NRF_PWM0->LOOP         = (PWM_LOOP_CNT_Disabled << PWM_LOOP_CNT_Pos);
NRF_PWM0->DECODER      = (PWM_DECODER_LOAD_Common << PWM_DECODER_LOAD_Pos) |
                        (PWM_DECODER_MODE_RefreshCount << PWM_DECODER_MODE_Pos);
NRF_PWM0->SEQ[0].PTR   = ((uint32_t)(seq0_ram) << PWM_SEQ_PTR_PTR_Pos);
NRF_PWM0->SEQ[0].CNT   = ((sizeof(seq0_ram) / sizeof(uint16_t)) <<
                          PWM_SEQ_CNT_CNT_Pos);
NRF_PWM0->SEQ[0].REFRESH = 0;
NRF_PWM0->SEQ[0].ENDDELAY = 0;
NRF_PWM0->TASKS_SEQSTART[0] = 1;

```

To completely stop the PWM generation and force the associated pins to a defined state, a STOP task can be triggered at any time. A STOPPED event is generated when the PWM generation has stopped at the end of currently running PWM period, and the pins go into their idle state as defined in GPIO OUT register. PWM generation can then only be restarted through a SEQSTART[n] task. SEQSTART[n] will resume PWM generation after having loaded the first value from the RAM buffer defined in the SEQ[n].PTR register.

The table below indicates when specific registers get sampled by the hardware. Care should be taken when updating these registers to avoid that values are applied earlier than expected.

| Register        | Taken into account by hardware                                                                                                               | Recommended (safe) update                                                                                                                                                                    |
|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SEQ[n].PTR      | When sending the SEQSTART[n] task                                                                                                            | After having received the SEQSTARTED[n] event                                                                                                                                                |
| SEQ[n].CNT      | When sending the SEQSTART[n] task                                                                                                            | After having received the SEQSTARTED[n] event                                                                                                                                                |
| SEQ[0].ENDDELAY | When sending the SEQSTART[0] task                                                                                                            | Before starting sequence [0] through a SEQSTART[0] task                                                                                                                                      |
|                 | Every time a new value from sequence [0] has been loaded from RAM and gets applied to the Wave Counter (indicated by the PWMPERIODEND event) | When no more value from sequence [0] gets loaded from RAM (indicated by the SEQEND[0] event)<br><br>At any time during sequence [1] (which starts when the SEQSTARTED[1] event is generated) |
| SEQ[1].ENDDELAY | When sending the SEQSTART[1] task                                                                                                            | Before starting sequence [1] through a SEQSTART[1] task                                                                                                                                      |
|                 | Every time a new value from sequence [1] has been loaded from RAM and gets applied to the Wave Counter (indicated by the PWMPERIODEND event) | When no more value from sequence [1] gets loaded from RAM (indicated by the SEQEND[1] event)<br><br>At any time during sequence [0] (which starts when the SEQSTARTED[0] event is generated) |
| SEQ[0].REFRESH  | When sending the SEQSTART[0] task                                                                                                            | Before starting sequence [0] through a SEQSTART[0] task                                                                                                                                      |
|                 | Every time a new value from sequence [0] has been loaded from RAM and gets applied to the Wave Counter (indicated by the PWMPERIODEND event) | At any time during sequence [1] (which starts when the SEQSTARTED[1] event is generated)                                                                                                     |
| SEQ[1].REFRESH  | When sending the SEQSTART[1] task                                                                                                            | Before starting sequence [1] through a SEQSTART[1] task                                                                                                                                      |
|                 | Every time a new value from sequence [1] has been loaded from RAM and gets applied to the Wave Counter (indicated by the PWMPERIODEND event) | At any time during sequence [0] (which starts when the SEQSTARTED[0] event is generated)                                                                                                     |
| COUNTERTOP      | In DECODER.LOAD=WaveForm: this register is ignored.                                                                                          | Before starting PWM generation through a SEQSTART[n] task                                                                                                                                    |
|                 | In all other LOAD modes: at the end of current PWM period (indicated by the PWMPERIODEND event)                                              | After a STOP task has been triggered, and the STOPPED event has been received.                                                                                                               |
| MODE            | Immediately                                                                                                                                  | Before starting PWM generation through a SEQSTART[n] task                                                                                                                                    |
|                 |                                                                                                                                              | After a STOP task has been triggered, and the STOPPED event has been received.                                                                                                               |
| DECODER         | Immediately                                                                                                                                  | Before starting PWM generation through a SEQSTART[n] task                                                                                                                                    |
|                 |                                                                                                                                              | After a STOP task has been triggered, and the STOPPED event has been received.                                                                                                               |
| PRESCALER       | Immediately                                                                                                                                  | Before starting PWM generation through a SEQSTART[n] task                                                                                                                                    |
|                 |                                                                                                                                              | After a STOP task has been triggered, and the STOPPED event has been received.                                                                                                               |
| LOOP            | Immediately                                                                                                                                  | Before starting PWM generation through a SEQSTART[n] task                                                                                                                                    |
|                 |                                                                                                                                              | After a STOP task has been triggered, and the STOPPED event has been received.                                                                                                               |
| PSEL.OUT[n]     | Immediately                                                                                                                                  | Before enabling the PWM instance through the ENABLE register                                                                                                                                 |

Table 110: When to safely update PWM registers

**Note:** SEQ[n].REFRESH and SEQ[n].ENDDELAY are ignored at the end of a complex sequence, indicated by a LOOPSDONE event. The reason for this is that the last value loaded from RAM is maintained until further action from software (restarting a new sequence, or stopping PWM generation).

A more complex example, where LOOP.CNT>0, is shown in the following figure:

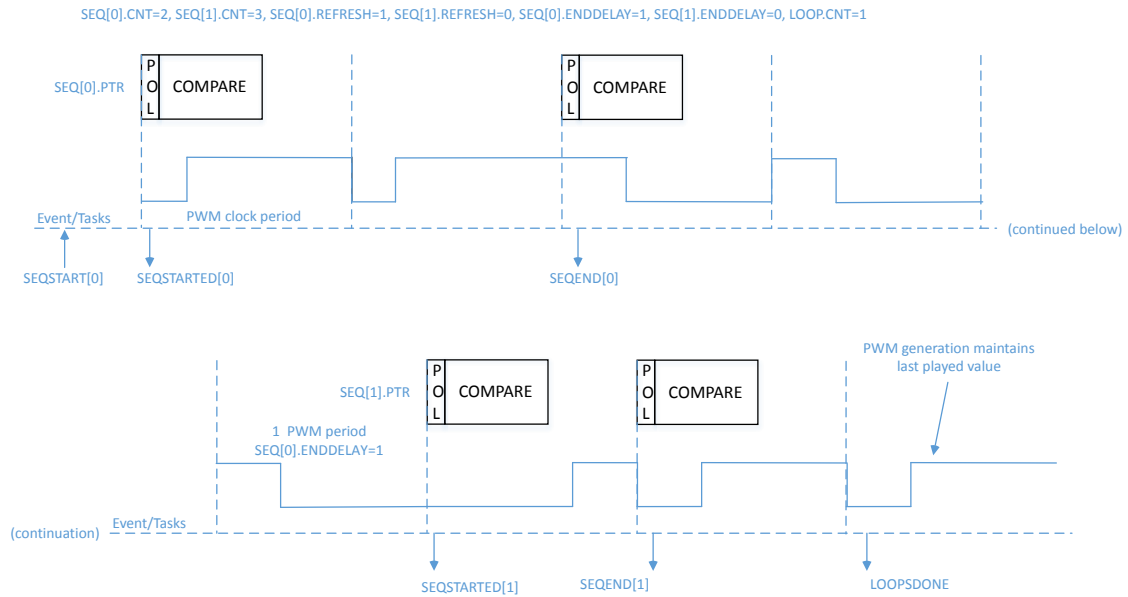


Figure 108: Example using two sequences

In this case, an automated playback takes place, consisting of SEQ[0], delay 0, SEQ[1], delay 1, then again SEQ[0], etc. The user can choose to start a complex playback with SEQ[0] or SEQ[1] through sending the SEQSTART[0] or SEQSTART[1] task. The complex playback always ends with delay 1.

The two sequences 0 and 1 are defined by the addresses of value tables in RAM (pointed to by SEQ[n].PTR) and the buffer size (SEQ[n].CNT). The rate at which a new value is loaded is defined individually for each sequence by SEQ[n].REFRESH. The chaining of sequence 1 following the sequence 0 is implicit, the LOOP.CNT register allows the chaining of sequence 1 to sequence 0 for a determined number of times. In other words, it allows to repeat a complex sequence a number of times in a fully automated way.

In the following code example, sequence 0 is defined with SEQ[0].REFRESH set to 1, meaning that a new PWM duty cycle is pushed every second PWM period. This complex sequence is started with the SEQSTART[0] task, so SEQ[0] is played first. Since SEQ[0].ENDDelay=1 there will be one PWM period delay between last period on sequence 0 and the first period on sequence 1. Since SEQ[1].ENDDelay=0 there is no delay 1, so SEQ[0] would be started immediately after the end of SEQ[1]. However, as LOOP.CNT is

1, the playback stops after having played SEQ[1] only once, and both SEQEND[1] and LOOPSDONE are generated (their order is not guaranteed in this case).

```

NRF_PWM0->PSEL.OUT[0] = (first_pin << PWM_PSEL_OUT_PIN_Pos) |
                        (PWM_PSEL_OUT_CONNECT_Connected <<
                         PWM_PSEL_OUT_CONNECT_Pos);
NRF_PWM0->ENABLE      = (PWM_ENABLE_ENABLE_Enabled << PWM_ENABLE_ENABLE_Pos);
NRF_PWM0->MODE        = (PWM_MODE_UPDOWN_Up << PWM_MODE_UPDOWN_Pos);
NRF_PWM0->PRESCALER   = (PWM_PRESCALER_PRESCALER_DIV_1 <<
                         PWM_PRESCALER_PRESCALER_Pos);
NRF_PWM0->COUNTERTOP  = (16000 << PWM_COUNTERTOP_COUNTERTOP_Pos); //1 msec
NRF_PWM0->LOOP        = (1 << PWM_LOOP_CNT_Pos);
NRF_PWM0->DECODER     = (PWM_DECODER_LOAD_Common << PWM_DECODER_LOAD_Pos) |
                        (PWM_DECODER_MODE_RefreshCount << PWM_DECODER_MODE_Pos);
NRF_PWM0->SEQ[0].PTR   = ((uint32_t)(seq0_ram) << PWM_SEQ_PTR_PTR_Pos);
NRF_PWM0->SEQ[0].CNT   = ((sizeof(seq0_ram) / sizeof(uint16_t)) <<
                         PWM_SEQ_CNT_CNT_Pos);

NRF_PWM0->SEQ[0].REFRESH = 1;
NRF_PWM0->SEQ[0].ENDDELAY = 1;
NRF_PWM0->SEQ[1].PTR   = ((uint32_t)(seq1_ram) << PWM_SEQ_PTR_PTR_Pos);
NRF_PWM0->SEQ[1].CNT   = ((sizeof(seq1_ram) / sizeof(uint16_t)) <<
                         PWM_SEQ_CNT_CNT_Pos);

NRF_PWM0->SEQ[1].REFRESH = 0;
NRF_PWM0->SEQ[1].ENDDELAY = 0;
NRF_PWM0->TASKS_SEQSTART[0] = 1;

```

The decoder can also be configured to asynchronously load new PWM duty cycle. If the DECODER.MODE register is set to NextStep, then the NEXTSTEP task will cause an update of internal compare registers on the next PWM period.

The following figures provide an overview of each part of an arbitrary sequence, in various modes (LOOP.CNT=0 and LOOP.CNT>0). In particular, the following are represented:

- Initial and final duty cycle on the PWM output(s)
- Chaining of SEQ[0] and SEQ[1] if LOOP.CNT>0
- Influence of registers on the sequence
- Events generated during a sequence
- DMA activity (loading of next value and applying it to the output(s))

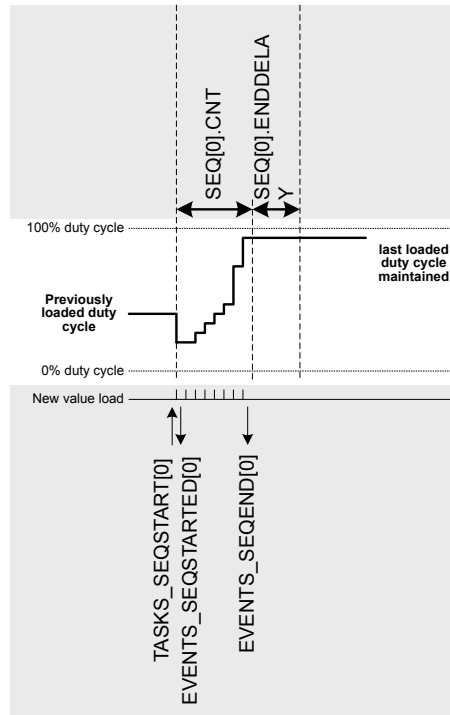


Figure 109: Single shot (LOOP.CNT=0)

**Note:** The single-shot example also applies to SEQ[1]. Only SEQ[0] is represented for simplicity.

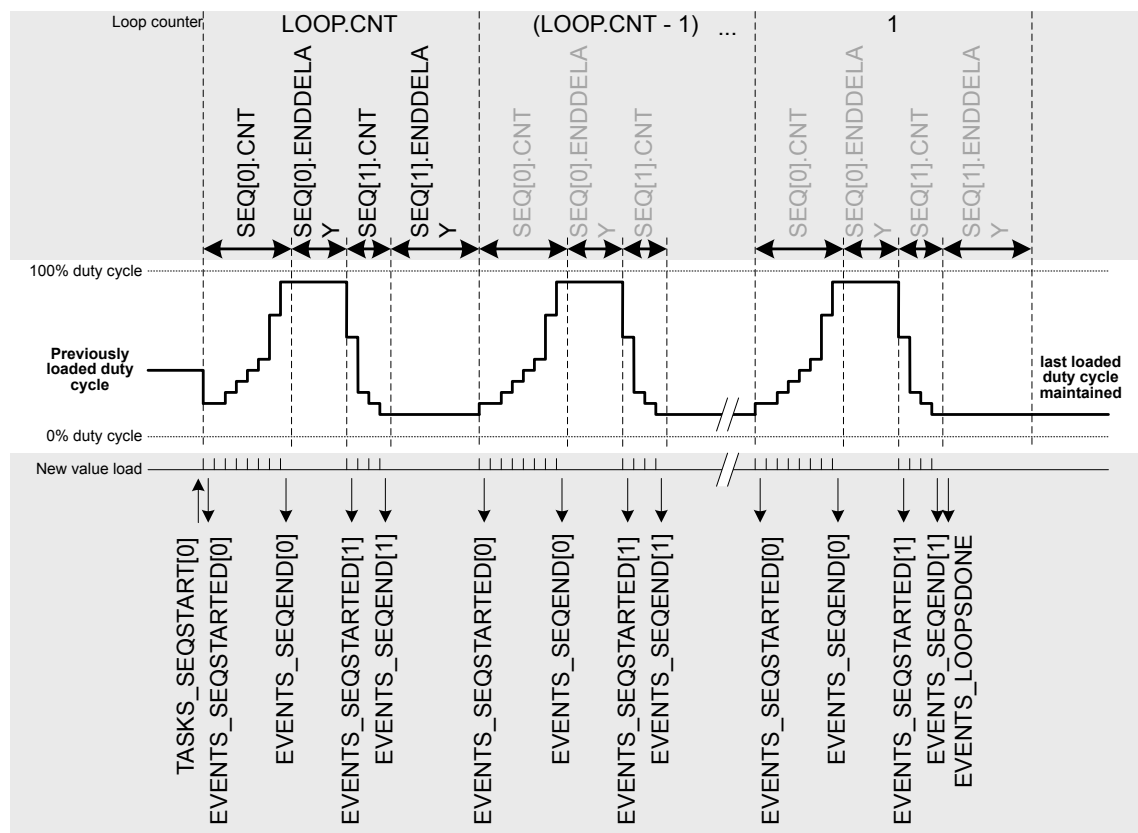


Figure 110: Complex sequence (LOOP.CNT&gt;0) starting with SEQ[0]



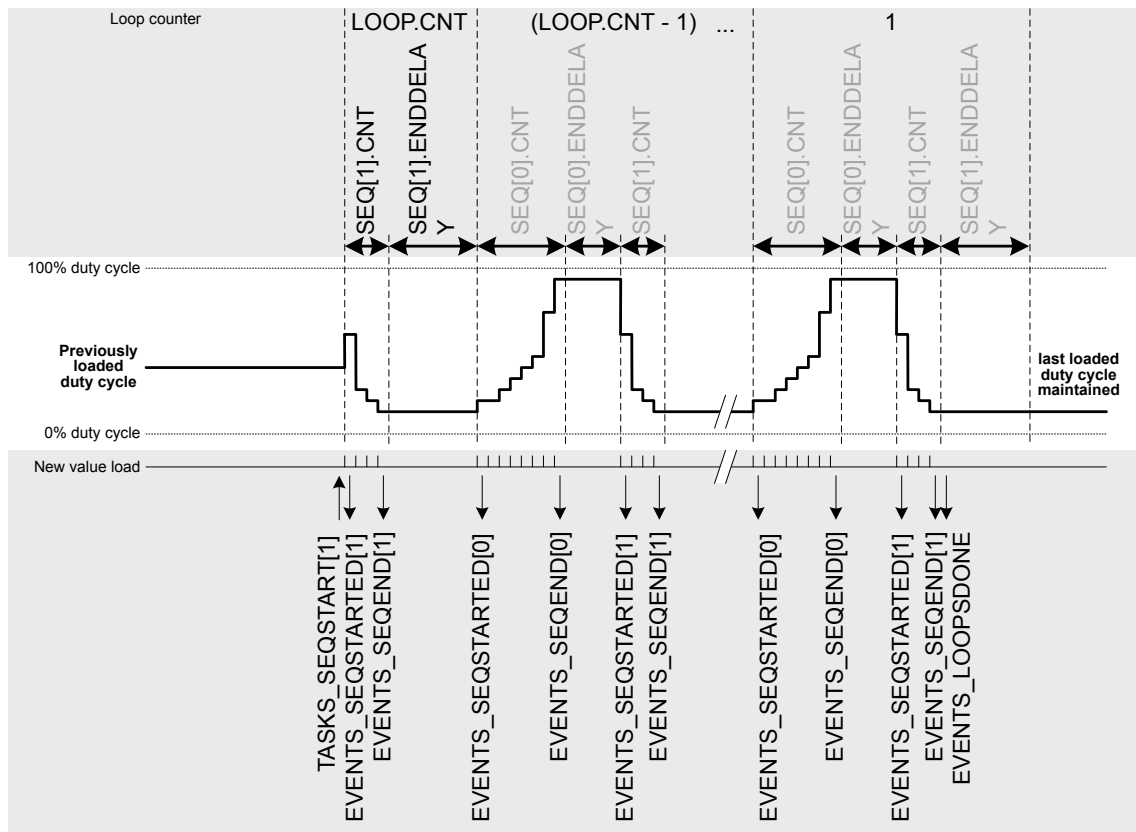


Figure 111: Complex sequence ( $LOOP.CNT > 0$ ) starting with  $SEQ[1]$

**Note:** If a sequence is in use in a simple or complex sequence, it must have a length of  $SEQ[n].CNT > 0$ .

This example shows how the PWM module can be configured to repeat a single sequence until stopped.

```
NRF_PWM0->PSEL.OUT[0] = (first_pin << PWM_PSEL_OUT_PIN_Pos) |
                        (PWM_PSEL_OUT_CONNECT_Connected <<
                          PWM_PSEL_OUT_CONNECT_Pos);

NRF_PWM0->ENABLE       = (PWM_ENABLE_ENABLE_Enabled << PWM_ENABLE_ENABLE_Pos);
NRF_PWM0->MODE         = (PWM_MODE_UPDOWN_Up << PWM_MODE_UPDOWN_Pos);
NRF_PWM0->PRESCALER    = (PWM_PRESCALER_PRESCALER_DIV_1 <<
                          PWM_PRESCALER_PRESCALER_Pos);

NRF_PWM0->COUNTERTOP   = (16000 << PWM_COUNTERTOP_COUNTERTOP_Pos); //1 msec
// Enable the shortcut from LOOPSDONE event to SEQSTART1 task for infinite loop
NRF_PWM0->SHORTS       = (PWM_SHORTS_LOOPSDONE_SEQSTART1_Enabled <<
                          PWM_SHORTS_LOOPSDONE_SEQSTART1_Pos);

// LOOP_CNT must be greater than 0 for the LOOPSDONE event to trigger and enable looping
NRF_PWM0->LOOP         = (1 << PWM_LOOP_CNT_Pos);
NRF_PWM0->DECODER      = (PWM_DECODER_LOAD_Common << PWM_DECODER_LOAD_Pos) |
                        (PWM_DECODER_MODE_RefreshCount << PWM_DECODER_MODE_Pos);

// To repeat a single sequence until stopped, it must be configured in SEQ[1]
NRF_PWM0->SEQ[1].PTR   = ((uint32_t)(seq0_ram) << PWM_SEQ_PTR_PTR_Pos);
NRF_PWM0->SEQ[1].CNT   = ((sizeof(seq0_ram) / sizeof(uint16_t)) <<
                          PWM_SEQ_CNT_CNT_Pos);

NRF_PWM0->SEQ[1].REFRESH = 0;
NRF_PWM0->SEQ[1].ENDDELAY = 0;
NRF_PWM0->TASKS_SEQSTART[1] = 1;
```

### 7.1.24.3 Limitations

Previous compare value is repeated if the PWM period is shorter than the time it takes for the EasyDMA to retrieve from RAM and update the internal compare registers. This is to ensure a glitch-free operation even for very short PWM periods.

Only SEQ[1] can trigger the **LOOPSDONE** event upon completion, not SEQ[0]. This requires looping to be enabled (**LOOP** > 0) and **SEQ[1].CNT** > 0 when sequence playback starts.

### 7.1.24.4 Pin configuration

The OUT[n] (n=0..3) signals associated with each PWM channel are mapped to physical pins according to the configuration of PSEL.OUT[n] registers. If PSEL.OUT[n].CONNECT is set to Disconnected, the associated PWM module signal will not be connected to any physical pins.

The PSEL.OUT[n] registers and their configurations are used as long as the PWM module is enabled and the PWM generation active (wave counter started). They are retained only as long as the device is in System ON mode (see section **POWER** for more information about power modes).

To ensure correct behavior in the PWM module, the pins that are used must be configured in the GPIO peripheral in the following way before the PWM module is enabled:

| PWM signal | PWM pin                                 | Direction | Output value | Comment                                 |
|------------|-----------------------------------------|-----------|--------------|-----------------------------------------|
| OUT[n]     | As specified in PSEL.OUT[n]<br>(n=0..3) | Output    | 0            | Idle state defined in GPIO OUT register |

Table 111: Recommended GPIO configuration before starting PWM generation

The idle state of a pin is defined by the OUT register in the GPIO module, to ensure that the pins used by the PWM module are driven correctly. If PWM generation is stopped by triggering a STOP task, the PWM module itself is temporarily disabled or the device temporarily enters System OFF. This configuration must be retained in the GPIO for the selected pins (I/Os) for as long as the PWM module is supposed to be connected to an external PWM circuit.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

### 7.1.24.5 Registers

| Base address | Domain      | Peripheral | Instance  | Secure mapping | DMA security | Description                   | Configuration |
|--------------|-------------|------------|-----------|----------------|--------------|-------------------------------|---------------|
| 0x50021000   | APPLICATION | PWM        | PWM0 : S  | US             | SA           | Pulse width modulation unit 0 |               |
| 0x40021000   |             |            | PWM0 : NS |                |              |                               |               |
| 0x50022000   | APPLICATION | PWM        | PWM1 : S  | US             | SA           | Pulse width modulation unit 1 |               |
| 0x40022000   |             |            | PWM1 : NS |                |              |                               |               |
| 0x50023000   | APPLICATION | PWM        | PWM2 : S  | US             | SA           | Pulse width modulation unit 2 |               |
| 0x40023000   |             |            | PWM2 : NS |                |              |                               |               |

Table 112: Instances

| Register          | Offset | Security | Description                                                                                                                                                                                                   |
|-------------------|--------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TASKS_STOP        | 0x004  |          | Stops PWM pulse generation on all channels at the end of current PWM period, and stops sequence playback                                                                                                      |
| TASKS_SEQSTART[n] | 0x008  |          | Loads the first PWM value on all enabled channels from sequence n, and starts playing that sequence at the rate defined in SEQ[n].REFRESH and/or DECODER.MODE. Causes PWM generation to start if not running. |

| Register              | Offset | Security | Description                                                                                                                                         |
|-----------------------|--------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| TASKS_NEXTSTEP        | 0x010  |          | Steps by one value in the current sequence on all enabled channels if DECODER.MODE=NextStep. Does not cause PWM generation to start if not running. |
| SUBSCRIBE_STOP        | 0x084  |          | Subscribe configuration for task STOP                                                                                                               |
| SUBSCRIBE_SEQSTART[n] | 0x088  |          | Subscribe configuration for task SEQSTART[n]                                                                                                        |
| SUBSCRIBE_NEXTSTEP    | 0x090  |          | Subscribe configuration for task NEXTSTEP                                                                                                           |
| EVENTS_STOPPED        | 0x104  |          | Response to STOP task, emitted when PWM pulses are no longer generated                                                                              |
| EVENTS_SEQSTARTED[n]  | 0x108  |          | First PWM period started on sequence n                                                                                                              |
| EVENTS_SEQEND[n]      | 0x110  |          | Emitted at end of every sequence n, when last value from RAM has been applied to wave counter                                                       |
| EVENTS_PWMPERIODEND   | 0x118  |          | Emitted at the end of each PWM period                                                                                                               |
| EVENTS_LOOPSDONE      | 0x11C  |          | Concatenated sequences have been played the amount of times defined in LOOP.CNT                                                                     |
| PUBLISH_STOPPED       | 0x184  |          | Publish configuration for event STOPPED                                                                                                             |
| PUBLISH_SEQSTARTED[n] | 0x188  |          | Publish configuration for event SEQSTARTED[n]                                                                                                       |
| PUBLISH_SEQEND[n]     | 0x190  |          | Publish configuration for event SEQEND[n]                                                                                                           |
| PUBLISH_PWMPERIODEND  | 0x198  |          | Publish configuration for event PWMPERIODEND                                                                                                        |
| PUBLISH_LOOPSDONE     | 0x19C  |          | Publish configuration for event LOOPSDONE                                                                                                           |
| SHORTS                | 0x200  |          | Shortcuts between local events and tasks                                                                                                            |
| INTEN                 | 0x300  |          | Enable or disable interrupt                                                                                                                         |
| INTENSET              | 0x304  |          | Enable interrupt                                                                                                                                    |
| INTENCLR              | 0x308  |          | Disable interrupt                                                                                                                                   |
| ENABLE                | 0x500  |          | PWM module enable register                                                                                                                          |
| MODE                  | 0x504  |          | Selects operating mode of the wave counter                                                                                                          |
| COUNTERTOP            | 0x508  |          | Value up to which the pulse generator counter counts                                                                                                |
| PRESCALER             | 0x50C  |          | Configuration for PWM_CLK                                                                                                                           |
| DECODER               | 0x510  |          | Configuration of the decoder                                                                                                                        |
| LOOP                  | 0x514  |          | Number of playbacks of a loop                                                                                                                       |
| SEQ[n].PTR            | 0x520  |          | Beginning address in RAM of this sequence                                                                                                           |
| SEQ[n].CNT            | 0x524  |          | Number of values (duty cycles) in this sequence                                                                                                     |
| SEQ[n].REFRESH        | 0x528  |          | Number of additional PWM periods between samples loaded into compare register                                                                       |
| SEQ[n].ENDEDELAY      | 0x52C  |          | Time added after the sequence                                                                                                                       |
| PSEL.OUT[n]           | 0x560  |          | Output pin select for PWM channel n                                                                                                                 |

Table 113: Register overview

### 7.1.24.5.1 TASKS\_STOP

Address offset: 0x004

Stops PWM pulse generation on all channels at the end of current PWM period, and stops sequence playback

|                  |            |            |       |                                                                                                          |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |
|------------------|------------|------------|-------|----------------------------------------------------------------------------------------------------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|--|--|
| Bit number       |            |            | 31    | 30                                                                                                       | 29           | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |  |
| ID               |            |            | A     |                                                                                                          |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |
| Reset 0x00000000 |            |            | 0     | 0                                                                                                        | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |  |  |
| ID               | Acce Field | Value ID   | Value |                                                                                                          | Description  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |
| A                | W          | TASKS_STOP |       | Stops PWM pulse generation on all channels at the end of current PWM period, and stops sequence playback |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |
|                  |            | Trigger    | 1     |                                                                                                          | Trigger task |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |

### 7.1.24.5.2 TASKS\_SEQSTART[n] (n=0..1)

Address offset: 0x008 + (n × 0x4)

Loads the first PWM value on all enabled channels from sequence n, and starts playing that sequence at the rate defined in SEQ[n]REFRESH and/or DECODER.MODE. Causes PWM generation to start if not running.

|                  |      |                |         |                                                                                       |       |                                                                                                                                                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|----------------|---------|---------------------------------------------------------------------------------------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |                |         | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                                                                                                                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |                |         | A                                                                                     |       |                                                                                                                                                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |                |         | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |       |                                                                                                                                                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field          | Value   | ID                                                                                    | Value | Description                                                                                                                                                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W    | TASKS_SEQSTART |         |                                                                                       |       | Loads the first PWM value on all enabled channels from sequence n, and starts playing that sequence at the rate defined in SEQ[n]REFRESH and/or DECODER.MODE. Causes PWM generation to start if not running. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                | Trigger | 1                                                                                     |       | Trigger task                                                                                                                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.24.5.3 TASKS\_NEXTSTEP

Address offset: 0x010

Steps by one value in the current sequence on all enabled channels if DECODER.MODE=NextStep. Does not cause PWM generation to start if not running.

|                  |            |                |                                                                                       |  |              |                                                                                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------------|---------------------------------------------------------------------------------------|--|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |                | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |              |                                                                                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |                | A                                                                                     |  |              |                                                                                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |                | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |  |              |                                                                                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID       | Value                                                                                 |  | Description  |                                                                                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W          | TASKS_NEXTSTEP |                                                                                       |  |              | Steps by one value in the current sequence on all enabled channels if DECODER.MODE=NextStep. Does not cause PWM generation to start if not running. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Trigger        | 1                                                                                     |  | Trigger task |                                                                                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.24.5.4 SUBSCRIBE\_STOP

Address offset: 0x084

Subscribe configuration for task STOP

|                  |            |  |  |          |  |  |          |  |  |                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|--|----------|--|--|----------|--|--|-------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |  |          |  |  |          |  |  | 31                                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |  |  |          |  |  |          |  |  | B                                               |    |    |    |    |    |    |    |    |    | A  |    |    |    |    |    |    |    |    |    | A  | A  | A | A | A | A | A | A | A |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |  |          |  |  |          |  |  | 0                                               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  |  | Value ID |  |  | Value    |  |  | Description                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |  |          |  |  | [255..0] |  |  | Channel that task <b>STOP</b> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |  |          |  |  |          |  |  |                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  |  | Disabled |  |  | 0        |  |  | Disable subscription                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  |  | Enabled  |  |  | 1        |  |  | Enable subscription                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.24.5.5 SUBSCRIBE\_SEQSTART[n] (n=0..1)

Address offset: 0x088 + (n × 0x4)

Subscribe configuration for task SEQSTART[n]

|                  |            |          |          |                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|-----------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                                                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |          |          | B                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |          | 0                                                               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |
| ID               | Acce Field | Value ID | Value    | Description                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] | Channel that task <a href="#">SEQSTART[n]</a> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        | Disable subscription                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        | Enable subscription                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.24.5.6 SUBSCRIBE\_NEXTSTEP

Address offset: 0x090

Subscribe configuration for task [NEXTSTEP](#)

|                  |            |  |          |  |          |  |                                                     |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|--|----------|--|-----------------------------------------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          |  |          |  |                                                     |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |
| ID               |            |  |          |  |          |  |                                                     |  |  | B  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  | A  | A | A | A | A | A | A | A | A |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |          |  |          |  |                                                     |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID |  | Value    |  | Description                                         |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          |  | [255..0] |  | Channel that task <b>NEXTSTEP</b> will subscribe to |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |  |          |  |                                                     |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled |  | 0        |  | Disable subscription                                |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  |  | 1        |  | Enable subscription                                 |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.24.5.7 EVENTS\_STOPPED

Address offset: 0x104

Response to STOP task, emitted when PWM pulses are no longer generated

|                  |            |                |       |                                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------------|-------|------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                |       | 31                                                                     | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |                |       | A                                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |                |       | 0                                                                      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID       | Value | Description                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | EVENTS_STOPPED |       | Response to STOP task, emitted when PWM pulses are no longer generated |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | NotGenerated   | 0     | Event not generated                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Generated      | 1     | Event generated                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.24.5.8 EVENTS\_SEQSTARTED[n] (n=0..1)

Address offset: 0x108 + (n × 0x4)

First PWM period started on sequence n

|                  |            |                   |       |                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|------------------|------------|-------------------|-------|----------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|
| Bit number       |            |                   |       | 31                                     | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |
| ID               |            |                   |       | A                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
| Reset 0x00000000 |            |                   |       | 0                                      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |
| ID               | Acce Field | Value ID          | Value | Description                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
| A                | RW         | EVENTS_SEQSTARTED |       | First PWM period started on sequence n |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            | NotGenerated      | 0     | Event not generated                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            | Generated         | 1     | Event generated                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |

### 7.1.24.5.9 EVENTS\_SEQEND[n] (n=0..1)

Address offset: 0x110 + (n × 0x4)

Emitted at end of every sequence n, when last value from RAM has been applied to wave counter

| Bit number       |              | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                                               |
|------------------|--------------|---------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------|
| ID               |              | A                                                                                     |                                                                                               |
| Reset 0x00000000 |              | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                                               |
| ID               | Access Field | Value ID                                                                              | Description                                                                                   |
| A                | RW           | EVENTS_SEQEND                                                                         | Emitted at end of every sequence n, when last value from RAM has been applied to wave counter |
|                  |              | NotGenerated                                                                          | 0<br>Event not generated                                                                      |
|                  |              | Generated                                                                             | 1<br>Event generated                                                                          |

### 7.1.24.5.10 EVENTS\_PWMPERIODEND

Address offset: 0x118

Emitted at the end of each PWM period

| Bit number       |              | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                       |
|------------------|--------------|---------------------------------------------------------------------------------------|---------------------------------------|
| ID               |              | A                                                                                     |                                       |
| Reset 0x00000000 |              | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                       |
| ID               | Access Field | Value ID                                                                              | Description                           |
| A                | RW           | EVENTS_PWMPERIODEND                                                                   | Emitted at the end of each PWM period |
|                  |              | NotGenerated                                                                          | 0<br>Event not generated              |
|                  |              | Generated                                                                             | 1<br>Event generated                  |

### 7.1.24.5.11 EVENTS\_LOOPSDONE

Address offset: 0x11C

Concatenated sequences have been played the amount of times defined in LOOP.CNT

This event triggers after the last SEQ[1] completion of the loop, and only if looping was enabled (LOOP > 0) when the sequence playback was started.

| Bit number       |              | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                                                                                                      |
|------------------|--------------|---------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| ID               |              | A                                                                                     |                                                                                                                                                      |
| Reset 0x00000000 |              | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                                                                                                      |
| ID               | Access Field | Value ID                                                                              | Description                                                                                                                                          |
| A                | RW           | EVENTS_LOOPSDONE                                                                      | Concatenated sequences have been played the amount of times defined in LOOP.CNT                                                                      |
|                  |              |                                                                                       | This event triggers after the last SEQ[1] completion of the loop, and only if looping was enabled (LOOP > 0) when the sequence playback was started. |
|                  |              | NotGenerated                                                                          | 0<br>Event not generated                                                                                                                             |
|                  |              | Generated                                                                             | 1<br>Event generated                                                                                                                                 |

### 7.1.24.5.12 PUBLISH\_STOPPED

Address offset: 0x184

Publish configuration for event STOPPED

|                  |            |  |          |          |                    |                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|----------|--------------------|---------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31       | 30                 | 29                                          | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |  |          | B        |                    |                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   |   |   |   |   |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |          | 0        |                    |                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID | Value    |                    | Description                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          | [255..0] |                    | Channel that event STOPPED will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |          |                    |                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled | 0        | Disable publishing |                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  | 1        | Enable publishing  |                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.24.5.13 PUBLISH\_SEQSTARTED[n] (n=0..1)

Address offset: 0x188 + (n × 0x4)

Publish configuration for event **SEQSTARTED[n]**

|                  |            |  |          |  |          |  |                                                                   |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|--|----------|--|-------------------------------------------------------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          |  |          |  |                                                                   |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |  |          |  |          |  |                                                                   |  |  | B  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  | A  | A | A | A | A | A | A |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |          |  |          |  |                                                                   |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID |  | Value    |  | Description                                                       |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          |  | [255..0] |  | Channel that event <a href="#">SEQSTARTED[n]</a> will publish to. |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |  |          |  |                                                                   |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled |  | 0        |  | Disable publishing                                                |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  |  | 1        |  | Enable publishing                                                 |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.24.5.14 PUBLISH\_SEQEND[n] (n=0..1)

Address offset: 0x190 + (n × 0x4)

Publish configuration for event **SEQEND[n]**

|                  |            |  |          |          |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|----------|----|------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31       | 30 | 29                                                   | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |  |          | B        |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   |   |   |   |   |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |          | 0        |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID | Value    |    | Description                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          | [255..0] |    | Channel that event <b>SEQEND[n]</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |          |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled | 0        |    | Disable publishing                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  | 1        |    | Enable publishing                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.24.5.15 PUBLISH\_PWMPERIODEND

Address offset: 0x198

Publish configuration for event **PWMPERIODEND**

|                  |            |  |          |  |          |  |                                                         |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|--|----------|--|---------------------------------------------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          |  |          |  |                                                         |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |
| ID               |            |  |          |  |          |  |                                                         |  |  | B  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  | A  | A | A | A | A | A | A | A | A |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |          |  |          |  |                                                         |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID |  | Value    |  | Description                                             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          |  | [255..0] |  | Channel that event <b>PWMPERIODEND</b> will publish to. |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |  |          |  |                                                         |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled |  | 0        |  | Disable publishing                                      |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  |  | 1        |  | Enable publishing                                       |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.24.5.16 PUBLISH\_LOOPSDONE

Address offset: 0x19C

Publish configuration for event [LOOPSDONE](#)

This event triggers after the last SEQ[1] completion of the loop, and only if looping was enabled (LOOP > 0) when the sequence playback was started.

| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| ID               |            |          | B                                                                                     |                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                              | Channel that event <b>LOOPSDONE</b> will publish to. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |                                                                                       |                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Disable publishing                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Enable publishing                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

### 7.1.24.5.17 SHORTS

Address offset: 0x200

Shortcuts between local events and tasks

|                  |                        |          |                                                                                       |                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------------------|----------|---------------------------------------------------------------------------------------|-------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |                        |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |                        |          | E D C B A                                                                             |                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |                        |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field             | Value ID | Value                                                                                 | Description                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW SEQEND0_STOP        |          |                                                                                       | Shortcut between event SEQEND[0] and task STOP        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                        | Disabled | 0                                                                                     | Disable shortcut                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                        | Enabled  | 1                                                                                     | Enable shortcut                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW SEQEND1_STOP        |          |                                                                                       | Shortcut between event SEQEND[1] and task STOP        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                        | Disabled | 0                                                                                     | Disable shortcut                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                        | Enabled  | 1                                                                                     | Enable shortcut                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW LOOPSDONE_SEQSTART0 |          |                                                                                       | Shortcut between event LOOPSDONE and task SEQSTART[0] |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                        | Disabled | 0                                                                                     | Disable shortcut                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                        | Enabled  | 1                                                                                     | Enable shortcut                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| D                | RW LOOPSDONE_SEQSTART1 |          |                                                                                       | Shortcut between event LOOPSDONE and task SEQSTART[1] |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                        | Disabled | 0                                                                                     | Disable shortcut                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                        | Enabled  | 1                                                                                     | Enable shortcut                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| E                | RW LOOPSDONE_STOP      |          |                                                                                       | Shortcut between event LOOPSDONE and task STOP        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                        | Disabled | 0                                                                                     | Disable shortcut                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                        | Enabled  | 1                                                                                     | Enable shortcut                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.24.5.18 INTEN

Address offset: 0x300

Enable or disable interrupt

|                  |            |          |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |
|------------------|------------|----------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---------------|--|--|--|--|--|--|--|
| Bit number       |            |          |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |
| ID               |            |          |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | H G F E D C B |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |
| B                | RW STOPPED |          |       | Enable or disable interrupt for event <a href="#">STOPPED</a>                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |



| Bit number       |      |                        | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                                                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|------------------------|---------------------------------------------------------------------------------------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |      |                        | H G F E D C B                                                                         |       |                                                                                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |                        | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0             |       |                                                                                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field                  | Value ID                                                                              | Value | Description                                                                                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                        | Disabled                                                                              | 0     | Disable                                                                                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                        | Enabled                                                                               | 1     | Enable                                                                                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C-D              | RW   | SEQSTARTED[i] (i=0..1) |                                                                                       |       | Enable or disable interrupt for event <a href="#">SEQSTARTED[i]</a>                                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                        | Disabled                                                                              | 0     | Disable                                                                                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                        | Enabled                                                                               | 1     | Enable                                                                                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| E-F              | RW   | SEQEND[i] (i=0..1)     |                                                                                       |       | Enable or disable interrupt for event <a href="#">SEQEND[i]</a>                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                        | Disabled                                                                              | 0     | Disable                                                                                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                        | Enabled                                                                               | 1     | Enable                                                                                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| G                | RW   | PWMPERIODEND           |                                                                                       |       | Enable or disable interrupt for event <a href="#">PWMPERIODEND</a>                                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                        | Disabled                                                                              | 0     | Disable                                                                                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                        | Enabled                                                                               | 1     | Enable                                                                                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| H                | RW   | LOOPSDONE              |                                                                                       |       | Enable or disable interrupt for event <a href="#">LOOPSDONE</a>                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                        |                                                                                       |       | This event triggers after the last SEQ[1] completion of the loop, and only if looping was enabled (LOOP > 0) when the sequence playback was started. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                        | Disabled                                                                              | 0     | Disable                                                                                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                        | Enabled                                                                               | 1     | Enable                                                                                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.24.5.19 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number       |      |                        | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                                                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|------------------------|---------------------------------------------------------------------------------------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |      |                        | H G F E D C B                                                                         |       |                                                                                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |                        | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                   |       |                                                                                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field                  | Value ID                                                                              | Value | Description                                                                                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW   | STOPPED                |                                                                                       |       | Write '1' to enable interrupt for event <a href="#">STOPPED</a>                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                        | Set                                                                                   | 1     | Enable                                                                                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                        | Disabled                                                                              | 0     | Read: Disabled                                                                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                        | Enabled                                                                               | 1     | Read: Enabled                                                                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C-D              | RW   | SEQSTARTED[i] (i=0..1) |                                                                                       |       | Write '1' to enable interrupt for event <a href="#">SEQSTARTED[i]</a>                                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                        | Set                                                                                   | 1     | Enable                                                                                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                        | Disabled                                                                              | 0     | Read: Disabled                                                                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                        | Enabled                                                                               | 1     | Read: Enabled                                                                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| E-F              | RW   | SEQEND[i] (i=0..1)     |                                                                                       |       | Write '1' to enable interrupt for event <a href="#">SEQEND[i]</a>                                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                        | Set                                                                                   | 1     | Enable                                                                                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                        | Disabled                                                                              | 0     | Read: Disabled                                                                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                        | Enabled                                                                               | 1     | Read: Enabled                                                                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| G                | RW   | PWMPERIODEND           |                                                                                       |       | Write '1' to enable interrupt for event <a href="#">PWMPERIODEND</a>                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                        | Set                                                                                   | 1     | Enable                                                                                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                        | Disabled                                                                              | 0     | Read: Disabled                                                                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                        | Enabled                                                                               | 1     | Read: Enabled                                                                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| H                | RW   | LOOPSDONE              |                                                                                       |       | Write '1' to enable interrupt for event <a href="#">LOOPSDONE</a>                                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                        |                                                                                       |       | This event triggers after the last SEQ[1] completion of the loop, and only if looping was enabled (LOOP > 0) when the sequence playback was started. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                        | Set                                                                                   | 1     | Enable                                                                                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                        | Disabled                                                                              | 0     | Read: Disabled                                                                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

|                  |            |  |          |                                                                             |    |    |    |               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|-----------------------------------------------------------------------------|----|----|----|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31                                                                          | 30 | 29 | 28 | 27            | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |  |          |                                                                             |    |    |    |               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | H |   |   |   |   | G | F | E | D | C | B |
| Reset 0x00000000 |            |  |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |    |    |    |               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field |  | Value ID | Value                                                                       |    |    |    | Description   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  | 1                                                                           |    |    |    | Read: Enabled |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.24.5.20 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number       |  |  | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  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| ID               |  |  | H G F E D C B                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 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| Reset 0x00000000 |  |  | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 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0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.24.5.21 ENABLE

Address offset: 0x500

PWM module enable register

|                  |            |        |          |       |    |                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|------------------|------------|--------|----------|-------|----|------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|
| Bit number       |            |        |          | 31    | 30 | 29                           | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |
| ID               |            |        |          |       |    |                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |  |  |
| Reset 0x00000000 |            |        |          | 0     | 0  | 0                            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |
| ID               | Acce Field |        | Value ID | Value |    | Description                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
| A                | RW         | ENABLE |          |       |    | Enable or disable PWM module |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            |        | Disabled | 0     |    | Disabled                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            |        | Enabled  | 1     |    | Enable                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |

### 7.1.24.5.22 MODE

Address offset: 0x504

Selects operating mode of the wave counter

|                  |            |        |           |       |    |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|------------------|------------|--------|-----------|-------|----|-----------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|
| Bit number       |            |        |           | 31    | 30 | 29                                                  | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |
| ID               |            |        |           |       |    |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |  |  |
| Reset 0x00000000 |            |        |           | 0     | 0  | 0                                                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |  |  |
| ID               | Acce Field |        | Value ID  | Value |    | Description                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
| A                | RW         | UPDOWN |           |       |    | Selects up mode or up-and-down mode for the counter |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            |        | Up        | 0     |    | Up counter, edge-aligned PWM duty cycle             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            |        | UpAndDown | 1     |    | Up and down counter, center-aligned PWM duty cycle  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |

### 7.1.24.5.23 COUNTERTOP

Address offset: 0x508

Value up to which the pulse generator counter counts

|                  |               |          |            |    |                                                                                                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|---------------|----------|------------|----|----------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |               |          | 31         | 30 | 29                                                                                                                                           | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |               |          |            |    |                                                                                                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A | A | A |
| Reset 0x000003FF |               |          | 0          | 0  | 0                                                                                                                                            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |   |   |
| ID               | Acce Field    | Value ID | Value      |    | Description                                                                                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW COUNTERTOP |          | [3..32767] |    | Value up to which the pulse generator counter counts. This register is ignored when DECODER.MODE=WaveForm and only values from RAM are used. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.24.5.24 PRESCALER

Address offset: 0x50C

Configuration for PWM\_CLK

|                  |      |           |         |                                                                                       |       |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|-----------|---------|---------------------------------------------------------------------------------------|-------|-------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |           |         | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |           |         | A A A                                                                                 |       |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |           |         | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |       |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field     | Value   | ID                                                                                    | Value | Description             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW   | PRESCALER |         |                                                                                       |       | Prescaler of PWM_CLK    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | DIV_1   | 0                                                                                     |       | Divide by 1 (16 MHz)    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | DIV_2   | 1                                                                                     |       | Divide by 2 (8 MHz)     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | DIV_4   | 2                                                                                     |       | Divide by 4 (4 MHz)     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | DIV_8   | 3                                                                                     |       | Divide by 8 (2 MHz)     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | DIV_16  | 4                                                                                     |       | Divide by 16 (1 MHz)    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | DIV_32  | 5                                                                                     |       | Divide by 32 (500 kHz)  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | DIV_64  | 6                                                                                     |       | Divide by 64 (250 kHz)  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | DIV_128 | 7                                                                                     |       | Divide by 128 (125 kHz) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.24.5.25 DECODER

Address offset: 0x510

Configuration of the decoder

| Bit number       |      |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |    |                                                                             |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|-------|---------------------------------------------------------------------------------------|----|-----------------------------------------------------------------------------|-------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |      |       | B A A                                                                                 |    |                                                                             |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |    |                                                                             |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field | Value                                                                                 | ID | Value                                                                       | Description |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW   | LOAD  |                                                                                       |    | How a sequence is read from RAM and spread to the compare register          |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Common                                                                                | 0  | 1st half word (16-bit) used in all PWM channels 0..3                        |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Grouped                                                                               | 1  | 1st half word (16-bit) used in channel 0..1; 2nd word in channel 2..3       |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Individual                                                                            | 2  | 1st half word (16-bit) in ch.0; 2nd in ch.1; ...; 4th in ch.3               |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | WaveForm                                                                              | 3  | 1st half word (16-bit) in ch.0; 2nd in ch.1; ...; 4th in COUNTERTOP         |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW   | MODE  |                                                                                       |    | Selects source for advancing the active sequence                            |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | RefreshCount                                                                          | 0  | SEQ[n].REFRESH is used to determine loading internal compare registers      |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | NextStep                                                                              | 1  | NEXTSTEP task causes a new value to be loaded to internal compare registers |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.24.5.26 LOOP

Address offset: 0x514

Number of playbacks of a loop

|                  |            |          |          |                                                                                       |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|----------|---------------------------------------------------------------------------------------|----------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          |          | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A                           |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value    | Description                                                                           |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | CNT      |          | Number of playbacks of pattern cycles                                                 |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |          | Disabled | 0                                                                                     | Looping disabled (stop at the end of the sequence) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.24.5.27 SEQ[n].PTR (n=0..1)

Address offset: 0x520 + (n × 0x20)

Beginning address in RAM of this sequence

|                  |            |  |  |                                                                                       |  |  |       |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                           |  |  |  |  |  |
|------------------|------------|--|--|---------------------------------------------------------------------------------------|--|--|-------|--|--|--|-------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------------------------------------|--|--|--|--|--|
| Bit number       |            |  |  | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |       |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                           |  |  |  |  |  |
| ID               |            |  |  | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A                           |  |  |       |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                           |  |  |  |  |  |
| Reset 0x00000000 |            |  |  | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |  |  |       |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                           |  |  |  |  |  |
| ID               | Acce Field |  |  | Value ID                                                                              |  |  | Value |  |  |  | Description |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                           |  |  |  |  |  |
| A                | RW PTR     |  |  |                                                                                       |  |  |       |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Beginning address in RAM of this sequence |  |  |  |  |  |

**Note:** See the memory chapter for details about which memories are available for EasyDMA.

### 7.1.24.5.28 SEQ[n].CNT (n=0..1)

Address offset: 0x524 + (n × 0x20)

Number of values (duty cycles) in this sequence

|                  |            |          |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |
|------------------|------------|----------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|---|--|--|--|---|--|--|--|---|--|--|--|---|--|--|--|---|--|--|--|---|--|--|--|
| Bit number       |            |          |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |
| ID               |            |          |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A |  |  |  | A |  |  |  | A |  |  |  | A |  |  |  | A |  |  |  | A |  |  |  | A |  |  |  |
| Reset 0x00000000 |            |          |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |
| ID               | Acce Field | Value ID | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |
| A                | RW CNT     |          |       | Number of values (duty cycles) in this sequence                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |
|                  |            | Disabled | 0     | Sequence is disabled, and shall not be started as it is empty                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |

#### 7.1.24.5.29 SEQ[n].REFRESH (n=0..1)

Address offset: 0x528 + (n × 0x20)

Number of additional PWM periods between samples loaded into compare register

| Bit number       |            |            |       | 31                                                                                                                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
|------------------|------------|------------|-------|----------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| ID               |            |            |       |                                                                                                                      |    |    |    |    |    |    |    |    |    |    |    | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |   |
| Reset 0x00000001 |            |            |       | 0                                                                                                                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| ID               | Acce Field | Value ID   | Value | Description                                                                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | CNT        |       | Number of additional PWM periods between samples loaded into compare register (load every REFRESH.CNT+1 PWM periods) |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Continuous | 0     | Update every PWM period                                                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.24.5.30 SEQ[n].ENDDELAY (n=0..1)

Address offset: 0x52C + (n × 0x20)

Time added after the sequence

|                  |  |  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               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| Bit number       |  |  | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         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|
| ID               |  |  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               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|
| Reset 0x00000000 |  |  | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 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  |   |   |

#### 7.1.24.5.31 PSEL.OUT[n] (n=0..3)

Address offset: 0x560 + (n × 0x4)

Output pin select for PWM channel n

|                  |            |              |                                                                                       |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|--------------|---------------------------------------------------------------------------------------|-------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |              | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |              | C B A A A A A A                                                                       |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0xFFFFFFFF |            |              | 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1     |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID     | Value                                                                                 | Description |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW PIN     |              | [0..31]                                                                               | Pin number  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW PORT    |              | [0..1]                                                                                | Port number |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW CONNECT |              |                                                                                       | Connection  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disconnected | 1                                                                                     | Disconnect  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Connected    | 0                                                                                     | Connect     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.25 QDEC — Quadrature decoder

The Quadrature decoder (QDEC) provides buffered decoding of quadrature-encoded sensor signals. It is suitable for mechanical and optical sensors.

The sample period and accumulation are configurable to match application requirements. The QDEC provides the following:

- Decoding of digital waveform from off-chip quadrature encoder.
- Sample accumulation eliminating hard real-time requirements to be enforced on application.
- Optional input de-bounce filters.
- Optional LED output signal for optical encoders.

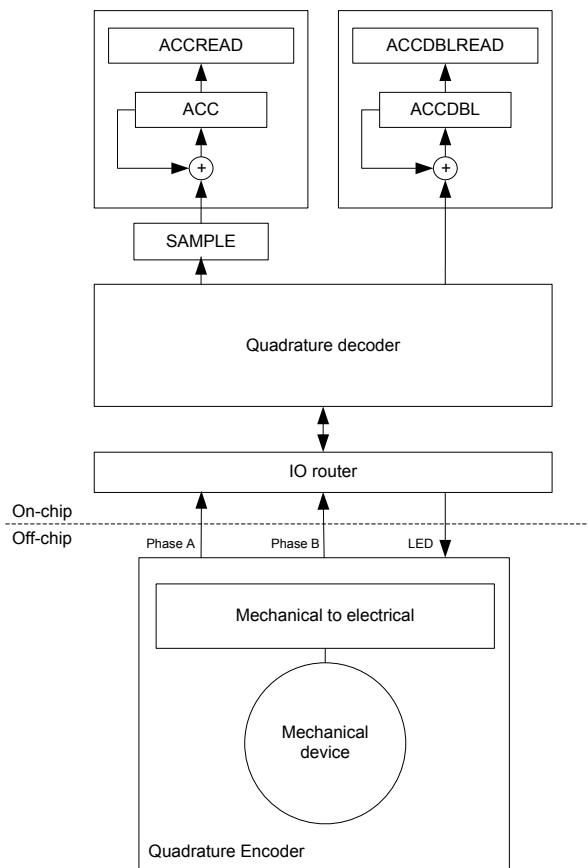


Figure 112: Quadrature decoder configuration

### 7.1.25.1 Sampling and decoding

The QDEC decodes the output from an incremental motion encoder by sampling the QDEC phase input pins (A and B).

The off-chip quadrature encoder is an incremental motion encoder outputting two waveforms, phase A and phase B. The two output waveforms are always 90 degrees out of phase, meaning that one always changes level before the other. The direction of movement is indicated by which of these two waveforms that changes level first. Invalid transitions may occur, that is when the two waveforms switch simultaneously. This may occur if the wheel rotates too fast relative to the sample rate set for the decoder.

The QDEC decodes the output from the off-chip encoder by sampling the QDEC phase input pins (A and B) at a fixed rate as specified in the SAMPLEPER register.

If the SAMPLEPER value needs to be changed, the QDEC shall be stopped using the STOP task. SAMPLEPER can be then changed upon receiving the STOPPED event, and QDEC can be restarted using the START task. Failing to do so may result in unpredictable behaviour.

It is good practice to change other registers (LEDPOL, REPORTPER, DBFEN and LEDPRE) only when the QDEC is stopped.

When started, the decoder continuously samples the two input waveforms and decodes these by comparing the current sample pair (n) with the previous sample pair (n-1).

The decoding of the sample pairs is described in the table below.

| Previous sample pair(n-1) |   | Current samples pair(n) |   | SAMPLE register | ACC operation | ACCDBL operation | Description                    |
|---------------------------|---|-------------------------|---|-----------------|---------------|------------------|--------------------------------|
| A                         | B | A                       | B |                 |               |                  |                                |
| 0                         | 0 | 0                       | 0 | 0               | No change     | No change        | No movement                    |
| 0                         | 0 | 0                       | 1 | 1               | Increment     | No change        | Movement in positive direction |
| 0                         | 0 | 1                       | 0 | -1              | Decrement     | No change        | Movement in negative direction |
| 0                         | 0 | 1                       | 1 | 2               | No change     | Increment        | Error: Double transition       |
| 0                         | 1 | 0                       | 0 | -1              | Decrement     | No change        | Movement in negative direction |
| 0                         | 1 | 0                       | 1 | 0               | No change     | No change        | No movement                    |
| 0                         | 1 | 1                       | 0 | 2               | No change     | Increment        | Error: Double transition       |
| 0                         | 1 | 1                       | 1 | 1               | Increment     | No change        | Movement in positive direction |
| 1                         | 0 | 0                       | 0 | 1               | Increment     | No change        | Movement in positive direction |
| 1                         | 0 | 0                       | 1 | 2               | No change     | Increment        | Error: Double transition       |
| 1                         | 0 | 1                       | 0 | 0               | No change     | No change        | No movement                    |
| 1                         | 0 | 1                       | 1 | -1              | Decrement     | No change        | Movement in negative direction |
| 1                         | 1 | 0                       | 0 | 2               | No change     | Increment        | Error: Double transition       |
| 1                         | 1 | 0                       | 1 | -1              | Decrement     | No change        | Movement in negative direction |
| 1                         | 1 | 1                       | 0 | 1               | Increment     | No change        | Movement in positive direction |
| 1                         | 1 | 1                       | 1 | 0               | No change     | No change        | No movement                    |

Table 114: Sampled value encoding

### 7.1.25.2 LED output

The LED output follows the sample period, and the LED is switched on a given period before sampling and switched off immediately after the inputs are sampled. The period the LED is switched on before sampling is given in the LEDPRE register.

The LED output pin polarity is specified in the LEDPOL register.

For using off-chip mechanical encoders not requiring a LED, the LED output can be disabled by writing value 'Disconnected' to the CONNECT field of the PSEL.LED register. In this case the QDEC will not acquire access to a LED output pin and the pin can be used for other purposes by the CPU.

### 7.1.25.3 Debounce filters

Each of the two-phase inputs have digital debounce filters.

When enabled through the DBFEN register, the filter inputs are sampled at a fixed 1 MHz frequency during the entire sample period (which is specified in the SAMPLEPER register), and the filters require all of the samples within this sample period to equal before the input signal is accepted and transferred to the output of the filter.

As a result, only input signal with a steady state longer than twice the period specified in SAMPLEPER are guaranteed to pass through the filter, and any signal with a steady state shorter than SAMPLEPER will always be suppressed by the filter. (This is assumed that the frequency during the debounce period never exceeds 500 kHz (as required by the Nyquist theorem when using a 1 MHz sample frequency).

The LED will always be ON when the debounce filters are enabled, as the inputs in this case will be sampled continuously.

Note that when the debounce filters are enabled, displacements reported by the QDEC peripheral are delayed by one SAMPLEPER period.

### 7.1.25.4 Accumulators

The quadrature decoder contains two accumulator registers, ACC and ACCDBL, that accumulate respectively valid motion sample values and the number of detected invalid samples (double transitions).

The ACC register will accumulate all valid values (1/-1) written to the SAMPLE register. This can be useful for preventing hard real-time requirements from being enforced on the application. When using the ACC register the application does not need to read every single sample from the SAMPLE register, but can instead fetch the ACC register whenever it fits the application. The ACC register will always hold the relative movement of the external mechanical device since the previous clearing of the ACC register. Sample values indicating a double transition (2) will not be accumulated in the ACC register.

An ACCOF event will be generated if the ACC receives a SAMPLE value that would cause the register to overflow or underflow. Any SAMPLE value that would cause an ACC overflow or underflow will be discarded, but any samples not causing the ACC to overflow or underflow will still be accepted.

The accumulator ACCDBL accumulates the number of detected double transitions since the previous clearing of the ACCDBL register.

The ACC and ACCDBL registers can be cleared by the READCLRACC and subsequently read using the ACCREAD and ACCDBLREAD registers.

The ACC register can be separately cleared by the RDCLRACC and subsequently read using the ACCREAD registers.

The ACCDBL register can be separately cleared by the RDCLRDBL and subsequently read using the ACCDBLREAD registers.

The REPORTPER register allows automating the capture of several samples before it can send out a REPORTRDY event in case a non-null displacement has been captured and accumulated, and a DBLRDY event in case one or more double-displacements have been captured and accumulated. The REPORTPER field in this register selects after how many samples the accumulators contents are evaluated to send (or not) REPORTRDY and DBLRDY events.

Using the RDCLRACC task (manually sent upon receiving the event, or using the DBLRDY\_RDCLRACC shortcut), ACCREAD can then be read.

In case at least one double transition has been captured and accumulated, a DBLRDY event is sent. Using the RDCLRDBL task (manually sent upon receiving the event, or using the DBLRDY\_RDCLRDBL shortcut), ACCDBLREAD can then be read.

### 7.1.25.5 Output/input pins

The QDEC uses a three-pin interface to the off-chip quadrature encoder.

These pins will be acquired when the QDEC is enabled in the ENABLE register. The pins acquired by the QDEC cannot be written by the CPU, but they can still be read by the CPU.

The pin numbers to be used for the QDEC are selected using the PSEL.n registers.

### 7.1.25.6 Pin configuration

The Phase A, Phase B, and LED signals are mapped to physical pins according to the configuration specified in the PSEL.A, PSEL.B, and PSEL.LED registers respectively.

If the CONNECT field value 'Disconnected' is specified in any of these registers, the associated signal will not be connected to any physical pin. The PSEL.A, PSEL.B, and PSEL.LED registers and their configurations are only used as long as the QDEC is enabled, and retained only as long as the device is in ON mode.



When the peripheral is disabled, the pins will behave as regular GPIOs, and use the configuration in their respective OUT bit field and PIN\_CNF[n] register.

To secure correct behavior in the QDEC, the pins used by the QDEC must be configured in the GPIO peripheral as described in [Table 115: GPIO configuration before enabling peripheral](#) on page 365 before enabling the QDEC. This configuration must be retained in the GPIO for the selected IOs as long as the QDEC is enabled.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

| QDEC signal | QDEC pin                 | Direction | Output value   | Comment |
|-------------|--------------------------|-----------|----------------|---------|
| Phase A     | As specified in PSEL.A   | Input     | Not applicable |         |
| Phase B     | As specified in PSEL.B   | Input     | Not applicable |         |
| LED         | As specified in PSEL.LED | Input     | Not applicable |         |

Table 115: GPIO configuration before enabling peripheral

### 7.1.25.7 Registers

| Base address | Domain      | Peripheral | Instance  | Secure mapping | DMA security | Description        | Configuration |
|--------------|-------------|------------|-----------|----------------|--------------|--------------------|---------------|
| 0x50033000   | APPLICATION | QDEC       | QDEC : S  | US             | NA           | Quadrature decoder |               |
| 0x40033000   |             |            | QDEC : NS |                |              |                    |               |

Table 116: Instances

| Register             | Offset | Security | Description                                                                     |
|----------------------|--------|----------|---------------------------------------------------------------------------------|
| TASKS_START          | 0x000  |          | Task starting the quadrature decoder                                            |
| TASKS_STOP           | 0x004  |          | Task stopping the quadrature decoder                                            |
| TASKS_READCLRACC     | 0x008  |          | Read and clear ACC and ACCDBL                                                   |
| TASKS_RDCLRACC       | 0x00C  |          | Read and clear ACC                                                              |
| TASKS_RDCLRDBL       | 0x010  |          | Read and clear ACCDBL                                                           |
| SUBSCRIBE_START      | 0x080  |          | Subscribe configuration for task <a href="#">START</a>                          |
| SUBSCRIBE_STOP       | 0x084  |          | Subscribe configuration for task <a href="#">STOP</a>                           |
| SUBSCRIBE_READCLRACC | 0x088  |          | Subscribe configuration for task <a href="#">READCLRACC</a>                     |
| SUBSCRIBE_RDCLRACC   | 0x08C  |          | Subscribe configuration for task <a href="#">RDCLRACC</a>                       |
| SUBSCRIBE_RDCLRDBL   | 0x090  |          | Subscribe configuration for task <a href="#">RDCLRDBL</a>                       |
| EVENTS_SAMPLERDY     | 0x100  |          | Event being generated for every new sample value written to the SAMPLE register |
| EVENTS_REPORTRDY     | 0x104  |          | Non-null report ready                                                           |
| EVENTS_ACCOF         | 0x108  |          | ACC or ACCDBL register overflow                                                 |
| EVENTS_DBLRDY        | 0x10C  |          | Double displacement(s) detected                                                 |
| EVENTS_STOPPED       | 0x110  |          | QDEC has been stopped                                                           |
| PUBLISH_SAMPLERDY    | 0x180  |          | Publish configuration for event <a href="#">SAMPLERDY</a>                       |
| PUBLISH_REPORTRDY    | 0x184  |          | Publish configuration for event <a href="#">REPORTRDY</a>                       |
| PUBLISH_ACCOF        | 0x188  |          | Publish configuration for event <a href="#">ACCOF</a>                           |
| PUBLISH_DBLRDY       | 0x18C  |          | Publish configuration for event <a href="#">DBLRDY</a>                          |
| PUBLISH_STOPPED      | 0x190  |          | Publish configuration for event <a href="#">STOPPED</a>                         |
| SHORTS               | 0x200  |          | Shortcuts between local events and tasks                                        |
| INTENSET             | 0x304  |          | Enable interrupt                                                                |
| INTENCLR             | 0x308  |          | Disable interrupt                                                               |
| ENABLE               | 0x500  |          | Enable the quadrature decoder                                                   |
| LEDPOL               | 0x504  |          | LED output pin polarity                                                         |
| SAMPLEPER            | 0x508  |          | Sample period                                                                   |
| SAMPLE               | 0x50C  |          | Motion sample value                                                             |

| Register  | Offset | Security | Description                                                                       |
|-----------|--------|----------|-----------------------------------------------------------------------------------|
| REPORTPER | 0x510  |          | Number of samples to be taken before REPORTRDY and DBLRDY events can be generated |
| ACC       | 0x514  |          | Register accumulating the valid transitions                                       |
| ACCREAD   | 0x518  |          | Snapshot of the ACC register, updated by the READCLRACC or RDCLRACC task          |
| PSEL.LED  | 0x51C  |          | Pin select for LED signal                                                         |
| PSEL.A    | 0x520  |          | Pin select for A signal                                                           |
| PSEL.B    | 0x524  |          | Pin select for B signal                                                           |
| DBFEN     | 0x528  |          | Enable input debounce filters                                                     |
| LEDPRE    | 0x540  |          | Time period the LED is switched ON prior to sampling                              |
| ACCDL     | 0x544  |          | Register accumulating the number of detected double transitions                   |
| ACCDLREAD | 0x548  |          | Snapshot of the ACCDL, updated by the READCLRACC or RDCLRDL task                  |

Table 117: Register overview

### 7.1.25.7.1 TASKS\_START

Address offset: 0x000

Task starting the quadrature decoder

When started, the SAMPLE register will be continuously updated at the rate given in the SAMPLEPER register.

|                  |      |             |         |                                                                                       |       |                                                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|-------------|---------|---------------------------------------------------------------------------------------|-------|-------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |             |         | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |             |         | A                                                                                     |       |                                                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |             |         | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |       |                                                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field       | Value   | ID                                                                                    | Value | Description                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W    | TASKS_START |         |                                                                                       |       | Task starting the quadrature decoder                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |             |         |                                                                                       |       | When started, the SAMPLE register will be continuously updated at the rate given in the SAMPLEPER register. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |             | Trigger | 1                                                                                     |       | Trigger task                                                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.25.7.2 TASKS\_STOP

Address offset: 0x004

Task stopping the quadrature decoder

|                  |            |            |          |                                                                                       |  |                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|------------|----------|---------------------------------------------------------------------------------------|--|--------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |            |          | A                                                                                     |  |                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |  |                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field |            | Value ID | Value                                                                                 |  | Description                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W          | TASKS_STOP |          |                                                                                       |  | Task stopping the quadrature decoder |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Trigger    |          | 1                                                                                     |  | Trigger task                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.25.7.3 TASKS\_READCLRACC

Address offset: 0x008

Read and clear ACC and ACCDL

Task transferring the content of ACC to ACCREAD and the content of ACCDL to ACCDLREAD, and then clearing the ACC and ACCDL registers. These read-and-clear operations will be done atomically.

| Bit number       |      |                  | 31       | 30      | 29    | 28                                                                                                                                                                                                | 27          | 26                            | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------|------|------------------|----------|---------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|-------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| ID               |      |                  |          |         |       |                                                                                                                                                                                                   |             |                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | A |
| Reset 0x00000000 |      |                  | 0        | 0       | 0     | 0                                                                                                                                                                                                 | 0           | 0                             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce | Field            | Value ID |         | Value |                                                                                                                                                                                                   | Description |                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | W    | TASKS_READCLRACC |          |         |       |                                                                                                                                                                                                   |             | Read and clear ACC and ACCDBL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |                  |          |         |       | Task transferring the content of ACC to ACCREAD and the content of ACCDBL to ACCDBLREAD, and then clearing the ACC and ACCDBL registers. These read-and-clear operations will be done atomically. |             |                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |                  |          | Trigger | 1     | Trigger task                                                                                                                                                                                      |             |                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 7.1.25.7.4 TASKS\_RDCLRACC

Address offset: 0x00C

Read and clear ACC

Task transferring the content of ACC to ACCREAD, and then clearing the ACC register. This read-and-clear operation will be done atomically.

| Bit number       |      |                |          | 31      | 30 | 29                                                                                                                                          | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |  |
|------------------|------|----------------|----------|---------|----|---------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|--|
| ID               |      |                |          |         |    |                                                                                                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |  |  |  |
| Reset 0x00000000 |      |                |          | 0       | 0  | 0                                                                                                                                           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |
| ID               | Acce | Field          | Value ID | Value   |    | Description                                                                                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
| A                | W    | TASKS_RDCLRACC |          |         |    | Read and clear ACC                                                                                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |                |          |         |    | Task transferring the content of ACC to ACCREAD, and then clearing the ACC register. This read-and-clear operation will be done atomically. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |                |          | Trigger | 1  | Trigger task                                                                                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |

#### 7.1.25.7.5 TASKS\_RDCLRDBL

Address offset: 0x010

Read and clear ACCDBL

Task transferring the content of ACCDBL to ACCDBLREAD, and then clearing the ACCDBL register. This read-and-clear operation will be done atomically.

|                  |      |                |          |                                                                                       |                                                                                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|----------------|----------|---------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |                |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |                |          | A                                                                                     |                                                                                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |                |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field          | Value ID | Value                                                                                 | Description                                                                                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W    | TASKS_RDCLRDBL |          |                                                                                       | Read and clear ACCDBL                                                                                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                |          |                                                                                       | Task transferring the content of ACCDBL to ACCDBLREAD, and then clearing the ACCDBL register. This read-and-clear operation will be done atomically. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Trigger          |      |                |          | 1                                                                                     | Trigger task                                                                                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

#### 7.1.25.7.6 SUBSCRIBE\_START

Address offset: 0x080

Subscribe configuration for task [START](#)

When started, the SAMPLE register will be continuously updated at the rate given in the SAMPLEPER register.

|                  |            |          |          |                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|-----------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                                                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |          |          | B                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |          | 0                                                         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce Field | Value ID | Value    | Description                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] | Channel that task <a href="#">START</a> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        | Disable subscription                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        | Enable subscription                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.25.7.7 SUBSCRIBE\_STOP

Address offset: 0x084

Subscribe configuration for task **STOP**

|                  |            |  |          |                                                                             |    |    |    |                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |  |  |   |  |  |  |
|------------------|------------|--|----------|-----------------------------------------------------------------------------|----|----|----|-------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|--|---|--|--|--|---|--|--|--|
| Bit number       |            |  |          | 31                                                                          | 30 | 29 | 28 | 27                                                    | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |  |   |  |  |  |   |  |  |  |
| ID               |            |  |          | B                                                                           |    |    |    |                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A |   |   |   | A |  |  |  | A |  |  |  | A |  |  |  |
| Reset 0x00000000 |            |  |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |    |    |    |                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |  |  |   |  |  |  |
| ID               | Acce Field |  | Value ID | Value                                                                       |    |    |    | Description                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |  |  |   |  |  |  |
| A                | RW CHIDX   |  |          | [255..0]                                                                    |    |    |    | Channel that task <span>STOP</span> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |  |  |   |  |  |  |
| B                | RW EN      |  |          |                                                                             |    |    |    |                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |  |  |   |  |  |  |
|                  |            |  | Disabled | 0                                                                           |    |    |    | Disable subscription                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |  |  |   |  |  |  |
|                  |            |  | Enabled  | 1                                                                           |    |    |    | Enable subscription                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |  |  |   |  |  |  |

#### 7.1.25.7.8 SUBSCRIBE\_READCLRACC

Address offset: 0x088

Subscribe configuration for task **READCLRACC**

Task transferring the content of ACC to ACCREAD and the content of ACCDBL to ACCDBLREAD, and then clearing the ACC and ACCDBL registers. These read-and-clear operations will be done atomically.

|                  |            |  |          |          |    |    |    |                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |  |  |
|------------------|------------|--|----------|----------|----|----|----|-------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|--|---|--|--|--|
| Bit number       |            |  |          | 31       | 30 | 29 | 28 | 27                                                          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |  |   |  |  |  |
| ID               |            |  |          | B        |    |    |    |                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A |   |   |   | A |  |  |  | A |  |  |  |
| Reset 0x00000000 |            |  |          | 0        |    |    |    |                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |  |  |
| ID               | Acce Field |  | Value ID | Value    |    |    |    | Description                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |  |  |
| A                | RW CHIDX   |  |          | [255..0] |    |    |    | Channel that task <span>READCLRACC</span> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |  |  |
| B                | RW EN      |  |          |          |    |    |    |                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |  |  |
|                  |            |  | Disabled | 0        |    |    |    | Disable subscription                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |  |  |
|                  |            |  | Enabled  | 1        |    |    |    | Enable subscription                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |  |  |

#### 7.1.25.7.9 SUBSCRIBE\_RDCLRACC

Address offset: 0x08C

Subscribe configuration for task **RDCLRACC**

Task transferring the content of ACC to ACCREAD, and then clearing the ACC register. This read-and-clear operation will be done atomically.

|                  |            |          |          |    |    |    |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|----|----|----|-----------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|--|---|---|---|---|---|---|---|
| Bit number       |            |          | 31       | 30 | 29 | 28 | 27                                                  | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |  |   |   |   |   |   |   |   |
| ID               |            |          | B        |    |    |    |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   |   |   |   |   |  |  |  | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          | 0        | 0  | 0  | 0  | 0                                                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |   |   |   |   |   |   |   |
| ID               | Acce Field | Value ID | Value    |    |    |    | Description                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] |    |    |    | Channel that task <b>RDCLRACC</b> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |    |    |    |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        |    |    |    | Disable subscription                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        |    |    |    | Enable subscription                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |   |   |   |   |   |   |

#### 7.1.25.7.10 SUBSCRIBE\_RDCLRDBL

Address offset: 0x090

Subscribe configuration for task **RDCLRDBL**

Task transferring the content of ACCDBL to ACCDBLREAD, and then clearing the ACCDBL register. This read-and-clear operation will be done atomically.

|                  |            |  |          |  |          |  |                                                              |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|--|----------|--|--------------------------------------------------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          |  |          |  |                                                              |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |
| ID               |            |  |          |  |          |  |                                                              |  |  | B  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  |    |    |    |   |   |   |   |   |   | A | A | A | A | A | A | A |   |
| Reset 0x00000000 |            |  |          |  |          |  |                                                              |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID |  | Value    |  | Description                                                  |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          |  | [255..0] |  | Channel that task <a href="#">RDCLRDBL</a> will subscribe to |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |  |          |  |                                                              |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled |  | 0        |  | Disable subscription                                         |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  |  | 1        |  | Enable subscription                                          |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.25.7.11 EVENTS\_SAMPLERDY

Address offset: 0x100

Event being generated for every new sample value written to the SAMPLE register

|                  |            |                  |       |                                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|------------------|------------|------------------|-------|---------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|
| Bit number       |            |                  |       | 31                                                                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |
| ID               |            |                  |       | A                                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
| Reset 0x00000000 |            |                  |       | 0                                                                               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |
| ID               | Acce Field | Value ID         | Value | Description                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
| A                | RW         | EVENTS_SAMPLERDY |       | Event being generated for every new sample value written to the SAMPLE register |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            | NotGenerated     | 0     | Event not generated                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            | Generated        | 1     | Event generated                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |

#### 7.1.25.7.12 EVENTS\_REPORTRDY

Address offset: 0x104

Non-null report ready

Event generated when REPORTPER number of samples has been accumulated in the ACC register and the content of the ACC register is not equal to 0. (Thus, this event is only generated if a motion is detected since the previous clearing of the ACC register).

| Bit number       |            |                  |       | 31                                                                                                                                                                                                                                                             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |   |
|------------------|------------|------------------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|---|
| ID               |            |                  |       |                                                                                                                                                                                                                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | A |
| Reset 0x00000000 |            |                  |       | 0                                                                                                                                                                                                                                                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |   |
| ID               | Acce Field | Value ID         | Value | Description                                                                                                                                                                                                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
| A                | RW         | EVENTS_REPORTRDY |       | Non-null report ready                                                                                                                                                                                                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            |                  |       | Event generated when REPORTPER number of samples has been accumulated in the ACC register and the content of the ACC register is not equal to 0. (Thus, this event is only generated if a motion is detected since the previous clearing of the ACC register). |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | NotGenerated     | 0     | Event not generated                                                                                                                                                                                                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | Generated        | 1     | Event generated                                                                                                                                                                                                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |

### 7.1.25.7.13 EVENTS\_ACCOF

Address offset: 0x108

ACC or ACCDBL register overflow

|                  |            |              |       |                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------------|-------|---------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |              |       | 31                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |              |       |                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |
| Reset 0x00000000 |            |              |       | 0                               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID     | Value | Description                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | EVENTS_ACCOF |       | ACC or ACCDBL register overflow |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | NotGenerated | 0     | Event not generated             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Generated    | 1     | Event generated                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.25.7.14 EVENTS\_DBLRDY

Address offset: 0x10C

Double displacement(s) detected

Event generated when REPORTPER number of samples has been accumulated and the content of the ACCDBL register is not equal to 0. (Thus, this event is only generated if a double transition is detected since the previous clearing of the ACCDBL register).

|                  |            |               |       |                                                                                                                                                                                                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|---------------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |               |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0                                                                                                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |               |       | A                                                                                                                                                                                                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |               |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                                                                                                                                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID      | Value | Description                                                                                                                                                                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | EVENTS_DBLRDY |       | Double displacement(s) detected                                                                                                                                                                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |               |       | Event generated when REPORTPER number of samples has been accumulated and the content of the ACCDBL register is not equal to 0. (Thus, this event is only generated if a double transition is detected since the previous clearing of the ACCDBL register). |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | NotGenerated  | 0     | Event not generated                                                                                                                                                                                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Generated     | 1     | Event generated                                                                                                                                                                                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.25.7.15 EVENTS\_STOPPED

Address offset: 0x110

QDEC has been stopped

|                  |            |                |       |                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|------------------|------------|----------------|-------|-----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|---|
| Bit number       |            |                |       | 31                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |   |
| ID               |            |                |       |                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | A |
| Reset 0x00000000 |            |                |       | 0                     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |   |
| ID               | Acce Field | Value ID       | Value | Description           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
| A                | RW         | EVENTS_STOPPED |       | QDEC has been stopped |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | NotGenerated   | 0     | Event not generated   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | Generated      | 1     | Event generated       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |

### 7.1.25.7.16 PUBLISH\_SAMPLERDY

Address offset: 0x180

Publish configuration for event [SAMPLERDY](#)

|                  |            |          |          |                                                                           |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
|------------------|------------|----------|----------|---------------------------------------------------------------------------|----|------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|--|
| Bit number       |            |          |          | 31                                                                        | 30 | 29                                                   | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |  |
| ID               |            |          |          | B                                                                         |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |  |
| Reset 0x00000000 |            |          |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| ID               | Acce Field |          | Value ID | Value                                                                     |    | Description                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| A                | RW CHIDX   |          |          | [255..0]                                                                  |    | Channel that event <b>SAMPLERDY</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| B                | RW EN      |          |          |                                                                           |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | Disabled | 0        | Disable publishing                                                        |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | Enabled  | 1        | Enable publishing                                                         |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |  |

### 7.1.25.7.17 PUBLISH\_REPORTRDY

Address offset: 0x184

Publish configuration for event [REPORTRDY](#)

Event generated when REPORTPER number of samples has been accumulated in the ACC register and the content of the ACC register is not equal to 0. (Thus, this event is only generated if a motion is detected since the previous clearing of the ACC register).

|                  |      |          |       |    |          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |                                                      |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|----------|-------|----|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|------------------------------------------------------|---|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |          |       | 31 | 30       | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                      |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |          |       | B  |          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A                                                    | A | A |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |          |       | 0  | 0        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |                                                      |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field    | Value | ID | Value    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | Description                                          |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW   | CHIDX    |       |    | [255..0] |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | Channel that event <b>REPORTRDY</b> will publish to. |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW   | EN       |       |    |          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |                                                      |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Disabled |       |    | 0        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | Disable publishing                                   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Enabled  |       |    | 1        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | Enable publishing                                    |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.25.7.18 PUBLISH\_ACCOF

Address offset: 0x188

Publish configuration for event [ACCOF](#)





| Bit number       |                         |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|-------------------------|----------|---------------------------------------------------------------------------------------|------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |                         |          | G F E D C B A                                                                         |                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |                         |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field              | Value ID | Value                                                                                 | Description                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW SAMPLERDY_STOP       | Enabled  | 1                                                                                     | Enable shortcut                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                         | Disabled | 0                                                                                     | Shortcut between event SAMPLERDY and task STOP       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                         | Disabled | 0                                                                                     | Disable shortcut                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW REPORTRDY_RDCLRACC   | Enabled  | 1                                                                                     | Enable shortcut                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                         | Disabled | 0                                                                                     | Shortcut between event REPORTRDY and task RDCLRACC   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                         | Disabled | 0                                                                                     | Disable shortcut                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| D                | RW REPORTRDY_STOP       | Enabled  | 1                                                                                     | Enable shortcut                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                         | Disabled | 0                                                                                     | Shortcut between event REPORTRDY and task STOP       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                         | Disabled | 0                                                                                     | Disable shortcut                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| E                | RW DBLRDY_RDCLRDBL      | Enabled  | 1                                                                                     | Enable shortcut                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                         | Disabled | 0                                                                                     | Shortcut between event DBLRDY and task RDCLRDBL      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                         | Disabled | 0                                                                                     | Disable shortcut                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| F                | RW DBLRDY_STOP          | Enabled  | 1                                                                                     | Enable shortcut                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                         | Disabled | 0                                                                                     | Shortcut between event DBLRDY and task STOP          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                         | Disabled | 0                                                                                     | Disable shortcut                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| G                | RW SAMPLERDY_READCLRACC | Enabled  | 1                                                                                     | Enable shortcut                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                         | Disabled | 0                                                                                     | Shortcut between event SAMPLERDY and task READCLRACC |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                         | Disabled | 0                                                                                     | Disable shortcut                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.25.7.22 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number       |              |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                                                                                                                                                                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|--------------|----------|---------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |              |          | E D C B A                                                                             |                                                                                                                                                                                                                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |              |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                                                                                                                                                                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field   | Value ID | Value                                                                                 | Description                                                                                                                                                                                                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW SAMPLERDY |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">SAMPLERDY</a>                                                                                                                                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Set      | 1                                                                                     | Enable                                                                                                                                                                                                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Disabled | 0                                                                                     | Read: Disabled                                                                                                                                                                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Enabled  | 1                                                                                     | Read: Enabled                                                                                                                                                                                                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW REPORTRDY |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">REPORTRDY</a>                                                                                                                                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              |          |                                                                                       | Event generated when REPORTPER number of samples has been accumulated in the ACC register and the content of the ACC register is not equal to 0. (Thus, this event is only generated if a motion is detected since the previous clearing of the ACC register). |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Set      | 1                                                                                     | Enable                                                                                                                                                                                                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Disabled | 0                                                                                     | Read: Disabled                                                                                                                                                                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  | Enabled      | 1        | Read: Enabled                                                                         |                                                                                                                                                                                                                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW ACCOF     |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">ACCOF</a>                                                                                                                                                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Set      | 1                                                                                     | Enable                                                                                                                                                                                                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Disabled | 0                                                                                     | Read: Disabled                                                                                                                                                                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Enabled  | 1                                                                                     | Read: Enabled                                                                                                                                                                                                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                                                                                                                                                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |            |          | E D C B A                                                                             |                                                                                                                                                                                                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                                                                                                                                                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                                                                                                                                                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| D                | RW DBLRDY  |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">DBLRDY</a>                                                                                                                                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |          |                                                                                       | Event generated when REPORTPER number of samples has been accumulated and the content of the ACCDBL register is not equal to 0. (Thus, this event is only generated if a double transition is detected since the previous clearing of the ACCDBL register). |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Set      | 1                                                                                     | Enable                                                                                                                                                                                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Read: Disabled                                                                                                                                                                                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Read: Enabled                                                                                                                                                                                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| E                | RW STOPPED |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">STOPPED</a>                                                                                                                                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Set      | 1                                                                                     | Enable                                                                                                                                                                                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Read: Disabled                                                                                                                                                                                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Read: Enabled                                                                                                                                                                                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.25.7.23 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number       |              | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                                                                                                                                                                                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|--------------|---------------------------------------------------------------------------------------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |              | E D C B A                                                                             |       |                                                                                                                                                                                                                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |              | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |       |                                                                                                                                                                                                                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field   | Value ID                                                                              | Value | Description                                                                                                                                                                                                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW SAMPLERDY |                                                                                       |       | Write '1' to disable interrupt for event <a href="#">SAMPLERDY</a>                                                                                                                                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Clear                                                                                 | 1     | Disable                                                                                                                                                                                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Disabled                                                                              | 0     | Read: Disabled                                                                                                                                                                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Enabled                                                                               | 1     | Read: Enabled                                                                                                                                                                                                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW REPORTRDY |                                                                                       |       | Write '1' to disable interrupt for event <a href="#">REPORTRDY</a>                                                                                                                                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              |                                                                                       |       | Event generated when REPORTPER number of samples has been accumulated in the ACC register and the content of the ACC register is not equal to 0. (Thus, this event is only generated if a motion is detected since the previous clearing of the ACC register). |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Clear                                                                                 | 1     | Disable                                                                                                                                                                                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Disabled                                                                              | 0     | Read: Disabled                                                                                                                                                                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Enabled                                                                               | 1     | Read: Enabled                                                                                                                                                                                                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW ACCOF     |                                                                                       |       | Write '1' to disable interrupt for event <a href="#">ACCOF</a>                                                                                                                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Clear                                                                                 | 1     | Disable                                                                                                                                                                                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Disabled                                                                              | 0     | Read: Disabled                                                                                                                                                                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Enabled                                                                               | 1     | Read: Enabled                                                                                                                                                                                                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| D                | RW DBLRDY    |                                                                                       |       | Write '1' to disable interrupt for event <a href="#">DBLRDY</a>                                                                                                                                                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              |                                                                                       |       | Event generated when REPORTPER number of samples has been accumulated and the content of the ACCDBL register is not equal to 0. (Thus, this event is only generated if a double transition is detected since the previous clearing of the ACCDBL register).    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Clear                                                                                 | 1     | Disable                                                                                                                                                                                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Disabled                                                                              | 0     | Read: Disabled                                                                                                                                                                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |



|                  |            |          |       |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|-------|----|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          | 31    | 30 | 29          | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |          |       |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |          | 0     |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID | Value |    | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | 256us    | 1     |    | 256 us      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | 512us    | 2     |    | 512 us      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | 1024us   | 3     |    | 1024 us     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | 2048us   | 4     |    | 2048 us     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | 4096us   | 5     |    | 4096 us     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | 8192us   | 6     |    | 8192 us     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | 16384us  | 7     |    | 16384 us    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | 32ms     | 8     |    | 32768 us    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | 65ms     | 9     |    | 65536 us    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | 131ms    | 10    |    | 131072 us   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.25.7.27 SAMPLE

Address offset: 0x50C

Motion sample value

|                  |            |        |  |          |         |  |       |  |  |                    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------|--|----------|---------|--|-------|--|--|--------------------|----|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |        |  |          |         |  |       |  |  | 31                 | 30 | 29          | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |        |  |          |         |  |       |  |  | A                  | A  | A           | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A | A | A |   |
| Reset 0x00000000 |            |        |  |          |         |  |       |  |  | 0                  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |        |  | Value ID |         |  | Value |  |  |                    |    | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | R          | SAMPLE |  |          | [-1..2] |  |       |  |  | Last motion sample |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

The value is a 2's complement value, and the sign gives the direction of the motion. The value '2' indicates a double transition.

### 7.1.25.7.28 REPORTPER

Address offset: 0x510

Number of samples to be taken before REPORTRDY and DBLRDY events can be generated

| Bit number       |            |                      | 31                                                                    | 30                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |        |   |                     |        |   |                     |        |   |                     |         |   |                      |         |   |                      |         |   |                      |         |   |                      |         |   |                      |       |   |                   |
|------------------|------------|----------------------|-----------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|--|--------|---|---------------------|--------|---|---------------------|--------|---|---------------------|---------|---|----------------------|---------|---|----------------------|---------|---|----------------------|---------|---|----------------------|---------|---|----------------------|-------|---|-------------------|
| ID               |            |                      | A A A A                                                               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |        |   |                     |        |   |                     |        |   |                     |         |   |                      |         |   |                      |         |   |                      |         |   |                      |         |   |                      |       |   |                   |
| Reset 0x00000000 |            |                      | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |        |   |                     |        |   |                     |        |   |                     |         |   |                      |         |   |                      |         |   |                      |         |   |                      |         |   |                      |       |   |                   |
| ID               | Acce Field | Value ID             | Value                                                                 | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |        |   |                     |        |   |                     |        |   |                     |         |   |                      |         |   |                      |         |   |                      |         |   |                      |         |   |                      |       |   |                   |
| A                | RW         | REPORTPER            |                                                                       | <p>Specifies the number of samples to be accumulated in the ACC register before the REPORTRDY and DBLRDY events can be generated</p> <p>The report period in [us] is given as: <math>RPUS = SP * RP</math> Where RPUS is the report period in [us/report], SP is the sample period in [us/sample] specified in SAMPLEPER, and RP is the report period in [samples/report] specified in REPORTPER .</p> <table><tr><td>10Smpl</td><td>0</td><td>10 samples / report</td></tr><tr><td>40Smpl</td><td>1</td><td>40 samples / report</td></tr><tr><td>80Smpl</td><td>2</td><td>80 samples / report</td></tr><tr><td>120Smpl</td><td>3</td><td>120 samples / report</td></tr><tr><td>160Smpl</td><td>4</td><td>160 samples / report</td></tr><tr><td>200Smpl</td><td>5</td><td>200 samples / report</td></tr><tr><td>240Smpl</td><td>6</td><td>240 samples / report</td></tr><tr><td>280Smpl</td><td>7</td><td>280 samples / report</td></tr><tr><td>1Smpl</td><td>8</td><td>1 sample / report</td></tr></table> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  | 10Smpl | 0 | 10 samples / report | 40Smpl | 1 | 40 samples / report | 80Smpl | 2 | 80 samples / report | 120Smpl | 3 | 120 samples / report | 160Smpl | 4 | 160 samples / report | 200Smpl | 5 | 200 samples / report | 240Smpl | 6 | 240 samples / report | 280Smpl | 7 | 280 samples / report | 1Smpl | 8 | 1 sample / report |
| 10Smpl           | 0          | 10 samples / report  |                                                                       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |        |   |                     |        |   |                     |        |   |                     |         |   |                      |         |   |                      |         |   |                      |         |   |                      |         |   |                      |       |   |                   |
| 40Smpl           | 1          | 40 samples / report  |                                                                       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |        |   |                     |        |   |                     |        |   |                     |         |   |                      |         |   |                      |         |   |                      |         |   |                      |         |   |                      |       |   |                   |
| 80Smpl           | 2          | 80 samples / report  |                                                                       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |        |   |                     |        |   |                     |        |   |                     |         |   |                      |         |   |                      |         |   |                      |         |   |                      |         |   |                      |       |   |                   |
| 120Smpl          | 3          | 120 samples / report |                                                                       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |        |   |                     |        |   |                     |        |   |                     |         |   |                      |         |   |                      |         |   |                      |         |   |                      |         |   |                      |       |   |                   |
| 160Smpl          | 4          | 160 samples / report |                                                                       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |        |   |                     |        |   |                     |        |   |                     |         |   |                      |         |   |                      |         |   |                      |         |   |                      |         |   |                      |       |   |                   |
| 200Smpl          | 5          | 200 samples / report |                                                                       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |        |   |                     |        |   |                     |        |   |                     |         |   |                      |         |   |                      |         |   |                      |         |   |                      |         |   |                      |       |   |                   |
| 240Smpl          | 6          | 240 samples / report |                                                                       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |        |   |                     |        |   |                     |        |   |                     |         |   |                      |         |   |                      |         |   |                      |         |   |                      |         |   |                      |       |   |                   |
| 280Smpl          | 7          | 280 samples / report |                                                                       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |        |   |                     |        |   |                     |        |   |                     |         |   |                      |         |   |                      |         |   |                      |         |   |                      |         |   |                      |       |   |                   |
| 1Smpl            | 8          | 1 sample / report    |                                                                       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |        |   |                     |        |   |                     |        |   |                     |         |   |                      |         |   |                      |         |   |                      |         |   |                      |         |   |                      |       |   |                   |

### 7.1.25.7.29 ACC

Address offset: 0x514

Register accumulating the valid transitions

|                  |            |     |          |               |    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-----|----------|---------------|----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |     |          | 31            | 30 | 29                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |     |          | A             | A  | A                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |     |          | 0             | 0  | 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |     | Value ID | Value         |    | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | R          | ACC |          | [-1024..1023] |    | <p>Register accumulating all valid samples (not double transition) read from the SAMPLE register</p> <p>Double transitions ( SAMPLE = 2 ) will not be accumulated in this register. The value is a 32 bit 2's complement value.</p> <p>If a sample that would cause this register to overflow or underflow is received, the sample will be ignored and an overflow event ( ACCOF ) will be generated. The ACC register is cleared by triggering the READCLRACC or the RDCLRACC task.</p> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.25.7.30 ACCREAD

Address offset: 0x518

Snapshot of the ACC register, updated by the READCLRACC or RDCLRACC task

|                  |            |         |          |               |    |    |    |                                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|---------|----------|---------------|----|----|----|-----------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |         |          | 31            | 30 | 29 | 28 | 27                                                                                | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |         |          | A             | A  | A  | A  | A                                                                                 | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |         |          | 0             | 0  | 0  | 0  | 0                                                                                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |         | Value ID | Value         |    |    |    | Description                                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | R          | ACCREAD |          | [-1024..1023] |    |    |    | Snapshot of the ACC register.                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |         |          |               |    |    |    | The ACCREAD register is updated when the READCLRACC or RDCLRACC task is triggered |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.25.7.31 PSEL.LED

Address offset: 0x51C

Pin select for LED signal

|                  |            |              |                                                                                       |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|--------------|---------------------------------------------------------------------------------------|-------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |              | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |              | C <span style="float:right">B A A A A A</span>                                        |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0xFFFFFFFF |            |              | 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1   |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID     | Value                                                                                 | Description |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW PIN     |              | [0..31]                                                                               | Pin number  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW PORT    |              | [0..1]                                                                                | Port number |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW CONNECT |              |                                                                                       | Connection  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disconnected | 1                                                                                     | Disconnect  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Connected    | 0                                                                                     | Connect     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.25.7.32 PSEL.A

Address offset: 0x520

Pin select for A signal

|                  |            |              |                                                                                       |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|--------------|---------------------------------------------------------------------------------------|-------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |              | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |              | C                                                                                     |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0xFFFFFFFF |            |              | 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1   |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID     | Value                                                                                 | Description |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW PIN     |              | [0..31]                                                                               | Pin number  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW PORT    |              | [0..1]                                                                                | Port number |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW CONNECT |              |                                                                                       | Connection  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disconnected | 1                                                                                     | Disconnect  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Connected    | 0                                                                                     | Connect     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.25.7.33 PSEL.B

Address offset: 0x524

Pin select for B signal

|                  |            |              |                                                                                       |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |
|------------------|------------|--------------|---------------------------------------------------------------------------------------|-------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------|--|--|--|--|--|--|--|
| Bit number       |            |              | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |
| ID               |            |              | C                                                                                     |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | B A A A A A |  |  |  |  |  |  |  |
| Reset 0xFFFFFFFF |            |              | 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1                       |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID     | Value                                                                                 | Description |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |
| A                | RW PIN     |              | [0..31]                                                                               | Pin number  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |
| B                | RW PORT    |              | [0..1]                                                                                | Port number |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |
| C                | RW CONNECT |              |                                                                                       | Connection  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |
|                  |            | Disconnected | 1                                                                                     | Disconnect  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |
|                  |            | Connected    | 0                                                                                     | Connect     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |

### 7.1.25.7.34 DBFEN

Address offset: 0x528

Enable input debounce filters

|                  |            |       |          |       |    |                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |
|------------------|------------|-------|----------|-------|----|---------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|
| Bit number       |            |       |          | 31    | 30 | 29                              | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |
| ID               |            |       |          |       |    |                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |  |
| Reset 0x00000000 |            |       |          | 0     | 0  | 0                               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |
| ID               | Acce Field |       | Value ID | Value |    | Description                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |
| A                | RW         | DBFEN |          |       |    | Enable input debounce filters   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |            |       | Disabled | 0     |    | Debounce input filters disabled |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |            |       | Enabled  | 1     |    | Debounce input filters enabled  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |

### 7.1.25.7.35 LEDPRE

Address offset: 0x540

Time period the LED is switched ON prior to sampling

|                  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |     |
|------------------|--|--|--|--|--|--|--|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----|
| Bit number       |  |  |  |  |  |  |  |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |     |
| ID               |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  | A  | A | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |     |
| Reset 0x00000010 |  |  |  |  |  |  |  |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0</ |

### 7.1.25.7.36 ACCDBL

Address offset: 0x544

Register accumulating the number of detected double transitions

|                  |            |          |         |                                                                                                                                                                                                                                                                                                                                                                                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          |         | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0                                                                                                                                                                                                                                                                                                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          |         | A A A A                                                                                                                                                                                                                                                                                                                                                                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          |         | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                                                                                                                                                                                                                                                                                                                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value   | Description                                                                                                                                                                                                                                                                                                                                                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | R          | ACCDBL   | [0..15] | <p>Register accumulating the number of detected double or illegal transitions. ( SAMPLE = 2 ).</p> <p>When this register has reached its maximum value the accumulation of double / illegal transitions will stop. An overflow event ( ACCOF ) will be generated if any double or illegal transitions are detected after the maximum value was reached. This field is cleared by triggering the READCLRACC or RDCLRDBL task.</p> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.25.7.37 ACCDBLREAD

Address offset: 0x548

Snapshot of the ACCDBL, updated by the READCLRACC or RDCLRDBL task

|                  |            |           |          |         |    |    |    |                                                                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-----------|----------|---------|----|----|----|-----------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |           |          | 31      | 30 | 29 | 28 | 27                                                                                                        | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |
| ID               |            |           |          |         |    |    |    |                                                                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A | A | A | A |
| Reset 0x00000000 |            |           |          | 0       | 0  | 0  | 0  | 0                                                                                                         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce Field |           | Value ID | Value   |    |    |    | Description                                                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | R          | ACCDLREAD |          | [0..15] |    |    |    | Snapshot of the ACCDBL register. This field is updated when the READCLRACC or RDCLRDBL task is triggered. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

## 7.1.25.8 Electrical specification

### 7.1.25.8.1 QDEC Electrical Specification

| Symbol              | Description                                           | Min. | Typ. | Max. | Units         |
|---------------------|-------------------------------------------------------|------|------|------|---------------|
| $t_{\text{SAMPLE}}$ | Time between sampling signals from quadrature decoder | ..   | ..   | ..   | $\mu\text{s}$ |
| $t_{\text{LED}}$    | Time from LED is turned on to signals are sampled     | ..   | ..   | ..   | $\mu\text{s}$ |

## 7.1.26 QSPI — Quad serial peripheral interface

The QSPI peripheral provides support for communicating with an external flash memory device using SPI.

Listed here are the main features for the QSPI peripheral:

- Single/dual/quad SPI input/output
- 6–96 MHz configurable clock frequency
- Single-word read/write access from/to external flash
- EasyDMA for block read and write transfers
- Up to 48 MB/sec EasyDMA read rate
- Execute in place (XIP) for executing program directly from external flash
- XIP access can optionally be disabled
- On-the-fly encryption and decryption, including EasyDMA and XIP

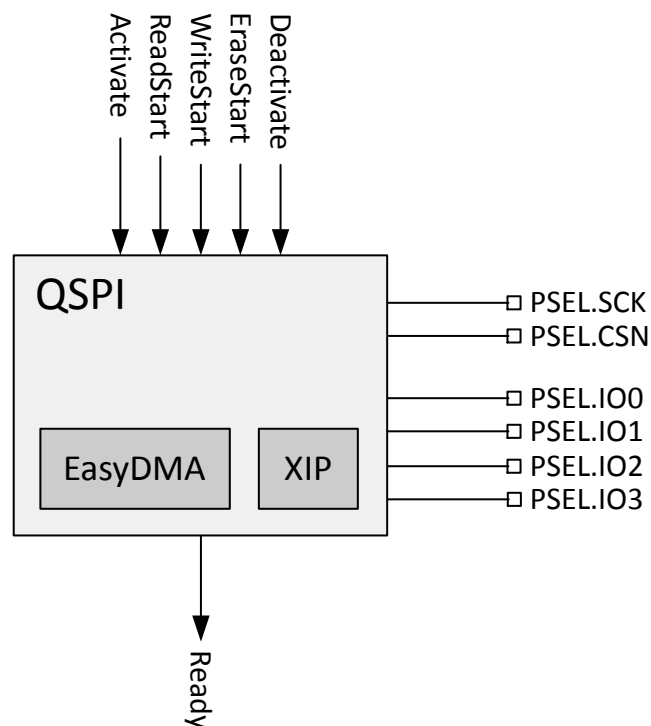


Figure 113: Block diagram

### 7.1.26.1 Configuring peripheral

Before any data can be transferred to or from the external flash memory, the peripheral needs to be configured.



1. Select input/output pins in [PSEL.SCK](#) on page 398, [PSEL.CSN](#) on page 398, [PSEL.IO0](#) on page 399, [PSEL.IO1](#) on page 399, [PSEL.IO2](#) on page 399, and [PSEL.IO3](#) on page 399. See [Reference circuitry](#) on page 768 for the recommended pins.
2. To ensure stable operation, set the GPIO drive strength to “high drive”. See the [GPIO — General purpose input/output](#) on page 209 chapter for details on how to configure GPIO drive strength.
3. Configure the interface towards the external flash memory using [IFCONFIG0](#) on page 400, [IFCONFIG1](#) on page 405, and [ADDRCONF](#) on page 406.
4. Enable the QSPI peripheral and acquire I/O pins using [ENABLE](#) on page 396.
5. Activate the external flash memory interface using the ACTIVATE task. The READY event will be generated when the interface has been activated and the external flash memory is ready for access.

**Important:**

If the [IFCONFIG0](#) on page 400 register is configured to use the quad mode, the external flash device also needs to be set in the quad mode before any data transfers can take place.

This can be done by sending custom instructions to the external flash device, as described in [Sending custom instructions](#) on page 383.

### 7.1.26.2 Write operation

A write operation to the external flash is configured using the [WRITE.DST](#) on page 397, [WRITE.SRC](#) on page 397, and [WRITE.CNT](#) on page 397 registers and started using the WRITESTART task.

The READY event is generated when the transfer is complete.

The QSPI peripheral automatically takes care of splitting DMA transfers into page writes.

### 7.1.26.3 Read operation

A read operation from the external flash is configured using the [READ.SRC](#) on page 396, [READ.DST](#) on page 396, and [READ.CNT](#) on page 397 registers and started using the READSTART task.

The READY event is generated when the transfer is complete.

### 7.1.26.4 Erase operation

Erase of pages/blocks of the external flash is configured using the [ERASE.PTR](#) on page 397 and [ERASE.LEN](#) on page 398 registers and started using the ERASESTART task.

The READY event is generated when the erase operation has been started.

Note that in this case the READY event will not indicate that the erase operation of the flash has been completed, but it only signals that the erase operation has been started. The actual status of the erase operation can normally be read from the external flash using a custom instruction, see [Sending custom instructions](#) on page 383.

### 7.1.26.5 Execute in place

Execute in place (XIP) allows the CPU to execute program code directly from the external flash.

After the external flash has been configured, the CPU can execute code from the external flash by accessing the XIP memory region. See the figure below and [Memory](#) on page 18 for details.

Note that the XIP memory region is read-only, writing to it will result in a bus error.

When accessing the XIP memory region, the start address of this XIP memory region will map to the address [XIPOFFSET](#) on page 400 of the external flash.

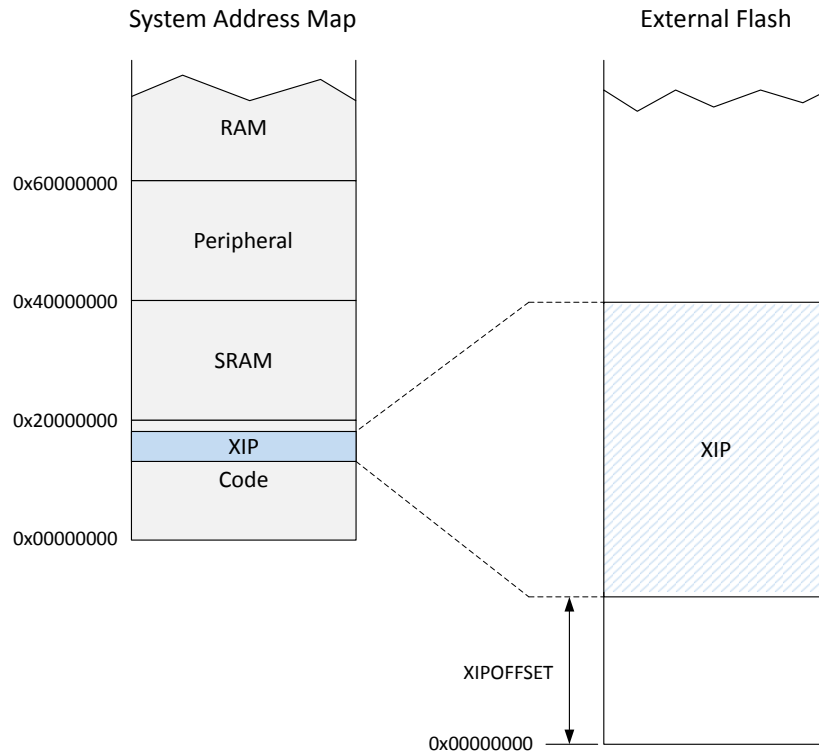


Figure 114: XIP memory map

### 7.1.26.6 Encryption

The contents of an external flash memory can be protected using stream cipher encryption. Encryption can be configured and enabled independently for XIP and EasyDMA, with separate keys and nonce.

Once configured and enabled, the stream cipher operates between the AHB bus and the external flash, encrypting and decrypting data passing through.

Figure [Figure 115: Stream cipher](#) on page 382 shows the stream cipher block with the three configuration registers. The stream cipher uses an AES 128 encryption operation to form the keystream from key, nonce and external memory address. The keystream then combines each 32-bit plaintext digit one at a time with the corresponding digit of the keystream.

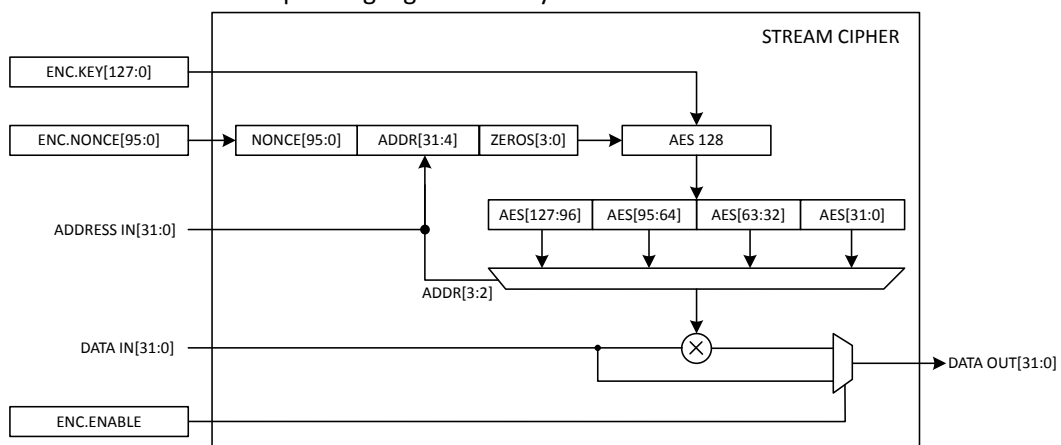


Figure 115: Stream cipher

**Note:** The same nonce and key must be used for both encryption and decryption of the same memory address.

The memory address used for encryption is the external flash memory address and thus independent of [XIPOFFSET](#) on page 400. This means a second firmware image can be encrypted and written using EasyDMA, then [XIPOFFSET](#) on page 400 set to point to the new firmware image before executing from it.

**Note:** Stream ciphers are symmetric. They do not differentiate between encrypting or decrypting, reading or writing. Thus, if the contents of a plain text external flash is read when stream cipher is enabled, the data provided to the MCU are encrypted.

## Execute in place (XIP)

Stream cipher for QSPI XIP is enabled by

1. Configuring keys using [XIP\\_ENC.KEY0](#) on page 401 through [XIP\\_ENC.KEY3](#) on page 402
2. Configuring nonce using [XIP\\_ENC.NONCE0](#) on page 402 through [XIP\\_ENC.NONCE2](#) on page 402
3. Setting [XIP\\_ENC.ENABLE](#) on page 403

Any instructions or data read from the XIP interface will now pass through the stream cipher.

## EasyDMA

Stream cipher for QSPI EasyDMA is enabled by

1. Configuring keys using [DMA\\_ENC.KEY0](#) on page 403 through [DMA\\_ENC.KEY3](#) on page 403
2. Configuring nonce using [DMA\\_ENC.NONCE0](#) on page 404 through [DMA\\_ENC.NONCE2](#) on page 404
3. Setting [DMA\\_ENC.ENABLE](#) on page 404

Any data read from, or written to, the external flash over the EasyDMA interface will now pass through the stream cipher.

### 7.1.26.7 Sending custom instructions

Custom instructions can be sent to the external flash using the [CINSTRCONF](#) on page 407, [CINSTRDAT0](#) on page 407, and [CINSTRDAT1](#) on page 408 registers. It is possible to send an instruction consisting of a one-byte opcode and up to 8 bytes of additional data and to read its response.

A custom instruction is prepared by first writing the data to be sent to [CINSTRDAT0](#) on page 407 and [CINSTRDAT1](#) on page 408 before writing the opcode and other configurations to the [CINSTRCONF](#) on page 407 register.

The custom instruction is sent when the [CINSTRCONF](#) on page 407 register is written and it is always sent on a single data line SPI interface.

The READY event will be generated when the custom instruction has been sent.

After a custom instruction has been sent, the [CINSTRDAT0](#) on page 407 and [CINSTRDAT1](#) on page 408 will contain the response bytes from the custom instruction.

Data of custom instructions are not part of the stream cipher encryption.

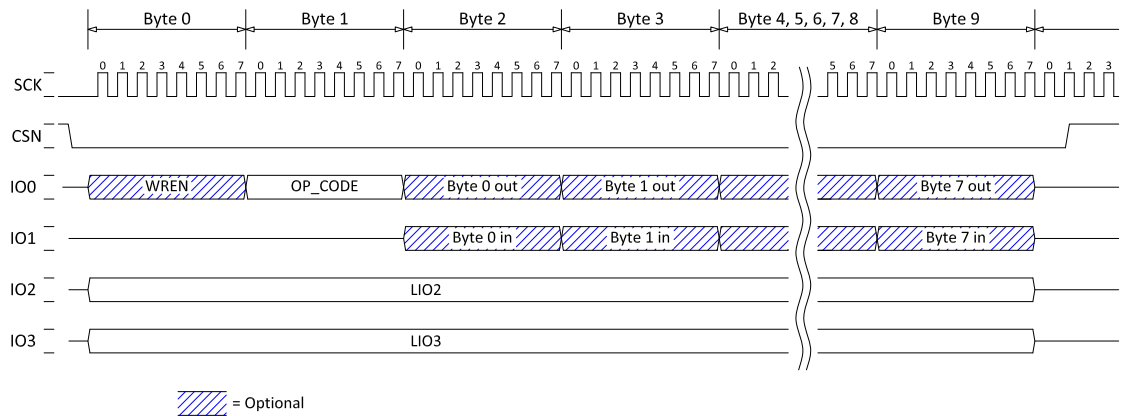


Figure 116: Sending custom instruction

### 7.1.26.7.1 Long frame mode

The LFEN and LFSTOP fields in the [CINSTRCONF](#) on page 407 control the operation of the custom instruction long frame mode. The long frame mode is a mechanism that permits arbitrary byte length custom instructions. While in long frame mode a long custom instruction sequence is split in multiple writes to the [CINSTRDAT0](#) on page 407 and [CINSTRDAT1](#) on page 408 registers.

To enable the long frame mode every write to the [CINSTRCONF](#) on page 407 register must have the LFEN field set to 1. The contents of the OP\_CODE field will be transmitted after the first write to [CINSTRCONF](#) on page 407 and will be omitted in every subsequent write to this register. For subsequent writes the number of data bytes as specified in the LENGTH field are transferred (that is the value of LENGTH - 1 data bytes). The values of the LIO2 and LIO3 fields are set in the first write to [CINSTRCONF](#) on page 407 and will apply for the entire custom instruction transmission until the long frame is finalized.

To finalize a long frame transmission, the LFSTOP field in [CINSTRCONF](#) on page 407 must be set to 1 in the last write to this register.

### 7.1.26.8 Deep power-down mode

The external flash memory can be put in deep power-down mode (DPM) to minimize its current consumption when there is no need to access the memory.

DPM is enabled in the [IFCONFIG0](#) on page 400 register and configured in the [DPM DUR](#) on page 406 register. The DPM status of the external memory can be read in the [STATUS](#) on page 405 register. The DPM DUR register has to be configured according to the external flash specification to get the information in the STATUS register and the timing of the READY event correct.

Entering/exiting DPM is controlled using the [IFCONFIG1](#) on page 405 register.

### 7.1.26.9 Instruction set

The table below shows the instruction set being used by the QSPI peripheral when communicating with an external flash device.

| Instruction | Opcode                                                         | Description                    |
|-------------|----------------------------------------------------------------|--------------------------------|
| WREN        | 0x06                                                           | Write enable                   |
| RDSR        | 0x05                                                           | Read status register           |
| WRSR        | 0x01                                                           | Write status register          |
| FASTREAD    | 0x0B                                                           | Read bytes at higher speed     |
| READ2O      | 0x3B                                                           | Dual-read output               |
| READ2IO     | 0xBB                                                           | Dual-read input/output         |
| READ4O      | 0x6B                                                           | Quad-read output               |
| READ4IO     | 0xEB                                                           | Quad-read input/output         |
| PP          | 0x02                                                           | Page program                   |
| PP2O        | 0xA2                                                           | Dual-page program output       |
| PP4O        | 0x32                                                           | Quad-page program output       |
| PP4IO       | 0x38                                                           | Quad-page program input/output |
| SE          | 0x20                                                           | Sector erase                   |
| BE          | 0xD8                                                           | Block erase                    |
| CE          | 0xC7                                                           | Chip erase                     |
| DP          | 0xB9                                                           | Enter deep power-down mode     |
| DPE         | 0xAB                                                           | Exit deep power-down mode      |
| EN4B        | Specified in the <a href="#">ADDRCONF</a> on page 406 register | Enable 32 bit address mode     |

Table 118: Instruction set

### 7.1.26.10 Interface description

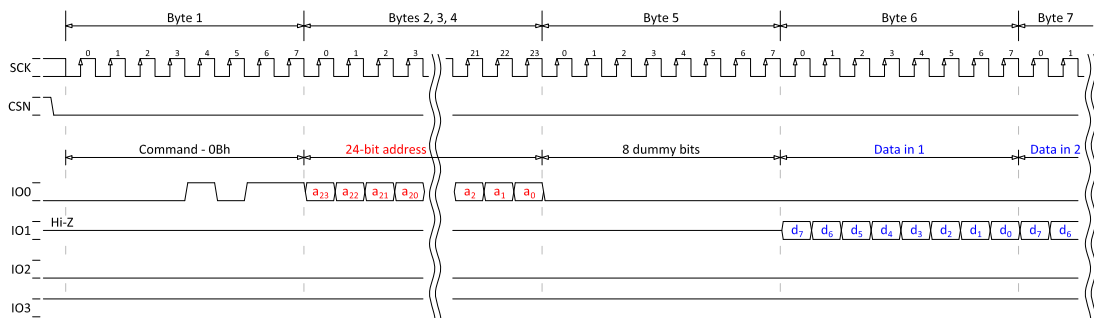


Figure 117: 24-bit FASTREAD, SPI MODE = MODE0

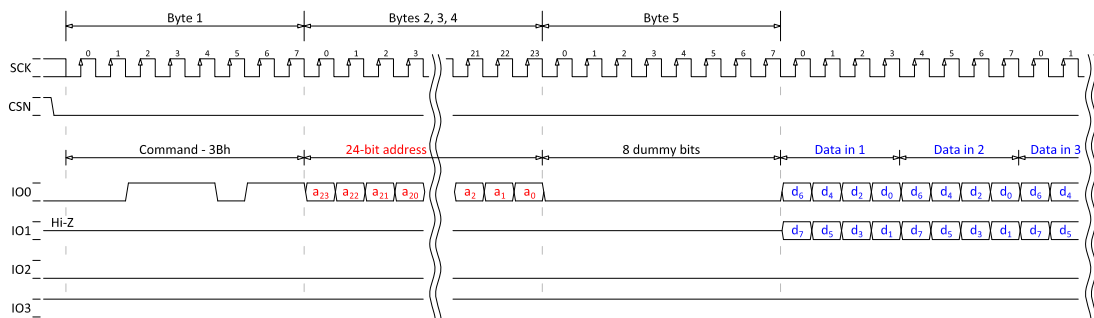


Figure 118: 24-bit READ2O (dual-read output), SPI MODE = MODE0

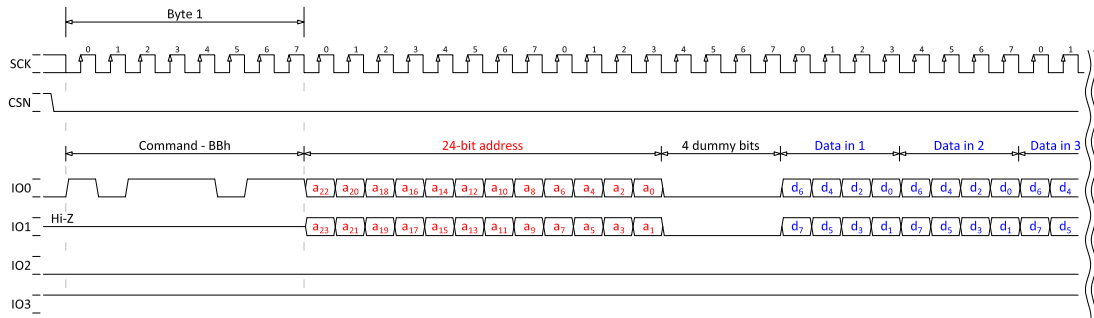


Figure 119: 24-bit READ2IO (dual read input/output), SPIMODE = MODE0

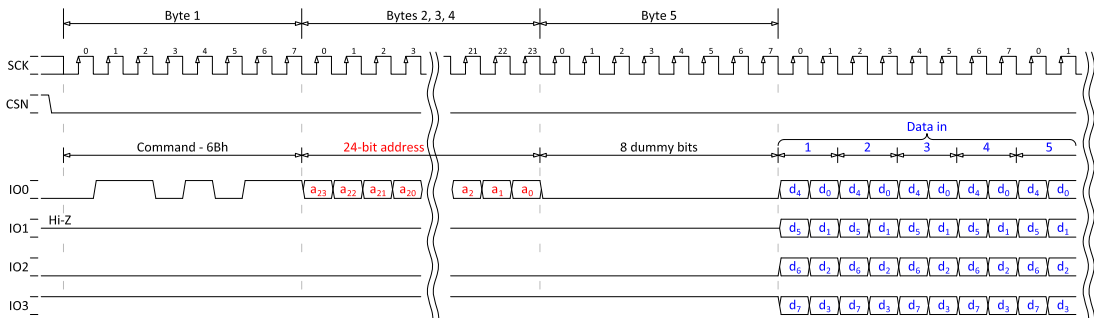


Figure 120: 24-bit READ4O (quad-read output), SPIMODE = MODE0

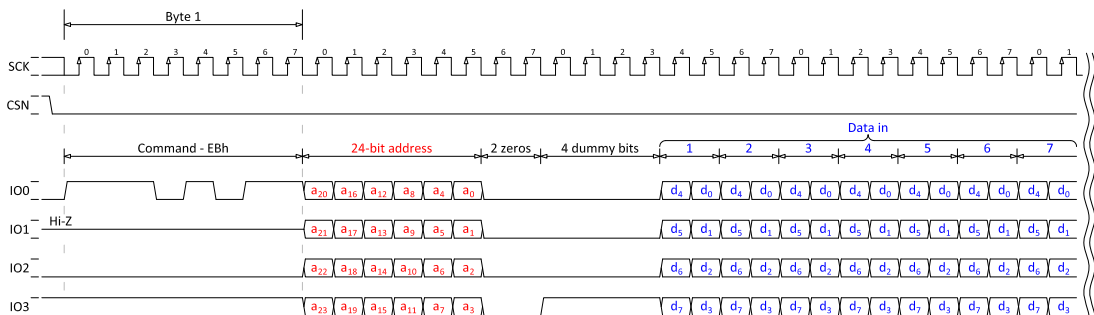


Figure 121: 24-bit READ4IO (quad-read input/output), SPIMODE = MODE0

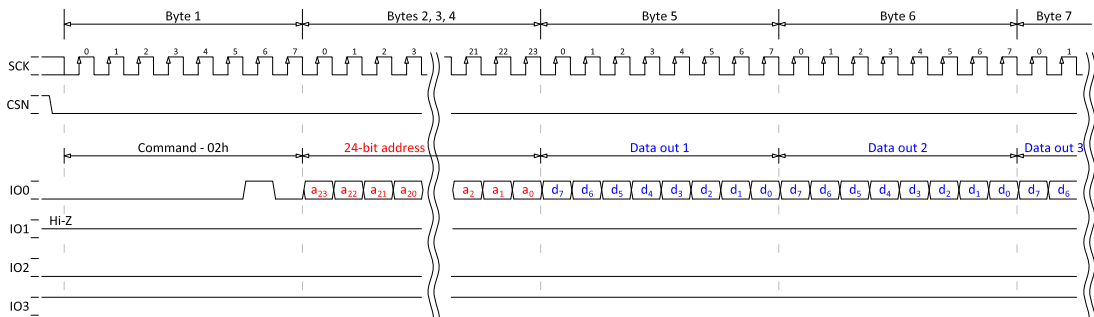


Figure 122: 24-bit PP (page program), SPIMODE = MODE0

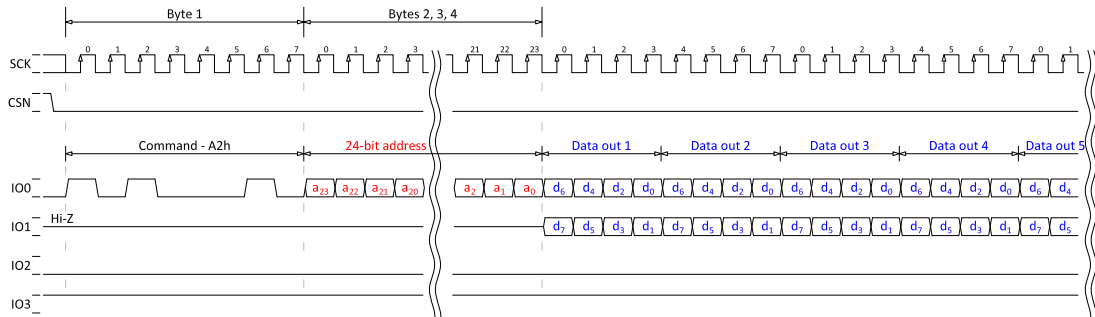


Figure 123: 24-bit PP2O (dual-page program output), SPI MODE = MODE0

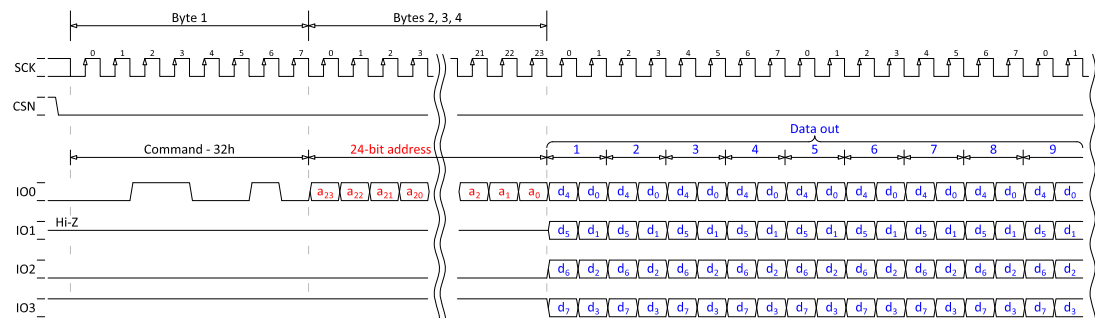


Figure 124: 24-bit PP4O (quad page program output), SPI MODE = MODE0

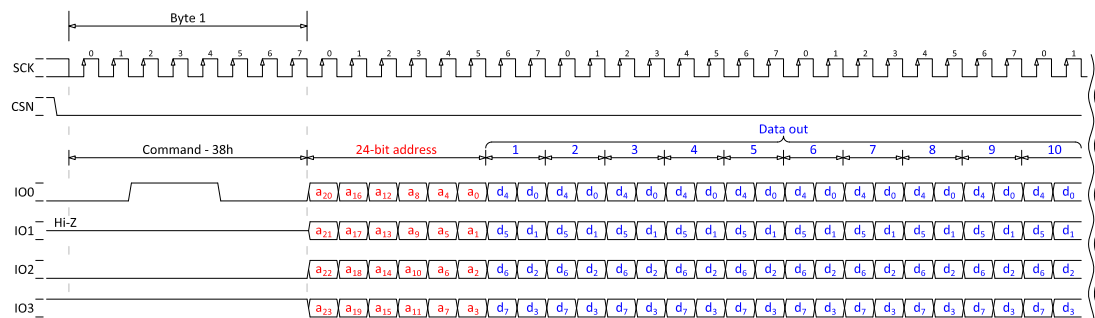


Figure 125: 24-bit PP4IO (quad page program input/output), SPI MODE = MODE0

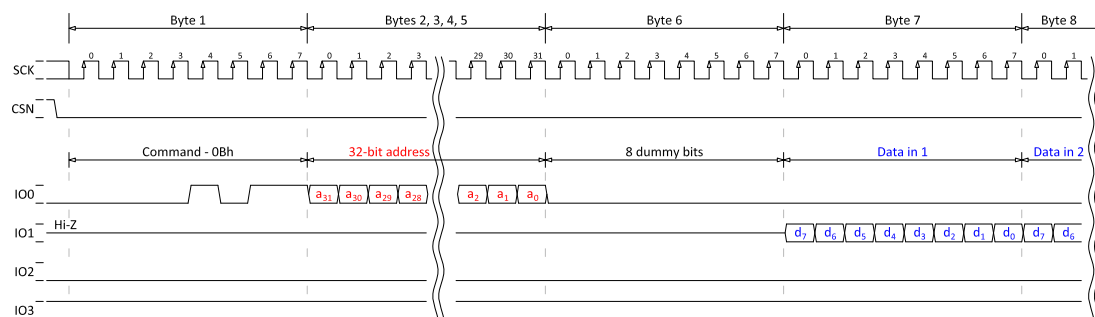


Figure 126: 32-bit FASTREAD, SPI MODE = MODE0

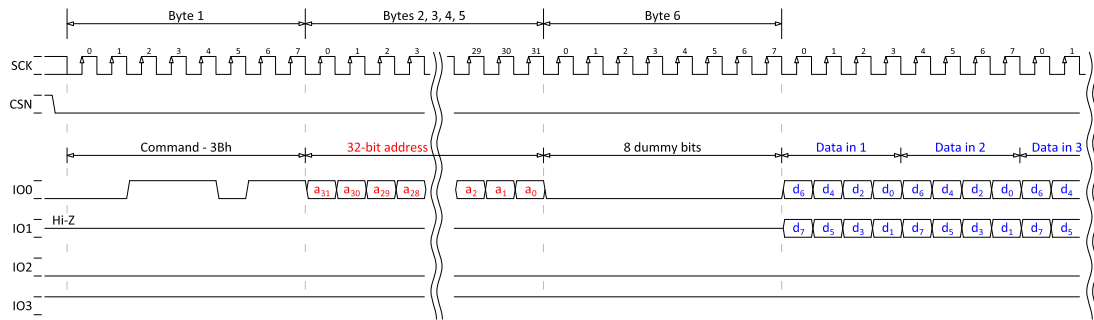


Figure 127: 32-bit READ2O (dual-read output), SPIMODE = MODE0

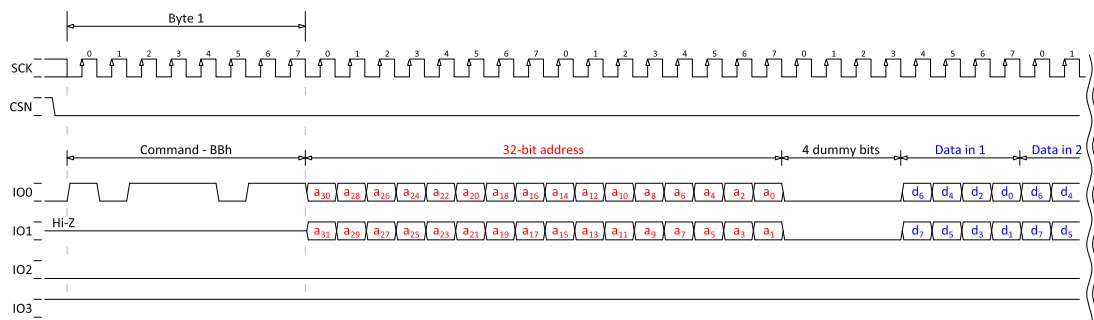


Figure 128: 32-bit READ2IO (dual read input/output), SPIMODE = MODE0

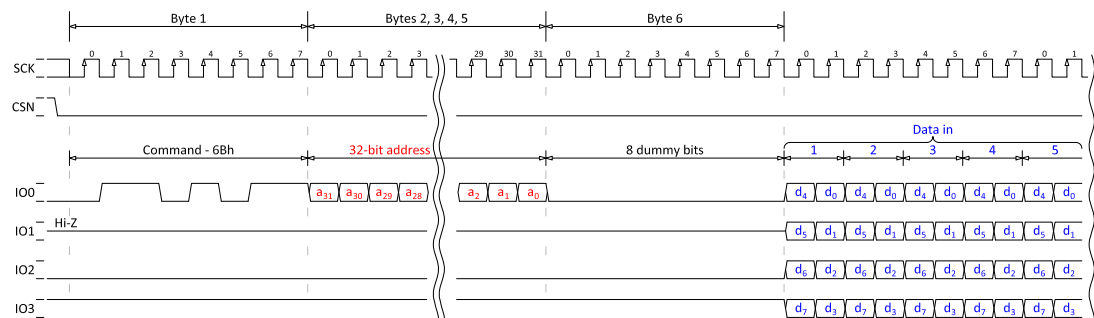


Figure 129: 32-bit READ4O (quad-read output), SPIMODE = MODE0

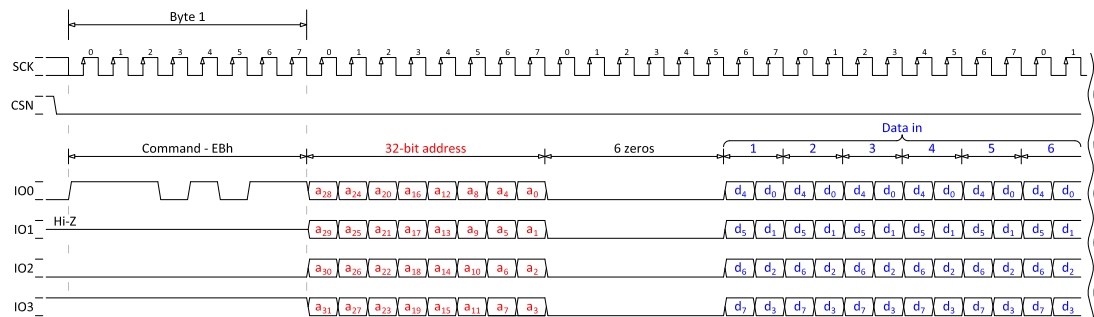


Figure 130: 32-bit READ4IO (quad-read input/output), SPIMODE = MODE0



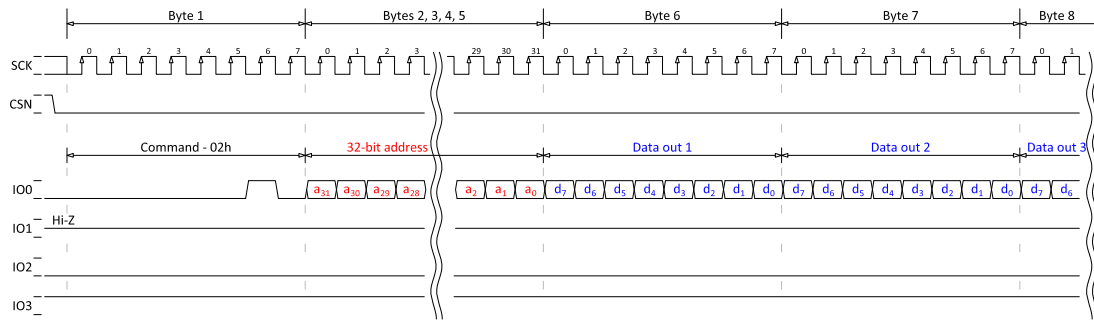


Figure 131: 32-bit PP (page program), SPI MODE = MODE0

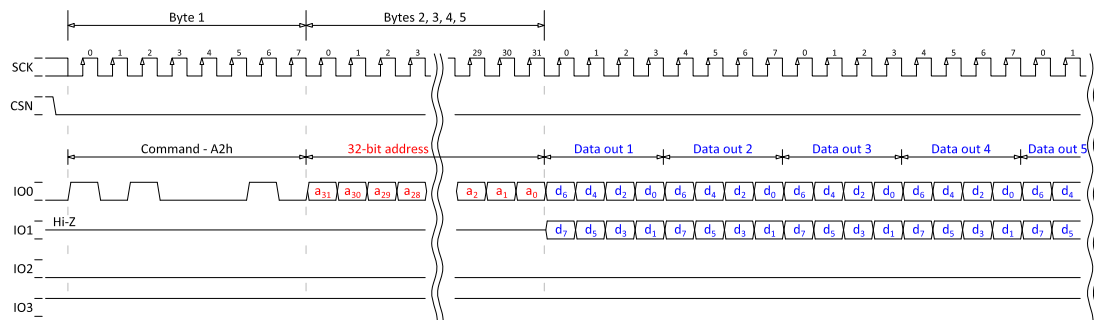


Figure 132: 32-bit PP2O (dual-page program output), SPI MODE = MODE0

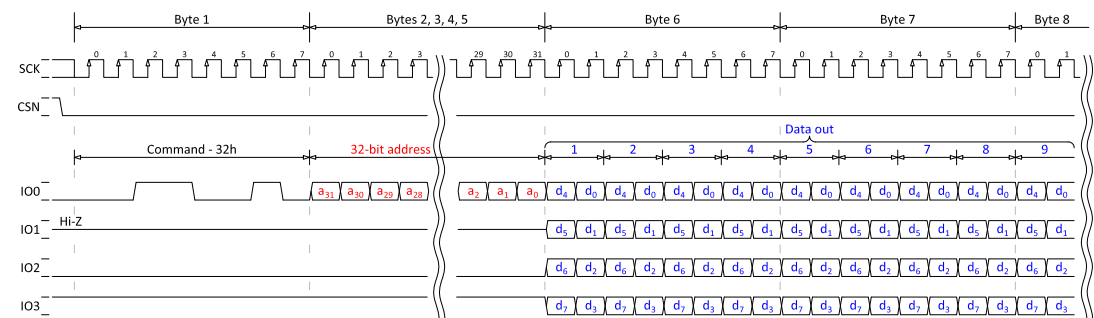


Figure 133: 32-bit PP4O (quad-page program output), SPI MODE = MODE0

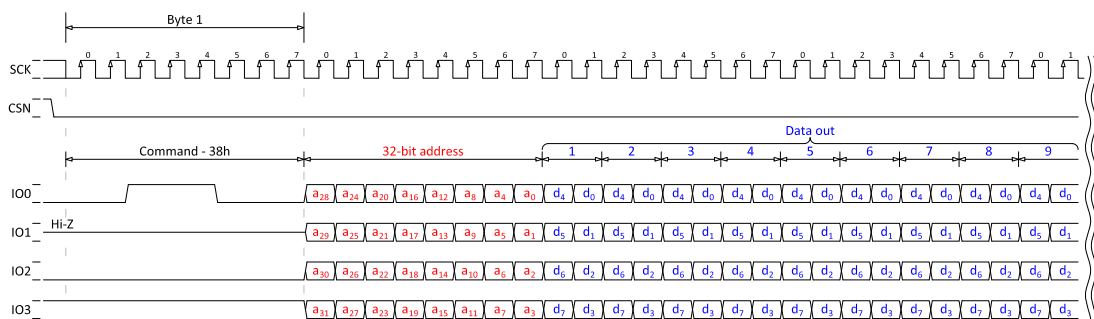


Figure 134: 32-bit PP4IO (quad page program input/output), SPI MODE = MODE0

## 7.1.26.11 Registers

| Base address | Domain      | Peripheral | Instance  | Secure mapping | DMA security | Description                                        | Configuration                                  |
|--------------|-------------|------------|-----------|----------------|--------------|----------------------------------------------------|------------------------------------------------|
| 0x5002B000   | APPLICATION | QSPI       | QSPI : S  | US             | SA           | External memory (quad serial peripheral) interface | Supports 192 MHz and 96 MHz PCLK192M frequency |
| 0x4002B000   |             |            | QSPI : NS |                |              |                                                    |                                                |

Table 119: Instances

| Register             | Offset | Security | Description                                                                            |
|----------------------|--------|----------|----------------------------------------------------------------------------------------|
| TASKS_ACTIVATE       | 0x000  |          | Activate QSPI interface                                                                |
| TASKS_READSTART      | 0x004  |          | Start transfer from external flash memory to internal RAM                              |
| TASKS_WRITESTART     | 0x008  |          | Start transfer from internal RAM to external flash memory                              |
| TASKS_ERASESTART     | 0x00C  |          | Start external flash memory erase operation                                            |
| TASKS_DEACTIVATE     | 0x010  |          | Deactivate QSPI interface                                                              |
| SUBSCRIBE_ACTIVATE   | 0x080  |          | Subscribe configuration for task <a href="#">ACTIVATE</a>                              |
| SUBSCRIBE_READSTART  | 0x084  |          | Subscribe configuration for task <a href="#">READSTART</a>                             |
| SUBSCRIBE_WRITESTART | 0x088  |          | Subscribe configuration for task <a href="#">WRITESTART</a>                            |
| SUBSCRIBE_ERASESTART | 0x08C  |          | Subscribe configuration for task <a href="#">ERASESTART</a>                            |
| SUBSCRIBE_DEACTIVATE | 0x090  |          | Subscribe configuration for task <a href="#">DEACTIVATE</a>                            |
| EVENTS_READY         | 0x100  |          | QSPI peripheral is ready. This event will be generated as a response to any QSPI task. |
| PUBLISH_READY        | 0x180  |          | Publish configuration for event <a href="#">READY</a>                                  |
| INTEN                | 0x300  |          | Enable or disable interrupt                                                            |
| INTENSET             | 0x304  |          | Enable interrupt                                                                       |
| INTENCLR             | 0x308  |          | Disable interrupt                                                                      |
| ENABLE               | 0x500  |          | Enable QSPI peripheral and acquire the pins selected in PSELn registers                |
| READ.SRC             | 0x504  |          | Flash memory source address                                                            |
| READ.DST             | 0x508  |          | RAM destination address                                                                |
| READ.CNT             | 0x50C  |          | Read transfer length                                                                   |
| WRITE.DST            | 0x510  |          | Flash destination address                                                              |
| WRITE.SRC            | 0x514  |          | RAM source address                                                                     |
| WRITE.CNT            | 0x518  |          | Write transfer length                                                                  |
| ERASE.PTR            | 0x51C  |          | Start address of flash block to be erased                                              |
| ERASE.LEN            | 0x520  |          | Size of block to be erased.                                                            |
| PSEL.SCK             | 0x524  |          | Pin select for serial clock SCK                                                        |
| PSEL.CSN             | 0x528  |          | Pin select for chip select signal CSN.                                                 |
| PSEL.IO0             | 0x530  |          | Pin select for serial data MOSI/IO0.                                                   |
| PSEL.IO1             | 0x534  |          | Pin select for serial data MISO/IO1.                                                   |
| PSEL.IO2             | 0x538  |          | Pin select for serial data IO2.                                                        |
| PSEL.IO3             | 0x53C  |          | Pin select for serial data IO3.                                                        |
| XIPOFFSET            | 0x540  |          | Address offset into the external memory for Execute in Place operation.                |
| IFCONFIG0            | 0x544  |          | Interface configuration.                                                               |
| XIPEN                | 0x54C  |          | Enable Execute in Place operation.                                                     |
| XIP_ENC.KEY0         | 0x560  |          | Bits 31:0 of XIP AES KEY                                                               |
| XIP_ENC.KEY1         | 0x564  |          | Bits 63:32 of XIP AES KEY                                                              |
| XIP_ENC.KEY2         | 0x568  |          | Bits 95:64 of XIP AES KEY                                                              |
| XIP_ENC.KEY3         | 0x56C  |          | Bits 127:96 of XIP AES KEY                                                             |
| XIP_ENC.NONCE0       | 0x570  |          | Bits 31:0 of XIP NONCE                                                                 |
| XIP_ENC.NONCE1       | 0x574  |          | Bits 63:32 of XIP NONCE                                                                |
| XIP_ENC.NONCE2       | 0x578  |          | Bits 95:64 of XIP NONCE                                                                |
| XIP_ENC.ENABLE       | 0x57C  |          | Enable stream cipher for XIP                                                           |
| DMA_ENC.KEY0         | 0x580  |          | Bits 31:0 of DMA AES KEY                                                               |
| DMA_ENC.KEY1         | 0x584  |          | Bits 63:32 of DMA AES KEY                                                              |

| Register       | Offset | Security | Description                                                         |
|----------------|--------|----------|---------------------------------------------------------------------|
| DMA_ENC.KEY2   | 0x588  |          | Bits 95:64 of DMA AES KEY                                           |
| DMA_ENC.KEY3   | 0x58C  |          | Bits 127:96 of DMA AES KEY                                          |
| DMA_ENC.NONCE0 | 0x590  |          | Bits 31:0 of DMA NONCE                                              |
| DMA_ENC.NONCE1 | 0x594  |          | Bits 63:32 of DMA NONCE                                             |
| DMA_ENC.NONCE2 | 0x598  |          | Bits 95:64 of DMA NONCE                                             |
| DMA_ENC.ENABLE | 0x59C  |          | Enable stream cipher for XIP                                        |
| IFCONFIG1      | 0x600  |          | Interface configuration.                                            |
| STATUS         | 0x604  |          | Status register.                                                    |
| DPMDUR         | 0x614  |          | Set the duration required to enter/exit deep power-down mode (DPM). |
| ADDRCONF       | 0x624  |          | Extended address configuration.                                     |
| CINSTRCONF     | 0x634  |          | Custom instruction configuration register.                          |
| CINSTRDAT0     | 0x638  |          | Custom instruction data register 0.                                 |
| CINSTRDAT1     | 0x63C  |          | Custom instruction data register 1.                                 |
| IFTIMING       | 0x640  |          | SPI interface timing.                                               |

Table 120: Register overview

### 7.1.26.11.1 TASKS\_ACTIVATE

Address offset: 0x000

Activate QSPI interface

Triggering this task activates the external flash memory interface and initiates communication with the external memory. The READY event is generated when the activation has been completed.

| Bit number       |            | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                                                                                                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|---------------------------------------------------------------------------------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |            | A                                                                                     |       |                                                                                                                                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |       |                                                                                                                                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID                                                                              | Value | Description                                                                                                                                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W          | TASKS_ACTIVATE                                                                        |       | Activate QSPI interface                                                                                                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |                                                                                       |       | Triggering this task activates the external flash memory interface and initiates communication with the external memory. The READY event is generated when the activation has been completed. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Trigger                                                                               | 1     | Trigger task                                                                                                                                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.26.11.2 TASKS\_READSTART

Address offset: 0x004

Start transfer from external flash memory to internal RAM

Start transfer from external flash memory to internal RAM. The READY event will be generated when transfer is complete.

| Bit number       |            |                 | 31    | 30                                                                                                                      | 29          | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |  |
|------------------|------------|-----------------|-------|-------------------------------------------------------------------------------------------------------------------------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|--|
| ID               |            |                 |       |                                                                                                                         |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |  |  |  |
| Reset 0x00000000 |            |                 | 0     | 0                                                                                                                       | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |  |  |  |
| ID               | Acce Field | Value ID        | Value |                                                                                                                         | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
| A                | W          | TASKS_READSTART |       | Start transfer from external flash memory to internal RAM                                                               |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            |                 |       | Start transfer from external flash memory to internal RAM. The READY event will be generated when transfer is complete. |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            | Trigger         | 1     | Trigger task                                                                                                            |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |

### 7.1.26.11.3 TASKS\_WRITESTART

Address offset: 0x008

Start transfer from internal RAM to external flash memory

Start transfer from internal RAM to external flash memory. The READY event will be generated when transfer is complete.

|                  |      |                  |          |         |       |                                                              |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------|------------------|----------|---------|-------|--------------------------------------------------------------|-------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |      |                  |          |         |       |                                                              |             |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |      |                  |          |         |       |                                                              |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |   |
| Reset 0x00000000 |      |                  |          |         |       |                                                              |             |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce | Field            | Value ID |         | Value |                                                              | Description |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | W    | TASKS_WRITESTART |          |         |       | Start transfer from internal RAM to external flash memory    |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |                  |          |         |       | Start transfer from internal RAM to external flash memory.   |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |                  |          |         |       | The READY event will be generated when transfer is complete. |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |                  |          | Trigger | 1     | Trigger task                                                 |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.26.11.4 TASKS\_ERASESTART

Address offset: 0x00C

Start external flash memory erase operation

Start external flash memory erase operation. The READY event will be generated when the erase operation has been started. Note, generation of the READY event does not imply that the erase operation is completed.

|                  |      |                  |          |                                                                                       |                                                                                                                                                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|------------------|----------|---------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |                  |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                                                                                                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |                  |          | A                                                                                     |                                                                                                                                                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |                  |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                                                                                                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field            | Value ID | Value                                                                                 | Description                                                                                                                                                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W    | TASKS_ERASESTART |          |                                                                                       | Start external flash memory erase operation                                                                                                                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                  |          |                                                                                       | Start external flash memory erase operation. The READY event will be generated when the erase operation has been started. Note, generation of the READY event does not imply that the erase operation is completed. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                  | Trigger  | 1                                                                                     | Trigger task                                                                                                                                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.26.11.5 TASKS\_DEACTIVATE

Address offset: 0x010

Deactivate QSPI interface



Start transfer from internal RAM to external flash memory. The READY event will be generated when transfer is complete.

|                  |            |          |                                                                                       |  |  |  |                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|--|--|--|-------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|---|--|--|--|---|--|--|--|---|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |
| ID               |            |          | B                                                                                     |  |  |  |                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A |  |  |  | A |  |  |  | A |  |  |  | A |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |  |  |  |                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 |  |  |  | Description                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                              |  |  |  | Channel that task <b>WRITESTART</b> will subscribe to |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |
| B                | RW EN      |          |                                                                                       |  |  |  |                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |
|                  |            | Disabled | 0                                                                                     |  |  |  | Disable subscription                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |
|                  |            | Enabled  | 1                                                                                     |  |  |  | Enable subscription                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |

#### 7.1.26.11.9 SUBSCRIBE\_ERASESTART

Address offset: 0x08C

Subscribe configuration for task **ERASESTART**

Start external flash memory erase operation. The READY event will be generated when the erase operation has been started. Note, generation of the READY event does not imply that the erase operation is completed.

|                  |            |          |                                                                                       |                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|----------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |          | B                                                                                     |                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                              | Channel that task <a href="#">ERASESTART</a> will subscribe to |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |                                                                                       |                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Disable subscription                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Enable subscription                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

#### 7.1.26.11.10 SUBSCRIBE\_DEACTIVATE

Address offset: 0x090

Subscribe configuration for task **DEACTIVATE**

Deactivate QSPI interface. This task might be needed to optimize current consumption in case there are any added current consumption when QSPI interface is activated, but idle.

|                  |            |          |                                                                                       |                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|-------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |          | B                                                                                     |                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                              | Channel that task <b>DEACTIVATE</b> will subscribe to |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |                                                                                       |                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Disable subscription                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Enable subscription                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

#### 7.1.26.11.11 EVENTS\_READY

Address offset: 0x100

QSPI peripheral is ready. This event will be generated as a response to any QSPI task.

|                  |            |  |              |  |       |  |                                                                                        |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|--------------|--|-------|--|----------------------------------------------------------------------------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |              |  |       |  |                                                                                        |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |  |              |  |       |  |                                                                                        |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |
| Reset 0x00000000 |            |  |              |  |       |  |                                                                                        |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID     |  | Value |  | Description                                                                            |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         |  | EVENTS_READY |  |       |  | QSPI peripheral is ready. This event will be generated as a response to any QSPI task. |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | NotGenerated |  | 0     |  | Event not generated                                                                    |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Generated    |  | 1     |  | Event generated                                                                        |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.26.11.12 PUBLISH\_READY

Address offset: 0x180

Publish configuration for event [READY](#)

|                  |            |          |          |          |       |                                                  |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|----------|-------|--------------------------------------------------|-------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          |          |       |                                                  |             |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |
| ID               |            |          |          |          |       |                                                  |             |  |  | B  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  |    |    |    |   |   |   |   |   |   | A | A | A | A | A | A | A |   |
| Reset 0x00000000 |            |          |          |          |       |                                                  |             |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |          | Value ID |          | Value |                                                  | Description |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | CHIDX    |          | [255..0] |       | Channel that event <b>READY</b> will publish to. |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW         | EN       |          |          |       |                                                  |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled |          | 0        |       | Disable publishing                               |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  |          | 1        |       | Enable publishing                                |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.26.11.13 INTEN

Address offset: 0x300

Enable or disable interrupt

|                  |            |          |       |                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|------------------|------------|----------|-------|-------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|---|
| Bit number       |            |          |       | 31                                                          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |   |
| ID               |            |          |       |                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | A |
| Reset 0x00000000 |            |          |       | 0                                                           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |   |
| ID               | Acce Field | Value ID | Value | Description                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
| A                | RW         | READY    |       | Enable or disable interrupt for event <a href="#">READY</a> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | Disabled | 0     | Disable                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | Enabled  | 1     | Enable                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |

### 7.1.26.11.14 INTENSET

Address offset: 0x304

Enable interrupt

|                  |            |          |       |                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|------------------|------------|----------|-------|---------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|---|
| Bit number       |            |          |       | 31                                                            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |   |
| ID               |            |          |       |                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | A |
| Reset 0x00000000 |            |          |       | 0                                                             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |   |
| ID               | Acce Field | Value ID | Value | Description                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
| A                | RW         | READY    |       | Write '1' to enable interrupt for event <a href="#">READY</a> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | Set      | 1     | Enable                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | Disabled | 0     | Read: Disabled                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | Enabled  | 1     | Read: Enabled                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |

### 7.1.26.11.15 INTENCLR

Address offset: 0x308

Disable interrupt

|                  |            |          |                                                                                       |                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|-------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          | A                                                                                     |                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                   |                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW READY   |          |                                                                                       | Write '1' to disable interrupt for event <span>READY</span> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Clear    | 1                                                                                     | Disable                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Read: Disabled                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Read: Enabled                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.26.11.16 ENABLE

Address offset: 0x500

Enable QSPI peripheral and acquire the pins selected in PSELn registers

|                  |            |          |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | ENABLE   |       | Enable or disable QSPI                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0     | Disable QSPI                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1     | Enable QSPI                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.26.11.17 READ.SRC

Address offset: 0x504

Flash memory source address

|                  |            |          |                                                                                       |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|-------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A                   |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                   |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 |  |  |  |  |  |  |  | Description |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW SRC     |          | Word-aligned flash memory source address.                                             |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.26.11.18 READ.DST

Address offset: 0x508

RAM destination address

|                  |            |          |                                                                                       |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|--|--|--|-------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A                   |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 |  |  |  | Description |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW DST     |          | Word-aligned RAM destination address.                                                 |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |



### 7.1.26.11.19 READ.CNT

Address offset: 0x50C

Read transfer length

|                  |      |       |       |    |       |    |                                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------|-------|-------|----|-------|----|------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |      |       |       | 31 | 30    | 29 | 28                                                                                 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |      |       |       |    |       |    |                                                                                    |    |    |    |    |    |    |    |    |    |    |    |    | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |      |       |       | 0  | 0     | 0  | 0                                                                                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |
| ID               | Acce | Field | Value | ID | Value |    | Description                                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW   | CNT   |       |    |       |    | Read transfer length in number of bytes. The length must be a multiple of 4 bytes. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.26.11.20 WRITE.DST

Address offset: 0x510

Flash destination address

|                  |            |  |          |       |    |    |    |                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|-------|----|----|----|-----------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31    | 30 | 29 | 28 | 27                                      | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |  |          | A     | A  | A  | A  | A                                       | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |          | 0     | 0  | 0  | 0  | 0                                       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID | Value |    |    |    | Description                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW DST     |  |          |       |    |    |    | Word-aligned flash destination address. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.26.11.21 WRITE.SRC

Address offset: 0x514

RAM source address

|                  |            |  |  |          |  |  |                                  |  |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|--|----------|--|--|----------------------------------|--|----|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |  |          |  |  |                                  |  | 31 | 30          | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |  |  |          |  |  |                                  |  | A  | A           | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A | A |   |
| Reset 0x00000000 |            |  |  |          |  |  |                                  |  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  |  | Value ID |  |  | Value                            |  |    | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW SRC     |  |  |          |  |  | Word-aligned RAM source address. |  |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.26.11.22 WRITE.CNT

Address offset: 0x518

Write transfer length

|                  |            |          |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          |       | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | CNT      |       | Write transfer length in number of bytes. The length must be a multiple of 4 bytes.   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.26.11.23 ERASE.PTR

Address offset: 0x51C

Start address of flash block to be erased

|                  |            |  |          |       |    |    |    |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|-------|----|----|----|---------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31    | 30 | 29 | 28 | 27                                                | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |  |          | A     | A  | A  | A  | A                                                 | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |          | 0     | 0  | 0  | 0  | 0                                                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID | Value |    |    |    | Description                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW PTR     |  |          |       |    |    |    | Word-aligned start address of block to be erased. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.26.11.24 ERASE.LEN

Address offset: 0x520

Size of block to be erased.

|                  |      |       |       |    |       |                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|------------------|------|-------|-------|----|-------|----------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|
| Bit number       |      |       |       | 31 | 30    | 29                                     | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |
| ID               |      |       |       | A  |       |                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |  |  |
| Reset 0x00000000 |      |       |       | 0  | 0     | 0                                      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |
| ID               | Acce | Field | Value | ID | Value | Description                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
| A                | RW   | LEN   |       |    | LEN   |                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |       | 4KB   |    | 0     | Erase 4 kB block (flash command 0x20)  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |       | 64KB  |    | 1     | Erase 64 kB block (flash command 0xD8) |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |       | All   |    | 2     | Erase all (flash command 0xC7)         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |

### 7.1.26.11.25 PSEL.SCK

Address offset: 0x524

Pin select for serial clock SCK

|                  |            |              |         |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------------|---------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |              |         | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |              |         | C           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | B |   |   |   | A | A | A | A | A |
| Reset 0xFFFFFFFF |            |              |         | 1           | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |   |
| ID               | Acce Field | Value ID     | Value   | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | PIN          | [0..31] | Pin number  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW         | PORT         | [0..1]  | Port number |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| C                | RW         | CONNECT      |         | Connection  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disconnected | 1       | Disconnect  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Connected    | 0       | Connect     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.26.11.26 PSEL.CSN

Address offset: 0x528

Pin select for chip select signal CSN.

|                  |            |              |         |    |    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |   |   |   |   |   |
|------------------|------------|--------------|---------|----|----|----|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|--|---|---|---|---|---|
| Bit number       |            |              | 31      | 30 | 29 | 28 | 27          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |   |   |   |   |   |
| ID               |            |              | C       |    |    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | B |   |   |   |   |   |   |   |  |  |  |  | A | A | A | A | A |
| Reset 0xFFFFFFFF |            |              | 1       |    |    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |   |   |   |   |   |
| ID               | Acce Field | Value ID     | Value   |    |    |    | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |   |   |   |   |   |
| A                | RW         | PIN          | [0..31] |    |    |    | Pin number  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |   |   |   |   |   |
| B                | RW         | PORT         | [0..1]  |    |    |    | Port number |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |   |   |   |   |   |
| C                | RW         | CONNECT      |         |    |    |    | Connection  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |   |   |   |   |   |
|                  |            | Disconnected | 1       |    |    |    | Disconnect  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |   |   |   |   |   |
|                  |            | Connected    | 0       |    |    |    | Connect     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |   |   |   |   |   |

### 7.1.26.11.27 PSEL.IO0

Address offset: 0x530

Pin select for serial data MOSI/IO0.

|                  |  |  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               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| Bit number       |  |  | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         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| ID               |  |  | C                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             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| Reset 0xFFFFFFFF |  |  | 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 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### 7.1.26.11.28 PSEL.IO1

Address offset: 0x534

Pin select for serial data MISO/IO1.

|                  |            |              |                                                                                       |            |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |   |  |   |  |
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| Bit number       |            |              | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |            |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |   |  |   |  |
| ID               |            |              | C                                                                                     |            |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | B |  |  |  | A |  | A |  | A |  | A |  |
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| ID               | Acce Field | Value ID     | Value                                                                                 |            | Description |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |   |  |   |  |
| A                | RW PIN     |              | [0..31]                                                                               |            | Pin number  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |   |  |   |  |
| B                | RW PORT    |              | [0..1]                                                                                |            | Port number |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |   |  |   |  |
| C                | RW CONNECT |              |                                                                                       |            | Connection  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |   |  |   |  |
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### 7.1.26.11.29 PSEL.IO2

Address offset: 0x538

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### 7.1.26.11.30 PSEL.IO3

Address offset: 0x53C

Pin select for serial data IO3.

|                  |      |              |         |                                                                         |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|------------------|------|--------------|---------|-------------------------------------------------------------------------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| Bit number       |      |              |         | 31                                                                      | 30          | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| ID               |      |              |         | C                                                                       |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
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| ID               | Acce | Field        | Value   | ID                                                                      | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| A                | RW   | PIN          | [0..31] |                                                                         | Pin number  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| B                | RW   | PORT         | [0..1]  |                                                                         | Port number |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| C                | RW   | CONNECT      |         |                                                                         | Connection  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
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|                  |      | Connected    | 0       |                                                                         | Connect     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

### 7.1.26.11.31 XIPOFFSET

Address offset: 0x540

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#### 7.1.26.11.32 IFCONFIG0

Address offset: 0x544

### Interface configuration.

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| Bit number       |      |           | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                |       |                                                             |  |                  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| A                | RW   | READOC    |                                                                                       |                                                |       | Configure number of data lines and opcode used for reading. |  |                  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | FASTREAD  | 0                                                                                     | Single data line SPI. FAST_READ (opcode 0x0B). |       |                                                             |  |                  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | READ2O    | 1                                                                                     | Dual data line SPI. READ2O (opcode 0x3B).      |       |                                                             |  |                  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | READ2IO   | 2                                                                                     | Dual data line SPI. READ2IO (opcode 0xBB).     |       |                                                             |  |                  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | READ4O    | 3                                                                                     | Quad data line SPI. READ4O (opcode 0x6B).      |       |                                                             |  |                  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | READ4IO   | 4                                                                                     | Quad data line SPI. READ4IO (opcode 0xEB).     |       |                                                             |  |                  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW   | WRITEOC   |                                                                                       |                                                |       | Configure number of data lines and opcode used for writing. |  |                  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | PP        | 0                                                                                     | Single data line SPI. PP (opcode 0x02).        |       |                                                             |  |                  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | PP2O      | 1                                                                                     | Dual data line SPI. PP2O (opcode 0xA2).        |       |                                                             |  |                  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | PP4O      | 2                                                                                     | Quad data line SPI. PP4O (opcode 0x32).        |       |                                                             |  |                  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | PP4IO     | 3                                                                                     | Quad data line SPI. PP4IO (opcode 0x38).       |       |                                                             |  |                  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | C         | RW                                                                                    | ADDRMODE                                       |       |                                                             |  | Addressing mode. |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 24BIT            | 0    |           |                                                                                       | 24-bit addressing.                             |       |                                                             |  |                  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 32BIT            | 1    |           |                                                                                       | 32-bit addressing.                             |       |                                                             |  |                  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| D                | RW   | DPMENABLE |                                                                                       |                                                |       | Enable deep power-down mode (DPM) feature.                  |  |                  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Disable   | 0                                                                                     | Disable DPM feature.                           |       |                                                             |  |                  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Enable    | 1                                                                                     | Enable DPM feature.                            |       |                                                             |  |                  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| G                | RW   | PPSIZE    |                                                                                       |                                                |       | Page size for commands PP, PP2O, PP4O and PP4IO.            |  |                  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | 256Bytes  | 0                                                                                     | 256 bytes.                                     |       |                                                             |  |                  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

|                  |            |          |                                                                             |    |    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|-----------------------------------------------------------------------------|----|----|----|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          | 31                                                                          | 30 | 29 | 28 | 27          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |
| ID               |            |          |                                                                             |    |    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | G  |    |   |   |   |   |   |   | D | C | B | B | B | A | A | A | A |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |    |    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field | Value ID | Value                                                                       |    |    |    | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | 512Bytes | 1                                                                           |    |    |    | 512 bytes.  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.26.11.33 XIPEN

Address offset: 0x54C

Enable Execute in Place operation.

|                  |      |       |         |    |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |                                                                                                                                                                                               |
|------------------|------|-------|---------|----|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit number       |      |       |         | 31 | 30    | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |                                                                                                                                                                                               |
| ID               |      |       |         |    |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |                                                                                                                                                                                               |
| Reset 0x00000001 |      |       |         | 0  | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |                                                                                                                                                                                               |
| ID               | Acce | Field | Value   | ID | Value |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   | Description                                                                                                                                                                                   |
| A                | RW   | XIPEN |         |    |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   | Enable XIP AHB Slave interface and access to XIP memory range                                                                                                                                 |
|                  |      |       |         |    |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   | When disabled, access to external memory is only available through EasyDMA and custom instructions. Access to disabled XIP interface will cause a Bus Error, and the value read is all zeros. |
|                  |      |       | Disable | 0  |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   | Disable XIP interface                                                                                                                                                                         |
|                  |      |       | Enable  | 1  |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   | Enable XIP interface                                                                                                                                                                          |

### 7.1.26.11.34 XIP\_ENC.KEY0

Address offset: 0x560

Bits 31:0 of XIP AES KEY

|                  |            |  |  |  |          |  |  |  |       |    |    |    |                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|--|--|----------|--|--|--|-------|----|----|----|--------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |  |  |          |  |  |  |       | 31 | 30 | 29 | 28                       | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |  |  |  |          |  |  |  |       | A  | A  | A  | A                        | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A | A | A |   |
| Reset 0x00000000 |            |  |  |  |          |  |  |  |       | 0  | 0  | 0  | 0                        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  |  |  | Value ID |  |  |  | Value |    |    |    | Description              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | W KEY0     |  |  |  |          |  |  |  |       |    |    |    | Bits 31:0 of XIP AES KEY |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.26.11.35 XIP\_ENC.KEY1

Address offset: 0x564

Bits 63:32 of XIP AES KEY

|                  |            |      |          |       |    |    |    |                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|------|----------|-------|----|----|----|---------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |      |          | 31    | 30 | 29 | 28 | 27                        | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |      |          | A     | A  | A  | A  | A                         | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |      |          | 0     | 0  | 0  | 0  | 0                         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |      | Value ID | Value |    |    |    | Description               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | W          | KEY1 |          |       |    |    |    | Bits 63:32 of XIP AES KEY |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.26.11.36 XIP\_ENC.KEY2

Address offset: 0x568

Bits 95:64 of XIP AES KEY

|                  |            |      |          |       |    |    |    |                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|------|----------|-------|----|----|----|---------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |      |          | 31    | 30 | 29 | 28 | 27                        | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |      |          | A     | A  | A  | A  | A                         | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |      |          | 0     | 0  | 0  | 0  | 0                         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |      | Value ID | Value |    |    |    | Description               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | W          | KEY2 |          |       |    |    |    | Bits 95:64 of XIP AES KEY |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.26.11.37 XIP\_ENC.KEY3

Address offset: 0x56C

Bits 127:96 of XIP AES KEY

|                  |            |      |          |       |    |    |    |                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|------|----------|-------|----|----|----|----------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |      |          | 31    | 30 | 29 | 28 | 27                         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |      |          | A     | A  | A  | A  | A                          | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |      |          | 0     | 0  | 0  | 0  | 0                          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |      | Value ID | Value |    |    |    | Description                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | W          | KEY3 |          |       |    |    |    | Bits 127:96 of XIP AES KEY |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.26.11.38 XIP\_ENC.NONCE0

Address offset: 0x570

Bits 31:0 of XIP NONCE

|                  |            |        |          |       |    |    |    |                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------|----------|-------|----|----|----|------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |        |          | 31    | 30 | 29 | 28 | 27                     | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |        |          | A     | A  | A  | A  | A                      | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |        |          | 0     | 0  | 0  | 0  | 0                      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |        | Value ID | Value |    |    |    | Description            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | W          | NONCE0 |          |       |    |    |    | Bits 31:0 of XIP NONCE |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.26.11.39 XIP\_ENC.NONCE1

Address offset: 0x574

Bits 63:32 of XIP NONCE

|                  |            |        |          |       |    |                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------|----------|-------|----|-------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |        |          | 31    | 30 | 29                      | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |        |          | A     | A  | A                       | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |        |          | 0     | 0  | 0                       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |        | Value ID | Value |    | Description             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | W          | NONCE1 |          |       |    | Bits 63:32 of XIP NONCE |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.26.11.40 XIP\_ENC.NONCE2

Address offset: 0x578

Bits 95:64 of XIP NONCE

|                  |            |        |          |                         |    |    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------|----------|-------------------------|----|----|----|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |        |          | 31                      | 30 | 29 | 28 | 27          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |        |          | A                       | A  | A  | A  | A           | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |        |          | 0                       | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |        | Value ID | Value                   |    |    |    | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | W          | NONCE2 |          | Bits 95:64 of XIP NONCE |    |    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.26.11.41 XIP\_ENC.ENABLE

Address offset: 0x57C

Enable stream cipher for XIP

|                  |      |        |          |                                                                                       |       |                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|--------|----------|---------------------------------------------------------------------------------------|-------|-----------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |        |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |        |          | A                                                                                     |       |                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |        |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |       |                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field  | Value    | ID                                                                                    | Value | Description                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW   | ENABLE |          |                                                                                       |       | Enable or disable stream cipher for XIP |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |        | Disabled |                                                                                       | 0     | Disable stream cipher for QSPI XIP      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |        | Enabled  |                                                                                       | 1     | Enable stream cipher for QSPI XIP       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.26.11.42 DMA\_ENC.KEY0

Address offset: 0x580

Bits 31:0 of DMA AES KEY

|                  |            |      |          |                                                                                       |  |  |  |                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|------|----------|---------------------------------------------------------------------------------------|--|--|--|--------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |      |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |      |          | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A                   |  |  |  |                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |      |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |  |  |  |                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field |      | Value ID | Value                                                                                 |  |  |  | Description              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W          | KEY0 |          |                                                                                       |  |  |  | Bits 31:0 of DMA AES KEY |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.26.11.43 DMA\_ENC.KEY1

Address offset: 0x584

Bits 63:32 of DMA AES KEY

| Bit number       |      |       |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|-------|----------|---------------------------------------------------------------------------------------|--|--|--|---------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |      |       |          | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A                   |  |  |  |                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |       |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |  |  |  |                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field | Value ID | Value                                                                                 |  |  |  | Description               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W    | KEY1  |          |                                                                                       |  |  |  | Bits 63:32 of DMA AES KEY |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.26.11.44 DMA\_ENC.KEY2

Address offset: 0x588

Bits 95:64 of DMA AES KEY

|                  |            |      |          |                                                                                       |  |  |  |                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|------|----------|---------------------------------------------------------------------------------------|--|--|--|---------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |      |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |      |          | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A                   |  |  |  |                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |      |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |  |  |  |                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field |      | Value ID | Value                                                                                 |  |  |  | Description               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W          | KEY2 |          |                                                                                       |  |  |  | Bits 95:64 of DMA AES KEY |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.26.11.45 DMA\_ENC.KEY3

Address offset: 0x58C





|                  |            |          |                                                                                       |                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|-----------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          | A                                                                                     |                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | ENABLE   |                                                                                       | Enable or disable stream cipher for XIP |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Disable stream cipher for QSPI XIP      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Enable stream cipher for QSPI XIP       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.26.11.50 IFCONFIG1

Address offset: 0x600

Interface configuration.

|                  |      |          |                                                                                       |  |          |  |                                                                                                                                              |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|----------|---------------------------------------------------------------------------------------|--|----------|--|----------------------------------------------------------------------------------------------------------------------------------------------|--|-----------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |          |  |                                                                                                                                              |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |          | G G G G                                                                               |  |          |  | E D                                                                                                                                          |  | A A A A A A A A |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00040480 |      |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 1 0 0 1 0 0 0 0 0 0                       |  |          |  |                                                                                                                                              |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field    | Value ID                                                                              |  | Value    |  | Description                                                                                                                                  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW   | SCKDELAY |                                                                                       |  | [0..255] |  | Minimum amount of time that the CSN pin must stay high before it can go low again. Value is specified in number of 16 MHz periods (62.5 ns). |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| D                | RW   | DPMEN    |                                                                                       |  |          |  | Enter/exit deep power-down mode (DPM) for external flash memory.                                                                             |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |          | Exit                                                                                  |  | 0        |  | Exit DPM.                                                                                                                                    |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |          | Enter                                                                                 |  | 1        |  | Enter DPM.                                                                                                                                   |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| E                | RW   | SPIMODE  |                                                                                       |  |          |  | Select SPI mode.                                                                                                                             |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |          | MODE0                                                                                 |  | 0        |  | Mode 0: Data are captured on the clock rising edge and data is output on a falling edge. Base level of clock is 0 (CPOL=0, CPHA=0).          |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |          | MODE3                                                                                 |  | 1        |  | Mode 3: Data are captured on the clock falling edge and data is output on a rising edge. Base level of clock is 1 (CPOL=1, CPHA=1).          |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| G                | RW   | SCKFREQ  |                                                                                       |  | [0..15]  |  | SCK frequency is given as 96 MHz / (SCKFREQ + 1).                                                                                            |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.26.11.51 STATUS

Address offset: 0x604

Status register.

| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----|--|--|--|--|--|--|--|
| ID               |            |          | F F F F F F F F                                                                       |                                                                                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | D C |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                                                                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |
| C                | R          | DPM      |                                                                                       | Deep power-down mode (DPM) status of external flash.                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | External flash is not in DPM.                                                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | External flash is in DPM.                                                                                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |
| D                | R          | READY    |                                                                                       | Ready status.                                                                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |
|                  |            | READY    | 1                                                                                     | QSPI peripheral is ready. It is allowed to trigger new tasks, writing custom instructions or enter/exit DPM.                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |
|                  |            | BUSY     | 0                                                                                     | QSPI peripheral is busy. It is not allowed to trigger any new tasks, writing custom instructions or enter/exit DPM.                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |
| F                | R          | SREG     |                                                                                       | Value of external flash device Status Register. When the external flash has two bytes status register this field includes the value of the low byte. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |  |  |  |

### 7.1.26.11.52 DPMDUR

Address offset: 0x614

Set the duration required to enter/exit deep power-down mode (DPM).

|                  |            |          |                                                                                       |                                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          | B B B B B B B B B B B B B B B B A A A A A A A A A A A A A A A A A                     |                                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0xFFFFFFFF |            |          | 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1                       |                                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW ENTER   |          | [0..0xFFFF]                                                                           | Duration needed by external flash to enter DPM. Duration is given as ENTER * 256 * 62.5 ns. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW EXIT    |          | [0..0xFFFF]                                                                           | Duration needed by external flash to exit DPM. Duration is given as EXIT * 256 * 62.5 ns.   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.26.11.53 ADDRCONF

Address offset: 0x624

Extended address configuration.

| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|----------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |            |          | F E D D C C C C C C C C C C B B B B B B A A A A A A A A A A                           |                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x000000B7 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 1 0 1 1 1   |                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW OPCODE  |          | [0xFF..0]                                                                             | Opcode that enters the 32-bit addressing mode.           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW BYTE0   |          | [0xFF..0]                                                                             | Byte 0 following opcode.                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW BYTE1   |          | [0xFF..0]                                                                             | Byte 1 following byte 0.                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| D                | RW MODE    |          |                                                                                       | Extended addressing mode.                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | NoInstr  | 0                                                                                     | Do not send any instruction.                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Opcode   | 1                                                                                     | Send opcode.                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | OpByte0  | 2                                                                                     | Send opcode, byte0.                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | All      | 3                                                                                     | Send opcode, byte0, byte1.                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| E                | RW WIPWAIT |          |                                                                                       | Wait for write complete before sending command.          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disable  | 0                                                                                     | No wait.                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enable   | 1                                                                                     | Wait.                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| F                | RW WREN    |          |                                                                                       | Send WREN (write enable opcode 0x06) before instruction. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disable  | 0                                                                                     | Do not send WREN.                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

|                  |            |          |       |                                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|-------|---------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |       | 31                                                                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |          |       | F E D D C C C C C C C C B B B B B B B A A A A A A A A                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Reset 0x000000B7 |            |          |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 1 0 1 1 1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field | Value ID | Value | Description                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enable   | 1     | Send WREN.                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.26.11.54 CINSTRCONF

Address offset: 0x634

Custom instruction configuration register.

A new custom instruction is sent every time this register is written. The READY event will be generated when the custom instruction has been sent.

| Bit number       |      |         |          | 31                                    | 30                                                                                                                  | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
|------------------|------|---------|----------|---------------------------------------|---------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| ID               |      |         |          | H G F E D C B B B B A A A A A A A A A |                                                                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| Reset 0x00002000 |      |         |          | 0                                     | 0                                                                                                                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |
| ID               | Acce | Field   | Value ID | Value                                 | Description                                                                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| A                | RW   | OPCODE  |          | [0..255]                              | Opcode of Custom instruction.                                                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| B                | RW   | LENGTH  |          |                                       | Length of custom instruction in number of bytes.                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |         | 1B       | 1                                     | Send opcode only.                                                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |         | 2B       | 2                                     | Send opcode, CINSTRDAT0.BYTE0.                                                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |         | 3B       | 3                                     | Send opcode, CINSTRDAT0.BYTE0 -> CINSTRDAT0.BYTE1.                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |         | 4B       | 4                                     | Send opcode, CINSTRDAT0.BYTE0 -> CINSTRDAT0.BYTE2.                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |         | 5B       | 5                                     | Send opcode, CINSTRDAT0.BYTE0 -> CINSTRDAT0.BYTE3.                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |         | 6B       | 6                                     | Send opcode, CINSTRDAT0.BYTE0 -> CINSTRDAT1.BYTE4.                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |         | 7B       | 7                                     | Send opcode, CINSTRDAT0.BYTE0 -> CINSTRDAT1.BYTE5.                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |         | 8B       | 8                                     | Send opcode, CINSTRDAT0.BYTE0 -> CINSTRDAT1.BYTE6.                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |         | 9B       | 9                                     | Send opcode, CINSTRDAT0.BYTE0 -> CINSTRDAT1.BYTE7.                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| C                | RW   | LIO2    |          | [0..1]                                | Level of the IO2 pin (if connected) during transmission of custom instruction.                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| D                | RW   | LIO3    |          | [0..1]                                | Level of the IO3 pin (if connected) during transmission of custom instruction.                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| E                | RW   | WIPWAIT |          |                                       | Wait for write complete before sending command.                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |         | Disable  | 0                                     | No wait.                                                                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |         | Enable   | 1                                     | Wait.                                                                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| F                | RW   | WREN    |          |                                       | Send WREN (write enable opcode 0x06) before instruction.                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |         | Disable  | 0                                     | Do not send WREN.                                                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |         | Enable   | 1                                     | Send WREN.                                                                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| G                | RW   | LFEN    |          |                                       | Enable long frame mode. When enabled, a custom instruction transaction has to be ended by writing the LFSTOP field. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |         | Disable  | 0                                     | Long frame mode disabled                                                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |         | Enable   | 1                                     | Long frame mode enabled                                                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| H                | RW   | LFSTOP  |          |                                       | Stop (finalize) long frame transaction                                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |         | Stop     | 1                                     | Stop                                                                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

### 7.1.26.11.55 CINSTRDAT0

Address offset: 0x638

Custom instruction data register 0.

| Bit number       |            |       |          |           |       |             |             |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
|------------------|------------|-------|----------|-----------|-------|-------------|-------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ID               |            |       |          |           |       |             |             |  |  | D  | D  | D  | D  | D  | D  | D  | D  | C  | C  | C  | C  | C  | C  | C  | B  | B  | B  | B  | B  | B  | B  | B | B | A | A | A | A | A | A | A | A | A | A |   |
| Reset 0x00000000 |            |       |          |           |       |             |             |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |       | Value ID |           | Value |             | Description |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | BYTE0 |          | [0..0xFF] |       | Data byte 0 |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW         | BYTE1 |          | [0..0xFF] |       | Data byte 1 |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| C                | RW         | BYTE2 |          | [0..0xFF] |       | Data byte 2 |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| D                | RW         | BYTE3 |          | [0..0xFF] |       | Data byte 3 |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.26.11.56 CINSTRDAT1

Address offset: 0x63C

Custom instruction data register 1.

| Bit number       |      |       |          |  |  |           |  |  |             | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
|------------------|------|-------|----------|--|--|-----------|--|--|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ID               |      |       |          |  |  |           |  |  |             | D  | D  | D  | D  | D  | D  | D  | D  | C  | C  | C  | C  | C  | C  | C  | B  | B  | B  | B  | B  | B  | B  | B | B | B | B | A | A | A | A | A | A | A | A |   |
| Reset 0x00000000 |      |       |          |  |  |           |  |  |             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce | Field | Value ID |  |  | Value     |  |  | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW   | BYTE4 |          |  |  | [0..0xFF] |  |  | Data byte 4 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW   | BYTE5 |          |  |  | [0..0xFF] |  |  | Data byte 5 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| C                | RW   | BYTE6 |          |  |  | [0..0xFF] |  |  | Data byte 6 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| D                | RW   | BYTE7 |          |  |  | [0..0xFF] |  |  | Data byte 7 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.26.11.57 IFTIMING

Address offset: 0x640

SPI interface timing.

|                  |            |          |                                                                                       |                                                                                                                                                                                                                                                                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                                                                                                                                                                                                                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          | C C C                                                                                 |                                                                                                                                                                                                                                                                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000200 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                   |                                                                                                                                                                                                                                                                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                                                                                                                                                                                                                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW RXDELAY |          | [7..0]                                                                                | Timing related to sampling of the input serial data. The value of RXDELAY specifies the number of 192 MHz cycles (5.208 ns) delay from the the rising edge of the SPI Clock (SCK) until the input serial data is sampled. As an example, if set to 0 the input serial data is sampled on the rising edge of SCK. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

## 7.1.26.12 Electrical specification

### 7.1.26.12.1 Timing specification

| Symbol                   | Description                                 | Min. | Typ. | Max. | Units |
|--------------------------|---------------------------------------------|------|------|------|-------|
| F <sub>QSPI,CLK</sub>    | SCK frequency                               | ..   | ..   | ..   | MHz   |
| DC <sub>QSPI,CLK</sub>   | SCK duty cycle                              | ..   | ..   | ..   | %     |
| F <sub>QSPI,XIP,16</sub> | XIP fetch frequency for 16 bit instructions | ..   | ..   | ..   | MHz   |
| F <sub>QSPI,XIP,32</sub> | XIP fetch frequency for 32 bit instructions | ..   | ..   | ..   | MHz   |

## 7.1.27 RADIO — 2.4 GHz radio

The 2.4 GHz radio transceiver is compatible with multiple radio standards such as 1 Mbps and 2 Mbps *Bluetooth* Low Energy modes, Long Range (125 kbps and 500 kbps) *Bluetooth* Low Energy modes, IEEE 802.15.4 250 kbps mode, as well as Nordic's proprietary 1 Mbps and 2 Mbps modes.

Listed here are main features for the RADIO:

- Multidomain 2.4 GHz radio transceiver
  - 1 Mbps and 2 Mbps *Bluetooth* Low Energy modes
  - Long Range (125 kbps and 500 kbps) *Bluetooth* Low Energy modes
  - Angle-of-arrival (AoA) and angle-of-departure (AoD) direction finding using *Bluetooth* Low Energy
  - IEEE 802.15.4 250 kbps mode
  - 1 Mbps and 2 Mbps Nordic proprietary modes
- Best in class link budget and low power operation
- Efficient data interface with EasyDMA support
- Automatic address filtering and pattern matching

EasyDMA, in combination with an automated packet assembler, packet disassembler, automated CRC generator and CRC checker, makes it easy to configure and use the RADIO. See the following figure for details.

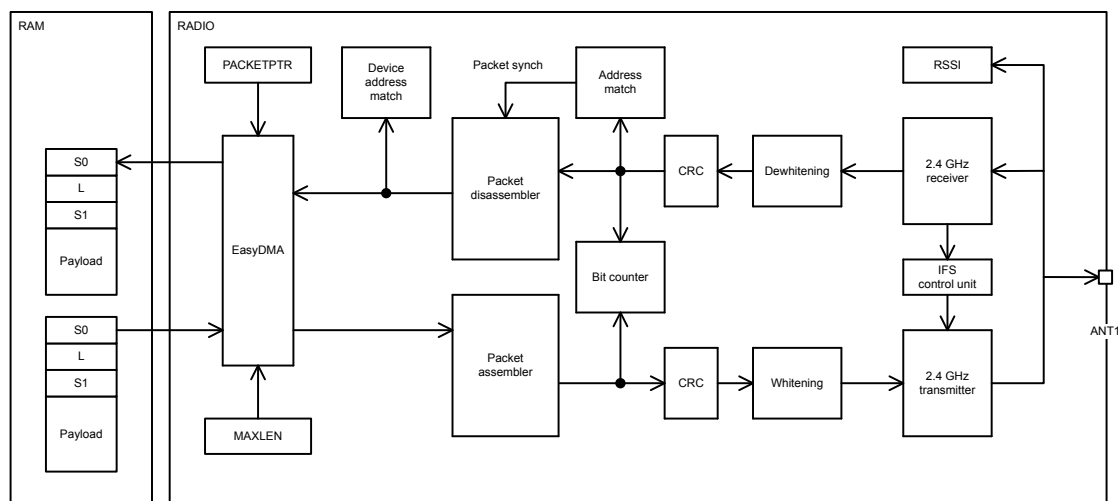


Figure 135: RADIO block diagram

The RADIO includes a device address match unit and an interframe spacing control unit that can be utilized to simplify address whitelisting and interframe spacing respectively in *Bluetooth* low energy and similar applications.

The RADIO also includes a received signal strength indicator (RSSI) and a bit counter. The bit counter generates events when a preconfigured number of bits are sent or received by the RADIO.

### 7.1.27.1 Packet configuration

A RADIO packet contains the fields PREAMBLE, ADDRESS, S0, LENGTH, S1, PAYLOAD, and CRC. For Long Range (125 kbps and 500 kbps) *Bluetooth* Low Energy modes, fields CI, TERM1 and TERM2 are also included.

The content of a RADIO packet is illustrated in the figures below. The RADIO sends the fields in the packet according to the order illustrated in the figures, starting on the left.



Figure 136: On-air packet layout

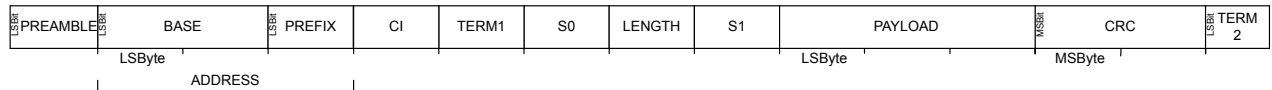


Figure 137: On-air packet layout for Long Range (125 kbps and 500 kbps) Bluetooth Low Energy modes

Not shown in the figures is the static payload add-on (the length of which is defined in [PCNF1.STATLEN](#), and which is 0 bytes in a standard BLE packet). The static payload add-on is sent between PAYLOAD and CRC fields. The RADIO sends the different fields in the packet in the order they are illustrated above, from left to right.

PREAMBLE is sent with least significant bit first on air. The size of the PREAMBLE depends on the mode selected in the [MODE](#) register:

- The PREAMBLE is one byte for [MODE](#) = Ble\_1Mbit as well as all Nordic proprietary operating modes ([MODE](#) = Nrf\_1Mbit and [MODE](#) = Nrf\_2Mbit), and [PCNF0.PLEN](#) has to be set accordingly. If the first bit of the ADDRESS is 0, the preamble will be set to 0xAA. Otherwise the PREAMBLE will be set to 0x55.
- For [MODE](#) = Ble\_2Mbit, the PREAMBLE must be set to 2 byte through [PCNF0.PLEN](#). If the first bit of the ADDRESS is 0, the preamble will be set to 0xAAAA. Otherwise the PREAMBLE will be set to 0x5555.
- For [MODE](#) = Ble\_LR125Kbit and [MODE](#) = Ble\_LR500Kbit, the PREAMBLE is 10 repetitions of 0x3C.
- For [MODE](#) = leee802154\_250Kbit, the PREAMBLE is 4 bytes and set to all zeros.

Radio packets are stored in memory inside instances of a RADIO packet data structure as illustrated below. The PREAMBLE, ADDRESS, CI, TERM1, TERM2, and CRC fields are omitted in this data structure. Fields S0, LENGTH, and S1 are optional.

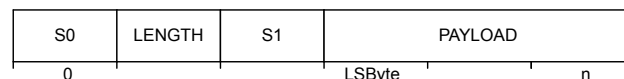


Figure 138: In-RAM representation of RADIO packet

The byte ordering on air is always least significant byte first for the ADDRESS and PAYLOAD fields, and most significant byte first for the CRC field. The ADDRESS fields are always transmitted and received least significant bit first. The CRC field is always transmitted and received most significant bit first. The endianness, i.e. the order in which the bits are sent and received, of the S0, LENGTH, S1, and PAYLOAD fields can be configured via [PCNF1.ENDIAN](#).

The sizes of the S0, LENGTH and S1 fields can be individually configured via SOLEN, LFLEN, and S1LEN in [PCNF0](#) respectively. If any of these fields are configured to be less than 8 bits, the least significant bits of the fields are used.

If S0, LENGTH, or S1 are specified with zero length, their fields will be omitted in memory. Otherwise each field will be represented as a separate byte, regardless of the number of bits in their on-air counterpart.

Independent of the configuration of [PCNF1.MAXLEN](#), the combined length of S0, LENGTH, S1, and PAYLOAD cannot exceed 258 bytes.

### 7.1.27.2 Address configuration

The on-air radio ADDRESS field is composed of two parts, the base address field and the address prefix field.

The size of the base address field is configurable via **PCNF1.BALEN**. The base address is truncated from the least significant byte if the **PCNF1.BALEN** is less than 4. See [Table 121: Definition of logical addresses](#) on page 411.

| Logical address | Base address | Prefix byte |
|-----------------|--------------|-------------|
| 0               | BASE0        | PREFIX0.AP0 |
| 1               | BASE1        | PREFIX0.AP1 |
| 2               | BASE1        | PREFIX0.AP2 |
| 3               | BASE1        | PREFIX0.AP3 |
| 4               | BASE1        | PREFIX1.AP4 |
| 5               | BASE1        | PREFIX1.AP5 |
| 6               | BASE1        | PREFIX1.AP6 |
| 7               | BASE1        | PREFIX1.AP7 |

Table 121: Definition of logical addresses

The on-air addresses are defined in the **BASE0/BASE1** and **PREFIX0/PREFIX1** registers. It is only when writing these registers that the user must relate to the actual on-air addresses. For other radio address registers, such as the **TXADDRESS**, **RXADDRESSES**, and **RXMATCH** registers, logical radio addresses ranging from 0 to 7 are being used. The relationship between the on-air radio addresses and the logical addresses is described in [Table 121: Definition of logical addresses](#) on page 411.

### 7.1.27.3 Data whitening

The RADIO is able to do packet whitening and de-whitening, enabled in **PCNF1.WHITEEN**. When enabled, whitening and de-whitening will be handled by the RADIO automatically as packets are sent and received.

The whitening word is generated using polynomial  $g(D) = D^7 + D^4 + 1$ , which then is XORed with the data packet that is to be whitened, or de-whitened. See the figure below.

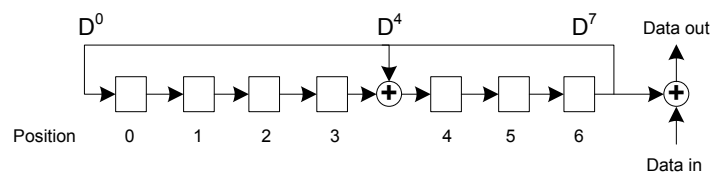


Figure 139: Data whitening and de-whitening

Whitening and de-whitening will be performed over the whole packet except for the preamble and the address fields.

Including the address field in CRC check (**CRCNF.SKIPADDR=Include**) is not supported for whitened packets.

The linear feedback shift register in the figure above is initialized via **DATAWHITEIV**.

### 7.1.27.4 CRC

The CRC generator in the RADIO calculates the CRC over the whole packet excluding the preamble. If desirable, the address field can be excluded from the CRC calculation as well.

See [CRCCNF](#) register for more information.

The CRC polynomial is configurable as illustrated in the following figure, where bit 0 in the [CRCPOLY](#) register corresponds to  $X^0$  and bit 1 corresponds to  $X^1$  etc. See [CRCPOLY](#) on page 467 for more information.

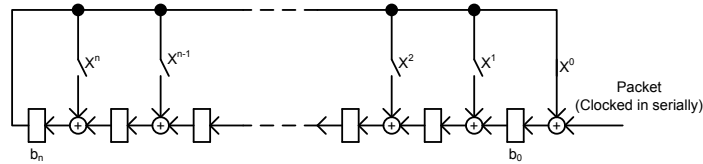


Figure 140: CRC generation of an  $n$  bit CRC

The figure shows that the CRC is calculated by feeding the packet serially through the CRC generator. Before the packet is clocked through the CRC generator, the CRC generator's latches  $b_0$  through  $b_n$  will be initialized with a predefined value specified in the [CRCINIT](#) register. After the whole packet has been clocked through the CRC generator,  $b_0$  through  $b_n$  will hold the resulting CRC. This value will be used by the RADIO during both transmission and reception. Latches  $b_0$  through  $b_n$  are not available to be read by the CPU at any time. However, a received CRC can be read by the CPU via the [RXCRC](#) register.

The length ( $n$ ) of the CRC is configurable, see [CRCCNF](#) for more information.

Once the entire packet, including the CRC, has been received and no errors were detected, the RADIO generates a [CRCOK](#) event. If CRC errors were detected, a [CRCERROR](#) event is generated.

The status of the CRC check can be read from the [CRCSTATUS](#) register after a packet has been received.

### 7.1.27.5 Radio states

Tasks and events are used to control the operating state of the RADIO.

The RADIO can enter the states described the table below.

| State     | Description                                                                                          |
|-----------|------------------------------------------------------------------------------------------------------|
| DISABLED  | No operations are going on inside the RADIO and the power consumption is at a minimum                |
| RXRU      | The RADIO is ramping up and preparing for reception                                                  |
| RXIDLE    | The RADIO is ready for reception to start                                                            |
| RX        | Reception has been started and the addresses enabled in the RXADDRESSES register are being monitored |
| TXRU      | The RADIO is ramping up and preparing for transmission                                               |
| TXIDLE    | The RADIO is ready for transmission to start                                                         |
| TX        | The RADIO is transmitting a packet                                                                   |
| RXDISABLE | The RADIO is disabling the receiver                                                                  |
| TXDISABLE | The RADIO is disabling the transmitter                                                               |

Table 122: RADIO state diagram

A state diagram showing an overview of the RADIO is shown in the following figure.



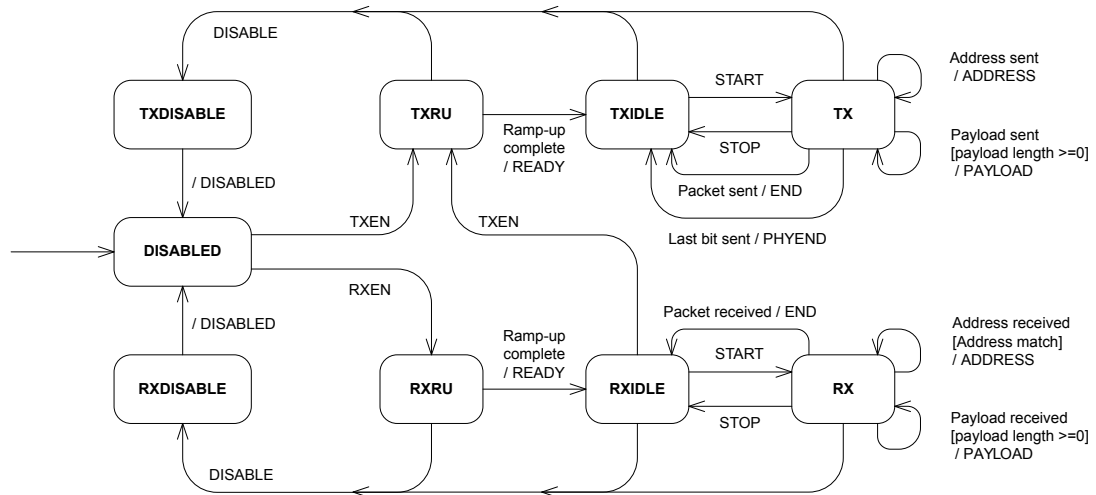


Figure 141: Radio states

This figure shows how the tasks and events relate to the RADIO's operation. The RADIO does not prevent a task from being triggered from the wrong state. If a task is triggered from the wrong state, for example if the **RXEN** task is triggered from the **RXDISABLE** state, this may lead to incorrect behavior. The **PAYLOAD** event is always generated even if the payload is zero.

The END to START shortcut should not be used with IEEE 802.15.4 250 kbps mode. Use the PHYEND to START shortcut instead.

The END to START shortcut should not be used with Long Range (125 kbps and 500 kbps) *Bluetooth* Low Energy modes. Use the PHYEND to START shortcut instead.

### 7.1.27.6 Transmit sequence

Before the RADIO is able to transmit a packet, it must first ramp-up in TX mode. See TXRU in [Figure 141: Radio states](#) on page 413 and [Figure 142: Transmit sequence](#) on page 414. A TXRU ramp-up sequence is initiated when the **TXEN** task is triggered. After the RADIO has successfully ramped up it will generate the **READY** event indicating that a packet transmission can be initiated. A packet transmission is initiated by triggering the **START** task. The **START** task can first be triggered after the RADIO has entered into the TXIDLE state.

The following figure illustrates a single packet transmission where the CPU manually triggers the different tasks needed to control the flow of the RADIO, i.e. no shortcuts are used. If shortcuts are not used, a certain amount of delay caused by CPU execution is expected between **READY** and **START**, and between **END** and **DISABLE**. As illustrated in [Figure 142: Transmit sequence](#) on page 414 the RADIO will by default transmit '1's between **READY** and **START**, and between **END** and **DISABLE**. What is transmitted can be programmed through the DTX field in the **MODECNFO** register.

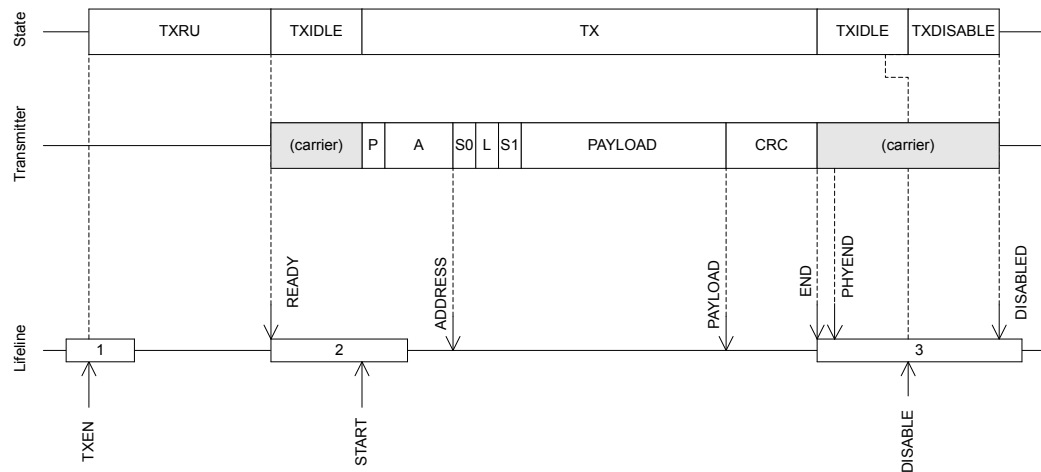


Figure 142: Transmit sequence

The following figure shows a slightly modified version of the transmit sequence where the RADIO is configured to use shortcuts between **READY** and **START**, and between **END** and **DISABLE**, which means that no delay is introduced.

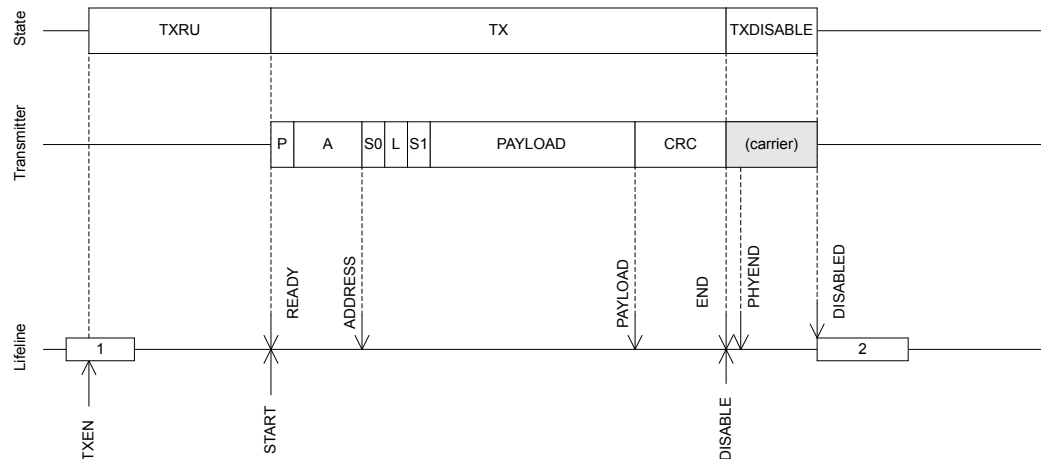


Figure 143: Transmit sequence using shortcuts to avoid delays

The RADIO is able to send multiple packets one after the other without having to disable and re-enable the RADIO between packets, as illustrated in the following figure.

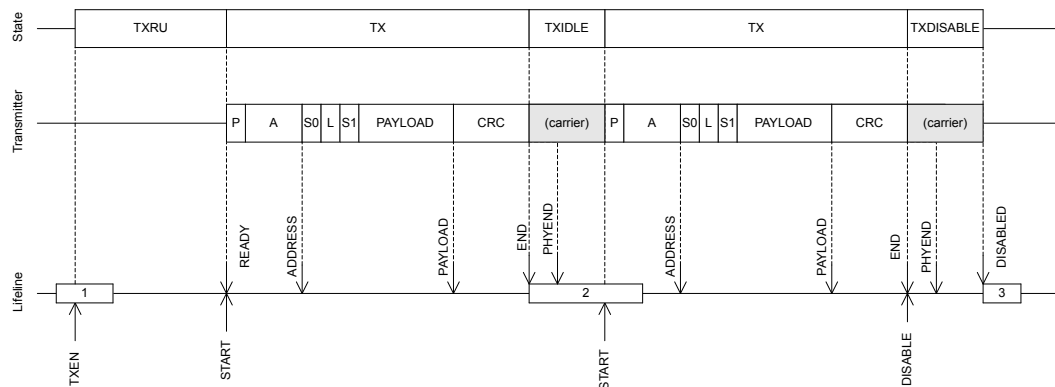


Figure 144: Transmission of multiple packets

### 7.1.27.7 Receive sequence

Before the RADIO is able to receive a packet, it must first ramp up in RX mode, see RXRU in [Figure 141: Radio states](#) on page 413 and [Figure 145: Receive sequence](#) on page 415.

An RXRU ramp up sequence is initiated when the **RXEN** task is triggered. After the RADIO has successfully ramped up it will generate the **READY** event indicating that a packet reception can be initiated. A packet reception is initiated by triggering the **START** task. As illustrated in [Figure 141: Radio states](#) on page 413, the **START** task can first be triggered after the RADIO has entered into the RXIDLE state.

The following figure shows a single packet reception where the CPU manually triggers the different tasks needed to control the flow of the RADIO, i.e. no shortcuts are used. If shortcuts are not used, a certain amount of delay caused by CPU execution is expected between **READY** and **START**, and between **END** and **DISABLE**. The RADIO will be listening and possibly receiving undefined data, represented with an 'X', from **START** and until a packet with valid preamble (P) is received.

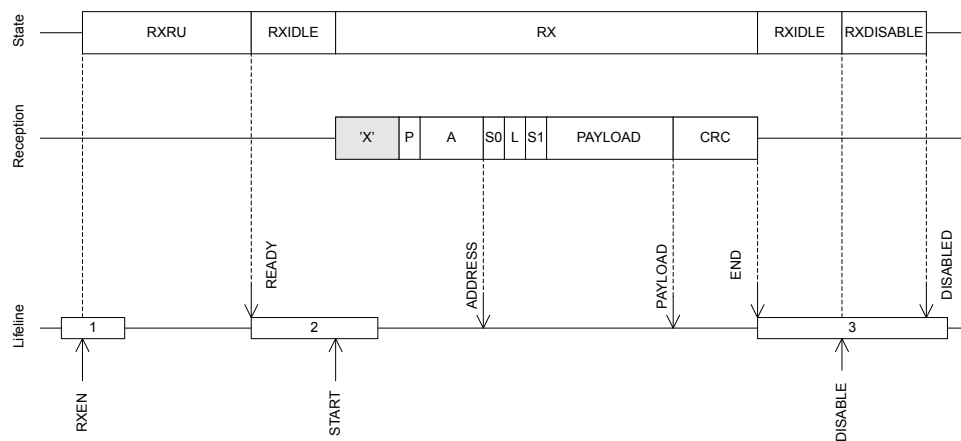


Figure 145: Receive sequence

The following figure shows a slightly modified version of the receive sequence, where the RADIO is configured to use shortcuts between **READY** and **START**, and between **END** and **DISABLE**, which means that no delay is introduced.

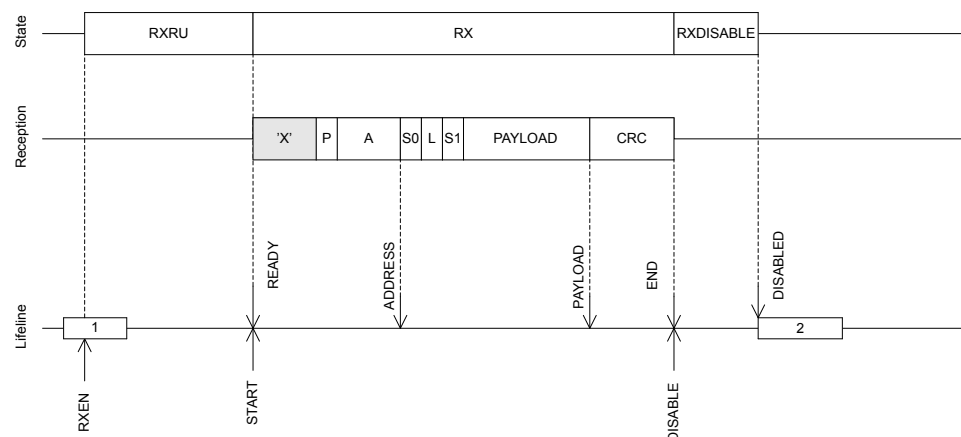


Figure 146: Receive sequence using shortcuts to avoid delays

The RADIO is able to receive consecutive packets without having to disable and re-enable the RADIO between packets, as illustrated in the figure below.

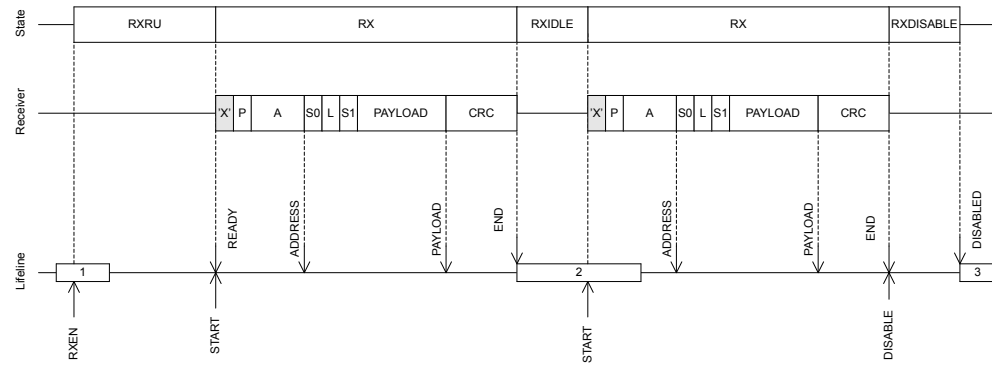


Figure 147: Reception of multiple packets

#### 7.1.27.8 Received signal strength indicator (RSSI)

The RADIO implements a mechanism for measuring the power in the received signal. This feature is called received signal strength indicator (RSSI).

The RSSI is measured continuously and the value filtered using a single-pole IIR filter. After a signal level change, the RSSI will settle after approximately `RSSISETTLE`.

Sampling of the received signal strength is started by using the `RSSISTART` task. The sample can be read from the `RSSISAMPLE` register.

The sample period of the RSSI is defined by `RSSIPERIOD`. The `RSSISAMPLE` will hold the filtered received signal strength after this sample period.

For the RSSI sample to be valid, the RADIO has to be enabled in receive mode (`RXEN` task) and the reception has to be started (`READY` event followed by `START` task).

#### 7.1.27.9 Interframe spacing (IFS)

Interframe spacing (IFS) is defined as the time, in microseconds, between two consecutive packets, starting from when the end of the last bit of the previous packet is received, to the beginning of the first bit of the subsequent packet that is transmitted. The RADIO is able to enforce this interval, as specified in the `TIFS` register, as long as the `TIFS` is not specified to be shorter than the RADIO's turnaround time, i.e. the time needed to switch off the receiver, and then switch the transmitter back on. The `TIFS` register can be written any time before the last bit on air is received.

This timing is illustrated in the figure below.

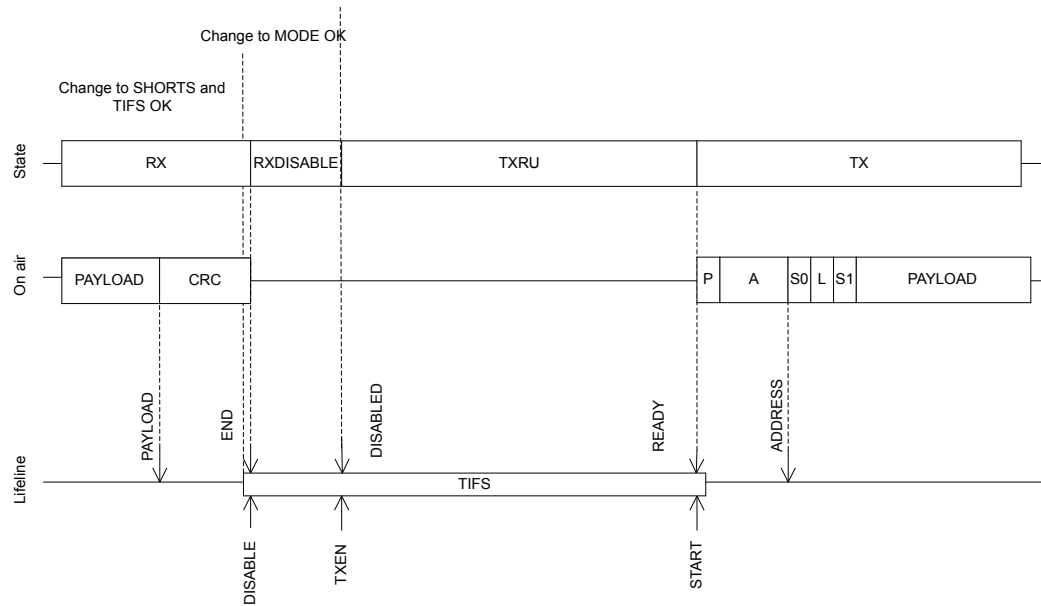


Figure 148: IFS timing detail

The TIFS duration starts after the last bit on air (just before the **END** event), and elapses with first bit being transmitted on air (just after **READY** event).

TIFS is only enforced if the shortcuts **END** to **DISABLE** and **DISABLED** to **TXEN** or **END** to **DISABLE** and **DISABLED** to **RXEN** are enabled.

TIFS is qualified for use in IEEE 802.15.4 250kbps mode, Long Range (125 kbps and 500 kbps) *Bluetooth* Low Energy modes, 1 Mbps and 2 Mbps *Bluetooth* Low Energy modes, using the default ramp-up mode.

**SHORTS** and **TIFS** registers are not double-buffered, and can be updated at any point before the last bit on air is received. The **MODE** register is double-buffered and sampled at the **TXEN** or **RXEN** task.

#### 7.1.27.10 Device address match

The device address match feature is tailored for address whitelisting in *Bluetooth* low energy and similar implementations.

This feature enables on-the-fly device address matching while receiving a packet on air. This feature only works in receive mode and when the RADIO is configured for little endian, see **PCNF1.ENDIAN**.

The device address match unit assumes that the first 48 bits of the payload are the device address and that bit number 6 in S0 is the TxAdd bit. See the *Bluetooth* Core Specification for more information about device addresses, TxAdd, and whitelisting.

The RADIO is able to listen for eight different device addresses at the same time. These addresses are specified in a DAB/DAP register pair, one pair per address, in addition to a TxAdd bit configured in the DACNF register. The DAB register specifies the 32 least significant bits of the device address, while the DAP register specifies the 16 most significant bits of the device address.

Each of the device addresses can be individually included or excluded from the matching mechanism. This is configured in the **DACNF** register.

#### 7.1.27.11 Bit counter

The RADIO implements a simple counter that can be configured to generate an event after a specific number of bits have been transmitted or received.

By using shortcuts, this counter can be started from different events generated by the RADIO and count relative to these.

The bit counter is started by triggering the **BCSTART** task, and stopped by triggering the **BCSTOP** task. A **BCMATCH** event will be generated when the bit counter has counted the number of bits specified in the **BCC** register. The bit counter will continue to count bits until the **DISABLED** event is generated or until the **BCSTOP** task is triggered. The CPU can therefore, after a **BCMATCH** event, reconfigure the **BCC** value for new **BCMATCH** events within the same packet.

The bit counter can only be started after the RADIO has received the **ADDRESS** event.

The bit counter will stop and reset on either the **BCSTOP**, **STOP**, or **DISABLE** task, or the **END** event.

The figure below illustrates how the bit counter can be used to generate a **BCMATCH** event in the beginning of the packet payload, and again generate a second **BCMATCH** event after sending 2 bytes (16 bits) of the payload.

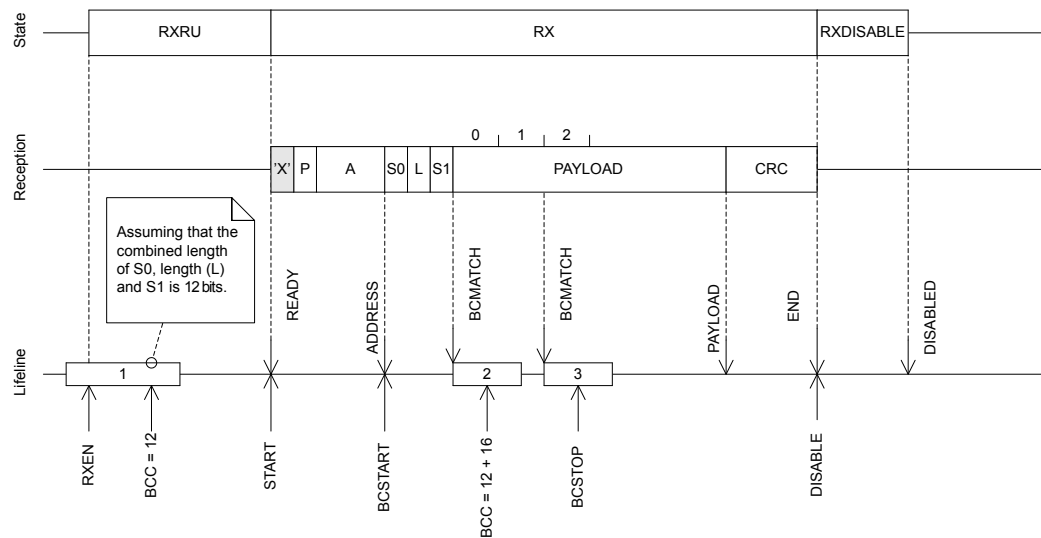


Figure 149: Bit counter example

### 7.1.27.12 Direction finding

The RADIO implements the Angle-of-Arrival (AoA) and Angle-of-Departure (AoD) Bluetooth Low Energy feature, which can be used to determine the direction of a peer device. The feature is available for the BLE 1 Mbps and BLE 2 Mbps modes.

When using this feature, the transmitter sends a packet with a continuous tone extension (CTE) appended to the packet, after the CRC. During the CTE, the receiver can take IQ samples of the incoming signal.

An antenna array is employed at the transmitter (AoD) or at the receiver (AoA). The AoD transmitter, or AoA receiver, switches between the antennas, in order to collect IQ samples from the different antenna pairs. The IQ samples can be used to calculate the relative path lengths between the antenna pairs, which can be used to estimate the direction of the transmitter.

#### 7.1.27.12.1 CTE format

The CTE is from 16  $\mu$ s to 160  $\mu$ s and consists of an unwhitened sequence of 1's, equivalent to a continuous tone nominally offset from the carrier by +250 kHz for the 1 Mbps PHY and +500 kHz for the 2 Mbps BLE PHYs. The format of the CTE, when switching and/or sampling, is shown below.

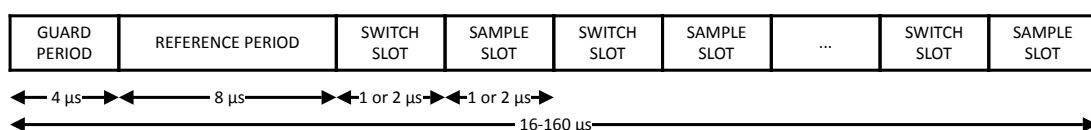


Figure 150: Constant tone extension (CTE) structure

Antenna switching is performed during switch slots and the guard period. The AoA/AoD feature requires that one IQ sample is taken for each microsecond within the reference period, and once for each sample slot. Oversampling is possible by changing the sample spacing as described in [IQ sampling](#) on page 422. The switch slot and sample slot durations are either 1 or 2  $\mu$ s, but must be equal. The format of the CTE and switching and sampling procedures may be configured prior to, or during, packet transmission and reception. Alternatively, during packet reception, these operations can be configured by reading specific fields of the packet contents.

### 7.1.27.12.2 Mode

Depending on the [DFEMODE](#), the device performs the following procedures:

|                   |                                           | DFEMODE |    |     |    |
|-------------------|-------------------------------------------|---------|----|-----|----|
|                   |                                           | AOA     |    | AOD |    |
|                   |                                           | TX      | RX | TX  | RX |
| AoA/AoD Procedure | Generating and transmitting CTE           | x       |    | x   |    |
|                   | Receiving, interpreting, and sampling CTE |         | x  |     | x  |
|                   | Antenna switching                         |         | x  | x   |    |

Table 123: AoA/AoD Procedures performed as a function of DFEMODE and TX/RX mode

### 7.1.27.12.3 Inline configuration

When inline configuration is enabled during RX, further configuration of the AoA/AoD procedures is performed based on the values of the CP bit and the CTEInfo octet within the packet. This is enabled by setting [CTEINLINECONF.CTEINLINCTRLIN](#). The CTEInfo octet is present only if the CP bit is set. The position of the CP bit and CTEInfo octet depends on whether the packet has a *Data Channel PDU* ([CTEINLINECONF.CTEINFOINS1=InS1](#)), or an *Advertising Channel PDU* ([CTEINLINECONF.CTEINFOINS1=NotInS1](#)).

#### Data channel PDU

For Data Channel PDUs, [PCNF0.SOLEN](#) must be 1 byte, and [PCNF0.LFLEN](#) must be 8 bits. To determine if S1 is present, the registers [CTEINLINECONF.SOMASK](#) and [CTEINLINECONF.SOCONF](#) forms a bitwise mask-and-test for the S0 field. If the bitwise AND between S0 and SOMASK equals SOCONF, then S1 is determined to be present. When present, the value of [PCNF0.S1LEN](#) will be ignored, as this is decided by the CP bit in the the following figure.

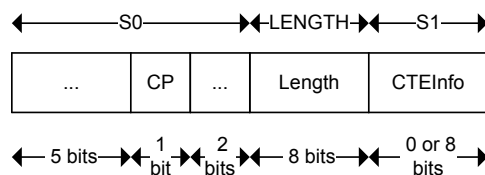


Figure 151: Data channel PDU header

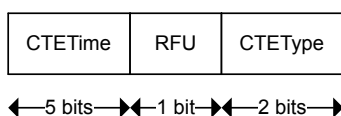
When encrypting and decrypting BLE packets using the [CCM](#) peripheral, it is also required to set [PCNF0.S1INCL=1](#). The CCM mode must be configured to use an 8-bit length field. The value of the CP bit is included in the calculation of the MIC, while the S1 field is ignored by the CCM calculation.

#### Advertising channel PDU

For advertising channel PDUs, the CTEInfo Flag replaces the CP bit. The CTEInfo Flag is within the extended header flag field in some of the advertising PDUs that employ the common extended advertising payload format (i.e. [AUX\\_SYNC\\_IND](#), [AUX\\_CHAIN\\_IND](#)). The format of such packets is shown in the following figure.

The `CTEINLINECONF.S0CONF` and `CTEINLINECONF.S0MASK` fields can be configured to accept only certain advertising PDU Types. If the extended header length is non-zero, the CTEInfo extended header flag is checked to determine whether CTEInfo is present. If a bit before the CTEInfo flag within the extended header flags is set, then the CTEInfo position is postponed 6 octets.

The CTEInfo field is shown in the following figure.



The CTETIME field defines the length of the CTE in 8  $\mu$ s units. The valid upper bound of values can be adjusted using [CTEINLINECONF.CTETIMEVALIDRANGE](#), including allowing use of the RFU bit within this field. If the CTETIME field is an invalid value of either 0 or 1, the CTE is assumed to be the minimum valid length of 16  $\mu$ s. The slot duration is determined by the CTEType field. In RX this determines whether the sample spacing as defined in [CTEINLINECONF.CTEINLINERXMODE1US](#) or [CTEINLINECONF.CTEINLINERXMODE2US](#) is used.

| CTEType | Description             | TX switch spacing | RX sample spacing during reference period | Sample spacing RX during reference period |
|---------|-------------------------|-------------------|-------------------------------------------|-------------------------------------------|
| 0       | AoA, no switching       | -                 | TSAMPLESPACING1                           | TSAMPLESPACING2                           |
| 1       | AoD, 1 $\mu$ s slots    | 2 $\mu$ s         | TSAMPLESPACING1                           | CTEINLINERXMODE1US                        |
| 2       | AoD, 2 $\mu$ s slots    | 4 $\mu$ s         | TSAMPLESPACING1                           | CTEINLINERXMODE2US                        |
| 3       | Reserved for future use |                   |                                           |                                           |

Table 124: Switching and sampling spacing based on CTEType

If [CTEINLINECONF.CTEINLINERLEN](#) is not set, then the packet is not parsed to determine the CTE parameters, and the antenna switching and sampling is controlled by other registers, see [Antenna switching](#) on page 421. The length of the CTE is given in 8  $\mu$ s units by [DFECTRL1.NUMBEROF8US](#). The start of the antenna switching and/or sampling (denoted as an AoA/AoD procedure), can be configured to start at some trigger with an additional offset. Using [DFECTRL1.DFEINEXTENSION](#), the trigger can be configured to be the end of the CRC, or alternatively, the ADDRESS event. The additional offset for antenna switching is configured using [DFECTRL2.TSWITCHOFFSET](#). Similarly, the additional offset for antenna sampling is configured using [DFECTRL2.TSAMPLEOFFSET](#).

The addition of the CTE to the transmitted packet is illustrated in the following figure.



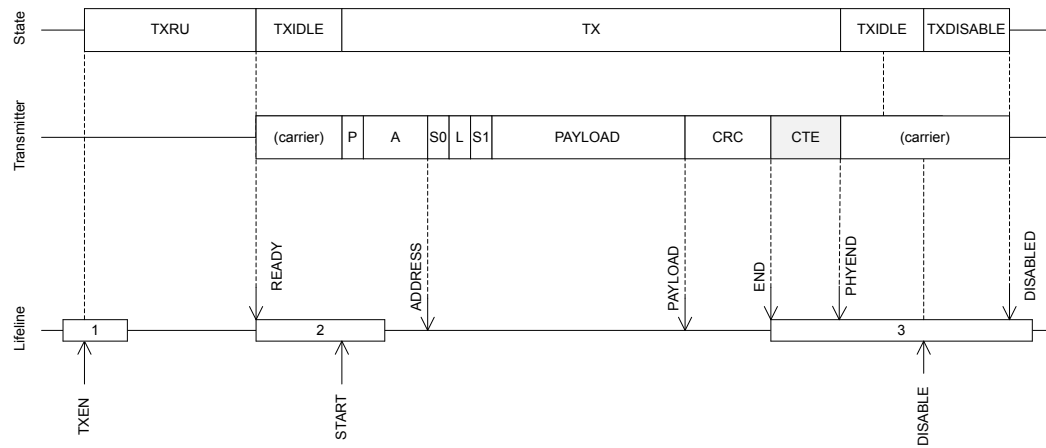


Figure 154: Transmit sequence with DFE

The presence of CTE within a received packet is signalled by the **CTEPRESENT** and **CTEWARNING** events illustrated in the figure below.

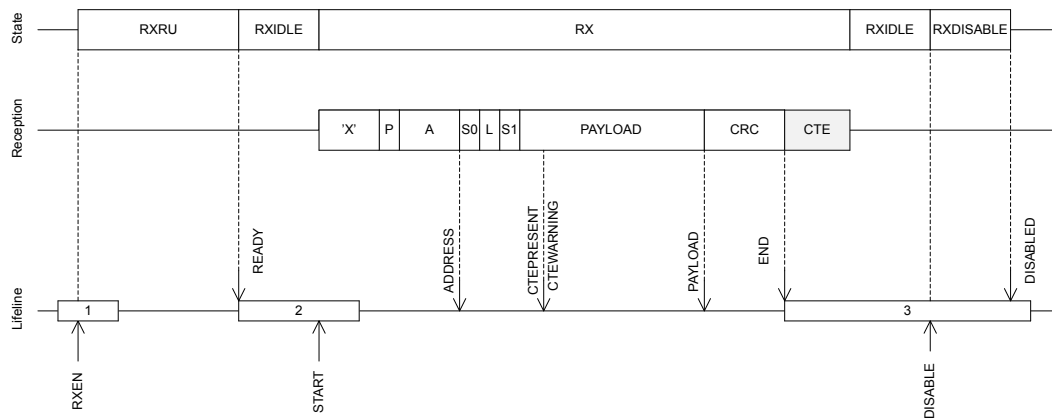


Figure 155: Receive sequence with DFE

### 7.1.27.12.6 Antenna switching

The RADIO can control up to 8 GPIO pins in order to control external antenna switches used in direction finding.

#### Pin configuration

The eight antenna selection signals are mapped to physical pins according to the pin numbers specified in the **PSEL.DFEGPIO[n]** registers. Only pins that have the **PSEL.DFEGPIO[n].CONNECTED** field set to *Connected* will be controlled by the RADIO. Pins that are *Disconnected* will be controlled by GPIO.

During transmission in AoD TX mode or reception in AoA RX mode, the RADIO automatically acquires the pins as needed. At times when the RADIO does not use the pin, the pin is released to its default state and controlled by the **GPIO** configuration. Thus, the pin must be configured using the **GPIO** peripheral.

| Pin acquired by RADIO | Direction                | Value                             | Comment                                                                                |
|-----------------------|--------------------------|-----------------------------------|----------------------------------------------------------------------------------------|
| Yes                   | Output                   | Specified in <b>SWITCHPATTERN</b> | Pin acquired by RADIO, and in use for DFE.                                             |
| No                    | Specified by <b>GPIO</b> | Specified by <b>GPIO</b>          | DFE not in progress. Pin has not been acquired by RADIO, but is available for DFE use. |

Table 125: Pin configuration matrix for a connected and enabled pin [n]

## Switch pattern configuration

The values of the GPIOs while switching during the CTE are configured by writing successively to the **SWITCHPATTERN** register. The first write to **SWITCHPATTERN** is the GPIO pattern applied from the call of **TASKS\_TXEN** or **TASKS\_RXEN** until the first antenna switch is triggered. The second write sets the pattern for the reference period and is applied at the start of the guard period. The following writes set the pattern for the remaining switch slots and are applied at the start of each switch slot. If writing beyond the total number of antenna slots, the pattern will wrap to **SWITCHPATTERN[2]** and start over again. During operation, when the end of the **SWITCHPATTERN** buffer is reached, the RADIO cycles back to **SWITCHPATTERN[2]**. At the end of the AoA/AoD procedure, **SWITCHPATTERN[0]** is applied to **DFECTRL1.TSWITCHSPACING** after the previous antenna switch. The **SWITCHPATTERN** buffer can be erased/cleared using **CLEARPATTERN**.

A minimum number of three patterns must be written to the **SWITCHPATTERN** register.

If **CTEINLINECONF.CTEINLINECTRLLEN** is not set, then the antenna switch spacing is determined by **DFECTRL1.TSWITCHSPACING** (otherwise described by [Table 124: Switching and sampling spacing based on CTEType](#) on page 420). **DFECTRL2.TSWITCHOFFSET** determines the position of the first switch compared to the configurable start of CTE (see **DFECTRL1.DFEINEXTENSION**).

### 7.1.27.12.7 IQ sampling

The RADIO uses DMA to write IQ samples recorded during the CTE to RAM. Alternatively, the magnitude and phase of the samples can be recorded using the **DFECTRL1.SAMPLETYPE** field. The samples are written to the location in RAM specified by **DFEPACKET.PTR**. The maximum number of samples to transfer are specified by **DFEPACKET.MAXCNT** and the number of samples transferred are given in **DFEPACKET.AMOUNT**. The IQ samples are recorded with respect to the RX carrier frequency. The format of the samples is provided in the following table.

| SAMPLETYPE       | Field     | Bits  | Description                                                                                           |
|------------------|-----------|-------|-------------------------------------------------------------------------------------------------------|
| 0: I_Q (default) | Q         | 31:16 | 12 bits signed, sign extended to 16 bits                                                              |
|                  | I         | 15:0  |                                                                                                       |
| 1: MagPhase      | reserved  | 31:29 | Always zero                                                                                           |
|                  | magnitude | 28:16 | 13 bits unsigned. Equals $1.646756 \cdot \sqrt{I^2 + Q^2}$                                            |
|                  | phase     | 15:0  | 9 bits signed, sign extended to 16 bits. Equals $64 \cdot \text{atan2}(Q, I)$ in the range [-201,201] |

Table 126: Format of samples

Oversampling is configured separately for the reference period and for the time after the reference period. During the reference period, the sample spacing is determined by **DFECTRL1.TSAMPLESPACINGREF**. **DFECTRL2.TSAMPLEOFFSET** determines the position of the first sample relative to the end of the last bit of the CRC.

For the time after the reference period, if **CTEINLINECONF.CTEINLINECTRLLEN** is disabled, the sample spacing is set in **DFECTRL1.TSAMPLESPACING**. However, when **CTEINLINECONF.CTEINLINECTRLLEN** is enabled, the sample spacing are determined by two different registers, depending on whether the device is in AoA or AoD RX-mode, as follows.

For AoD RX mode, the sample spacing after the reference period is determined by the CTEType in the packet, as listed in the table below.

| CTEType             | Sample spacing                          |
|---------------------|-----------------------------------------|
| AoD 1 $\mu$ s slots | <b>CTEINLINECONF.CTEINLINERXMODE1US</b> |
| AoD 2 $\mu$ s slots | <b>CTEINLINECONF.CTEINLINERXMODE2US</b> |
| Other               | <b>DFECTRL1.TSAMPLESPACING</b>          |

Table 127: Sample spacing when **CTEINLINECONF.CTEINLINECTRLLEN** is set and the device is in AoD RX mode

For AoA RX mode, the sample spacing after the reference period is determined by [DFECTRL1.TSWITCHSPACING](#), as listed in the table below.

| <a href="#">DFECTRL1.TSWITCHSPACING</a> | Sample spacing                                   |
|-----------------------------------------|--------------------------------------------------|
| 2 $\mu$ s                               | <a href="#">CTEINLINECONF.CTEINLINERXMODE1US</a> |
| 4 $\mu$ s                               | <a href="#">CTEINLINECONF.CTEINLINERXMODE2US</a> |
| Other                                   | <a href="#">DFECTRL1.TSAMPLESPACING</a>          |

Table 128: Sample spacing when [CTEINLINECONF.CTEINLINECTRLLEN](#) is set and the device is in AoA RX mode

For the reference- and switching periods, [DFECTRL1.TSAMPLESPACINGREF](#) and [DFECTRL1.TSAMPLESPACING](#) can be used to achieve oversampling.

### 7.1.27.13 IEEE 802.15.4 operation

With the [MODE=ieee802154\\_250kbit](#) the RADIO will comply with the IEEE 802.15.4-2006 standard implementing its 250 kbps, 2450 MHz, O-QPSK PHY.

The IEEE 802.15.4 standard differs from Nordic's proprietary and *Bluetooth* low energy modes. Notable differences include modulation scheme, channel structure, packet structure, security, and medium access control.

The main features of the IEEE 802.15.4 mode are:

- Ultra-low power 250 kbps, 2450 MHz, IEEE 802.15.4-2006 compliant link
- Clear channel assessment
- Energy detection scan
- CRC generation

#### 7.1.27.13.1 Packet structure

The IEEE 802.15.4 standard defines an on-the-air frame/packet that is different from what is used in BLE mode.

The following figure provides an overview of the physical frame structure and its timing.

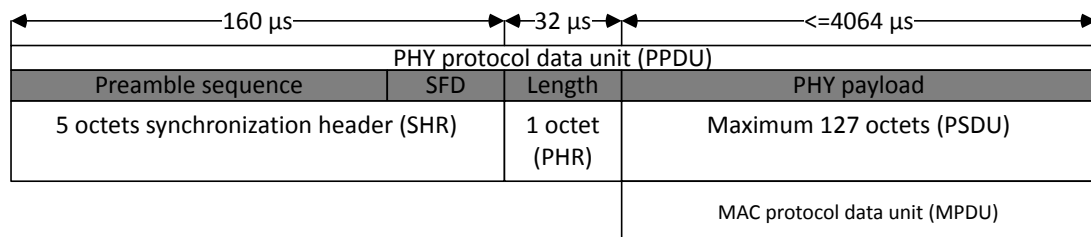


Figure 156: IEEE 802.15.4 frame format (PPDU)

The standard uses the term *octet* for an 8-bit storage unit within the PPDU. For timing, the value *symbol* is used, and it has a duration of 16  $\mu$ s.

The total usable payload (PSDU) is 127 octets, but when CRC is in use, this is reduced to 125 octets of usable payload.

The preamble sequence consists of four octets that are all zero, and are used for synchronizing the RADIO's receiver. Following the preamble is the single octet *start of frame delimiter (SFD)*, with a fixed value of 0xA7. An alternate SFD can be programmed through the [SFD](#) register, providing an initial level of frame filtering for those who choose non-standard compliance. It is a valuable feature when operating in a congested or private network. The preamble sequence and the SFD are generated by the RADIO, and are not programmed by the user into the frame buffer.

Following the five octet *synchronization header (SHR)* is the single octet *phy header (PHR)*. The least significant seven bits of PHR denote the frame length of the following PSDU. The most significant bit is reserved and is set to zero for frames that are standard compliant. The RADIO reports all eight bits which can be used to carry additional information. The PHR is the first byte written to the frame data memory pointed to by [PACKETPTR](#). Frames with zero length are discarded, and the [FRAMESTART](#) event is not generated in this case.

The next N octets carry the data of the PHY packet, where N equals the value of the PHR. For an implementation also using the IEEE 802.15.4 MAC layer, the PHY data is a MAC frame of N-2 octets, since two octets occupy a CRC field.

As illustrated in the figure below, an IEEE 802.15.4 MAC layer frame always consists of

- A header:
  - The frame control field (FCF)
  - The sequence number
  - Addressing fields
- A payload
- The 16-bit frame control sequence (FCS)

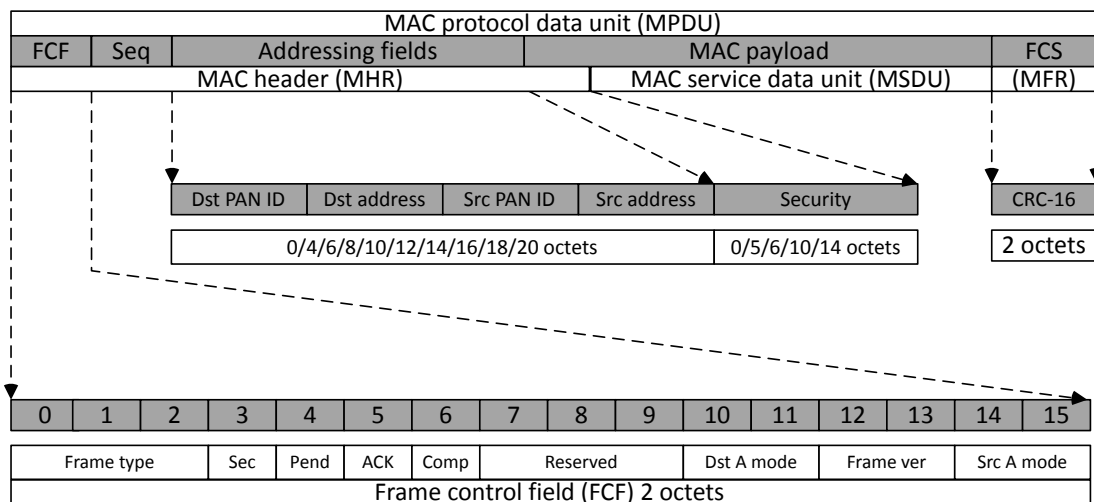


Figure 157: IEEE 802.15.4 frame format (MPDU)

The two FCF octets contain information about the frame type, addressing, and other control flags. This field is decoded when using the assisted operating modes offered by the RADIO.

The sequence number is a single octet in size and is unique for a frame. It is used in the associated acknowledgement frame sent upon successful frame reception.

The addressing field can be zero (acknowledgement frame) or up to 20 octets in size. The field is used to direct packets to the correct recipient and denote its origin. IEEE 802.15.4 bases its addressing on networks being organized in PANs with 16-bit identifier and nodes having a 16-bit or 64-bit address. In the assisted receive mode, these parameters are analyzed for address matching and acknowledgement.

The MAC payload carries the data of the next higher layer, or in the case of a MAC command frame, information used by the MAC layer itself.

The two last octets contain the 16-bit ITU-T CRC. The FCS is calculated over the MAC header (MHR) and MAC payload (MSDU) parts of the frame. This field is calculated automatically when sending a frame, or indicated in the [CRCSTATUS](#) register when a frame is received. If configured, this feature is taken care of autonomously by the CRC module.

### 7.1.27.13.2 Operating frequencies

The IEEE 802.15.4 standard defines 16 channels, 11 - 26, of 5 MHz each, in the 2450 MHz frequency band.

To choose the correct channel center frequency, the **FREQUENCY** register must be programmed according to the table below.

| IEEE 802.15.4 channel | Center frequency (MHz) | FREQUENCY setting |
|-----------------------|------------------------|-------------------|
| Channel 11            | 2405                   | 5                 |
| Channel 12            | 2410                   | 10                |
| Channel 13            | 2415                   | 15                |
| Channel 14            | 2420                   | 20                |
| Channel 15            | 2425                   | 25                |
| Channel 16            | 2430                   | 30                |
| Channel 17            | 2435                   | 35                |
| Channel 18            | 2440                   | 40                |
| Channel 19            | 2445                   | 45                |
| Channel 20            | 2450                   | 50                |
| Channel 21            | 2455                   | 55                |
| Channel 22            | 2460                   | 60                |
| Channel 23            | 2465                   | 65                |
| Channel 24            | 2470                   | 70                |
| Channel 25            | 2475                   | 75                |
| Channel 26            | 2480                   | 80                |

Table 129: IEEE 802.15.4 center frequency definition

### 7.1.27.13.3 Energy detection (ED)

As required by the IEEE 802.15.4 standard, it must be possible to sample the received signal power within the bandwidth of a channel, for the purpose of determining presence of activity.

To prevent the channel signal from being decoded, the shortcut between the **READY** event and the **START** task should be disabled before putting the RADIO in receive mode. The energy detection (ED) measurement time, where RSSI samples are averaged, is 8 symbol periods, corresponding to 128  $\mu$ s. The standard further specifies the measurement to be a number between 0 and 255, where 0 shall indicate received power less than 10 dB above the selected receiver sensitivity. The power range of the ED values must be at least a 40 dB linear mapping with accuracy of  $\pm 6$  dB. See section 6.9.7 *Receiver ED* in the IEEE 802.15.4 standard for further details.

The following example shows how to perform a single energy detection measurement and convert to IEEE 802.15.4 scale.

#### IEEE 802.15.4 ED measurement example

```
#define ED_RSSISCALE 4 // From electrical specifications
uint8_t sample_ed(void)
{
    int val;
    NRF_RADIO->TASKS_EDSTART = 1; // Start
    while (NRF_RADIO->EVENTS_EDEND != 1) {
        // CPU can sleep here or do something else
        // Use of interrupts are encouraged
    }
    val = NRF_RADIO->EDSAMPLE; // Read level
    return (uint8_t)(val > 63 ? 255 : val * ED_RSSISCALE); // Convert to IEEE 802.15.4 scale
}
```

For scaling between hardware value and dBm, see equation [Figure 159: Conversion between hardware value and dBm](#) on page 427.

The `mlme-scan.req` primitive of the MAC layer uses the ED measurement to detect channels where there might be wireless activity. To assist this primitive, a tailored mode of operation is available where the ED measurement runs for a defined number of iterations keeping track of the maximum ED level. This is engaged by writing the `EDCNT` register to a value different from 0, where it will run the specified number of iterations and report the maximum energy measurement in the `EDSAMPLE` register. The scan is started with `EDSTART` task and its end indicated with the `EDEND` event. This significantly reduces the interrupt frequency and therefore power consumption. The following figure shows how the ED measurement will operate depending on the `EDCNT` register.

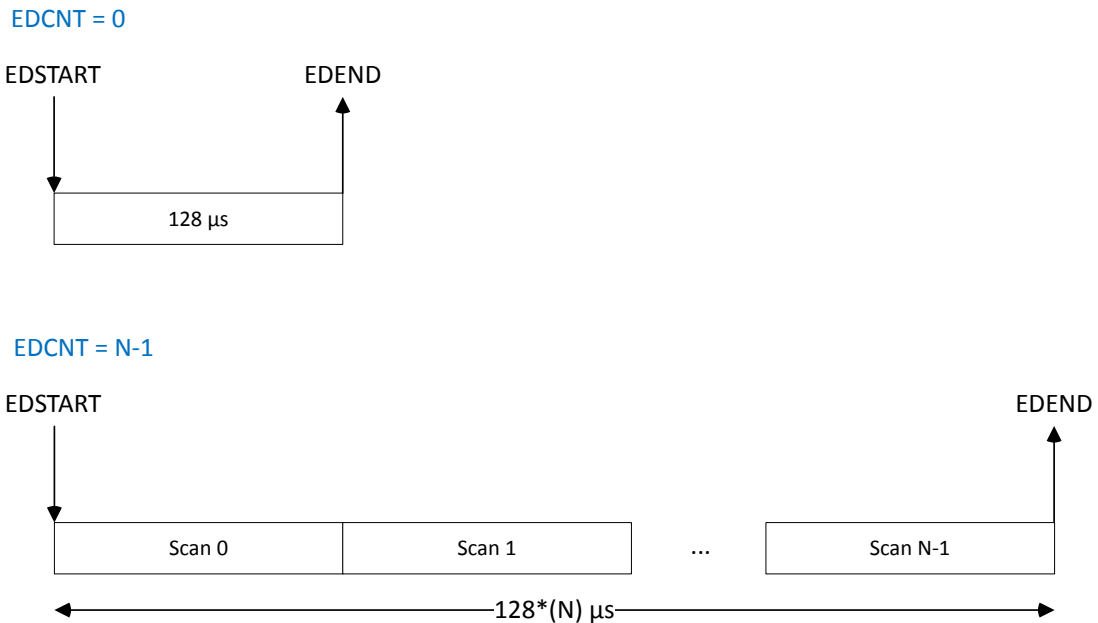


Figure 158: Energy detection measurement examples

The scan is stopped by writing the `EDSTOP` task. It will be followed by the `EDSTOPPED` event when the module has terminated.

#### 7.1.27.13.4 Clear channel assessment (CCA)

IEEE 802.15.4 implements a listen-before-talk channel access method to avoid collisions when transmitting, known as *carrier sense multiple access with collision avoidance (CSMA-CA)*. The key part of this is measuring if the wireless medium is busy or not.

The following clear channel assesment modes are supported:

- **CCA Mode 1** (energy above threshold): The medium is reported busy upon detecting any energy above the ED threshold.
- **CCA Mode 2** (carrier sense only): The medium is reported busy upon detection of a signal compliant with the IEEE 802.15.4 standard with the same modulation and spreading characteristics.
- **CCA Mode 3** (carrier sense with energy above threshold): The medium is reported busy using a logical combination (AND/OR) between the results from CCA Mode 1 and CCA Mode 2.

The clear channel assessment should survey a period equal to 8 symbols or  $128 \mu\text{s}$ .

The RADIO must be in receive mode and be able to receive correct packets when performing the CCA. The shortcut between `READY` and `START` must be disabled if baseband processing is not to be performed while the measurement is running.

#### CCA Mode 1

**CCA Mode 1** is enabled by first configuring the field `CCACTRL.CCAMODE`=EdMode and writing the `CCACTRL.CCAEDTHRES` field to a chosen value. Once the `CCASTART` task is written, the RADIO will

perform a ED measurement for 8 symbols and compare the measured level with that found in the `CCACTRL.CCAEDTHRES` field. If the measured value is higher than or equal to this threshold, the `CCABUSY` event is generated. If the measured level is less than the threshold, the `CCAIDLE` event is generated.

## CCA Mode 2

*CCA Mode 2* is enabled by configuring `CCACTRL.CCAMODE=CarrierMode`. The RADIO will sample to see if a valid SFD is found during the 8 symbols. If a valid SFD is detected, the `CCABUSY` event is generated and the device should not send any data. The `CCABUSY` event is also generated if the scan was performed during an ongoing frame reception. In the case where the measurement period completes with no SFD detection, the `CCAIDLE` event is generated. With `CCACTRL.CCACORRCNT` not being zero, the algorithm will look at the correlator output in addition to the SFD detection signal. If a SFD is reported during the scan period, it will terminate immediately indicating busy medium. Similarly, if the number of peaks above `CCACTRL.CCACORRTHRES` crosses the `CCACTRL.CCACORRCNT`, the `CCACTRL.CCABUSY` event is generated. If less than `CCACORRCOUNT` crossings are found and no SFD is reported, the `CCAIDLE` event will be generated and the device can send data.

## CCA Mode 3

*CCA Mode 3* is enabled by configuring `CCACTRL.CCAMODE=CarrierAndEdMode` or `CCACTRL.CCAMODE=CarrierOrEdMode`, performing the required logical combination of the result from CCA Mode 1 and 2. The `CCABUSY` or `CCAIDLE` events are generated by ANDing or ORing the *energy above threshold* and *carrier detection* scans.

## Shortcuts

An ongoing CCA can always be stopped by issuing the `CCASTOP` task. This will trigger the associated `CCASTOPPED` event.

For CCA mode automation, a number of shortcuts are available.

- To automatically switch between RX (when performing the CCA) and to TX where the packet is sent, the shortcut between `CCAIDLE` and `TXEN`, in conjunction with the short between `CCAIDLE` and `STOP` must be used.
- To automatically disable the RADIO whenever the CCA reports a busy medium, the shortcut between `CCABUSY` and `DISABLE` can be used.
- To immediately start a CCA after ramping up into RX mode, the shortcut between `RXREADY` and `CCASTART` can be used.

## Conversion

The conversion from a `CCAEDTHRES`, `CCA`, or `EDLEVEL` value to dBm can be done with the following equation, where `VALHARDWARE` is the hardware-reported values, being either `CCAEDTHRES`, `CCA` or `EDLEVEL`, and constants `ED_RSSISCALE` and `ED_RSSIOFFS` are from electrical specifications.

$$P_{RF}[dBm] = ED\_RSSIOFFS + ED\_RSSISCALE \times VAL_{HARDWARE}$$

Figure 159: Conversion between hardware value and dBm

### 7.1.27.13.5 Cyclic redundancy check (CRC)

IEEE 802.15.4 uses a 16-bit ITU-T cyclic redundancy check (CRC) calculated over the MAC header (MHR) and MAC service data unit (MSDU).

The standard defines the following generator polynomial:

$$G(x) = x^{16} + x^{12} + x^5 + 1$$

In receive mode the RADIO will trigger the CRC module when the first octet after the frame length (PHR) is received. The CRC will then update on each consecutive octet received. When a complete frame is received the **CRCSTATUS** register will be updated accordingly and the **CRCOK** or **CRCERROR** events generated. When the CRC module is enabled it will not write the two last octets (CRC) to the frame Data RAM. When transmitting, the CRC will be computed on the fly, starting with the first octet after PHR, and inserted as the two last octets in the frame. The EasyDMA will fetch frame length minus 2 octets from RAM and insert the CRC octets insitu.

Below is a code snippet for configuring the CRC module for correct operation when in IEEE 802.15.4 mode. The **CRCNCF** is written to 16-bit CRC and the **CRCPOLY** is written to 0x11021. The start value used by IEEE 802.15.4 is zero and **CRCINIT** is configured to reflect this.

```
/* 16-bit CRC with ITU-T polynomial with 0 as start condition*/
NRF_RADIO->CRCCNF = ((RADIO_CRCCNF_SKIPADDR_Ieee802154 << RADIO_CRCCNF_SKIPADDR_Pos) |
                     (RADIO_CRCCNF_LEN_Two << RADIO_CRCCNF_LEN_Pos));
NRF_RADIO->CRCPOLY = 0x11021;
NRF_RADIO->CRCINIT = 0;
```

The ENDIANESS subregister must be set to little-endian since the FCS field is transmitted from left bit to right.

### 7.1.27.13.6 Transmit sequence

The transmission is started by first putting the RADIO in receive mode and triggering the **RXEN** task.

An outline of the IEEE 802.15.4 transmission is illustrated in the figure below.

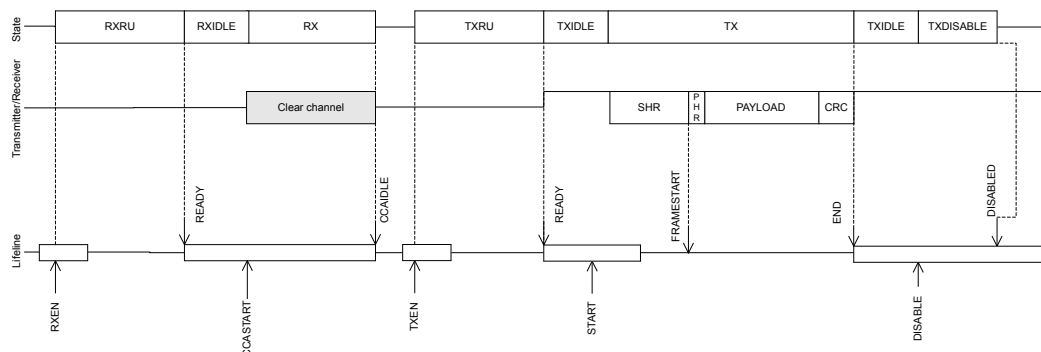


Figure 160: IEEE 802.15.4 transmit sequence

The receiver will ramp up and enter the RXIDLE state where the **READY** event is generated. Upon receiving the ready event, the CCA is started by triggering the **CCASTART** task. The chosen mode of assessment (**CCACTRL.CCAMODE** register) will be performed and signal the **CCAIDLE** or **CCABUSY** event 128 µs later. If the **CCABUSY** event is received, the RADIO will have to retry the CCA after a specific back-off period. This is outlined in the *IEEE 802.15.4 standard, Figure 69 in section 7.5.1.4 The CSMA-CA algorithm*.

If the **CCAIDLE** event is generated, a write to the **TXEN** task register enters the RADIO in TXRU state. The **READY** event will be generated when the RADIO is in TXIDLE state and ready to transmit. With the **PACKETPTR** pointing to the length (PHR) field of the frame, the **START** task can be written. The RADIO will send the four octet preamble sequence followed by the start of frame delimiter (**SFD** register). The first byte read from the Data RAM is the length field (PHR) followed by the transmission of the number of bytes indicated as the frame length. If the CRC module is configured it will run for PHR-2 octets. The last two octets will be substituted with the results from running the CRC. The necessary CRC parameters are sampled on the **START** task. The FCS field of the frame is little endian.

In addition to the already available shortcuts, one is provided between **READY** event and **CCASTART** task so that a CCA can automatically start when the receiver is ready. A second shortcut has been added between



CCAIDLE event and the TXEN task, so that upon detecting a clear channel the RADIO can immediately enter transmit mode.

### 7.1.27.13.7 Receive sequence

The reception is started by first putting the RADIO in receive mode. After writing to the RXEN task, the RADIO will start ramping up and enter the RXRU state.

When the READY event is generated, the RADIO enters the RXIDLE mode. For the baseband processing to be enabled, the START task must be written. An outline of the IEEE 802.15.4 reception can be found in the figure below.

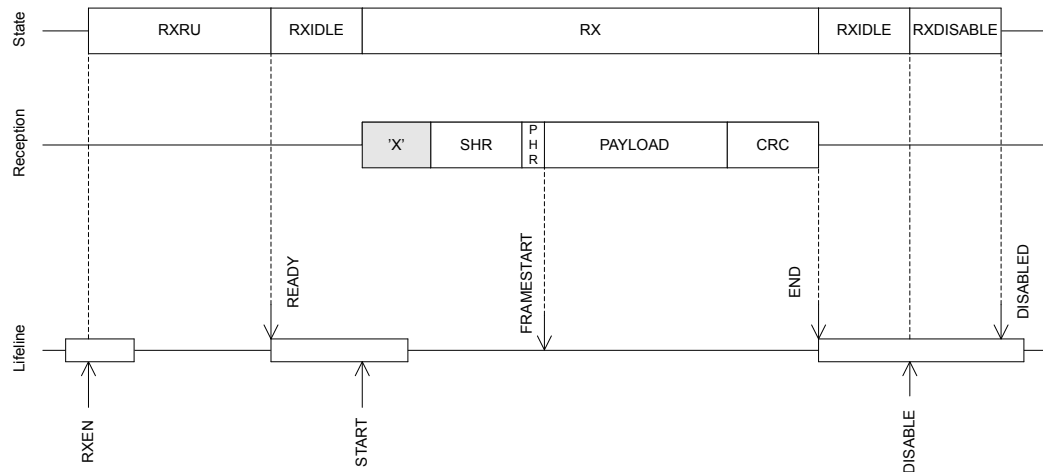


Figure 161: IEEE 802.15.4 receive sequence

When a valid SHR is received the RADIO will start storing future octets (starting with PHR) to the data memory pointed to by PACKETPTR. After the SFD octet is received the FRAMESTART event is generated. If the CRC module is enabled it will start updating with the second byte received (first byte in payload) and run for the full frame length. The two last bytes in the frame are not written to RAM when CRC is configured. However, if the result of the CRC after running the full frame is zero, the CRCOK event will be generated. The END event is generated when the last octet has been received and is available in data memory.

When a packet is received a link quality indicator (LQI) is also generated and appended immediately after the last received octet. When using an IEEE 802.15.4 compliant frame, this will be just after the MSDU since the FCS is not reported. In the case of a non-compliant frame it will be appended after the full frame. The LQI reported by hardware must be converted to IEEE 802.15.4 range by an 8-bit saturating multiplication by 4, as shown in IEEE 802.15.4 ED measurement example on page 425. The LQI is only valid for frames equal to or longer than three octets. When receiving a frame the RSSI (reported as negative dB) will be measured at three points during the reception. These three values will be sorted and the middle one selected (median 3) to be remapped within the LQI range. The following figure illustrates the LQI measurement and how the data is arranged in data memory.

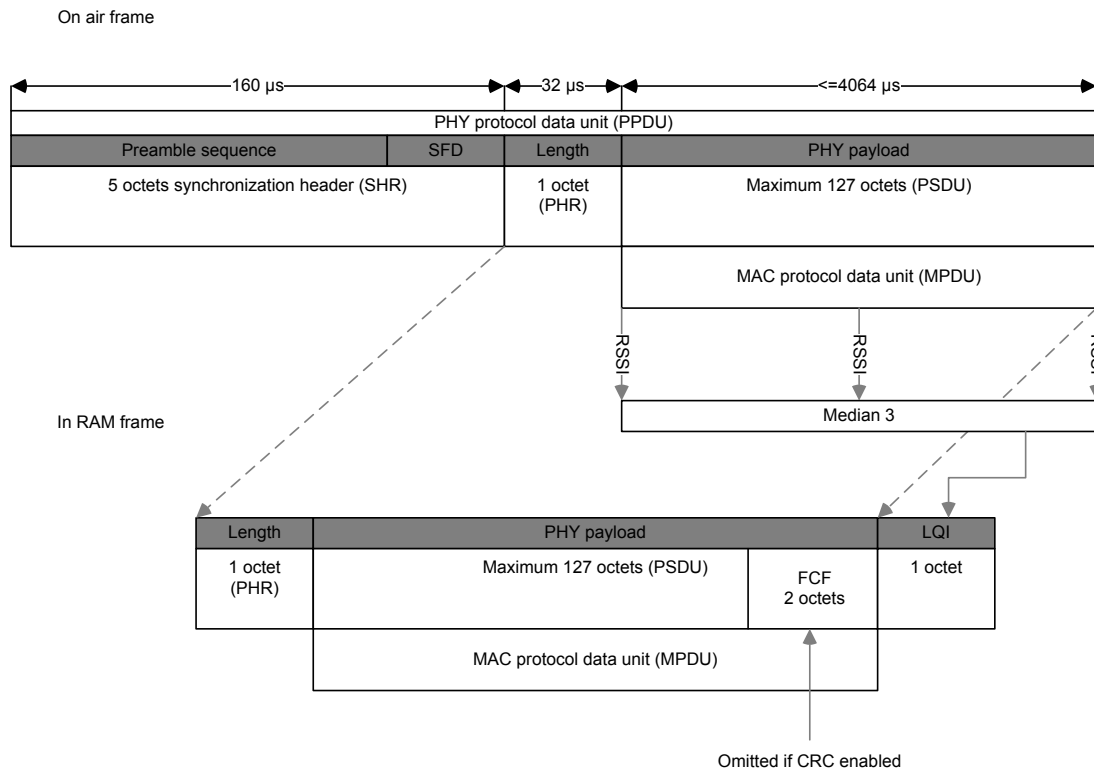


Figure 162: IEEE 802.15.4 frame in data memory

A shortcut has been added between the **FRAMESTART** event and the **BCSTART** task. This can be used to trigger a **BCMATCH** event after N bits, such as when inspecting the MAC addressing fields.

### 7.1.27.13.8 Interframe spacing (IFS)

The IEEE 802.15.4 standard defines a specific time that is allotted for the MAC sublayer to process received data. Interframe spacing (IFS) is used to prevent that two frames are transmitted too close together. If the transmission is requesting an acknowledgement, the space before the second frame shall be at least one IFS period.

The IFS is determined to be one of the following:

- IFS equals `macMinSIFSPeriod` (12 symbols) if the MPDU is less than or equal to `aMaxSIFSFrameSize` (18 octets) octets
- IFS equals `macMinLIFSPeriod` (40 symbols) if the MPDU is larger than `aMaxSIFSFrameSize`

Using the efficient assisted modes in the RADIO, the **TIFS** will be programmed with the correct value based on the frame being transmitted. If the assisted modes are not being used the user must update the **TIFS** register manually. The figure below provides details on what IFS period is valid in both acknowledged and unacknowledged transmissions.

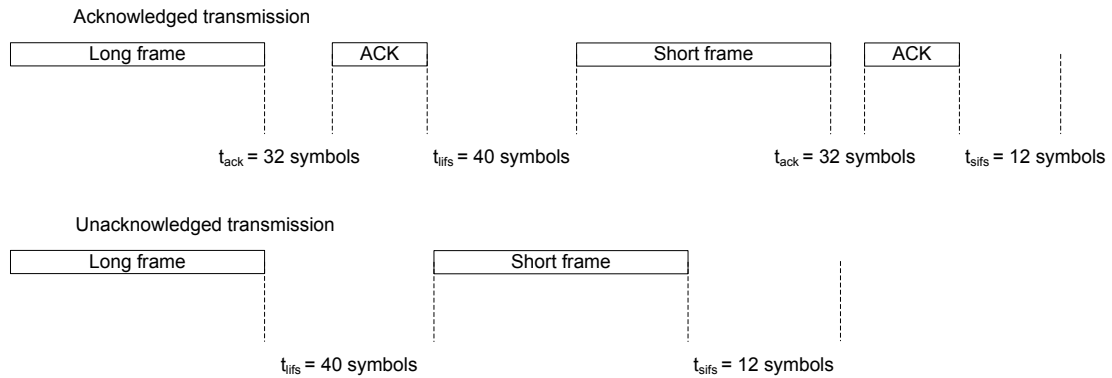


Figure 163: Interframe spacing examples

### 7.1.27.14 EasyDMA

The RADIO uses EasyDMA to read and write packets to RAM without CPU involvement.

As illustrated in [Figure 135: RADIO block diagram](#) on page 409, the RADIO's EasyDMA utilizes the same [PACKETPTR](#) for receiving and transmitting packets. This pointer should be reconfigured by the CPU each time before RADIO is started by the [START](#) task. The [PACKETPTR](#) register is double-buffered, meaning that it can be updated and prepared for the next transmission.

The [END](#) event indicates that the last bit has been processed by the RADIO. The [DISABLED](#) event is issued to acknowledge that a [DISABLE](#) task is done.

The structure of a packet is described in detail in [Packet configuration](#) on page 409. The data that is stored in Data RAM and transported by EasyDMA consists of the following fields:

- S0
- LENGTH
- S1
- PAYLOAD

In addition, a static add-on is sent immediately after the payload.

The size of each of the above fields in the frame is configurable (see [Packet configuration](#) on page 409), and the space occupied in RAM depends on these settings. The size of the field can be zero, as long as the resulting frame complies with the chosen RF protocol.

All fields are extended in size to align with a byte boundary in RAM. For instance, a 3-bit long field on air will occupy 1 byte in RAM while a 9-bit long field will be extended to 2 bytes.

The packet's elements can be configured as follows:

- CI, TERM1, and TERM2 fields are only present in *Bluetooth* Low Energy Long Range mode
- S0 is configured through the [PCNF0.SOLEN](#) field
- LENGTH is configured through the [PCNF0.LFLEN](#) field
- S1 is configured through the [PCNF0.S1LEN](#) field
- Payload size is configured through the value in RAM corresponding to the LENGTH field
- Static add-on size is configured through the [PCNF1.STATLEN](#) field

The [PCNF1.MAXLEN](#) field configures the maximum packet payload plus add-on size in number of bytes that can be transmitted or received by the RADIO. This feature can be used to ensure that the RADIO does not overwrite, or read beyond, the RAM assigned to the packet payload. This means that if the LENGTH field of the packet payload exceeds [PCNF1.STATLEN](#), and the LENGTH field in the packet specifies a packet larger than configured in [PCNF1.MAXLEN](#), the payload will be truncated to the length specified in [PCNF1.MAXLEN](#).

**Note:** The `PCNF1.MAXLEN` field includes the payload and the add-on, but excludes the size occupied by the `S0`, `LENGTH`, and `S1` fields. This has to be taken into account when allocating RAM.

If the payload and add-on length is specified larger than `PCNF1.MAXLEN`, the RADIO will still transmit or receive in the same way as before, except the payload is now truncated to `PCNF1.MAXLEN`. The packet's `LENGTH` field will not be altered when the payload is truncated. The RADIO will calculate CRC as if the packet length is equal to `PCNF1.MAXLEN`.

**Note:** If `PACKETPTR` is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See [Memory](#) on page 18 for more information about the different memory regions.

The `END` event indicates that the last bit has been processed by the RADIO. The `DISABLED` event is issued to acknowledge that an `DISABLE` task is done.

### 7.1.27.15 Registers

| Base address | Domain  | Peripheral | Instance | Secure mapping | DMA security | Description   | Configuration |
|--------------|---------|------------|----------|----------------|--------------|---------------|---------------|
| 0x41008000   | NETWORK | RADIO      | RADIO    | NS             | NA           | 2.4 GHz radio |               |

Table 130: Instances

| Register                         | Offset | Security | Description                                                              |
|----------------------------------|--------|----------|--------------------------------------------------------------------------|
| <code>TASKS_TXEN</code>          | 0x000  |          | Enable RADIO in TX mode                                                  |
| <code>TASKS_RXEN</code>          | 0x004  |          | Enable RADIO in RX mode                                                  |
| <code>TASKS_START</code>         | 0x008  |          | Start RADIO                                                              |
| <code>TASKS_STOP</code>          | 0x00C  |          | Stop RADIO                                                               |
| <code>TASKS_DISABLE</code>       | 0x010  |          | Disable RADIO                                                            |
| <code>TASKS_RSSISTART</code>     | 0x014  |          | Start the RSSI and take one single sample of the receive signal strength |
| <code>TASKS_RSSISTOP</code>      | 0x018  |          | Stop the RSSI measurement                                                |
| <code>TASKS_BCSTART</code>       | 0x01C  |          | Start the bit counter                                                    |
| <code>TASKS_BCSTOP</code>        | 0x020  |          | Stop the bit counter                                                     |
| <code>TASKS_EDSTART</code>       | 0x024  |          | Start the energy detect measurement used in IEEE 802.15.4 mode           |
| <code>TASKS_EDSTOP</code>        | 0x028  |          | Stop the energy detect measurement                                       |
| <code>TASKS_CCASTART</code>      | 0x02C  |          | Start the clear channel assessment used in IEEE 802.15.4 mode            |
| <code>TASKS_CCASTOP</code>       | 0x030  |          | Stop the clear channel assessment                                        |
| <code>SUBSCRIBE_TXEN</code>      | 0x080  |          | Subscribe configuration for task <code>TXEN</code>                       |
| <code>SUBSCRIBE_RXEN</code>      | 0x084  |          | Subscribe configuration for task <code>RXEN</code>                       |
| <code>SUBSCRIBE_START</code>     | 0x088  |          | Subscribe configuration for task <code>START</code>                      |
| <code>SUBSCRIBE_STOP</code>      | 0x08C  |          | Subscribe configuration for task <code>STOP</code>                       |
| <code>SUBSCRIBE_DISABLE</code>   | 0x090  |          | Subscribe configuration for task <code>DISABLE</code>                    |
| <code>SUBSCRIBE_RSSISTART</code> | 0x094  |          | Subscribe configuration for task <code>RSSISTART</code>                  |
| <code>SUBSCRIBE_RSSISTOP</code>  | 0x098  |          | Subscribe configuration for task <code>RSSISTOP</code>                   |
| <code>SUBSCRIBE_BCSTART</code>   | 0x09C  |          | Subscribe configuration for task <code>BCSTART</code>                    |
| <code>SUBSCRIBE_BCSTOP</code>    | 0x0A0  |          | Subscribe configuration for task <code>BCSTOP</code>                     |
| <code>SUBSCRIBE_EDSTART</code>   | 0x0A4  |          | Subscribe configuration for task <code>EDSTART</code>                    |
| <code>SUBSCRIBE_EDSTOP</code>    | 0x0A8  |          | Subscribe configuration for task <code>EDSTOP</code>                     |
| <code>SUBSCRIBE_CCASTART</code>  | 0x0AC  |          | Subscribe configuration for task <code>CCASTART</code>                   |
| <code>SUBSCRIBE_CCASTOP</code>   | 0x0B0  |          | Subscribe configuration for task <code>CCASTOP</code>                    |
| <code>EVENTS_READY</code>        | 0x100  |          | RADIO has ramped up and is ready to be started                           |
| <code>EVENTS_ADDRESS</code>      | 0x104  |          | Address sent or received                                                 |
| <code>EVENTS_PAYLOAD</code>      | 0x108  |          | Packet payload sent or received                                          |
| <code>EVENTS_END</code>          | 0x10C  |          | Packet sent or received                                                  |

| Register           | Offset | Security | Description                                                                                                  |
|--------------------|--------|----------|--------------------------------------------------------------------------------------------------------------|
| EVENTS_DISABLED    | 0x110  |          | RADIO has been disabled                                                                                      |
| EVENTS_DEVMATCH    | 0x114  |          | A device address match occurred on the last received packet                                                  |
| EVENTS_DEVMISS     | 0x118  |          | No device address match occurred on the last received packet                                                 |
| EVENTS_RSSIEND     | 0x11C  |          | Sampling of receive signal strength complete                                                                 |
| EVENTS_BCMATCH     | 0x128  |          | Bit counter reached bit count value                                                                          |
| EVENTS_CRCOK       | 0x130  |          | Packet received with CRC ok                                                                                  |
| EVENTS_CRCERROR    | 0x134  |          | Packet received with CRC error                                                                               |
| EVENTS_FRAMESTART  | 0x138  |          | IEEE 802.15.4 length field received                                                                          |
| EVENTS_EDEND       | 0x13C  |          | Sampling of energy detection complete. A new ED sample is ready for readout from the RADIO.EDSAMPLE register |
| EVENTS_EDSTOPPED   | 0x140  |          | The sampling of energy detection has stopped                                                                 |
| EVENTS_CCAIDLE     | 0x144  |          | Wireless medium in idle - clear to send                                                                      |
| EVENTS_CCABUSY     | 0x148  |          | Wireless medium busy - do not send                                                                           |
| EVENTS_CCASTOPPED  | 0x14C  |          | The CCA has stopped                                                                                          |
| EVENTS_RATEBOOST   | 0x150  |          | Ble_LR CI field received, receive mode is changed from Ble_LR125Kbit to Ble_LR500Kbit.                       |
| EVENTS_TXREADY     | 0x154  |          | RADIO has ramped up and is ready to be started TX path                                                       |
| EVENTS_RXREADY     | 0x158  |          | RADIO has ramped up and is ready to be started RX path                                                       |
| EVENTS_MHRMATCH    | 0x15C  |          | MAC header match found                                                                                       |
| EVENTS_PHYEND      | 0x16C  |          | Generated when last bit is sent on air                                                                       |
| EVENTS_CTEPRESENT  | 0x170  |          | CTE is present (early warning right after receiving CTEInfo byte)                                            |
| PUBLISH_READY      | 0x180  |          | Publish configuration for event <a href="#">READY</a>                                                        |
| PUBLISH_ADDRESS    | 0x184  |          | Publish configuration for event <a href="#">ADDRESS</a>                                                      |
| PUBLISH_PAYLOAD    | 0x188  |          | Publish configuration for event <a href="#">PAYLOAD</a>                                                      |
| PUBLISH_END        | 0x18C  |          | Publish configuration for event <a href="#">END</a>                                                          |
| PUBLISH_DISABLED   | 0x190  |          | Publish configuration for event <a href="#">DISABLED</a>                                                     |
| PUBLISH_DEVMATCH   | 0x194  |          | Publish configuration for event <a href="#">DEVMATCH</a>                                                     |
| PUBLISH_DEVMISS    | 0x198  |          | Publish configuration for event <a href="#">DEVMISS</a>                                                      |
| PUBLISH_RSSIEND    | 0x19C  |          | Publish configuration for event <a href="#">RSSIEND</a>                                                      |
| PUBLISH_BCMATCH    | 0x1A8  |          | Publish configuration for event <a href="#">BCMATCH</a>                                                      |
| PUBLISH_CRCOK      | 0x1B0  |          | Publish configuration for event <a href="#">CRCOK</a>                                                        |
| PUBLISH_CRCERROR   | 0x1B4  |          | Publish configuration for event <a href="#">CRCERROR</a>                                                     |
| PUBLISH_FRAMESTART | 0x1B8  |          | Publish configuration for event <a href="#">FRAMESTART</a>                                                   |
| PUBLISH_EDEND      | 0x1BC  |          | Publish configuration for event <a href="#">EDEND</a>                                                        |
| PUBLISH_EDSTOPPED  | 0x1C0  |          | Publish configuration for event <a href="#">EDSTOPPED</a>                                                    |
| PUBLISH_CCAIDLE    | 0x1C4  |          | Publish configuration for event <a href="#">CCAIDLE</a>                                                      |
| PUBLISH_CCABUSY    | 0x1C8  |          | Publish configuration for event <a href="#">CCABUSY</a>                                                      |
| PUBLISH_CCASTOPPED | 0x1CC  |          | Publish configuration for event <a href="#">CCASTOPPED</a>                                                   |
| PUBLISH_RATEBOOST  | 0x1D0  |          | Publish configuration for event <a href="#">RATEBOOST</a>                                                    |
| PUBLISH_TXREADY    | 0x1D4  |          | Publish configuration for event <a href="#">TXREADY</a>                                                      |
| PUBLISH_RXREADY    | 0x1D8  |          | Publish configuration for event <a href="#">RXREADY</a>                                                      |
| PUBLISH_MHRMATCH   | 0x1DC  |          | Publish configuration for event <a href="#">MHRMATCH</a>                                                     |
| PUBLISH_PHYEND     | 0x1EC  |          | Publish configuration for event <a href="#">PHYEND</a>                                                       |
| PUBLISH_CTEPRESENT | 0x1F0  |          | Publish configuration for event <a href="#">CTEPRESENT</a>                                                   |
| SHORTS             | 0x200  |          | Shortcuts between local events and tasks                                                                     |
| INTENSET           | 0x304  |          | Enable interrupt                                                                                             |
| INTENCLR           | 0x308  |          | Disable interrupt                                                                                            |
| CRCSTATUS          | 0x400  |          | CRC status                                                                                                   |
| RXMATCH            | 0x408  |          | Received address                                                                                             |
| RXCRC              | 0x40C  |          | CRC field of previously received packet                                                                      |
| DAI                | 0x410  |          | Device address match index                                                                                   |
| PDUSTAT            | 0x414  |          | Payload status                                                                                               |
| CTESTATUS          | 0x44C  |          | CTEInfo parsed from received packet                                                                          |

| Register         | Offset | Security | Description                                                       |
|------------------|--------|----------|-------------------------------------------------------------------|
| DFESTATUS        | 0x458  |          | DFE status information                                            |
| PACKETPTR        | 0x504  |          | Packet pointer                                                    |
| FREQUENCY        | 0x508  |          | Frequency                                                         |
| TXPOWER          | 0x50C  |          | Output power                                                      |
| MODE             | 0x510  |          | Data rate and modulation                                          |
| PCNF0            | 0x514  |          | Packet configuration register 0                                   |
| PCNF1            | 0x518  |          | Packet configuration register 1                                   |
| BASE0            | 0x51C  |          | Base address 0                                                    |
| BASE1            | 0x520  |          | Base address 1                                                    |
| PREFIX0          | 0x524  |          | Prefixes bytes for logical addresses 0-3                          |
| PREFIX1          | 0x528  |          | Prefixes bytes for logical addresses 4-7                          |
| TXADDRESS        | 0x52C  |          | Transmit address select                                           |
| RXADDRESSES      | 0x530  |          | Receive address select                                            |
| CRCCNF           | 0x534  |          | CRC configuration                                                 |
| CRCPOLY          | 0x538  |          | CRC polynomial                                                    |
| CRCINIT          | 0x53C  |          | CRC initial value                                                 |
| TIFS             | 0x544  |          | Interframe spacing in $\mu$ s                                     |
| RSSISAMPLE       | 0x548  |          | RSSI sample                                                       |
| STATE            | 0x550  |          | Current radio state                                               |
| DATAWHITEIV      | 0x554  |          | Data whitening initial value                                      |
| BCC              | 0x560  |          | Bit counter compare                                               |
| DAB[n]           | 0x600  |          | Device address base segment n                                     |
| DAP[n]           | 0x620  |          | Device address prefix n                                           |
| DACNF            | 0x640  |          | Device address match configuration                                |
| MHRMATCHCONF     | 0x644  |          | Search pattern configuration                                      |
| MHRMATCHMAS      | 0x648  |          | Pattern mask                                                      |
| MODECNF0         | 0x650  |          | Radio mode configuration register 0                               |
| SFD              | 0x660  |          | IEEE 802.15.4 start of frame delimiter                            |
| EDCNT            | 0x664  |          | IEEE 802.15.4 energy detect loop count                            |
| EDSAMPLE         | 0x668  |          | IEEE 802.15.4 energy detect level                                 |
| CCACTRL          | 0x66C  |          | IEEE 802.15.4 clear channel assessment control                    |
| DFEMODE          | 0x900  |          | Whether to use Angle-of-Arrival (AOA) or Angle-of-Departure (AOD) |
| CTEINLINECONF    | 0x904  |          | Configuration for CTE inline mode                                 |
| DFECTRL1         | 0x910  |          | Various configuration for Direction finding                       |
| DFECTRL2         | 0x914  |          | Start offset for Direction finding                                |
| SWITCHPATTERN    | 0x928  |          | GPIO patterns to be used for each antenna                         |
| CLEARPATTERN     | 0x92C  |          | Clear the GPIO pattern array for antenna control                  |
| PSEL.DFEGPIO[n]  | 0x930  |          | Pin select for DFE pin n                                          |
| DFEPACKET.PTR    | 0x950  |          | Data pointer                                                      |
| DFEPACKET.MAXCNT | 0x954  |          | Maximum number of buffer words to transfer                        |
| DFEPACKET.AMOUNT | 0x958  |          | Number of samples transferred in the last transaction             |
| POWER            | 0xFFC  |          | Peripheral power control                                          |

Table 131: Register overview

### 7.1.27.15.1 TASKS\_TXEN

Address offset: 0x000

Enable RADIO in TX mode

|                  |            |            |  |          |   |  |       |  |  |             |                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|------------|--|----------|---|--|-------|--|--|-------------|-------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |            |  |          |   |  |       |  |  | 31          | 30                      | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |            |  |          |   |  |       |  |  |             |                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |   |
| Reset 0x00000000 |            |            |  |          |   |  |       |  |  | 0           | 0                       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |            |  | Value ID |   |  | Value |  |  | Description |                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_TXEN |  |          |   |  |       |  |  |             | Enable RADIO in TX mode |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Trigger    |  |          | 1 |  |       |  |  |             | Trigger task            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.27.15.2 TASKS\_RXEN

Address offset: 0x004

### Enable RADIO in RX mode

|                  |            |            |  |          |   |  |       |  |  |             |                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|------------|--|----------|---|--|-------|--|--|-------------|-------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |            |  |          |   |  |       |  |  | 31          | 30                      | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |            |  |          |   |  |       |  |  | A           |                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |            |  |          |   |  |       |  |  | 0           | 0                       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |            |  | Value ID |   |  | Value |  |  | Description |                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_RXEN |  |          |   |  |       |  |  |             | Enable RADIO in RX mode |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Trigger    |  |          | 1 |  |       |  |  |             | Trigger task            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.27.15.3 TASKS\_START

Address offset: 0x008

Start RADIO

|                  |            |             |          |              |    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-------------|----------|--------------|----|----|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |             |          | 31           | 30 | 29 | 28          | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |             |          | A            |    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |             |          | 0            | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |             | Value ID | Value        |    |    | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_START |          |              |    |    | Start RADIO |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Trigger     | 1        | Trigger task |    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 7.1.27.15.4 TASKS\_STOP

Address offset: 0x00C

Stop RADIO

|                  |            |            |  |          |   |  |       |  |  |             |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|------------|--|----------|---|--|-------|--|--|-------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |            |  |          |   |  |       |  |  | 31          | 30           | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |            |  |          |   |  |       |  |  | A           |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |            |  |          |   |  |       |  |  | 0           | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |            |  | Value ID |   |  | Value |  |  | Description |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_STOP |  |          |   |  |       |  |  |             | Stop RADIO   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Trigger    |  |          | 1 |  |       |  |  |             | Trigger task |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.27.15.5 TASKS DISABLE

Address offset: 0x010

## Disable RADIO

|                  |            |               |          |   |       |              |             |               |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|---------------|----------|---|-------|--------------|-------------|---------------|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |               |          |   |       |              |             |               |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |               |          |   |       |              |             |               |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |
| Reset 0x00000000 |            |               |          |   |       |              |             |               |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |               | Value ID |   | Value |              | Description |               |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_DISABLE |          |   |       |              |             | Disable RADIO |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Trigger       |          | 1 |       | Trigger task |             |               |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.27.15.6 TASKS\_RSSISTART

Address offset: 0x014

Start the RSSI and take one single sample of the receive signal strength

|                  |            |                 |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|-----------------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |                 |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |                 |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |                 |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID        | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W          | TASKS_RSSISTART |       | Start the RSSI and take one single sample of the receive signal strength              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Trigger         | 1     | Trigger task                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.27.15.7 TASKS\_RSSISTOP

Address offset: 0x018

Stop the RSSI measurement

|                  |            |                |  |          |   |  |       |  |  |             |                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------------|--|----------|---|--|-------|--|--|-------------|---------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                |  |          |   |  |       |  |  | 31          | 30                        | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |                |  |          |   |  |       |  |  |             |                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |   |
| Reset 0x00000000 |            |                |  |          |   |  |       |  |  | 0           | 0                         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |                |  | Value ID |   |  | Value |  |  | Description |                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_RSSISTOP |  |          |   |  |       |  |  |             | Stop the RSSI measurement |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Trigger        |  |          | 1 |  |       |  |  |             | Trigger task              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.27.15.8 TASKS\_BCSTART

Address offset: 0x01C

Start the bit counter

|                  |            |                                                                                       |  |       |  |                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|---------------------------------------------------------------------------------------|--|-------|--|-----------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |       |  |                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            | A                                                                                     |  |       |  |                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |  |       |  |                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID                                                                              |  | Value |  | Description           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W          | TASKS_BCSTART                                                                         |  |       |  | Start the bit counter |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Trigger                                                                               |  | 1     |  | Trigger task          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.27.15.9 TASKS\_BCSTOP

Address offset: 0x020

Stop the bit counter



|                  |            |              |          |   |       |              |             |                      |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------------|----------|---|-------|--------------|-------------|----------------------|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |              |          |   |       |              |             |                      |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |              |          |   |       |              |             |                      |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |   |
| Reset 0x00000000 |            |              |          |   |       |              |             |                      |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |              | Value ID |   | Value |              | Description |                      |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_BCSTOP |          |   |       |              |             | Stop the bit counter |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Trigger      |          | 1 |       | Trigger task |             |                      |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.27.15.10 TASKS\_EDSTART

Address offset: 0x024

Start the energy detect measurement used in IEEE 802.15.4 mode

|                  |            |               |          |   |       |              |             |                                                                |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|---------------|----------|---|-------|--------------|-------------|----------------------------------------------------------------|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |               |          |   |       |              |             |                                                                |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |               |          |   |       |              |             |                                                                |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |   |
| Reset 0x00000000 |            |               |          |   |       |              |             |                                                                |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |               | Value ID |   | Value |              | Description |                                                                |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_EDSTART |          |   |       |              |             | Start the energy detect measurement used in IEEE 802.15.4 mode |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Trigger       |          | 1 |       | Trigger task |             |                                                                |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.27.15.11 TASKS\_EDSTOP

Address offset: 0x028

Stop the energy detect measurement

|                  |            |              |  |          |   |  |       |              |  |             |                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------------|--|----------|---|--|-------|--------------|--|-------------|------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |              |  |          |   |  |       |              |  | 31          | 30                                 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |              |  |          |   |  |       |              |  |             |                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |
| Reset 0x00000000 |            |              |  |          |   |  |       |              |  | 0           | 0                                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |              |  | Value ID |   |  | Value |              |  | Description |                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_EDSTOP |  |          |   |  |       |              |  |             | Stop the energy detect measurement |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Trigger      |  |          | 1 |  |       | Trigger task |  |             |                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.27.15.12 TASKS\_CCASTART

Address offset: 0x02C

Start the clear channel assessment used in IEEE 802.15.4 mode

|                  |            |                |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |                |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |                |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |                |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID       | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W          | TASKS_CCASTART |       | Start the clear channel assessment used in IEEE 802.15.4 mode                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Trigger        | 1     | Trigger task                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.27.15.13 TASKS\_CCASTOP

Address offset: 0x030

Stop the clear channel assessment

| Bit number       |            | 31                                                                | 30 | 29      | 28 | 27          | 26 | 25                                | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------|------------|-------------------------------------------------------------------|----|---------|----|-------------|----|-----------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| ID               |            |                                                                   |    |         |    |             |    |                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | A |
| Reset 0x00000000 |            | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |    |         |    |             |    |                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | 0 |
| ID               | Acce Field | Value ID                                                          |    | Value   |    | Description |    |                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_CCASTOP                                                     |    | Trigger |    | 1           |    | Stop the clear channel assessment |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |                                                                   |    |         |    |             |    | Trigger task                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.27.15.14 SUBSCRIBE\_TXEN

Address offset: 0x080

Subscribe configuration for task **TXEN**

|                  |            |  |  |          |  |  |          |  |  |                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|--|----------|--|--|----------|--|--|-------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |  |          |  |  |          |  |  | 31                                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |
| ID               |            |  |  |          |  |  |          |  |  | B                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  |    |    |    |   |   |   |   |   |   | A | A | A | A | A | A | A |   |
| Reset 0x00000000 |            |  |  |          |  |  |          |  |  | 0                                               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  |  | Value ID |  |  | Value    |  |  | Description                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |  |          |  |  | [255..0] |  |  | Channel that task <b>TXEN</b> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |  |          |  |  |          |  |  |                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  |  | Disabled |  |  | 0        |  |  | Disable subscription                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  |  | Enabled  |  |  | 1        |  |  | Enable subscription                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.27.15.15 SUBSCRIBE\_RXEN

Address offset: 0x084

Subscribe configuration for task **RXEN**

|                  |            |  |          |                                                                           |    |                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|---------------------------------------------------------------------------|----|-------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31                                                                        | 30 | 29                                              | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |  |          | B                                                                         |    |                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |    |                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field |  | Value ID | Value                                                                     |    | Description                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          | [255..0]                                                                  |    | Channel that task <b>RXEN</b> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |                                                                           |    |                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled | 0                                                                         |    | Disable subscription                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  | 1                                                                         |    | Enable subscription                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.27.15.16 SUBSCRIBE\_START

Address offset: 0x088

Subscribe configuration for task **START**

|                  |            |          |                                                                                       |  |                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|--|--------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          | B A A A A A A A                                                                       |  |                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |  |                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 |  | Description                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                              |  | Channel that task <span>START</span> will subscribe to |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW EN      |          |                                                                                       |  |                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     |  | Disable subscription                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     |  | Enable subscription                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.27.15.17 SUBSCRIBE\_STOP

Address offset: 0x08C

Subscribe configuration for task **STOP**

|                  |            |          |                                                                                       |                      |                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|----------------------|-------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                      |                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |          | B                                                                                     |                      |                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |                      |                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 |                      | Description                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                              |                      | Channel that task <span>STOP</span> will subscribe to |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |                                                                                       |                      |                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Disable subscription |                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Enable subscription  |                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

## 7.1.27.15.18 SUBSCRIBE\_DISABLE

Address offset: 0x090

Subscribe configuration for task **DISABLE**

|                  |            |          |          |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|----------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |          |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |          |          | B                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value    | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0] | Channel that task <span>DISABLE</span> will subscribe to                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |          |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0        | Disable subscription                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1        | Enable subscription                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

## 7.1.27.15.19 SUBSCRIBE\_RSSISTART

Address offset: 0x094

Subscribe configuration for task **RSSISTART**

|                  |            |          |                                                                                       |  |                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|--|------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |          | B                                                                                     |  |                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |  |                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 |  | Description                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                              |  | Channel that task <span>RSSISTART</span> will subscribe to |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |                                                                                       |  |                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     |  | Disable subscription                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     |  | Enable subscription                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

## 7.1.27.15.20 SUBSCRIBE\_RSSISTOP

Address offset: 0x098

Subscribe configuration for task **RSSISTOP**

|                  |            |          |          |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|-----------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                                                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |          |          | B                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   |   |   |   |   |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |          |          | 0                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID | Value    | Description                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] | Channel that task <b>RSSISTOP</b> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        | Disable subscription                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        | Enable subscription                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.27.15.21 SUBSCRIBE\_BCSTART

Address offset: 0x09C

Subscribe configuration for task **BCSTART**

|                  |            |  |          |  |          |  |                                                    |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|--|----------|--|----------------------------------------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          |  |          |  |                                                    |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |  |          |  |          |  |                                                    |  |  | B  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  | A  | A | A | A | A | A | A |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |          |  |          |  |                                                    |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID |  | Value    |  | Description                                        |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          |  | [255..0] |  | Channel that task <b>BCSTART</b> will subscribe to |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |  |          |  |                                                    |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled |  | 0        |  | Disable subscription                               |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  |  | 1        |  | Enable subscription                                |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.27.15.22 SUBSCRIBE\_BCSTOP

Address offset: 0x0A0

Subscribe configuration for task **BCSTOP**

|                  |            |  |          |          |    |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|----------|----|---------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31       | 30 | 29                                                | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |  |          | B        |    |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   |   |   |   |   |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |          | 0        |    |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID | Value    |    | Description                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          | [255..0] |    | Channel that task <b>BCSTOP</b> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |          |    |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled | 0        |    | Disable subscription                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  | 1        |    | Enable subscription                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.27.15.23 SUBSCRIBE\_EDSTART

Address offset: 0x0A4

Subscribe configuration for task **EDSTART**

|                  |            |       |          |          |                      |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-------|----------|----------|----------------------|----------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |       |          | 31       | 30                   | 29                                                 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |       |          | B        |                      |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   |   |   |   |   |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |       |          | 0        |                      |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |       | Value ID | Value    |                      | Description                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | CHIDX |          | [255..0] |                      | Channel that task <b>EDSTART</b> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW         | EN    |          |          |                      |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |       | Disabled | 0        | Disable subscription |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |       | Enabled  | 1        | Enable subscription  |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.27.15.24 SUBSCRIBE\_EDSTOP

Address offset: 0x0A8

Subscribe configuration for task **EDSTOP**

|                  |            |          |                                                                                       |                      |                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|----------------------|---------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                      |                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |          | B                                                                                     |                      |                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                      |                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 |                      | Description                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                              |                      | Channel that task <b>EDSTOP</b> will subscribe to |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |                                                                                       |                      |                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Disable subscription |                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Enable subscription  |                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

### 7.1.27.15.25 SUBSCRIBE\_CCASTART

Address offset: 0x0AC

Subscribe configuration for task **CCASTART**

|                  |            |          |                                                                                       |                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|----------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |          | B                                                                                     |                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                              | Channel that task CCASTART will subscribe to |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |                                                                                       |                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Disable subscription                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Enable subscription                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

### 7.1.27.15.26 SUBSCRIBE\_CCASTOP

Address offset: 0x0B0

Subscribe configuration for task **CCASTOP**

|                  |            |          |                                                                                       |                      |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|----------------------|----------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                      |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |          | B                                                                                     |                      |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                      |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 |                      | Description                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                              |                      | Channel that task <b>CCASTOP</b> will subscribe to |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |                                                                                       |                      |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Disable subscription |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Enable subscription  |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

### 7.1.27.15.27 EVENTS\_READY

Address offset: 0x100

RADIO has ramped up and is ready to be started

|                  |            |              |       |                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|------------------|------------|--------------|-------|------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|---|
| Bit number       |            |              |       | 31                                             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |   |
| ID               |            |              |       |                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | A |
| Reset 0x00000000 |            |              |       | 0                                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |   |
| ID               | Acce Field | Value ID     | Value | Description                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
| A                | RW         | EVENTS_READY |       | RADIO has ramped up and is ready to be started |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | NotGenerated | 0     | Event not generated                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | Generated    | 1     | Event generated                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |

### 7.1.27.15.28 EVENTS\_ADDRESS

Address offset: 0x104

Address sent or received

|                  |            |                |          |              |       |                          |                     |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------------|----------|--------------|-------|--------------------------|---------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                |          |              |       |                          |                     |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |                |          |              |       |                          |                     |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |
| Reset 0x00000000 |            |                |          |              |       |                          |                     |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |                | Value ID |              | Value |                          | Description         |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | EVENTS_ADDRESS |          |              |       | Address sent or received |                     |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |                |          | NotGenerated |       | 0                        | Event not generated |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |                |          | Generated    |       | 1                        | Event generated     |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.27.15.29 EVENTS\_PAYLOAD

Address offset: 0x108

Packet payload sent or received

|                  |            |                |       |                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|------------------|------------|----------------|-------|---------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|---|
| Bit number       |            |                |       | 31                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |   |
| ID               |            |                |       |                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | A |
| Reset 0x00000000 |            |                |       | 0                               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |   |
| ID               | Acce Field | Value ID       | Value | Description                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
| A                | RW         | EVENTS_PAYLOAD |       | Packet payload sent or received |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | NotGenerated   | 0     | Event not generated             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | Generated      | 1     | Event generated                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |

### 7.1.27.15.30 EVENTS\_END

Address offset: 0x10C

Packet sent or received

|                  |            |              |       |                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------------|-------|-------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |              |       | 31                      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |              |       |                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |
| Reset 0x00000000 |            |              |       | 0                       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |
| ID               | Acce Field | Value ID     | Value | Description             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | EVENTS_END   |       | Packet sent or received |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | NotGenerated | 0     | Event not generated     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Generated    | 1     | Event generated         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.27.15.31 EVENTS\_DISABLED

Address offset: 0x110

RADIO has been disabled

|                  |            |                 |       |                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|------------------|------------|-----------------|-------|-------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|---|
| Bit number       |            |                 |       | 31                      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |   |
| ID               |            |                 |       |                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  | A |
| Reset 0x00000000 |            |                 |       | 0                       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |   |
| ID               | Acce Field | Value ID        | Value | Description             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
| A                | RW         | EVENTS_DISABLED |       | RADIO has been disabled |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|                  |            | NotGenerated    | 0     | Event not generated     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|                  |            | Generated       | 1     | Event generated         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |

### 7.1.27.15.32 EVENTS\_DEVMATCH

Address offset: 0x114

A device address match occurred on the last received packet

|                  |            |  |                 |  |       |  |                                                             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|-----------------|--|-------|--|-------------------------------------------------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |                 |  |       |  |                                                             |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |  |                 |  |       |  |                                                             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |   |
| Reset 0x00000000 |            |  |                 |  |       |  |                                                             |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID        |  | Value |  | Description                                                 |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         |  | EVENTS_DEVMATCH |  |       |  | A device address match occurred on the last received packet |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | NotGenerated    |  | 0     |  | Event not generated                                         |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Generated       |  | 1     |  | Event generated                                             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.27.15.33 EVENTS\_DEVMISS

Address offset: 0x118

No device address match occurred on the last received packet

|                  |      |                |              |    |       |                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|------------------|------|----------------|--------------|----|-------|--------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|--|
| Bit number       |      |                |              | 31 | 30    | 29                                                           | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |
| ID               |      |                |              | A  |       |                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| Reset 0x00000000 |      |                |              | 0  | 0     | 0                                                            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |  |
| ID               | Acce | Field          | Value        | ID | Value | Description                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| A                | RW   | EVENTS_DEVMISS |              |    |       | No device address match occurred on the last received packet |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |      |                | NotGenerated | 0  |       | Event not generated                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |      |                | Generated    | 1  |       | Event generated                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |

### 7.1.27.15.34 EVENTS\_RSSIEND

Address offset: 0x11C

Sampling of receive signal strength complete

A new RSSI sample is ready for readout from the RADIO.RSSISAMPLE register

|                  |            |                |       |                                                                              |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |
|------------------|------------|----------------|-------|------------------------------------------------------------------------------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|---|--|
| Bit number       |            |                | 31    | 30                                                                           | 29          | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |   |  |
| ID               |            |                |       |                                                                              |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  | A |  |
| Reset 0x00000000 |            |                | 0     | 0                                                                            | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |   |  |
| ID               | Acce Field | Value ID       | Value |                                                                              | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |
| A                | RW         | EVENTS_RSSIEND |       | Sampling of receive signal strength complete                                 |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |
|                  |            |                |       | A new RSSI sample is ready for readout from the<br>RADIO.RSSISAMPLE register |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |
|                  |            | NotGenerated   | 0     | Event not generated                                                          |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |
|                  |            | Generated      | 1     | Event generated                                                              |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |

### 7.1.27.15.35 EVENTS\_BCMATCH

Address offset: 0x128

Bit counter reached bit count value

Bit counter value is specified in the RADIO.BCC register

|                  |            |                |                                                                                       |                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------------|---------------------------------------------------------------------------------------|----------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |                | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |                | A                                                                                     |                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |                | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID       | Value                                                                                 | Description                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | EVENTS_BCMATCH |                                                                                       | Bit counter reached bit count value                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |                |                                                                                       | Bit counter value is specified in the RADIO.BCC register |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | NotGenerated   | 0                                                                                     | Event not generated                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Generated      | 1                                                                                     | Event generated                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.27.15.36 EVENTS\_CRCOK

Address offset: 0x130

Packet received with CRC ok

|                  |            |              |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|--------------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |              |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |              |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |              |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID     | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | EVENTS_CRCOK |       | Packet received with CRC ok                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | NotGenerated | 0     | Event not generated                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Generated    | 1     | Event generated                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.27.15.37 EVENTS\_CRCERROR

Address offset: 0x134

Packet received with CRC error

|                  |            |                 |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|-----------------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |                 |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |                 |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |                 |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID        | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | EVENTS_CRCERROR |       | Packet received with CRC error                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | NotGenerated    | 0     | Event not generated                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Generated       | 1     | Event generated                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.27.15.38 EVENTS\_FRAMESTART

Address offset: 0x138

IEEE 802.15.4 length field received



|                  |            |                   |          |              |       |                                     |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-------------------|----------|--------------|-------|-------------------------------------|-------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                   |          |              |       |                                     |             |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |                   |          |              |       |                                     |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |   |
| Reset 0x00000000 |            |                   |          |              |       |                                     |             |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |                   | Value ID |              | Value |                                     | Description |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | EVENTS_FRAMESTART |          |              |       | IEEE 802.15.4 length field received |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |                   |          | NotGenerated | 0     | Event not generated                 |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |                   |          | Generated    | 1     | Event generated                     |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.27.15.39 EVENTS\_EDEND

Address offset: 0x13C

Sampling of energy detection complete. A new ED sample is ready for readout from the RADIO.EDSAMPLE register

|                  |            |              |       |                                                                                                              |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|------------------|------------|--------------|-------|--------------------------------------------------------------------------------------------------------------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|--|--|
| Bit number       |            |              | 31    | 30                                                                                                           | 29          | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |  |  |
| ID               |            |              | A     |                                                                                                              |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| Reset 0x00000000 |            |              | 0     | 0                                                                                                            | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |  |
| ID               | Acce Field | Value ID     | Value |                                                                                                              | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| A                | RW         | EVENTS_EDEND |       | Sampling of energy detection complete. A new ED sample is ready for readout from the RADIO.EDSAMPLE register |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | NotGenerated | 0     | Event not generated                                                                                          |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | Generated    | 1     | Event generated                                                                                              |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |  |

### 7.1.27.15.40 EVENTS\_EDSTOPPED

Address offset: 0x140

The sampling of energy detection has stopped

|                  |            |                  |       |                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|------------------|------------|------------------|-------|----------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|---|
| Bit number       |            |                  |       | 31                                           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |   |
| ID               |            |                  |       |                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | A |
| Reset 0x00000000 |            |                  |       | 0                                            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |   |
| ID               | Acce Field | Value ID         | Value | Description                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
| A                | RW         | EVENTS_EDSTOPPED |       | The sampling of energy detection has stopped |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | NotGenerated     | 0     | Event not generated                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | Generated        | 1     | Event generated                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |

### 7.1.27.15.41 EVENTS\_CCAIDLE

Address offset: 0x144

Wireless medium in idle - clear to send

|                  |            |                |       |                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|------------------|------------|----------------|-------|-----------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|---|
| Bit number       |            |                |       | 31                                      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |   |
| ID               |            |                |       |                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | A |
| Reset 0x00000000 |            |                |       | 0                                       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |   |
| ID               | Acce Field | Value ID       | Value | Description                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
| A                | RW         | EVENTS_CCAIDLE |       | Wireless medium in idle - clear to send |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | NotGenerated   | 0     | Event not generated                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | Generated      | 1     | Event generated                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |

### 7.1.27.15.42 EVENTS\_CCABUSY

Address offset: 0x148

Wireless medium busy - do not send

| Bit number       |                   |              | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|-------------------|--------------|---------------------------------------------------------------------------------------|------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |                   |              | A                                                                                     |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |                   |              | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field        | Value ID     | Value                                                                                 | Description                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW EVENTS_CCABUSY |              |                                                                                       | Wireless medium busy - do not send |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                   | NotGenerated | 0                                                                                     | Event not generated                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                   | Generated    | 1                                                                                     | Event generated                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.27.15.43 EVENTS\_CCASTOPPED

Address offset: 0x14C

The CCA has stopped

|                  |                      |              |                                                                                       |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|----------------------|--------------|---------------------------------------------------------------------------------------|---------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |                      |              | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |                      |              | A                                                                                     |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |                      |              | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field           | Value ID     | Value                                                                                 | Description         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW EVENTS_CCASTOPPED |              |                                                                                       | The CCA has stopped |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                      | NotGenerated | 0                                                                                     | Event not generated |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                      | Generated    | 1                                                                                     | Event generated     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.27.15.44 EVENTS\_RATEBOOST

Address offset: 0x150

Ble\_LR CI field received, receive mode is changed from Ble\_LR125Kbit to Ble\_LR500Kbit.

|                  |                     |              |                                                                                       |                                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|---------------------|--------------|---------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |                     |              | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |                     |              | A                                                                                     |                                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |                     |              | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |                                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field          | Value ID     | Value                                                                                 | Description                                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW EVENTS_RATEBOOST |              |                                                                                       | Ble_LR CI field received, receive mode is changed from<br><br>Ble_LR125Kbit to Ble_LR500Kbit. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                     | NotGenerated | 0                                                                                     | Event not generated                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                     | Generated    | 1                                                                                     | Event generated                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.27.15.45 EVENTS\_TXREADY

Address offset: 0x154

RADIO has ramped up and is ready to be started TX path

|                  |            |                |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |                |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |                |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |                |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID       | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | EVENTS_TXREADY |       | RADIO has ramped up and is ready to be started TX path                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | NotGenerated   | 0     | Event not generated                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Generated      | 1     | Event generated                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.27.15.46 EVENTS\_RXREADY

Address offset: 0x158

RADIO has ramped up and is ready to be started RX path

| Bit number       |            |                | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------------|---------------------------------------------------------------------------------------|--------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |            |                | A                                                                                     |                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |                | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID       | Value                                                                                 | Description                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | EVENTS_RXREADY |                                                                                       | RADIO has ramped up and is ready to be started RX path |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | NotGenerated   | 0                                                                                     | Event not generated                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Generated      | 1                                                                                     | Event generated                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.27.15.47 EVENTS\_MHRMATCH

Address offset: 0x15C

MAC header match found

|                  |            |                 |                                                                                       |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|-----------------|---------------------------------------------------------------------------------------|------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |                 | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |                 | A                                                                                     |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |                 | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID        | Value                                                                                 | Description            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | EVENTS_MHRMATCH |                                                                                       | MAC header match found |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | NotGenerated    | 0                                                                                     | Event not generated    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Generated       | 1                                                                                     | Event generated        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.27.15.48 EVENTS\_PHYEND

Address offset: 0x16C

Generated when last bit is sent on air

|                  |            |               |                                                                                       |                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|---------------|---------------------------------------------------------------------------------------|----------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |               | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |               | A                                                                                     |                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |               | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID      | Value                                                                                 | Description                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | EVENTS_PHYEND |                                                                                       | Generated when last bit is sent on air |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | NotGenerated  | 0                                                                                     | Event not generated                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Generated     | 1                                                                                     | Event generated                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.27.15.49 EVENTS\_CTEPRESENT

Address offset: 0x170

CTE is present (early warning right after receiving CTEInfo byte)

|                  |      |                   |              |    |                                                                   |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
|------------------|------|-------------------|--------------|----|-------------------------------------------------------------------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|
| Bit number       |      |                   |              | 31 | 30                                                                | 29          | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |
| ID               |      |                   |              | A  |                                                                   |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
| Reset 0x00000000 |      |                   |              | 0  | 0                                                                 | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |
| ID               | Acce | Field             | Value        | ID | Value                                                             | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
| A                | RW   | EVENTS_CTEPRESENT |              |    | CTE is present (early warning right after receiving CTEInfo byte) |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |                   | NotGenerated | 0  | Event not generated                                               |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |                   | Generated    | 1  | Event generated                                                   |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |

### 7.1.27.15.50 PUBLISH\_READY

Address offset: 0x180

Publish configuration for event [READY](#)

|                  |            |  |          |  |          |  |                                                  |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|--|----------|--|--------------------------------------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          |  |          |  |                                                  |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |
| ID               |            |  |          |  |          |  |                                                  |  |  | B  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  |    |    |    |   |   |   |   |   |   | A | A | A | A | A | A | A |   |   |   |
| Reset 0x00000000 |            |  |          |  |          |  |                                                  |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID |  | Value    |  | Description                                      |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         |  | CHIDX    |  | [255..0] |  | Channel that event <b>READY</b> will publish to. |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW         |  | EN       |  |          |  |                                                  |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled |  | 0        |  | Disable publishing                               |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  |  | 1        |  | Enable publishing                                |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.27.15.51 PUBLISH\_ADDRESS

Address offset: 0x184

Publish configuration for event [ADDRESS](#)

|                  |            |       |          |          |       |                                             |             |                    |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-------|----------|----------|-------|---------------------------------------------|-------------|--------------------|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |       |          |          |       |                                             |             |                    |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |
| ID               |            |       |          |          |       |                                             |             |                    |  | B  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  |    |    |    |   |   |   |   |   |   | A | A | A | A | A | A | A |   |   |
| Reset 0x00000000 |            |       |          |          |       |                                             |             |                    |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |       | Value ID |          | Value |                                             | Description |                    |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | CHIDX |          | [255..0] |       | Channel that event ADDRESS will publish to. |             |                    |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW         | EN    |          | Disabled |       | 0                                           |             | Disable publishing |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |       |          | Enabled  |       | 1                                           |             | Enable publishing  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |       |          |          |       |                                             |             |                    |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.27.15.52 PUBLISH\_PAYLOAD

Address offset: 0x188

Publish configuration for event [PAYLOAD](#)

|                  |            |          |  |          |   |  |       |                    |  |             |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|--|----------|---|--|-------|--------------------|--|-------------|----------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |  |          |   |  |       |                    |  | 31          | 30                                                 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |
| ID               |            |          |  |          |   |  |       |                    |  | B           |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  |    |    |    |   |   |   |   |   |   | A | A | A | A | A | A | A |   |   |   |
| Reset 0x00000000 |            |          |  |          |   |  |       |                    |  | 0           | 0                                                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |          |  | Value ID |   |  | Value |                    |  | Description |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | CHIDX    |  |          |   |  |       | [255..0]           |  |             | Channel that event <b>PAYLOAD</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW         | EN       |  |          |   |  |       |                    |  |             |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled |  |          | 0 |  |       | Disable publishing |  |             |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  |  |          | 1 |  |       | Enable publishing  |  |             |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |



|                  |            |          |  |          |    |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |
|------------------|------------|----------|--|----------|----|----------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|--|
| Bit number       |            |          |  | 31       | 30 | 29                                                 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |  |
| ID               |            |          |  | B        |    |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A |  |
| Reset 0x00000000 |            |          |  | 0        | 0  | 0                                                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |  |
| ID               | Acce Field | Value ID |  | Value    |    | Description                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |
| A                | RW CHIDX   |          |  | [255..0] |    | Channel that event <b>DEVMISS</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |
| B                | RW EN      | Disabled |  | 0        |    | Disable publishing                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | Enabled  |  | 1        |    | Enable publishing                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |

### 7.1.27.15.57 PUBLISH\_RSSIEND

Address offset: 0x19C

Publish configuration for event [RSSIEND](#)

A new RSSI sample is ready for readout from the RADIO.RSSISAMPLE register

|                  |            |          |          |                                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|-------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                                                                      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |          |          | B                                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field | Value ID | Value    | Description                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] | Channel that event <span>RSSIEND</span> will publish to.                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |                                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        | Disable publishing                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        | Enable publishing                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.27.15.58 PUBLISH\_BCMATCH

Address offset: 0x1A8

Publish configuration for event [BCMATCH](#)

Bit counter value is specified in the RADIO.BCC register

|                  |            |          |          |          |    |                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|----------|----|----------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31       | 30 | 29                                                       | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |          |          | B        |    |                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |          |          | 0        |    |                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |          | Value ID | Value    |    | Description                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          |          | [255..0] |    | Channel that event <span>BCMATCH</span> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |          |    |                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled |          | 0        |    | Disable publishing                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  |          | 1        |    | Enable publishing                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.27.15.59 PUBLISH\_CRCOK

Address offset: 0x1B0

Publish configuration for event [CRCOK](#)

|                  |            |          |          |                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|-----------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                                                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |          |          | B                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |          | 0                                                         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce Field | Value ID | Value    | Description                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] | Channel that event <a href="#">CRCOK</a> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        | Disable publishing                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        | Enable publishing                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.27.15.60 PUBLISH\_CRCERROR

Address offset: 0x1B4

Publish configuration for event [CRCERROR](#)

|                  |            |          |          |                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|--------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                                                           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |          |          | B                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |          | 0                                                            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce Field | Value ID | Value    | Description                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] | Channel that event <a href="#">CRCERROR</a> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        | Disable publishing                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        | Enable publishing                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.27.15.61 PUBLISH\_FRAMESTART

Address offset: 0x1B8

Publish configuration for event [FRAMESTART](#)

|                  |            |  |          |          |    |                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|----------|----|------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31       | 30 | 29                                             | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |  |          | B        |    |                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   |   |   |   |   |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |          | 0        |    |                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID | Value    |    | Description                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          | [255..0] |    | Channel that event FRAMESTART will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  | Disabled | 0        |    | Disable publishing                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  | 1        |    | Enable publishing                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.27.15.62 PUBLISH\_EDEND

Address offset: 0x1BC

Publish configuration for event [EDEND](#)

|                  |            |  |          |          |                    |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|----------|--------------------|--------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31       | 30                 | 29                                               | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |  |          | B        |                    |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   |   |   |   |   |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |          | 0        |                    |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID | Value    |                    | Description                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          | [255..0] |                    | Channel that event <b>EDEND</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |          |                    |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled | 0        | Disable publishing |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  | 1        | Enable publishing  |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |





|                  |            |          |          |                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                                             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |          |          | B                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |          | 0                                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce Field | Value ID | Value    | Description                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] | Channel that event CCASTOPPED will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        | Disable publishing                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        | Enable publishing                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.27.15.67 PUBLISH\_RATEBOOST

Address offset: 0x1D0

Publish configuration for event **RATEBOOST**

|                  |            |  |  |          |    |          |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|--|----------|----|----------|----|------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |  | 31       | 30 | 29       | 28 | 27                                                   | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |  |  | B        |    |          |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   |   |   |   |   |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |  | 0        |    |          |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  |  | Value ID |    | Value    |    | Description                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |  |          |    | [255..0] |    | Channel that event <b>RATEBOOST</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |  |          |    |          |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  |  | Disabled |    | 0        |    | Disable publishing                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  |  | Enabled  |    | 1        |    | Enable publishing                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.27.15.68 PUBLISH\_TXREADY

Address offset: 0x1D4

Publish configuration for event **TXREADY**

|                  |            |  |          |                                                                         |                    |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|-------------------------------------------------------------------------|--------------------|----------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31                                                                      | 30                 | 29                                                 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |  |          | B                                                                       |                    |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |                    |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field |  | Value ID | Value                                                                   |                    | Description                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          | [255..0]                                                                |                    | Channel that event <b>TXREADY</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |                                                                         |                    |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled | 0                                                                       | Disable publishing |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  | 1                                                                       | Enable publishing  |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.27.15.69 PUBLISH\_RXREADY

Address offset: 0x1D8

Publish configuration for event **RXREADY**

|                  |            |  |          |          |    |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|----------|----|----------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31       | 30 | 29                                                 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |  |          | B        |    |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |          | 0        |    |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID | Value    |    | Description                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          | [255..0] |    | Channel that event <b>RXREADY</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |          |    |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled | 0        |    | Disable publishing                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  | 1        |    | Enable publishing                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.27.15.70 PUBLISH\_MHRMATCH

Address offset: 0x1DC

Publish configuration for event [MHRMATCH](#)

|                  |            |          |                                                                                       |  |  |  |                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|--|--|--|--------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |          | B                                                                                     |  |  |  |                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |  |  |  |                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 |  |  |  | Description                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                              |  |  |  | Channel that event <a href="#">MHRMATCH</a> will publish to. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |                                                                                       |  |  |  |                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     |  |  |  | Disable publishing                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     |  |  |  | Enable publishing                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

### 7.1.27.15.71 PUBLISH\_PHYEND

Address offset: 0x1EC

Publish configuration for event [PHYEND](#)

|                  |            |          |                                                                                       |                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|---------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |          | B                                                                                     |                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                              | Channel that event <span>PHYEND</span> will publish to. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |                                                                                       |                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Disable publishing                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Enable publishing                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

### 7.1.27.15.72 PUBLISH\_CTEPRESENT

Address offset: 0x1F0

Publish configuration for event [CTEPRESENT](#)

|                  |            |          |                                                                                       |  |  |  |                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|--|--|--|-------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |          | B                                                                                     |  |  |  |                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |  |  |  |                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 |  |  |  | Description                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                              |  |  |  | Channel that event <span>CTEPRESENT</span> will publish to. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |                                                                                       |  |  |  |                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     |  |  |  | Disable publishing                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     |  |  |  | Enable publishing                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

### 7.1.27.15.73 SHORTS

Address offset: 0x200

Shortcuts between local events and tasks

| Bit number       |      |                    |          | 31                                                                      | 30                                                               | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
|------------------|------|--------------------|----------|-------------------------------------------------------------------------|------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| ID               |      |                    |          | U T S R Q P O N M L K H G F E D C B A                                   |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| Reset 0x00000000 |      |                    |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| ID               | Acce | Field              | Value ID | Value                                                                   | Description                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| A                | RW   | READY_START        |          |                                                                         | Shortcut between event <b>READY</b> and task <b>START</b>        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                    | Disabled | 0                                                                       | Disable shortcut                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                    | Enabled  | 1                                                                       | Enable shortcut                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| B                | RW   | END_DISABLE        |          |                                                                         | Shortcut between event <b>END</b> and task <b>DISABLE</b>        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                    | Disabled | 0                                                                       | Disable shortcut                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                    | Enabled  | 1                                                                       | Enable shortcut                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| C                | RW   | DISABLED_TXEN      |          |                                                                         | Shortcut between event <b>DISABLED</b> and task <b>TXEN</b>      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                    | Disabled | 0                                                                       | Disable shortcut                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                    | Enabled  | 1                                                                       | Enable shortcut                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| D                | RW   | DISABLED_RXEN      |          |                                                                         | Shortcut between event <b>DISABLED</b> and task <b>RXEN</b>      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                    | Disabled | 0                                                                       | Disable shortcut                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                    | Enabled  | 1                                                                       | Enable shortcut                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| E                | RW   | ADDRESS_RSSISTART  |          |                                                                         | Shortcut between event <b>ADDRESS</b> and task <b>RSSISTART</b>  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                    | Disabled | 0                                                                       | Disable shortcut                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                    | Enabled  | 1                                                                       | Enable shortcut                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| F                | RW   | END_START          |          |                                                                         | Shortcut between event <b>END</b> and task <b>START</b>          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                    | Disabled | 0                                                                       | Disable shortcut                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                    | Enabled  | 1                                                                       | Enable shortcut                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| G                | RW   | ADDRESS_BCSTART    |          |                                                                         | Shortcut between event <b>ADDRESS</b> and task <b>BCSTART</b>    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                    | Disabled | 0                                                                       | Disable shortcut                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                    | Enabled  | 1                                                                       | Enable shortcut                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| H                | RW   | DISABLED_RSSISTOP  |          |                                                                         | Shortcut between event <b>DISABLED</b> and task <b>RSSISTOP</b>  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                    | Disabled | 0                                                                       | Disable shortcut                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                    | Enabled  | 1                                                                       | Enable shortcut                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| K                | RW   | RXREADY_CCASTART   |          |                                                                         | Shortcut between event <b>RXREADY</b> and task <b>CCASTART</b>   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                    | Disabled | 0                                                                       | Disable shortcut                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                    | Enabled  | 1                                                                       | Enable shortcut                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| L                | RW   | CCAIDLE_TXEN       |          |                                                                         | Shortcut between event <b>CCAIDLE</b> and task <b>TXEN</b>       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                    | Disabled | 0                                                                       | Disable shortcut                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                    | Enabled  | 1                                                                       | Enable shortcut                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| M                | RW   | CCABUSY_DISABLE    |          |                                                                         | Shortcut between event <b>CCABUSY</b> and task <b>DISABLE</b>    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                    | Disabled | 0                                                                       | Disable shortcut                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                    | Enabled  | 1                                                                       | Enable shortcut                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| N                | RW   | FRAMESTART_BCSTART |          |                                                                         | Shortcut between event <b>FRAMESTART</b> and task <b>BCSTART</b> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                    | Disabled | 0                                                                       | Disable shortcut                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                    | Enabled  | 1                                                                       | Enable shortcut                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| O                | RW   | READY_EDSTART      |          |                                                                         | Shortcut between event <b>READY</b> and task <b>EDSTART</b>      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                    | Disabled | 0                                                                       | Disable shortcut                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                    | Enabled  | 1                                                                       | Enable shortcut                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| P                | RW   | EDEND_DISABLE      |          |                                                                         | Shortcut between event <b>EDEND</b> and task <b>DISABLE</b>      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                    | Disabled | 0                                                                       | Disable shortcut                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                    | Enabled  | 1                                                                       | Enable shortcut                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| Q                | RW   | CCAIDLE_STOP       |          |                                                                         | Shortcut between event <b>CCAIDLE</b> and task <b>STOP</b>       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                    | Disabled | 0                                                                       | Disable shortcut                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                    | Enabled  | 1                                                                       | Enable shortcut                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| R                | RW   | TXREADY_START      |          |                                                                         | Shortcut between event <b>TXREADY</b> and task <b>START</b>      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                    | Disabled | 0                                                                       | Disable shortcut                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                    | Enabled  | 1                                                                       | Enable shortcut                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| S                | RW   | RXREADY_START      |          |                                                                         | Shortcut between event <b>RXREADY</b> and task <b>START</b>      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                    | Disabled | 0                                                                       | Disable shortcut                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

| Bit number       |                   |          | 31                    | 30 | 29                                             | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15              | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |
|------------------|-------------------|----------|-----------------------|----|------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|--|
| ID               |                   |          | U T S R Q P O N M L K |    |                                                |    |    |    |    |    |    |    |    |    |    |    |    |    | H G F E D C B A |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| Reset 0x00000000 |                   |          | 0                     | 0  | 0                                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |  |
| ID               | Acce Field        | Value ID | Value                 |    | Description                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |                 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| T                | RW PHYEND_DISABLE | Enabled  | 1                     |    | Enable shortcut                                |    |    |    |    |    |    |    |    |    |    |    |    |    |                 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |                   | Disabled | 0                     |    | Shortcut between event PHYEND and task DISABLE |    |    |    |    |    |    |    |    |    |    |    |    |    |                 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |                   | Enabled  | 1                     |    | Enable shortcut                                |    |    |    |    |    |    |    |    |    |    |    |    |    |                 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| U                | RW PHYEND_START   | Disabled | 0                     |    | Shortcut between event PHYEND and task START   |    |    |    |    |    |    |    |    |    |    |    |    |    |                 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |                   | Enabled  | 1                     |    | Enable shortcut                                |    |    |    |    |    |    |    |    |    |    |    |    |    |                 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |                   | Disabled | 0                     |    | Disable shortcut                               |    |    |    |    |    |    |    |    |    |    |    |    |    |                 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |                   | Enabled  | 1                     |    | Enable shortcut                                |    |    |    |    |    |    |    |    |    |    |    |    |    |                 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |

### 7.1.27.15.74 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number       |             |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|-------------|----------|---------------------------------------------------------------------------------------|---------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |             |          | a Z V U T S R Q P O N M L K I                                                         |                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  | H G F E D C B A |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |             |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                   |                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field  | Value ID | Value                                                                                 | Description                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW READY    |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">READY</a>             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |             | Set      | 1                                                                                     | Enable                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |             | Disabled | 0                                                                                     | Read: Disabled                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |             | Enabled  | 1                                                                                     | Read: Enabled                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW ADDRESS  |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">ADDRESS</a>           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |             | Set      | 1                                                                                     | Enable                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |             | Disabled | 0                                                                                     | Read: Disabled                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |             | Enabled  | 1                                                                                     | Read: Enabled                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW PAYLOAD  |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">PAYLOAD</a>           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |             | Set      | 1                                                                                     | Enable                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |             | Disabled | 0                                                                                     | Read: Disabled                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |             | Enabled  | 1                                                                                     | Read: Enabled                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| D                | RW END      |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">END</a>               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |             | Set      | 1                                                                                     | Enable                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |             | Disabled | 0                                                                                     | Read: Disabled                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |             | Enabled  | 1                                                                                     | Read: Enabled                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| E                | RW DISABLED |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">DISABLED</a>          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |             | Set      | 1                                                                                     | Enable                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |             | Disabled | 0                                                                                     | Read: Disabled                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |             | Enabled  | 1                                                                                     | Read: Enabled                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| F                | RW DEVMATCH |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">DEVMATCH</a>          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |             | Set      | 1                                                                                     | Enable                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |             | Disabled | 0                                                                                     | Read: Disabled                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |             | Enabled  | 1                                                                                     | Read: Enabled                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| G                | RW DEVMISS  |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">DEVMISS</a>           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |             | Set      | 1                                                                                     | Enable                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |             | Disabled | 0                                                                                     | Read: Disabled                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |             | Enabled  | 1                                                                                     | Read: Enabled                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| H                | RW RSSIEND  |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">RSSIEND</a>           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |             |          |                                                                                       | A new RSSI sample is ready for readout from the RADIO.RSSISAMPLE register |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |             | Set      | 1                                                                                     | Enable                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

| Bit number       |      |                | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                                    |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|------------------|------|----------------|---------------------------------------------------------------------------------------|-------|--------------------------------------------------------------------|--|--|--------------------------------------------------------------------|--|--|-------------------------|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|--|--|
| ID               |      |                | a Z                                                                                   |       |                                                                    |  |  |                                                                    |  |  | V U T S R Q P O N M L K |  |  |  |  |  |  |  | I               |  |  |  |  |  |  |  | H G F E D C B A |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |                | 0 0 0 0 0 0 0 0                                                                       |       |                                                                    |  |  |                                                                    |  |  | 0 0 0 0 0 0 0 0         |  |  |  |  |  |  |  | 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  | 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field          | Value ID                                                                              | Value | Description                                                        |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
| I                | RW   | BCMATCH        | Disabled                                                                              | 0     | Read: Disabled                                                     |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |                | Enabled                                                                               | 1     | Read: Enabled                                                      |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |                |                                                                                       |       | Write '1' to enable interrupt for event <a href="#">BCMATCH</a>    |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |                |                                                                                       |       | Bit counter value is specified in the RADIO.BCC register           |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |                | Set                                                                                   | 1     | Enable                                                             |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
| K                | RW   | CRCOK          | Disabled                                                                              | 0     | Read: Disabled                                                     |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |                | Enabled                                                                               | 1     | Read: Enabled                                                      |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |                |                                                                                       |       | Write '1' to enable interrupt for event <a href="#">CRCOK</a>      |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |                | Set                                                                                   | 1     | Enable                                                             |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |                | Disabled                                                                              | 0     | Read: Disabled                                                     |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
| L                | RW   | CRCERROR       | Enabled                                                                               | 1     | Read: Enabled                                                      |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |                |                                                                                       |       | Write '1' to enable interrupt for event <a href="#">CRCERROR</a>   |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |                | Set                                                                                   | 1     | Enable                                                             |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |                | Disabled                                                                              | 0     | Read: Disabled                                                     |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |                | Enabled                                                                               | 1     | Read: Enabled                                                      |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
| M                | RW   | FRAMESTART     |                                                                                       |       | Write '1' to enable interrupt for event <a href="#">FRAMESTART</a> |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |                | Set                                                                                   | 1     | Enable                                                             |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |                | Disabled                                                                              | 0     | Read: Disabled                                                     |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |                | Enabled                                                                               | 1     | Read: Enabled                                                      |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |                | N                                                                                     | RW    | EDEND                                                              |  |  | Write '1' to enable interrupt for event <a href="#">EDEND</a>      |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
| Set              | 1    | Enable         |                                                                                       |       |                                                                    |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
| Disabled         | 0    | Read: Disabled |                                                                                       |       |                                                                    |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
| Enabled          | 1    | Read: Enabled  |                                                                                       |       |                                                                    |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
| O                | RW   | EDSTOPPED      |                                                                                       |       |                                                                    |  |  | Write '1' to enable interrupt for event <a href="#">EDSTOPPED</a>  |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |                | Set                                                                                   | 1     | Enable                                                             |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |                | Disabled                                                                              | 0     | Read: Disabled                                                     |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |                | Enabled                                                                               | 1     | Read: Enabled                                                      |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |                | P                                                                                     | RW    | CCAIDLE                                                            |  |  | Write '1' to enable interrupt for event <a href="#">CCAIDLE</a>    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
| Set              | 1    | Enable         |                                                                                       |       |                                                                    |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
| Disabled         | 0    | Read: Disabled |                                                                                       |       |                                                                    |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
| Enabled          | 1    | Read: Enabled  |                                                                                       |       |                                                                    |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
| Q                | RW   | CCABUSY        |                                                                                       |       |                                                                    |  |  | Write '1' to enable interrupt for event <a href="#">CCABUSY</a>    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |                | Set                                                                                   | 1     | Enable                                                             |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |                | Disabled                                                                              | 0     | Read: Disabled                                                     |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |                | Enabled                                                                               | 1     | Read: Enabled                                                      |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |                | R                                                                                     | RW    | CCASTOPPED                                                         |  |  | Write '1' to enable interrupt for event <a href="#">CCASTOPPED</a> |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
| Set              | 1    | Enable         |                                                                                       |       |                                                                    |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
| Disabled         | 0    | Read: Disabled |                                                                                       |       |                                                                    |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
| Enabled          | 1    | Read: Enabled  |                                                                                       |       |                                                                    |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
| S                | RW   | RATEBOOST      |                                                                                       |       |                                                                    |  |  | Write '1' to enable interrupt for event <a href="#">RATEBOOST</a>  |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |                | Set                                                                                   | 1     | Enable                                                             |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |                | Disabled                                                                              | 0     | Read: Disabled                                                     |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |                | Enabled                                                                               | 1     | Read: Enabled                                                      |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |                | T                                                                                     | RW    | TXREADY                                                            |  |  | Write '1' to enable interrupt for event <a href="#">TXREADY</a>    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
| Set              | 1    | Enable         |                                                                                       |       |                                                                    |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
| Disabled         | 0    | Read: Disabled |                                                                                       |       |                                                                    |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
| Enabled          | 1    | Read: Enabled  |                                                                                       |       |                                                                    |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
| U                | RW   | RXREADY        |                                                                                       |       |                                                                    |  |  | Write '1' to enable interrupt for event <a href="#">RXREADY</a>    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |                | Set                                                                                   | 1     | Enable                                                             |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |      |                | Disabled                                                                              | 0     | Read: Disabled                                                     |  |  |                                                                    |  |  |                         |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |

| Bit number       |            |            | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                    |               |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|------------------|------------|------------|---------------------------------------------------------------------------------------|--------------------------------------------------------------------|---------------|--|-------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|-----------------|--|--|--|--|--|--|--|--|--|
| ID               |            |            | a Z                                                                                   |                                                                    |               |  | V U T S R Q P O N M L K |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | I |  |  |  | H G F E D C B A |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |            | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |                                                                    |               |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |                 |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID   | Value                                                                                 |                                                                    | Description   |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled    | 1                                                                                     |                                                                    | Read: Enabled |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |                 |  |  |  |  |  |  |  |  |  |
| V                | RW         | MHRMATCH   |                                                                                       | Write '1' to enable interrupt for event <a href="#">MHRMATCH</a>   |               |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |            | Set        | 1                                                                                     | Enable                                                             |               |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled   | 0                                                                                     | Read: Disabled                                                     |               |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled    | 1                                                                                     | Read: Enabled                                                      |               |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |                 |  |  |  |  |  |  |  |  |  |
| Z                | RW         | PHYEND     |                                                                                       | Write '1' to enable interrupt for event <a href="#">PHYEND</a>     |               |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |            | Set        | 1                                                                                     | Enable                                                             |               |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled   | 0                                                                                     | Read: Disabled                                                     |               |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled    | 1                                                                                     | Read: Enabled                                                      |               |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |                 |  |  |  |  |  |  |  |  |  |
| a                | RW         | CTEPRESENT |                                                                                       | Write '1' to enable interrupt for event <a href="#">CTEPRESENT</a> |               |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |            | Set        | 1                                                                                     | Enable                                                             |               |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled   | 0                                                                                     | Read: Disabled                                                     |               |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |                 |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled    | 1                                                                                     | Read: Enabled                                                      |               |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |                 |  |  |  |  |  |  |  |  |  |

### 7.1.27.15.75 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number       |      |          |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                   |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |
|------------------|------|----------|----------|---------------------------------------------------------------------------------------|-------------------------------------------------------------------|--|--|--|--|--|--|-------------------------|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|--|
| ID               |      |          |          | a Z                                                                                   |                                                                   |  |  |  |  |  |  | V U T S R Q P O N M L K |  |  |  |  |  |  |  | I |  |  |  |  |  |  |  | H G F E D C B A |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |          |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                   |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |
| ID               | Acce | Field    | Value ID | Value                                                                                 | Description                                                       |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |
| A                | RW   | READY    |          |                                                                                       | Write '1' to disable interrupt for event <a href="#">READY</a>    |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |
|                  |      |          | Clear    | 1                                                                                     | Disable                                                           |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |
|                  |      |          | Disabled | 0                                                                                     | Read: Disabled                                                    |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |
|                  |      |          | Enabled  | 1                                                                                     | Read: Enabled                                                     |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |
| B                | RW   | ADDRESS  |          |                                                                                       | Write '1' to disable interrupt for event <a href="#">ADDRESS</a>  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |
|                  |      |          | Clear    | 1                                                                                     | Disable                                                           |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |
|                  |      |          | Disabled | 0                                                                                     | Read: Disabled                                                    |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |
|                  |      |          | Enabled  | 1                                                                                     | Read: Enabled                                                     |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |
| C                | RW   | PAYLOAD  |          |                                                                                       | Write '1' to disable interrupt for event <a href="#">PAYLOAD</a>  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |
|                  |      |          | Clear    | 1                                                                                     | Disable                                                           |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |
|                  |      |          | Disabled | 0                                                                                     | Read: Disabled                                                    |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |
|                  |      |          | Enabled  | 1                                                                                     | Read: Enabled                                                     |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |
| D                | RW   | END      |          |                                                                                       | Write '1' to disable interrupt for event <a href="#">END</a>      |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |
|                  |      |          | Clear    | 1                                                                                     | Disable                                                           |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |
|                  |      |          | Disabled | 0                                                                                     | Read: Disabled                                                    |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |
|                  |      |          | Enabled  | 1                                                                                     | Read: Enabled                                                     |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |
| E                | RW   | DISABLED |          |                                                                                       | Write '1' to disable interrupt for event <a href="#">DISABLED</a> |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |
|                  |      |          | Clear    | 1                                                                                     | Disable                                                           |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |
|                  |      |          | Disabled | 0                                                                                     | Read: Disabled                                                    |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |
|                  |      |          | Enabled  | 1                                                                                     | Read: Enabled                                                     |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |
| F                | RW   | DEVMATCH |          |                                                                                       | Write '1' to disable interrupt for event <a href="#">DEVMATCH</a> |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |
|                  |      |          | Clear    | 1                                                                                     | Disable                                                           |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |
|                  |      |          | Disabled | 0                                                                                     | Read: Disabled                                                    |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |
|                  |      |          | Enabled  | 1                                                                                     | Read: Enabled                                                     |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |
| G                | RW   | DEVMISS  |          |                                                                                       | Write '1' to disable interrupt for event <a href="#">DEVMISS</a>  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |
|                  |      |          | Clear    | 1                                                                                     | Disable                                                           |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |

| Bit number       |      |            |                                                                           | 31    | 30                                                               | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |
|------------------|------|------------|---------------------------------------------------------------------------|-------|------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|
| ID               |      |            |                                                                           | a     | Z                                                                |    |    |    | V  | U  | T  | S  | R  | Q  | P  | O  | N  | M  | L  | K  |    |    |    | I  |    |   |   | H | G | F | E | D | C | B | A |  |  |  |
| Reset 0x00000000 |      |            |                                                                           | 0     | 0                                                                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |
| ID               | Acce | Field      | Value ID                                                                  | Value | Description                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
| H                | RW   | RSSIEND    | Disabled                                                                  | 0     | Read: Disabled                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Enabled                                                                   | 1     | Read: Enabled                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Write '1' to disable interrupt for event <a href="#">RSSIEND</a>          |       |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | A new RSSI sample is ready for readout from the RADIO.RSSISAMPLE register |       |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Clear                                                                     | 1     | Disable                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Disabled                                                                  | 0     | Read: Disabled                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Enabled                                                                   | 1     | Read: Enabled                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Write '1' to disable interrupt for event <a href="#">BCMATCH</a>          |       |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Bit counter value is specified in the RADIO.BCC register                  |       |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Clear                                                                     | 1     | Disable                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
| K                | RW   | CRCOK      | Disabled                                                                  | 0     | Read: Disabled                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Enabled                                                                   | 1     | Read: Enabled                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Write '1' to disable interrupt for event <a href="#">CRCOK</a>            |       |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Clear                                                                     | 1     | Disable                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Disabled                                                                  | 0     | Read: Disabled                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
| L                | RW   | CRCERROR   | Disabled                                                                  | 0     | Read: Disabled                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Enabled                                                                   | 1     | Read: Enabled                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Write '1' to disable interrupt for event <a href="#">CRCERROR</a>         |       |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Clear                                                                     | 1     | Disable                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Disabled                                                                  | 0     | Read: Disabled                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
| M                | RW   | FRAMESTART | Disabled                                                                  | 0     | Read: Disabled                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Enabled                                                                   | 1     | Read: Enabled                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Write '1' to disable interrupt for event <a href="#">FRAMESTART</a>       |       |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Clear                                                                     | 1     | Disable                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Disabled                                                                  | 0     | Read: Disabled                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
| N                | RW   | EDEND      | Disabled                                                                  | 0     | Read: Disabled                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Enabled                                                                   | 1     | Read: Enabled                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Write '1' to disable interrupt for event <a href="#">EDEND</a>            |       |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Clear                                                                     | 1     | Disable                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Disabled                                                                  | 0     | Read: Disabled                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
| O                | RW   | EDSTOPPED  | Disabled                                                                  | 0     | Read: Disabled                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Enabled                                                                   | 1     | Read: Enabled                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Write '1' to disable interrupt for event <a href="#">EDSTOPPED</a>        |       |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Clear                                                                     | 1     | Disable                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Disabled                                                                  | 0     | Read: Disabled                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
| P                | RW   | CCAIDLE    | Disabled                                                                  | 0     | Read: Disabled                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Enabled                                                                   | 1     | Read: Enabled                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Write '1' to disable interrupt for event <a href="#">CCAIDLE</a>          |       |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Clear                                                                     | 1     | Disable                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Disabled                                                                  | 0     | Read: Disabled                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
| Q                | RW   | CCABUSY    | Disabled                                                                  | 0     | Read: Disabled                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Enabled                                                                   | 1     | Read: Enabled                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Write '1' to disable interrupt for event <a href="#">CCABUSY</a>          |       |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Clear                                                                     | 1     | Disable                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Disabled                                                                  | 0     | Read: Disabled                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
| R                | RW   | CCASTOPPED | Disabled                                                                  | 0     | Read: Disabled                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Enabled                                                                   | 1     | Read: Enabled                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Write '1' to disable interrupt for event <a href="#">CCASTOPPED</a>       |       |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Clear                                                                     | 1     | Disable                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Disabled                                                                  | 0     | Read: Disabled                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
| S                | RW   | RATEBOOST  | Disabled                                                                  | 0     | Read: Disabled                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Enabled                                                                   | 1     | Read: Enabled                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Write '1' to disable interrupt for event <a href="#">RATEBOOST</a>        |       |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Clear                                                                     | 1     | Disable                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |            | Disabled                                                                  | 0     | Read: Disabled                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
| T                | RW   | TXREADY    |                                                                           |       | Write '1' to disable interrupt for event <a href="#">TXREADY</a> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |

| Bit number       |      |            | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                                     |  |  |  |  |  |  |  |  |  |  |  |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|------------|---------------------------------------------------------------------------------------|-------|---------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|-------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               | a Z  |            |                                                                                       |       |                                                                     |  |  |  |  |  |  |  |  |  |  |  | V U T S R Q P O N M L K I H G F E D C B A |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |            | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |       |                                                                     |  |  |  |  |  |  |  |  |  |  |  |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field      | Value ID                                                                              | Value | Description                                                         |  |  |  |  |  |  |  |  |  |  |  |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |            | Clear                                                                                 | 1     | Disable                                                             |  |  |  |  |  |  |  |  |  |  |  |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |            | Disabled                                                                              | 0     | Read: Disabled                                                      |  |  |  |  |  |  |  |  |  |  |  |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |            | Enabled                                                                               | 1     | Read: Enabled                                                       |  |  |  |  |  |  |  |  |  |  |  |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |            |                                                                                       |       |                                                                     |  |  |  |  |  |  |  |  |  |  |  |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| U                | RW   | RXREADY    |                                                                                       |       | Write '1' to disable interrupt for event <a href="#">RXREADY</a>    |  |  |  |  |  |  |  |  |  |  |  |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |            | Clear                                                                                 | 1     | Disable                                                             |  |  |  |  |  |  |  |  |  |  |  |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |            | Disabled                                                                              | 0     | Read: Disabled                                                      |  |  |  |  |  |  |  |  |  |  |  |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |            | Enabled                                                                               | 1     | Read: Enabled                                                       |  |  |  |  |  |  |  |  |  |  |  |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |            |                                                                                       |       |                                                                     |  |  |  |  |  |  |  |  |  |  |  |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| V                | RW   | MHRMATCH   |                                                                                       |       | Write '1' to disable interrupt for event <a href="#">MHRMATCH</a>   |  |  |  |  |  |  |  |  |  |  |  |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |            | Clear                                                                                 | 1     | Disable                                                             |  |  |  |  |  |  |  |  |  |  |  |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |            | Disabled                                                                              | 0     | Read: Disabled                                                      |  |  |  |  |  |  |  |  |  |  |  |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |            | Enabled                                                                               | 1     | Read: Enabled                                                       |  |  |  |  |  |  |  |  |  |  |  |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |            |                                                                                       |       |                                                                     |  |  |  |  |  |  |  |  |  |  |  |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Z                | RW   | PHYEND     |                                                                                       |       | Write '1' to disable interrupt for event <a href="#">PHYEND</a>     |  |  |  |  |  |  |  |  |  |  |  |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |            | Clear                                                                                 | 1     | Disable                                                             |  |  |  |  |  |  |  |  |  |  |  |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |            | Disabled                                                                              | 0     | Read: Disabled                                                      |  |  |  |  |  |  |  |  |  |  |  |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |            | Enabled                                                                               | 1     | Read: Enabled                                                       |  |  |  |  |  |  |  |  |  |  |  |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |            |                                                                                       |       |                                                                     |  |  |  |  |  |  |  |  |  |  |  |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| a                | RW   | CTEPRESENT |                                                                                       |       | Write '1' to disable interrupt for event <a href="#">CTEPRESENT</a> |  |  |  |  |  |  |  |  |  |  |  |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |            | Clear                                                                                 | 1     | Disable                                                             |  |  |  |  |  |  |  |  |  |  |  |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |            | Disabled                                                                              | 0     | Read: Disabled                                                      |  |  |  |  |  |  |  |  |  |  |  |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |            | Enabled                                                                               | 1     | Read: Enabled                                                       |  |  |  |  |  |  |  |  |  |  |  |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |            |                                                                                       |       |                                                                     |  |  |  |  |  |  |  |  |  |  |  |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.27.15.76 CRCSTATUS

Address offset: 0x400

CRC status

|                  |      |           |          |                                                                                       |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|-----------|----------|---------------------------------------------------------------------------------------|--------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |           |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |           |          | A                                                                                     |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |           |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field     | Value ID | Value                                                                                 | Description                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | R    | CRCSTATUS |          |                                                                                       | CRC status of packet received  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | CRCErr   | 0                                                                                     | Packet received with CRC error |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | CRCOk    | 1                                                                                     | Packet received with CRC ok    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.27.15.77 RXMATCH

Address offset: 0x408

Received address

|                  |            |          |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          |       | A A A                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | R          | RXMATCH  |       | Received address                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |          |       | Logical address of which previous packet was received                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.27.15.78 RXCRC

Address offset: 0x40C



CRC field of previously received packet

| Bit number       |            | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                         |
|------------------|------------|---------------------------------------------------------------------------------------|-----------------------------------------|
| ID               |            | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A                           |                                         |
| Reset 0x00000000 |            | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                         |
| ID               | Acce Field | Value ID                                                                              | Description                             |
| A                | R          | RXCRC                                                                                 | CRC field of previously received packet |
|                  |            |                                                                                       | CRC field of previously received packet |

### 7.1.27.15.79 DAI

Address offset: 0x410

Device address match index

| Bit number       |            | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                               |
|------------------|------------|---------------------------------------------------------------------------------------|-------------------------------------------------------------------------------|
| ID               |            | A A A                                                                                 |                                                                               |
| Reset 0x00000000 |            | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                               |
| ID               | Acce Field | Value ID                                                                              | Description                                                                   |
| A                | R          | DAI                                                                                   | Device address match index                                                    |
|                  |            |                                                                                       | Index (n) of device address, see DAB[n] and DAP[n], that got an address match |

### 7.1.27.15.80 PDUSTAT

Address offset: 0x414

Payload status

| Bit number       |            | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                           |
|------------------|------------|---------------------------------------------------------------------------------------|-----------------------------------------------------------|
| ID               |            | B B A                                                                                 |                                                           |
| Reset 0x00000000 |            | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                           |
| ID               | Acce Field | Value ID                                                                              | Description                                               |
| A                | R          | PDUSTAT                                                                               | Status on payload length vs. PCNF1.MAXLEN                 |
|                  |            | LessThan                                                                              | Payload less than PCNF1.MAXLEN                            |
|                  |            | GreaterThan                                                                           | Payload greater than PCNF1.MAXLEN                         |
| B                | R          | CISTAT                                                                                | Status on what rate packet is received with in Long Range |
|                  |            | LR125kbit                                                                             | Frame is received at 125 kbps                             |
|                  |            | LR500kbit                                                                             | Frame is received at 500 kbps                             |

### 7.1.27.15.81 CTESTATUS

Address offset: 0x44C

CTEInfo parsed from received packet

| Bit number       |            | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                            |
|------------------|------------|---------------------------------------------------------------------------------------|----------------------------|
| ID               |            | C C B A A A A A                                                                       |                            |
| Reset 0x00000000 |            | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                            |
| ID               | Acce Field | Value ID                                                                              | Description                |
| A                | R          | CTETIME                                                                               | CTETime parsed from packet |
| B                | R          | RFU                                                                                   | RFU parsed from packet     |
| C                | R          | CTETYPE                                                                               | CTEType parsed from packet |

### 7.1.27.15.82 DFESTATUS

Address offset: 0x458

DfE status information

|                  |      |                |           |                                                                                       |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|----------------|-----------|---------------------------------------------------------------------------------------|-------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |                |           | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |                |           | B A A A                                                                               |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |                |           | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field          | Value ID  | Value                                                                                 | Description                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | R    | SWITCHINGSTATE |           |                                                                                       | Internal state of switching state machine |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                | Idle      | 0                                                                                     | Switching state Idle                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                | Offset    | 1                                                                                     | Switching state Offset                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                | Guard     | 2                                                                                     | Switching state Guard                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                | Ref       | 3                                                                                     | Switching state Ref                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                | Switching | 4                                                                                     | Switching state Switching                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                | Ending    | 5                                                                                     | Switching state Ending                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | R    | SAMPLINGSTATE  |           |                                                                                       | Internal state of sampling state machine  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                | Idle      | 0                                                                                     | Sampling state Idle                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                | Sampling  | 1                                                                                     | Sampling state Sampling                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.27.15.83 PACKETPTR

Address offset: 0x504

Packet pointer

|                  |            |           |                                                                                       |  |  |  |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|-----------|---------------------------------------------------------------------------------------|--|--|--|----------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |           | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |           | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A                   |  |  |  |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x01000000 |            |           | 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |  |  |  |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID  | Value                                                                                 |  |  |  | Description    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | PACKETPTR |                                                                                       |  |  |  | Packet pointer |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

Packet address to be used for the next transmission or reception. When transmitting, the packet pointed to by this address will be transmitted and when receiving, the received packet will be written to this address. This address is a byte aligned RAM address.

**Note:** See the memory chapter for details about which memories are available for EasyDMA.

### 7.1.27.15.84 FREQUENCY

Address offset: 0x508

Frequency

| Bit number       |      |           | 31       | 30       | 29                                       | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
|------------------|------|-----------|----------|----------|------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| ID               |      |           |          |          |                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000002 |      |           | 0        | 0        | 0                                        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| ID               | Acce | Field     | Value ID | Value    | Description                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW   | FREQUENCY |          | [0..100] | Radio channel frequency                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           |          |          | Frequency = 2400 + FREQUENCY (MHz).      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW   | MAP       |          |          | Channel map selection.                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | Default  | 0        | Channel map between 2400 MHz .. 2500 MHz |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           |          |          | Frequency = 2400 + FREQUENCY (MHz)       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | Low      | 1        | Channel map between 2360 MHz .. 2460 MHz |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           |          |          | Frequency = 2360 + FREQUENCY (MHz)       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.27.15.85 TXPOWER

Address offset: 0x50C

Output power

| Bit number       |              | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                                                                                                                                                                                                                                                                                                                                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|--------------|---------------------------------------------------------------------------------------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |              | A A A A A A A A                                                                       |       |                                                                                                                                                                                                                                                                                                                                                                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |              | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |       |                                                                                                                                                                                                                                                                                                                                                                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Access Field | Value ID                                                                              | Value | Description                                                                                                                                                                                                                                                                                                                                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW           | TXPOWER                                                                               |       | <p>RADIO output power</p> <p>Output power in number of dBm, i.e. if the value -20 is specified the output power will be set to -20 dBm.</p> <p>When the radio is operated on 1.2V, the output power is increased by 3 dBm, i.e. if the value -20 is specified, the output power will be set to -17 dBm.</p> <p>See <a href="#">VREQCTRL - Voltage request control</a> on page 54 for how to control voltage.</p> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | 0dBm                                                                                  | 0x0   | 0 dBm                                                                                                                                                                                                                                                                                                                                                                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Neg1dBm                                                                               | 0xFF  | -1 dBm                                                                                                                                                                                                                                                                                                                                                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Neg2dBm                                                                               | 0xFE  | -2 dBm                                                                                                                                                                                                                                                                                                                                                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Neg3dBm                                                                               | 0xFD  | -3 dBm                                                                                                                                                                                                                                                                                                                                                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Neg4dBm                                                                               | 0xFC  | -4 dBm                                                                                                                                                                                                                                                                                                                                                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Neg5dBm                                                                               | 0xFB  | -5 dBm                                                                                                                                                                                                                                                                                                                                                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Neg6dBm                                                                               | 0xFA  | -6 dBm                                                                                                                                                                                                                                                                                                                                                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Neg7dBm                                                                               | 0xF9  | -7 dBm                                                                                                                                                                                                                                                                                                                                                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Neg8dBm                                                                               | 0xF8  | -8 dBm                                                                                                                                                                                                                                                                                                                                                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Neg12dBm                                                                              | 0xF4  | -12 dBm                                                                                                                                                                                                                                                                                                                                                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Neg16dBm                                                                              | 0xF0  | -16 dBm                                                                                                                                                                                                                                                                                                                                                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Neg20dBm                                                                              | 0xEC  | -20 dBm                                                                                                                                                                                                                                                                                                                                                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Neg30dBm                                                                              | 0xE2  | -40 dBm                                                                                                                                                                                                                                                                                                                                                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Neg40dBm                                                                              | 0xD8  | -40 dBm                                                                                                                                                                                                                                                                                                                                                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

Deprecated

### 7.1.27.15.86 MODE

Address offset: 0x510

## Data rate and modulation

| Bit number       |            |                    | 31    | 30 | 29                                                                                                  | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |   |   |   |   |
|------------------|------------|--------------------|-------|----|-----------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|---|---|---|---|
| ID               |            |                    |       |    |                                                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | A | A | A | A |
| Reset 0x00000000 |            |                    | 0     | 0  | 0                                                                                                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |   |   |   |   |
| ID               | Acce Field | Value ID           | Value |    | Description                                                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |   |   |   |
| A                | RW         | MODE               |       |    | Radio data rate and modulation setting. The radio supports frequency-shift keying (FSK) modulation. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |   |   |   |
|                  |            | Nrf_1Mbit          | 0     |    | 1 Mbps Nordic proprietary radio mode                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |   |   |   |
|                  |            | Nrf_2Mbit          | 1     |    | 2 Mbps Nordic proprietary radio mode                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |   |   |   |
|                  |            | Ble_1Mbit          | 3     |    | 1 Mbps BLE                                                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |   |   |   |
|                  |            | Ble_2Mbit          | 4     |    | 2 Mbps BLE                                                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |   |   |   |
|                  |            | Ble_LR125Kbit      | 5     |    | Long range 125 kbps TX, 125 kbps and 500 kbps RX                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |   |   |   |
|                  |            | Ble_LR500Kbit      | 6     |    | Long range 500 kbps TX, 125 kbps and 500 kbps RX                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |   |   |   |
|                  |            | leee802154_250Kbit | 15    |    | IEEE 802.15.4-2006 250 kbps                                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |   |   |   |

### 7.1.27.15.87 PCNF0

Address offset: 0x514

Packet configuration register 0

| Bit number       |      |         |           | 31 | 30                                                  | 29 | 28                                                          | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
|------------------|------|---------|-----------|----|-----------------------------------------------------|----|-------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| ID               |      |         |           | J  | J                                                   | I  |                                                             |    | H  | H  | G  | G  | F  |    |    |    | E  | E  | E  | E  | C  |    |    |    |    |   |   |   |   |   | A |   |   |   | A | A | A |
| Reset 0x00000000 |      |         |           | 0  | 0                                                   | 0  | 0                                                           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |
| ID               | Acce | Field   | Value     | ID | Value                                               |    | Description                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW   | LFLEN   |           |    |                                                     |    | Length on air of LENGTH field in number of bits.            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| C                | RW   | SOLEN   |           |    |                                                     |    | Length on air of S0 field in number of bytes.               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| E                | RW   | S1LEN   |           |    |                                                     |    | Length on air of S1 field in number of bits.                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| F                | RW   | S1INCL  |           |    |                                                     |    | Include or exclude S1 field in RAM                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |         | Automatic | 0  | Include S1 field in RAM only if S1LEN > 0           |    |                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |         | Include   | 1  | Always include S1 field in RAM independent of S1LEN |    |                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| G                | RW   | CILEN   |           |    |                                                     |    | Length of code indicator - long range                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| H                | RW   | PLEN    |           |    |                                                     |    | Length of preamble on air. Decision point: TASKS_START task |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |         | 8bit      | 0  | 8-bit preamble                                      |    |                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |         | 16bit     | 1  | 16-bit preamble                                     |    |                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |         | 32bitZero | 2  | 32-bit zero preamble - used for IEEE 802.15.4       |    |                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |         | LongRange | 3  | Preamble - used for BLE long range                  |    |                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| I                | RW   | CRCINC  |           |    |                                                     |    | Indicates if LENGTH field contains CRC or not               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |         | Exclude   | 0  | LENGTH does not contain CRC                         |    |                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |         | Include   | 1  | LENGTH includes CRC                                 |    |                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| J                | RW   | TERMLEN |           |    |                                                     |    | Length of TERM field in Long Range operation                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.27.15.88 PCNF1

Address offset: 0x518

Packet configuration register 1

| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                                                                                                                                                                                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |            |          | E D C C C B B B B B B B A A A A A A A                                                 |                                                                                                                                                                                                                                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |                                                                                                                                                                                                                                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                                                                                                                                                                                                                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW MAXLEN  |          | [0..255]                                                                              | Maximum length of packet payload. If the packet payload is larger than MAXLEN, the radio will truncate the payload to MAXLEN.                                                                                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW STATLEN |          | [0..255]                                                                              | Static length in number of bytes<br><br>The static length parameter is added to the total length of the payload when sending and receiving packets, e.g. if the static length is set to N the radio will receive or send N bytes more than what is defined in the LENGTH field of the packet. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW BALEN   |          | [2..4]                                                                                | Base address length in number of bytes<br><br>The address field is composed of the base address and the one byte long address prefix, e.g. set BALEN=2 to get a total address of 3 bytes.                                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| D                | RW ENDIAN  |          |                                                                                       | On-air endianness of packet, this applies to the S0, LENGTH, S1, and the PAYLOAD fields.                                                                                                                                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Little   | 0                                                                                     | Least significant bit on air first                                                                                                                                                                                                                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Big      | 1                                                                                     | Most significant bit on air first                                                                                                                                                                                                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| E                | RW WHITEEN |          |                                                                                       | Enable or disable packet whitening<br><br>Including the address field to CRC check is not supported for whitened packets.                                                                                                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Disable                                                                                                                                                                                                                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Enable                                                                                                                                                                                                                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.27.15.89 BASE0

Address offset: 0x51C

Base address 0

| Bit number       |            |       |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|-------|----------|---------------------------------------------------------------------------------------|--|--|--|----------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |            |       |          | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A                         |  |  |  |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |       |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |  |  |  |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field |       | Value ID | Value                                                                                 |  |  |  | Description    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | BASE0 |          |                                                                                       |  |  |  | Base address 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.27.15.90 BASE1

Address offset: 0x520

Base address 1

|                  |            |  |          |                                                                                       |  |  |  |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|--|----------|---------------------------------------------------------------------------------------|--|--|--|----------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |  |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |  |          | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A                         |  |  |  |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |  |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |  |  |  |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field |  | Value ID | Value                                                                                 |  |  |  | Description    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW BASE1   |  |          |                                                                                       |  |  |  | Base address 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.27.15.91 PREFIX0

Address offset: 0x524

## Prefixes bytes for logical addresses 0-3

|                  |            |                |       |    |    |    |                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------------|-------|----|----|----|-------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                | 31    | 30 | 29 | 28 | 27                | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |                | D     | D  | D  | D  | D                 | D  | D  | C  | C  | C  | C  | C  | C  | C  | B  | B  | B  | B  | B  | B  | B  | B  | B | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |                | 0     | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID       | Value |    |    |    | Description       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A-D              | RW         | AP[i] (i=0..3) |       |    |    |    | Address prefix i. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

## 7.1.27.15.92 PREFIX1

Address offset: 0x528

## Prefixes bytes for logical addresses 4-7

|                  |                                                                                       |  |                |  |       |  |                   |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|---------------------------------------------------------------------------------------|--|----------------|--|-------|--|-------------------|--|-------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |                |  |       |  |                   |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | D D D D D D D D C C C C C C C C B B B B B B B A A A A A A A A                         |  |                |  |       |  |                   |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |  |                |  |       |  |                   |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field                                                                            |  | Value ID       |  | Value |  |                   |  | Description |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A-D              | RW                                                                                    |  | AP[i] (i=4..7) |  |       |  | Address prefix i. |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

## 7.1.27.15.93 TXADDRESS

Address offset: 0x52C

## Transmit address select

|                  |            |           |                                                       |    |    |    |                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-----------|-------------------------------------------------------|----|----|----|-------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |           | 31                                                    | 30 | 29 | 28 | 27                      | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |           |                                                       |    |    |    |                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | A | A | A |   |
| Reset 0x00000000 |            |           | 0                                                     | 0  | 0  | 0  | 0                       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID  | Value                                                 |    |    |    | Description             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | TXADDRESS |                                                       |    |    |    | Transmit address select |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |           | Logical address to be used when transmitting a packet |    |    |    |                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

## 7.1.27.15.94 RXADDRESSES

Address offset: 0x530

## Receive address select

|                  |            |                  |          |   |       |         |             |                                                   |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|------------------|----------|---|-------|---------|-------------|---------------------------------------------------|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                  |          |   |       |         |             |                                                   |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |                  |          |   |       |         |             |                                                   |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | H  | G  | F | E | D | C | B | A |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |                  |          |   |       |         |             |                                                   |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |                  | Value ID |   | Value |         | Description |                                                   |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A-H              | RW         | ADDR[i] (i=0..7) |          |   |       |         |             | Enable or disable reception on logical address i. |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled         |          | 0 |       | Disable |             |                                                   |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled          |          | 1 |       | Enable  |             |                                                   |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

## 7.1.27.15.95 CRCCNF

Address offset: 0x534

## CRC configuration



Interframe spacing in  $\mu$ s

|            |  |  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              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| Bit number |  |  | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               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| ID         |  |  | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A 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## 7.1.27.15.100 STATE

Address offset: 0x550

Current radio state

|                  |            |           |                                                                                       |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|-----------|---------------------------------------------------------------------------------------|----------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |           | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |           | A A A A                                                                               |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| ID               | Acce Field | Value ID  | Value                                                                                 | Description                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | R          | STATE     |                                                                                       | Current radio state              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled  | 0                                                                                     | RADIO is in the Disabled state   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | RxRu      | 1                                                                                     | RADIO is in the RXRU state       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | RxIdle    | 2                                                                                     | RADIO is in the RXIDLE state     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Rx        | 3                                                                                     | RADIO is in the RX state         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | RxDisable | 4                                                                                     | RADIO is in the RXDISABLED state |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | TxRu      | 9                                                                                     | RADIO is in the TXRU state       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | TxIdle    | 10                                                                                    | RADIO is in the TXIDLE state     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Tx        | 11                                                                                    | RADIO is in the TX state         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | TxDisable | 12                                                                                    | RADIO is in the TXDISABLED state |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

## 7.1.27.15.101 DATAWHITEIV

Address offset: 0x554

Data whitening initial value





|                  |            |                   |       |    |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-------------------|-------|----|------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                   | 31    | 30 | 29                                                               | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |                   |       |    |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    | P  | O  | N  | M  | L  | K  | J | I | H | G | F | E | D | C | B | A |
| Reset 0x00000000 |            |                   | 0     | 0  | 0                                                                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID          | Value |    | Description                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A-H              | RW         | ENA[i] (i=0..7)   |       |    | Enable or disable device address matching using device address i |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled          | 0     |    | Disabled                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled           | 1     |    | Enabled                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| I-P              | RW         | TXADD[i] (i=0..7) |       |    | TxAdd for device address i                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.27.15.106 MHRMATCHCONF

Address offset: 0x644

## Search pattern configuration

|                  |            |              |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|--------------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |              | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |              | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |              | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID     | Value                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Description |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | MHRMATCHCONF | Search pattern configuration                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.27.15.107 MHRMATCHMAS

Address offset: 0x648

### Pattern mask

|                  |            |             |          |       |    |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-------------|----------|-------|----|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |             |          | 31    | 30 | 29           | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |             |          | A     | A  | A            | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |             |          | 0     | 0  | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |             | Value ID | Value |    | Description  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | MHRMATCHMAS |          |       |    | Pattern mask |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.27.15.108 MODECNF0

Address offset: 0x650

## Radio mode configuration register 0

| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                                                         |                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |   |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------|--------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----|--|---|--|
| ID               |            |          |                                                                                       |                                                                                                         |                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | C C |  | A |  |
| Reset 0x00000200 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                                                         |                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |   |  |
| ID               | Acce Field | Value ID | Value                                                                                 |                                                                                                         | Description        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |   |  |
| A                | RW RU      |          |                                                                                       |                                                                                                         | Radio ramp-up time |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |   |  |
|                  |            | Default  | 0                                                                                     | Default ramp-up time (tRXEN and tTXEN), compatible with firmware written for nRF51                      |                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |   |  |
|                  |            | Fast     | 1                                                                                     | Fast ramp-up (tRXEN,FAST and tTXEN,FAST), see electrical specification for more information             |                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |   |  |
|                  |            |          |                                                                                       | When enabled, TIFS is not enforced by hardware and software needs to control when to turn on the Radio. |                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |   |  |

| Bit number       |            | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|---------------------------------------------------------------------------------------|-------|--------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |            | C C A                                                                                 |       |                                                                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000200 |            | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0                 |       |                                                                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID                                                                              | Value | Description                                                                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW DTX     |                                                                                       |       | Default TX value                                                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |                                                                                       |       | Specifies what the RADIO will transmit when it is not started, i.e. between:                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |                                                                                       |       | RADIO.EVENTS_READY and RADIO.TASKS_START                                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |                                                                                       |       | RADIO.EVENTS_END and RADIO.TASKS_START                                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |                                                                                       |       | RADIO.EVENTS_END and RADIO.EVENTS_DISABLED                                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |                                                                                       |       | <b>Note:</b> For IEEE 802.15.4 250 kbps mode only Center is a valid setting                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |                                                                                       |       | <b>Note:</b> For Bluetooth Low Energy Long Range mode only Center is a valid setting                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | B1                                                                                    | 0     | Transmit '1'                                                                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | B0                                                                                    | 1     | Transmit '0'                                                                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Center                                                                                | 2     | Transmit center frequency                                                                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |                                                                                       |       | When tuning the crystal for center frequency, the RADIO must be set in DTX = Center mode to be able to achieve the expected accuracy |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.27.15.109 SFD

Address offset: 0x660

IEEE 802.15.4 start of frame delimiter

|                  |            |          |                                                                                       |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|-------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          | A A A A A A A A                                                                       |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x000000A7 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 0 1 1 1     |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | SFD      | IEEE 802.15.4 start of frame delimiter                                                |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.27.15.110 EDCNT

Address offset: 0x664

IEEE 802.15.4 energy detect loop count

Number of iterations to perform an ED scan. If set to 0 one scan is performed, otherwise the specified number + 1 of ED scans will be performed and the max ED value tracked in EDSAMPLE.

|                  |            |       |          |                                        |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |
|------------------|------------|-------|----------|----------------------------------------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|--|
| Bit number       |            |       |          | 31                                     | 30          | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |  |
| ID               |            |       |          |                                        |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A | A | A |  |
| Reset 0x00000000 |            |       |          | 0                                      | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |  |
| ID               | Acce Field |       | Value ID | Value                                  | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |
| A                | RW         | EDCNT |          | IEEE 802.15.4 energy detect loop count |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |

### 7.1.27.15.111 EDSAMPLE

Address offset: 0x668

## IEEE 802.15.4 energy detect level

|                  |            |          |  |          |    |                                                                                                                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|------------------|------------|----------|--|----------|----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|
| Bit number       |            |          |  | 31       | 30 | 29                                                                                                                                                                 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |
| ID               |            |          |  |          |    |                                                                                                                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A | A | A | A | A | A | A | A |   |  |  |
| Reset 0x00000000 |            |          |  | 0        | 0  | 0                                                                                                                                                                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |
| ID               | Acce Field | Value ID |  | Value    |    | Description                                                                                                                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
| A                | R          | EDLVL    |  | [0..127] |    | IEEE 802.15.4 energy detect level                                                                                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            |          |  |          |    | Register value must be converted to IEEE 802.15.4 range by an 8-bit saturating multiplication by factor ED_RSSISCALE, as shown in the code example for ED sampling |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |

## 7.1.27.15.112 CCACTRL

Address offset: 0x66C

## IEEE 802.15.4 clear channel assessment control

| Bit number       |      |              | 31               | 30 | 29 | 28                                                                                                           | 27                                                                                                              | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |
|------------------|------|--------------|------------------|----|----|--------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|
| ID               |      |              | D                | D  | D  | D                                                                                                            | D                                                                                                               | D  | D  | D  | C  | C  | C  | C  | C  | C  | C  | C  | B  | B  | B  | B  | B  | B  | B | B | B | B | B | B | B | B | A | A | A |  |  |
| Reset 0x052D0000 |      |              | 0                | 0  | 0  | 0                                                                                                            | 0                                                                                                               | 0  | 1  | 0  | 1  | 0  | 0  | 1  | 0  | 1  | 1  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |
| ID               | Acce | Field        | Value            |    | ID | Value                                                                                                        | Description                                                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
| A                | RW   | CCAMODE      |                  |    |    |                                                                                                              | CCA mode of operation                                                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |              | EdMode           |    | 0  | Energy above threshold                                                                                       |                                                                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |              |                  |    |    | Will report busy whenever energy is detected above CCAEDTHRES                                                |                                                                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |              | CarrierMode      |    | 1  | Carrier seen                                                                                                 |                                                                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |              |                  |    |    | Will report busy whenever compliant IEEE 802.15.4 signal is seen                                             |                                                                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |              | CarrierAndEdMode |    | 2  | Energy above threshold AND carrier seen                                                                      |                                                                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |              | CarrierOrEdMode  |    | 3  | Energy above threshold OR carrier seen                                                                       |                                                                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
| B                | RW   | CCAEDTHRES   |                  |    |    |                                                                                                              | CCA energy busy threshold. Used in all the CCA modes except CarrierMode.                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |              |                  |    |    | Must be converted from IEEE 802.15.4 range by dividing by factor ED_RSSISCALE - similar to EDSAMPLE register |                                                                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |              |                  |    |    |                                                                                                              |                                                                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
| C                | RW   | CCACORRTHRES |                  |    |    |                                                                                                              | CCA correlator busy threshold. Only relevant to CarrierMode, CarrierAndEdMode, and CarrierOrEdMode.             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
| D                | RW   | CCACORRCNT   |                  |    |    |                                                                                                              | Limit for occurrences above CCACORRTHRES. When not equal to zero the correlator based signal detect is enabled. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |

## 7.1.27.15.113 DFEMODE

Address offset: 0x900

Whether to use Angle-of-Arrival (AOA) or Angle-of-Departure (AOD)

|                  |            |           |          |          |       |                                  |             |                                   |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-----------|----------|----------|-------|----------------------------------|-------------|-----------------------------------|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |           |          |          |       |                                  |             |                                   |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |           |          |          |       |                                  |             |                                   |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  | A  |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |           |          |          |       |                                  |             |                                   |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |           | Value ID |          | Value |                                  | Description |                                   |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | DFEOPMODE |          |          |       | Direction finding operation mode |             |                                   |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |           |          | Disabled |       | 0                                |             | Direction finding mode disabled   |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |           |          | AoD      |       | 2                                |             | Direction finding mode set to AoD |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |           |          | AoA      |       | 3                                |             | Direction finding mode set to AoA |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.27.15.114 CTEINLINECONF

Address offset: 0x904

Configuration for CTE inline mode

| Bit number       |      |                    | 31       | 30 | 29                                                     | 28                                                                                                                                                | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------|------|--------------------|----------|----|--------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| ID               |      |                    | I        | I  | I                                                      | I                                                                                                                                                 | I  | I  | I  | I  | H  | H  | H  | H  | H  | H  | H  | G  | G  | G  | F  | F  | F  | F  | E | E | C | B | A |   |   |   |   |   |
| Reset 0x00002800 |      |                    | 0        | 0  | 0                                                      | 0                                                                                                                                                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 1  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce | Field              | Value    | ID | Value                                                  | Description                                                                                                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW   | CTEINLINECTRLIN    |          |    |                                                        | Enable parsing of CTEInfo from received packet in BLE modes                                                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |                    | Enabled  | 1  | Parsing of CTEInfo is enabled                          |                                                                                                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |                    | Disabled | 0  | Parsing of CTEInfo is disabled                         |                                                                                                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| B                | RW   | CTEINFOINS1        |          |    |                                                        | CTEInfo is S1 byte or not                                                                                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |                    | InS1     | 1  | CTEInfo is in S1 byte (data PDU)                       |                                                                                                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |                    | NotInS1  | 0  | CTEInfo is NOT in S1 byte (advertising PDU)            |                                                                                                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| C                | RW   | CTEERRORHANDLING   |          |    |                                                        | Sampling/switching if CRC is not OK                                                                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |                    | Yes      | 1  | Sampling and antenna switching also when CRC is not OK |                                                                                                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |                    | No       | 0  | No sampling and antenna switching when CRC is not OK   |                                                                                                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| E                | RW   | CTETIMEVALIDRANGE  |          |    |                                                        | Max range of CTETime                                                                                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |                    |          |    |                                                        | Note: Valid range is 2-20 in BLE core spec. If larger than 20, it can be an indication of an error in the received packet.                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |                    | 20       | 0  | 20 in 8us unit (default)                               |                                                                                                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |                    |          |    | Set to 20 if parsed CTETime is larger han 20           |                                                                                                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |                    | 31       | 1  | 31 in 8us unit                                         |                                                                                                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| 63               | 2    | 63 in 8us unit     |          |    |                                                        |                                                                                                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| F                | RW   | CTEINLINERXMODE1US |          |    |                                                        | Spacing between samples for the samples in the SWITCHING period when CTEINLINEMODE is set                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |                    |          |    |                                                        | When the device is in AoD mode, this is used when the received CTEType is "AoD 1 us". When in AoA mode, this is used when TSWITCHSPACING is 2 us. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |                    | 4us      | 1  | 4us                                                    |                                                                                                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |                    | 2us      | 2  | 2us                                                    |                                                                                                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |                    | 1us      | 3  | 1us                                                    |                                                                                                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |                    | 500ns    | 4  | 0.5us                                                  |                                                                                                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |                    | 250ns    | 5  | 0.25us                                                 |                                                                                                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |                    | 125ns    | 6  | 0.125us                                                |                                                                                                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

**Note:** Valid range is 2-20 in BLE core spec. If larger than 20, it can be an indication of an error in the received packet.

| Bit number       |      |                    | 31    | 30 | 29 | 28    | 27 | 26                                                                                                                                                | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------|------|--------------------|-------|----|----|-------|----|---------------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| ID               |      |                    | I     | I  | I  | I     | I  | I                                                                                                                                                 | I  | I  | H  | H  | H  | H  | H  | H  | H  | G  | G  | G  | F  | F  | F  | F  | E | E | C | B | A |   |   |   |   |   |
| Reset 0x00002800 |      |                    | 0     | 0  | 0  | 0     | 0  | 0                                                                                                                                                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 1  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce | Field              | Value |    | ID | Value |    | Description                                                                                                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| G                | RW   | CTEINLINERXMODE2US |       |    |    |       |    | Spacing between samples for the samples in the SWITCHING period when CTEINLINEMODE is set                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |                    |       |    |    |       |    | When the device is in AoD mode, this is used when the received CTEType is "AoD 2 us". When in AoA mode, this is used when TSWITCHSPACING is 4 us. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |                    | 4us   | 1  |    |       |    | 4us                                                                                                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |                    | 2us   | 2  |    |       |    | 2us                                                                                                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |                    | 1us   | 3  |    |       |    | 1us                                                                                                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |                    | 500ns | 4  |    |       |    | 0.5us                                                                                                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |                    | 250ns | 5  |    |       |    | 0.25us                                                                                                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |                    | 125ns | 6  |    |       |    | 0.125us                                                                                                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| H                | RW   | S0CONF             |       |    |    |       |    | S0 bit pattern to match                                                                                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |                    |       |    |    |       |    | The least significant bit always corresponds to the first bit of S0 received.                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| I                | RW   | S0MASK             |       |    |    |       |    | S0 bit mask to set which bit to match                                                                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |                    |       |    |    |       |    | The least significant bit always corresponds to the first bit of S0 received.                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.27.15.115 DFECTRL1

Address offset: 0x910

Various configuration for Direction finding

| Bit number       |            |                   | 31      | 30                                                                        | 29                                                       | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |  |  |  |
|------------------|------------|-------------------|---------|---------------------------------------------------------------------------|----------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|--|--|--|
| ID               |            |                   |         |                                                                           |                                                          |    |    |    |    |    |    |    | I  | I  | I  | I  | H  | H  | H  | H  | G  | G  | G  | F  | E | E | E | C | C | C | B | A | A | A | A | A |  |  |  |
| Reset 0x00023282 |            |                   | 0       | 0                                                                         | 0                                                        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 1  | 1  | 0  | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |   |  |  |  |
| ID               | Acce Field | Value ID          | Value   | Description                                                               |                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
| A                | RW         | NUMBEROF8US       |         | Length of the AoA/AoD procedure in number of 8 us units                   |                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            |                   |         | Always used in TX mode, but in RX mode only when CTEINLINECTRLLEN is 0    |                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            |                   |         |                                                                           |                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
| B                | RW         | DFEINEXTENSION    |         | Add CTE extension and do antenna switching/sampling in this extension     |                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            |                   | CRC     | 1                                                                         | AoA/AoD procedure triggered at end of CRC                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            |                   | Payload | 0                                                                         | Antenna switching/sampling is done in the packet payload |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
| C                | RW         | TSWITCHSPACING    |         | Interval between every time the antenna is changed in the SWITCHING state |                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            |                   | 4us     | 1                                                                         | 4us                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            |                   | 2us     | 2                                                                         | 2us                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            |                   | 1us     | 3                                                                         | 1us                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
| E                | RW         | TSAMPLESPACINGREF |         | Interval between samples in the REFERENCE period                          |                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            |                   | 4us     | 1                                                                         | 4us                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            |                   | 2us     | 2                                                                         | 2us                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            |                   | 1us     | 3                                                                         | 1us                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            |                   | 500ns   | 4                                                                         | 0.5us                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            |                   | 250ns   | 5                                                                         | 0.25us                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  | 125ns      | 6                 | 0.125us |                                                                           |                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
| F                | RW         | SAMPLETYPE        |         | Whether to sample I/Q or magnitude/phase                                  |                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            |                   | IQ      | 0                                                                         | Complex samples in I and Q                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |  |

| Bit number       |              |                | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|--------------|----------------|---------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |              |                | I I I I H H H H G G G F E E E C C C B A A A A A A                                     |                                                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00023282 |              |                | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 1 1 0 0 1 0 1 0 0 0 0 0 1 0                       |                                                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Access Field | Value ID       | Value                                                                                 | Description                                                                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | MagPhase       | 1                                                                                     | Complex samples as magnitude and phase                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| G                | RW           | TSAMPLESPACING |                                                                                       | Interval between samples in the SWITCHING period when CTEINLINECTRLLEN is 0                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              |                |                                                                                       | <div>Note: Not used when CTEINLINECTRLLEN is set. Then either CTEINLINERXMODE1US or CTEINLINERXMODE2US are used.</div> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | 4us            | 1                                                                                     | 4us                                                                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | 2us            | 2                                                                                     | 2us                                                                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | 1us            | 3                                                                                     | 1us                                                                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | 500ns          | 4                                                                                     | 0.5us                                                                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | 250ns          | 5                                                                                     | 0.25us                                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | 125ns          | 6                                                                                     | 0.125us                                                                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| H                | RW           | REPEATPATTERN  |                                                                                       | Repeat every antenna pattern N times.                                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | NoRepeat       | 0                                                                                     | Do not repeat (1 time in total)                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| I                | RW           | AGCBACKOFFGAIN |                                                                                       | Gain will be lowered by the specified number of gain steps at the start of CTE                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              |                |                                                                                       | <div>Note: First LNAGAIN gain drops, then MIXGAIN, then AAFGAIN</div>                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.27.15.116 DFCTRL2

Address offset: 0x914

Start offset for Direction finding

| Bit number       |            |               | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |                                                                                                                                                        |  |  |  |  |  |  |  |  |  |  |  |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|---------------|---------------------------------------------------------------------------------------|--|--|--|--------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|-----------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |            |               | B B B B B B B B B B B B B B                                                           |  |  |  |                                                                                                                                                        |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A A A A A A A |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| ID               | Acce Field | Value ID      | Value                                                                                 |  |  |  | Description                                                                                                                                            |  |  |  |  |  |  |  |  |  |  |  |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | TSWITCHOFFSET |                                                                                       |  |  |  | Signed value offset after the end of the CRC before starting switching in number of 16M cycles                                                         |  |  |  |  |  |  |  |  |  |  |  |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW         | TSAMPLEOFFSET |                                                                                       |  |  |  | Signed value offset before starting sampling in number of 16M cycles relative to the beginning of the REFERENCE state<br>- 12 us after switching start |  |  |  |  |  |  |  |  |  |  |  |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.27.15.117 SWITCHPATTERN

Address offset: 0x928

GPIO patterns to be used for each antenna

Maximum 8 GPIOs can be controlled. To secure correct signal levels on the pins, the pins must be configured in the GPIO peripheral as described in Pin configuration.

If, during switching, the total number of antenna slots is bigger than the number of written patterns, the RADIO loops back to the pattern used after the reference pattern.

A minimum number of 3 patterns must be written.

| Bit number |  | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  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### 7.1.27.15.118 CLEARPATTERN

Address offset: 0x92C

Clear the GPIO pattern array for antenna control

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0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.27.15.119 PSEL.DFEGPIO[n] (n=0..7)

Address offset: 0x930 + (n × 0x4)

Pin select for DFE pin n

Must be set before enabling the radio

|                  |      |         |              |    |       |    |    |    |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |             |   |   |   |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|---------|--------------|----|-------|----|----|----|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|--|-------------|---|---|---|-------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |         |              | 31 | 30    | 29 | 28 | 27 | 26      | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |  |             |   |   |   |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |         |              | C  |       |    |    |    |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | B |   |   |   |   |   |   |   |   |  |  |  | A           | A | A | A | A           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0xFFFFFFFF |      |         |              | 1  | 1     | 1  | 1  | 1  | 1       | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  |  |  |             |   |   |   |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field   | Value        | ID | Value |    |    |    |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  | Description |   |   |   |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW   | PIN     |              |    |       |    |    |    | [0..31] |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |             |   |   |   | Pin number  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW   | PORT    |              |    |       |    |    |    | [0..1]  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |             |   |   |   | Port number |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW   | CONNECT |              |    |       |    |    |    |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |             |   |   |   | Connection  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |         | Disconnected |    |       |    |    |    | 1       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |             |   |   |   | Disconnect  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |         | Connected    |    |       |    |    |    | 0       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |             |   |   |   | Connect     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.27.15.120 DFEPACKET.PTR

Address offset: 0x950

Data pointer



|                  |            |  |          |       |    |    |    |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|-------|----|----|----|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31    | 30 | 29 | 28 | 27           | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |  |          | A     | A  | A  | A  | A            | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |          | 0     | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID | Value |    |    |    | Description  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW PTR     |  |          |       |    |    |    | Data pointer |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

**Note:** See the memory chapter for details about which memories are available for EasyDMA.

### 7.1.27.15.121 DFEPACKET.MAXCNT

Address offset: 0x954

Maximum number of buffer words to transfer

|                  |            |        |          |       |    |    |    |                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------|----------|-------|----|----|----|--------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |        |          | 31    | 30 | 29 | 28 | 27                                         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |
| ID               |            |        |          |       |    |    |    |                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  | A  | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00001000 |            |        |          | 0     | 0  | 0  | 0  | 0                                          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |   |   |   |
| ID               | Acce Field |        | Value ID | Value |    |    |    | Description                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | MAXCNT |          |       |    |    |    | Maximum number of buffer words to transfer |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.27.15.122 DFEPACKET.AMOUNT

Address offset: 0x958

Number of samples transferred in the last transaction

|                  |            |        |          |       |    |    |    |                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------|----------|-------|----|----|----|-------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |        |          | 31    | 30 | 29 | 28 | 27                                                    | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |        |          |       |    |    |    |                                                       |    |    |    |    |    |    |    |    |    |    |    | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |        |          | 0     | 0  | 0  | 0  | 0                                                     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |
| ID               | Acce Field |        | Value ID | Value |    |    |    | Description                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | R          | AMOUNT |          |       |    |    |    | Number of samples transferred in the last transaction |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.27.15.123 POWER

Address offset: 0xFFC

Peripheral power control

|                  |      |       |          |       |                                                                                                                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------|-------|----------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |      |       |          | 31    | 30                                                                                                                                                    | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |      |       |          |       |                                                                                                                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |
| Reset 0x00000001 |      |       |          | 0     | 0                                                                                                                                                     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| ID               | Acce | Field | Value ID | Value | Description                                                                                                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW   | POWER |          |       | Peripheral power control. The peripheral and its registers will be reset to its initial state by switching the peripheral off and then back on again. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |       | Disabled | 0     | Peripheral is powered off                                                                                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |       | Enabled  | 1     | Peripheral is powered on                                                                                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

## 7.1.27.16 Electrical specification

### 7.1.27.16.1 General radio characteristics

| Symbol                    | Description                      | Min. | Typ. | Max. | Units       |
|---------------------------|----------------------------------|------|------|------|-------------|
| $f_{OP}$                  | Operating frequencies            | ..   | ..   | ..   | MHz         |
| $f_{PLL,CH,SP}$           | PLL channel spacing              | ..   | ..   | ..   | MHz         |
| $f_{DELTA,1M}$            | Frequency deviation @ 1 Mbps     | ..   | ..   | ..   | kHz         |
| $f_{DELTA,BLE,1M}$        | Frequency deviation @ BLE 1 Mbps | ..   | ..   | ..   | kHz         |
| $f_{DELTA,2M}$            | Frequency deviation @ 2 Mbps     | ..   | ..   | ..   | kHz         |
| $f_{DELTA,BLE,2M}$        | Frequency deviation @ BLE 2 Mbps | ..   | ..   | ..   | kHz         |
| $fsk_{BPS}$               | On-the-air data rate             | ..   | ..   | ..   | kbps        |
| $f_{chip, IEEE 802.15.4}$ | Chip rate in IEEE 802.15.4 mode  | ..   | ..   | ..   | kchip,<br>s |

### 7.1.27.16.2 Radio current consumption (transmitter)

| Symbol                   | Description                                       | Min. | Typ. | Max. | Units |
|--------------------------|---------------------------------------------------|------|------|------|-------|
| $I_{TX,0dBm,DCDC}$       | TX only run current (DC/DC, 3 V) $P_{RF} = 0$ dBm |      | 3.2  |      | mA    |
| $I_{TX,0dBm}$            | TX only run current $P_{RF} = 0$ dBm              | ..   | ..   | ..   | mA    |
| $I_{TX,MINUS4dBm,DCDC}$  | TX only run current DC/DC, 3 V $P_{RF} = -4$ dBm  | ..   | ..   | ..   | mA    |
| $I_{TX,MINUS4dBm}$       | TX only run current $P_{RF} = -4$ dBm             | ..   | ..   | ..   | mA    |
| $I_{TX,MINUS8dBm,DCDC}$  | TX only run current DC/DC, 3 V $P_{RF} = -8$ dBm  | ..   | ..   | ..   | mA    |
| $I_{TX,MINUS8dBm}$       | TX only run current $P_{RF} = -8$ dBm             | ..   | ..   | ..   | mA    |
| $I_{TX,MINUS12dBm,DCDC}$ | TX only run current DC/DC, 3 V $P_{RF} = -12$ dBm | ..   | ..   | ..   | mA    |
| $I_{TX,MINUS12dBm}$      | TX only run current $P_{RF} = -12$ dBm            | ..   | ..   | ..   | mA    |
| $I_{TX,MINUS16dBm,DCDC}$ | TX only run current DC/DC, 3 V $P_{RF} = -16$ dBm | ..   | ..   | ..   | mA    |
| $I_{TX,MINUS16dBm}$      | TX only run current $P_{RF} = -16$ dBm            | ..   | ..   | ..   | mA    |
| $I_{TX,MINUS20dBm,DCDC}$ | TX only run current DC/DC, 3 V $P_{RF} = -20$ dBm | ..   | ..   | ..   | mA    |
| $I_{TX,MINUS20dBm}$      | TX only run current $P_{RF} = -20$ dBm            | ..   | ..   | ..   | mA    |
| $I_{TX,MINUS40dBm,DCDC}$ | TX only run current DC/DC, 3 V $P_{RF} = -40$ dBm | ..   | ..   | ..   | mA    |
| $I_{TX,MINUS40dBm}$      | TX only run current $P_{RF} = -40$ dBm            | ..   | ..   | ..   | mA    |
| $I_{START,TX,DCDC}$      | TX start-up current DC/DC, 3 V, $P_{RF} = 4$ dBm  | ..   | ..   | ..   | mA    |
| $I_{START,TX}$           | TX start-up current, $P_{RF} = 4$ dBm             | ..   | ..   | ..   | mA    |

### 7.1.27.16.3 Radio current consumption (Receiver)

| Symbol                 | Description                                        | Min. | Typ. | Max. | Units |
|------------------------|----------------------------------------------------|------|------|------|-------|
| $I_{RX,1M,DCDC}$       | RX only run current (DC/DC, 3 V) 1 Mbps/1 Mbps BLE |      | 2.6  |      | mA    |
| $I_{RX,1M}$            | RX only run current (LDO, 3 V) 1 Mbps/1 Mbps BLE   |      | 7.0  |      | mA    |
| $I_{RX,2M,DCDC}$       | RX only run current (DC/DC, 3 V) 2 Mbps/2 Mbps BLE |      | 3.0  |      | mA    |
| $I_{RX,2M}$            | RX only run current (LDO, 3 V) 2 Mbps/2 Mbps BLE   | ..   | ..   | ..   | mA    |
| $I_{START,RX,1M,DCDC}$ | RX start-up current (DC/DC, 3 V) 1 Mbps/1 Mbps BLE | ..   | ..   | ..   | mA    |
| $I_{START,RX,1M}$      | RX start-up current 1 Mbps/1 Mbps BLE              | ..   | ..   | ..   | mA    |

### 7.1.27.16.4 Transmitter specification

| Symbol     | Description            | Min. | Typ. | Max. | Units |
|------------|------------------------|------|------|------|-------|
| $P_{RF}$   | Maximum output power   |      | 3.0  |      | dBm   |
| $P_{RFC}$  | RF power control range | ..   | ..   | ..   | dB    |
| $P_{RFCR}$ | RF power accuracy      | ..   | ..   | ..   | dB    |

| Symbol                       | Description                                        | Min. | Typ. | Max. | Units |
|------------------------------|----------------------------------------------------|------|------|------|-------|
| $P_{RF1,1}$                  | 1st Adjacent Channel Transmit Power 1 MHz (1 Mbps) | ..   | ..   | ..   | dBc   |
| $P_{RF2,1}$                  | 2nd Adjacent Channel Transmit Power 2 MHz (1 Mbps) | ..   | ..   | ..   | dBc   |
| $P_{RF1,2}$                  | 1st Adjacent Channel Transmit Power 2 MHz (2 Mbps) | ..   | ..   | ..   | dBc   |
| $P_{RF2,2}$                  | 2nd Adjacent Channel Transmit Power 4 MHz (2 Mbps) | ..   | ..   | ..   | dBc   |
| $E_{vm}$                     | Error vector magnitude IEEE 802.15.4               | ..   | ..   | ..   | %rms  |
| $P_{harm2nd, IEEE 802.15.4}$ | 2nd harmonics in IEEE 802.15.4 mode                | ..   | ..   | ..   | dBm   |
| $P_{harm3rd, IEEE 802.15.4}$ | 3rd harmonics in IEEE 802.15.4                     | ..   | ..   | ..   | dBm   |

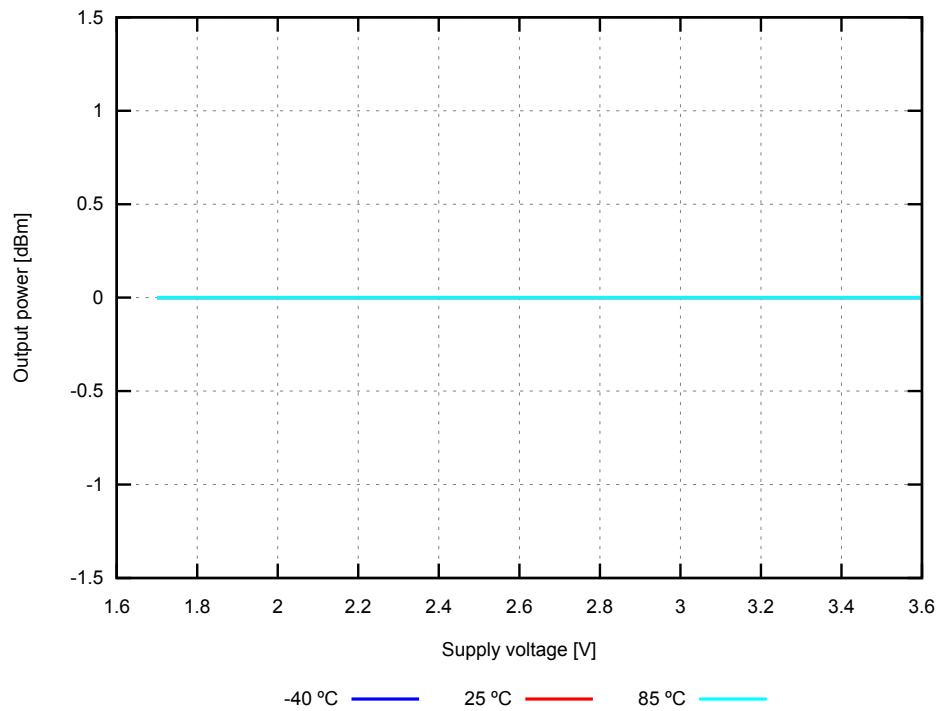


Figure 164: Output power, 1 Mbps Bluetooth low energy mode, at maximum TXPOWER setting (typical values)

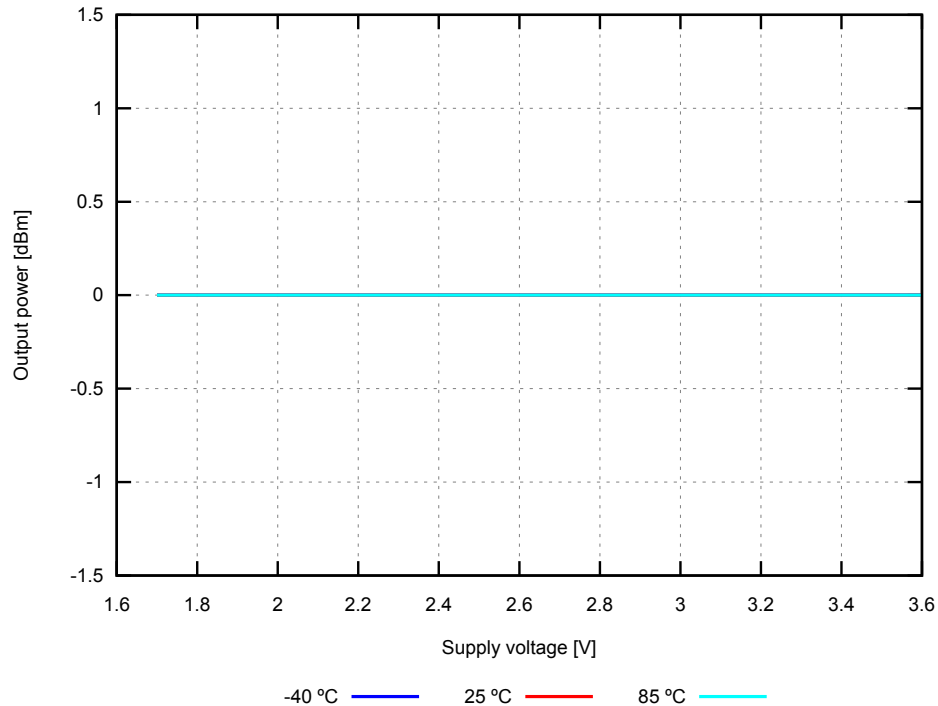


Figure 165: Output power, 1 Mbps Bluetooth low energy mode, at 0 dBm TXPOWER setting (typical values)

### 7.1.27.16.5 Receiver operation

| Symbol                          | Description                                                                                 | Min. | Typ.  | Max. | Units |
|---------------------------------|---------------------------------------------------------------------------------------------|------|-------|------|-------|
| P <sub>RX,MAX</sub>             | Maximum received signal strength at < 0.1% PER                                              | ..   | ..    | ..   | dBm   |
| P <sub>SENS,IT,1M</sub>         | Sensitivity, 1 Mbps nRF mode ideal transmitter <sup>14</sup>                                | ..   | ..    | ..   | dBm   |
| P <sub>SENS,IT,2M</sub>         | Sensitivity, 2 Mbps nRF mode ideal transmitter <sup>15</sup>                                | ..   | ..    | ..   | dBm   |
| P <sub>SENS,IT,SP,1M,BLE</sub>  | Sensitivity, 1 Mbps BLE ideal transmitter, packet length ≤ 37 bytes BER=1E-3 <sup>16</sup>  |      | -97.5 |      | dBm   |
| P <sub>SENS,IT,LP,1M,BLE</sub>  | Sensitivity, 1 Mbps BLE ideal transmitter, packet length ≥ 128 bytes BER=1E-4 <sup>17</sup> | ..   | ..    | ..   | dBm   |
| P <sub>SENS,IT,SP,2M,BLE</sub>  | Sensitivity, 2 Mbps BLE ideal transmitter, packet length ≤ 37 bytes                         |      | -94.3 |      | dBm   |
| P <sub>SENS,IT,BLE LE125k</sub> | Sensitivity, 125 kbps BLE mode                                                              | ..   | ..    | ..   | dBm   |
| P <sub>SENS,IT,BLE LE500k</sub> | Sensitivity, 500 kbps BLE mode                                                              | ..   | ..    | ..   | dBm   |
| P <sub>SENS,IEEE 802.15.4</sub> | Sensitivity in IEEE 802.15.4 mode                                                           | ..   | ..    | ..   | dBm   |

<sup>14</sup> Typical sensitivity applies when ADDR0 is used for receiver address correlation. When ADDR[1...7] are used for receiver address correlation, the typical sensitivity for this mode is degraded by 3 dB.

<sup>15</sup> Typical sensitivity applies when ADDR0 is used for receiver address correlation. When ADDR[1..7] are used for receiver address correlation, the typical sensitivity for this mode is degraded by 3 dB.

<sup>16</sup> As defined in the *Bluetooth Core Specification v4.0 Volume 6: Core System Package (Low Energy Controller Volume)*

<sup>17</sup> Equivalent BER limit < 10E-04

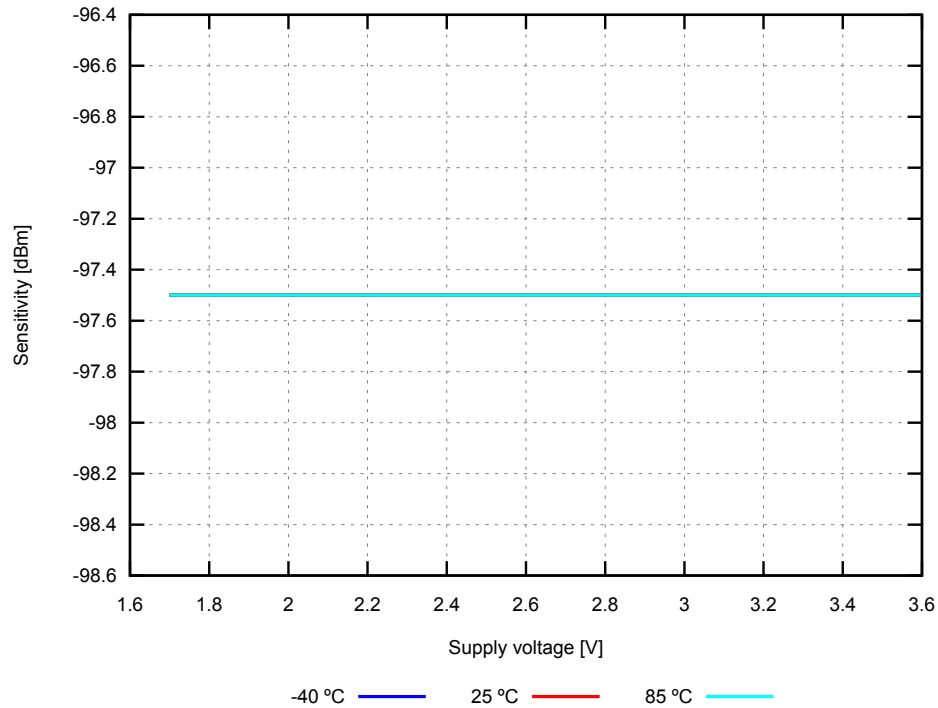


Figure 166: Sensitivity, 1 Mbps Bluetooth low energy mode, Regulator = LDO (typical values)

### 7.1.27.16.6 RX selectivity

RX selectivity with equal modulation on interfering signal<sup>18</sup>

| Symbol                          | Description                                              | Min. | Typ. | Max. | Units |
|---------------------------------|----------------------------------------------------------|------|------|------|-------|
| C/I <sub>1M,co-channel</sub>    | 1Mbps mode, Co-Channel interference                      | ..   | ..   | ..   | dB    |
| C/I <sub>1M,-1MHz</sub>         | 1 Mbps mode, Adjacent (-1 MHz) interference              | ..   | ..   | ..   | dB    |
| C/I <sub>1M,+1MHz</sub>         | 1 Mbps mode, Adjacent (+1 MHz) interference              | ..   | ..   | ..   | dB    |
| C/I <sub>1M,-2MHz</sub>         | 1 Mbps mode, Adjacent (-2 MHz) interference              | ..   | ..   | ..   | dB    |
| C/I <sub>1M,+2MHz</sub>         | 1 Mbps mode, Adjacent (+2 MHz) interference              | ..   | ..   | ..   | dB    |
| C/I <sub>1M,-3MHz</sub>         | 1 Mbps mode, Adjacent (-3 MHz) interference              | ..   | ..   | ..   | dB    |
| C/I <sub>1M,+3MHz</sub>         | 1 Mbps mode, Adjacent (+3 MHz) interference              | ..   | ..   | ..   | dB    |
| C/I <sub>1M,±6MHz</sub>         | 1 Mbps mode, Adjacent (≥6 MHz) interference              | ..   | ..   | ..   | dB    |
| C/I <sub>1MBLE,co-channel</sub> | 1 Mbps BLE mode, Co-Channel interference                 | ..   | ..   | ..   | dB    |
| C/I <sub>1MBLE,-1MHz</sub>      | 1 Mbps BLE mode, Adjacent (-1 MHz) interference          | ..   | ..   | ..   | dB    |
| C/I <sub>1MBLE,+1MHz</sub>      | 1 Mbps BLE mode, Adjacent (+1 MHz) interference          | ..   | ..   | ..   | dB    |
| C/I <sub>1MBLE,-2MHz</sub>      | 1 Mbps BLE mode, Adjacent (-2 MHz) interference          | ..   | ..   | ..   | dB    |
| C/I <sub>1MBLE,+2MHz</sub>      | 1 Mbps BLE mode, Adjacent (+2 MHz) interference          | ..   | ..   | ..   | dB    |
| C/I <sub>1MBLE,&gt;3MHz</sub>   | 1 Mbps BLE mode, Adjacent (≥3 MHz) interference          | ..   | ..   | ..   | dB    |
| C/I <sub>1MBLE,image</sub>      | Image frequency interference                             | ..   | ..   | ..   | dB    |
| C/I <sub>1MBLE,image,1MHz</sub> | Adjacent (1 MHz) interference to in-band image frequency | ..   | ..   | ..   | dB    |
| C/I <sub>2M,co-channel</sub>    | 2 Mbps mode, Co-Channel interference                     | ..   | ..   | ..   | dB    |
| C/I <sub>2M,-2MHz</sub>         | 2 Mbps mode, Adjacent (-2 MHz) interference              | ..   | ..   | ..   | dB    |
| C/I <sub>2M,+2MHz</sub>         | 2 Mbps mode, Adjacent (+2 MHz) interference              | ..   | ..   | ..   | dB    |
| C/I <sub>2M,-4MHz</sub>         | 2 Mbps mode, Adjacent (-4 MHz) interference              | ..   | ..   | ..   | dB    |
| C/I <sub>2M,+4MHz</sub>         | 2 Mbps mode, Adjacent (+4 MHz) interference              | ..   | ..   | ..   | dB    |

<sup>18</sup> Desired signal level at PIN = -67 dBm. One interferer is used, having equal modulation as the desired signal. The input power of the interferer where the sensitivity equals BER = 0.1% is presented

| Symbol                                | Description                                              | Min. | Typ. | Max. | Units |
|---------------------------------------|----------------------------------------------------------|------|------|------|-------|
| C/I <sub>2M,-6MHz</sub>               | 2 Mbps mode, Adjacent (-6 MHz) interference              | ..   | ..   | ..   | dB    |
| C/I <sub>2M,+6MHz</sub>               | 2 Mbps mode, Adjacent (+6 MHz) interference              | ..   | ..   | ..   | dB    |
| C/I <sub>2M,≥12MHz</sub>              | 2 Mbps mode, Adjacent (≥12 MHz) interference             | ..   | ..   | ..   | dB    |
| C/I <sub>2M BLE,co-channel</sub>      | 2 Mbps BLE mode, Co-Channel interference                 | ..   | ..   | ..   | dB    |
| C/I <sub>2M BLE,±2MHz</sub>           | 2 Mbps BLE mode, Adjacent (±2 MHz) interference          | ..   | ..   | ..   | dB    |
| C/I <sub>2M BLE,±4MHz</sub>           | 2 Mbps BLE mode, Adjacent (±4 MHz) interference          | ..   | ..   | ..   | dB    |
| C/I <sub>2M BLE,≥6MHz</sub>           | 2 Mbps BLE mode, Adjacent (≥6 MHz) interference          | ..   | ..   | ..   | dB    |
| C/I <sub>2M BLE,image</sub>           | Image frequency interference                             | ..   | ..   | ..   | dB    |
| C/I <sub>2M BLE,image, 2MHz</sub>     | Adjacent (2 MHz) interference to in-band image frequency | ..   | ..   | ..   | dB    |
| C/I <sub>125k BLE LR,co-channel</sub> | 125 kbps BLE LR mode, Co-Channel interference            | ..   | ..   | ..   | dB    |
| C/I <sub>125k BLE LR,-1MHz</sub>      | 125 kbps BLE LR mode, Adjacent (-1 MHz) interference     | ..   | ..   | ..   | dB    |
| C/I <sub>125k BLE LR,+1MHz</sub>      | 125 kbps BLE LR mode, Adjacent (+1 MHz) interference     | ..   | ..   | ..   | dB    |
| C/I <sub>125k BLE LR,-2MHz</sub>      | 125 kbps BLE LR mode, Adjacent (-2 MHz) interference     | ..   | ..   | ..   | dB    |
| C/I <sub>125k BLE LR,+2MHz</sub>      | 125 kbps BLE LR mode, Adjacent (+2 MHz) interference     | ..   | ..   | ..   | dB    |
| C/I <sub>125k BLE LR,≥3MHz</sub>      | 125 kbps BLE LR mode, Adjacent (≥3 MHz) interference     | ..   | ..   | ..   | dB    |
| C/I <sub>125k BLE LR,image</sub>      | Image frequency interference                             | ..   | ..   | ..   | dB    |
| C/I <sub>IEEE 802.15.4,-5MHz</sub>    | IEEE 802.15.4 mode, Adjacent (-5 MHz) rejection          | ..   | ..   | ..   | dB    |
| C/I <sub>IEEE 802.15.4,+5MHz</sub>    | IEEE 802.15.4 mode, Adjacent (+5 MHz) rejection          | ..   | ..   | ..   | dB    |
| C/I <sub>IEEE 802.15.4, 10MHz </sub>  | IEEE 802.15.4 mode, Alternate (10 MHz) rejection         | ..   | ..   | ..   | dB    |

### 7.1.27.16.7 RX intermodulation

#### RX intermodulation<sup>19</sup>

| Symbol                      | Description                                                               | Min. | Typ. | Max. | Units |
|-----------------------------|---------------------------------------------------------------------------|------|------|------|-------|
| P <sub>IMD,5TH,1M</sub>     | IMD performance, 1 Mbps, 5th offset channel, packet length ≤ 37 bytes     | ..   | ..   | ..   | dBm   |
| P <sub>IMD,5TH,1M,BLE</sub> | IMD performance, BLE 1 Mbps, 5th offset channel, packet length ≤ 37 bytes | ..   | ..   | ..   | dBm   |
| P <sub>IMD,5TH,2M</sub>     | IMD performance, 2 Mbps, 5th offset channel, packet length ≤ 37 bytes     | ..   | ..   | ..   | dBm   |
| P <sub>IMD,5TH,2M,BLE</sub> | IMD performance, BLE 2 Mbps, 5th offset channel, packet length ≤ 37 bytes | ..   | ..   | ..   | dBm   |

### 7.1.27.16.8 Radio timing

| Symbol                        | Description                                                                                                              | Min. | Typ. | Max. | Units |
|-------------------------------|--------------------------------------------------------------------------------------------------------------------------|------|------|------|-------|
| t <sub>TXEN,BLE,1M</sub>      | Time between TXEN task and READY event after channel FREQUENCY configured (1 Mbps BLE and 150 μs TIFS)                   | ..   | ..   | ..   | μs    |
| t <sub>TXEN,FAST,BLE,1M</sub> | Time between TXEN task and READY event after channel FREQUENCY configured (1 Mbps BLE with fast ramp-up and 150 μs TIFS) | ..   | ..   | ..   | μs    |
| t <sub>TXDIS,BLE,1M</sub>     | When in TX, delay between DISABLE task and DISABLED event for MODE = Nrf_1Mbit and MODE = Ble_1Mbit                      | ..   | ..   | ..   | μs    |
| t <sub>RXEN,BLE,1M</sub>      | Time between the RXEN task and READY event after channel FREQUENCY configured (1 Mbps BLE)                               | ..   | ..   | ..   | μs    |

<sup>19</sup> Desired signal level at PIN = -64 dBm. Two interferers with equal input power are used. The interferer closest in frequency is not modulated, the other interferer is modulated equal with the desired signal. The input power of the interferers where the sensitivity equals BER = 0.1% is presented.

| Symbol                         | Description                                                                                                     | Min. | Typ. | Max. | Units   |
|--------------------------------|-----------------------------------------------------------------------------------------------------------------|------|------|------|---------|
| $t_{RXEN,FAST,BLE,1M}$         | Time between the RXEN task and READY event after channel FREQUENCY configured (1 Mbps BLE with fast ramp-up)    | ..   | ..   | ..   | $\mu s$ |
| $t_{RXDIS,BLE,1M}$             | When in RX, delay between DISABLE task and DISABLED event for MODE = Nrf_1Mbit and MODE = Ble_1Mbit             | ..   | ..   | ..   | $\mu s$ |
| $t_{TXDIS,BLE,2M}$             | When in TX, delay between DISABLE task and DISABLED event for MODE = Nrf_2Mbit and MODE = Ble_2Mbit             | ..   | ..   | ..   | $\mu s$ |
| $t_{RXDIS,BLE,2M}$             | When in RX, delay between DISABLE task and DISABLED event for MODE = Nrf_2Mbit and MODE = Ble_2Mbit             | ..   | ..   | ..   | $\mu s$ |
| $t_{TXEN,IEEE\ 802.15.4}$      | Time between TXEN task and READY event after channel FREQUENCY configured (IEEE 802.15.4)                       | ..   | ..   | ..   | $\mu s$ |
| $t_{TXEN,FAST,IEEE\ 802.15.4}$ | Time between TXEN task and READY event after channel FREQUENCY configured (IEEE 802.15.4 with fast ramp-up)     | ..   | ..   | ..   | $\mu s$ |
| $t_{TXDIS,IEEE\ 802.15.4}$     | When in TX, delay between DISABLE task and DISABLED event (IEEE 802.15.4)                                       | ..   | ..   | ..   | $\mu s$ |
| $t_{RXEN,IEEE\ 802.15.4}$      | Time between the RXEN task and READY event after channel FREQUENCY configured (IEEE 802.15.4)                   | ..   | ..   | ..   | $\mu s$ |
| $t_{RXEN,FAST,IEEE\ 802.15.4}$ | Time between the RXEN task and READY event after channel FREQUENCY configured (IEEE 802.15.4 with fast ramp-up) | ..   | ..   | ..   | $\mu s$ |
| $t_{RXDIS,IEEE\ 802.15.4}$     | When in RX, delay between DISABLE task and DISABLED event (IEEE 802.15.4)                                       | ..   | ..   | ..   | $\mu s$ |
| $t_{RX-to-TX\ turnaround}$     | Maximum TX-to-RX or RX-to-TX turnaround time in IEEE 802.15.4 mode                                              | ..   | ..   | ..   | $\mu s$ |

### 7.1.27.16.9 Received signal strength indicator (RSSI) specifications

| Symbol              | Description                                  | Min. | Typ. | Max. | Units   |
|---------------------|----------------------------------------------|------|------|------|---------|
| $RSSI_{ACC}$        | RSSI accuracy valid range -90 to -20 dBm     | ..   | ..   | ..   | dB      |
| $RSSI_{RESOLUTION}$ | RSSI resolution                              | ..   | ..   | ..   | dB      |
| $RSSI_{PERIOD}$     | RSSI sampling time from RSSI_START task      | ..   | ..   | ..   | $\mu s$ |
| $RSSI_{SETTLE}$     | RSSI settling time after signal level change | ..   | ..   | ..   | $\mu s$ |

### 7.1.27.16.10 Jitter

| Symbol                | Description                                                                                     | Min. | Typ. | Max. | Units   |
|-----------------------|-------------------------------------------------------------------------------------------------|------|------|------|---------|
| $t_{DISABLED/JITTER}$ | Jitter on DISABLED event relative to END event when shortcut between END and DISABLE is enabled | ..   | ..   | ..   | $\mu s$ |
| $t_{READY/JITTER}$    | Jitter on READY event relative to TXEN and RXEN task                                            | ..   | ..   | ..   | $\mu s$ |

### 7.1.27.16.11 IEEE 802.15.4 energy detection constants

| Symbol          | Description                                                           | Min. | Typ. | Max. | Units |
|-----------------|-----------------------------------------------------------------------|------|------|------|-------|
| $ED\_RSSISCALE$ | Scaling value when converting between hardware-reported value and dBm | 4    | 4    | 4    |       |
| $ED\_RSSIOFFS$  | Offset value when converting between hardware-reported value and dBm  | -92  | -92  | -92  |       |

## 7.1.28 RNG — Random number generator

The Random number generator (RNG) generates true non-deterministic random numbers based on internal thermal noise that are suitable for cryptographic purposes. The RNG does not require a seed value.

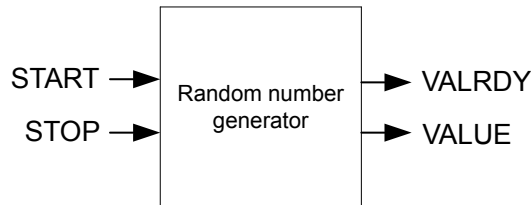


Figure 167: Random number generator

The RNG is started by triggering the START task and stopped by triggering the STOP task. When started, new random numbers are generated continuously and written to the VALUE register when ready. A VALRDY event is generated for every new random number that is written to the VALUE register. This means that after a VALRDY event is generated the CPU has the time until the next VALRDY event to read out the random number from the VALUE register before it is overwritten by a new random number.

### 7.1.28.1 Bias correction

A bias correction algorithm is employed on the internal bit stream to remove any bias toward '1' or '0'. The bits are then queued into an eight-bit register for parallel readout from the VALUE register.

It is possible to enable bias correction in the CONFIG register. This will result in slower value generation, but will ensure a statistically uniform distribution of the random values.

### 7.1.28.2 Speed

The time needed to generate one random byte of data is unpredictable, and may vary from one byte to the next. This is especially true when bias correction is enabled.

### 7.1.28.3 Registers

| Base address | Domain  | Peripheral | Instance | Secure mapping | DMA security | Description             | Configuration |
|--------------|---------|------------|----------|----------------|--------------|-------------------------|---------------|
| 0x41009000   | NETWORK | RNG        | RNG      | NS             | NA           | Random number generator |               |

Table 132: Instances

| Register        | Offset | Security | Description                                                                     |
|-----------------|--------|----------|---------------------------------------------------------------------------------|
| TASKS_START     | 0x000  |          | Task starting the random number generator                                       |
| TASKS_STOP      | 0x004  |          | Task stopping the random number generator                                       |
| SUBSCRIBE_START | 0x080  |          | Subscribe configuration for task <a href="#">START</a>                          |
| SUBSCRIBE_STOP  | 0x084  |          | Subscribe configuration for task <a href="#">STOP</a>                           |
| EVENTS_VALRDY   | 0x100  |          | Event being generated for every new random number written to the VALUE register |
| PUBLISH_VALRDY  | 0x180  |          | Publish configuration for event <a href="#">VALRDY</a>                          |
| SHORTS          | 0x200  |          | Shortcuts between local events and tasks                                        |
| INTENSET        | 0x304  |          | Enable interrupt                                                                |
| INTENCLR        | 0x308  |          | Disable interrupt                                                               |
| CONFIG          | 0x504  |          | Configuration register                                                          |



| Register | Offset | Security | Description          |
|----------|--------|----------|----------------------|
| VALUE    | 0x508  |          | Output random number |

Table 133: Register overview

### 7.1.28.3.1 TASKS\_START

Address offset: 0x000

Task starting the random number generator

| Bit number       |            |             |       | 31                                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |
|------------------|------------|-------------|-------|-------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|
| ID               |            |             |       | A                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
| Reset 0x00000000 |            |             |       | 0                                         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |
| ID               | Acce Field | Value ID    | Value | Description                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
| A                | W          | TASKS_START |       | Task starting the random number generator |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            | Trigger     | 1     | Trigger task                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |

### 7.1.28.3.2 TASKS\_STOP

Address offset: 0x004

Task stopping the random number generator

|                  |              |          |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|--------------|----------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |              |          |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |              |          |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |              |          |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field   | Value ID | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W TASKS_STOP |          |       | Task stopping the random number generator                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Trigger  | 1     | Trigger task                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.28.3.3 SUBSCRIBE\_START

Address offset: 0x080

Subscribe configuration for task **START**

|                  |            |          |                                                                                       |                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|--------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          | B A A A A A A A                                                                       |                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                              | Channel that task <b>START</b> will subscribe to |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW EN      |          |                                                                                       |                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Disable subscription                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Enable subscription                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.28.3.4 SUBSCRIBE\_STOP

Address offset: 0x084

Subscribe configuration for task **STOP**

|                  |            |          |          |    |                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|----|-------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          | 31       | 30 | 29                                                    | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |          | B        |    |                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A |
| Reset 0x00000000 |            |          | 0        | 0  | 0                                                     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |
| ID               | Acce Field | Value ID | Value    |    | Description                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] |    | Channel that task <span>STOP</span> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |    |                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        |    | Disable subscription                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        |    | Enable subscription                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.28.3.5 EVENTS\_VALRDY

Address offset: 0x100

Event being generated for every new random number written to the VALUE register

|                  |            |               |       |    |                                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|---------------|-------|----|---------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |               | 31    | 30 | 29                                                                              | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |               | A     |    |                                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |               | 0     | 0  | 0                                                                               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID      | Value |    | Description                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | EVENTS_VALRDY |       |    | Event being generated for every new random number written to the VALUE register |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | NotGenerated  | 0     |    | Event not generated                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Generated     | 1     |    | Event generated                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 7.1.28.3.6 PUBLISH\_VALRDY

Address offset: 0x180

Publish configuration for event VALRDY

|                  |            |  |          |                                                                         |    |                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|-------------------------------------------------------------------------|----|--------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31                                                                      | 30 | 29                                         | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |  |          | B                                                                       |    |                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |    |                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field |  | Value ID | Value                                                                   |    | Description                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          | [255..0]                                                                |    | Channel that event VALRDY will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |                                                                         |    |                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled | 0                                                                       |    | Disable publishing                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  | 1                                                                       |    | Enable publishing                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.28.3.7 SHORTS

Address offset: 0x200

## Shortcuts between local events and tasks

|                  |            |             |          |       |    |                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |  |
|------------------|------------|-------------|----------|-------|----|---------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|---|--|
| Bit number       |            |             |          | 31    | 30 | 29                                          | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |   |  |
| ID               |            |             |          |       |    |                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | A |  |
| Reset 0x00000000 |            |             |          | 0     | 0  | 0                                           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |   |  |
| ID               | Acce Field |             | Value ID | Value |    | Description                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |  |
| A                | RW         | VALRDY_STOP |          |       |    | Shortcut between event VALRDY and task STOP |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |  |
|                  |            |             | Disabled | 0     |    | Disable shortcut                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |  |
|                  |            |             | Enabled  | 1     |    | Enable shortcut                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |  |

### 7.1.28.3.8 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |            |          | A                                                                                     |                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW VALRDY  |          |                                                                                       | Write '1' to enable interrupt for event VALRDY |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Set      | 1                                                                                     | Enable                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Read: Disabled                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Read: Enabled                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.28.3.9 INTENCLR

Address offset: 0x308

Disable interrupt

|                  |            |          |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW VALRDY  |          |       | Write '1' to disable interrupt for event VALRDY                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Clear    | 1     | Disable                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0     | Read: Disabled                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1     | Read: Enabled                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.28.3.10 CONFIG

Address offset: 0x504

Configuration register

|                  |            |        |          |                                                                                       |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|--------|----------|---------------------------------------------------------------------------------------|-----------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |        |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |        |          | A                                                                                     |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |        |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field |        | Value ID | Value                                                                                 | Description     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | DERCEN |          |                                                                                       | Bias correction |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |        | Disabled | 0                                                                                     | Disabled        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |        | Enabled  | 1                                                                                     | Enabled         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.28.3.11 VALUE

Address offset: 0x508

Output random number

|                  |      |       |          |                                                                                       |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|-------|----------|---------------------------------------------------------------------------------------|-------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |       |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |       |          | A A A A A A A A                                                                       |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |       |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field | Value ID | Value                                                                                 | Description             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | R    | VALUE |          | [0..255]                                                                              | Generated random number |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

## 7.1.28.4 Electrical specification

### 7.1.28.4.1 RNG Electrical Specification

| Symbol                 | Description                                                                                                                            | Min. | Typ. | Max. | Units         |
|------------------------|----------------------------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| $t_{\text{RNG,START}}$ | Time from setting the START task to generation begins.<br>This is a one-time delay on START signal and does not apply between samples. | ..   | ..   | ..   | $\mu\text{s}$ |
| $t_{\text{RNG,RAW}}$   | Run time per byte without bias correction. Uniform distribution of 0 and 1 is not guaranteed.                                          | ..   | ..   | ..   | $\mu\text{s}$ |
| $t_{\text{RNG,BC}}$    | Run time per byte with bias correction. Uniform distribution of 0 and 1 is guaranteed. Time to generate a byte cannot be guaranteed.   | ..   | ..   | ..   | $\mu\text{s}$ |

## 7.1.29 RTC — Real-time counter

The real-time counter (RTC) module provides a generic, low-power timer on the low frequency clock source (LFCLK).

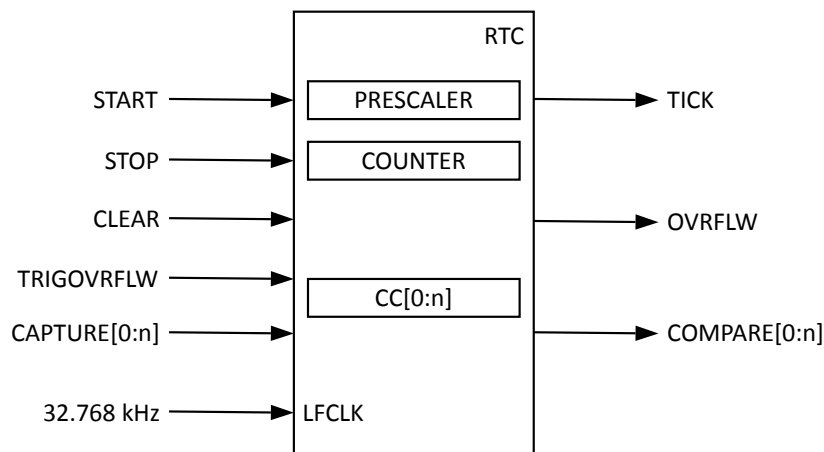


Figure 168: RTC block diagram

The RTC module features a 24-bit COUNTER, a 12-bit (1/X) prescaler, capture/compare registers, and a tick event generator.

### 7.1.29.1 Clock source

The RTC will run off the LFCLK.

When started, the RTC will automatically request the LFCLK source with RC oscillator if the LFCLK is not already running.

See [CLOCK — Clock control](#) on page 61 for more information about clock sources.

### 7.1.29.2 Resolution versus overflow and the prescaler

The relationship between the prescaler, counter resolution and overflow is summarized in the table below.

| Prescaler  | Counter resolution | Overflow       |
|------------|--------------------|----------------|
| 0          | 30.517 $\mu$ s     | 512 seconds    |
| $2^8-1$    | 7812.5 $\mu$ s     | 131072 seconds |
| $2^{12}-1$ | 125 ms             | 582.542 hours  |

Table 134: RTC resolution versus overflow

The counter increment frequency is given by the following equation:

$$f_{\text{RTC}} [\text{kHz}] = 32.768 / (\text{PRESCALER} + 1)$$

The **PRESCALER** register can only be written when the RTC is stopped.

The prescaler is restarted on tasks **START**, **CLEAR** and **TRIGOVRFW**. That is, the prescaler value is latched to an internal register (<<PRESC>>) on these tasks.

Examples:

1. Desired COUNTER frequency 100 Hz (10 ms counter period)

$$\text{PRESCALER} = \text{round}(32.768 \text{ kHz} / 100 \text{ Hz}) - 1 = 327$$

$$f_{\text{RTC}} = 99.9 \text{ Hz}$$

$$10009.576 \mu\text{s counter period}$$

2. Desired COUNTER frequency 8 Hz (125 ms counter period)

$$\text{PRESCALER} = \text{round}(32.768 \text{ kHz} / 8 \text{ Hz}) - 1 = 4095$$

$$f_{\text{RTC}} = 8 \text{ Hz}$$

$$125 \text{ ms counter period}$$

### 7.1.29.3 Counter register

The internal <<COUNTER>> register increments on LFCLK when the internal **PRESCALER** register (<<PRESC>>) is 0x00. <<PRESC>> is reloaded from the **PRESCALER** register. If enabled, the **TICK** event occurs on each increment of the **COUNTER**.

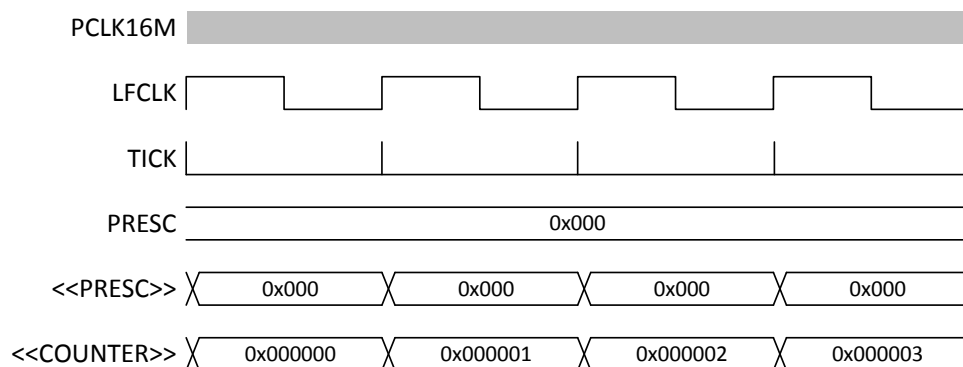


Figure 169: Timing diagram - COUNTER\_PRESCALER\_0

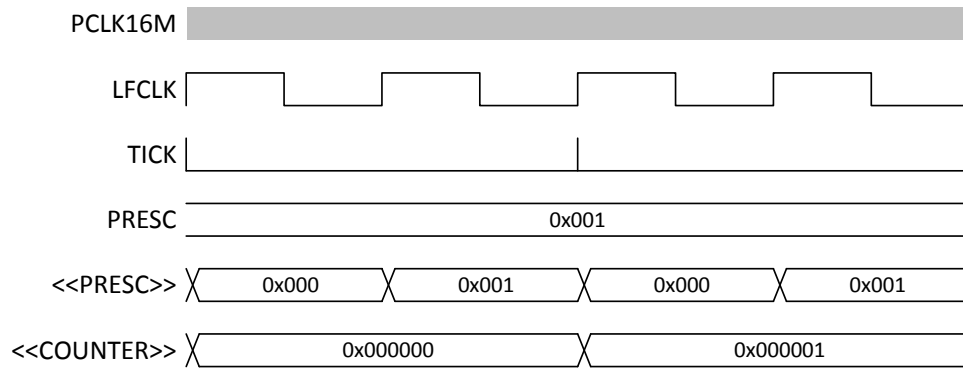


Figure 170: Timing diagram - COUNTER\_PRESCALER\_1

### 7.1.29.3.1 Reading the counter register

To read the COUNTER register, the internal <<COUNTER>> value is sampled.

To ensure that the <<COUNTER>> is safely sampled (considering that an LFCLK transition may occur during a read), the CPU and core memory bus are halted for four PCLK16M cycles. In addition, the read takes the CPU two PCLK16M cycles, resulting in the COUNTER register read taking maximum six PCLK16M clock cycles.

### 7.1.29.4 Overflow

An **OVRFLW** event is generated on **COUNTER** register overflow (overflowing from 0xFFFFF to 0).

The **TRIGOVRFLW** task will set the **COUNTER** value to 0xFFFFF0, to allow software test of the overflow condition.

**Note:** The **OVRFLW** event is disabled by default.

### 7.1.29.5 Tick event

The **TICK** event enables low-power tickless RTOS implementation, as it optionally provides a regular interrupt source for an RTOS with no need for use of the ARM SysTick feature.

Using the **TICK** event, rather than the SysTick, allows the CPU to be powered down while keeping RTOS scheduling active.

**Note:** The **TICK** event is disabled by default.

### 7.1.29.6 Event control

To optimize the RTC power consumption, events in the RTC can be individually disabled to prevent PCLK16M and HFCLK from being requested when those events are triggered. This is managed using the **EVTEN** register. Especially important is the **TICK** event.

This means that the RTC implements a slightly different task and event system compared to the standard system described in [Peripheral interface](#) on page 136. The RTC task and event system is illustrated in the figure below.

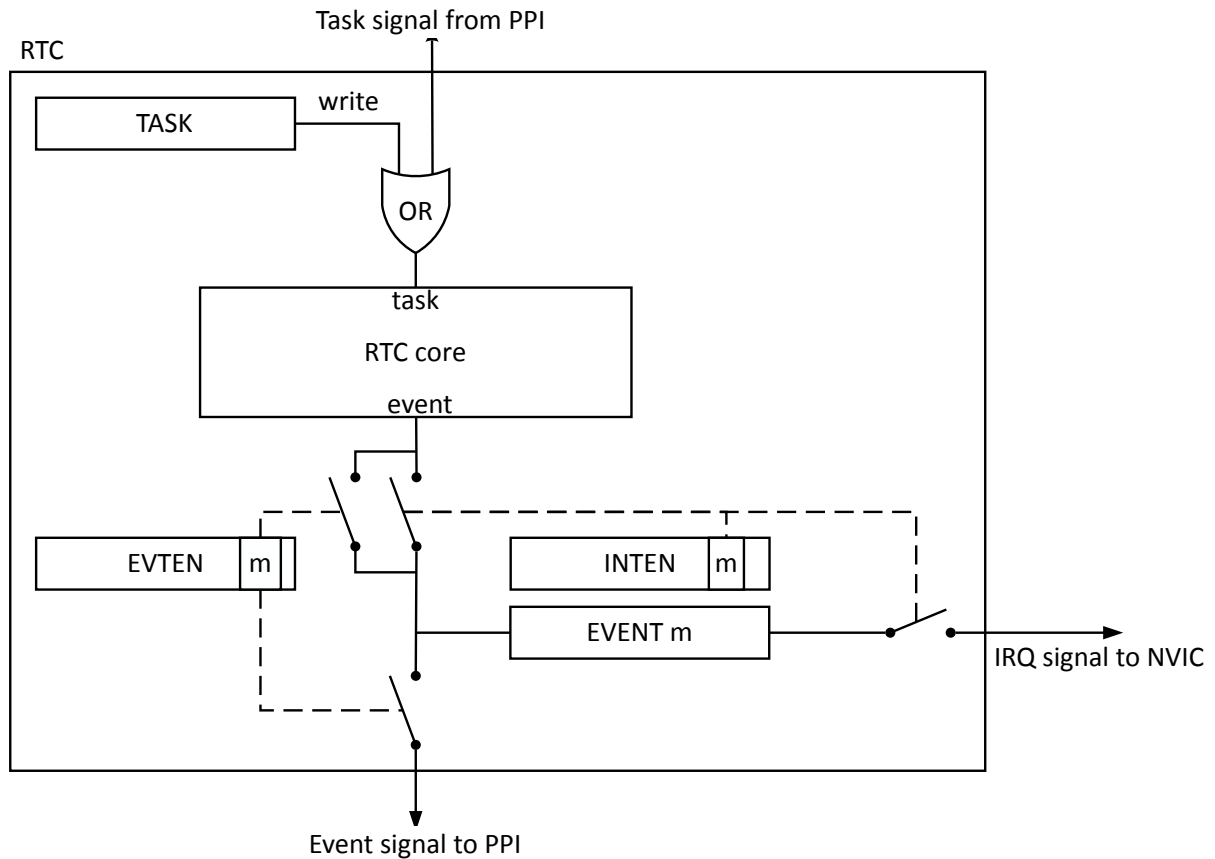


Figure 171: Tasks, events and interrupts in the RTC

### 7.1.29.7 Capture

The RTC implements one capture task for every available capture/compare register.

Every time `TASKS_CAPTURE[n]` is triggered, `<<COUNTER>>` is copied to the corresponding `CC[n]` register.

If the `CAPTURE` and `CLEAR` tasks are triggered at the same time, the `CAPTURE` task will be prioritized. This means that the `CC[n]` register for the corresponding `CAPTURE[n]` task will be set to the captured value before the counter is reset. There is a delay of 6 PCLK16M periods from when the `TASKS_CAPTURE[n]` is triggered until the corresponding `CC[n]` register is updated.

The `CAPTURE[n]` tasks will not generate `COMPARE[n]` events, even though `CC[n]` will then equal the COUNTER.

### 7.1.29.8 Compare

The RTC implements one `COMPARE` event for every available compare register.

When the `COUNTER` is incremented and then becomes equal to the value specified in the register `CC[n]`, the corresponding compare event `COMPARE[n]` is generated.

When writing a `CC[n]` register, the following behavior of the RTC `COMPARE` event should be noted:

- If a `CC` value is 0 when a `CLEARCLEAR` task is set, this will not trigger a `COMPARE` event.

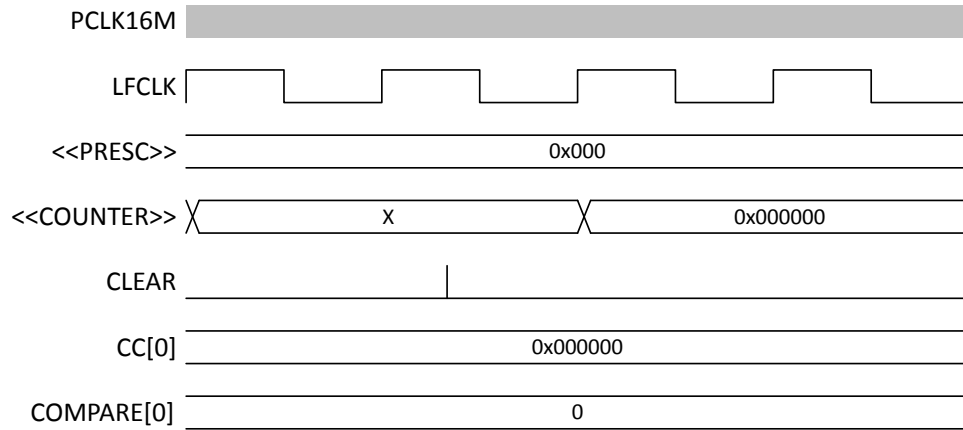


Figure 172: Timing diagram - COMPARE\_CLEAR

- If a **CC** value is N, and the **COUNTER** value is N when the **START** task is set, this will not trigger a **COMPARE** event.

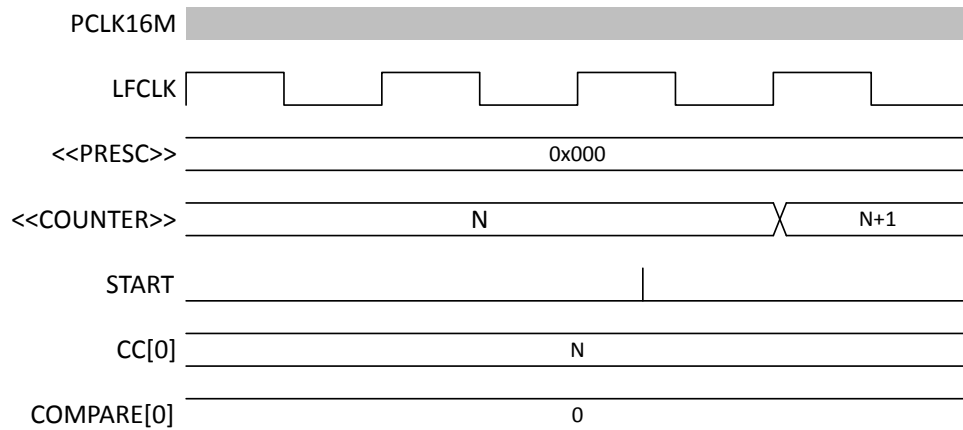


Figure 173: Timing diagram - COMPARE\_START

- A **COMPARE** event occurs when a **CC** value is N, and the **COUNTER** value transitions from N-1 to N.

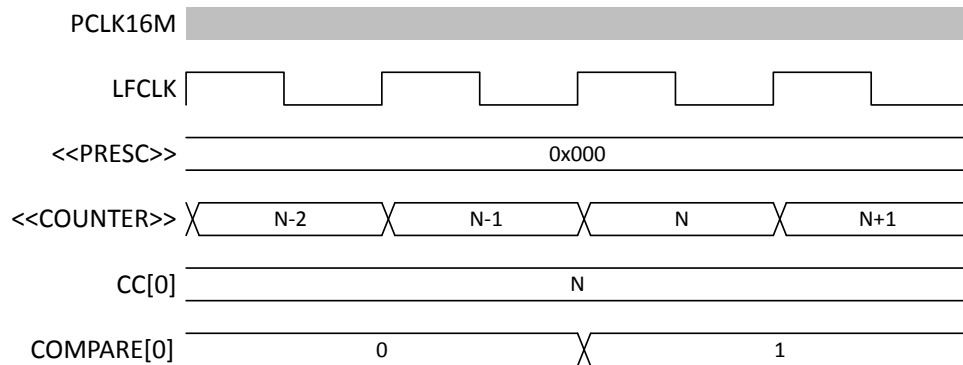


Figure 174: Timing diagram - COMPARE

- If the **COUNTER** value is N, writing N+2 to a **CC** register is guaranteed to trigger a **COMPARE** event at N+2.



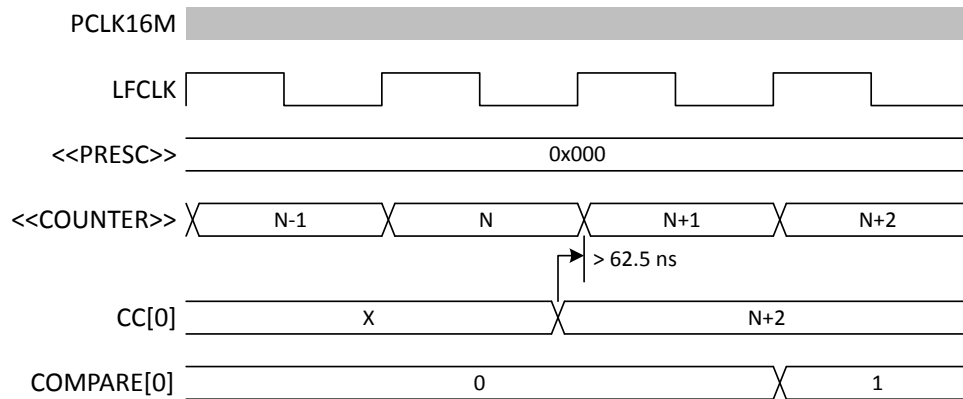


Figure 175: Timing diagram - COMPARE\_N+2

- If the **COUNTER** value is N, writing N or N+1 to a **CC** register may not trigger a **COMPARE** event.

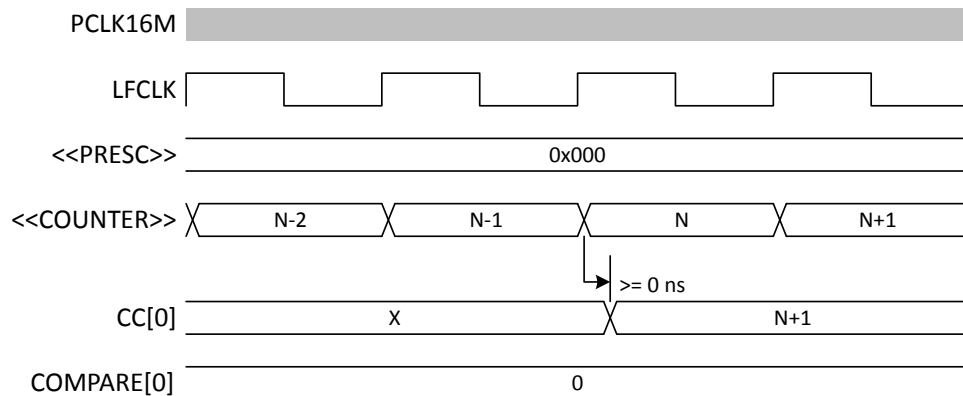


Figure 176: Timing diagram - COMPARE\_N+1

- If the **COUNTER** value is N, and the current **CC** value is N+1 or N+2 when a new **CC** value is written, a match may trigger on the previous **CC** value before the new value takes effect. If the current **CC** value is greater than N+2 when the new value is written, there will be no event due to the old value.

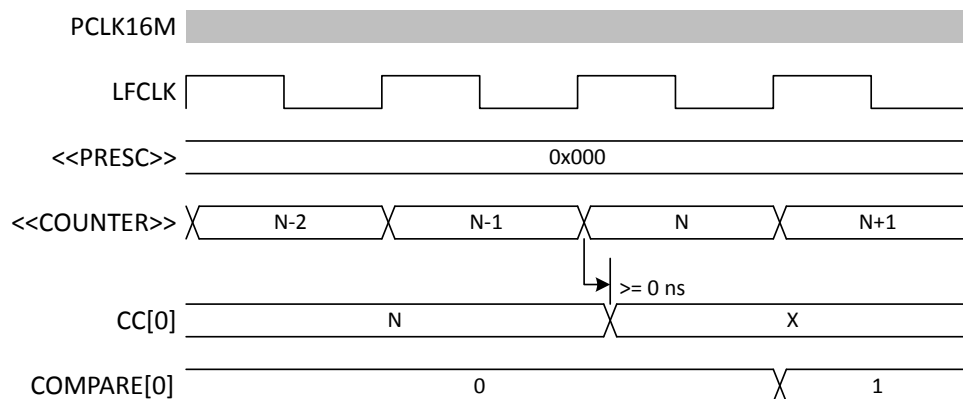


Figure 177: Timing diagram - COMPARE\_N-1

- If the **COMPARE[i]\_CLEAR** short is enabled, the **COUNTER** will be cleared one **LFCLK** after the **COMPARE** event.

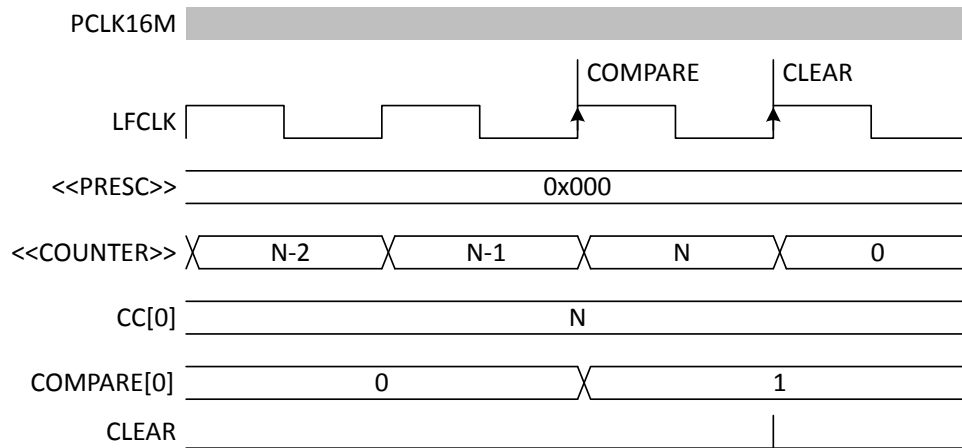


Figure 178: Timing diagram - COMPARE\_CLEAR

### 7.1.29.9 Task and event jitter/delay

Jitter or delay in the RTC, is due to the peripheral clock being a low frequency clock (LFCLK), which is not synchronous to the faster PCLK16M.

Registers in the peripheral interface that are part of the PCLK16M domain, have a set of mirrored registers in the LFCLK domain. For example, the **COUNTER** value accessible from the CPU is in the PCLK16M domain, and is latched on a read from an internal COUNTER register in the LFCLK domain. The **COUNTER** register is modified each time the RTC ticks. The registers are synchronised between the two clock domains (PCLK16M and LFCLK).

1. **CLEAR** and **STOP** (and **TRIGOVFLW**, which is not shown) will be delayed as long as it takes for the peripheral to clock a falling edge and a rising edge of the LFCLK. This is between 15.2585  $\mu$ s and 45.7755  $\mu$ s – rounded to 15  $\mu$ s and 46  $\mu$ s for the remainder of the section.

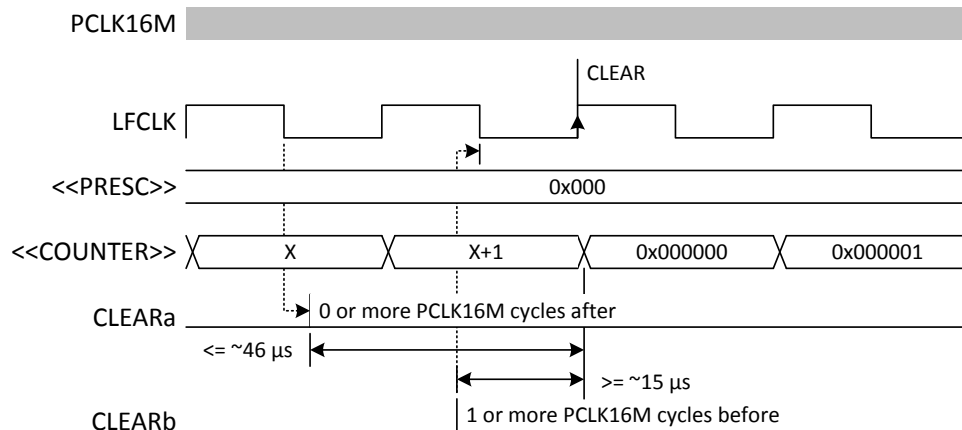


Figure 179: Timing diagram - DELAY\_CLEAR

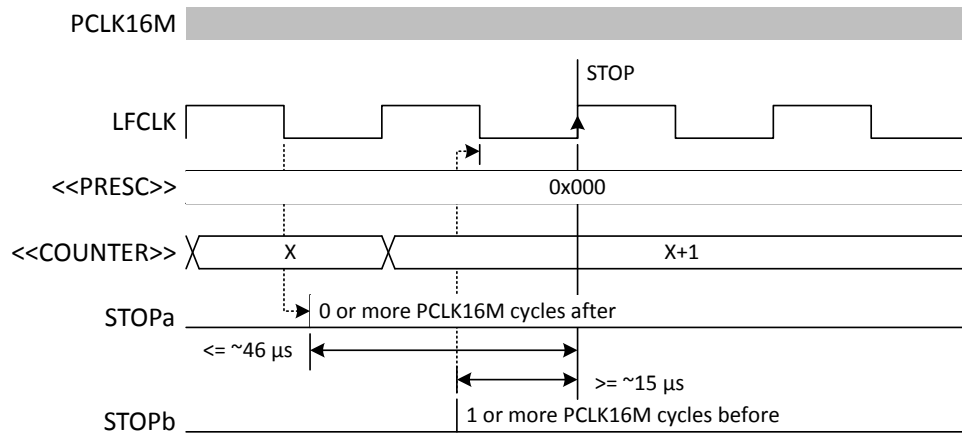


Figure 180: Timing diagram - DELAY\_STOP

**Note:** When a **STOP** task is triggered, the PCLK16M domain will immediately prevent the generation of any EVENTS from the RTC. However, as seen in the figure above, the **COUNTER** value can still increment one final time.

- The **START** task will start the RTC. Assuming that the LFCLK was previously running and stable, the first increment of **COUNTER** (and instance of TICK event) will be typically after  $30.5 \mu\text{s} \pm 15 \mu\text{s}$ . Additional delay will occur if the RTC is started before the LFCLK is running, see **CLOCK — Clock control** on page 61 for LFLK startup times. The software should therefore wait for the first TICK if it has to make sure that the RTC is running. Sending a TRIGOVFLW task sets the **COUNTER** to a value close to overflow. However, since the update of **COUNTER** relies on a stable LFCLK, sending this task while LFCLK is not running will also add additional delay as described above. The figures show the smallest and largest delays on the **START** task, appearing as a  $\pm 15 \mu\text{s}$  jitter on the first **COUNTER** increment.

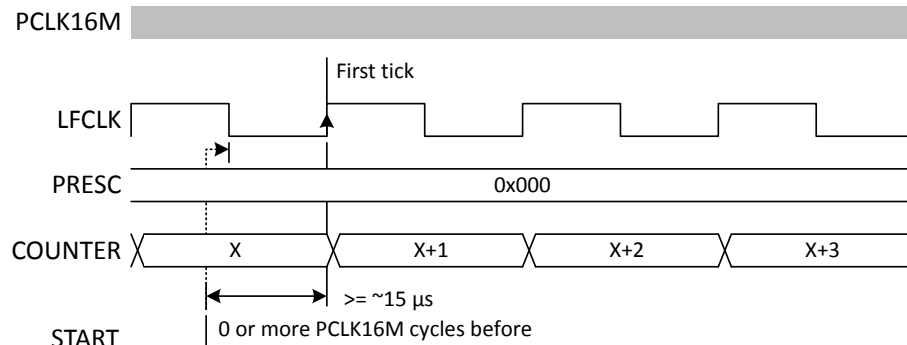


Figure 181: Timing diagram - JITTER\_START-

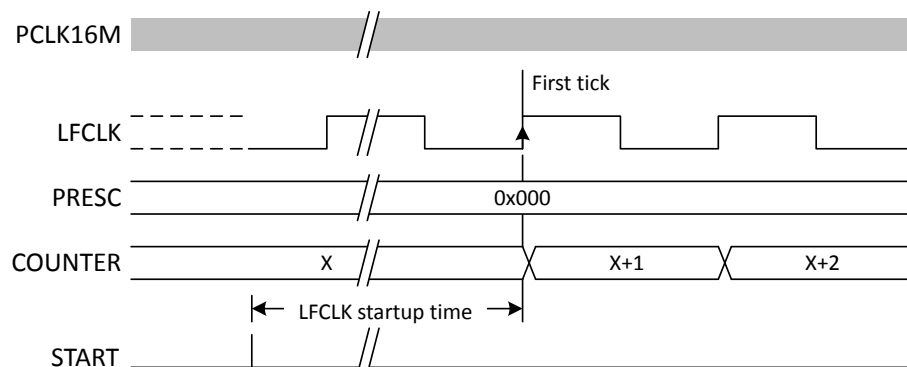


Figure 182: Timing diagram - JITTER\_START+

Tables below summarize the jitter introduced on tasks and events.

| Task                                     | Delay             |
|------------------------------------------|-------------------|
| CAPTURE, CLEAR, START, STOP, TRIGOVRFLOW | +15 to 46 $\mu$ s |

Table 135: RTC jitter magnitudes on tasks

| Operation/Function               | Jitter         |
|----------------------------------|----------------|
| START to COUNTER increment       | +/- 15 $\mu$ s |
| COMPARE to COMPARE <sup>20</sup> | +/- 62.5 ns    |

Table 136: RTC jitter magnitudes on events

## 7.1.29.10 Registers

| Base address | Domain      | Peripheral | Instance  | Secure mapping | DMA security | Description         | Configuration |
|--------------|-------------|------------|-----------|----------------|--------------|---------------------|---------------|
| 0x50014000   | APPLICATION | RTC        | RTC0 : S  | US             | NA           | Real time counter 0 |               |
| 0x40014000   |             |            | RTC0 : NS |                |              |                     |               |
| 0x50015000   | APPLICATION | RTC        | RTC1 : S  | US             | NA           | Real time counter 1 |               |
| 0x40015000   |             |            | RTC1 : NS |                |              |                     |               |
| 0x41011000   | NETWORK     | RTC        | RTC0      | NS             | NA           | Real-time counter 0 |               |
| 0x41016000   | NETWORK     | RTC        | RTC1      | NS             | NA           | Real-time counter 1 |               |

Table 137: Instances

| Register              | Offset | Security | Description                                                  |
|-----------------------|--------|----------|--------------------------------------------------------------|
| TASKS_START           | 0x000  |          | Start RTC counter                                            |
| TASKS_STOP            | 0x004  |          | Stop RTC counter                                             |
| TASKS_CLEAR           | 0x008  |          | Clear RTC counter                                            |
| TASKS_TRIGOVRFLOW     | 0x00C  |          | Set counter to 0xFFFFF0                                      |
| TASKS_CAPTURE[n]      | 0x040  |          | Capture RTC counter to CC[n] register                        |
| SUBSCRIBE_START       | 0x080  |          | Subscribe configuration for task <a href="#">START</a>       |
| SUBSCRIBE_STOP        | 0x084  |          | Subscribe configuration for task <a href="#">STOP</a>        |
| SUBSCRIBE_CLEAR       | 0x088  |          | Subscribe configuration for task <a href="#">CLEAR</a>       |
| SUBSCRIBE_TRIGOVRFLOW | 0x08C  |          | Subscribe configuration for task <a href="#">TRIGOVRFLOW</a> |
| SUBSCRIBE_CAPTURE[n]  | 0x0C0  |          | Subscribe configuration for task <a href="#">CAPTURE[n]</a>  |
| EVENTS_TICK           | 0x100  |          | Event on counter increment                                   |
| EVENTS_OVRFLOW        | 0x104  |          | Event on counter overflow                                    |
| EVENTS_COMPARE[n]     | 0x140  |          | Compare event on CC[n] match                                 |
| PUBLISH_TICK          | 0x180  |          | Publish configuration for event <a href="#">TICK</a>         |
| PUBLISH_OVRFLOW       | 0x184  |          | Publish configuration for event <a href="#">OVRFLOW</a>      |
| PUBLISH_COMPARE[n]    | 0x1C0  |          | Publish configuration for event <a href="#">COMPARE[n]</a>   |
| SHORTS                | 0x200  |          | Shortcuts between local events and tasks                     |
| INTENSET              | 0x304  |          | Enable interrupt                                             |
| INTENCLR              | 0x308  |          | Disable interrupt                                            |
| EVTEN                 | 0x340  |          | Enable or disable event routing                              |
| EVTENSET              | 0x344  |          | Enable event routing                                         |
| EVTENCLR              | 0x348  |          | Disable event routing                                        |
| COUNTER               | 0x504  |          | Current counter value                                        |

<sup>20</sup> Assumes RTC runs continuously between these events.

**Note:** 32.768 kHz clock jitter is additional to the numbers provided above.

| Register | Offset | Security | Description                                                                                       |
|----------|--------|----------|---------------------------------------------------------------------------------------------------|
| PRESALER | 0x508  |          | 12-bit prescaler for counter frequency (32768/(PRESALER+1)). Must be written when RTC is stopped. |
| CC[n]    | 0x540  |          | Compare register n                                                                                |

Table 138: Register overview

### 7.1.29.10.1 TASKS\_START

Address offset: 0x000

Start RTC counter

|                  |               |          |                                                                                       |                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|---------------|----------|---------------------------------------------------------------------------------------|-------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |               |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |               |          | A                                                                                     |                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |               |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field    | Value ID | Value                                                                                 | Description       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W TASKS_START |          |                                                                                       | Start RTC counter |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |               | Trigger  | 1                                                                                     | Trigger task      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.29.10.2 TASKS\_STOP

Address offset: 0x004

Stop RTC counter

|                  |              |          |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|--------------|----------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |              |          |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |              |          |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |              |          |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field   | Value ID | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W TASKS_STOP |          |       | Stop RTC counter                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Trigger  | 1     | Trigger task                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.29.10.3 TASKS\_CLEAR

Address offset: 0x008

Clear RTC counter

|                  |            |             |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|-------------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |             |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |             |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |             |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID    | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W          | TASKS_CLEAR |       | Clear RTC counter                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Trigger     | 1     | Trigger task                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.29.10.4 TASKS\_TRIGOVFLW

Address offset: 0x00C

Set counter to 0xFFFFF0

|                  |            |                 |          |   |       |                         |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-----------------|----------|---|-------|-------------------------|-------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                 |          |   |       |                         |             |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |                 |          |   |       |                         |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |   |
| Reset 0x00000000 |            |                 |          |   |       |                         |             |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |                 | Value ID |   | Value |                         | Description |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_TRIGOVFLW |          |   |       | Set counter to 0xFFFFF0 |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Trigger         |          | 1 |       | Trigger task            |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.29.10.5 TASKS\_CAPTURE[n] (n=0..3)

Address offset: 0x040 + (n × 0x4)

Capture RTC counter to CC[n] register

|                  |            |               |       |                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|---------------|-------|---------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |               |       | 31                                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |               |       |                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |
| Reset 0x00000000 |            |               |       | 0                                     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |
| ID               | Acce Field | Value ID      | Value | Description                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_CAPTURE |       | Capture RTC counter to CC[n] register |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Trigger       | 1     | Trigger task                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.29.10.6 SUBSCRIBE\_START

Address offset: 0x080

Subscribe configuration for task **START**

|                  |            |          |          |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |
|------------------|------------|----------|----------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------------------------|--|--|--|--|--|--|--|
| Bit number       |            |          |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |
| ID               |            |          |          | B                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value    | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0] | Channel that task <b>START</b> will subscribe to                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |
| B                | RW EN      |          |          |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |
|                  |            | Disabled | 0        | Disable subscription                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1        | Enable subscription                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |

### 7.1.29.10.7 SUBSCRIBE\_STOP

Address offset: 0x084

Subscribe configuration for task **STOP**

|                  |            |       |          |          |                      |                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-------|----------|----------|----------------------|-------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |       |          | 31       | 30                   | 29                                              | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |       |          | B        |                      |                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   |   |   |   |   |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |       |          | 0        |                      |                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |       | Value ID | Value    |                      | Description                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | CHIDX |          | [255..0] |                      | Channel that task <b>STOP</b> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW         | EN    |          |          |                      |                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |       | Disabled | 0        | Disable subscription |                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |       | Enabled  | 1        | Enable subscription  |                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.29.10.8 SUBSCRIBE\_CLEAR

Address offset: 0x088

Subscribe configuration for task **CLEAR**

|                  |            |          |          |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|--------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                                               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |          |          | B                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |          | 0                                                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |
| ID               | Acce Field | Value ID | Value    | Description                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] | Channel that task <b>CLEAR</b> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        | Disable subscription                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        | Enable subscription                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.29.10.9 SUBSCRIBE\_TRIGOVRLW

Address offset: 0x08C

Subscribe configuration for task **TRIGOVRLW**

|                  |            |  |          |  |          |  |                                                      |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|--|----------|--|------------------------------------------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          |  |          |  |                                                      |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |
| ID               |            |  |          |  |          |  |                                                      |  |  | B  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  |    |    |    |   |   |   |   |   |   | A | A | A | A | A | A | A |   |
| Reset 0x00000000 |            |  |          |  |          |  |                                                      |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID |  | Value    |  | Description                                          |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          |  | [255..0] |  | Channel that task <b>TRIGOVRLW</b> will subscribe to |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |  |          |  |                                                      |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled |  | 0        |  | Disable subscription                                 |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  |  | 1        |  | Enable subscription                                  |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.29.10.10 SUBSCRIBE\_CAPTURE[n] (n=0..3)

Address offset: 0x0C0 + (n × 0x4)

Subscribe configuration for task **CAPTURE[n]**

|                  |            |  |          |          |    |                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|----------|----|------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31       | 30 | 29                                             | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |  |          | B        |    |                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |          | 0        | 0  | 0                                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce Field |  | Value ID | Value    |    | Description                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          | [255..0] |    | Channel that task CAPTURE[n] will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |          |    |                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled | 0        |    | Disable subscription                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  | 1        |    | Enable subscription                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.29.10.11 EVENTS\_TICK

Address offset: 0x100

Event on counter increment

|                  |                |              |       |                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |
|------------------|----------------|--------------|-------|----------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|
| Bit number       |                |              |       | 31                         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |
| ID               |                |              |       |                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |  |
| Reset 0x00000000 |                |              |       | 0                          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |
| ID               | Acce Field     | Value ID     | Value | Description                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |
| A                | RW EVENTS_TICK |              |       | Event on counter increment |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |                | NotGenerated | 0     | Event not generated        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |                | Generated    | 1     | Event generated            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |

### 7.1.29.10.12 EVENTS\_OVRFLW

Address offset: 0x104

Event on counter overflow

|                  |            |               |                                                                                       |                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|---------------|---------------------------------------------------------------------------------------|---------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |               | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |               | A                                                                                     |                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |               | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                   |                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID      | Value                                                                                 | Description               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | EVENTS_OVRFLW |                                                                                       | Event on counter overflow |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | NotGenerated  | 0                                                                                     | Event not generated       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Generated     | 1                                                                                     | Event generated           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.29.10.13 EVENTS\_COMPARE[n] (n=0..3)

Address offset: 0x140 + (n × 0x4)

Compare event on CC[n] match

|                  |            |                |                                                                                       |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------------|---------------------------------------------------------------------------------------|------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |                | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |                | A                                                                                     |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |                | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                   |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID       | Value                                                                                 | Description                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | EVENTS_COMPARE |                                                                                       | Compare event on CC[n] match |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | NotGenerated   | 0                                                                                     | Event not generated          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Generated      | 1                                                                                     | Event generated              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.29.10.14 PUBLISH\_TICK

Address offset: 0x180

Publish configuration for event TICK

|                  |            |          |          |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|----------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |          |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |          |          | B                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value    | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0] | Channel that event <b>TICK</b> will publish to.                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |          |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0        | Disable publishing                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1        | Enable publishing                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

### 7.1.29.10.15 PUBLISH\_OVRFLW

Address offset: 0x184

Publish configuration for event OVRFLW



|                  |            |          |          |    |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|----|---------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          | 31       | 30 | 29                                                | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |          | B        |    |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          | 0        | 0  | 0                                                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce Field | Value ID | Value    |    | Description                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] |    | Channel that event <b>OVRFLW</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |    |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        |    | Disable publishing                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        |    | Enable publishing                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.29.10.16 PUBLISH\_COMPARE[n] (n=0..3)

Address offset: 0x1C0 + (n × 0x4)

Publish configuration for event **COMPARE[n]**

|                  |            |  |          |  |          |  |                                                |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|--|----------|--|------------------------------------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          |  |          |  |                                                |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |
| ID               |            |  |          |  |          |  |                                                |  |  | B  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  |    |    |    |   |   |   |   |   |   | A | A | A | A | A | A | A |   |
| Reset 0x00000000 |            |  |          |  |          |  |                                                |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID |  | Value    |  | Description                                    |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          |  | [255..0] |  | Channel that event COMPARE[n] will publish to. |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |  |          |  |                                                |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled |  | 0        |  | Disable publishing                             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  |  | 1        |  | Enable publishing                              |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.29.10.17 SHORTS

Address offset: 0x200

Shortcuts between local events and tasks

|                  |                                 |          |                                                                                       |                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|---------------------------------|----------|---------------------------------------------------------------------------------------|--------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |                                 |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |                                 |          | D C B A                                                                               |                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |                                 |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                   |                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field                      | Value ID | Value                                                                                 | Description                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A-D              | RW COMPARE[i]_CLEAR<br>(i=0..3) |          |                                                                                       | Shortcut between event COMPARE[i] and task CLEAR |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                                 | Disabled | 0                                                                                     | Disable shortcut                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                                 | Enabled  | 1                                                                                     | Enable shortcut                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

#### 7.1.29.10.18 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number       |            |          | 31    | 30 | 29                                                             | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |  |  |
|------------------|------------|----------|-------|----|----------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|--|--|
| ID               |            |          |       |    |                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    | F  | E  | D  | C  |    |    |   |   |   |   |   |   |   |   |   |   | B | A |  |  |
| Reset 0x00000000 |            |          | 0     | 0  | 0                                                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |  |  |
| ID               | Acce Field | Value ID | Value |    | Description                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |
| A                | RW TICK    |          |       |    | Write '1' to enable interrupt for event <a href="#">TICK</a>   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            | Set      | 1     |    | Enable                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            | Disabled | 0     |    | Read: Disabled                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            | Enabled  | 1     |    | Read: Enabled                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |
| B                | RW OVRFLW  |          |       |    | Write '1' to enable interrupt for event <a href="#">OVRFLW</a> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            | Set      | 1     |    | Enable                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |

| Bit number       |            |                     | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |             |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|---------------------|---------------------------------------------------------------------------------------|-------------|----------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |            |                     | F E D C B A                                                                           |             |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |                     | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |             |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID            | Value                                                                                 | Description |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C-F              | RW         | COMPARE[i] (i=0..3) | Disabled                                                                              | 0           | Read: Disabled |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |                     | Enabled                                                                               | 1           | Read: Enabled  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |                     | Set                                                                                   | 1           | Enable         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |                     | Disabled                                                                              | 0           | Read: Disabled |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |                     | Enabled                                                                               | 1           | Read: Enabled  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.29.10.19 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number       |            |                     | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |
|------------------|------------|---------------------|---------------------------------------------------------------------------------------|---------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----|--|
| ID               |            |                     | F E D C                                                                               |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | B A |  |
| Reset 0x00000000 |            |                     | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |
| ID               | Acce Field | Value ID            | Value                                                                                 | Description                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |
| A                | RW         | TICK                |                                                                                       | Write '1' to disable interrupt for event <a href="#">TICK</a>       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |
|                  |            | Clear               | 1                                                                                     | Disable                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |
|                  |            | Disabled            | 0                                                                                     | Read: Disabled                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |
|                  |            | Enabled             | 1                                                                                     | Read: Enabled                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |
| B                | RW         | OVRFLW              |                                                                                       | Write '1' to disable interrupt for event <a href="#">OVRFLW</a>     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |
|                  |            | Clear               | 1                                                                                     | Disable                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |
|                  |            | Disabled            | 0                                                                                     | Read: Disabled                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |
|                  |            | Enabled             | 1                                                                                     | Read: Enabled                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |
| C-F              | RW         | COMPARE[i] (i=0..3) |                                                                                       | Write '1' to disable interrupt for event <a href="#">COMPARE[i]</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |
|                  |            | Clear               | 1                                                                                     | Disable                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |
|                  |            | Disabled            | 0                                                                                     | Read: Disabled                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |
|                  |            | Enabled             | 1                                                                                     | Read: Enabled                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |

### 7.1.29.10.20 EVTEN

Address offset: 0x340

Enable or disable event routing

| Bit number       |            |                     | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |
|------------------|------------|---------------------|---------------------------------------------------------------------------------------|-------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|---|
| ID               |            |                     | F E D C                                                                               |                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | B | A |
| Reset 0x00000000 |            |                     | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |
| ID               | Acce Field | Value ID            | Value                                                                                 | Description                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |
| A                | RW         | TICK                |                                                                                       | Enable or disable event routing for event <span>TICK</span>       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |
|                  |            | Disabled            | 0                                                                                     | Disable                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |
|                  |            | Enabled             | 1                                                                                     | Enable                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |
| B                | RW         | OVRFLW              |                                                                                       | Enable or disable event routing for event <span>OVRFLW</span>     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |
|                  |            | Disabled            | 0                                                                                     | Disable                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |
|                  |            | Enabled             | 1                                                                                     | Enable                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |
| C-F              | RW         | COMPARE[i] (i=0..3) |                                                                                       | Enable or disable event routing for event <span>COMPARE[i]</span> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |
|                  |            | Disabled            | 0                                                                                     | Disable                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |
|                  |            | Enabled             | 1                                                                                     | Enable                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |



|                  |            |         |          |                                                                                       |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|---------|----------|---------------------------------------------------------------------------------------|--|--|--|---------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |         |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |         |          | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A                           |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |         |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                   |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field |         | Value ID | Value                                                                                 |  |  |  | Description   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | R          | COUNTER |          |                                                                                       |  |  |  | Counter value |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

#### 7.1.29.10.24 PRESCALER

Address offset: 0x508

12-bit prescaler for counter frequency  $(32768 / (\text{PRESCALER} + 1))$ . Must be written when RTC is stopped.

|                  |              |  |          |                                                                                       |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|--------------|--|----------|---------------------------------------------------------------------------------------|--|--|--|-----------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |              |  |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |              |  |          | A A A A A A A A A A A A A A A A A A A A A A A A A A                                   |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |              |  |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                   |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field   |  | Value ID | Value                                                                                 |  |  |  | Description     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW PRESCALER |  |          |                                                                                       |  |  |  | Prescaler value |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

#### 7.1.29.10.25 CC[n] (n=0..3)

Address offset:  $0x540 + (n \times 0x4)$

Compare register n

|                  |            |  |          |       |    |    |    |               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|-------|----|----|----|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31    | 30 | 29 | 28 | 27            | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |  |          |       |    |    |    |               |    |    |    |    |    |    |    | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A | A |   |
| Reset 0x00000000 |            |  |          | 0     | 0  | 0  | 0  | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID | Value |    |    |    | Description   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW COMPARE |  |          |       |    |    |    | Compare value |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.29.11 Electrical specification

## 7.1.30 SAADC — Successive approximation analog-to-digital converter

The SAADC is a differential successive approximation register (SAR) analog-to-digital converter.

Listed here are the main features of SAADC:

- 8/10/12-bit resolution, 14-bit resolution with oversampling
- Multiple analog inputs:
  - AIN0 to AIN7 pins
  - VDD pin
  - VDDHDIV5 (through VDDH pin)
- Up to eight input channels:
  - One channel per single-ended input and two channels per differential input
  - Scan mode can be configured with both single-ended channels and differential channels
  - Each channel can be configured to select any of the above analog inputs
- Full scale input range (0 to VDD)
- Sampling triggered via a task from software or a PPI channel for full flexibility on sample frequency source from low-power 32.768 kHz RTC or more accurate 1/16 MHz timers

- One-shot conversion mode to sample a single channel
- Scan mode to sample a series of channels in sequence with configurable sample delay
- Support for direct sample transfer to RAM using EasyDMA
- Interrupts on single sample and full buffer events
- Samples stored as 16-bit two's complement values for differential and single-ended sampling
- Continuous sampling without the need of an external timer
- Internal resistor string
- On-the-fly limit checking

### 7.1.30.1 Shared resources

The ADC can coexist with COMP and other peripherals using one of AIN0–AIN7, provided these are assigned to different pins.

It is not recommended to select the same analog input pin for both modules.

### 7.1.30.2 Overview

The ADC supports up to eight external analog input channels. It can be operated in One-shot mode with sampling under software control, or Continuous mode with a programmable sampling rate.

The analog inputs can be configured as eight single-ended inputs, four differential inputs or a combination of these. Each channel can be configured to select:

- AIN0 to AIN7 pins
- VDD pin
- VDDH DIV5 (through VDDH pin)

Channels can be sampled individually in one-shot or continuous sampling modes, or, using scan mode, multiple channels can be sampled in sequence. Channels can also be oversampled to improve noise performance.

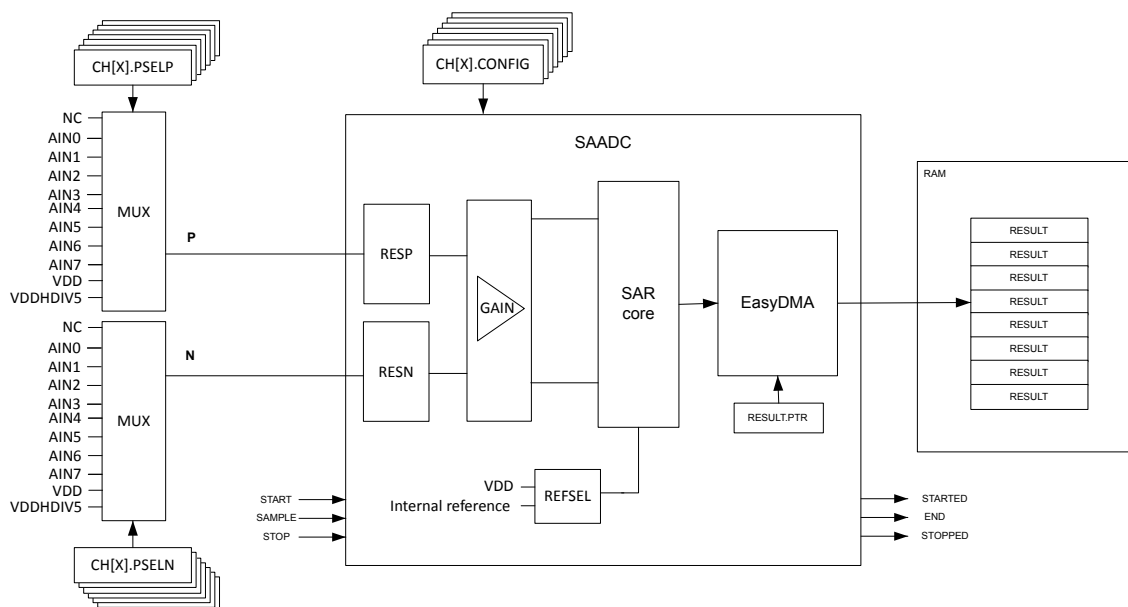


Figure 183: Simplified ADC block diagram

Internally, the ADC is always a differential analog-to-digital converter, but by default it is configured with single-ended input in the MODE field of the CH[n].CONFIG register. In single-ended mode, the negative input will be shorted to ground internally.

The assumption in single-ended mode is that the internal ground of the ADC is the same as the external ground that the measured voltage is referred to. The ADC is thus sensitive to ground bounce on the PCB in single-ended mode. If this is a concern we recommend using differential measurement.

### 7.1.30.3 Digital output

The output result of the ADC depends on the settings in the CH[n].CONFIG and RESOLUTION registers as follows:

$$\text{RESULT} = [V(P) - V(N)] * \text{GAIN/REFERENCE} * 2^{(\text{RESOLUTION} - m)}$$

where

**V(P)**

is the voltage at input P

**V(N)**

is the voltage at input N

**GAIN**

is the selected gain setting

**m**

is the mode setting. Use m=0 if CONFIG.MODE=SE, or m=1 if CONFIG.MODE=Diff

**REFERENCE**

is the selected reference voltage

The result generated by the ADC will deviate from the expected due DC errors like offset, gain, differential non-linearity (DNL), and integral non-linearity (INL). See [Electrical specification](#) for details on these parameters. The result can also vary due to AC errors like non-linearities in the GAIN block, settling errors due to high source impedance and sampling jitter. For battery measurement, the DC errors are most noticeable.

The ADC has a wide selection of gains controlled in the GAIN field of the CH[n].CONFIG register. If CH[n].CONFIG.REFSEL=0, the input range of the ADC core is nominally  $\pm 0.6$  V differential and the input must be scaled accordingly.

The ADC has a temperature dependent offset. If the ADC is to operate over a large temperature range, we recommend running CALIBRATEOFFSET at regular intervals. The CALIBRATEDONE event will be fired when the calibration has been completed. Note that the DONE and RESULTDONE events will also be generated.

### 7.1.30.4 Analog inputs and channels

Up to eight analog input channels, CH[n](n=0..7), can be configured.

See [Shared resources](#) on page 505 for shared input with comparators.

Any one of the available channels can be enabled for the ADC to operate in one-shot mode. If more than one CH[n] is configured, the ADC enters scan mode.

An analog input is selected as a positive converter input if CH[n].PSELP is set, setting CH[n].PSELP also enables the particular channel.

An analog input is selected as a negative converter input if CH[n].PSELN is set. The CH[n].PSELN register will have no effect unless differential mode is enabled, see MODE field in CH[n].CONFIG register.

If more than one of the CH[n].PSELP registers is set, the device enters scan mode. Input selections in scan mode are controlled by the CH[n].PSELP and CH[n].PSELN registers, where CH[n].PSELN is only used if the particular scan channel is specified as differential, see MODE field in CH[n].CONFIG register.

**Important:** Channels selected for COMP cannot be used at the same time for ADC sampling, though channels not selected for use by these blocks can be used by the ADC.

### 7.1.30.5 Operation modes

The ADC input configuration supports one-shot mode, continuous mode and scan mode.

**Note:** Scan mode and oversampling cannot be combined.

The ADC indicates a single ongoing conversion via the register [STATUS](#) on page 525. During scan mode, oversampling, or continuous modes, more than a single conversion take place in the ADC. As consequence, the value reflected in STATUS register will toggle at the end of each single conversion.

#### 7.1.30.5.1 One-shot mode

One-shot operation is configured by enabling only one of the available channels defined by CH[n].PSEL, CH[n].PSELN, and CH[n].CONFIG registers.

Upon a SAMPLE task, the ADC starts to sample the input voltage. The CH[n].CONFIG.TACQ controls the acquisition time.

A DONE event signals that one sample has been taken.

In this mode, the RESULTDONE event has the same meaning as DONE when no oversampling takes place. Note that both events may occur before the actual value has been transferred into RAM by EasyDMA. For more information, see [EasyDMA](#) on page 509.

#### 7.1.30.5.2 Continuous mode

Continuous sampling can be achieved by using the internal timer in the ADC, or triggering the SAMPLE task from one of the general purpose timers through the PPI system.

Care shall be taken to ensure that the sample rate fulfils the following criteria, depending on how many channels are active:

$$f_{\text{SAMPLE}} < 1 / (t_{\text{ACQ}} + t_{\text{conv}})$$

The SAMPLERATE register can be used as a local timer instead of triggering individual SAMPLE tasks. When SAMPLERATE.MODE is set to Timers, it is sufficient to trigger SAMPLE task only once in order to start the SAADC and triggering the STOP task will stop sampling. The SAMPLERATE.CC field controls the sample rate.

The SAMPLERATE timer mode cannot be combined with SCAN mode, and only one channel can be enabled in this mode.

A DONE event signals that one sample has been taken.

In this mode, the RESULTDONE event has the same meaning as DONE when no oversampling takes place. Note that both events may occur before the actual value has been transferred into RAM by EasyDMA.

#### 7.1.30.5.3 Oversampling

An accumulator in the ADC can be used to average noise on the analog input. In general, oversampling improves the signal-to-noise ratio (SNR). Oversampling, however, does not improve the integral non-linearity (INL), or differential non-linearity (DNL).

Oversampling and scan should not be combined, since oversampling and scan will average over input channels.

The accumulator is controlled in the OVERSAMPLE register. The SAMPLE task must be set  $2^{\text{OVERSAMPLE}}$  number of times before the result is written to RAM. This can be achieved by:

- Configuring a fixed sampling rate using the local timer or a general purpose timer and the PPI system to trigger a SAMPLE task
- Triggering SAMPLE  $2^{\text{OVERSAMPLE}}$  times from software
- Enabling BURST mode

CH[n].CONFIG.BURST can be enabled to avoid setting SAMPLE task  $2^{\text{OVERSAMPLE}}$  times. With BURST = 1 the ADC will sample the input  $2^{\text{OVERSAMPLE}}$  times as fast as it can (actual timing:  $<(t_{\text{ACQ}}+t_{\text{CONV}}) \times 2^{\text{OVERSAMPLE}}$ ). Thus, for the user it will just appear like the conversion took a bit longer time, but other than that, it is similar to one-shot mode.

A DONE event signals that one sample has been taken.

In this mode, the RESULTDONE event signals that enough conversions have taken place for an oversampled result to get transferred into RAM. Note that both events may occur before the actual value has been transferred into RAM by EasyDMA.

#### 7.1.30.5.4 Scan mode

A channel is considered enabled if CH[n].PSEL is set. If more than one channel, CH[n], is enabled, the ADC enters scan mode.

In scan mode, one SAMPLE task will trigger one conversion per enabled channel. The time it takes to sample all channels is:

$$\text{Total time} < \text{Sum}(\text{CH}[x].t_{\text{ACQ}}+t_{\text{CONV}}), x=0..\text{enabled channels}$$

A DONE event signals that one sample has been taken.

In this mode, the RESULTDONE event signals has the same meaning as DONE when no oversampling takes place. Note that both events may occur before the actual values have been transferred into RAM by EasyDMA.

The figure below provides an example of results placement in Data RAM, with an even RESULT.MAXCNT. In this example, channels 1, 2 and 5 are enabled, all others are disabled.

|                                       | 31                           | 16 | 15                           | 0 |
|---------------------------------------|------------------------------|----|------------------------------|---|
| RESULT.PTR                            | CH[2] 1 <sup>st</sup> result |    | CH[1] 1 <sup>st</sup> result |   |
| RESULT.PTR + 4                        | CH[1] 2 <sup>nd</sup> result |    | CH[5] 1 <sup>st</sup> result |   |
| RESULT.PTR + 8                        | CH[5] 2 <sup>nd</sup> result |    | CH[2] 2 <sup>nd</sup> result |   |
|                                       | ( ... )                      |    |                              |   |
| RESULT.PTR +<br>2*(RESULT.MAXCNT - 2) | CH[5] last result            |    | CH[2] last result            |   |

Figure 184: Example of RAM placement (even RESULT.MAXCNT), channels 1, 2 and 5 enabled

The figure below provides an example of results placement in Data RAM, with an odd RESULT.MAXCNT. In this example, channels 1, 2 and 5 are enabled, all others are disabled. The last 32-bit word is populated only with one 16-bit result.

|                                       | 31                           | 16 | 15                           | 0 |
|---------------------------------------|------------------------------|----|------------------------------|---|
| RESULT.PTR                            | CH[2] 1 <sup>st</sup> result |    | CH[1] 1 <sup>st</sup> result |   |
| RESULT.PTR + 4                        | CH[1] 2 <sup>nd</sup> result |    | CH[5] 1 <sup>st</sup> result |   |
| RESULT.PTR + 8                        | CH[5] 2 <sup>nd</sup> result |    | CH[2] 2 <sup>nd</sup> result |   |
|                                       | ( ... )                      |    |                              |   |
| RESULT.PTR +<br>2*(RESULT.MAXCNT - 1) |                              |    | CH[5] last result            |   |

Figure 185: Example of RAM placement (odd RESULT.MAXCNT), channels 1, 2 and 5 enabled



### 7.1.30.6 EasyDMA

After configuring RESULT.PTR and RESULT.MAXCNT, the ADC resources are started by triggering the START task. The ADC is using EasyDMA to store results in a Result buffer in RAM.

The Result buffer is located at the address specified in the RESULT.PTR register. The RESULT.PTR register is double-buffered and it can be updated and prepared for the next START task immediately after the STARTED event is generated. The size of the Result buffer is specified in the RESULT.MAXCNT register and the ADC will generate an END event when it has filled up the Result buffer, see [Figure 186: ADC](#) on page 509. Results are stored in little-endian byte order in Data RAM. Every sample will be sign extended to 16 bit before stored in the Result buffer.

The ADC is stopped by triggering the STOP task. The STOP task will terminate an ongoing sampling. The ADC will generate a STOPPED event when it has stopped. If the ADC is already stopped when the STOP task is triggered, the STOPPED event will still be generated.

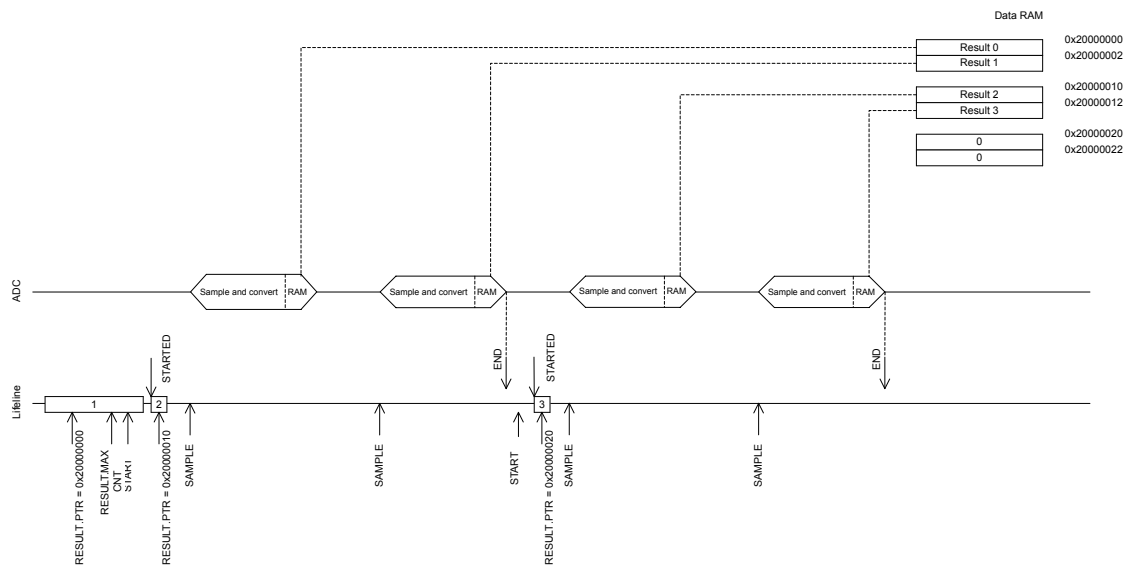


Figure 186: ADC

If the RESULT.PTR is not pointing to a RAM region accessible from the peripheral, an EasyDMA transfer may result in a HardFault and/or memory corruption. See [Memory](#) on page 18 for more information about the different memory regions.

The EasyDMA will have finished accessing the RAM when the END or STOPPED event has been generated.

The RESULT.AMOUNT register can be read following an END event or a STOPPED event to see how many results have been transferred to the Result buffer in RAM since the START task was triggered.

In scan mode, SAMPLE tasks can be triggered once the START task is triggered. The END event is generated when the number of samples transferred to memory reaches the value specified by RESULT.MAXCNT. After an END event, the START task needs to be triggered again before new samples can be taken. Also make sure that the size of the Result buffer is large enough to have space for minimum one result from each of the enabled channels, by specifying RESULT.MAXCNT  $\geq$  number of channels enabled. For more information about the scan mode, see [Scan mode](#) on page 508.

### 7.1.30.7 Resistor ladder

The ADC has an internal resistor string for positive and negative input.

See [Figure 187: Resistor ladder for positive input \(negative input is equivalent, using RESN instead of RESP\)](#) on page 510. The resistors are controlled in the CH[n].CONFIG.RESP and CH[n].CONFIG.RESN registers.

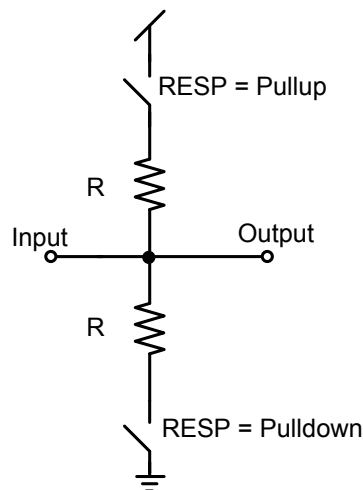


Figure 187: Resistor ladder for positive input (negative input is equivalent, using RESN instead of RESP)

### 7.1.30.8 Reference

The ADC can use two different references, controlled in the REFSEL field of the CH[n].CONFIG register.

These are:

- Internal reference
- VDD as reference

The internal reference results in an input range of  $\pm 0.6$  V on the ADC core. VDD as reference results in an input range of  $\pm VDD/4$  on the ADC core. The gain block can be used to change the effective input range of the ADC.

$$\text{Input range} = (+/- 0.6 \text{ V or } \pm VDD/4) / \text{Gain}$$

For example, choosing VDD as reference, single ended input (grounded negative input), and a gain of 1/4 the input range will be:

$$\text{Input range} = (VDD/4) / (1/4) = VDD$$

With internal reference, single ended input (grounded negative input), and a gain of 1/6 the input range will be:

$$\text{Input range} = (0.6 \text{ V}) / (1/6) = 3.6 \text{ V}$$

The AIN0-AIN7 inputs cannot exceed VDD, or be lower than VSS.

### 7.1.30.9 Acquisition time

To sample the input voltage, the ADC connects a capacitor to the input.

For illustration, see [Figure 188: Simplified ADC sample network](#) on page 511. The acquisition time indicates how long the capacitor is connected, see TACQ field in CH[n].CONFIG register. The required acquisition time depends on the source ( $R_{\text{source}}$ ) resistance. For high source resistance the acquisition time should be increased, see [Table 139: Acquisition time](#) on page 511.

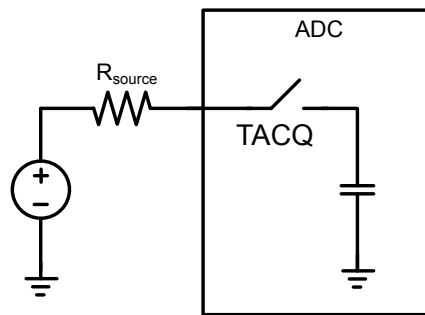


Figure 188: Simplified ADC sample network

| TACQ [ $\mu$ s] | Maximum source resistance [kOhm] |
|-----------------|----------------------------------|
| 3               | 10                               |
| 5               | 40                               |
| 10              | 100                              |
| 15              | 200                              |
| 20              | 400                              |
| 40              | 800                              |

Table 139: Acquisition time

When using `VDDHDI5` as input, the acquisition time needs to be 10  $\mu$ s or higher.

#### 7.1.30.10 Limits event monitoring

A channel can be event monitored by configuring limit register `CH[n].LIMIT`.

If the conversion result is higher than the defined high limit, or lower than the defined low limit, the appropriate event will get fired.

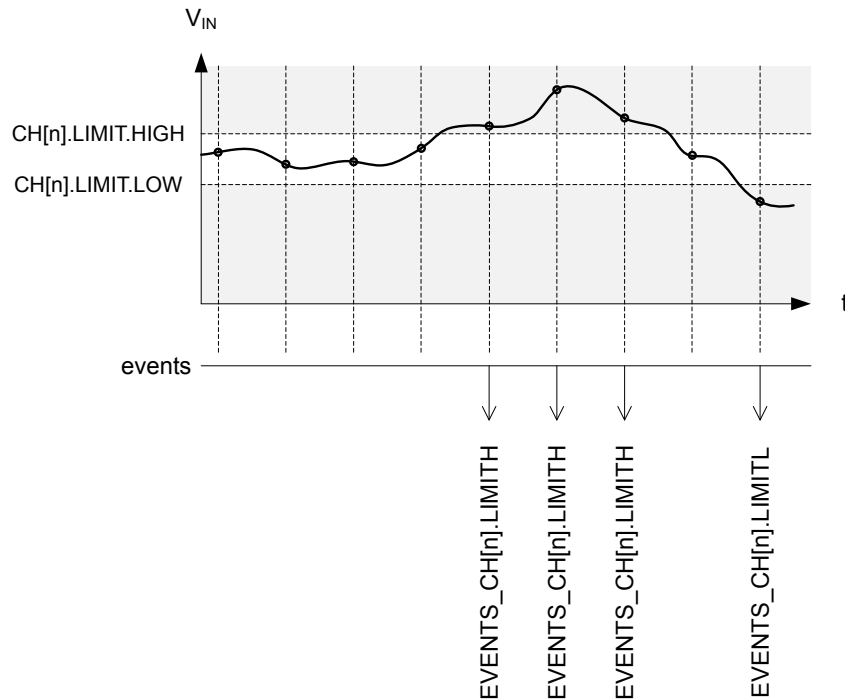


Figure 189: Example of limits monitoring on channel 'n'

Note that when setting the limits, CH[n].LIMIT.HIGH shall always be higher than or equal to CH[n].LIMIT.LOW. In other words, an event can be fired only when the input signal has been sampled outside of the defined limits. It is not possible to fire an event when the input signal is inside a defined range by swapping high and low limits.

The comparison to limits always takes place, there is no need to enable it. If comparison is not required on a channel, the software shall simply ignore the related events. In that situation, the value of the limits registers is irrelevant, so it does not matter if CH[n].LIMIT.LOW is lower than CH[n].LIMIT.HIGH or not.

### 7.1.30.11 Registers

| Base address | Domain      | Peripheral | Instance   | Secure mapping | DMA security | Description                 | Configuration |
|--------------|-------------|------------|------------|----------------|--------------|-----------------------------|---------------|
| 0x5000E000   | APPLICATION | SAADC      | SAADC : S  | US             | SA           | Successive approximation    |               |
| 0x4000E000   |             |            | SAADC : NS |                |              | analog-to-digital converter |               |

Table 140: Instances

| Register               | Offset | Security | Description                                                                                                                              |
|------------------------|--------|----------|------------------------------------------------------------------------------------------------------------------------------------------|
| TASKS_START            | 0x000  |          | Start the ADC and prepare the result buffer in RAM                                                                                       |
| TASKS_SAMPLE           | 0x004  |          | Take one ADC sample, if scan is enabled all channels are sampled                                                                         |
| TASKS_STOP             | 0x008  |          | Stop the ADC and terminate any on-going conversion                                                                                       |
| TASKS_CALIBRATEOFFSET  | 0x00C  |          | Starts offset auto-calibration                                                                                                           |
| SUBSCRIBE_START        | 0x080  |          | Subscribe configuration for task <a href="#">START</a>                                                                                   |
| SUBSCRIBE_SAMPLE       | 0x084  |          | Subscribe configuration for task <a href="#">SAMPLE</a>                                                                                  |
| SUBSCRIBE_STOP         | 0x088  |          | Subscribe configuration for task <a href="#">STOP</a>                                                                                    |
| SUBSCRIBE_CALIBRATEOFF | 0x08C  |          | Subscribe configuration for task <a href="#">CALIBRATEOFFSET</a>                                                                         |
| EVENTS_STARTED         | 0x100  |          | The ADC has started                                                                                                                      |
| EVENTS_END             | 0x104  |          | The ADC has filled up the Result buffer                                                                                                  |
| EVENTS_DONE            | 0x108  |          | A conversion task has been completed. Depending on the mode, multiple conversions might be needed for a result to be transferred to RAM. |

| Register              | Offset | Security | Description                                                                                                                                                                          |
|-----------------------|--------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| EVENTS_RESULTDONE     | 0x10C  |          | A result is ready to get transferred to RAM.                                                                                                                                         |
| EVENTS_CALIBRATEDONE  | 0x110  |          | Calibration is complete                                                                                                                                                              |
| EVENTS_STOPPED        | 0x114  |          | The ADC has stopped                                                                                                                                                                  |
| EVENTS_CH[n].LIMITH   | 0x118  |          | Last results is equal or above CH[n].LIMIT.HIGH                                                                                                                                      |
| EVENTS_CH[n].LIMITL   | 0x11C  |          | Last results is equal or below CH[n].LIMIT.LOW                                                                                                                                       |
| PUBLISH_STARTED       | 0x180  |          | Publish configuration for event <a href="#">STARTED</a>                                                                                                                              |
| PUBLISH_END           | 0x184  |          | Publish configuration for event <a href="#">END</a>                                                                                                                                  |
| PUBLISH_DONE          | 0x188  |          | Publish configuration for event <a href="#">DONE</a>                                                                                                                                 |
| PUBLISH_RESULTDONE    | 0x18C  |          | Publish configuration for event <a href="#">RESULTDONE</a>                                                                                                                           |
| PUBLISH_CALIBRATEDONE | 0x190  |          | Publish configuration for event <a href="#">CALIBRATEDONE</a>                                                                                                                        |
| PUBLISH_STOPPED       | 0x194  |          | Publish configuration for event <a href="#">STOPPED</a>                                                                                                                              |
| PUBLISH_CH[n].LIMITH  | 0x198  |          | Publish configuration for event <a href="#">CH[n].LIMITH</a>                                                                                                                         |
| PUBLISH_CH[n].LIMITL  | 0x19C  |          | Publish configuration for event <a href="#">CH[n].LIMITL</a>                                                                                                                         |
| INTEN                 | 0x300  |          | Enable or disable interrupt                                                                                                                                                          |
| INTENSET              | 0x304  |          | Enable interrupt                                                                                                                                                                     |
| INTENCLR              | 0x308  |          | Disable interrupt                                                                                                                                                                    |
| STATUS                | 0x400  |          | Status                                                                                                                                                                               |
| ENABLE                | 0x500  |          | Enable or disable ADC                                                                                                                                                                |
| CH[n].PSEL            | 0x510  |          | Input positive pin selection for CH[n]                                                                                                                                               |
| CH[n].PSELN           | 0x514  |          | Input negative pin selection for CH[n]                                                                                                                                               |
| CH[n].CONFIG          | 0x518  |          | Input configuration for CH[n]                                                                                                                                                        |
| CH[n].LIMIT           | 0x51C  |          | High/low limits for event monitoring a channel                                                                                                                                       |
| RESOLUTION            | 0x5F0  |          | Resolution configuration                                                                                                                                                             |
| OVERSAMPLE            | 0x5F4  |          | Oversampling configuration. OVERSAMPLE should not be combined with SCAN.<br>The RESOLUTION is applied before averaging, thus for high OVERSAMPLE a higher RESOLUTION should be used. |
| SAMPLERATE            | 0x5F8  |          | Controls normal or continuous sample rate                                                                                                                                            |
| RESULT.PTR            | 0x62C  |          | Data pointer                                                                                                                                                                         |
| RESULT.MAXCNT         | 0x630  |          | Maximum number of buffer words to transfer                                                                                                                                           |
| RESULT.AMOUNT         | 0x634  |          | Number of buffer words transferred since last START                                                                                                                                  |

Table 141: Register overview

### 7.1.30.11.1 TASKS\_START

Address offset: 0x000

Start the ADC and prepare the result buffer in RAM

|                  |            |             |                                                                                       |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|-------------|---------------------------------------------------------------------------------------|----------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |             | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |             | A                                                                                     |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |             | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID    | Value                                                                                 | Description                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W          | TASKS_START |                                                                                       | Start the ADC and prepare the result buffer in RAM |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Trigger     | 1                                                                                     | Trigger task                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.30.11.2 TASKS\_SAMPLE

Address offset: 0x004

Take one ADC sample, if scan is enabled all channels are sampled

|                  |      |              |         |    |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|--------------|---------|----|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|--|------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |              |         | 31 | 30    | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |  |                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |              |         | A  |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |              |         | 0  | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field        | Value   | ID | Value |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  | Description                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W    | TASKS_SAMPLE |         |    |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  | Take one ADC sample, if scan is enabled all channels are sampled |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |              | Trigger | 1  |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  | Trigger task                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.30.11.3 TASKS\_STOP

Address offset: 0x008

Stop the ADC and terminate any on-going conversion

|                  |            |            |          |   |       |                                                    |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|------------|----------|---|-------|----------------------------------------------------|-------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |            |          |   |       |                                                    |             |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |            |          |   |       |                                                    |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |   |
| Reset 0x00000000 |            |            |          |   |       |                                                    |             |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |            | Value ID |   | Value |                                                    | Description |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_STOP |          |   |       | Stop the ADC and terminate any on-going conversion |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Trigger    |          | 1 |       | Trigger task                                       |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.30.11.4 TASKS\_CALIBRATEOFFSET

Address offset: 0x00C

Starts offset auto-calibration

|                  |            |                       |       |                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-----------------------|-------|--------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                       |       | 31                             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |                       |       |                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |
| Reset 0x00000000 |            |                       |       | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |
| ID               | Acce Field | Value ID              | Value | Description                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_CALIBRATEOFFSET |       | Starts offset auto-calibration |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Trigger               | 1     | Trigger task                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.30.11.5 SUBSCRIBE\_START

Address offset: 0x080

Subscribe configuration for task [START](#)

|                  |            |          |          |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|----------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          |          | B A A A A A A A                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value    | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0] | Channel that task <span>START</span> will subscribe to                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW EN      |          |          |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0        | Disable subscription                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1        | Enable subscription                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.30.11.6 SUBSCRIBE\_SAMPLE

Address offset: 0x084

Subscribe configuration for task [SAMPLE](#)

|                  |            |          |          |                                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|----------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                                                                         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |          |          | B                                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |          | 0                                                                          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |
| ID               | Acce Field | Value ID | Value    | Description                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] | Channel that task <span style="color:blue">SAMPLE</span> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |                                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        | Disable subscription                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        | Enable subscription                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.30.11.7 SUBSCRIBE\_STOP

Address offset: 0x088

Subscribe configuration for task **STOP**

|                  |            |          |          |                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|-------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                                                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |          |          | B                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |          | 0                                                     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce Field | Value ID | Value    | Description                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] | Channel that task <span>STOP</span> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        | Disable subscription                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        | Enable subscription                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.30.11.8 SUBSCRIBE\_CALIBRATEOFFSET

Address offset: 0x08C

Subscribe configuration for task **CALIBRATEOFFSET**

|                  |            |  |  |          |    |          |    |    |    |                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|--|----------|----|----------|----|----|----|------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |  | 31       | 30 | 29       | 28 | 27 | 26 | 25                                                         | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |  |  | B        |    |          |    |    |    |                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   |   |   |   |   |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |  | 0        |    |          |    |    |    |                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  |  | Value ID |    | Value    |    |    |    | Description                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |  |          |    | [255..0] |    |    |    | Channel that task <b>CALIBRATEOFFSET</b> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |  | Disabled |    | 0        |    |    |    | Disable subscription                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  |  | Enabled  |    | 1        |    |    |    | Enable subscription                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.30.11.9 EVENTS\_STARTED

Address offset: 0x100

The ADC has started

|                  |            |                |       |                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|------------------|------------|----------------|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|
| Bit number       |            |                |       | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |
| ID               |            |                |       | A                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
| Reset 0x00000000 |            |                |       | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |
| ID               | Acce Field | Value ID       | Value | Description         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
| A                | RW         | EVENTS_STARTED |       | The ADC has started |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            | NotGenerated   | 0     | Event not generated |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            | Generated      | 1     | Event generated     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |

### 7.1.30.11.10 EVENTS\_END

Address offset: 0x104

The ADC has filled up the Result buffer

|                  |               |              |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|---------------|--------------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |               |              |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |               |              |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |               |              |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field    | Value ID     | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW EVENTS_END |              |       | The ADC has filled up the Result buffer                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |               | NotGenerated | 0     | Event not generated                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |               | Generated    | 1     | Event generated                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.30.11.11 EVENTS\_DONE

Address offset: 0x108

A conversion task has been completed. Depending on the mode, multiple conversions might be needed for a result to be transferred to RAM.

|                  |                |              |                                                                                       |                                                                                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|----------------|--------------|---------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |                |              | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |                |              | A                                                                                     |                                                                                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |                |              | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |                                                                                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field     | Value ID     | Value                                                                                 | Description                                                                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW EVENTS_DONE |              |                                                                                       | A conversion task has been completed. Depending on the mode, multiple conversions might be needed for a result to be transferred to RAM. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                | NotGenerated | 0                                                                                     | Event not generated                                                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                | Generated    | 1                                                                                     | Event generated                                                                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.30.11.12 EVENTS\_RESULTDONE

Address offset: 0x10C

A result is ready to get transferred to RAM.

|                  |            |                   |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|-------------------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |                   |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |                   |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |                   |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID          | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | EVENTS_RESULTDONE |       | A result is ready to get transferred to RAM.                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | NotGenerated      | 0     | Event not generated                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Generated         | 1     | Event generated                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.30.11.13 EVENTS\_CALIBRATEDONE

Address offset: 0x110

Calibration is complete



|                  |            |                      |       |                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|------------------|------------|----------------------|-------|-------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|---|
| Bit number       |            |                      |       | 31                      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |   |
| ID               |            |                      |       |                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | A |
| Reset 0x00000000 |            |                      |       | 0                       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |   |
| ID               | Acce Field | Value ID             | Value | Description             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
| A                | RW         | EVENTS_CALIBRATEDONE |       | Calibration is complete |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | NotGenerated         | 0     | Event not generated     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | Generated            | 1     | Event generated         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |

#### 7.1.30.11.14 EVENTS\_STOPPED

Address offset: 0x114

The ADC has stopped

|                  |            |                |       |                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|------------------|------------|----------------|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|---|
| Bit number       |            |                |       | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |   |
| ID               |            |                |       |                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | A |
| Reset 0x00000000 |            |                |       | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |   |
| ID               | Acce Field | Value ID       | Value | Description         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
| A                | RW         | EVENTS_STOPPED |       | The ADC has stopped |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | NotGenerated   | 0     | Event not generated |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | Generated      | 1     | Event generated     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |

#### 7.1.30.11.15 EVENTS\_CH[n].LIMITH (n=0..7)

Address offset: 0x118 + (n × 0x8)

Last results is equal or above CH[n].LIMIT.HIGH

|                  |            |              |       |                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|------------------|------------|--------------|-------|-------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|---|
| Bit number       |            |              |       | 31                                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |   |
| ID               |            |              |       |                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | A |
| Reset 0x00000000 |            |              |       | 0                                               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |   |
| ID               | Acce Field | Value ID     | Value | Description                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
| A                | RW         | LIMITH       |       | Last results is equal or above CH[n].LIMIT.HIGH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | NotGenerated | 0     | Event not generated                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | Generated    | 1     | Event generated                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |

#### 7.1.30.11.16 EVENTS\_CH[n].LIMITL (n=0..7)

Address offset: 0x11C + (n × 0x8)

Last results is equal or below CH[n].LIMIT.LOW

|                  |            |        |              |       |                     |                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|------------------|------------|--------|--------------|-------|---------------------|------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|---|
| Bit number       |            |        |              | 31    | 30                  | 29                                             | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |   |
| ID               |            |        |              |       |                     |                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | A |
| Reset 0x00000000 |            |        |              | 0     | 0                   | 0                                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |   |
| ID               | Acce Field |        | Value ID     | Value |                     | Description                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
| A                | RW         | LIMITL |              |       |                     | Last results is equal or below CH[n].LIMIT.LOW |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            |        | NotGenerated | 0     | Event not generated |                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            |        | Generated    | 1     | Event generated     |                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |

#### 7.1.30.11.17 PUBLISH\_STARTED

Address offset: 0x180

Publish configuration for event **STARTED**

|                  |            |          |          |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|----------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                                                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |          |          | B                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |          | 0                                                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce Field | Value ID | Value    | Description                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] | Channel that event <b>STARTED</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        | Disable publishing                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        | Enable publishing                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.30.11.18 PUBLISH\_END

Address offset: 0x184

Publish configuration for event **END**

|                  |            |  |          |  |          |  |                                                |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|--|----------|--|------------------------------------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          |  |          |  |                                                |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |
| ID               |            |  |          |  |          |  |                                                |  |  | B  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  |    |    |    |   |   |   |   |   |   | A | A | A | A | A | A | A |   |
| Reset 0x00000000 |            |  |          |  |          |  |                                                |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID |  | Value    |  | Description                                    |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          |  | [255..0] |  | Channel that event <b>END</b> will publish to. |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |  |          |  |                                                |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled |  | 0        |  | Disable publishing                             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  |  | 1        |  | Enable publishing                              |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.30.11.19 PUBLISH\_DONE

Address offset: 0x188

Publish configuration for event **DONE**

|                  |            |          |          |                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|-------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |          |          | B                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |          | 0                                               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce Field | Value ID | Value    | Description                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] | Channel that event <b>DONE</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        | Disable publishing                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        | Enable publishing                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.30.11.20 PUBLISH\_RESULTDONE

Address offset: 0x18C

Publish configuration for event **RESULTDONE**

|                  |            |          |          |                                                                         |    |                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|-------------------------------------------------------------------------|----|-------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                                                                      | 30 | 29                                                    | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |          |          | B                                                                       |    |                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |    |                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field |          | Value ID | Value                                                                   |    | Description                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          |          | [255..0]                                                                |    | Channel that event <b>RESULTDONE</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |                                                                         |    |                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled |          | 0                                                                       |    | Disable publishing                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  |          | 1                                                                       |    | Enable publishing                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |



|                  |            |          |          |    |    |    |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|----|----|----|--------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          | 31       | 30 | 29 | 28 | 27                                               | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |          | B        |    |    |    |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   |   |   |   |   |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |          | 0        |    |    |    |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID | Value    |    |    |    | Description                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] |    |    |    | Channel that event CH[n].LIMITL will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |    |    |    |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        |    |    |    | Disable publishing                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        |    |    |    | Enable publishing                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.30.11.25 INTEN

Address offset: 0x300

Enable or disable interrupt

| Bit number       |      |               |          | 31                                          | 30                                                                  | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
|------------------|------|---------------|----------|---------------------------------------------|---------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| ID               |      |               |          | V U T S R Q P O N M L K J I H G F E D C B A |                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |      |               |          | 0                                           | 0                                                                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce | Field         | Value ID | Value                                       | Description                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW   | STARTED       |          |                                             | Enable or disable interrupt for event <a href="#">STARTED</a>       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |               | Disabled | 0                                           | Disable                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |               | Enabled  | 1                                           | Enable                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW   | END           |          |                                             | Enable or disable interrupt for event <a href="#">END</a>           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |               | Disabled | 0                                           | Disable                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |               | Enabled  | 1                                           | Enable                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| C                | RW   | DONE          |          |                                             | Enable or disable interrupt for event <a href="#">DONE</a>          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |               | Disabled | 0                                           | Disable                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |               | Enabled  | 1                                           | Enable                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| D                | RW   | RESULTDONE    |          |                                             | Enable or disable interrupt for event <a href="#">RESULTDONE</a>    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |               | Disabled | 0                                           | Disable                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |               | Enabled  | 1                                           | Enable                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| E                | RW   | CALIBRATEDONE |          |                                             | Enable or disable interrupt for event <a href="#">CALIBRATEDONE</a> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |               | Disabled | 0                                           | Disable                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |               | Enabled  | 1                                           | Enable                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| F                | RW   | STOPPED       |          |                                             | Enable or disable interrupt for event <a href="#">STOPPED</a>       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |               | Disabled | 0                                           | Disable                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |               | Enabled  | 1                                           | Enable                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| G                | RW   | CH0LIMITH     |          |                                             | Enable or disable interrupt for event <a href="#">CH0LIMITH</a>     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |               | Disabled | 0                                           | Disable                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |               | Enabled  | 1                                           | Enable                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| H                | RW   | CH0LIMITL     |          |                                             | Enable or disable interrupt for event <a href="#">CH0LIMITL</a>     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |               | Disabled | 0                                           | Disable                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |               | Enabled  | 1                                           | Enable                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| I                | RW   | CH1LIMITH     |          |                                             | Enable or disable interrupt for event <a href="#">CH1LIMITH</a>     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |               | Disabled | 0                                           | Disable                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |               | Enabled  | 1                                           | Enable                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| J                | RW   | CH1LIMITL     |          |                                             | Enable or disable interrupt for event <a href="#">CH1LIMITL</a>     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |               | Disabled | 0                                           | Disable                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |               | Enabled  | 1                                           | Enable                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| K                | RW   | CH2LIMITH     |          |                                             | Enable or disable interrupt for event <a href="#">CH2LIMITH</a>     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |               | Disabled | 0                                           | Disable                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |               | Enabled  | 1                                           | Enable                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| L                | RW   | CH2LIMITL     |          |                                             | Enable or disable interrupt for event <a href="#">CH2LIMITL</a>     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |               | Disabled | 0                                           | Disable                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

|                  |            |           |          |                                                                         |    |                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
|------------------|------------|-----------|----------|-------------------------------------------------------------------------|----|-----------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|
| Bit number       |            |           |          | 31                                                                      | 30 | 29                                                              | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |
| ID               |            |           |          | V U T S R Q P O N M L K J I H G F E D C B A                             |    |                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
| Reset 0x00000000 |            |           |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |    |                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
| ID               | Acce Field |           | Value ID | Value                                                                   |    | Description                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            |           | Enabled  | 1                                                                       |    | Enable                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
| M                | RW         | CH3LIMITH |          |                                                                         |    | Enable or disable interrupt for event <a href="#">CH3LIMITH</a> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            |           | Disabled | 0                                                                       |    | Disable                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            |           | Enabled  | 1                                                                       |    | Enable                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
| N                | RW         | CH3LIMITL |          |                                                                         |    | Enable or disable interrupt for event <a href="#">CH3LIMITL</a> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            |           | Disabled | 0                                                                       |    | Disable                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            |           | Enabled  | 1                                                                       |    | Enable                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
| O                | RW         | CH4LIMITH |          |                                                                         |    | Enable or disable interrupt for event <a href="#">CH4LIMITH</a> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            |           | Disabled | 0                                                                       |    | Disable                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            |           | Enabled  | 1                                                                       |    | Enable                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
| P                | RW         | CH4LIMITL |          |                                                                         |    | Enable or disable interrupt for event <a href="#">CH4LIMITL</a> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            |           | Disabled | 0                                                                       |    | Disable                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            |           | Enabled  | 1                                                                       |    | Enable                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
| Q                | RW         | CH5LIMITH |          |                                                                         |    | Enable or disable interrupt for event <a href="#">CH5LIMITH</a> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            |           | Disabled | 0                                                                       |    | Disable                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            |           | Enabled  | 1                                                                       |    | Enable                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
| R                | RW         | CH5LIMITL |          |                                                                         |    | Enable or disable interrupt for event <a href="#">CH5LIMITL</a> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            |           | Disabled | 0                                                                       |    | Disable                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            |           | Enabled  | 1                                                                       |    | Enable                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
| S                | RW         | CH6LIMITH |          |                                                                         |    | Enable or disable interrupt for event <a href="#">CH6LIMITH</a> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            |           | Disabled | 0                                                                       |    | Disable                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            |           | Enabled  | 1                                                                       |    | Enable                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
| T                | RW         | CH6LIMITL |          |                                                                         |    | Enable or disable interrupt for event <a href="#">CH6LIMITL</a> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            |           | Disabled | 0                                                                       |    | Disable                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            |           | Enabled  | 1                                                                       |    | Enable                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
| U                | RW         | CH7LIMITH |          |                                                                         |    | Enable or disable interrupt for event <a href="#">CH7LIMITH</a> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            |           | Disabled | 0                                                                       |    | Disable                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            |           | Enabled  | 1                                                                       |    | Enable                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
| V                | RW         | CH7LIMITL |          |                                                                         |    | Enable or disable interrupt for event <a href="#">CH7LIMITL</a> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            |           | Disabled | 0                                                                       |    | Disable                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            |           | Enabled  | 1                                                                       |    | Enable                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |

### 7.1.30.11.26 INTENSET

Address offset: 0x304

## Enable interrupt

|                  |      |         |          |    |       |                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------|---------|----------|----|-------|-----------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |      |         |          |    | 31    | 30                                                              | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |
| ID               |      |         |          |    |       |                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    | V  | U  | T  | S  | R  | Q  | P  | O | N | M | L | K | J | I | H | G | F | E | D | C | B | A |
| Reset 0x00000000 |      |         |          |    | 0     | 0                                                               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce | Field   | Value    | ID | Value | Description                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW   | STARTED |          |    |       | Write '1' to enable interrupt for event <a href="#">STARTED</a> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |         | Set      |    | 1     | Enable                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |         | Disabled |    | 0     | Read: Disabled                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |         | Enabled  |    | 1     | Read: Enabled                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW   | END     |          |    |       | Write '1' to enable interrupt for event <a href="#">END</a>     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |         | Set      |    | 1     | Enable                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |         | Disabled |    | 0     | Read: Disabled                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |         | Enabled  |    | 1     | Read: Enabled                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

| Bit number       |      |               | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|---------------|---------------------------------------------------------------------------------------|-------|-----------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |      |               | V U T S R Q P O N M L K J I H G F E D C B A                                           |       |                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |               | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |       |                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field         | Value ID                                                                              | Value | Description                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW   | DONE          |                                                                                       |       | Write '1' to enable interrupt for event <a href="#">DONE</a>          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Set                                                                                   | 1     | Enable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Disabled                                                                              | 0     | Read: Disabled                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Enabled                                                                               | 1     | Read: Enabled                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| D                | RW   | RESULTDONE    |                                                                                       |       | Write '1' to enable interrupt for event <a href="#">RESULTDONE</a>    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Set                                                                                   | 1     | Enable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Disabled                                                                              | 0     | Read: Disabled                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Enabled                                                                               | 1     | Read: Enabled                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| E                | RW   | CALIBRATEDONE |                                                                                       |       | Write '1' to enable interrupt for event <a href="#">CALIBRATEDONE</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Set                                                                                   | 1     | Enable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Disabled                                                                              | 0     | Read: Disabled                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Enabled                                                                               | 1     | Read: Enabled                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| F                | RW   | STOPPED       |                                                                                       |       | Write '1' to enable interrupt for event <a href="#">STOPPED</a>       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Set                                                                                   | 1     | Enable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Disabled                                                                              | 0     | Read: Disabled                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Enabled                                                                               | 1     | Read: Enabled                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| G                | RW   | CH0LIMITH     |                                                                                       |       | Write '1' to enable interrupt for event <a href="#">CH0LIMITH</a>     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Set                                                                                   | 1     | Enable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Disabled                                                                              | 0     | Read: Disabled                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Enabled                                                                               | 1     | Read: Enabled                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| H                | RW   | CH0LIMITL     |                                                                                       |       | Write '1' to enable interrupt for event <a href="#">CH0LIMITL</a>     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Set                                                                                   | 1     | Enable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Disabled                                                                              | 0     | Read: Disabled                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Enabled                                                                               | 1     | Read: Enabled                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| I                | RW   | CH1LIMITH     |                                                                                       |       | Write '1' to enable interrupt for event <a href="#">CH1LIMITH</a>     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Set                                                                                   | 1     | Enable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Disabled                                                                              | 0     | Read: Disabled                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Enabled                                                                               | 1     | Read: Enabled                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| J                | RW   | CH1LIMITL     |                                                                                       |       | Write '1' to enable interrupt for event <a href="#">CH1LIMITL</a>     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Set                                                                                   | 1     | Enable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Disabled                                                                              | 0     | Read: Disabled                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Enabled                                                                               | 1     | Read: Enabled                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| K                | RW   | CH2LIMITH     |                                                                                       |       | Write '1' to enable interrupt for event <a href="#">CH2LIMITH</a>     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Set                                                                                   | 1     | Enable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Disabled                                                                              | 0     | Read: Disabled                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Enabled                                                                               | 1     | Read: Enabled                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| L                | RW   | CH2LIMITL     |                                                                                       |       | Write '1' to enable interrupt for event <a href="#">CH2LIMITL</a>     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Set                                                                                   | 1     | Enable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Disabled                                                                              | 0     | Read: Disabled                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Enabled                                                                               | 1     | Read: Enabled                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| M                | RW   | CH3LIMITH     |                                                                                       |       | Write '1' to enable interrupt for event <a href="#">CH3LIMITH</a>     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Set                                                                                   | 1     | Enable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Disabled                                                                              | 0     | Read: Disabled                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Enabled                                                                               | 1     | Read: Enabled                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| N                | RW   | CH3LIMITL     |                                                                                       |       | Write '1' to enable interrupt for event <a href="#">CH3LIMITL</a>     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Set                                                                                   | 1     | Enable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Disabled                                                                              | 0     | Read: Disabled                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Enabled                                                                               | 1     | Read: Enabled                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| O                | RW   | CH4LIMITH     |                                                                                       |       | Write '1' to enable interrupt for event <a href="#">CH4LIMITH</a>     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Set                                                                                   | 1     | Enable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

| Bit number       |      |           | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|-----------|---------------------------------------------------------------------------------------|-------|-------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |      |           | V U T S R Q P O N M L K J I H G F E D C B A                                           |       |                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |           | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |       |                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field     | Value ID                                                                              | Value | Description                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| P                | RW   | CH4LIMITL | Disabled                                                                              | 0     | Read: Disabled                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Enabled                                                                               | 1     | Read: Enabled                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Set                                                                                   | 1     | Write '1' to enable interrupt for event <a href="#">CH4LIMITL</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Disabled                                                                              | 0     | Read: Disabled                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Enabled                                                                               | 1     | Read: Enabled                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Q                | RW   | CH5LIMITH |                                                                                       |       | Write '1' to enable interrupt for event <a href="#">CH5LIMITH</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Set                                                                                   | 1     | Enable                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Disabled                                                                              | 0     | Read: Disabled                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Enabled                                                                               | 1     | Read: Enabled                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           |                                                                                       |       |                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| R                | RW   | CH5LIMITL |                                                                                       |       | Write '1' to enable interrupt for event <a href="#">CH5LIMITL</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Set                                                                                   | 1     | Enable                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Disabled                                                                              | 0     | Read: Disabled                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Enabled                                                                               | 1     | Read: Enabled                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           |                                                                                       |       |                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| S                | RW   | CH6LIMITH |                                                                                       |       | Write '1' to enable interrupt for event <a href="#">CH6LIMITH</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Set                                                                                   | 1     | Enable                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Disabled                                                                              | 0     | Read: Disabled                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Enabled                                                                               | 1     | Read: Enabled                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           |                                                                                       |       |                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| T                | RW   | CH6LIMITL |                                                                                       |       | Write '1' to enable interrupt for event <a href="#">CH6LIMITL</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Set                                                                                   | 1     | Enable                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Disabled                                                                              | 0     | Read: Disabled                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Enabled                                                                               | 1     | Read: Enabled                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           |                                                                                       |       |                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| U                | RW   | CH7LIMITH |                                                                                       |       | Write '1' to enable interrupt for event <a href="#">CH7LIMITH</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Set                                                                                   | 1     | Enable                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Disabled                                                                              | 0     | Read: Disabled                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Enabled                                                                               | 1     | Read: Enabled                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           |                                                                                       |       |                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| V                | RW   | CH7LIMITL |                                                                                       |       | Write '1' to enable interrupt for event <a href="#">CH7LIMITL</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Set                                                                                   | 1     | Enable                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Disabled                                                                              | 0     | Read: Disabled                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Enabled                                                                               | 1     | Read: Enabled                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           |                                                                                       |       |                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.30.11.27 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|--------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |            |          | V U T S R Q P O N M L K J I H G F E D C B A                                           |                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW STARTED |          |                                                                                       | Write '1' to disable interrupt for event STARTED |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Clear    | 1                                                                                     | Disable                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Read: Disabled                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Read: Enabled                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW END     |          |                                                                                       | Write '1' to disable interrupt for event END     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Clear    | 1                                                                                     | Disable                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Read: Disabled                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Read: Enabled                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW DONE    |          |                                                                                       | Write '1' to disable interrupt for event DONE    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

| Bit number       |      |               | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|---------------|---------------------------------------------------------------------------------------|-------|------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |      |               | V U T S R Q P O N M L K J I H G F E D C B A                                           |       |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |               | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |       |                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field         | Value ID                                                                              | Value | Description                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Clear                                                                                 | 1     | Disable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Disabled                                                                              | 0     | Read: Disabled                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Enabled                                                                               | 1     | Read: Enabled                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| D                | RW   | RESULTDONE    |                                                                                       |       | Write '1' to disable interrupt for event <a href="#">RESULTDONE</a>    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Clear                                                                                 | 1     | Disable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Disabled                                                                              | 0     | Read: Disabled                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Enabled                                                                               | 1     | Read: Enabled                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| E                | RW   | CALIBRATEDONE |                                                                                       |       | Write '1' to disable interrupt for event <a href="#">CALIBRATEDONE</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Clear                                                                                 | 1     | Disable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Disabled                                                                              | 0     | Read: Disabled                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Enabled                                                                               | 1     | Read: Enabled                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| F                | RW   | STOPPED       |                                                                                       |       | Write '1' to disable interrupt for event <a href="#">STOPPED</a>       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Clear                                                                                 | 1     | Disable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Disabled                                                                              | 0     | Read: Disabled                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Enabled                                                                               | 1     | Read: Enabled                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| G                | RW   | CH0LIMITH     |                                                                                       |       | Write '1' to disable interrupt for event <a href="#">CH0LIMITH</a>     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Clear                                                                                 | 1     | Disable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Disabled                                                                              | 0     | Read: Disabled                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Enabled                                                                               | 1     | Read: Enabled                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| H                | RW   | CH0LIMITL     |                                                                                       |       | Write '1' to disable interrupt for event <a href="#">CH0LIMITL</a>     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Clear                                                                                 | 1     | Disable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Disabled                                                                              | 0     | Read: Disabled                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Enabled                                                                               | 1     | Read: Enabled                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| I                | RW   | CH1LIMITH     |                                                                                       |       | Write '1' to disable interrupt for event <a href="#">CH1LIMITH</a>     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Clear                                                                                 | 1     | Disable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Disabled                                                                              | 0     | Read: Disabled                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Enabled                                                                               | 1     | Read: Enabled                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| J                | RW   | CH1LIMITL     |                                                                                       |       | Write '1' to disable interrupt for event <a href="#">CH1LIMITL</a>     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Clear                                                                                 | 1     | Disable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Disabled                                                                              | 0     | Read: Disabled                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Enabled                                                                               | 1     | Read: Enabled                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| K                | RW   | CH2LIMITH     |                                                                                       |       | Write '1' to disable interrupt for event <a href="#">CH2LIMITH</a>     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Clear                                                                                 | 1     | Disable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Disabled                                                                              | 0     | Read: Disabled                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Enabled                                                                               | 1     | Read: Enabled                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| L                | RW   | CH2LIMITL     |                                                                                       |       | Write '1' to disable interrupt for event <a href="#">CH2LIMITL</a>     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Clear                                                                                 | 1     | Disable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Disabled                                                                              | 0     | Read: Disabled                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Enabled                                                                               | 1     | Read: Enabled                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| M                | RW   | CH3LIMITH     |                                                                                       |       | Write '1' to disable interrupt for event <a href="#">CH3LIMITH</a>     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Clear                                                                                 | 1     | Disable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Disabled                                                                              | 0     | Read: Disabled                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Enabled                                                                               | 1     | Read: Enabled                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| N                | RW   | CH3LIMITL     |                                                                                       |       | Write '1' to disable interrupt for event <a href="#">CH3LIMITL</a>     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Clear                                                                                 | 1     | Disable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Disabled                                                                              | 0     | Read: Disabled                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Enabled                                                                               | 1     | Read: Enabled                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| O                | RW   | CH4LIMITH     |                                                                                       |       | Write '1' to disable interrupt for event <a href="#">CH4LIMITH</a>     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Clear                                                                                 | 1     | Disable                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |               | Disabled                                                                              | 0     | Read: Disabled                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |



| Bit number       |      |           | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|-----------|---------------------------------------------------------------------------------------|-------|--------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |      |           | V U T S R Q P O N M L K J I H G F E D C B A                                           |       |                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |           | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |       |                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field     | Value ID                                                                              | Value | Description                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| P                | RW   | CH4LIMITL | Enabled                                                                               | 1     | Read: Enabled                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Clear                                                                                 | 1     | Write '1' to disable interrupt for event <a href="#">CH4LIMITL</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Disabled                                                                              | 0     | Disable                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Enabled                                                                               | 1     | Read: Disabled                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Q                | RW   | CH5LIMITH | Enabled                                                                               | 1     | Read: Enabled                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Clear                                                                                 | 1     | Write '1' to disable interrupt for event <a href="#">CH5LIMITH</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Disabled                                                                              | 0     | Disable                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Enabled                                                                               | 1     | Read: Disabled                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| R                | RW   | CH5LIMITL | Enabled                                                                               | 1     | Read: Enabled                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Clear                                                                                 | 1     | Write '1' to disable interrupt for event <a href="#">CH5LIMITL</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Disabled                                                                              | 0     | Disable                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Enabled                                                                               | 1     | Read: Disabled                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| S                | RW   | CH6LIMITH | Enabled                                                                               | 1     | Read: Enabled                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Clear                                                                                 | 1     | Write '1' to disable interrupt for event <a href="#">CH6LIMITH</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Disabled                                                                              | 0     | Disable                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Enabled                                                                               | 1     | Read: Disabled                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| T                | RW   | CH6LIMITL | Enabled                                                                               | 1     | Read: Enabled                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Clear                                                                                 | 1     | Write '1' to disable interrupt for event <a href="#">CH6LIMITL</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Disabled                                                                              | 0     | Disable                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Enabled                                                                               | 1     | Read: Disabled                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| U                | RW   | CH7LIMITH | Enabled                                                                               | 1     | Read: Enabled                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Clear                                                                                 | 1     | Write '1' to disable interrupt for event <a href="#">CH7LIMITH</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Disabled                                                                              | 0     | Disable                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Enabled                                                                               | 1     | Read: Disabled                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| V                | RW   | CH7LIMITL | Enabled                                                                               | 1     | Read: Enabled                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Clear                                                                                 | 1     | Write '1' to disable interrupt for event <a href="#">CH7LIMITL</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Disabled                                                                              | 0     | Disable                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Enabled                                                                               | 1     | Read: Disabled                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.30.11.28 STATUS

Address offset: 0x400

Status

|                  |            |        |          |                                                                                       |                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|--------|----------|---------------------------------------------------------------------------------------|---------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |        |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |        |          | A                                                                                     |                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |        |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field |        | Value ID | Value                                                                                 | Description                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | R          | STATUS |          |                                                                                       | Status                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |        | Ready    | 0                                                                                     | ADC is ready. No on-going conversion.       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |        | Busy     | 1                                                                                     | ADC is busy. Single conversion in progress. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.30.11.29 ENABLE

Address offset: 0x500

Enable or disable ADC

|                  |      |        |          |    |       |    |                                                                                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------|--------|----------|----|-------|----|----------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |      |        |          | 31 | 30    | 29 | 28                                                                                                                         | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |      |        |          |    |       |    |                                                                                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | A |   |   |   |
| Reset 0x00000000 |      |        |          | 0  | 0     | 0  | 0                                                                                                                          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce | Field  | Value    | ID | Value |    | Description                                                                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW   | ENABLE |          |    |       |    | Enable or disable ADC                                                                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |        | Disabled |    | 0     |    | Disable ADC                                                                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |        | Enabled  |    | 1     |    | Enable ADC                                                                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |        |          |    |       |    | When enabled, the ADC will acquire access to the analog input pins specified in the CH[n].PSELP and CH[n].PSELN registers. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.30.11.30 CH[n].PSELP (n=0..7)

Address offset:  $0x510 + (n \times 0x10)$

Input positive pin selection for CH[n]

| Bit number       |            |              | 31    | 30 | 29                            | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |  |
|------------------|------------|--------------|-------|----|-------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|--|
| ID               |            |              |       |    |                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A | A | A | A | A |  |
| Reset 0x00000000 |            |              | 0     | 0  | 0                             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |  |
| ID               | Acce Field | Value ID     | Value |    | Description                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| A                | RW         | PSELP        |       |    | Analog positive input channel |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | NC           | 0     |    | Not connected                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | AnalogInput0 | 1     |    | AIN0                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | AnalogInput1 | 2     |    | AIN1                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | AnalogInput2 | 3     |    | AIN2                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | AnalogInput3 | 4     |    | AIN3                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | AnalogInput4 | 5     |    | AIN4                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | AnalogInput5 | 6     |    | AIN5                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | AnalogInput6 | 7     |    | AIN6                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | AnalogInput7 | 8     |    | AIN7                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | VDD          | 9     |    | VDD                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | VDDHDIV5     | 0xD   |    | VDDH/5                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |  |

### 7.1.30.11.31 CH[n].PSELN (n=0..7)

Address offset:  $0x514 + (n \times 0x10)$

Input negative pin selection for CH[n]

| Bit number       |      |       |              | 31 | 30            | 29                                                  | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |
|------------------|------|-------|--------------|----|---------------|-----------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ID               |      |       |              |    |               |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A | A | A | A | A |
| Reset 0x00000000 |      |       |              | 0  | 0             | 0                                                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |   |
| ID               | Acce | Field | Value        | ID | Value         | Description                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW   | PSELN |              |    |               | Analog negative input, enables differential channel |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |       | NC           | 0  | Not connected |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |       | AnalogInput0 | 1  | AIN0          |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |       | AnalogInput1 | 2  | AIN1          |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |       | AnalogInput2 | 3  | AIN2          |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |       | AnalogInput3 | 4  | AIN3          |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |       | AnalogInput4 | 5  | AIN4          |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |       | AnalogInput5 | 6  | AIN5          |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |       | AnalogInput6 | 7  | AIN6          |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |       | AnalogInput7 | 8  | AIN7          |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

|                  |            |          |                                                                       |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|-----------------------------------------------------------------------|----|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          | 31                                                                    | 30 | 29          | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |          | A A A A A                                                             |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field | Value ID | Value                                                                 |    | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | VDD      | 9                                                                     |    | VDD         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | VDDHDIV5 | 0xD                                                                   |    | VDDH/5      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.30.11.32 CH[n].CONFIG (n=0..7)

Address offset:  $0x518 + (n \times 0x10)$

Input configuration for CH[n]

| Bit number       |      |          | 31    | 30                                                                        | 29    | 28                                                                  | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
|------------------|------|----------|-------|---------------------------------------------------------------------------|-------|---------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| ID               |      |          | G     |                                                                           |       |                                                                     |    |    |    |    |    |    |    |    |    |    |    |    | F  | E  | E  | E  | D  |    |   | C | C | C | B |   |   | B | A |   |   | A |
| Reset 0x00020000 |      |          | 0     | 0                                                                         | 0     | 0                                                                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |
| ID               | Acce | Field    | Value | ID                                                                        | Value | Description                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW   | RESP     |       |                                                                           |       | Positive channel resistor control                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      | Bypass   | 0     | Bypass resistor ladder                                                    |       |                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      | Pulldown | 1     | Pull-down to GND                                                          |       |                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      | Pullup   | 2     | Pull-up to VDD                                                            |       |                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      | VDD1_2   | 3     | Set input at VDD/2                                                        |       |                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW   | RESN     |       |                                                                           |       | Negative channel resistor control                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      | Bypass   | 0     | Bypass resistor ladder                                                    |       |                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      | Pulldown | 1     | Pull-down to GND                                                          |       |                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      | Pullup   | 2     | Pull-up to VDD                                                            |       |                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      | VDD1_2   | 3     | Set input at VDD/2                                                        |       |                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| C                | RW   | GAIN     |       |                                                                           |       | Gain control                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      | Gain1_6  | 0     | 1/6                                                                       |       |                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      | Gain1_5  | 1     | 1/5                                                                       |       |                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      | Gain1_4  | 2     | 1/4                                                                       |       |                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      | Gain1_3  | 3     | 1/3                                                                       |       |                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      | Gain1_2  | 4     | 1/2                                                                       |       |                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      | Gain1    | 5     | 1                                                                         |       |                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      | Gain2    | 6     | 2                                                                         |       |                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      | Gain4    | 7     | 4                                                                         |       |                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| D                | RW   | REFSEL   |       |                                                                           |       | Reference control                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      | Internal | 0     | Internal reference (0.6 V)                                                |       |                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      | VDD1_4   | 1     | VDD/4 as reference                                                        |       |                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| E                | RW   | TACQ     |       |                                                                           |       | Acquisition time, the time the ADC uses to sample the input voltage |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      | 3us      | 0     | 3 us                                                                      |       |                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      | 5us      | 1     | 5 us                                                                      |       |                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      | 10us     | 2     | 10 us                                                                     |       |                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      | 15us     | 3     | 15 us                                                                     |       |                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      | 20us     | 4     | 20 us                                                                     |       |                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      | 40us     | 5     | 40 us                                                                     |       |                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| F                | RW   | MODE     |       |                                                                           |       | Enable differential mode                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      | SE       | 0     | Single ended, PSELN will be ignored, negative input to ADC shorted to GND |       |                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      | Diff     | 1     | Differential                                                              |       |                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| G                | RW   | BURST    |       |                                                                           |       | Enable burst mode                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      | Disabled | 0     | Burst mode is disabled (normal operation)                                 |       |                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

|                  |  |  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               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### 7.1.30.11.33 CH[n].LIMIT (n=0..7)

Address offset: 0x51C + (n × 0x10)

High/low limits for event monitoring a channel

|                  |            |          |  |                    |    |    |    |                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|--|--------------------|----|----|----|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |  | 31                 | 30 | 29 | 28 | 27               | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |          |  | B                  | B  | B  | B  | B                | B  | B  | B  | B  | B  | B  | B  | B  | B  | B  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x7FFF8000 |            |          |  | 0                  | 1  | 1  | 1  | 1                | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID |  | Value              |    |    |    | Description      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW LOW     |          |  | [-32768 to +32767] |    |    |    | Low level limit  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| B                | RW HIGH    |          |  | [-32768 to +32767] |    |    |    | High level limit |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.30.11.34 RESOLUTION

Address offset: 0x5F0

Resolution configuration

|                  |            |  |          |  |       |  |                    |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|--|-------|--|--------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          |  |       |  |                    |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |  |          |  |       |  |                    |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | A | A | A |   |
| Reset 0x00000001 |            |  |          |  |       |  |                    |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| ID               | Acce Field |  | Value ID |  | Value |  | Description        |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW VAL     |  |          |  |       |  | Set the resolution |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | 8bit     |  | 0     |  | 8 bit              |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | 10bit    |  | 1     |  | 10 bit             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | 12bit    |  | 2     |  | 12 bit             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | 14bit    |  | 3     |  | 14 bit             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.30.11.35 OVERSAMPLE

Address offset: 0x5F4

Oversampling configuration. OVERSAMPLE should not be combined with SCAN. The RESOLUTION is applied before averaging, thus for high OVERSAMPLE a higher RESOLUTION should be used.

|                  |      |            |          |                                                                                       |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|------------|----------|---------------------------------------------------------------------------------------|---------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |            |          | A A A A                                                                               |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field      | Value ID | Value                                                                                 | Description         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW   | OVERSAMPLE |          |                                                                                       | Oversample control  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |            | Bypass   | 0                                                                                     | Bypass oversampling |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |            | Over2x   | 1                                                                                     | Oversample 2x       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |            | Over4x   | 2                                                                                     | Oversample 4x       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |            | Over8x   | 3                                                                                     | Oversample 8x       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |            | Over16x  | 4                                                                                     | Oversample 16x      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

|                  |      |       |          |       |    |    |                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
|------------------|------|-------|----------|-------|----|----|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|
| Bit number       |      |       |          | 31    | 30 | 29 | 28              | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |
| ID               |      |       |          |       |    |    |                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | A | A | A | A |  |  |
| Reset 0x00000000 |      |       |          | 0     | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |
| ID               | Acce | Field | Value ID | Value |    |    | Description     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |       | Over32x  | 5     |    |    | Oversample 32x  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |       | Over64x  | 6     |    |    | Oversample 64x  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |       | Over128x | 7     |    |    | Oversample 128x |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |       | Over256x | 8     |    |    | Oversample 256x |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |

### 7.1.30.11.36 SAMPLERATE

Address offset: 0x5F8

Controls normal or continuous sample rate

| Bit number       |      |       |          | 31         | 30                                                               | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |
|------------------|------|-------|----------|------------|------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ID               |      |       |          |            |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | B  | A  | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |      |       |          | 0          | 0                                                                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |   |   |   |
| ID               | Acce | Field | Value ID | Value      | Description                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW   | CC    |          | [80..2047] | Capture and compare value. Sample rate is 16 MHz/CC              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW   | MODE  |          |            | Select mode for sample rate control                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |       | Task     | 0          | Rate is controlled from SAMPLE task                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |       | Timers   | 1          | Rate is controlled from local timer (use CC to control the rate) |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.30.11.37 RESULT.PTR

Address offset: 0x62C

Data pointer

|                  |            |  |  |          |  |  |       |  |  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|--|----------|--|--|-------|--|--|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |  |          |  |  |       |  |  | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |  |  |          |  |  |       |  |  | A            | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |  |          |  |  |       |  |  | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  |  | Value ID |  |  | Value |  |  | Description  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW PTR     |  |  |          |  |  |       |  |  | Data pointer |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

**Note:** See the memory chapter for details about which memories are available for EasyDMA.

### 7.1.30.11.38 RESULT.MAXCNT

Address offset: 0x630

Maximum number of buffer words to transfer

|                  |            |  |          |       |    |                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|-------|----|--------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31    | 30 | 29                                         | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |  |          |       |    |                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |          | 0     | 0  | 0                                          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field |  | Value ID | Value |    | Description                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW MAXCNT  |  |          |       |    | Maximum number of buffer words to transfer |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.30.11.39 RESULT.AMOUNT

Address offset: 0x634

Number of buffer words transferred since last START

|                  |      |        |       |    |       |                                                                                                               |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------|--------|-------|----|-------|---------------------------------------------------------------------------------------------------------------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |      |        |       | 31 | 30    | 29                                                                                                            | 28          | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |      |        |       |    |       |                                                                                                               |             |    |    |    |    |    |    |    |    |    |    |    |    | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |      |        |       | 0  | 0     | 0                                                                                                             | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce | Field  | Value | ID | Value |                                                                                                               | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | R    | AMOUNT |       |    |       | Number of buffer words transferred since last START. This register can be read after an END or STOPPED event. |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

## 7.1.30.12 Electrical specification

### 7.1.30.12.1 SAADC Electrical Specification

| Symbol                | Description                                                                                                                       | Min. | Typ. | Max. | Units  |
|-----------------------|-----------------------------------------------------------------------------------------------------------------------------------|------|------|------|--------|
| DNL <sub>10</sub>     | Differential non-linearity, 10-bit resolution                                                                                     | ..   | ..   | ..   | LSB10b |
| INL <sub>10</sub>     | Integral non-linearity, 10-bit resolution                                                                                         | ..   | ..   | ..   | LSB10b |
| V <sub>OS</sub>       | Differential offset error (calibrated), 10-bit resolution <sup>a</sup>                                                            | ..   | ..   | ..   | LSB10b |
| E <sub>VDDHDIV5</sub> | Error on VDDHDIV5 input                                                                                                           | ..   | ..   | ..   | %      |
| C <sub>EG</sub>       | Gain error temperature coefficient                                                                                                | ..   | ..   | ..   | %/°C   |
| f <sub>SAMPLE</sub>   | Maximum sampling rate                                                                                                             | ..   | ..   | ..   | kHz    |
| t <sub>ACQ,10k</sub>  | Acquisition time (configurable), source Resistance <= 10kOhm                                                                      | ..   | ..   | ..   | μs     |
| t <sub>ACQ,40k</sub>  | Acquisition time (configurable), source Resistance <= 40kOhm                                                                      | ..   | ..   | ..   | μs     |
| t <sub>ACQ,100k</sub> | Acquisition time (configurable), source Resistance <= 100kOhm                                                                     | ..   | ..   | ..   | μs     |
| t <sub>ACQ,200k</sub> | Acquisition time (configurable), source Resistance <= 200kOhm                                                                     | ..   | ..   | ..   | μs     |
| t <sub>ACQ,400k</sub> | Acquisition time (configurable), source Resistance <= 400kOhm                                                                     | ..   | ..   | ..   | μs     |
| t <sub>ACQ,800k</sub> | Acquisition time (configurable), source Resistance <= 800kOhm                                                                     | ..   | ..   | ..   | μs     |
| t <sub>CONV</sub>     | Conversion time                                                                                                                   | ..   | ..   | ..   | μs     |
| E <sub>G1/6</sub>     | Error <sup>b</sup> for Gain = 1/6                                                                                                 | ..   | ..   | ..   | %      |
| E <sub>G1/4</sub>     | Error <sup>b</sup> for Gain = 1/4                                                                                                 | ..   | ..   | ..   | %      |
| E <sub>G1/2</sub>     | Error <sup>b</sup> for Gain = 1/2                                                                                                 | ..   | ..   | ..   | %      |
| E <sub>G1</sub>       | Error <sup>b</sup> for Gain = 1                                                                                                   | ..   | ..   | ..   | %      |
| C <sub>SAMPLE</sub>   | Sample and hold capacitance at maximum gain <sup>21</sup>                                                                         | ..   | ..   | ..   | pF     |
| R <sub>INPUT</sub>    | Input resistance                                                                                                                  | ..   | ..   | ..   | MΩ     |
| E <sub>NOB</sub>      | Effective number of bits, differential mode, 12-bit resolution, 1/1 gain, 3 μs acquisition time, HFXO, 200 ksp/s                  | ..   | ..   | ..   | Bit    |
| S <sub>NDR</sub>      | Peak signal to noise and distortion ratio, differential mode, 12-bit resolution, 1/1 gain, 3 μs acquisition time, HFXO, 200 ksp/s | ..   | ..   | ..   | dB     |
| S <sub>FDR</sub>      | Spurious free dynamic range, differential mode, 12-bit resolution, 1/1 gain, 3 μs acquisition time, HFXO, 200 ksp/s               | ..   | ..   | ..   | dBc    |
| R <sub>LADDER</sub>   | Ladder resistance                                                                                                                 | ..   | ..   | ..   | kΩ     |

<sup>a</sup> Digital output code at zero volt differential input.

<sup>b</sup> Does not include temperature drift

<sup>21</sup> Maximum gain corresponds to highest capacitance.

### 7.1.30.13 Performance factors

Clock jitter, affecting sample timing accuracy, and circuit noise can affect ADC performance.

Jitter can be between START tasks or from START task to acquisition. START timer accuracy and startup times of regulators and references will contribute to variability. Sources of circuit noise may include CPU activity and the DC/DC regulator. Best ADC performance is achieved using START timing based on the TIMER module, HFXO clock source, and Constant Latency mode.

### 7.1.31 SPIM — Serial peripheral interface master with EasyDMA

The SPI master can communicate with multiple SPI slaves using individual chip select signals for each slave.

Listed here are the main features for the SPIM

- EasyDMA direct transfer to/from RAM
- SPI mode 0-3
- Individual selection of I/O pins
- Optional D/CX output line for distinguishing between command and data bytes

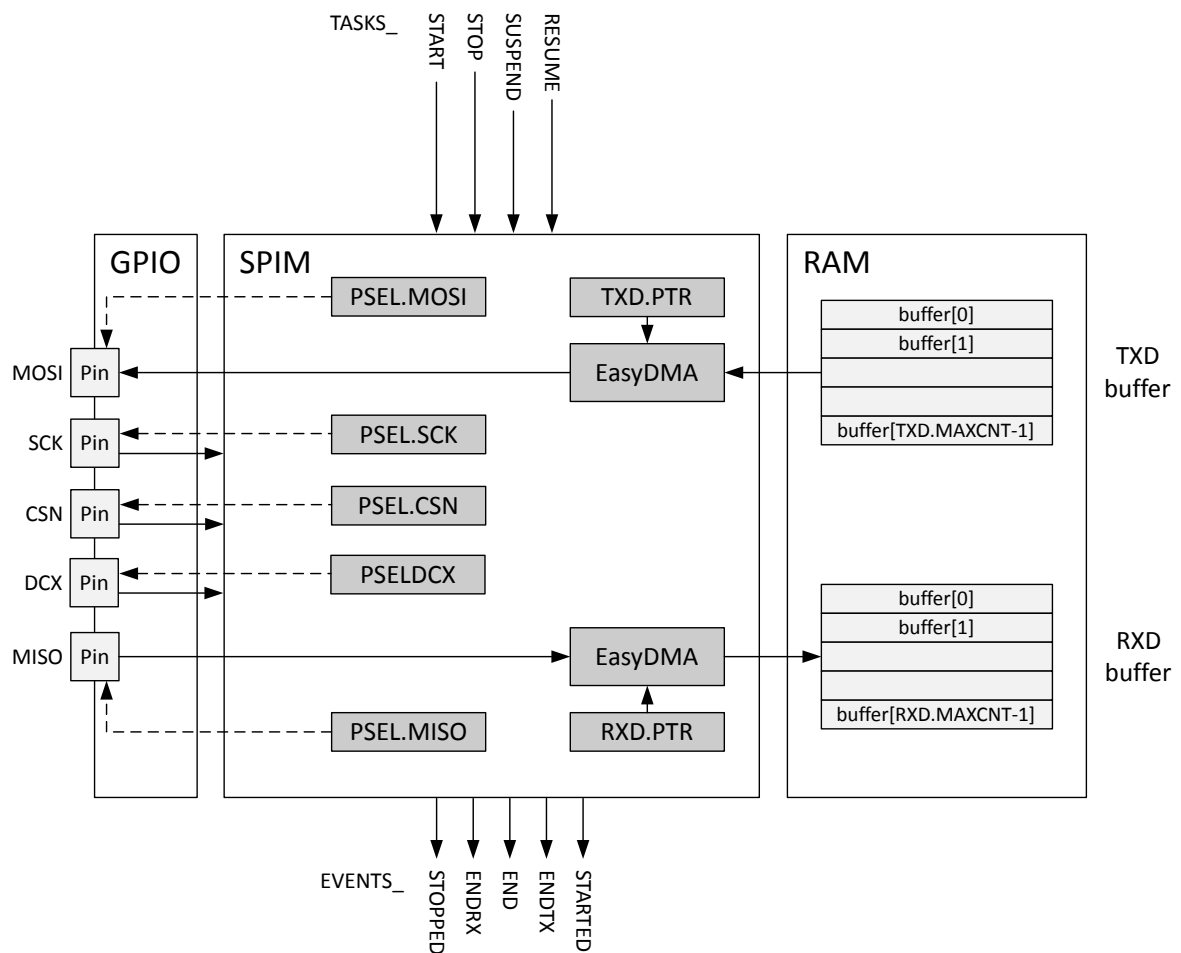


Figure 190: SPIM — SPI master with EasyDMA

### 7.1.31.1 SPI master transaction sequence

An SPI master transaction is started by triggering the START task. When started, a number of bytes will be transmitted/received on MOSI/MISO.

The following figure illustrates an SPI master transaction:

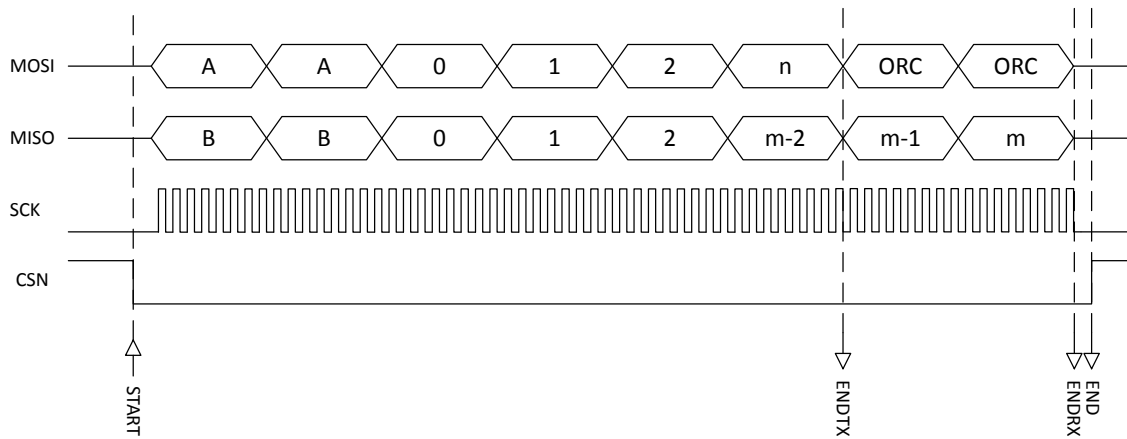


Figure 191: SPI master transaction

The ENDTX is generated when all bytes in buffer `TXD.PTR` on page 546 are transmitted. The number of bytes in the transmit buffer is specified in register `TXD.MAXCNT` on page 546. The ENDRX event will be generated when buffer `RXD.PTR` on page 545 is full, that is when the number of bytes specified in register `RXD.MAXCNT` on page 545 have been received. The transaction stops automatically after all bytes have been transmitted/received. When the maximum number of bytes in receive buffer is larger than the number of bytes in the transmit buffer, the contents of register `ORC` on page 549 will be transmitted after the last byte in the transmit buffer has been transmitted.

The END event will be generated after both the ENDRX and ENDTX events have been generated.

The SPI master can be stopped in the middle of a transaction by triggering the STOP task. When triggering the STOP task the SPIM will complete the transmission/reception of the current byte before stopping. A STOPPED event is generated when the SPI master has stopped.

If the ENDTX event has not already been generated when the SPI master has come to a stop, the ENDTX event will be generated even if all bytes in the buffer `TXD.PTR` on page 546 have not been transmitted.

If the ENDRX event has not already been generated when the SPI master has come to a stop, the ENDRX event will be generated even if the buffer `RXD.PTR` on page 545 is not full.

A transaction can be suspended and resumed using the SUSPEND and RESUME tasks, receptively. When the SUSPEND task is triggered the SPI master will complete transmitting and receiving the current ongoing byte before it is suspended.

### 7.1.31.2 D/CX functionality

Some SPI slaves, for example display drivers, require an additional signal from the SPI master to distinguish between command and data bytes. For display drivers this line is often called D/CX.

The SPIM provides support for such a D/CX output line. The D/CX line is set low during transmission of command bytes and high during transmission of data bytes.

The D/CX pin number is selected using `PSELDCX` on page 548 and the number of command bytes preceding the data bytes is configured using `DCXCNT` on page 548.



It is not allowed to write to the [DCXCNT](#) on page 548 during an ongoing transmission.

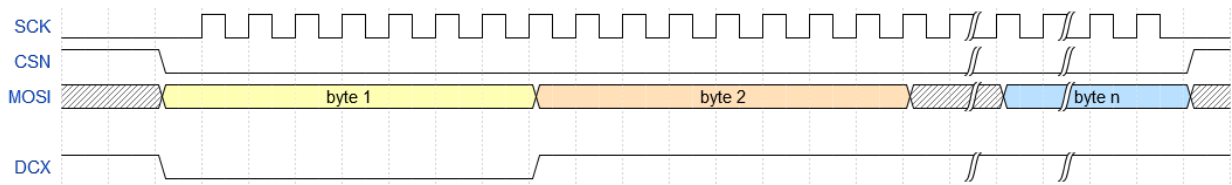


Figure 192: D/CX example. *SPIM.DCXCNT = 1.*

### 7.1.31.3 Pin configuration

The SCK, CSN, DCX, MOSI, and MISO signals associated with the SPIM are mapped to physical pins according to the configuration specified in the PSEL.n registers.

The contents of registers [PSEL.SCK](#) on page 543, [PSEL.CSN](#) on page 544, [PSELDCX](#) on page 548, [PSEL.MOSI](#) on page 543 and [PSEL.MISO](#) on page 544 are only used when the SPIM is enabled and retained only as long as the device is in System ON mode. The PSEL.n registers can only be configured when the SPIM is disabled. Enabling/disabling is done using register [ENABLE](#) on page 543.

To ensure correct behavior, the pins used by the SPIM must be configured in the GPIO peripheral as described in [Table 142: GPIO configuration](#) on page 533 before the SPIM is enabled.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

| SPI master signal | SPI master pin                                        | Direction | Output value        | Comments |
|-------------------|-------------------------------------------------------|-----------|---------------------|----------|
| SCK               | As specified in <a href="#">PSEL.SCK</a> on page 543  | Output    | Same as CONFIG.CPOL |          |
| CSN               | As specified in <a href="#">PSEL.CSN</a> on page 544  | Output    | Same as CONFIG.CPOL |          |
| DCX               | As specified in <a href="#">PSELDCX</a> on page 548   | Output    | 1                   |          |
| MOSI              | As specified in <a href="#">PSEL.MOSI</a> on page 543 | Output    | 0                   |          |
| MISO              | As specified in <a href="#">PSEL.MISO</a> on page 544 | Input     | Not applicable      |          |

Table 142: GPIO configuration

Some SPIM instances do not support automatic control of CSN, and for those the available GPIO pins need to be used to control CSN directly. See [Table 145: Instances](#) on page 535 for information about what features are supported in the various SPIM instances.

The SPIM supports SPI modes 0 through 3. The clock polarity (CPOL) and the clock phase (CPHA) are configured in register [CONFIG](#) on page 547.

| Mode      | Clock polarity  | Clock phase  |
|-----------|-----------------|--------------|
|           | CPOL            | CPHA         |
| SPI_MODE0 | 0 (Active High) | 0 (Leading)  |
| SPI_MODE1 | 0 (Active High) | 1 (Trailing) |
| SPI_MODE2 | 1 (Active Low)  | 0 (Leading)  |
| SPI_MODE3 | 1 (Active Low)  | 1 (Trailing) |

Table 143: SPI modes

### 7.1.31.4 Shared resources

The SPI shares registers and other resources with other peripherals that have the same ID as the SPI. Therefore, the user must disable all peripherals that have the same ID as the SPI before the SPI can be configured and used.

Disabling a peripheral that has the same ID as the SPI will not reset any of the registers that are shared with the SPI. It is therefore important to configure all relevant SPI registers explicitly to secure that it operates correctly.

See the Instantiation table in [Instantiation](#) on page 136 for details on peripherals and their IDs.

### 7.1.31.5 EasyDMA

The SPIM implements EasyDMA for accessing RAM without CPU involvement.

The SPIM peripheral implements the following EasyDMA channels:

| Channel | Type   | Register Cluster |
|---------|--------|------------------|
| TXD     | READER | TXD              |
| RXD     | WRITER | RXD              |

Table 144: SPIM EasyDMA Channels

For detailed information regarding the use of EasyDMA, see [EasyDMA](#) on page 140.

The .PTR and .MAXCNT registers are double-buffered. They can be updated and prepared for the next transmission immediately after having received the STARTED event.

The SPI master will automatically stop transmitting after TXD.MAXCNT bytes have been transmitted and RXD.MAXCNT bytes have been received. If RXD.MAXCNT is larger than TXD.MAXCNT, the remaining transmitted bytes will contain the value defined in the ORC register. If TXD.MAXCNT is larger than RXD.MAXCNT, the superfluous received bytes will be discarded.

The ENDRX/ENDTX event indicate that EasyDMA has finished accessing respectively the RX/TX buffer in RAM. The END event gets generated when both RX and TX are finished accessing the buffers in RAM.

If several AHB bus masters try to access the same AHB slave at the same time, AHB bus congestion might occur, and the behaviour of the EasyDMA channel will depend on the SPIM instance. Refer to [Table 145: Instances](#) on page 535 for information about what behaviour is supported in the various instances.

### 7.1.31.6 Low power

When putting the system in low power and the peripheral is not needed, lowest possible power consumption is achieved by stopping, and then disabling the peripheral.

The STOP task may not be always needed (the peripheral might already be stopped), but if it is sent, software shall wait until the STOPPED event was received as a response before disabling the peripheral through the ENABLE register.

## 7.1.31.7 Registers

| Base address             | Domain      | Peripheral | Instance   | Secure mapping | DMA security | Description               | Configuration                                                                                                                                                                                       |
|--------------------------|-------------|------------|------------|----------------|--------------|---------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x50008000<br>0x40008000 | APPLICATION | SPIM       | SPIM0 : S  | US             | SA           | SPI master 0              | Not supported: > 8 Mbps data rate, IFTIMING.x registers, hardware CSN control (PSEL.CSN), stalling mechanism during AHB bus contention                                                              |
|                          |             |            | SPIM0 : NS |                |              |                           |                                                                                                                                                                                                     |
| 0x50009000<br>0x40009000 | APPLICATION | SPIM       | SPIM1 : S  | US             | SA           | SPI master 1              | Not supported: > 8 Mbps data rate, IFTIMING.x registers, hardware CSN control (PSEL.CSN), stalling mechanism during AHB bus contention                                                              |
|                          |             |            | SPIM1 : NS |                |              |                           |                                                                                                                                                                                                     |
| 0x5000A000<br>0x4000A000 | APPLICATION | SPIM       | SPIM2 : S  | US             | SA           | SPI master 2 (high-speed) | Up to 32 Mbps SPI when using dedicated pins                                                                                                                                                         |
|                          |             |            | SPIM2 : NS |                |              |                           |                                                                                                                                                                                                     |
| 0x41013000               | NETWORK     | SPIM       | SPIM0      | NS             | NA           | SPI master 0              | > 8 Mbps data rate not supported<br><br>IFTIMING.x registers not implemented<br><br>Hardware CSN control (PSEL.CSN) not supported<br><br>Stalling mechanism during AHB bus contention not supported |

Table 145: Instances

| Register          | Offset | Security | Description                                              |
|-------------------|--------|----------|----------------------------------------------------------|
| TASKS_START       | 0x010  |          | Start SPI transaction                                    |
| TASKS_STOP        | 0x014  |          | Stop SPI transaction                                     |
| TASKS_SUSPEND     | 0x01C  |          | Suspend SPI transaction                                  |
| TASKS_RESUME      | 0x020  |          | Resume SPI transaction                                   |
| SUBSCRIBE_START   | 0x090  |          | Subscribe configuration for task <a href="#">START</a>   |
| SUBSCRIBE_STOP    | 0x094  |          | Subscribe configuration for task <a href="#">STOP</a>    |
| SUBSCRIBE_SUSPEND | 0x09C  |          | Subscribe configuration for task <a href="#">SUSPEND</a> |
| SUBSCRIBE_RESUME  | 0x0A0  |          | Subscribe configuration for task <a href="#">RESUME</a>  |
| EVENTS_STOPPED    | 0x104  |          | SPI transaction has stopped                              |
| EVENTS_ENDRX      | 0x110  |          | End of RXD buffer reached                                |
| EVENTS_END        | 0x118  |          | End of RXD buffer and TXD buffer reached                 |
| EVENTS_ENDTX      | 0x120  |          | End of TXD buffer reached                                |
| EVENTS_STARTED    | 0x14C  |          | Transaction started                                      |
| PUBLISH_STOPPED   | 0x184  |          | Publish configuration for event <a href="#">STOPPED</a>  |
| PUBLISH_ENDRX     | 0x190  |          | Publish configuration for event <a href="#">ENDRX</a>    |
| PUBLISH_END       | 0x198  |          | Publish configuration for event <a href="#">END</a>      |
| PUBLISH_ENDTX     | 0x1A0  |          | Publish configuration for event <a href="#">ENDTX</a>    |
| PUBLISH_STARTED   | 0x1CC  |          | Publish configuration for event <a href="#">STARTED</a>  |
| SHORTS            | 0x200  |          | Shortcuts between local events and tasks                 |
| INTENSET          | 0x304  |          | Enable interrupt                                         |
| INTENCLR          | 0x308  |          | Disable interrupt                                        |

| Register         | Offset | Security | Description                                                                                                                                                            |
|------------------|--------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| STALLSTAT        | 0x400  |          | Stall status for EasyDMA RAM accesses. The fields in this register is set to STALL by hardware whenever a stall occurs and can be cleared (set to NOSTALL) by the CPU. |
| ENABLE           | 0x500  |          | Enable SPIM                                                                                                                                                            |
| PSEL.SCK         | 0x508  |          | Pin select for SCK                                                                                                                                                     |
| PSEL.MOSI        | 0x50C  |          | Pin select for MOSI signal                                                                                                                                             |
| PSEL.MISO        | 0x510  |          | Pin select for MISO signal                                                                                                                                             |
| PSEL.CSN         | 0x514  |          | Pin select for CSN                                                                                                                                                     |
| FREQUENCY        | 0x524  |          | SPI frequency. Accuracy depends on the HFCLK source selected.                                                                                                          |
| RXD.PTR          | 0x534  |          | Data pointer                                                                                                                                                           |
| RXD.MAXCNT       | 0x538  |          | Maximum number of bytes in receive buffer                                                                                                                              |
| RXD.AMOUNT       | 0x53C  |          | Number of bytes transferred in the last transaction                                                                                                                    |
| RXD.LIST         | 0x540  |          | EasyDMA list type                                                                                                                                                      |
| TXD.PTR          | 0x544  |          | Data pointer                                                                                                                                                           |
| TXD.MAXCNT       | 0x548  |          | Number of bytes in transmit buffer                                                                                                                                     |
| TXD.AMOUNT       | 0x54C  |          | Number of bytes transferred in the last transaction                                                                                                                    |
| TXD.LIST         | 0x550  |          | EasyDMA list type                                                                                                                                                      |
| CONFIG           | 0x554  |          | Configuration register                                                                                                                                                 |
| IFTIMING.RXDELAY | 0x560  |          | Sample delay for input serial data on MISO                                                                                                                             |
| IFTIMING.CSNDUR  | 0x564  |          | Minimum duration between edge of CSN and edge of SCK and minimum duration CSN must stay high between transactions                                                      |
| CSNPOL           | 0x568  |          | Polarity of CSN output                                                                                                                                                 |
| PSELDCX          | 0x56C  |          | Pin select for DCX signal                                                                                                                                              |
| DCXCNT           | 0x570  |          | DCX configuration                                                                                                                                                      |
| ORC              | 0x5C0  |          | Byte transmitted after TXD.MAXCNT bytes have been transmitted in the case when RXD.MAXCNT is greater than TXD.MAXCNT                                                   |

Table 146: Register overview

### 7.1.31.7.1 TASKS\_START

Address offset: 0x010

Start SPI transaction

|                  |            |             |          |                                                                                       |  |  |  |                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|-------------|----------|---------------------------------------------------------------------------------------|--|--|--|-----------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |             |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |             |          | A                                                                                     |  |  |  |                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |             |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |  |  |  |                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field |             | Value ID | Value                                                                                 |  |  |  | Description           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W          | TASKS_START |          |                                                                                       |  |  |  | Start SPI transaction |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Trigger     |          | 1                                                                                     |  |  |  | Trigger task          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.31.7.2 TASKS\_STOP

Address offset: 0x014

Stop SPI transaction

| Bit number       |            | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|---------------------------------------------------------------------------------------|-------|----------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |            | A                                                                                     |       |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |       |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID                                                                              | Value | Description          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W          | TASKS_STOP                                                                            |       | Stop SPI transaction |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Trigger                                                                               | 1     | Trigger task         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.31.7.3 TASKS\_SUSPEND

Address offset: 0x01C

Suspend SPI transaction

| Bit number       |                 | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                         |
|------------------|-----------------|---------------------------------------------------------------------------------------|-------------------------|
| ID               |                 | A                                                                                     |                         |
| Reset 0x00000000 |                 | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                         |
| ID               | Acces Field     | Value ID                                                                              | Description             |
| A                | W TASKS_SUSPEND |                                                                                       | Suspend SPI transaction |
|                  |                 | Trigger                                                                               | 1 Trigger task          |

### 7.1.31.7.4 TASKS\_RESUME

Address offset: 0x020

Resume SPI transaction

| Bit number       |                | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                        |
|------------------|----------------|---------------------------------------------------------------------------------------|------------------------|
| ID               |                | A                                                                                     |                        |
| Reset 0x00000000 |                | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                        |
| ID               | Acces Field    | Value ID                                                                              | Description            |
| A                | W TASKS_RESUME |                                                                                       | Resume SPI transaction |
|                  |                | Trigger                                                                               | 1 Trigger task         |

### 7.1.31.7.5 SUBSCRIBE\_START

Address offset: 0x090

Subscribe configuration for task [START](#)

|                  |            |          |          |    |                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|----|--------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          | 31       | 30 | 29                                                     | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |          | B        |    |                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          | 0        | 0  | 0                                                      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce Field | Value ID | Value    |    | Description                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] |    | Channel that task <span>START</span> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |    |                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        |    | Disable subscription                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        |    | Enable subscription                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.31.7.6 SUBSCRIBE\_STOP

Address offset: 0x094

Subscribe configuration for task [STOP](#)

|                  |            |          |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          | B A A A A A A A                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Description                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Channel that task <span>STOP</span> will subscribe to |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW EN      |          |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Disable subscription                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Enable subscription                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.31.7.7 SUBSCRIBE\_SUSPEND

Address offset: 0x09C

Subscribe configuration for task **SUSPEND**

|                  |            |          |                                                                                       |                      |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|----------------------|----------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                      |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |          | B                                                                                     |                      |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                   |                      |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 |                      | Description                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                              |                      | Channel that task <b>SUSPEND</b> will subscribe to |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |                                                                                       |                      |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Disable subscription |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Enable subscription  |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

### 7.1.31.7.8 SUBSCRIBE\_RESUME

Address offset: 0x0A0

Subscribe configuration for task **RESUME**

|                  |            |          |          |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|----------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |          |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |          |          | B                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value    | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0] | Channel that task <b>RESUME</b> will subscribe to                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |          |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0        | Disable subscription                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1        | Enable subscription                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

### 7.1.31.7.9 EVENTS\_STOPPED

Address offset: 0x104

SPI transaction has stopped

|                  |                   |              |                                                                                       |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|-------------------|--------------|---------------------------------------------------------------------------------------|-----------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |                   |              | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |                   |              | A                                                                                     |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |                   |              | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field        | Value ID     | Value                                                                                 | Description                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW EVENTS_STOPPED |              |                                                                                       | SPI transaction has stopped |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                   | NotGenerated | 0                                                                                     | Event not generated         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                   | Generated    | 1                                                                                     | Event generated             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.31.7.10 EVENTS\_ENDRX

Address offset: 0x110

End of RXD buffer reached

|                  |            |              |       |                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------------|-------|---------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |              |       | 31                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |              |       |                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |
| Reset 0x00000000 |            |              |       | 0                         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID     | Value | Description               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | EVENTS_ENDRX |       | End of RXD buffer reached |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | NotGenerated | 0     | Event not generated       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Generated    | 1     | Event generated           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.31.7.11 EVENTS\_END

Address offset: 0x118

End of RXD buffer and TXD buffer reached

|                  |            |              |       |                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------------|-------|------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |              |       | 31                                       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |              |       |                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |
| Reset 0x00000000 |            |              |       | 0                                        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |
| ID               | Acce Field | Value ID     | Value | Description                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | EVENTS_END   |       | End of RXD buffer and TXD buffer reached |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | NotGenerated | 0     | Event not generated                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Generated    | 1     | Event generated                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.31.7.12 EVENTS\_ENDTX

Address offset: 0x120

End of TXD buffer reached

|                  |            |              |       |                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------------|-------|---------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |              |       | 31                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |              |       |                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |
| Reset 0x00000000 |            |              |       | 0                         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |
| ID               | Acce Field | Value ID     | Value | Description               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | EVENTS_ENDTX |       | End of TXD buffer reached |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | NotGenerated | 0     | Event not generated       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Generated    | 1     | Event generated           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.31.7.13 EVENTS\_STARTED

Address offset: 0x14C

Transaction started

|                  |            |                |       |                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|------------------|------------|----------------|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|---|
| Bit number       |            |                |       | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |   |
| ID               |            |                |       |                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  | A |
| Reset 0x00000000 |            |                |       | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |   |
| ID               | Acce Field | Value ID       | Value | Description         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
| A                | RW         | EVENTS_STARTED |       | Transaction started |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|                  |            | NotGenerated   | 0     | Event not generated |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|                  |            | Generated      | 1     | Event generated     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |

### 7.1.31.7.14 PUBLISH\_STOPPED

Address offset: 0x184

Publish configuration for event STOPPED

|                  |            |          |          |                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|---------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                                          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |          |          | B                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |          | 0                                           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce Field | Value ID | Value    | Description                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] | Channel that event STOPPED will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        | Disable publishing                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        | Enable publishing                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.31.7.15 PUBLISH\_ENDRX

Address offset: 0x190

Publish configuration for event **ENDRX**

|                  |            |          |          |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|--------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                                               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |          |          | B                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |          | 0                                                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce Field | Value ID | Value    | Description                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] | Channel that event <b>ENDRX</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        | Disable publishing                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        | Enable publishing                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.31.7.16 PUBLISH\_END

Address offset: 0x198

Publish configuration for event **END**

|                  |            |  |          |                                                                         |                    |                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|-------------------------------------------------------------------------|--------------------|------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31                                                                      | 30                 | 29                                             | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |  |          | B                                                                       |                    |                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |                    |                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field |  | Value ID | Value                                                                   |                    | Description                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          | [255..0]                                                                |                    | Channel that event <b>END</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |                                                                         |                    |                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled | 0                                                                       | Disable publishing |                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  | 1                                                                       | Enable publishing  |                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.31.7.17 PUBLISH\_ENDTX

Address offset: 0x1A0

Publish configuration for event **ENDTX**

|                  |            |  |  |          |    |          |    |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|--|----------|----|----------|----|--------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |  | 31       | 30 | 29       | 28 | 27                                               | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |  |  | B        |    |          |    |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |  | 0        |    |          |    |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  |  | Value ID |    | Value    |    | Description                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |  |          |    | [255..0] |    | Channel that event <b>ENDTX</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |  |          |    |          |    |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  |  | Disabled |    | 0        |    | Disable publishing                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  |  | Enabled  |    | 1        |    | Enable publishing                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |



### 7.1.31.7.18 PUBLISH\_STARTED

Address offset: 0x1CC

Publish configuration for event [STARTED](#)

|                  |            |          |                                                                                       |                    |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|--------------------|----------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                    |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |          | B                                                                                     |                    |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                   |                    |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 |                    | Description                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                              |                    | Channel that event <b>STARTED</b> will publish to. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |                                                                                       |                    |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Disable publishing |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Enable publishing  |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

### 7.1.31.7.19 SHORTS

Address offset: 0x200

Shortcuts between local events and tasks

|                  |              |          |                                                                                       |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|--------------|----------|---------------------------------------------------------------------------------------|---------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |              |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |              |          | A                                                                                     |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |              |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acces Field  | Value ID | Value                                                                                 | Description                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW END_START |          |                                                                                       | Shortcut between event <span>END</span> and task <span>START</span> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Disabled | 0                                                                                     | Disable shortcut                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Enabled  | 1                                                                                     | Enable shortcut                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.31.7.20 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |   |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|-------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|---|--|---|--|---|--|--|--|--|--|--|--|
| ID               |            |          | E                                                                                     |                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  | D |  |  |  | C |  | B |  | A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |   |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |   |  |  |  |  |  |  |  |
| A                | RW STOPPED |          |                                                                                       | Write '1' to enable interrupt for event STOPPED |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |   |  |  |  |  |  |  |  |
|                  |            | Set      | 1                                                                                     | Enable                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |   |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Read: Disabled                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |   |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Read: Enabled                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |   |  |  |  |  |  |  |  |
| B                | RW ENDRX   |          |                                                                                       | Write '1' to enable interrupt for event ENDRX   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |   |  |  |  |  |  |  |  |
|                  |            | Set      | 1                                                                                     | Enable                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |   |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Read: Disabled                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |   |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Read: Enabled                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |   |  |  |  |  |  |  |  |
| C                | RW END     |          |                                                                                       | Write '1' to enable interrupt for event END     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |   |  |  |  |  |  |  |  |
|                  |            | Set      | 1                                                                                     | Enable                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |   |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Read: Disabled                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |   |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Read: Enabled                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |   |  |  |  |  |  |  |  |
| D                | RW ENDTX   |          |                                                                                       | Write '1' to enable interrupt for event ENDTX   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |   |  |  |  |  |  |  |  |
|                  |            | Set      | 1                                                                                     | Enable                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |   |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Read: Disabled                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |   |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Read: Enabled                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |   |  |  |  |  |  |  |  |

|                  |            |          |       |                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|-------|-----------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |       | 31                                                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |          |       | E                                                               |    |    |    |    |    |    |    |    |    |    |    | D  |    |    |    | C  |    | B  |    | A  |    |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |          |       | 0                                                               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID | Value | Description                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| E                | RW         | STARTED  |       | Write '1' to enable interrupt for event <a href="#">STARTED</a> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Set      | 1     | Enable                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0     | Read: Disabled                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1     | Read: Enabled                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.31.7.21 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number       |      |         |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |   |  |  |  |   |  |  |  |  |  |  |  |
|------------------|------|---------|----------|---------------------------------------------------------------------------------------|------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|---|---|--|--|--|---|--|--|--|--|--|--|--|
| ID               |      |         |          | E                                                                                     |                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | D |  |  |  | C | B |  |  |  | A |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |         |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |   |  |  |  |   |  |  |  |  |  |  |  |
| ID               | Acce | Field   | Value ID | Value                                                                                 | Description                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |   |  |  |  |   |  |  |  |  |  |  |  |
| A                | RW   | STOPPED |          |                                                                                       | Write '1' to disable interrupt for event <a href="#">STOPPED</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |   |  |  |  |   |  |  |  |  |  |  |  |
|                  |      |         | Clear    | 1                                                                                     | Disable                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |   |  |  |  |   |  |  |  |  |  |  |  |
|                  |      |         | Disabled | 0                                                                                     | Read: Disabled                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |   |  |  |  |   |  |  |  |  |  |  |  |
|                  |      |         | Enabled  | 1                                                                                     | Read: Enabled                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |   |  |  |  |   |  |  |  |  |  |  |  |
| B                | RW   | ENDRX   |          |                                                                                       | Write '1' to disable interrupt for event <a href="#">ENDRX</a>   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |   |  |  |  |   |  |  |  |  |  |  |  |
|                  |      |         | Clear    | 1                                                                                     | Disable                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |   |  |  |  |   |  |  |  |  |  |  |  |
|                  |      |         | Disabled | 0                                                                                     | Read: Disabled                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |   |  |  |  |   |  |  |  |  |  |  |  |
|                  |      |         | Enabled  | 1                                                                                     | Read: Enabled                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |   |  |  |  |   |  |  |  |  |  |  |  |
| C                | RW   | END     |          |                                                                                       | Write '1' to disable interrupt for event <a href="#">END</a>     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |   |  |  |  |   |  |  |  |  |  |  |  |
|                  |      |         | Clear    | 1                                                                                     | Disable                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |   |  |  |  |   |  |  |  |  |  |  |  |
|                  |      |         | Disabled | 0                                                                                     | Read: Disabled                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |   |  |  |  |   |  |  |  |  |  |  |  |
|                  |      |         | Enabled  | 1                                                                                     | Read: Enabled                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |   |  |  |  |   |  |  |  |  |  |  |  |
| D                | RW   | ENDTX   |          |                                                                                       | Write '1' to disable interrupt for event <a href="#">ENDTX</a>   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |   |  |  |  |   |  |  |  |  |  |  |  |
|                  |      |         | Clear    | 1                                                                                     | Disable                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |   |  |  |  |   |  |  |  |  |  |  |  |
|                  |      |         | Disabled | 0                                                                                     | Read: Disabled                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |   |  |  |  |   |  |  |  |  |  |  |  |
|                  |      |         | Enabled  | 1                                                                                     | Read: Enabled                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |   |  |  |  |   |  |  |  |  |  |  |  |
| E                | RW   | STARTED |          |                                                                                       | Write '1' to disable interrupt for event <a href="#">STARTED</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |   |  |  |  |   |  |  |  |  |  |  |  |
|                  |      |         | Clear    | 1                                                                                     | Disable                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |   |  |  |  |   |  |  |  |  |  |  |  |
|                  |      |         | Disabled | 0                                                                                     | Read: Disabled                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |   |  |  |  |   |  |  |  |  |  |  |  |
|                  |      |         | Enabled  | 1                                                                                     | Read: Enabled                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |   |  |  |  |   |  |  |  |  |  |  |  |

### 7.1.31.7.22 STALLSTAT

Address offset: 0x400

Stall status for EasyDMA RAM accesses. The fields in this register is set to STALL by hardware whenever a stall occurs and can be cleared (set to NOSTALL) by the CPU.

|                  |            |          |        |    |                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|--------|----|-------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          | 31     | 30 | 29                                  | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |          |        |    |                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |          | 0      | 0  | 0                                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID | Value  |    | Description                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW TX      |          | [1..0] |    | Stall status for EasyDMA RAM reads  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | NOSTALL  | 0      |    | No stall                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | STALL    | 1      |    | A stall has occurred                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| B                | RW RX      |          | [1..0] |    | Stall status for EasyDMA RAM writes |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | NOSTALL  | 0      |    | No stall                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | STALL    | 1      |    | A stall has occurred                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.31.7.23 ENABLE

Address offset: 0x500

## Enable SPIM

|                  |            |  |  |          |  |  |       |  |  |                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|--|----------|--|--|-------|--|--|------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |  |          |  |  |       |  |  | 31                     | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |  |  |          |  |  |       |  |  |                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |  |          |  |  |       |  |  | 0                      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  |  | Value ID |  |  | Value |  |  | Description            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW ENABLE  |  |  |          |  |  |       |  |  | Enable or disable SPIM |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  |  | Disabled |  |  | 0     |  |  | Disable SPIM           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  |  | Enabled  |  |  | 7     |  |  | Enable SPIM            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.31.7.24 PSEL.SCK

Address offset: 0x508

## Pin select for SCK

|                  |            |  |              |         |  |             |  |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|--------------|---------|--|-------------|--|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |              |         |  |             |  |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |  |              |         |  |             |  |  |  | C  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | B  |    |   |   |   |   |   |   |   |   | A | A | A | A | A |
| Reset 0xFFFFFFFF |            |  |              |         |  |             |  |  |  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ID               | Acce Field |  | Value ID     | Value   |  | Description |  |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW PIN     |  |              | [0..31] |  | Pin number  |  |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW PORT    |  |              | [0..1]  |  | Port number |  |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| C                | RW CONNECT |  |              |         |  | Connection  |  |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disconnected | 1       |  | Disconnect  |  |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Connected    | 0       |  | Connect     |  |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.31.7.25 PSEL.MOSI

Address offset: 0x50C

### Pin select for MOSI signal

|                  |            |              |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |             |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |              | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15          | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |              | C       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |             |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Reset 0xFFFFFFFF |            |              | 1       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |             |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field | Value ID     | Value   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | Description |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW PIN     |              | [0..31] |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | Pin number  |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| B                | RW PORT    |              | [0..1]  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | Port number |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| C                | RW CONNECT |              |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | Connection  |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disconnected | 1       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | Disconnect  |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Connected    | 0       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | Connect     |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 7.1.31.7.26 PSEL.MISO

Address offset: 0x510

### Pin select for MISO signal

|                  |            |              |                                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |             |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------------|-----------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |              | 31                                                                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15          | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |              | C                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |             |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Reset 0xFFFFFFFF |            |              | 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |             |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field | Value ID     | Value                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | Description |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW PIN     |              | [0..31]                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | Pin number  |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| B                | RW PORT    |              | [0..1]                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | Port number |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| C                | RW CONNECT |              |                                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | Connection  |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disconnected | 1                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | Disconnect  |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Connected    | 0                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | Connect     |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.31.7.27 PSEL.CSN

Address offset: 0x514

### Pin select for CSN

|                  |            |              |         |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------------|---------|----|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |              | 31      | 30 | 29          | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |              | C       |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Reset 0xFFFFFFFF |            |              | 1       |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field | Value ID     | Value   |    | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW PIN     |              | [0..31] |    | Pin number  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| B                | RW PORT    |              | [0..1]  |    | Port number |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| C                | RW CONNECT |              |         |    | Connection  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disconnected | 1       |    | Disconnect  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Connected    | 0       |    | Connect     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.31.7.28 FREQUENCY

Address offset: 0x524

SPI frequency. Accuracy depends on the HFCLK source selected.

|                  |            |           |          |      |       |            |             |                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-----------|----------|------|-------|------------|-------------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |           |          |      |       |            |             |                      | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |           |          |      |       |            |             |                      | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |   |
| Reset 0x04000000 |            |           |          |      |       |            |             |                      | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |           | Value ID |      | Value |            | Description |                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | FREQUENCY |          | K125 |       | 0x02000000 |             | SPI master data rate |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |           |          | K250 |       | 0x04000000 |             | 250 kbps             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |           |          | K500 |       | 0x08000000 |             | 500 kbps             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |           |          | M1   |       | 0x10000000 |             | 1 Mbps               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |           |          | M2   |       | 0x20000000 |             | 2 Mbps               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |           |          | M4   |       | 0x40000000 |             | 4 Mbps               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |           |          | M8   |       | 0x80000000 |             | 8 Mbps               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |           |          | M16  |       | 0x0A000000 |             | 16 Mbps              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |           |          | M32  |       | 0x14000000 |             | 32 Mbps              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.31.7.29 RXD.PTR

Address offset: 0x534

Data pointer

|            |  |  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| Bit number |  |  | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        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**Note:** See the memory chapter for details about which memories are available for EasyDMA.

### 7.1.31.7.30 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in receive buffer

|                  |      |        |       |    |             |                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
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| Bit number       |      |        |       | 31 | 30          | 29                                        | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |      |        |       |    |             |                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |      |        |       | 0  | 0           | 0                                         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
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| A                | RW   | MAXCNT |       |    | [1..0xffff] | Maximum number of bytes in receive buffer |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.31.7.31 RXD.AMOUNT

Address offset: 0x53C

Number of bytes transferred in the last transaction

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### 7.1.31.7.32 RXD.LIST

Address offset: 0x540

EasyDMA list type

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A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**Note:** See the memory chapter for details about which memories are available for EasyDMA.

### 7.1.31.7.34 TXD.MAXCNT

Address offset: 0x548

Number of bytes in transmit buffer

|                  |            |        |          |                                                                                       |                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|--------|----------|---------------------------------------------------------------------------------------|--------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |        |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |        |          |                                                                                       |                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |        |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field |        | Value ID | Value                                                                                 | Description                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | MAXCNT |          | [1..0xffff]                                                                           | Maximum number of bytes in transmit buffer |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.31.7.35 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transferred in the last transaction

|                  |      |        |          |                                                                                       |                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|--------|----------|---------------------------------------------------------------------------------------|-----------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |        |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |        |          |                                                                                       |                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |        |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field  | Value ID | Value                                                                                 | Description                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | R    | AMOUNT |          | [1..0xffff]                                                                           | Number of bytes transferred in the last transaction |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.31.7.36 TXD.LIST

Address offset: 0x550

EasyDMA list type

|                  |      |       |           |                                                                                       |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|-------|-----------|---------------------------------------------------------------------------------------|----------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |       |           | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |       |           | A A                                                                                   |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |       |           | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field | Value ID  | Value                                                                                 | Description          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW   | LIST  |           |                                                                                       | List type            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Disabled  | 0                                                                                     | Disable EasyDMA list |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | ArrayList | 1                                                                                     | Use array list       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.31.7.37 CONFIG

Address offset: 0x554

Configuration register

|                  |            |            |                                                                                       |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|------------|---------------------------------------------------------------------------------------|---------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |            | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |            | C B A                                                                                 |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |            | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID   | Value                                                                                 | Description                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW ORDER   |            |                                                                                       | Bit order                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | MsbFirst   | 0                                                                                     | Most significant bit shifted out first                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | LsbFirst   | 1                                                                                     | Least significant bit shifted out first                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW CPHA    |            |                                                                                       | Serial clock (SCK) phase                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Leading    | 0                                                                                     | Sample on leading edge of clock, shift serial data on trailing edge |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Trailing   | 1                                                                                     | Sample on trailing edge of clock, shift serial data on leading edge |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW CPOL    |            |                                                                                       | Serial clock (SCK) polarity                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | ActiveHigh | 0                                                                                     | Active high                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | ActiveLow  | 1                                                                                     | Active low                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.31.7.38 IFTIMING.RXDELAY

Address offset: 0x560

Sample delay for input serial data on MISO

|                  |            |          |                                                                                       |                                                                                                                                                                                                                                                                                                                                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                                                                                                                                                                                                                                                                                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          | A A A                                                                                 |                                                                                                                                                                                                                                                                                                                                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000002 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0             |                                                                                                                                                                                                                                                                                                                                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                                                                                                                                                                                                                                                                                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW RXDELAY |          | [7..0]                                                                                | Sample delay for input serial data on MISO. The value specifies the number of 64 MHz clock cycles (15.625 ns) delay from the the sampling edge of SCK (leading edge for CONFIG.CPHA = 0, trailing edge for CONFIG.CPHA = 1) until the input serial data is sampled. As an example, if RXDELAY = 0 and CONFIG.CPHA = 0, the input serial data is sampled on the rising edge of SCK. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |





|                  |      |        |          |          |    |                                                                                                                                                                                                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------|--------|----------|----------|----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |      |        |          | 31       | 30 | 29                                                                                                                                                                                                                                                 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |
| ID               |      |        |          |          |    |                                                                                                                                                                                                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A | A | A | A |
| Reset 0x00000000 |      |        |          | 0        | 0  | 0                                                                                                                                                                                                                                                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |   |
| ID               | Acce | Field  | Value ID | Value    |    | Description                                                                                                                                                                                                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW   | DCXCNT |          | 0x0..0xF |    | This register specifies the number of command bytes preceding the data bytes. The PSEL.DCX line will be low during transmission of command bytes and high during transmission of data bytes. Value 0xF indicates that all bytes are command bytes. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.31.7.43 ORC

Address offset: 0x5C0

Byte transmitted after TXD.MAXCNT bytes have been transmitted in the case when RXD.MAXCNT is greater than TXD.MAXCNT

|                  |            |          |                                                                                       |                                                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          | A A A A A A A A                                                                       |                                                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW ORC     |          |                                                                                       | Byte transmitted after TXD.MAXCNT bytes have been transmitted in the case when RXD.MAXCNT is greater than TXD.MAXCNT. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

## 7.1.31.8 Electrical specification

### 7.1.31.8.1 Timing specifications

| Symbol                    | Description                                    | Min. | Typ. | Max. | Units |
|---------------------------|------------------------------------------------|------|------|------|-------|
| f <sub>SPIM</sub>         | Bit rates for SPIM <sup>22</sup>               | ..   | ..   | ..   | Mbps  |
| t <sub>SPIM,START</sub>   | Time from START task to transmission started   | ..   | ..   | ..   | μs    |
| t <sub>SPIM,CCLK</sub>    | SCK period                                     | ..   | ..   | ..   | ns    |
| t <sub>SPIM,RSCK,LD</sub> | SCK rise time, standard drive <sup>23</sup>    | ..   | ..   | ..   |       |
| t <sub>SPIM,RSCK,HD</sub> | SCK rise time, high drive <sup>23</sup>        | ..   | ..   | ..   |       |
| t <sub>SPIM,FSCK,LD</sub> | SCK fall time, standard drive <sup>23</sup>    | ..   | ..   | ..   |       |
| t <sub>SPIM,FSCK,HD</sub> | SCK fall time, high drive <sup>23</sup>        | ..   | ..   | ..   |       |
| t <sub>SPIM,WHCK</sub>    | SCK high time <sup>23</sup>                    | ..   | ..   | ..   |       |
| t <sub>SPIM,WLCK</sub>    | SCK low time <sup>23</sup>                     | ..   | ..   | ..   |       |
| t <sub>SPIM,SUMI</sub>    | MISO to CLK edge setup time                    | ..   | ..   | ..   | ns    |
| t <sub>SPIM,HMI</sub>     | CLK edge to MISO hold time                     | ..   | ..   | ..   | ns    |
| t <sub>SPIM,VMO</sub>     | CLK edge to MOSI valid, SCK frequency <= 8 MHz | ..   | ..   | ..   | ns    |
| t <sub>SPIM,VMO,HS</sub>  | CLK edge to MOSI valid, SCK frequency > 8 MHz  | ..   | ..   | ..   | ns    |
| t <sub>SPIM,HMO</sub>     | MOSI hold time after CLK edge                  | ..   | ..   | ..   | ns    |

<sup>22</sup> High bit rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.

<sup>23</sup> At 25pF load, including GPIO pin capacitance, see GPIO spec.

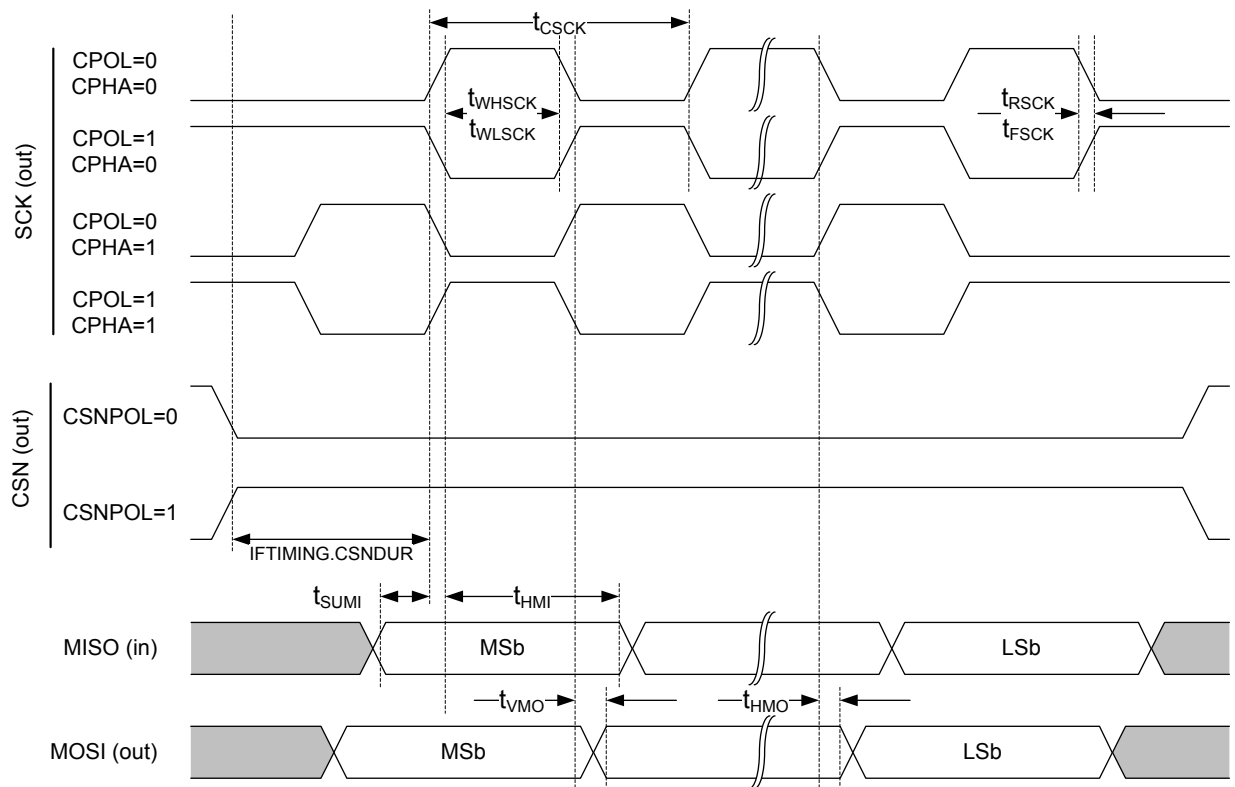


Figure 193: SPIM timing diagram

### 7.1.32 SPIS — Serial peripheral interface slave with EasyDMA

SPI slave (SPIS) is implemented with EasyDMA support for ultra low power serial communication from an external SPI master. EasyDMA in conjunction with hardware-based semaphore mechanisms removes all real-time requirements associated with controlling the SPI slave from a low priority CPU execution context.

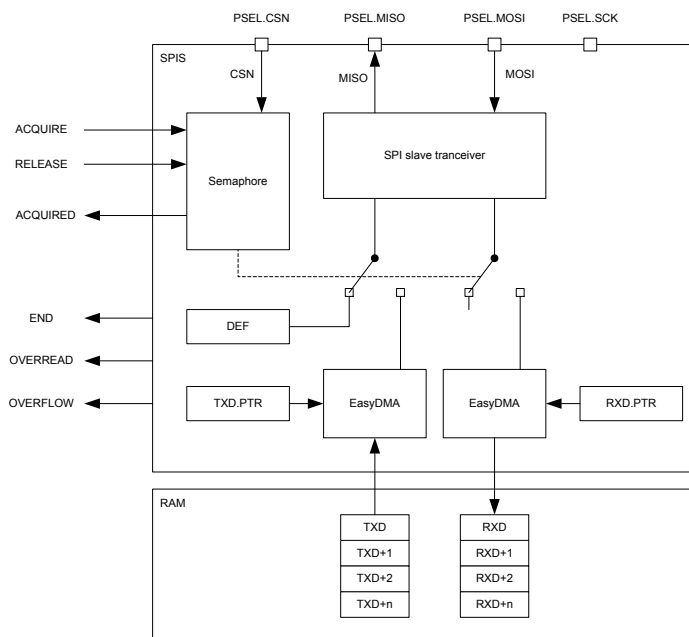


Figure 194: SPI slave

The SPIS supports SPI modes 0 through 3. The CONFIG register allows setting CPOL and CPHA appropriately.

| Mode      | Clock polarity  | Clock phase       |
|-----------|-----------------|-------------------|
|           | CPOL            | CPHA              |
| SPI_MODE0 | 0 (Active High) | 0 (Trailing Edge) |
| SPI_MODE1 | 0 (Active High) | 1 (Leading Edge)  |
| SPI_MODE2 | 1 (Active Low)  | 0 (Trailing Edge) |
| SPI_MODE3 | 1 (Active Low)  | 1 (Leading Edge)  |

Table 147: SPI modes

### 7.1.32.1 Shared resources

The SPI slave shares registers and other resources with other peripherals that have the same ID as the SPI slave. Therefore, you must disable all peripherals that have the same ID as the SPI slave before the SPI slave can be configured and used.

Disabling a peripheral that has the same ID as the SPI slave will not reset any of the registers that are shared with the SPI slave. It is important to configure all relevant SPI slave registers explicitly to secure that it operates correctly.

The Instantiation table in [Instantiation](#) on page 136 shows which peripherals have the same ID as the SPI slave.

### 7.1.32.2 EasyDMA

The SPIS implements EasyDMA for accessing RAM without CPU involvement.

The SPIS peripheral implements the following EasyDMA channels:

| Channel | Type   | Register Cluster |
|---------|--------|------------------|
| TXD     | READER | TXD              |
| RXD     | WRITER | RXD              |

Table 148: SPIS EasyDMA Channels

For detailed information regarding the use of EasyDMA, see [EasyDMA](#) on page 140.

If RXD.MAXCNT is larger than TXD.MAXCNT, the remaining transmitted bytes will contain the value defined in the ORC register.

The END event indicates that EasyDMA has finished accessing the buffer in RAM.

### 7.1.32.3 SPI slave operation

SPI slave uses two memory pointers, RXD.PTR and TXD.PTR, that point to the RXD buffer (receive buffer) and TXD buffer (transmit buffer) respectively. Since these buffers are located in RAM, which can be accessed by both the SPI slave and the CPU, a hardware based semaphore mechanism is implemented to enable safe sharing.

See [Figure 195: SPI transaction when shortcut between END and ACQUIRE is enabled](#) on page 553.

Before the CPU can safely update the RXD.PTR and TXD.PTR pointers it must first acquire the SPI semaphore. The CPU can acquire the semaphore by triggering the ACQUIRE task and then receiving the ACQUIRED event. When the CPU has updated the RXD.PTR and TXD.PTR pointers the CPU must release the semaphore before the SPI slave will be able to acquire it. The CPU releases the semaphore by triggering

the RELEASE task. This is illustrated in [Figure 195: SPI transaction when shortcut between END and ACQUIRE is enabled](#) on page 553. Triggering the RELEASE task when the semaphore is not granted to the CPU will have no effect.

The semaphore mechanism does not, at any time, prevent the CPU from performing read or write access to the RXD.PTR register, the TXD.PTR registers, or the RAM that these pointers are pointing to. The semaphore is only telling when these can be updated by the CPU so that safe sharing is achieved.

The semaphore is by default assigned to the CPU after the SPI slave is enabled. No ACQUIRED event will be generated for this initial semaphore handover. An ACQUIRED event will be generated immediately if the ACQUIRE task is triggered while the semaphore is assigned to the CPU.

The SPI slave will try to acquire the semaphore when CSN goes low. If the SPI slave does not manage to acquire the semaphore at this point, the transaction will be ignored. This means that all incoming data on MOSI will be discarded, and the DEF (default) character will be clocked out on the MISO line throughout the whole transaction. This will also be the case even if the semaphore is released by the CPU during the transaction. In case of a race condition where the CPU and the SPI slave try to acquire the semaphore at the same time, as illustrated in lifeline item 2 in [Figure 195: SPI transaction when shortcut between END and ACQUIRE is enabled](#) on page 553, the semaphore will be granted to the CPU.

If the SPI slave acquires the semaphore, the transaction will be granted. The incoming data on MOSI will be stored in the RXD buffer and the data in the TXD buffer will be clocked out on MISO.

When a granted transaction is completed and CSN goes high, the SPI slave will automatically release the semaphore and generate the END event.

As long as the semaphore is available the SPI slave can be granted multiple transactions one after the other. If the CPU is not able to reconfigure the TXD.PTR and RXD.PTR between granted transactions, the same TX data will be clocked out and the RX buffers will be overwritten. To prevent this from happening, the END\_ACQUIRE shortcut can be used. With this shortcut enabled the semaphore will be handed over to the CPU automatically after the granted transaction has completed, giving the CPU the ability to update the TXPTR and RXPTR between every granted transaction.

If the CPU tries to acquire the semaphore while it is assigned to the SPI slave, an immediate handover will not be granted. However, the semaphore will be handed over to the CPU as soon as the SPI slave has released the semaphore after the granted transaction is completed. If the END\_ACQUIRE shortcut is enabled and the CPU has triggered the ACQUIRE task during a granted transaction, only one ACQUIRE request will be served following the END event.

The MAXRX register specifies the maximum number of bytes the SPI slave can receive in one granted transaction. If the SPI slave receives more than MAXRX number of bytes, an OVERFLOW will be indicated in the STATUS register and the incoming bytes will be discarded.

The MAXTX parameter specifies the maximum number of bytes the SPI slave can transmit in one granted transaction. If the SPI slave is forced to transmit more than MAXTX number of bytes, an OVERREAD will be indicated in the STATUS register and the ORC character will be clocked out.

The RXD.AMOUNT and TXD.AMOUNT registers are updated when a granted transaction is completed. The TXD.AMOUNT register indicates how many bytes were read from the TX buffer in the last transaction, that is, ORC (over-read) characters are not included in this number. Similarly, the RXD.AMOUNT register indicates how many bytes were written into the RX buffer in the last transaction.

The ENDRX event is generated when the RX buffer has been filled.

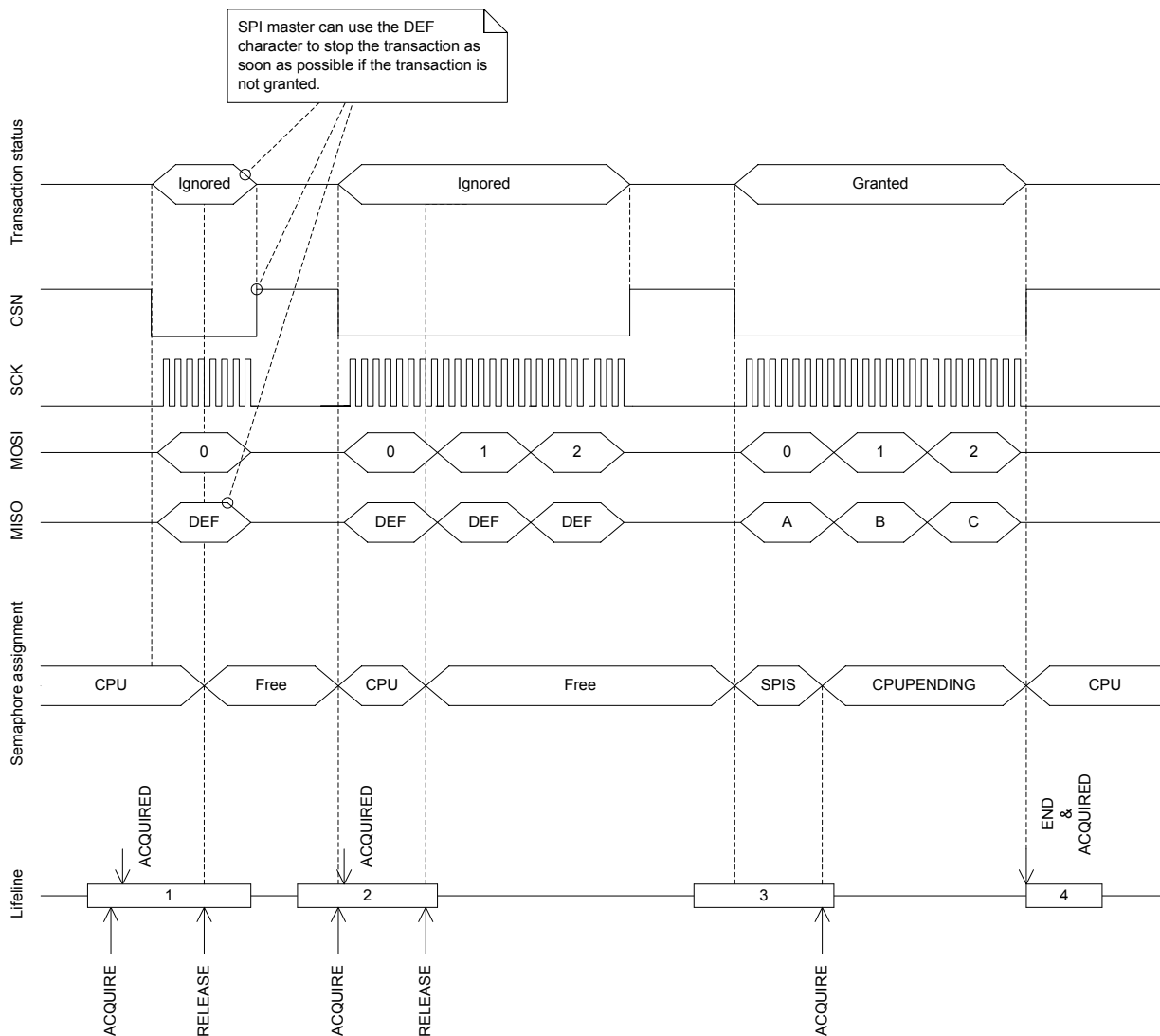


Figure 195: SPI transaction when shortcut between END and ACQUIRE is enabled

#### 7.1.32.4 Pin configuration

The CSN, SCK, MOSI, and MISO signals associated with the SPI slave are mapped to physical pins according to the configuration specified in the PSEL.CSN, PSEL.SCK, PSEL.MOSI, and PSEL.MISO registers respectively. If the CONNECT field of any of these registers is set to Disconnected, the associated SPI slave signal will not be connected to any physical pins.

The PSEL.CSN, PSEL.SCK, PSEL.MOSI, and PSEL.MISO registers and their configurations are only used as long as the SPI slave is enabled, and retained only as long as the device is in System ON mode, see [POWER — Power control](#) on page 36 chapter for more information about power modes. When the peripheral is disabled, the pins will behave as regular GPIOs, and use the configuration in their respective OUT bit field and PIN\_CNF[n] register. PSEL.CSN, PSEL.SCK, PSEL.MOSI, and PSEL.MISO must only be configured when the SPI slave is disabled.

To secure correct behavior in the SPI slave, the pins used by the SPI slave must be configured in the GPIO peripheral as described in [Table 149: GPIO configuration before enabling peripheral](#) on page 554 before enabling the SPI slave. This is to secure that the pins used by the SPI slave are driven correctly if the SPI slave itself is temporarily disabled, or if the device temporarily enters System OFF. This configuration must be retained in the GPIO for the selected I/Os as long as the SPI slave is to be recognized by an external SPI master.

The MISO line is set in high impedance as long as the SPI slave is not selected with CSN.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

| SPI signal | SPI pin                   | Direction | Output value   | Comment                                      |
|------------|---------------------------|-----------|----------------|----------------------------------------------|
| CSN        | As specified in PSEL.CSN  | Input     | Not applicable |                                              |
| SCK        | As specified in PSEL.SCK  | Input     | Not applicable |                                              |
| MOSI       | As specified in PSEL.MOSI | Input     | Not applicable |                                              |
| MISO       | As specified in PSEL.MISO | Input     | Not applicable | Emulates that the SPI slave is not selected. |

Table 149: GPIO configuration before enabling peripheral

## 7.1.32.5 Registers

| Base address | Domain      | Peripheral | Instance   | Secure mapping | DMA security | Description | Configuration |
|--------------|-------------|------------|------------|----------------|--------------|-------------|---------------|
| 0x50008000   | APPLICATION | SPIS       | SPIS0 : S  | US             | SA           | SPI slave 0 |               |
| 0x40008000   |             |            | SPIS0 : NS |                |              |             |               |
| 0x50009000   | APPLICATION | SPIS       | SPIS1 : S  | US             | SA           | SPI slave 1 |               |
| 0x40009000   |             |            | SPIS1 : NS |                |              |             |               |
| 0x41013000   | NETWORK     | SPIS       | SPIS0      | NS             | NA           | SPI slave 0 |               |

Table 150: Instances

| Register          | Offset | Security | Description                                                 |
|-------------------|--------|----------|-------------------------------------------------------------|
| TASKS_ACQUIRE     | 0x024  |          | Acquire SPI semaphore                                       |
| TASKS_RELEASE     | 0x028  |          | Release SPI semaphore, enabling the SPI slave to acquire it |
| SUBSCRIBE_ACQUIRE | 0x0A4  |          | Subscribe configuration for task <a href="#">ACQUIRE</a>    |
| SUBSCRIBE_RELEASE | 0x0A8  |          | Subscribe configuration for task <a href="#">RELEASE</a>    |
| EVENTS_END        | 0x104  |          | Granted transaction completed                               |
| EVENTS_ENDRX      | 0x110  |          | End of RXD buffer reached                                   |
| EVENTS_ACQUIRED   | 0x128  |          | Semaphore acquired                                          |
| PUBLISH_END       | 0x184  |          | Publish configuration for event <a href="#">END</a>         |
| PUBLISH_ENDRX     | 0x190  |          | Publish configuration for event <a href="#">ENDRX</a>       |
| PUBLISH_ACQUIRED  | 0x1A8  |          | Publish configuration for event <a href="#">ACQUIRED</a>    |
| SHORTS            | 0x200  |          | Shortcuts between local events and tasks                    |
| INTENSET          | 0x304  |          | Enable interrupt                                            |
| INTENCLR          | 0x308  |          | Disable interrupt                                           |
| SEMSTAT           | 0x400  |          | Semaphore status register                                   |
| STATUS            | 0x440  |          | Status from last transaction                                |
| ENABLE            | 0x500  |          | Enable SPI slave                                            |
| PSEL.SCK          | 0x508  |          | Pin select for SCK                                          |
| PSEL.MISO         | 0x50C  |          | Pin select for MISO signal                                  |
| PSEL.MOSI         | 0x510  |          | Pin select for MOSI signal                                  |
| PSEL.CSN          | 0x514  |          | Pin select for CSN signal                                   |
| PSELSCK           | 0x508  |          | Pin select for SCK                                          |
| PSELMISO          | 0x50C  |          | Pin select for MISO                                         |
| PSELMOSI          | 0x510  |          | Pin select for MOSI                                         |
| PSELCSN           | 0x514  |          | Pin select for CSN                                          |
| RXDPTR            | 0x534  |          | RXD data pointer                                            |
| MAXRX             | 0x538  |          | Maximum number of bytes in receive buffer                   |
| AMOUNTRX          | 0x53C  |          | Number of bytes received in last granted transaction        |
| RXD.PTR           | 0x534  |          | RXD data pointer                                            |
| RXD.MAXCNT        | 0x538  |          | Maximum number of bytes in receive buffer                   |
| RXD.AMOUNT        | 0x53C  |          | Number of bytes received in last granted transaction        |

### 7.1.32.5.1 TASKS\_ACQUIRE

## Acquire SPI semaphore

### 7.1.32.5.2 TASKS\_RELEASE

Release SPI semaphore, enabling the SPI slave to acquire it

### 7.1.32.5.3 SUBSCRIBE\_ACQUIRE

## Subscribe configuration for task ACQUIRE



**NORDIC**  
SEMICONDUCTOR

### 7.1.32.5.4 SUBSCRIBE\_RELEASE

Address offset: 0x0A8

Subscribe configuration for task **RELEASE**

|                  |            |          |                                                                                       |                      |                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |   |  |   |  |   |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|----------------------|----------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|---|--|---|--|---|--|---|--|---|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                      |                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |   |  |   |  |   |  |
| ID               |            |          | B                                                                                     |                      |                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A |  |  |  | A |  | A |  | A |  | A |  | A |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |                      |                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |   |  |   |  |   |  |
| ID               | Acce Field | Value ID | Value                                                                                 |                      | Description                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |   |  |   |  |   |  |
| A                | RW CHIDX   |          | [255..0]                                                                              |                      | Channel that task <span>RELEASE</span> will subscribe to |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |   |  |   |  |   |  |
| B                | RW EN      |          |                                                                                       |                      |                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |   |  |   |  |   |  |
|                  |            | Disabled | 0                                                                                     | Disable subscription |                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |   |  |   |  |   |  |
|                  |            | Enabled  | 1                                                                                     | Enable subscription  |                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |   |  |   |  |   |  |   |  |

### 7.1.32.5.5 EVENTS\_END

Address offset: 0x104

Granted transaction completed

|                  |               |              |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|---------------|--------------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |               |              |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |               |              |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |               |              |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field    | Value ID     | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW EVENTS_END |              |       | Granted transaction completed                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |               | NotGenerated | 0     | Event not generated                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |               | Generated    | 1     | Event generated                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.32.5.6 EVENTS\_ENDRX

Address offset: 0x110

End of RXD buffer reached

|                  |            |              |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|--------------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |              |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |              |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |              |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID     | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | EVENTS_ENDRX |       | End of RXD buffer reached                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | NotGenerated | 0     | Event not generated                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Generated    | 1     | Event generated                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.32.5.7 EVENTS\_ACQUIRED

Address offset: 0x128

Semaphore acquired



|                  |            |                 |       |                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|------------------|------------|-----------------|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|---|
| Bit number       |            |                 |       | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |   |
| ID               |            |                 |       |                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | A |
| Reset 0x00000000 |            |                 |       | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |   |
| ID               | Acce Field | Value ID        | Value | Description         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
| A                | RW         | EVENTS_ACQUIRED |       | Semaphore acquired  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | NotGenerated    | 0     | Event not generated |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | Generated       | 1     | Event generated     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |

### 7.1.32.5.8 PUBLISH\_END

Address offset: 0x184

Publish configuration for event [END](#)

|                  |            |  |          |                                                                           |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|---------------------------------------------------------------------------|----|------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31                                                                        | 30 | 29                                                   | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |  |          | B                                                                         |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field |  | Value ID | Value                                                                     |    | Description                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          | [255..0]                                                                  |    | Channel that event <span>END</span> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |                                                                           |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled | 0                                                                         |    | Disable publishing                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  | 1                                                                         |    | Enable publishing                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.32.5.9 PUBLISH\_ENDRX

Address offset: 0x190

Publish configuration for event [ENDRX](#)

|                  |            |          |          |                                                                         |    |                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|-------------------------------------------------------------------------|----|-----------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                                                                      | 30 | 29                                                        | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |          |          | B                                                                       |    |                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |    |                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field |          | Value ID | Value                                                                   |    | Description                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | CHIDX    |          | [255..0]                                                                |    | Channel that event <a href="#">ENDRX</a> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW         | EN       |          |                                                                         |    |                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        | Disable publishing                                                      |    |                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        | Enable publishing                                                       |    |                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.32.5.10 PUBLISH\_ACQUIRED

Address offset: 0x1A8

Publish configuration for event [ACQUIRED](#)

|                  |            |          |          |                    |    |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|--------------------|----|-----------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                 | 30 | 29                                                  | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |          |          | B                  |    |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |          |          | 0                  |    |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |          | Value ID | Value              |    | Description                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | CHIDX    |          | [255..0]           |    | Channel that event <b>ACQUIRED</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW         | EN       |          |                    |    |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        | Disable publishing |    |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        | Enable publishing  |    |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.32.5.11 SHORTS

Address offset: 0x200

Shortcuts between local events and tasks

|                  |            |             |       |                                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|------------------|------------|-------------|-------|-----------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|
| Bit number       |            |             |       | 31                                                                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |
| ID               |            |             |       | A                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
| Reset 0x00000000 |            |             |       | 0                                                                     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |
| ID               | Acce Field | Value ID    | Value | Description                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
| A                | RW         | END_ACQUIRE |       | Shortcut between event <span>END</span> and task <span>ACQUIRE</span> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            | Disabled    | 0     | Disable shortcut                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            | Enabled     | 1     | Enable shortcut                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |

### 7.1.32.5.12 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number       |      |          |          | 31    | 30                                                               | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
|------------------|------|----------|----------|-------|------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| ID               |      |          |          | C     |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | B |   |   | A |   |   |   |   |  |
| Reset 0x00000000 |      |          |          | 0     | 0                                                                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |
| ID               | Acce | Field    | Value ID | Value | Description                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| A                | RW   | END      |          |       | Write '1' to enable interrupt for event <a href="#">END</a>      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |          | Set      | 1     | Enable                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |          | Disabled | 0     | Read: Disabled                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |          | Enabled  | 1     | Read: Enabled                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| B                | RW   | ENDRX    |          |       | Write '1' to enable interrupt for event <a href="#">ENDRX</a>    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |          | Set      | 1     | Enable                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |          | Disabled | 0     | Read: Disabled                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |          | Enabled  | 1     | Read: Enabled                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| C                | RW   | ACQUIRED |          |       | Write '1' to enable interrupt for event <a href="#">ACQUIRED</a> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |          | Set      | 1     | Enable                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |          | Disabled | 0     | Read: Disabled                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |          | Enabled  | 1     | Read: Enabled                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

### 7.1.32.5.13 INTENCLR

Address offset: 0x308

Disable interrupt

|                  |      |       |  |          |    |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |                                                                |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|-------|--|----------|----|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|----------------------------------------------------------------|----------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |       |  | 31       | 30 | 29    | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |                                                                |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |       |  |          |    |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | C |   |   |   |   |   | B |   |   |  |  |                                                                | A              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |       |  | 0        | 0  | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |                                                                |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field |  | Value    | ID | Value |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | Description                                                    |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW   | END   |  |          |    |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | Write '1' to disable interrupt for event <a href="#">END</a>   |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       |  | Clear    |    | 1     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |                                                                | Disable        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       |  | Disabled |    | 0     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |                                                                | Read: Disabled |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       |  | Enabled  |    | 1     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |                                                                | Read: Enabled  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW   | ENDRX |  |          |    |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | Write '1' to disable interrupt for event <a href="#">ENDRX</a> |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       |  | Clear    |    | 1     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |                                                                | Disable        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       |  | Disabled |    | 0     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |                                                                | Read: Disabled |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       |  | Enabled  |    | 1     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |                                                                | Read: Enabled  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

|                  |            |          |       |    |                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |   |  |
|------------------|------------|----------|-------|----|-------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|--|--|--|--|--|---|--|
| Bit number       |            |          | 31    | 30 | 29                                                                | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |  |  |  |  |  |   |  |
| ID               |            |          |       |    |                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   | C |   |   |   |   |   |   |   |   |   | B |  |  |  |  |  | A |  |
| Reset 0x00000000 |            |          | 0     | 0  | 0                                                                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |  |  |  |  |  |   |  |
| ID               | Acce Field | Value ID | Value |    | Description                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |   |  |
| C                | RW         | ACQUIRED |       |    | Write '1' to disable interrupt for event <a href="#">ACQUIRED</a> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |   |  |
|                  |            | Clear    | 1     |    | Disable                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |   |  |
|                  |            | Disabled | 0     |    | Read: Disabled                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |   |  |
|                  |            | Enabled  | 1     |    | Read: Enabled                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |   |  |

#### 7.1.32.5.14 SEMSTAT

Address offset: 0x400

### Semaphore status register

| Bit number       |      |         |            | 31    | 30                                                                | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
|------------------|------|---------|------------|-------|-------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| ID               |      |         |            |       |                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| Reset 0x00000001 |      |         |            | 0     | 0                                                                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |  |
| ID               | Acce | Field   | Value ID   | Value | Description                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| A                | R    | SEMSTAT |            |       | Semaphore status                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |         | Free       | 0     | Semaphore is free                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |         | CPU        | 1     | Semaphore is assigned to CPU                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |         | SPIS       | 2     | Semaphore is assigned to SPI slave                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |         | CPUPending | 3     | Semaphore is assigned to SPI but a handover to the CPU is pending |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

#### 7.1.32.5.15 STATUS

Address offset: 0x440

Status from last transaction

Individual bits are cleared by writing a '1' to the bits that shall be cleared

| Bit number       |      |            | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |    |       |                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|------------|---------------------------------------------------------------------------------------|----|-------|---------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |      |            | B A                                                                                   |    |       |                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |            | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |    |       |                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field      | Value                                                                                 | ID | Value | Description                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW   | OVERREAD   |                                                                                       |    |       | TX buffer over-read detected, and prevented |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | NotPresent | 0                                                                                     |    |       | Read: error not present                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Present    | 1                                                                                     |    |       | Read: error present                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Clear      | 1                                                                                     |    |       | Write: clear error on writing '1'           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW   | OVERFLOW   |                                                                                       |    |       | RX buffer overflow detected, and prevented  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | NotPresent | 0                                                                                     |    |       | Read: error not present                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Present    | 1                                                                                     |    |       | Read: error present                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Clear      | 1                                                                                     |    |       | Write: clear error on writing '1'           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.32.5.16 ENABLE

Address offset: 0x500

### Enable SPI slave

|                  |            |  |          |       |  |                             |  |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|-------|--|-----------------------------|--|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          |       |  |                             |  |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |  |          |       |  |                             |  |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | A | A | A | A |   |   |
| Reset 0x00000000 |            |  |          |       |  |                             |  |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID | Value |  | Description                 |  |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW ENABLE  |  |          |       |  | Enable or disable SPI slave |  |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled | 0     |  | Disable SPI slave           |  |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  | 2     |  | Enable SPI slave            |  |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.32.5.17 PSEL.SCK

Address offset: 0x508

## Pin select for SCK

|                  |      |              |         |                                                                         |       |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------|--------------|---------|-------------------------------------------------------------------------|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |      |              |         | 31                                                                      | 30    | 29          | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |      |              |         | C                                                                       |       |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Reset 0xFFFFFFFF |      |              |         | 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 |       |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce | Field        | Value   | ID                                                                      | Value | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW   | PIN          | [0..31] |                                                                         |       | Pin number  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| B                | RW   | PORT         | [0..1]  |                                                                         |       | Port number |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| C                | RW   | CONNECT      |         |                                                                         |       | Connection  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      | Disconnected | 1       |                                                                         |       | Disconnect  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      | Connected    | 0       |                                                                         |       | Connect     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 7.1.32.5.18 PSEL.MISO

Address offset: 0x50C

### Pin select for MISO signal

|                  |            |              |         |    |    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------------|---------|----|----|----|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |              | 31      | 30 | 29 | 28 | 27          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |              | C       |    |    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | B | A | A | A | A |
| Reset 0xFFFFFFFF |            |              | 1       | 1  | 1  | 1  | 1           | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |   |
| ID               | Acce Field | Value ID     | Value   |    |    |    | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW PIN     |              | [0..31] |    |    |    | Pin number  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW PORT    |              | [0..1]  |    |    |    | Port number |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| C                | RW CONNECT |              |         |    |    |    | Connection  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disconnected | 1       |    |    |    | Disconnect  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Connected    | 0       |    |    |    | Connect     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.32.5.19 PSEL.MOSI

Address offset: 0x510

### Pin select for MOSI signal

|                  |      |         |              |    |         |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------|---------|--------------|----|---------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |      |         |              | 31 | 30      | 29          | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |      |         |              | C  |         |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | B |   |   |   | A | A | A | A | A |
| Reset 0xFFFFFFFF |      |         |              | 1  | 1       | 1           | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |   |
| ID               | Acce | Field   | Value        | ID | Value   | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW   | PIN     |              |    | [0..31] | Pin number  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW   | PORT    |              |    | [0..1]  | Port number |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| C                | RW   | CONNECT |              |    |         | Connection  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |         | Disconnected |    | 1       | Disconnect  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |         | Connected    |    | 0       | Connect     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.32.5.20 PSEL.CSN

Address offset: 0x514

Pin select for CSN signal

|                  |      |         |              |    |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |             |            |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|---------|--------------|----|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|-------------|------------|---|---|---|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |         |              | 31 | 30      | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |             |            |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |         |              | C  |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | B |   |   |   |   |   |   |   |   |  |  |             | A          | A | A | A | A |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0xFFFFFFFF |      |         |              | 1  | 1       | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  |  |             |            |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field   | Value        | ID | Value   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | Description |            |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW   | PIN     |              |    | [0..31] |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | Pin number  |            |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW   | PORT    |              |    | [0..1]  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | Port number |            |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW   | CONNECT |              |    |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | Connection  |            |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |         | Disconnected |    | 1       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |             | Disconnect |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |         | Connected    |    | 0       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |             | Connect    |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.32.5.21 PSELSCK ( Deprecated )

Address offset: 0x508

Pin select for SCK

|                  |            |              |            |                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------------|------------|---------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |              |            | 31                                          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |              |            | A                                           | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0xFFFFFFFF |            |              |            | 1                                           | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ID               | Acce Field | Value ID     | Value      | Description                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | PSELSCK      | [0..31]    | Pin number configuration for SPI SCK signal |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disconnected | 0xFFFFFFFF | Disconnect                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.32.5.22 PSELMISO ( Deprecated )

Address offset: 0x50C

Pin select for MISO

|                  |            |              |          |            |    |    |    |                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------------|----------|------------|----|----|----|----------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |              |          | 31         | 30 | 29 | 28 | 27                                           | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |              |          | A          | A  | A  | A  | A                                            | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0xFFFFFFFF |            |              |          | 1          | 1  | 1  | 1  | 1                                            | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ID               | Acce Field |              | Value ID | Value      |    |    |    | Description                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | PSELMISO     |          | [0..31]    |    |    |    | Pin number configuration for SPI MISO signal |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disconnected |          | 0xFFFFFFFF |    |    |    | Disconnect                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.32.5.23 PSELMOSI ( Deprecated )

Address offset: 0x510

Pin select for MOSI

|                  |            |              |          |            |    |    |    |                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------------|----------|------------|----|----|----|----------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |              |          | 31         | 30 | 29 | 28 | 27                                           | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |              |          | A          | A  | A  | A  | A                                            | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0xFFFFFFFF |            |              |          | 1          | 1  | 1  | 1  | 1                                            | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ID               | Acce Field |              | Value ID | Value      |    |    |    | Description                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | PSELMOSI     |          | [0..31]    |    |    |    | Pin number configuration for SPI MOSI signal |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disconnected |          | 0xFFFFFFFF |    |    |    | Disconnect                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.32.5.24 PSELCSN ( Deprecated )

Address offset: 0x514

Pin select for CSN

|                  |            |              |            |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|--------------|------------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |              |            | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |              |            | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0xFFFFFFFF |            |              |            | 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID     | Value      | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW PSELCSN |              | [0..31]    | Pin number configuration for SPI CSN signal                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disconnected | 0xFFFFFFFF | Disconnect                                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.32.5.25 RXDPTR ( Deprecated )

Address offset: 0x534

RXD data pointer

|                  |            |          |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Description |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW RXDPTR  |          | RXD data pointer                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**Note:** See the memory chapter for details about which memories are available for EasyDMA.

### 7.1.32.5.26 MAXRX ( Deprecated )

Address offset: 0x538

Maximum number of bytes in receive buffer

| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|-------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |            |          | A A A A A A A A A A A A A A A A                                                       |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW MAXRX   |          | [1..0xffff]                                                                           | Maximum number of bytes in receive buffer |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.32.5.27 AMOUNTRX ( Deprecated )

Address offset: 0x53C

Number of bytes received in last granted transaction

|                  |            |          |                                                                                       |                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|----------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          | A A A A A A A A A A A A A A A A                                                       |                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | R AMOUNTRX |          | [1..0xffff]                                                                           | Number of bytes received in the last granted transaction |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.32.5.28 RXD.PTR

Address offset: 0x534

## RXD data pointer

|                  |            |  |          |       |    |    |    |                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|-------|----|----|----|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31    | 30 | 29 | 28 | 27               | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |  |          | A     | A  | A  | A  | A                | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |          | 0     | 0  | 0  | 0  | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID | Value |    |    |    | Description      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW PTR     |  |          |       |    |    |    | RXD data pointer |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

**Note:** See the memory chapter for details about which memories are available for EasyDMA.

## 7.1.32.5.29 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in receive buffer

|                  |            |        |          |             |    |    |    |                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------|----------|-------------|----|----|----|-------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |        |          | 31          | 30 | 29 | 28 | 27                                        | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |        |          |             |    |    |    |                                           |    |    |    |    |    |    |    |    |    |    |    | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |        |          | 0           | 0  | 0  | 0  | 0                                         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |
| ID               | Acce Field |        | Value ID | Value       |    |    |    | Description                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | MAXCNT |          | [1..0xffff] |    |    |    | Maximum number of bytes in receive buffer |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

## 7.1.32.5.30 RXD.AMOUNT

Address offset: 0x53C

Number of bytes received in last granted transaction

|                  |  |  |  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            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|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| Bit number       |  |  |  | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      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|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |  |  |  | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                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|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |  |  |  | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 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## 7.1.32.5.31 RXD.LIST

Address offset: 0x540

EasyDMA list type

|                  |       |       |           |                                                                                       |                      |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|-------|-------|-----------|---------------------------------------------------------------------------------------|----------------------|-------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |       |       |           | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                      |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |       |       |           | A A                                                                                   |                      |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |       |       |           | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0           |                      |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acces | Field | Value     | ID                                                                                    | Value                | Description |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW    | LIST  |           |                                                                                       |                      | List type   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |       |       | Disabled  | 0                                                                                     | Disable EasyDMA list |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |       |       | ArrayList | 1                                                                                     | Use array list       |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

## 7.1.32.5.32 TXDPTR ( Deprecated )

Address offset: 0x544

TXD data pointer

|                  |            |  |          |       |    |    |    |                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|-------|----|----|----|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31    | 30 | 29 | 28 | 27               | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |  |          | A     | A  | A  | A  | A                | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |          | 0     | 0  | 0  | 0  | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID | Value |    |    |    | Description      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW TXDPTR  |  |          |       |    |    |    | TXD data pointer |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

**Note:** See the memory chapter for details about which memories are available for EasyDMA.

### 7.1.32.5.33 MAXTX ( Deprecated )

Address offset: 0x548

Maximum number of bytes in transmit buffer

|                  |            |          |             |    |    |    |                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|-------------|----|----|----|--------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          | 31          | 30 | 29 | 28 | 27                                         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |          |             |    |    |    |                                            |    |    |    |    |    |    |    |    |    |    |    | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          | 0           | 0  | 0  | 0  | 0                                          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |
| ID               | Acce Field | Value ID | Value       |    |    |    | Description                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | MAXTX    | [1..0xffff] |    |    |    | Maximum number of bytes in transmit buffer |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.32.5.34 AMOUNTTX ( Deprecated )

Address offset: 0x54C

Number of bytes transmitted in last granted transaction

|                  |            |          |             |    |    |    |                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|-------------|----|----|----|---------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          | 31          | 30 | 29 | 28 | 27                                                      | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |          |             |    |    |    |                                                         |    |    |    |    |    |    |    |    |    |    |    | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          | 0           | 0  | 0  | 0  | 0                                                       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |
| ID               | Acce Field | Value ID | Value       |    |    |    | Description                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | R          | AMOUNTTX | [1..0xffff] |    |    |    | Number of bytes transmitted in last granted transaction |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.32.5.35 TXD.PTR

Address offset: 0x544

TXD data pointer

|                  |            |  |          |       |    |    |    |                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|-------|----|----|----|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31    | 30 | 29 | 28 | 27               | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |  |          | A     | A  | A  | A  | A                | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |          | 0     | 0  | 0  | 0  | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID | Value |    |    |    | Description      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW PTR     |  |          |       |    |    |    | TXD data pointer |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

**Note:** See the memory chapter for details about which memories are available for EasyDMA.

### 7.1.32.5.36 TXD.MAXCNT

Address offset: 0x548

Maximum number of bytes in transmit buffer



|                  |            |        |          |             |       |  |  |  |  |    |    |    |    |                                            |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------|----------|-------------|-------|--|--|--|--|----|----|----|----|--------------------------------------------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |        |          |             |       |  |  |  |  | 31 | 30 | 29 | 28 | 27                                         | 26          | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |
| ID               |            |        |          |             |       |  |  |  |  |    |    |    |    |                                            |             |    |    |    |    | A  |    |    |    |    |    |    |    |    |    | A  | A  | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |        |          |             |       |  |  |  |  | 0  | 0  | 0  | 0  | 0                                          | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |
| ID               | Acce Field |        | Value ID |             | Value |  |  |  |  |    |    |    |    |                                            | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | MAXCNT |          | [1..0xffff] |       |  |  |  |  |    |    |    |    | Maximum number of bytes in transmit buffer |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.32.5.37 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transmitted in last granted transaction

|                  |            |          |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Accs Field | Value ID | Value                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Description                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | R          | AMOUNT   | [1..0xffff]                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Number of bytes transmitted in last granted transaction |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

#### 7.1.32.5.38 TXD.LIST

Address offset: 0x550

## EasyDMA list type

|                  |            |  |           |  |       |    |                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|-----------|--|-------|----|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |           |  | 31    | 30 | 29                   | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |  |           |  |       |    |                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A | A |
| Reset 0x00000000 |            |  |           |  | 0     | 0  | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |
| ID               | Acce Field |  | Value ID  |  | Value |    | Description          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW LIST    |  |           |  |       |    | List type            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled  |  | 0     |    | Disable EasyDMA list |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | ArrayList |  | 1     |    | Use array list       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.32.5.39 CONFIG

Address offset: 0x554

## Configuration register

|                  |            |            |       |                                                                     |                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|------------|-------|---------------------------------------------------------------------|-----------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |            | 31    | 30                                                                  | 29                          | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |            | C B A |                                                                     |                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |            | 0     | 0                                                                   | 0                           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |
| ID               | Acce Field | Value ID   | Value |                                                                     | Description                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW ORDER   |            |       |                                                                     | Bit order                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | MsbFirst   | 0     | Most significant bit shifted out first                              |                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | LsbFirst   | 1     | Least significant bit shifted out first                             |                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| B                | RW CPHA    |            |       |                                                                     | Serial clock (SCK) phase    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Leading    | 0     | Sample on leading edge of clock, shift serial data on trailing edge |                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Trailing   | 1     | Sample on trailing edge of clock, shift serial data on leading edge |                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| C                | RW CPOL    |            |       |                                                                     | Serial clock (SCK) polarity |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | ActiveHigh | 0     | Active high                                                         |                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | ActiveLow  | 1     | Active low                                                          |                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.32.5.40 DEF

Address offset: 0x55C

Default character. Character clocked out in case of an ignored transaction.

|                  |      |       |       |                                                                                       |       |                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|-------|-------|---------------------------------------------------------------------------------------|-------|-----------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |       |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |       |       | A A A A A A A A                                                                       |       |                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |       |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |       |                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field | Value | ID                                                                                    | Value | Description                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW   | DEF   |       |                                                                                       |       | Default character. Character clocked out in case of an ignored transaction. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.32.5.41 ORC

Address offset: 0x5C0

Over-read character

|            |  |  |  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           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| Bit number |  |  |  | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            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## 7.1.32.6 Electrical specification

### 7.1.32.6.1 SPIS slave interface electrical specifications

| Symbol                  | Description                                             | Min. | Typ. | Max. | Units |
|-------------------------|---------------------------------------------------------|------|------|------|-------|
| f <sub>SPIS</sub>       | Bit rates for SPIS <sup>24</sup>                        | ..   | ..   | ..   | Mbps  |
| t <sub>SPIS,START</sub> | Time from RELEASE task to receive/transmit (CSN active) | ..   | ..   | ..   | µs    |

### 7.1.32.6.2 Serial Peripheral Interface Slave (SPIS) timing specifications

| Symbol                   | Description                       | Min. | Typ. | Max. | Units |
|--------------------------|-----------------------------------|------|------|------|-------|
| t <sub>SPIS,CSCKIN</sub> | SCK input period                  | ..   | ..   | ..   | ns    |
| t <sub>SPIS,RFCKIN</sub> | SCK input rise/fall time          | ..   | ..   | ..   | ns    |
| t <sub>SPIS,WHCKIN</sub> | SCK input high time               | ..   | ..   | ..   | ns    |
| t <sub>SPIS,WLCKIN</sub> | SCK input low time                | ..   | ..   | ..   | ns    |
| t <sub>SPIS,SUCSN</sub>  | CSN to CLK setup time             | ..   | ..   | ..   | ns    |
| t <sub>SPIS,HCSN</sub>   | CLK to CSN hold time              | ..   | ..   | ..   | ns    |
| t <sub>SPIS,ASA</sub>    | CSN to MISO driven                | ..   | ..   | ..   | ns    |
| t <sub>SPIS,ASO</sub>    | CSN to MISO valid <sup>a</sup>    | ..   | ..   | ..   | ns    |
| t <sub>SPIS,DISSO</sub>  | CSN to MISO disabled <sup>a</sup> | ..   | ..   | ..   | ns    |
| t <sub>SPIS,CWH</sub>    | CSN inactive time                 | ..   | ..   | ..   | ns    |
| t <sub>SPIS,VSO</sub>    | CLK edge to MISO valid            | ..   | ..   | ..   | ns    |
| t <sub>SPIS,HSO</sub>    | MISO hold time after CLK edge     | ..   | ..   | ..   | ns    |

<sup>24</sup> High bit rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.

<sup>a</sup> At 25pF load, including GPIO capacitance, see GPIO spec.

| Symbol          | Description                 | Min. | Typ. | Max. | Units |
|-----------------|-----------------------------|------|------|------|-------|
| $t_{SPIS,SUSI}$ | MOSI to CLK edge setup time | ..   | ..   | ..   | ns    |
| $t_{SPIS,HSI}$  | CLK edge to MOSI hold time  | ..   | ..   | ..   | ns    |

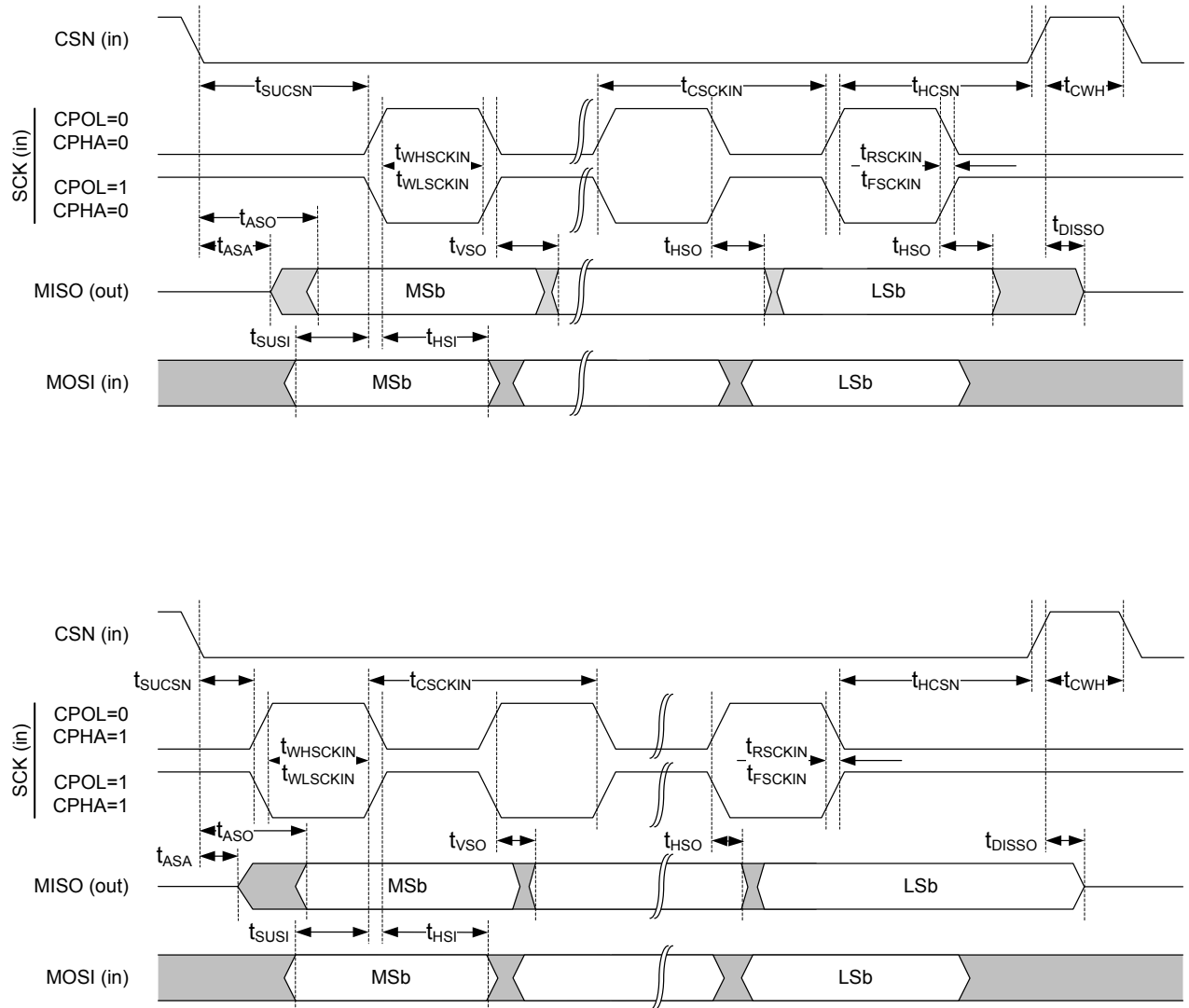


Figure 196: SPIS timing diagram



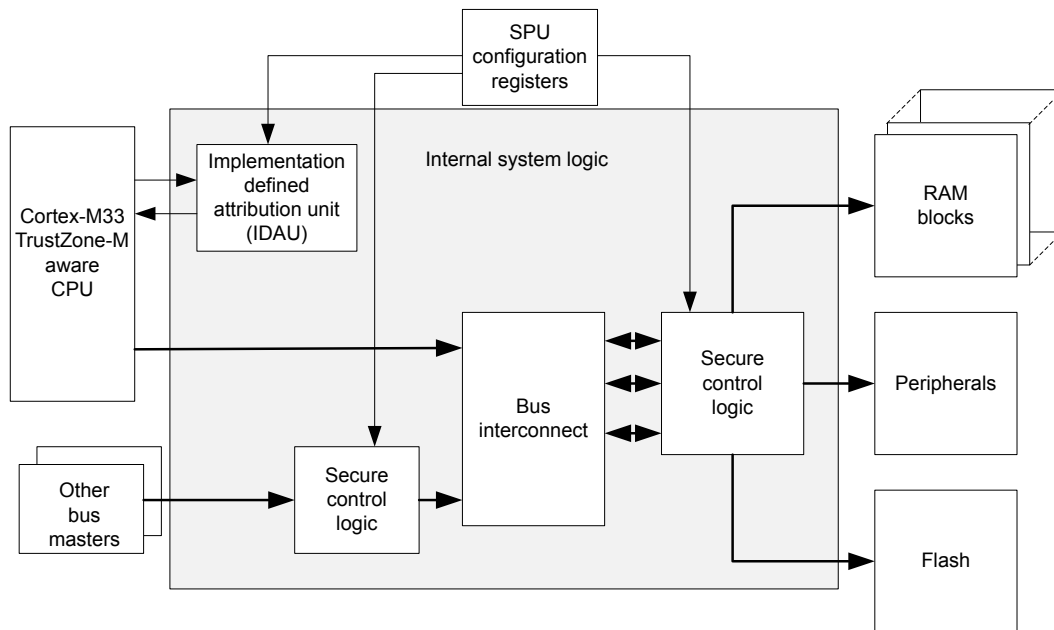


Figure 198: Simplified view of the protection of RAM, flash and peripherals using SPU

The protection logic implements a read-as-zero/write-ignore (RAZ/WI) policy:

- A blocked read operation will always return a zero value on the bus, preventing information leak
- A write operation to a forbidden region or peripheral will be ignored

An error is reported through dedicated error signals. For security state violations from an M33 master this will be a SecureFault exception, for other violations this will be an SPU event. The SPU event can be configured to generate an interrupt towards the CPU.

Other resources like pins and DPPI channels are protected by comparing the security attributes of the protected resource with the security attribute of the peripheral that wants to access it. The SPU is the only place where those security attributes can be configured.

#### 7.1.33.1.1 Special considerations for ARM TrustZone for Cortex-M enabled system

For a ARM TrustZone for Cortex-M enabled CPU, the SPU also controls custom logic.

Custom logic is shown as the implementation defined attribution unit (IDAU) in figure [Figure 198: Simplified view of the protection of RAM, flash and peripherals using SPU](#) on page 569. Full support is provided for:

- ARM TrustZone for Cortex-M related instructions, like test target (TT) for reporting the security attributes of a region
- Non-secure callable (NSC) regions, to implement secure entry points from non-secure code

The SPU provides the necessary registers to configure the security attributes for memory regions and peripherals. However, as a requirement to use the SPU, the secure attribution unit (SAU) needs to be disabled and all memory set as non-secure in the ARM core. This will allow the SPU to control the IDAU and set the security attribution of all addresses as originally intended.

#### 7.1.33.2 Flash access control

The flash memory space is divided in regions, each of them with configurable permissions settings.

The flash memory space is divided into 64 regions of 16 KiB.

For each region, four different types of permissions can be configured:

#### Read

Allows data read access to the region. Note that code fetch from this region is not controlled by the read permission but by the execute permission described below.

#### Write

Allows write or erase access to the region

#### Execute

Allows code fetch from this region, even if data read is disabled

#### Secure

Allows only bus accesses with the security attribute set to access the region

Permissions can be set independently. For example, it is possible to configure a flash region to be accessible only through secure transfer, being read-only (no write allowed) and non-executable (no code fetch allowed). For each region, permissions can be set and then locked by using the [FLASHREGION\[n\].PERM.LOCK](#) bit, to prevent subsequent modifications.

Note that the debugger is able to step through execute-protected memory regions.

The following figure shows the flash memory space and the divided regions:

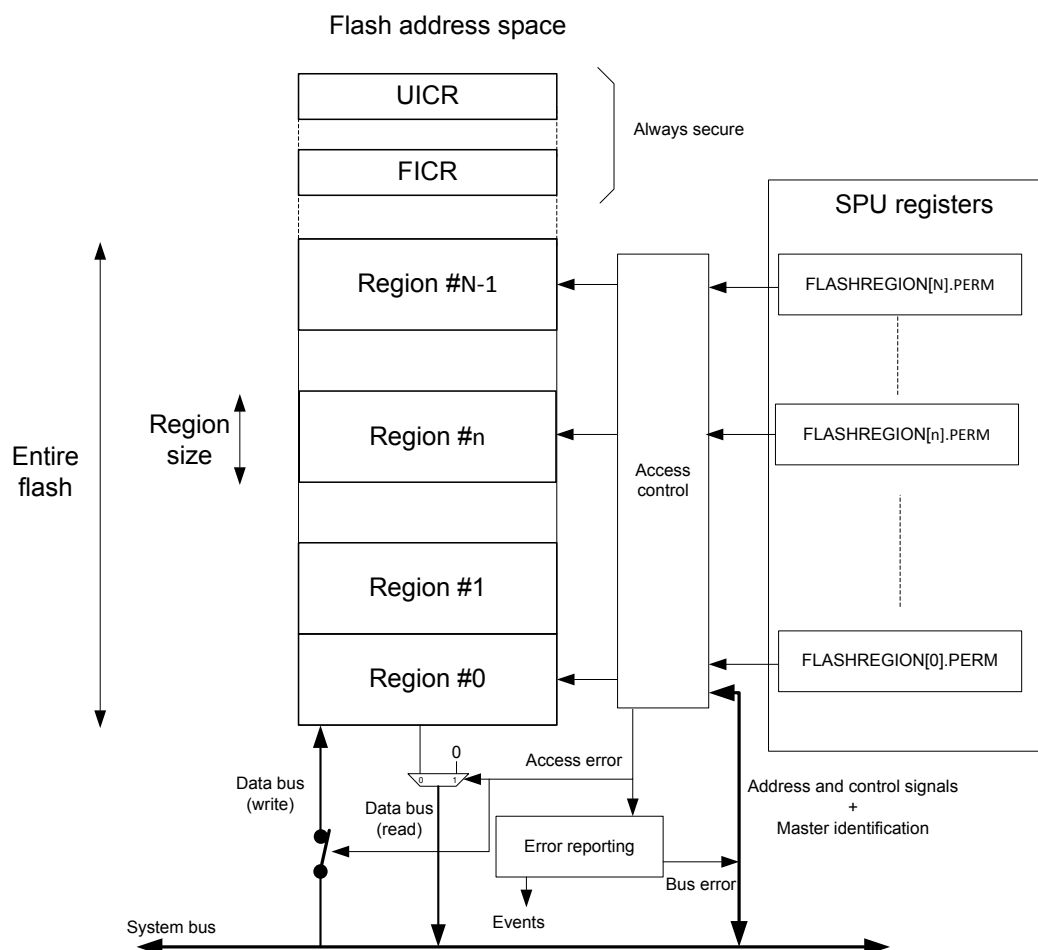


Figure 199: Definition of the N=64 regions, each of 16 KiB, in the flash memory space

### 7.1.33.2.1 Non-secure callable (NSC) region definition in flash

The SPU provides support for the definition of non-secure callable (NSC) sub-regions to allow non-secure to secure function calls.

A non-secure callable sub-region can only exist within an existing secure region and its definition is done using two registers:

- `FLASHNSC[n].REGION`, used to select the secure region that will contain the NSC sub-region
- `FLASHNSC[n].SIZE`, used to define the size of the NSC sub-region within the secure region

The NSC sub-region will be defined from the highest address in that region, going downwards. Figure below illustrates the NSC sub-regions and the registers used for their definition:

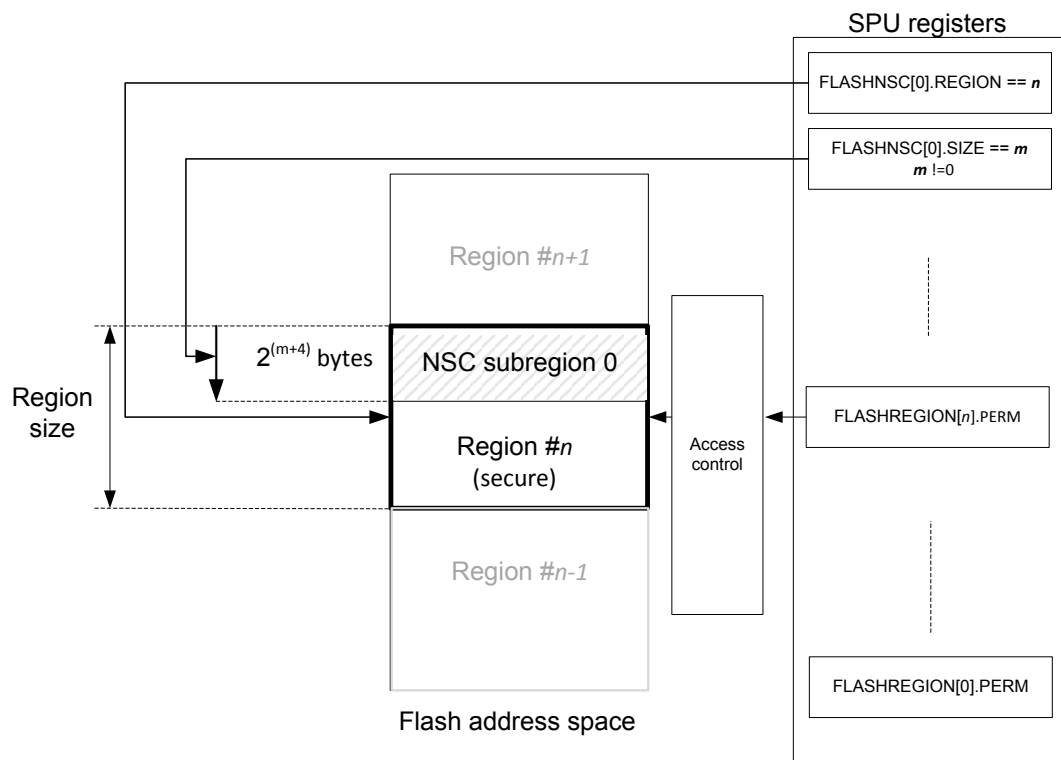


Figure 200: Non-secure callable region definition in the flash memory space

The NSC sub-region will only be defined if:

- `FLASHNSC[i].SIZE` value is non zero
- `FLASHNSC[i].REGION` defines a secure region

If `FLASHNSC[i].REGION` and `FLASHNSC[j].REGION` have the same value, there is only one sub-region defined as NSC, with the size given by the maximum of `FLASHNSC[i].SIZE` and `FLASHNSC[j].SIZE`.

If `FLASHNSC[i].REGION` defines a non-secure region, then there is no non-secure callable region defined and the selected region stays non-secure.

### 7.1.33.2.2 Flash access error reporting

The SPU and the logic controlled by it will respond with a certain behavior once an access violation is detected.

The following will happen once the logic controlled by the SPU detects an access violation on one of the flash ports:

- The faulty transfer will be blocked

- In case of a read transfer, the bus will be driven to zero
- Feedback will be sent to the master through specific bus error signals, if this is supported by the master. Moreover, the SPU will receive an event that can optionally trigger an interrupt towards the CPU.
- SecureFault exception will be triggered if security violation is detected for access from Cortex-M33
- BusFault exception will be triggered when read/write/execute protection violation is detected for Cortex-M33
- FLASHACCERR event will be triggered if any access violations are detected for all master types except for Cortex-M33 security violation

The following table summarizes the SPU behavior based on the type of initiator and access violation:

| Master type   | Security violation        | Read/Write/Execute protection violation |
|---------------|---------------------------|-----------------------------------------|
| Cortex-M33    | SecureFault exception     | BusFault exception, FLASHACCERR event   |
| EasyDMA       | RAZ/WI, FLASHACCERR event | RAZ/WI, FLASHACCERR event               |
| Other masters | RAZ/WI, FLASHACCERR event | RAZ/WI, FLASHACCERR event               |

Table 152: Error reporting for flash access errors

For a Cortex-M33 master, the SecureFault exception will take precedence over the BusFault exception if a security violation occurs simultaneously with another type of violation.

### 7.1.33.2.3 UICR and FICR protections

The user information configuration registers (UICR) and factory information configuration registers (FICR) are always considered as secure. FICR registers are read-only. UICR registers can be read and written by secure code only.

Writing new values to user information configuration registers must follow the procedure described in [NVMC — Non-volatile memory controller](#) on page 318. Code execution from FICR and UICR address spaces will always be reported as access violation, an exception to this rule applies during a debug session.

### 7.1.33.3 RAM access control

The RAM memory space is divided in regions, each of them with configurable permissions settings.

The RAM memory space is divided into 64 regions of 8 KiB.

For each region, four different types of permissions can be configured:

#### Read

Allows data read access to the region. Code fetch from this region is not controlled by the read permission but by the execute permission described below.

#### Write

Allows write access to the region

#### Execute

Allows code fetch from this region

#### Secure

Allows only bus accesses with the security attribute set to access the region

Permissions can be set independently. For example, it is possible to configure a RAM region to be accessible only through secure transfer, being read-only (no write allowed) and non-executable (no



code fetch allowed). For each region, permissions can be set and then locked to prevent subsequent modifications by using the `RAMREGION[n].PERM.LOCK` bit.

The following figure shows the RAM memory space and the devided regions:

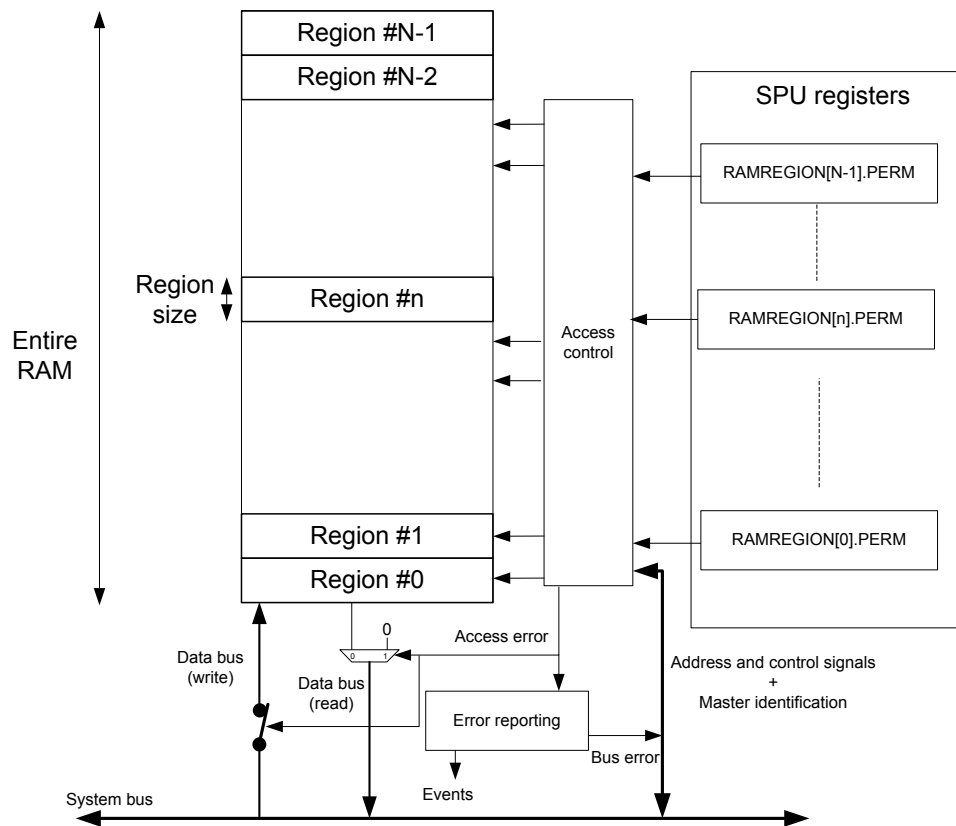


Figure 201: Definition of the N=64 regions, each of 8 KiB, in the RAM memory space

#### 7.1.33.3.1 Non-secure callable (NSC) region definition in RAM

The SPU provides support for the definition of non-secure callable (NSC) sub-regions to allow non-secure to secure function calls.

A non-secure callable sub-region can only exist within an existing secure region and its definition is done using two registers:

- `RAMNSC[n].REGION`, used to select the secure region that will contain the NSC sub-region
- `RAMNSC[n].SIZE`, used to define the size of the NSC sub-region within the secure region

The NSC sub-region will be defined from the highest address in that region, going downwards. Figure below illustrates the NSC sub-regions and the registers used for their definition:

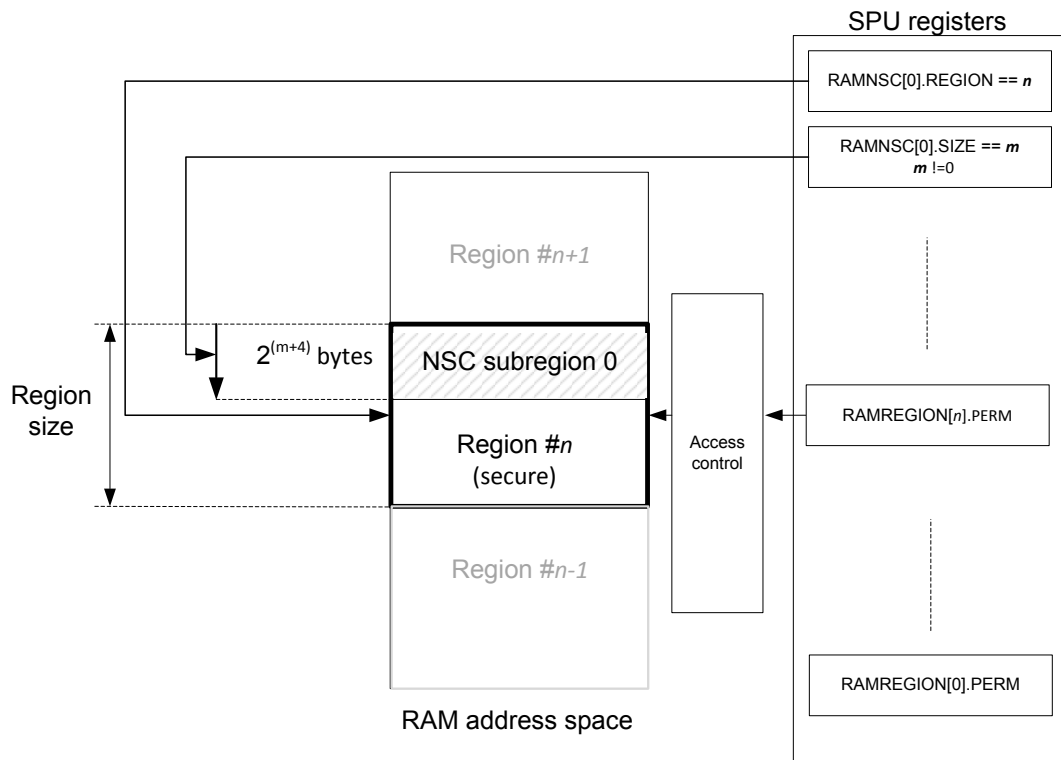


Figure 202: Non-secure callable region definition in the RAM memory space

The NSC sub-region will only be defined if:

- `RAMNSC[i].SIZE` value is non zero
- `RAMNSC[i].REGION` defines a secure region

If `RAMNSC[i].REGION` and `RAMNSC[j].REGION` have the same value, there is only one sub-region defined as NSC, with the size given by the maximum of `RAMNSC[i].SIZE` and `RAMNSC[j].SIZE`.

If `RAMNSC[i].REGION` defines a non-secure region, then there is no non-secure callable region defined and the selected region stays non-secure.

### 7.1.33.3.2 RAM access error reporting

The SPU and the logic controlled by it will respond with a certain behavior once an access violation is detected.

The following will happen once the logic controlled by the SPU detects an access violation on one of the RAM ports:

- The faulty transfer will be blocked
- In case of a read transfer, the bus will be driven to zero
- Feedback will be sent to the master through specific bus error signals, if this is supported by the master
- SecureFault exception will be triggered if security violation is detected for access from Cortex-M33
- BusFault exception will be triggered when read/write/execute protection violation is detected for Cortex-M33. The SPU will also generate an event that can optionally trigger an interrupt towards the CPU.
- `RAMACCERR` event will be triggered if any access violations are detected for all master types but for Cortex-M33 security violation

The following table summarizes the SPU behavior based on the type of initiator and access violation:

| Master type   | Security violation      | Read/Write/Execute protection violation |
|---------------|-------------------------|-----------------------------------------|
| Cortex-M33    | SecureFault exception   | BusFault exception, RAMACCERR event     |
| EasyDMA       | RAZ/WI, RAMACCERR event | RAZ/WI, RAMACCERR event                 |
| Other masters | RAZ/WI, RAMACCERR event | RAZ/WI, RAMACCERR event                 |

Table 153: Error reporting for RAM access errors

For a Cortex-M33 master, the SecureFault exception will take precedence over the BusFault exception if a security violation occurs simultaneously with another type of violation.

#### 7.1.33.4 Peripheral access control

Access controls are defined by the characteristics of the peripheral.

Peripherals can have their security attribute set as:

##### Always secure

For a peripheral related to system control

##### Always non-secure

For some general-purpose peripherals

##### Configurable

For general-purpose peripherals that may be configured for secure only access

The full list of peripherals and their corresponding security attributes can be found in [Memory](#) on page 18. For each peripheral with ID  $n$ , [PERIPHID\[n\].PERM](#) will show whether the security attribute for this peripheral is configurable or not.

If not hardcoded, the security attribute can be configured using the [PERIPHID\[id\].PERM](#).

At reset, all user-selectable and split security peripherals are set to be secure, with secure DMA where present.

Secure code can access both secure peripherals and non-secure peripherals.

##### 7.1.33.4.1 Peripherals with split security

Peripherals with split security are defined to handle use-cases when both secure and non-secure code needs to control the same resource.

When peripherals with split security have their security attribute set to non-secure, access to specific registers and bitfields within some registers is dependent on the security attribute of the bus transfer. For example, some registers will not be accessible for a non-secure transfer.

When peripherals with split security have their security attribute set to secure, then only secure transfers can access their registers.

See [Instantiation](#) on page 136 for an overview of split security peripherals. Respective peripheral chapters explain the specific security behavior of each peripheral.

##### 7.1.33.4.2 Peripheral address mapping

Peripherals that have non-secure security mapping have their address starting with 0x4XXX\_XXXX. Peripherals that have secure security mapping have their address starting with 0x5XXX\_XXXX.

Peripherals with a user-selectable security mapping are available at an address starting with:

- 0x4XXX\_XXXX, if the peripheral security attribute is set to non-secure
- 0x5XXX\_XXXX, if the peripheral security attribute is set to secure

**Note:** Accesses to the 0x4XXX\_XXXX address range from secure or non-secure code for a peripheral marked as secure will result in a bus-error.

Secure code accessing the 0x5XXX\_XXXX address range of a peripheral marked as non-secure will also result in a bus-error.

Peripherals with a split security mapping are available at an address starting with:

- 0x4XXX\_XXXX for non-secure access and 0x5XXX\_XXXX for secure access, if the peripheral security attribute is set to non-secure
  - Secure registers in the 0x4XXX\_XXXX range are not visible for secure or non-secure code, and an attempt to access such a register will result in write-ignore, read-as-zero behavior
  - Secure code can access both non-secure and secure registers in the 0x5XXX\_XXXX range
- 0x5XXX\_XXXX, if the peripheral security attribute is set to secure

Any attempt to access the 0x5000\_0000-0x5FFF\_FFFF address range from non-secure code will be ignored and generate a SecureFault exception.

The table below illustrates the address mapping for the three type of peripherals in all possible configurations

| Security-features and configuration                  | Is mapped at 0x4XXX_XXXX?     | Is mapped at 0x5XXX_XXXX? |
|------------------------------------------------------|-------------------------------|---------------------------|
| Secure peripheral                                    | No                            | Yes                       |
| Non-secure peripheral                                | Yes                           | No                        |
| Split-security peripheral, with attribute=secure     | No                            | Yes                       |
| Split-security peripheral, with attribute=non-secure | Yes, restricted functionality | Yes                       |

Table 154: Peripheral's address mapping in relation to its security-features and configuration

#### 7.1.33.4.3 Special considerations for peripherals with DMA master

Peripherals containing a DMA master can be configured so the security attribute of the DMA transfers is different from the security attribute of the peripheral itself. This allows a secure peripheral to do non-secure data transfers to or from the system memories.

The following conditions must be met:

- The DMA field of `PERIPHID[n].PERM.SECURITYMAPPING` should read as "SeparateAttribute"
- The peripheral itself should be secure (`PERIPHID[n].PERM.SECATTR == 1`)

Then it is possible to select the security attribute of the DMA transfers using the field `DMASEC` (`PERIPHID[n].PERM.DMASEC == Secure` and `PERIPHID[n].PERM.DMASEC == NonSecure`) in `PERIPHID[n].PERM`.

#### 7.1.33.4.4 Peripheral access error reporting

Peripherals send error reports once access violation is detected.

The following will happen if the logic controlled by the SPU detects an access violation on one of the peripherals:

- The faulty transfer will be blocked
- In case of a read transfer, the bus will be driven to zero
- Feedback is sent to the master through specific bus error signals, if this is supported by the master. If the master is a processor supporting ARM TrustZone for Cortex-M, a SecureFault exception will be generated for security related errors.
- The `PERIPHACCERR` event will be triggered

### 7.1.33.5 Pin access control

Access to device pins can be controlled by the SPU. A pin can be declared as secure so that only secure peripherals or secure code can access it. Pins declared as non-secure can be accessed by both secure and non-secure peripherals or code.

The security attribute of each pin can be individually configured in SPU's `GPIOPORT[n].PERM` register. When the secure attribute is set for a pin, only peripherals that have the secure attribute set will be able to read the value of the pin or change it.

Peripherals can select the pin(s) they need access to through their PSEL register(s). If a peripheral has its attribute set to non-secure, but one of its PSEL registers selects a pin with the attribute set to secure, the SPU controlled logic will ensure that the pin selection is not propagated. In addition, the pin value will always be read as zero, to prevent a non-secure peripheral from obtaining a value from a secure pin. Whereas access to other pins with attribute set as non-secure will not be blocked.

Pins can be assigned to other domains than the application domain by changing the MCUSEL value in the GPIO PIN\_CNF[n] register. Domains that do not have a pin assigned to them can neither control that pin nor read its status. Any pin configuration set in a domain that doesn't have ownership of that pin will not take effect until the MCUSEL is updated to assign that pin to the domain. Within each domain, pin access is controlled by that domain's local security configuration and peripheral PSEL registers. This is illustrated in the following figure:

**Note:** The SPU setting will still count when the APP domain accesses its local GPIO peripheral, as local registers are still writable even though MCUSEL is set to a different domain. Any changes in the APP GPIO peripheral done to a GPIO controlled by another domain will not affect the GPIO pad until MCUSEL is changed to APP.

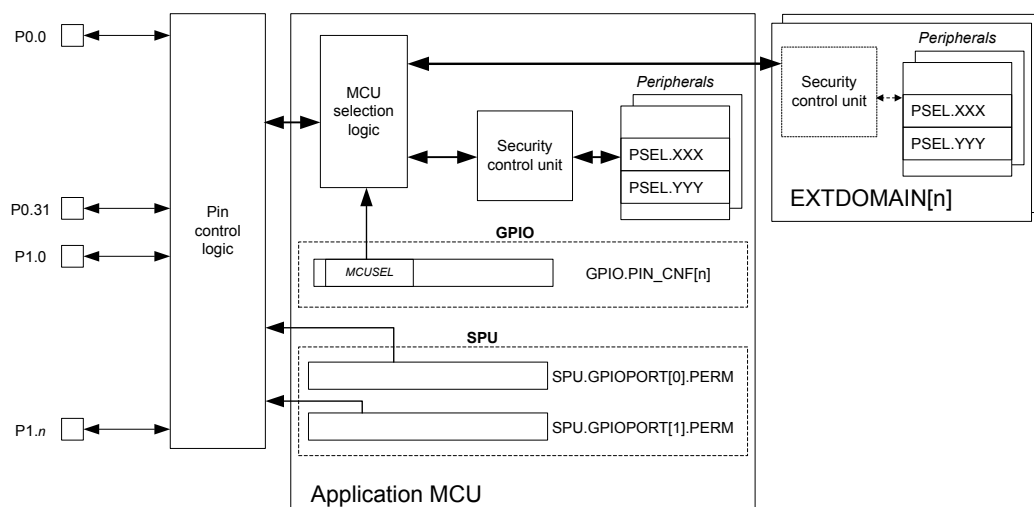


Figure 203: Pin access for domains other than the application domain

### 7.1.33.6 DPPI access control

Access to DPPI channels can be restricted. A channel can be declared as secure so that only secure peripherals can access it.

The security attribute of a DPPI channel is configured in `DPPI[n].PERM (n=0..0)` on page 587. When the secure attribute is set for a channel, only peripherals that have the secure attribute set will be able to publish events to this channel or subscribe to this channel to receive tasks.

The DPPI controller peripheral (DPPIC) is a split security peripheral, i.e., its security behavior depends on the security attributes of both the DPPIC and the accessing party. See [Special considerations regarding the DPPIC configuration registers](#) on page 578 for more information about the DPPIC security behavior.

If a non-secure peripheral wants to publish an event on a secure DPPI channel, the channel will ignore the event. If a non-secure peripheral subscribes to a secure DPPI channel, it will not receive any events from this channel. The following figure illustrates the principle of operation of the security logic for a subscribed channel:

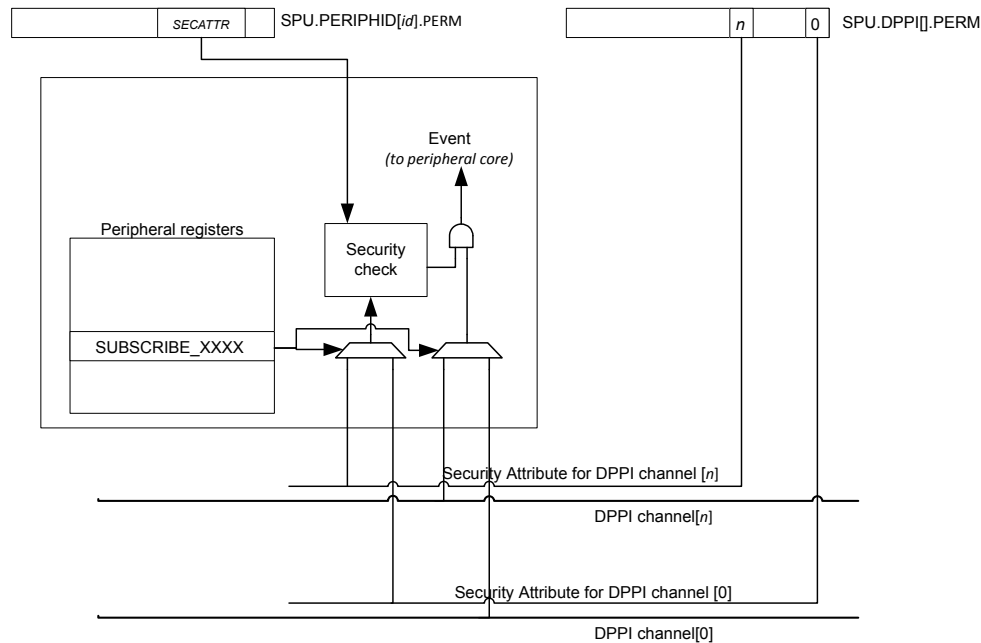


Figure 204: Subscribed channel security concept

No error reporting mechanism is associated with the DPPI access control logic.

#### 7.1.33.6.1 Special considerations regarding the DPPIC configuration registers

DPPI channels can be enabled, disabled and grouped through the DPPI controller (DPPIC). The DPPIC is a split-security peripheral, and handles both secure and non-secure accesses.

A non-secure peripheral access will only be able to configure and control DPPI channels defined as non-secure in SPU's `DPPI[n].PERM` register(s). A secure peripheral access can control all DPPI channels, independently of the configuration in the `DPPI[n].PERM` register(s).

The DPPIC allows the creation of group of channels to be able to enable or disable all channels within a group simultaneously. The security attribute of a group of channels (secure or non-secure) is defined as follows:

- If all channels (enabled or not) in the group are non-secure, then the group is considered non-secure
- If at least one of the channels (enabled or not) in the group is secure, then the group is considered secure

A non-secure access to a DPPIC register, or a bitfield controlling a channel marked as secure in `DPPI[n].PERM` register(s), will be ignored:

- Write accesses will have no effect
- Read will always return a zero value

No exceptions are thrown when a non-secure access targets a register or bitfield controlling a secure channel. For example, if the bit *i* is set in the `DPPI[n].PERM` register (declaring the DPPI channel *i* as secure), then:

- Non-secure write accesses to registers CHEN, CHENSET and CHENCLR will not be able to write to bit  $i$  of those registers
- Non-secure write accesses to registers TASK\_CHG[j].EN and TASK\_CHG[j].DIS will be ignored if the channel group  $j$  contains at least one channel defined as secure (it can be the channel  $i$  itself or any channel declared as secured)
- Non-secure read accesses to registers CHEN, CHENSET and CHENCLR will always read zero for the bit at position  $i$

For the channel configuration registers (DPPIC.CHG[n]), access from non-secure code is only possible if the included channels are all non-secure, whether the channels are enabled or not. If a DPPIC.CHG[g] register included one or more secure channels, then the group  $g$  is considered as secure and only a secure transfer can read or write DPPIC.CHG[g]. A non-secure write will be ignored and a non-secure read will return zero.

The DPPIC can subscribe to secure or non-secure channels through SUBSCRIBE\_CHG[n] registers in order to trigger task for enabling or disabling groups of channels. But an event from a non-secure channel will be ignored if the group subscribing to this channel is secure. An event from a secure channel can trigger both secure and non-secure tasks.

### 7.1.33.7 External domain access control

Other domains with their own CPUs can access peripherals, flash and RAM memories. The SPU allows controlling accesses from those bus masters.

The external domains can access application MCU memories and peripherals. External domains are assigned security attributes as described in register EXTDOMAIN[n].PERM.

| Domain      | Capability register                                         | Permission register                                   |
|-------------|-------------------------------------------------------------|-------------------------------------------------------|
| Network MCU | EXTDOMAIN[n].PERM (n=0..0) on page 586, SECUREMAPPING field | EXTDOMAIN[n].PERM (n=0..0) on page 586, SECATTR field |

Table 155: Register mapping for external domains

The figure below illustrates how the security control units are used to assign security attributes to transfers initiated by the external domains:

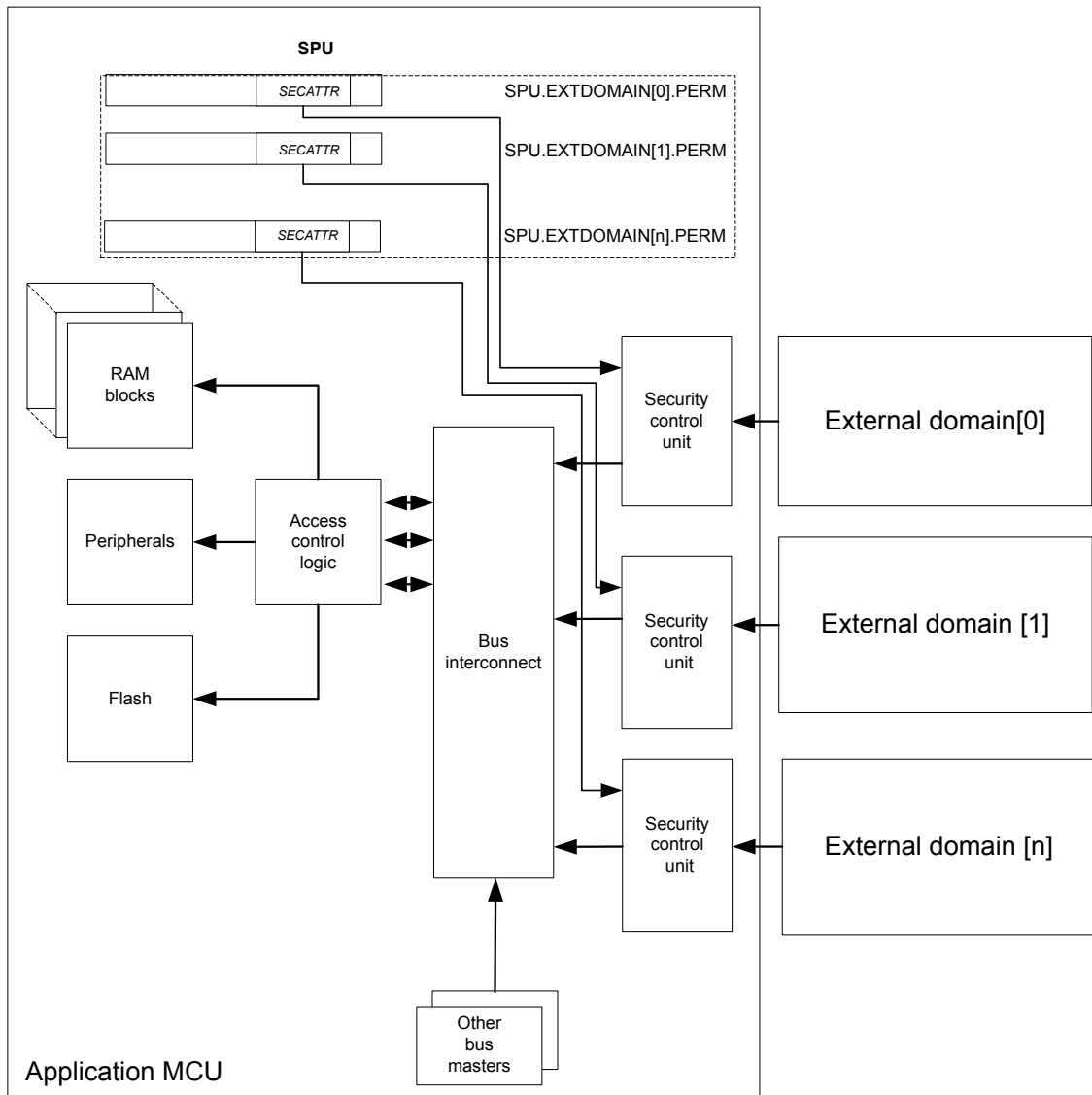


Figure 205: Access control from external domains

#### 7.1.33.8 TrustZone for Cortex-M ID allocation

Flash and RAM regions, as well as non-secure and secure peripherals, are assigned unique TrustZone IDs.

**Note:** TrustZone ID should not be confounded with the peripheral ID used to identify peripherals.

The table below shows the TrustZone ID allocation:



| Regions                | TrustZone Cortex-M ID |
|------------------------|-----------------------|
| Flash regions 0..63    | 0..63                 |
| RAM regions 0..63      | 64..127               |
| UICR                   | 252                   |
| FICR                   | 252                   |
| CACHEDATA              | 252                   |
| CACHEINFO              | 252                   |
| Non-secure peripherals | 253                   |
| Secure peripherals     | 254                   |

Table 156: TrustZone ID allocation

### 7.1.33.9 Registers

| Base address | Domain      | Peripheral | Instance | Secure mapping | DMA security | Description            | Configuration |
|--------------|-------------|------------|----------|----------------|--------------|------------------------|---------------|
| 0x50003000   | APPLICATION | SPU        | SPU      | S              | NA           | System protection unit |               |

Table 157: Instances

| Register             | Offset | Security | Description                                                                                              |
|----------------------|--------|----------|----------------------------------------------------------------------------------------------------------|
| EVENTS_RAMACCERR     | 0x100  |          | A security violation has been detected for the RAM memory space                                          |
| EVENTS_FLASHACCERR   | 0x104  |          | A security violation has been detected for the flash memory space                                        |
| EVENTS_PERIPHACCERR  | 0x108  |          | A security violation has been detected on one or several peripherals                                     |
| PUBLISH_RAMACCERR    | 0x180  |          | Publish configuration for event <a href="#">RAMACCERR</a>                                                |
| PUBLISH_FLASHACCERR  | 0x184  |          | Publish configuration for event <a href="#">FLASHACCERR</a>                                              |
| PUBLISH_PERIPHACCERR | 0x188  |          | Publish configuration for event <a href="#">PERIPHACCERR</a>                                             |
| INTEN                | 0x300  |          | Enable or disable interrupt                                                                              |
| INTENSET             | 0x304  |          | Enable interrupt                                                                                         |
| INTENCLR             | 0x308  |          | Disable interrupt                                                                                        |
| CAP                  | 0x400  |          | Show implemented features for the current device                                                         |
| CPULOCK              | 0x404  |          | Configure bits to lock down CPU features at runtime                                                      |
| EXTDOMAIN[n].PERM    | 0x440  |          | Access for bus access generated from the external domain n<br>List capabilities of the external domain n |
| DPPI[n].PERM         | 0x480  |          | Select between secure and non-secure attribute for the DPPI channels.                                    |
| DPPI[n].LOCK         | 0x484  |          | Prevent further modification of the corresponding PERM register                                          |
| GPIOPORT[n].PERM     | 0x4C0  |          | Select between secure and non-secure attribute for pins 0 to 31 of port n. Retained                      |
| GPIOPORT[n].LOCK     | 0x4C4  |          | Prevent further modification of the corresponding PERM register                                          |
| FLASHNSC[n].REGION   | 0x500  |          | Define which flash region can contain the non-secure callable (NSC) region n                             |
| FLASHNSC[n].SIZE     | 0x504  |          | Define the size of the non-secure callable (NSC) region n                                                |
| RAMNSC[n].REGION     | 0x540  |          | Define which RAM region can contain the non-secure callable (NSC) region n                               |
| RAMNSC[n].SIZE       | 0x544  |          | Define the size of the non-secure callable (NSC) region n                                                |
| FLASHREGION[n].PERM  | 0x600  |          | Access permissions for flash region n                                                                    |
| RAMREGION[n].PERM    | 0x700  |          | Access permissions for RAM region n                                                                      |
| PERIPHID[n].PERM     | 0x800  |          | List capabilities and access permissions for the peripheral with ID n                                    |

Table 158: Register overview

### 7.1.33.9.1 EVENTS\_RAMACCERR

Address offset: 0x100

A security violation has been detected for the RAM memory space

| Bit number       |            |                  | 31    | 30 | 29                                                              | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |
|------------------|------------|------------------|-------|----|-----------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|
| ID               |            |                  |       |    |                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |  |
| Reset 0x00000000 |            |                  | 0     | 0  | 0                                                               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |  |
| ID               | Acce Field | Value ID         | Value |    | Description                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |
| A                | RW         | EVENTS_RAMACCERR |       |    | A security violation has been detected for the RAM memory space |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | NotGenerated     | 0     |    | Event not generated                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | Generated        | 1     |    | Event generated                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |

### 7.1.33.9.2 EVENTS\_FLASHACCERR

Address offset: 0x104

A security violation has been detected for the flash memory space

| Bit number       |            |                    | 31    | 30 | 29                                                                | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |   |  |
|------------------|------------|--------------------|-------|----|-------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|---|--|
| ID               |            |                    |       |    |                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | A |  |
| Reset 0x00000000 |            |                    | 0     | 0  | 0                                                                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |   |  |
| ID               | Acce Field | Value ID           | Value |    | Description                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |  |
| A                | RW         | EVENTS_FLASHACCERR |       |    | A security violation has been detected for the flash memory space |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |  |
|                  |            | NotGenerated       | 0     |    | Event not generated                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |  |
|                  |            | Generated          | 1     |    | Event generated                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |  |

### 7.1.33.9.3 EVENTS\_PERIPHACCERR

Address offset: 0x108

A security violation has been detected on one or several peripherals

|                  |            |                     |       |                                                                      |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |
|------------------|------------|---------------------|-------|----------------------------------------------------------------------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|---|--|
| Bit number       |            |                     | 31    | 30                                                                   | 29          | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |   |  |
| ID               |            |                     |       |                                                                      |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  | A |  |
| Reset 0x00000000 |            |                     | 0     | 0                                                                    | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |   |  |
| ID               | Acce Field | Value ID            | Value |                                                                      | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |
| A                | RW         | EVENTS_PERIPHACCERR |       | A security violation has been detected on one or several peripherals |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |
|                  |            | NotGenerated        | 0     | Event not generated                                                  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |
|                  |            | Generated           | 1     | Event generated                                                      |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |

### 7.1.33.9.4 PUBLISH\_RAMACCERR

Address offset: 0x180

Publish configuration for event [RAMACCERR](#)

|                  |            |          |          |                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|---------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                                                            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |          |          | B                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |          | 0                                                             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce Field | Value ID | Value    | Description                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] | Channel that event <a href="#">RAMACCERR</a> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        | Disable publishing                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        | Enable publishing                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.33.9.5 PUBLISH\_FLASHACCERR

Address offset: 0x184

Publish configuration for event [FLASHACCERR](#)

|                  |            |  |          |          |                    |                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|----------|--------------------|--------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31       | 30                 | 29                                                     | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |  |          | B        |                    |                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |          | 0        | 0                  | 0                                                      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce Field |  | Value ID | Value    |                    | Description                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          | [255..0] |                    | Channel that event <b>FLASHACCERR</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |          |                    |                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled | 0        | Disable publishing |                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  | 1        | Enable publishing  |                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.33.9.6 PUBLISH\_PERIPHACCERR

Address offset: 0x188

Publish configuration for event [PERIPHACCERR](#)

|                  |            |          |          |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                                                               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |
| ID               |            |          |          | B                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |          | 0                                                                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |   |
| ID               | Acce Field | Value ID | Value    | Description                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] | Channel that event <a href="#">PERIPHACCERR</a> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        | Disable publishing                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        | Enable publishing                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.33.9.7 INTEN

Address offset: 0x300

Enable or disable interrupt

|                  |            |             |          |                                                                   |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-------------|----------|-------------------------------------------------------------------|----|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |             |          | 31                                                                | 30 | 29          | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |             |          |                                                                   |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | C | B | A |
| Reset 0x00000000 |            |             |          | 0                                                                 | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |
| ID               | Acce Field |             | Value ID | Value                                                             |    | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | RAMACCERR   |          | Enable or disable interrupt for event <a href="#">RAMACCERR</a>   |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled    | 0        | Disable                                                           |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled     | 1        | Enable                                                            |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW         | FLASHACCERR |          | Enable or disable interrupt for event <a href="#">FLASHACCERR</a> |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

| Bit number       |                 |                                                                    | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|-----------------|--------------------------------------------------------------------|---------------------------------------------------------------------------------------|-------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |                 |                                                                    | C B A                                                                                 |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |                 |                                                                    | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field      | Value ID                                                           | Value                                                                                 | Description |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW PERIPHACCERR | Disabled                                                           | 0                                                                                     | Disable     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                 | Enabled                                                            | 1                                                                                     | Enable      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                 | Enable or disable interrupt for event <a href="#">PERIPHACCERR</a> |                                                                                       |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                 | Disabled                                                           | 0                                                                                     | Disable     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                 | Enabled                                                            | 1                                                                                     | Enable      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.33.9.8 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number       |                 |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|-----------------|----------|---------------------------------------------------------------------------------------|------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |                 |          | C B A                                                                                 |                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |                 |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field      | Value ID | Value                                                                                 | Description                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW RAMACCERR    |          |                                                                                       | Write '1' to enable interrupt for event RAMACCERR    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                 | Set      | 1                                                                                     | Enable                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                 | Disabled | 0                                                                                     | Read: Disabled                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                 | Enabled  | 1                                                                                     | Read: Enabled                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW FLASHACCERR  |          |                                                                                       | Write '1' to enable interrupt for event FLASHACCERR  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                 | Set      | 1                                                                                     | Enable                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                 | Disabled | 0                                                                                     | Read: Disabled                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                 | Enabled  | 1                                                                                     | Read: Enabled                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW PERIPHACCERR |          |                                                                                       | Write '1' to enable interrupt for event PERIPHACCERR |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                 | Set      | 1                                                                                     | Enable                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                 | Disabled | 0                                                                                     | Read: Disabled                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                 | Enabled  | 1                                                                                     | Read: Enabled                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.33.9.9 INTENCLR

Address offset: 0x308

Disable interrupt

|                  |                 |          |                                                                                       |                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|-----------------|----------|---------------------------------------------------------------------------------------|-----------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |                 |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |                 |          | C B A                                                                                 |                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |                 |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field      | Value ID | Value                                                                                 | Description                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW RAMACCERR    |          |                                                                                       | Write '1' to disable interrupt for event <a href="#">RAMACCERR</a>    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                 | Clear    | 1                                                                                     | Disable                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                 | Disabled | 0                                                                                     | Read: Disabled                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                 | Enabled  | 1                                                                                     | Read: Enabled                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW FLASHACCERR  |          |                                                                                       | Write '1' to disable interrupt for event <a href="#">FLASHACCERR</a>  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                 | Clear    | 1                                                                                     | Disable                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                 | Disabled | 0                                                                                     | Read: Disabled                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                 | Enabled  | 1                                                                                     | Read: Enabled                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW PERIPHACCERR |          |                                                                                       | Write '1' to disable interrupt for event <a href="#">PERIPHACCERR</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

|                  |            |          |       |                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|-------|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |       | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |          |       |                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | C | B | A |   |
| Reset 0x00000000 |            |          |       | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID | Value | Description    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Clear    | 1     | Disable        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0     | Read: Disabled |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1     | Read: Enabled  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.33.9.10 CAP

Address offset: 0x400

Show implemented features for the current device

|                  |            |              |       |    |                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------------|-------|----|-------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |              | 31    | 30 | 29                                  | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |              | A     |    |                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000001 |            |              | 0     | 0  | 0                                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| ID               | Acce Field | Value ID     | Value |    | Description                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | R          | TZM          |       |    | Show ARM TrustZone status           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | NotAvailable | 0     |    | ARM TrustZone support not available |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled      | 1     |    | ARM TrustZone support is available  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.33.9.11 CPULOCK

Address offset: 0x404

Configure bits to lock down CPU features at runtime

Write '1' to any position to set the corresponding lock bit, which will remain set until the next reset

Any '0' writes to this register will be ignored

| Bit number       |      |              | 31       | 30 | 29    | 28                                                                                                                                                                                      | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
|------------------|------|--------------|----------|----|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| ID               |      |              |          |    |       |                                                                                                                                                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | E | D | C | B | A |
| Reset 0x00000000 |      |              | 0        | 0  | 0     | 0                                                                                                                                                                                       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce | Field        | Value    | ID | Value | Description                                                                                                                                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW   | LOCKSVTAIRCR |          |    |       | Write '1' to prevent updating the secure interrupt configuration until the next reset                                                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |              |          |    |       | When set to '1', this lock bit prevents changes to:                                                                                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |              |          |    |       | <ul style="list-style-type: none"><li>The Secure vector table base address</li><li>Handling of Secure interrupt priority</li><li>BusFault, HardFault, and NMI security target</li></ul> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |              | Locked   |    | 1     | Disables writes to the VTOR_S, AIRCR.PRIS, and AIRCR.BFHFNMINS registers                                                                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |              | Unlocked |    | 0     | These registers can be updated                                                                                                                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW   | LOCKNSVTOR   |          |    |       | Write '1' to prevent updating the non-secure vector table base address until the next reset                                                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |              |          |    |       | When set to '1', this lock bit prevents changes to the Non-secure interrupt vector table base address register VTOR_NS                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |              | Locked   |    | 1     | The address of the non-secure vector table is locked                                                                                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |              | Unlocked |    | 0     | The address of the non-secure vector table can be updated                                                                                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

| Bit number       |      |           | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |    |                                                                                                                                                                            |                                                                                                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|-----------|---------------------------------------------------------------------------------------|----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |      |           | E D C B A                                                                             |    |                                                                                                                                                                            |                                                                                                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |           | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |    |                                                                                                                                                                            |                                                                                                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field     | Value                                                                                 | ID | Value                                                                                                                                                                      | Description                                                                                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW   | LOCKSMPU  |                                                                                       |    |                                                                                                                                                                            | Write '1' to prevent updating the secure MPU regions until the next reset                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           |                                                                                       |    |                                                                                                                                                                            | When set to '1', this lock bit prevents changes to programmed Secure MPU memory regions and all writes to the registers are ignored                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Locked                                                                                | 1  | Disables writes to the MPU_CTRL, MPU_RNR, MPU_RBAR, MPU_RLAR, MPU_RBAR_An and MPU_RLAR_An from software or from a debug agent connected to the processor in Secure state   |                                                                                                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Unlocked                                                                              | 0  | These registers can be updated                                                                                                                                             |                                                                                                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| D                | RW   | LOCKNSMPU |                                                                                       |    |                                                                                                                                                                            | Write '1' to prevent updating the Non-secure MPU regions until the next reset                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           |                                                                                       |    |                                                                                                                                                                            | When set to '1', this lock bit prevents changes to programmed Non-secure MPU memory regions already programmed. All writes to the registers are ignored |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Locked                                                                                | 1  | Disables writes to the MPU_CTRL_NS, MPU_RNR_NS, MPU_RBAR_NS, MPU_RLAR_NS, MPU_RBAR_A_NSn and MPU_RLAR_A_NSn from software or from a debug agent connected to the processor |                                                                                                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Unlocked                                                                              | 0  | These registers can be updated                                                                                                                                             |                                                                                                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| E                | RW   | LOCKSAU   |                                                                                       |    |                                                                                                                                                                            | Write '1' to prevent updating the secure SAU regions until the next reset                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           |                                                                                       |    |                                                                                                                                                                            | When set to '1', this lock bit prevents changes to Secure SAU memory regions already programmed. All writes to the registers are ignored                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Locked                                                                                | 1  | Disables writes to the SAU_CTRL, SAU_RNR, SAU_RBAR and SAU_RLAR registers from software or from a debug agent connected to the processor                                   |                                                                                                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |           | Unlocked                                                                              | 0  | These registers can be updated                                                                                                                                             |                                                                                                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

#### 7.1.33.9.12 EXTDOMAIN[n].PERM (n=0..0)

Address offset:  $0x440 + (n \times 0x4)$

Access for bus access generated from the external domain n

List capabilities of the external domain n

| Bit number       |      |               | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                                                                                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |
|------------------|------|---------------|---------------------------------------------------------------------------------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|---|--|--|--|---|--|--|--|
| ID               |      |               |                                                                                       |       |                                                                                                                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | C |  |  |  | B |  |  |  | A |  |  |  |
| Reset 0x00000002 |      |               | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0           |       |                                                                                                                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |
| ID               | Acce | Field         | Value ID                                                                              | Value | Description                                                                                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |
| A                | R    | SECUREMAPPING |                                                                                       |       | Define configuration capabilities for TrustZone Cortex-M secure attribute                                                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |
|                  |      |               | NonSecure                                                                             | 0     | <div><b>Note:</b> This does not affect DPPI in the external domain</div> The bus access from this external domain always have the non-secure attribute set                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |
|                  |      |               | Secure                                                                                | 1     | The bus access from this external domain always have the secure attribute set                                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |
|                  |      |               | UserSelectable                                                                        | 2     | Non-secure or secure attribute for bus access from this domain is defined by the EXTDOMAIN[n].PERM register                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |
| B                | RW   | SECATTR       |                                                                                       |       | Peripheral security mapping                                                                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |
|                  |      |               | NonSecure                                                                             | 0     | <div><b>Note:</b> This bit has effect only if EXTDOMAIN[n].PERM.SECUREMAPPING reads as UserSelectable</div> Bus accesses from this domain have the non-secure attribute set |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |
|                  |      |               | Secure                                                                                | 1     | Bus accesses from this domain have secure attribute set                                                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |
| C                | RW   | LOCK          |                                                                                       |       |                                                                                                                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |
|                  |      |               | Unlocked                                                                              | 0     | This register can be updated                                                                                                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |
|                  |      |               | Locked                                                                                | 1     | The content of this register can't be changed until the next reset                                                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |

### 7.1.33.9.13 DPPI[n].PERM (n=0..0)

Address offset: 0x480 + (n × 0x8)

Select between secure and non-secure attribute for the DPPI channels.

|                  |            |                      |                                                                                       |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------------------|---------------------------------------------------------------------------------------|-------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |                      | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |                      | f e d c b a Z Y X W V U T S R Q P O N M L K J I H G F E D C B A                       |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0xFFFFFFFF |            |                      | 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1           |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID             | Value                                                                                 | Description                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A-f              | RW         | CHANNEL[i] (i=0..31) |                                                                                       | Select secure attribute.                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Secure               | 1                                                                                     | Channeli has its secure attribute set     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | NonSecure            | 0                                                                                     | Channeli has its non-secure attribute set |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.33.9.14 DPPI[n].LOCK (n=0..0)

Address offset: 0x484 + (n × 0x8)

Prevent further modification of the corresponding PERM register

|                  |            |  |          |       |    |                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |  |
|------------------|------------|--|----------|-------|----|---------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|---|--|
| Bit number       |            |  |          | 31    | 30 | 29                                                      | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |   |  |
| ID               |            |  |          |       |    |                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | A |  |
| Reset 0x00000000 |            |  |          | 0     | 0  | 0                                                       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |   |  |
| ID               | Acce Field |  | Value ID | Value |    | Description                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |  |
| A                | RW LOCK    |  |          |       |    |                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |  |
|                  |            |  | Locked   | 1     |    | DPPI[n].PERM register can't be changed until next reset |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |  |
|                  |            |  | Unlocked | 0     |    | DPPI[n].PERM register content can be changed            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |  |

#### 7.1.33.9.15 GPIOPORT[n].PERM (n=0..1) ( Retained )

Address offset:  $0x4C0 + (n \times 0x8)$

This register is a retained register

Select between secure and non-secure attribute for pins 0 to 31 of port n.

|                  |            |                  |       |                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|------------------|-------|----------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                  |       | 31                                           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |                  |       | f                                            | e  | d  | c  | b  | a  | Z  | Y  | X  | W  | V  | U  | T  | S  | R  | Q  | P  | O  | N  | M  | L  | K  | J | I | H | G | F | E | D | C | B | A |
| Reset 0xFFFFFFFF |            |                  |       | 1                                            | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ID               | Acce Field | Value ID         | Value | Description                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A-f              | RW         | PIN[i] (i=0..31) |       | Select secure attribute attribute for PIN i. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Secure           | 1     | Pin i has its secure attribute set           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | NonSecure        | 0     | Pin i has its non-secure attribute set       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 7.1.33.9.16 GPIOPORT[n].LOCK (n=0..1)

Address offset:  $0x4C4 + (n \times 0x8)$

Prevent further modification of the corresponding PERM register

|                  |      |       |          |                                                                                       |                                                             |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|-------|----------|---------------------------------------------------------------------------------------|-------------------------------------------------------------|-------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |       |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                             |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |       |          | A                                                                                     |                                                             |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |       |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                     |                                                             |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field | Value    | ID                                                                                    | Value                                                       | Description |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW   | LOCK  |          |                                                                                       |                                                             |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Locked   | 1                                                                                     | GPIOPORT[n].PERM register can't be changed until next reset |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Unlocked | 0                                                                                     | GPIOPORT[n].PERM register content can be changed            |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

#### 7.1.33.9.17 FLASHNSC[n].REGION (n=0..1)

Address offset:  $0x500 + (n \times 0x8)$

Define which flash region can contain the non-secure callable (NSC) region n

|                  |            |          |       |                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|-------|--------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |       | 31                                                                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |          |       |                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | B |   | A |   | A | A | A | A | A |
| Reset 0x00000000 |            |          |       | 0                                                                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |
| ID               | Acce Field | Value ID | Value | Description                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | REGION   |       | Region number                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW         | LOCK     |       |                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Unlocked | 0     | This register can be updated                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Locked   | 1     | The content of this register can't be changed until the next reset |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |



Define the size of the non-secure callable (NSC) region  $n$

#### 7.1.33.9.19 RAMNSC[n].REGION (n=0..1)

Define which RAM region can contain the non-secure callable (NSC) region n

#### 7.1.33.9.20 RAMNSC[n].SIZE (n=0..1)

Define the size of the non-secure callable (NSC) region  $n$

| Bit number       |      |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                                                                                                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |   |   |
|------------------|------|-------|---------------------------------------------------------------------------------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|---|--|--|--|---|---|---|
| ID               |      |       |                                                                                       |       |                                                                                                                                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | B |  |  |  | A |  |  |  | A | A | A |
| Reset 0x00000000 |      |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |       |                                                                                                                                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |   |   |
| ID               | Acce | Field | Value ID                                                                              | Value | Description                                                                                                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |   |   |
| A                | RW   | SIZE  | Disabled                                                                              | 0     | Size of the non-secure callable (NSC) region n<br>The region n is not defined as a non-secure callable region.<br>Normal security attributes (secure or non-secure) are enforced. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |   |   |
|                  |      |       | 32                                                                                    | 1     | The region n is defined as non-secure callable with a 32-byte size                                                                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |   |   |
|                  |      |       | 64                                                                                    | 2     | The region n is defined as non-secure callable with a 64-byte size                                                                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |   |   |
|                  |      |       | 128                                                                                   | 3     | The region n is defined as non-secure callable with a 128-byte size                                                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |   |   |
|                  |      |       | 256                                                                                   | 4     | The region n is defined as non-secure callable with a 256-byte size                                                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |   |   |
|                  |      |       | 512                                                                                   | 5     | The region n is defined as non-secure callable with a 512-byte size                                                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |   |   |
|                  |      |       | 1024                                                                                  | 6     | The region n is defined as non-secure callable with a 1024-byte size                                                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |   |   |
|                  |      |       | 2048                                                                                  | 7     | The region n is defined as non-secure callable with a 2048-byte size                                                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |   |   |
|                  |      |       | 4096                                                                                  | 8     | The region n is defined as non-secure callable with a 4096-byte size                                                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |   |   |
|                  |      |       |                                                                                       |       |                                                                                                                                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |   |   |
| B                | RW   | LOCK  | Unlocked                                                                              | 0     | This register can be updated                                                                                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |   |   |
|                  |      |       | Locked                                                                                | 1     | The content of this register can't be changed until the next reset                                                                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |   |   |   |

### 7.1.33.9.21 FLASHREGION[n].PERM (n=0..63)

Address offset:  $0x600 + (n \times 0x4)$

Access permissions for flash region n

| Bit number       |            |            | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |       |  |  |  |
|------------------|------------|------------|---------------------------------------------------------------------------------------|-------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|---|--|--|--|-------|--|--|--|
| ID               |            |            |                                                                                       |                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | E |  |  |  | D |  |  |  | C B A |  |  |  |
| Reset 0x00000017 |            |            | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 1 1             |                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |       |  |  |  |
| ID               | Acce Field | Value ID   | Value                                                                                 | Description                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |       |  |  |  |
| A                | RW EXECUTE |            |                                                                                       | Configure instruction fetch permissions from flash region n |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |       |  |  |  |
|                  |            | Enable     | 1                                                                                     | Allow instruction fetches from flash region n               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |       |  |  |  |
|                  |            | Disable    | 0                                                                                     | Block instruction fetches from flash region n               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |       |  |  |  |
| B                | RW WRITE   |            |                                                                                       | Configure write permission for flash region n               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |       |  |  |  |
|                  |            | Enable     | 1                                                                                     | Allow write operation to region n                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |       |  |  |  |
|                  |            | Disable    | 0                                                                                     | Block write operation to region n                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |       |  |  |  |
| C                | RW READ    |            |                                                                                       | Configure read permissions for flash region n               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |       |  |  |  |
|                  |            | Enable     | 1                                                                                     | Allow read operation from flash region n                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |       |  |  |  |
|                  |            | Disable    | 0                                                                                     | Block read operation from flash region n                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |       |  |  |  |
| D                | RW SECATTR |            |                                                                                       | Security attribute for flash region n                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |       |  |  |  |
|                  |            | Non_Secure | 0                                                                                     | Flash region n security attribute is non-secure             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |       |  |  |  |
|                  |            | Secure     | 1                                                                                     | Flash region n security attribute is secure                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |       |  |  |  |
| E                | RW LOCK    |            |                                                                                       |                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |       |  |  |  |
|                  |            | Unlocked   | 0                                                                                     | This register can be updated                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |   |  |  |  |       |  |  |  |

|                  |            |          |       |    |                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |
|------------------|------------|----------|-------|----|--------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|--|--|
| Bit number       |            |          | 31    | 30 | 29                                                                 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |  |  |
| ID               |            |          |       |    |                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | E |   |   |   | D |   | C |   | B | A |  |  |
| Reset 0x00000017 |            |          | 0     | 0  | 0                                                                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |   |  |  |
| ID               | Acce Field | Value ID | Value |    | Description                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            | Locked   | 1     |    | The content of this register can't be changed until the next reset |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |  |

### 7.1.33.9.22 RAMREGION[n].PERM (n=0..63)

Address offset:  $0x700 + (n \times 0x4)$

Access permissions for RAM region n

| Bit number       |      |         | 31                                                                      | 30 | 29                                                                 | 28                                                        | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |   |  |  |   |  |  |
|------------------|------|---------|-------------------------------------------------------------------------|----|--------------------------------------------------------------------|-----------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|---|--|--|---|--|--|
| ID               |      |         |                                                                         |    |                                                                    |                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | E |   |   | D |   |   | C |   |  | B |  |  | A |  |  |
| Reset 0x00000017 |      |         | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 1 1 |    |                                                                    |                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |   |  |  |   |  |  |
| ID               | Acce | Field   | Value                                                                   | ID | Value                                                              | Description                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |   |  |  |   |  |  |
| A                | RW   | EXECUTE |                                                                         |    |                                                                    | Configure instruction fetch permissions from RAM region n |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |   |  |  |   |  |  |
|                  |      |         | Enable                                                                  | 1  | Allow instruction fetches from RAM region n                        |                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |   |  |  |   |  |  |
|                  |      |         | Disable                                                                 | 0  | Block instruction fetches from RAM region n                        |                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |   |  |  |   |  |  |
| B                | RW   | WRITE   |                                                                         |    |                                                                    | Configure write permission for RAM region n               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |   |  |  |   |  |  |
|                  |      |         | Enable                                                                  | 1  | Allow write operation to RAM region n                              |                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |   |  |  |   |  |  |
|                  |      |         | Disable                                                                 | 0  | Block write operation to RAM region n                              |                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |   |  |  |   |  |  |
| C                | RW   | READ    |                                                                         |    |                                                                    | Configure read permissions for RAM region n               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |   |  |  |   |  |  |
|                  |      |         | Enable                                                                  | 1  | Allow read operation from RAM region n                             |                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |   |  |  |   |  |  |
|                  |      |         | Disable                                                                 | 0  | Block read operation from RAM region n                             |                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |   |  |  |   |  |  |
| D                | RW   | SECATTR |                                                                         |    |                                                                    | Security attribute for RAM region n                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |   |  |  |   |  |  |
|                  |      |         | Non_Secure                                                              | 0  | RAM region n security attribute is non-secure                      |                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |   |  |  |   |  |  |
|                  |      |         | Secure                                                                  | 1  | RAM region n security attribute is secure                          |                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |   |  |  |   |  |  |
| E                | RW   | LOCK    |                                                                         |    |                                                                    |                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |   |  |  |   |  |  |
|                  |      |         | Unlocked                                                                | 0  | This register can be updated                                       |                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |   |  |  |   |  |  |
|                  |      |         | Locked                                                                  | 1  | The content of this register can't be changed until the next reset |                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |   |  |  |   |  |  |

### 7.1.33.9.23 PERIPHID[n].PERM (n=0..255)

Address offset:  $0x800 + (n \times 0x4)$

List capabilities and access permissions for the peripheral with ID n

Reset values are unique per peripheral instantiation. Please refer to the peripheral instantiation table.  
Entries not listed in the instantiation table are undefined.

|                  |      |               |                |    |    |                                                                                                |    |                                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------|---------------|----------------|----|----|------------------------------------------------------------------------------------------------|----|---------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |      |               | 31             | 30 | 29 | 28                                                                                             | 27 | 26                                                                        | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |      |               | F              |    |    |                                                                                                |    |                                                                           |    |    |    |    | E  |    |    |    |    |    |    |    |    |    | D  |    |   |   |   |   |   |   | C | B | B | A | A |
| Reset 0x00000012 |      |               | 0              | 0  | 0  | 0                                                                                              | 0  | 0                                                                         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| ID               | Acce | Field         | Value          |    | ID | Value                                                                                          |    | Description                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | R    | SECUREMAPPING |                |    |    |                                                                                                |    | Define configuration capabilities for TrustZone Cortex-M secure attribute |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |               | NonSecure      |    | 0  | This peripheral is always accessible as a non-secure peripheral                                |    |                                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |               | Secure         |    | 1  | This peripheral is always accessible as a secure peripheral                                    |    |                                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |               | UserSelectable |    | 2  | Non-secure or secure attribute for this peripheral is defined by the PERIPHID[n].PERM register |    |                                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.34 SWI — Software interrupts



**NORDIC**<sup>®</sup>  
SEMICONDUCTOR

### 7.1.34.1 Registers

| Base address | Domain  | Peripheral | Instance | Secure mapping | DMA security | Description          | Configuration |
|--------------|---------|------------|----------|----------------|--------------|----------------------|---------------|
| 0x4101A000   | NETWORK | SWI        | SWI0     | NS             | NA           | Software interrupt 0 |               |
| 0x4101B000   | NETWORK | SWI        | SWI1     | NS             | NA           | Software interrupt 1 |               |
| 0x4101C000   | NETWORK | SWI        | SWI2     | NS             | NA           | Software interrupt 2 |               |
| 0x4101D000   | NETWORK | SWI        | SWI3     | NS             | NA           | Software interrupt 3 |               |

Table 159: Instances

## 7.1.35 TEMP — Temperature sensor

The temperature sensor measures die temperature over the temperature range of the device. Linearity compensation can be implemented if required by the application.

Listed here are the main features for TEMP:

- Temperature range is greater than or equal to operating temperature of the device
- Resolution is 0.25 degrees

TEMP is started by triggering the START task.

When the temperature measurement is completed, a DATARDY event will be generated and the result of the measurement can be read from the TEMP register.

To achieve the measurement accuracy stated in the electrical specification, the crystal oscillator must be selected as the HFCLK source, see [CLOCK — Clock control](#) on page 61 for more information.

When the temperature measurement is completed, TEMP analog electronics power down to save power.

TEMP only supports one-shot operation, meaning that every TEMP measurement has to be explicitly started using the START task.

### 7.1.35.1 Registers

| Base address | Domain  | Peripheral | Instance | Secure mapping | DMA security | Description        | Configuration |
|--------------|---------|------------|----------|----------------|--------------|--------------------|---------------|
| 0x41010000   | NETWORK | TEMP       | TEMP     | NS             | NA           | Temperature sensor |               |

Table 160: Instances

| Register        | Offset | Security | Description                                             |
|-----------------|--------|----------|---------------------------------------------------------|
| TASKS_START     | 0x000  |          | Start temperature measurement                           |
| TASKS_STOP      | 0x004  |          | Stop temperature measurement                            |
| SUBSCRIBE_START | 0x080  |          | Subscribe configuration for task <a href="#">START</a>  |
| SUBSCRIBE_STOP  | 0x084  |          | Subscribe configuration for task <a href="#">STOP</a>   |
| EVENTS_DATARDY  | 0x100  |          | Temperature measurement complete, data ready            |
| PUBLISH_DATARDY | 0x180  |          | Publish configuration for event <a href="#">DATARDY</a> |
| INTENSET        | 0x304  |          | Enable interrupt                                        |
| INTENCLR        | 0x308  |          | Disable interrupt                                       |
| TEMP            | 0x508  |          | Temperature in °C (0.25° steps)                         |
| A0              | 0x520  |          | Slope of 1st piece wise linear function                 |
| A1              | 0x524  |          | Slope of 2nd piece wise linear function                 |
| A2              | 0x528  |          | Slope of 3rd piece wise linear function                 |
| A3              | 0x52C  |          | Slope of 4th piece wise linear function                 |
| A4              | 0x530  |          | Slope of 5th piece wise linear function                 |

| Register | Offset | Security | Description                                   |
|----------|--------|----------|-----------------------------------------------|
| A5       | 0x534  |          | Slope of 6th piece wise linear function       |
| B0       | 0x540  |          | y-intercept of 1st piece wise linear function |
| B1       | 0x544  |          | y-intercept of 2nd piece wise linear function |
| B2       | 0x548  |          | y-intercept of 3rd piece wise linear function |
| B3       | 0x54C  |          | y-intercept of 4th piece wise linear function |
| B4       | 0x550  |          | y-intercept of 5th piece wise linear function |
| B5       | 0x554  |          | y-intercept of 6th piece wise linear function |
| T0       | 0x560  |          | End point of 1st piece wise linear function   |
| T1       | 0x564  |          | End point of 2nd piece wise linear function   |
| T2       | 0x568  |          | End point of 3rd piece wise linear function   |
| T3       | 0x56C  |          | End point of 4th piece wise linear function   |
| T4       | 0x570  |          | End point of 5th piece wise linear function   |

Table 161: Register overview

#### 7.1.35.1.1 TASKS\_START

Address offset: 0x000

Start temperature measurement

|                  |            |             |       |                                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-------------|-------|-------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |             |       | 31                                                                      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |             |       | A                                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |             |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field | Value ID    | Value | Description                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_START |       | Start temperature measurement                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Trigger     | 1     | Trigger task                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.35.1.2 TASKS\_STOP

Address offset: 0x004

### Stop temperature measurement

|                  |            |            |          |   |       |  |  |  |                              |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|------------|----------|---|-------|--|--|--|------------------------------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |            |          |   |       |  |  |  |                              | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |            |          |   |       |  |  |  |                              |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |   |
| Reset 0x00000000 |            |            |          |   |       |  |  |  |                              | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |            | Value ID |   | Value |  |  |  |                              | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_STOP |          |   |       |  |  |  | Stop temperature measurement |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Trigger    |          | 1 |       |  |  |  | Trigger task                 |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.35.1.3 SUBSCRIBE\_START

Address offset: 0x080

## Subscribe configuration for task **START**

|                  |            |          |          |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|--------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                                               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |          |          | B                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |          | 0                                                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce Field | Value ID | Value    | Description                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] | Channel that task <b>START</b> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        | Disable subscription                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        | Enable subscription                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.35.1.4 SUBSCRIBE\_STOP

Address offset: 0x084

Subscribe configuration for task **STOP**

|                  |            |          |          |                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|-------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                                                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |          |          | B                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |          | 0                                                     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce Field | Value ID | Value    | Description                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] | Channel that task <span>STOP</span> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        | Disable subscription                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        | Enable subscription                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.35.1.5 EVENTS\_DATARDY

Address offset: 0x100

Temperature measurement complete, data ready

|                  |            |                |       |                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |
|------------------|------------|----------------|-------|----------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|
| Bit number       |            |                |       | 31                                           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |
| ID               |            |                |       |                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |  |
| Reset 0x00000000 |            |                |       | 0                                            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |
| ID               | Acce Field | Value ID       | Value | Description                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |
| A                | RW         | EVENTS_DATARDY |       | Temperature measurement complete, data ready |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | NotGenerated   | 0     | Event not generated                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | Generated      | 1     | Event generated                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |

#### 7.1.35.1.6 PUBLISH\_DATARDY

Address offset: 0x180

Publish configuration for event **DATARDY**

|                  |            |  |  |          |    |          |    |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|--|----------|----|----------|----|----------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |  | 31       | 30 | 29       | 28 | 27                                                 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |  |  | B        |    |          |    |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   |   |   |   |   |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |  | 0        |    |          |    |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  |  | Value ID |    | Value    |    | Description                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |  |          |    | [255..0] |    | Channel that event <b>DATARDY</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |  |          |    |          |    |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  |  | Disabled |    | 0        |    | Disable publishing                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  |  | Enabled  |    | 1        |    | Enable publishing                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.35.1.7 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number       |      |         |          | 31    | 30 | 29                                                              | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |
|------------------|------|---------|----------|-------|----|-----------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|--|
| ID               |      |         |          | A     |    |                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| Reset 0x00000000 |      |         |          | 0     | 0  | 0                                                               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |  |
| ID               | Acce | Field   | Value ID | Value |    | Description                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| A                | RW   | DATARDY |          |       |    | Write '1' to enable interrupt for event <a href="#">DATARDY</a> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |      |         | Set      | 1     |    | Enable                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |      |         | Disabled | 0     |    | Read: Disabled                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |      |         | Enabled  | 1     |    | Read: Enabled                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |

### 7.1.35.1.8 INTENCLR

Address offset: 0x308

Disable interrupt

|                  |            |          |                                                                                       |                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|--------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          | A                                                                                     |                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW DATARDY |          |                                                                                       | Write '1' to disable interrupt for event DATARDY |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Clear    | 1                                                                                     | Disable                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Read: Disabled                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Read: Enabled                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.35.1.9 TEMP

Address offset: 0x508

Temperature in °C (0.25° steps)

|            |  |  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              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| Bit number |  |  | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               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| ID         |  |  | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A 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### 7.1.35.1.10 A0

Address offset: 0x520

Slope of 1st piece wise linear function



|                  |            |  |          |       |    |    |    |                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|-------|----|----|----|-----------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31    | 30 | 29 | 28 | 27                                      | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |  |          |       |    |    |    |                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| Reset 0x000002D9 |            |  |          | 0     | 0  | 0  | 0  | 0                                       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field |  | Value ID | Value |    |    |    | Description                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW A0      |  |          |       |    |    |    | Slope of 1st piece wise linear function |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.35.1.11 A1

Address offset: 0x524

Slope of 2nd piece wise linear function

|                  |            |  |          |       |    |    |    |                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|-------|----|----|----|-----------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31    | 30 | 29 | 28 | 27                                      | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |
| ID               |            |  |          |       |    |    |    |                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000322 |            |  |          | 0     | 0  | 0  | 0  | 0                                       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field |  | Value ID | Value |    |    |    | Description                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW A1      |  |          |       |    |    |    | Slope of 2nd piece wise linear function |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.35.1.12 A2

Address offset: 0x528

Slope of 3rd piece wise linear function

|                  |            |  |          |       |    |                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|-------|----|-----------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31    | 30 | 29                                      | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |  |          |       |    |                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000355 |            |  |          | 0     | 0  | 0                                       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field |  | Value ID | Value |    | Description                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW A2      |  |          |       |    | Slope of 3rd piece wise linear function |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.35.1.13 A3

Address offset: 0x52C

Slope of 4th piece wise linear function

|                  |            |  |          |                                         |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|-----------------------------------------|----|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31                                      | 30 | 29          | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |  |          |                                         |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| Reset 0x000003DF |            |  |          | 0                                       | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field |  | Value ID | Value                                   |    | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW A3      |  |          | Slope of 4th piece wise linear function |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.35.1.14 A4

Address offset: 0x530

Slope of 5th piece wise linear function

|                  |  |  |  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            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| Bit number       |  |  |  | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      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| ID               |  |  |  | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                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### 7.1.35.1.15 A5

Address offset: 0x534

Slope of 6th piece wise linear function

|                  |            |  |          |                                         |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|-----------------------------------------|----|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31                                      | 30 | 29          | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |  |          |                                         |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| Reset 0x000004B7 |            |  |          | 0                                       | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field |  | Value ID | Value                                   |    | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW A5      |  |          | Slope of 6th piece wise linear function |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.35.1.16 B0

Address offset: 0x540

y-intercept of 1st piece wise linear function

|                  |            |  |  |          |    |       |    |                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|--|----------|----|-------|----|-----------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |  | 31       | 30 | 29    | 28 | 27                                            | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |  |  |          |    |       |    |                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000FC7 |            |  |  | 0        | 0  | 0     | 0  | 0                                             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field |  |  | Value ID |    | Value |    | Description                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW B0      |  |  |          |    |       |    | y-intercept of 1st piece wise linear function |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.35.1.17 B1

Address offset: 0x544

y-intercept of 2nd piece wise linear function

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| Bit number       |  |  |  | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      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### 7.1.35.1.18 B2

Address offset: 0x548

y-intercept of 3rd piece wise linear function

|                  |            |  |  |          |    |       |    |                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|--|----------|----|-------|----|-----------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |  | 31       | 30 | 29    | 28 | 27                                            | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |  |  |          |    |       |    |                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000F6C |            |  |  | 0        | 0  | 0     | 0  | 0                                             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field |  |  | Value ID |    | Value |    | Description                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW B2      |  |  |          |    |       |    | y-intercept of 3rd piece wise linear function |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.35.1.19 B3

Address offset: 0x54C

y-intercept of 4th piece wise linear function

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### 7.1.35.1.20 B4

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### 7.1.35.1.22 T0

Address offset: 0x560

End point of 1st piece wise linear function

|                  |            |  |          |  |       |  |                                             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|--|-------|--|---------------------------------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          |  |       |  |                                             |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |
| ID               |            |  |          |  |       |  |                                             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  |    |   |   |   |   |   |   |   |   | A | A | A | A | A | A | A |   |   |   |   |
| Reset 0x000000E1 |            |  |          |  |       |  |                                             |  |  | 0  |    |    |    |    |    |    |    |    |    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| ID               | Acce Field |  | Value ID |  | Value |  | Description                                 |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         |  | T0       |  |       |  | End point of 1st piece wise linear function |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.35.1.23 T1

Address offset: 0x564

End point of 2nd piece wise linear function

|            |  |  |  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  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| Bit number |  |  |  | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            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### 7.1.35.1.25 T3

Address offset: 0x56C

End point of 4th piece wise linear function

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| A                | RW   | T3    |       | End point of 4th piece wise linear function |       |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.35.1.26 T4

Address offset: 0x570

End point of 5th piece wise linear function

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## 7.1.35.2 Electrical specification

### 7.1.35.2.1 Temperature Sensor Electrical Specification

| Symbol                  | Description                                               | Min. | Typ. | Max. | Units |
|-------------------------|-----------------------------------------------------------|------|------|------|-------|
| t <sub>TEMP</sub>       | Time required for temperature measurement                 | ..   | ..   | ..   | µs    |
| T <sub>TEMP,RANGE</sub> | Temperature sensor range                                  | ..   | ..   | ..   | °C    |
| T <sub>TEMP,ACC</sub>   | Temperature sensor accuracy                               | ..   | ..   | ..   | °C    |
| T <sub>TEMP,RES</sub>   | Temperature sensor resolution                             | ..   | ..   | ..   | °C    |
| T <sub>TEMP,STB</sub>   | Sample to sample stability at constant device temperature | ..   | ..   | ..   | °C    |
| T <sub>TEMP,OFFST</sub> | Sample offset at 25°C                                     | ..   | ..   | ..   | °C    |

## 7.1.36 TIMER — Timer/counter

The TIMER can operate in two modes: timer and counter.

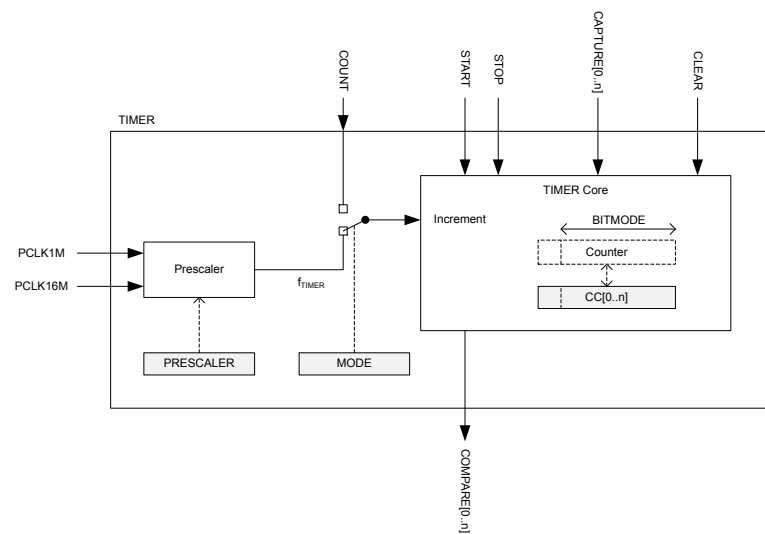


Figure 206: Block schematic for timer/counter

The timer/counter runs on the high-frequency clock source (HFCLK) and includes a four-bit (1/2X) prescaler that can divide the timer input clock from the HFCLK controller. Clock source selection between PCLK16M and PCLK1M is automatic according to TIMER base frequency set by the prescaler. The TIMER base frequency is always given as 16 MHz divided by the prescaler value.

The PPI system allows a TIMER event to trigger a task of any other system peripheral of the device. The PPI system also enables the TIMER task/event features to generate periodic output and PWM signals to any GPIO. The number of input/outputs used at the same time is limited by the number of GPIOTE channels.

The TIMER can operate in two modes, Timer mode and Counter mode. In both modes, the TIMER is started by triggering the START task, and stopped by triggering the STOP task. After the timer is stopped the timer can resume timing/counting by triggering the START task again. When timing/counting is resumed, the timer will continue from the value it had prior to being stopped.

In Timer mode, the TIMER's internal Counter register is incremented by one for every tick of the timer frequency  $f_{\text{TIMER}}$  as illustrated in [Figure 206: Block schematic for timer/counter](#) on page 601. The timer frequency is derived from PCLK16M as shown below, using the values specified in the PRESCALER register:

$$f_{\text{TIMER}} = 16 \text{ MHz} / (2^{\text{PRESCALER}})$$

When  $f_{\text{TIMER}} \leq 1 \text{ MHz}$  the TIMER will use PCLK1M instead of PCLK16M for reduced power consumption.

In counter mode, the TIMER's internal Counter register is incremented by one each time the COUNT task is triggered, that is, the timer frequency and the prescaler are not utilized in counter mode. Similarly, the COUNT task has no effect in Timer mode.

The TIMER's maximum value is configured by changing the bit-width of the timer in the [BITMODE](#) on page 609 register.

[PRESCALER](#) on page 609 and the [BITMODE](#) on page 609 must only be updated when the timer is stopped. If these registers are updated while the TIMER is started then this may result in unpredictable behavior.

When the timer is incremented beyond its maximum value the Counter register will overflow and the TIMER will automatically start over from zero.

The Counter register can be cleared, that is, its internal value set to zero explicitly, by triggering the CLEAR task.

The TIMER implements multiple capture/compare registers.

Independent of prescaler setting the accuracy of the TIMER is equivalent to one tick of the timer frequency  $f_{\text{TIMER}}$  as illustrated in [Figure 206: Block schematic for timer/counter](#) on page 601.

### 7.1.36.1 Capture

The TIMER implements one capture task for every available capture/compare register.

Every time the CAPTURE[n] task is triggered, the Counter value is copied to the CC[n] register.

### 7.1.36.2 Compare

The TIMER implements one COMPARE event for every available capture/compare register.

A COMPARE event is generated when the Counter is incremented and then becomes equal to the value specified in one of the capture compare registers. When the Counter value becomes equal to the value specified in a capture compare register CC[n], the corresponding compare event COMPARE[n] is generated.

**BITMODE** on page 609 specifies how many bits of the Counter register and the capture/compare register that are used when the comparison is performed. Other bits will be ignored.

The COMPARE event can be configured to operate in one-shot mode, by configuring the corresponding ONESHOTEN[n] register. When enabled, the COMPARE[n] event is generated only once after a write to CC[n].

### 7.1.36.3 Task delays

After the TIMER is started, the CLEAR task, COUNT task and the STOP task will guarantee to take effect within one clock cycle of the PCLK16M.

### 7.1.36.4 Task priority

If the START task and the STOP task are triggered at the same time, that is, within the same period of PCLK16M, the STOP task will be prioritized.

If one or more of the CAPTURE tasks and the CLEAR task is triggered at the same time, that is, within the same period of PCLK16M, the CAPTURE tasks will be prioritized. This means that the CC registers will capture the Counter value before the CLEAR task is triggered.

## 7.1.36.5 Registers

| Base address             | Domain      | Peripheral | Instance    | Secure mapping | DMA security | Description | Configuration                          |
|--------------------------|-------------|------------|-------------|----------------|--------------|-------------|----------------------------------------|
| 0x5000F000<br>0x4000F000 | APPLICATION | TIMER      | TIMER0 : S  | US             | NA           | Timer 0     |                                        |
|                          |             |            | TIMER0 : NS |                |              |             |                                        |
| 0x50010000<br>0x40010000 | APPLICATION | TIMER      | TIMER1 : S  | US             | NA           | Timer 1     |                                        |
|                          |             |            | TIMER1 : NS |                |              |             |                                        |
| 0x50011000<br>0x40011000 | APPLICATION | TIMER      | TIMER2 : S  | US             | NA           | Timer 2     |                                        |
|                          |             |            | TIMER2 : NS |                |              |             |                                        |
| 0x4100C000               | NETWORK     | TIMER      | TIMER0      | NS             | NA           | Timer 0     | 8 capture compare channels implemented |
| 0x41018000               | NETWORK     | TIMER      | TIMER1      | NS             | NA           | Timer 1     | 8 capture compare channels implemented |
| 0x41019000               | NETWORK     | TIMER      | TIMER2      | NS             | NA           | Timer 2     | 8 capture compare channels implemented |

Table 162: Instances

| Register             | Offset | Security | Description                                                                       |
|----------------------|--------|----------|-----------------------------------------------------------------------------------|
| TASKS_START          | 0x000  |          | Start Timer                                                                       |
| TASKS_STOP           | 0x004  |          | Stop Timer                                                                        |
| TASKS_COUNT          | 0x008  |          | Increment Timer (Counter mode only)                                               |
| TASKS_CLEAR          | 0x00C  |          | Clear time                                                                        |
| TASKS_SHUTDOWN       | 0x010  |          | Shut down timer <span>Deprecated</span>                                           |
| TASKS_CAPTURE[n]     | 0x040  |          | Capture Timer value to CC[n] register                                             |
| SUBSCRIBE_START      | 0x080  |          | Subscribe configuration for task <a href="#">START</a>                            |
| SUBSCRIBE_STOP       | 0x084  |          | Subscribe configuration for task <a href="#">STOP</a>                             |
| SUBSCRIBE_COUNT      | 0x088  |          | Subscribe configuration for task <a href="#">COUNT</a>                            |
| SUBSCRIBE_CLEAR      | 0x08C  |          | Subscribe configuration for task <a href="#">CLEAR</a>                            |
| SUBSCRIBE_SHUTDOWN   | 0x090  |          | Subscribe configuration for task <a href="#">SHUTDOWN</a> <span>Deprecated</span> |
| SUBSCRIBE_CAPTURE[n] | 0x0C0  |          | Subscribe configuration for task <a href="#">CAPTURE[n]</a>                       |
| EVENTS_COMPARE[n]    | 0x140  |          | Compare event on CC[n] match                                                      |
| PUBLISH_COMPARE[n]   | 0x1C0  |          | Publish configuration for event <a href="#">COMPARE[n]</a>                        |
| SHORTS               | 0x200  |          | Shortcuts between local events and tasks                                          |
| INTEN                | 0x300  |          | Enable or disable interrupt                                                       |
| INTENSET             | 0x304  |          | Enable interrupt                                                                  |
| INTENCLR             | 0x308  |          | Disable interrupt                                                                 |
| MODE                 | 0x504  |          | Timer mode selection                                                              |
| BITMODE              | 0x508  |          | Configure the number of bits used by the TIMER                                    |
| PRESCALER            | 0x510  |          | Timer prescaler register                                                          |
| CC[n]                | 0x540  |          | Capture/Compare register n                                                        |
| ONESHOTEN[n]         | 0x580  |          | Enable one-shot operation for Capture/Compare channel n                           |

Table 163: Register overview

### 7.1.36.5.1 TASKS\_START

Address offset: 0x000

Start Timer

|                  |            |             |       |                                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-------------|-------|---------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |             |       | 31                                                                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |             |       | A                                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |             |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field | Value ID    | Value | Description                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_START |       | Start Timer                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Trigger     | 1     | Trigger task                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.36.5.2 TASKS\_STOP

Address offset: 0x004

### Stop Timer

|                  |            |            |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|------------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |            |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |            |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |            |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID   | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W          | TASKS_STOP |       | Stop Timer                                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Trigger    | 1     | Trigger task                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.36.5.3 TASKS\_COUNT

Address offset: 0x008

### Increment Timer (Counter mode only)

|                  |            |             |          |                                                                                       |                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|-------------|----------|---------------------------------------------------------------------------------------|-------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |             |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |             |          | A                                                                                     |                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |             |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field |             | Value ID | Value                                                                                 | Description                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W          | TASKS_COUNT |          |                                                                                       | Increment Timer (Counter mode only) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Trigger     | 1        | Trigger task                                                                          |                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

#### 7.1.36.5.4 TASKS\_CLEAR

Address offset: 0x00C

Clear time

|                  |            |             |         |          |  |   |       |  |              |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-------------|---------|----------|--|---|-------|--|--------------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |             |         |          |  |   |       |  |              | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |             |         |          |  |   |       |  |              |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |   |
| Reset 0x00000000 |            |             |         |          |  |   |       |  |              | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |             |         | Value ID |  |   | Value |  |              | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_CLEAR |         |          |  |   |       |  |              | Clear time  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |             | Trigger |          |  | 1 |       |  | Trigger task |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.36.5.5 TASKS SHUTDOWN ( Deprecated )

Address offset: 0x010

Shut down timer



|                  |            |                |  |          |  |  |       |  |  |              |                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------------|--|----------|--|--|-------|--|--|--------------|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                |  |          |  |  |       |  |  | 31           | 30              | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10         | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |                |  |          |  |  |       |  |  |              |                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |   |   |   |   |   |   |   |   | A |   |   |   |   |
| Reset 0x00000000 |            |                |  |          |  |  |       |  |  | 0            | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |                |  | Value ID |  |  | Value |  |  | Description  |                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_SHUTDOWN |  |          |  |  |       |  |  |              | Shut down timer |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | Deprecated |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |                |  | Trigger  |  |  | 1     |  |  | Trigger task |                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.36.5.6 TASKS\_CAPTURE[n] (n=0..5)

Address offset: 0x040 + (n × 0x4)

Capture Timer value to CC[n] register

|                  |            |               |          |         |       |   |             |                                       |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|---------------|----------|---------|-------|---|-------------|---------------------------------------|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |               |          |         |       |   |             |                                       |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |               |          |         |       |   |             |                                       |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   | A |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |               |          |         |       |   |             |                                       |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |               | Value ID |         | Value |   | Description |                                       |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_CAPTURE |          | Trigger |       | 1 |             | Capture Timer value to CC[n] register |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |               |          | Trigger |       | 1 |             | Trigger task                          |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.36.5.7 SUBSCRIBE\_START

Address offset: 0x080

Subscribe configuration for task **START**

|            |  |  |  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           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| Bit number |  |  |  | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            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### 7.1.36.5.8 SUBSCRIBE\_STOP

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| Bit number       |            |          |          | 31                                                                      | 30 | 29                                                    | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |
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| A                | RW CHIDX   |          |          | [255..0]                                                                |    | Channel that task <span>STOP</span> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
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### 7.1.36.5.9 SUBSCRIBE\_COUNT

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Subscribe configuration for task **COUNT**

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| A                | RW CHIDX   |  |          | [255..0] |    | Channel that task <b>COUNT</b> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
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### 7.1.36.5.10 SUBSCRIBE\_CLEAR

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Subscribe configuration for task **CLEAR**

|                  |            |  |          |  |          |  |                                                        |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|--|----------|--|--------------------------------------------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          |  |          |  |                                                        |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |
| ID               |            |  |          |  |          |  |                                                        |  |  | B  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  |    |    |    |   |   |   |   |   |   | A | A | A | A | A | A | A |   |
| Reset 0x00000000 |            |  |          |  |          |  |                                                        |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID |  | Value    |  | Description                                            |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          |  | [255..0] |  | Channel that task <span>CLEAR</span> will subscribe to |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |  |          |  |                                                        |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled |  | 0        |  | Disable subscription                                   |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  |  | 1        |  | Enable subscription                                    |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.36.5.11 SUBSCRIBE\_SHUTDOWN ( Deprecated )

Address offset: 0x090

Subscribe configuration for task **SHUTDOWN**

|                  |            |          |          |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|-----------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                                                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |          |          | B                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |          | 0                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field | Value ID | Value    | Description                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | CHIDX    | [255..0] | Channel that task <b>SHUTDOWN</b> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW         | EN       |          |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        | Disable subscription                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        | Enable subscription                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.36.5.12 SUBSCRIBE\_CAPTURE[n] (n=0..5)

Address offset: 0x0C0 + (n × 0x4)

Subscribe configuration for task **CAPTURE[n]**

|                  |            |          |          |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|----------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |          |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |          |          | B                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value    | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0] | Channel that task <span>CAPTURE[n]</span> will subscribe to                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |          |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0        | Disable subscription                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1        | Enable subscription                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

### 7.1.36.5.13 EVENTS\_COMPARE[n] (n=0..5)

Address offset:  $0x140 + (n \times 0x4)$

Compare event on CC[n] match

|                  |                   |              |                                                                                       |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|-------------------|--------------|---------------------------------------------------------------------------------------|------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |                   |              | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |                   |              | A                                                                                     |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |                   |              | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field        | Value ID     | Value                                                                                 | Description                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW EVENTS_COMPARE |              |                                                                                       | Compare event on CC[n] match |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                   | NotGenerated | 0                                                                                     | Event not generated          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                   | Generated    | 1                                                                                     | Event generated              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.36.5.14 PUBLISH\_COMPARE[n] (n=0..5)

Address offset:  $0x1C0 + (n \times 0x4)$

Publish configuration for event COMPARE[n]

|                  |            |          |                                                                                       |  |                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|--|------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |          | B                                                                                     |  |                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |  |                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 |  | Description                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                              |  | Channel that event COMPARE[n] will publish to. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |                                                                                       |  |                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     |  | Disable publishing                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     |  | Enable publishing                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

### 7.1.36.5.15 SHORTS

Address offset: 0x200

Shortcuts between local events and tasks

|                  |                                 |          |                                                                                       |                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|---------------------------------|----------|---------------------------------------------------------------------------------------|--------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |                                 |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |                                 |          | L K J I H G                                                                           |                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | F E D C B A |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |                                 |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field                      | Value ID | Value                                                                                 | Description                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A-F              | RW COMPARE[i]_CLEAR<br>(i=0..5) |          |                                                                                       | Shortcut between event COMPARE[i] and task CLEAR |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                                 | Disabled | 0                                                                                     | Disable shortcut                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                                 | Enabled  | 1                                                                                     | Enable shortcut                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| G-L              | RW COMPARE[i]_STOP<br>(i=0..5)  |          |                                                                                       | Shortcut between event COMPARE[i] and task STOP  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                                 | Disabled | 0                                                                                     | Disable shortcut                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                                 | Enabled  | 1                                                                                     | Enable shortcut                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.36.5.16 INTEN

Address offset: 0x300

Enable or disable interrupt

| Bit number       |                        |          |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------------------|----------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |                        |          |       | F E D C B A                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |                        |          |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field             | Value ID | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A-F              | RW COMPARE[i] (i=0..5) |          |       | Enable or disable interrupt for event COMPARE[i]                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                        | Disabled | 0     | Disable                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                        | Enabled  | 1     | Enable                                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.36.5.17 INTENSET

Address offset: 0x304

Enable interrupt

|                  |                        |          |                                                                                       |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------------------|----------|---------------------------------------------------------------------------------------|----------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |                        |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |                        |          | F E D C B A                                                                           |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |                        |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field             | Value ID | Value                                                                                 | Description                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A-F              | RW COMPARE[i] (i=0..5) |          |                                                                                       | Write '1' to enable interrupt for event COMPARE[i] |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                        | Set      | 1                                                                                     | Enable                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                        | Disabled | 0                                                                                     | Read: Disabled                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                        | Enabled  | 1                                                                                     | Read: Enabled                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.36.5.18 INTENCLR

Address offset: 0x308

Disable interrupt

|                  |                        |          |                                                                                       |                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------------------|----------|---------------------------------------------------------------------------------------|-----------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |                        |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |                        |          | F E D C B A                                                                           |                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |                        |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field             | Value ID | Value                                                                                 | Description                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A-F              | RW COMPARE[i] (i=0..5) |          |                                                                                       | Write '1' to disable interrupt for event COMPARE[i] |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                        | Clear    | 1                                                                                     | Disable                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                        | Disabled | 0                                                                                     | Read: Disabled                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                        | Enabled  | 1                                                                                     | Read: Enabled                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.36.5.19 MODE

Address offset: 0x504

Timer mode selection

|                  |            |                 |                                                                                       |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|-----------------|---------------------------------------------------------------------------------------|-------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |                 | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |                 | A A                                                                                   |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |                 | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID        | Value                                                                                 | Description                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW MODE    |                 |                                                                                       | Timer mode                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Timer           | 0                                                                                     | Select Timer mode             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Counter         | 1                                                                                     | Select Counter mode           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | LowPowerCounter | 2                                                                                     | Select Low Power Counter mode |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |                 |                                                                                       | Deprecated                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |



### 7.1.36.5.20 BITMODE

Address offset: 0x508

Configure the number of bits used by the TIMER

|                  |      |         |       |    |       |                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |
|------------------|------|---------|-------|----|-------|------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|--|
| Bit number       |      |         |       | 31 | 30    | 29                     | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |  |
| ID               |      |         |       |    |       |                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A | A |  |
| Reset 0x00000000 |      |         |       | 0  | 0     | 0                      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |  |
| ID               | Acce | Field   | Value | ID | Value | Description            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |
| A                | RW   | BITMODE |       |    |       | Timer bit width        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |         | 16Bit |    | 0     | 16 bit timer bit width |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |         | 08Bit |    | 1     | 8 bit timer bit width  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |         | 24Bit |    | 2     | 24 bit timer bit width |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |         | 32Bit |    | 3     | 32 bit timer bit width |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |

### 7.1.36.5.21 PRESCALER

Address offset: 0x510

Timer prescaler register

|                  |            |           |          |        |    |                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-----------|----------|--------|----|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |           |          | 31     | 30 | 29              | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |           |          |        |    |                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | A | A | A | A |   |
| Reset 0x00000004 |            |           |          | 0      | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| ID               | Acce Field |           | Value ID | Value  |    | Description     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | PRESCALER |          | [0..9] |    | Prescaler value |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.36.5.22 CC[n] (n=0..5)

Address offset: 0x540 + (n × 0x4)

Capture/Compare register n

|                  |            |    |          |                       |    |    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----|----------|-----------------------|----|----|----|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |    |          | 31                    | 30 | 29 | 28 | 27          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |    |          | A                     | A  | A  | A  | A           | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |    |          | 0                     | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |    | Value ID | Value                 |    |    |    | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | CC |          | Capture/Compare value |    |    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

Only the number of bits indicated by BITMODE will be used by the TIMER.

### 7.1.36.5.23 ONESHOTEN[n] (n=0..5)

Address offset: 0x580 + (n × 0x4)

Enable one-shot operation for Capture/Compare channel n

| Bit number       |      |           |          | 31    | 30                                                                                               | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |
|------------------|------|-----------|----------|-------|--------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|
| ID               |      |           |          |       |                                                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |  |  |
| Reset 0x00000000 |      |           |          | 0     | 0                                                                                                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |
| ID               | Acce | Field     | Value ID | Value | Description                                                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
| A                | RW   | ONESHOTEN |          |       | Enable one-shot operation                                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |           |          |       | Configures the corresponding compare-channel for one-shot operation                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |           | Disable  | 0     | Disable one-shot operation                                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |           |          |       | Compare event is generated every time the Counter matches CC[n]                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |           | Enable   | 1     | Enable one-shot operation                                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |           |          |       | Compare event is generated the first time the Counter matches CC[n] after CC[n] has been written |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |

### 7.1.36.6 Electrical specification

## 7.1.37 TWIM — I<sup>2</sup>C compatible two-wire interface master with EasyDMA

TWI master with EasyDMA (TWIM) is a two-wire half-duplex master which can communicate with multiple slave devices connected to the same bus

Listed here are the main features for TWIM:

- I<sup>2</sup>C compatible
- Supported baud rates: 100, 250, 400 and 1000 kbps
- Support for clock stretching (non I<sup>2</sup>C compliant)
- EasyDMA

The two-wire interface can communicate with a bi-directional wired-AND bus with two lines (SCL, SDA). The protocol makes it possible to interconnect up to 127 individually addressable devices. TWIM is not compatible with CBUS.

The GPIOs used for each two-wire interface line can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pinout and efficient use of board space and signal routing.

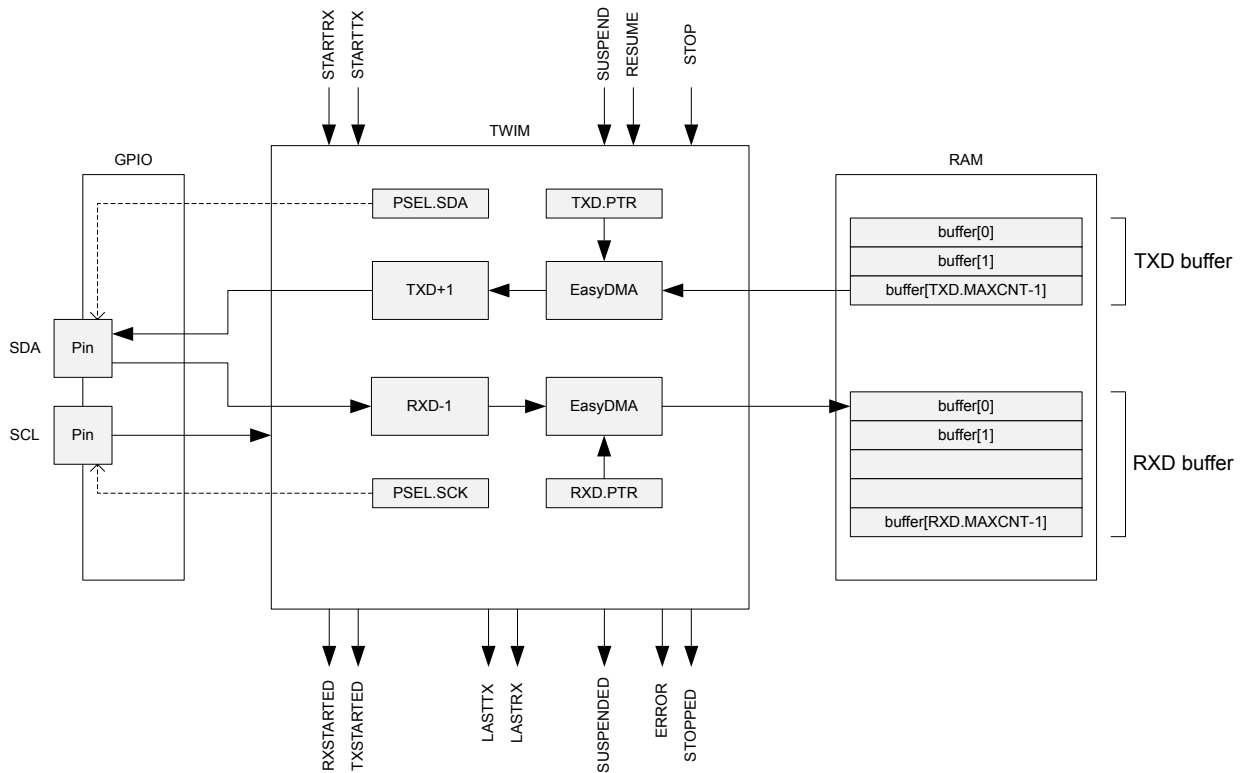


Figure 207: TWI master with EasyDMA

A typical TWI setup consists of one master and one or more slaves. For an example, see [Figure 208: A typical TWI setup comprising one master and three slaves](#) on page 611. This TWIM is only able to operate as a single master on the TWI bus. Multi-master bus configuration is not supported.

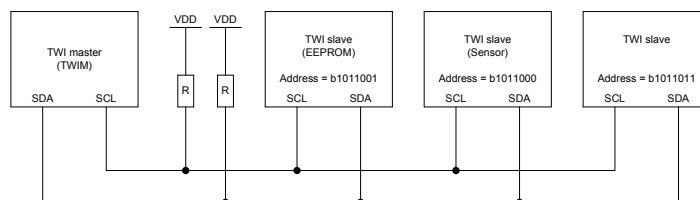


Figure 208: A typical TWI setup comprising one master and three slaves

This TWI master supports clock stretching performed by the slaves. Note that the SCK pulse following a stretched clock cycle may be shorter than specified by the I2C specification.

The TWI master is started by triggering the STARTTX or STARTRX tasks, and stopped by triggering the STOP task. The TWI master will generate a STOPPED event when it has stopped following a STOP task. The TWI master cannot get stopped while it is suspended, so the STOP task has to be issued after the TWI master has been resumed.

After the TWI master is started, the STARTTX task or the STARTRX task should not be triggered again before the TWI master has stopped, i.e. following a LASTRX, LASTTX or STOPPED event.

If a NACK is clocked in from the slave, the TWI master will generate an ERROR event.

### 7.1.37.1 Shared resources

The TWI master shares registers and other resources with other peripherals that have the same ID as the TWI master. Therefore, you must disable all peripherals that have the same ID as the TWI master before the TWI master can be configured and used.

Disabling a peripheral that has the same ID as the TWI master will not reset any of the registers that are shared with the TWI master. It is therefore important to configure all relevant registers explicitly to secure that the TWI master operates correctly.

The Instantiation table in [Instantiation](#) on page 136 shows which peripherals have the same ID as the TWI.

### 7.1.37.2 EasyDMA

The TWIM implements EasyDMA for accessing RAM without CPU involvement.

The TWIM peripheral implements the following EasyDMA channels:

| Channel | Type   | Register Cluster |
|---------|--------|------------------|
| TXD     | READER | TXD              |
| RXD     | WRITER | RXD              |

Table 164: TWIM EasyDMA Channels

For detailed information regarding the use of EasyDMA, see [EasyDMA](#) on page 140.

The .PTR and .MAXCNT registers are double-buffered. They can be updated and prepared for the next RX/TX transmission immediately after having received the RXSTARTED/TXSTARTED event.

The STOPPED event indicates that EasyDMA has finished accessing the buffer in RAM.

### 7.1.37.3 Master write sequence

A TWI master write sequence is started by triggering the STARTTX task. After the STARTTX task has been triggered, the TWI master will generate a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 0 (WRITE=0, READ=1).

The address must match the address of the slave device that the master wants to write to. The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK=1) generated by the slave.

After receiving the ACK bit, the TWI master will clock out the data bytes found in the transmit buffer located in RAM at the address specified in the TXD.PTR register. Each byte clocked out from the master will be followed by an ACK/NACK bit clocked in from the slave.

A typical TWI master write sequence is illustrated in [Figure 209: TWI master writing data to a slave](#) on page 613. Occurrence 2 in the figure illustrates clock stretching performed by the TWI master following a SUSPEND task.

A SUSPENDED event indicates that the SUSPEND task has taken effect; this event can be used to synchronize the software.



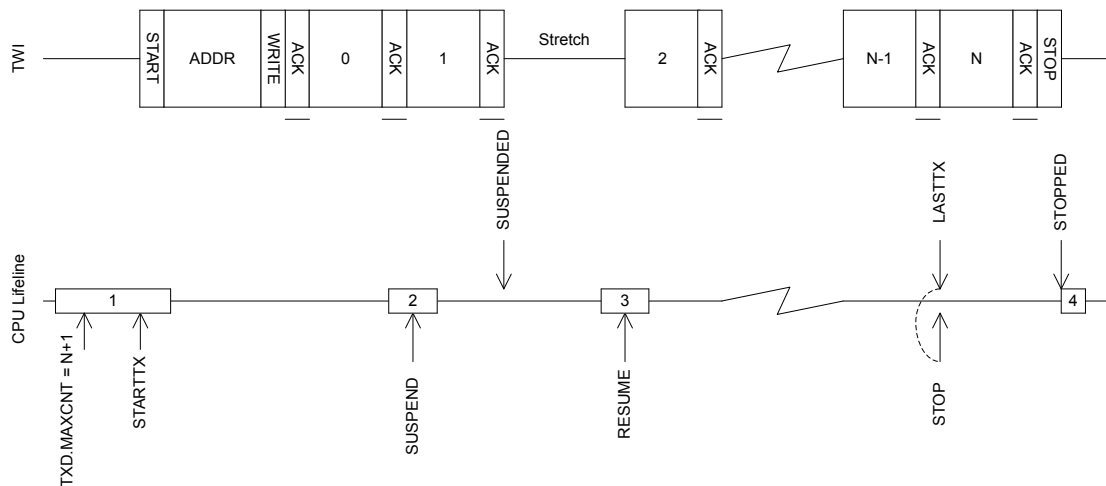


Figure 209: TWI master writing data to a slave

The TWI master will generate a LASTTX event when it starts to transmit the last byte, this is illustrated in [Figure 209: TWI master writing data to a slave](#) on page 613

The TWI master is stopped by triggering the STOP task, this task should be triggered during the transmission of the last byte to secure that the TWI will stop as fast as possible after sending the last byte. It is safe to use the shortcut between LASTTX and STOP to accomplish this.

Note that the TWI master does not stop by itself when the whole RAM buffer has been sent, or when an error occurs. The STOP task must be issued, through the use of a local or PPI shortcut, or in software as part of the error handler.

The TWI master cannot get stopped while it is suspended, so the STOP task has to be issued after the TWI master has been resumed.

#### 7.1.37.4 Master read sequence

A TWI master read sequence is started by triggering the STARTRX task. After the STARTRX task has been triggered the TWI master will generate a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 1 (WRITE = 0, READ = 1). The address must match the address of the slave device that the master wants to read from. The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK = 1) generated by the slave.

After having sent the ACK bit the TWI slave will send data to the master using the clock generated by the master.

Data received will be stored in RAM at the address specified in the RXD.PTR register. The TWI master will generate an ACK after all but the last byte received from the slave. The TWI master will generate a NACK after the last byte received to indicate that the read sequence shall stop.

A typical TWI master read sequence is illustrated in [Figure 210: The TWI master reading data from a slave](#) on page 614. Occurrence 2 in the figure illustrates clock stretching performed by the TWI master following a SUSPEND task.

A SUSPENDED event indicates that the SUSPEND task has taken effect; this event can be used to synchronize the software.

The TWI master will generate a LASTRX event when it is ready to receive the last byte, this is illustrated in [Figure 210: The TWI master reading data from a slave](#) on page 614. If RXD.MAXCNT > 1 the LASTRX event is generated after sending the ACK of the previously received byte. If RXD.MAXCNT = 1 the LASTRX event is generated after receiving the ACK following the address and READ bit.

The TWI master is stopped by triggering the STOP task, this task must be triggered before the NACK bit is supposed to be transmitted. The STOP task can be triggered at any time during the reception of the last byte. It is safe to use the shortcut between LASTRX and STOP to accomplish this.

Note that the TWI master does not stop by itself when the RAM buffer is full, or when an error occurs. The STOP task must be issued, through the use of a local or PPI shortcut, or in software as part of the error handler.

The TWI master cannot get stopped while it is suspended, so the STOP task has to be issued after the TWI master has been resumed.

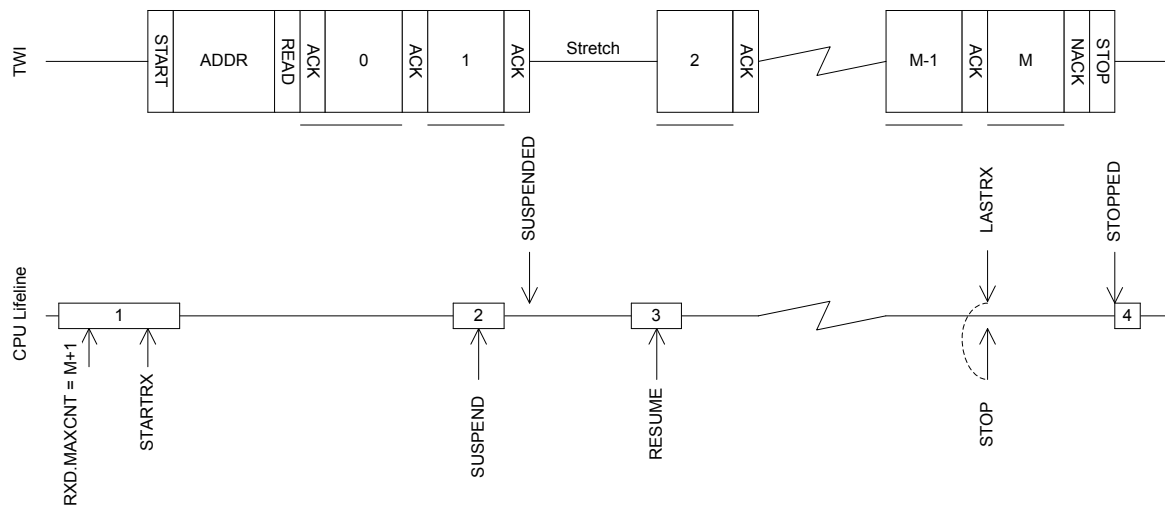


Figure 210: The TWI master reading data from a slave

### 7.1.37.5 Master repeated start sequence

A typical repeated start sequence is one in which the TWI master writes two bytes to the slave followed by reading four bytes from the slave. This example uses shortcuts to perform the simplest type of repeated start sequence, i.e. one write followed by one read. The same approach can be used to perform a repeated start sequence where the sequence is read followed by write.

The figure [Figure 211: A repeated start sequence, where the TWI master writes two bytes followed by reading 4 bytes from the slave](#) on page 614 illustrates this:

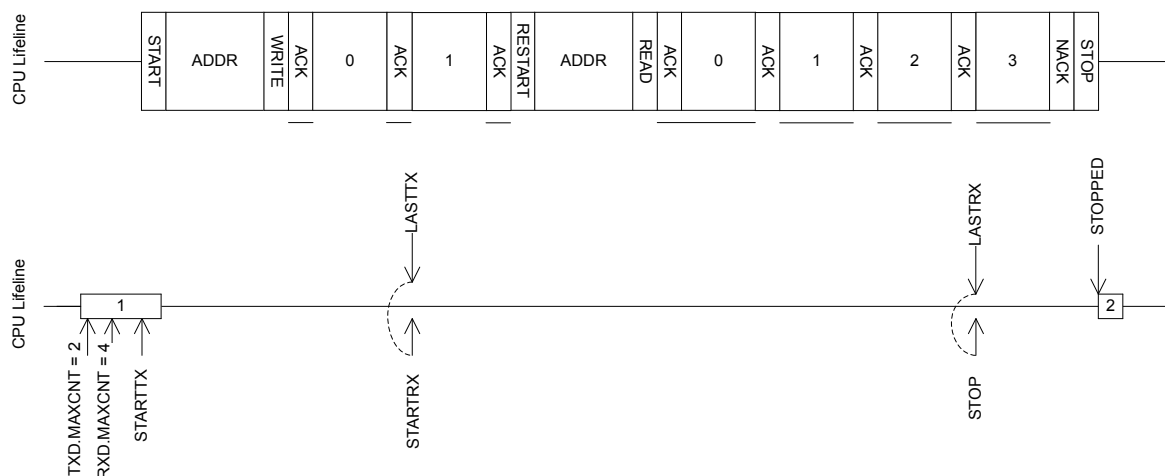


Figure 211: A repeated start sequence, where the TWI master writes two bytes followed by reading 4 bytes from the slave

If a more complex repeated start sequence is needed and the TWI firmware drive is serviced in a low priority interrupt it may be necessary to use the SUSPEND task and SUSPENDED event to guarantee that the correct tasks are generated at the correct time. This is illustrated in [Figure 212: A double repeated start sequence using the SUSPEND task to secure safe operation in low priority interrupts](#) on page 615.

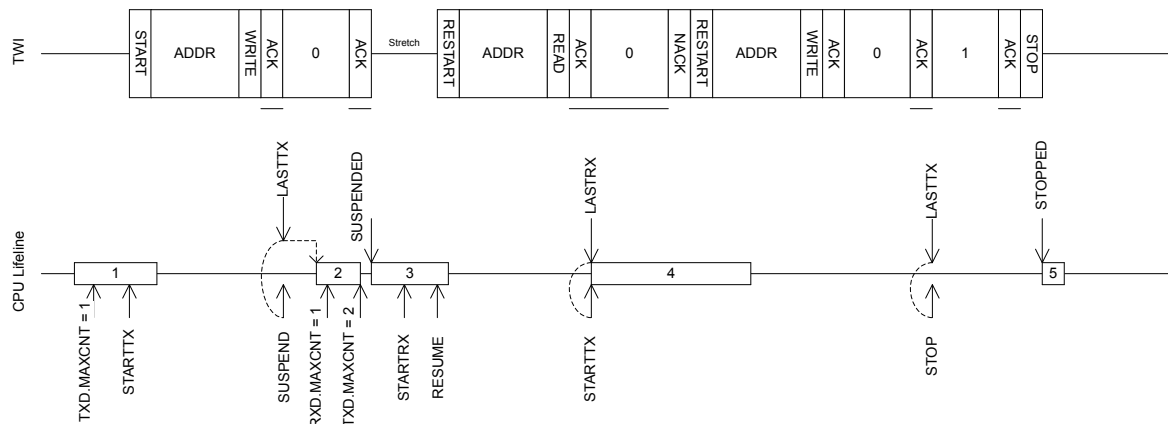


Figure 212: A double repeated start sequence using the SUSPEND task to secure safe operation in low priority interrupts

### 7.1.37.6 Low power

When putting the system in low power and the peripheral is not needed, lowest possible power consumption is achieved by stopping, and then disabling the peripheral.

The STOP task may not be always needed (the peripheral might already be stopped), but if it is sent, software shall wait until the STOPPED event was received as a response before disabling the peripheral through the ENABLE register.

### 7.1.37.7 Master mode pin configuration

The SCL and SDA signals associated with the TWI master are mapped to physical pins according to the configuration specified in the PSEL.SCL and PSEL.SDA registers respectively.

The PSEL.SCL and PSEL.SDA registers and their configurations are only used as long as the TWI master is enabled, and retained only as long as the device is in ON mode. When the peripheral is disabled, the pins will behave as regular GPIOs, and use the configuration in their respective OUT bit field and PIN\_CNF[n] register. PSEL.SCL, PSEL.SDA must only be configured when the TWI master is disabled.

To secure correct signal levels on the pins used by the TWI master when the system is in OFF mode, and when the TWI master is disabled, these pins must be configured in the GPIO peripheral as described in [Table 165: GPIO configuration before enabling peripheral](#) on page 615.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

| TWI master signal | TWI master pin           | Direction | Output value   | Drive strength |
|-------------------|--------------------------|-----------|----------------|----------------|
| SCL               | As specified in PSEL.SCL | Input     | Not applicable | S0D1           |
| SDA               | As specified in PSEL.SDA | Input     | Not applicable | S0D1           |

Table 165: GPIO configuration before enabling peripheral

## 7.1.37.8 Registers

| Base address | Domain      | Peripheral | Instance   | Secure mapping | DMA security | Description               | Configuration |
|--------------|-------------|------------|------------|----------------|--------------|---------------------------|---------------|
| 0x50008000   | APPLICATION | TWIM       | TWIM0 : S  | US             | SA           | Two-wire interface master | 0             |
| 0x40008000   |             |            | TWIM0 : NS |                |              |                           |               |
| 0x50009000   | APPLICATION | TWIM       | TWIM1 : S  | US             | SA           | Two-wire interface master | 1             |
| 0x40009000   |             |            | TWIM1 : NS |                |              |                           |               |
| 0x41013000   | NETWORK     | TWIM       | TWIM0      | NS             | NA           | Two-wire interface master | 0             |

Table 166: Instances

| Register          | Offset | Security | Description                                                                                       |
|-------------------|--------|----------|---------------------------------------------------------------------------------------------------|
| TASKS_STARTRX     | 0x000  |          | Start TWI receive sequence                                                                        |
| TASKS_STARTTX     | 0x008  |          | Start TWI transmit sequence                                                                       |
| TASKS_STOP        | 0x014  |          | Stop TWI transaction. Must be issued while the TWI master is not suspended.                       |
| TASKS_SUSPEND     | 0x01C  |          | Suspend TWI transaction                                                                           |
| TASKS_RESUME      | 0x020  |          | Resume TWI transaction                                                                            |
| SUBSCRIBE_STARTRX | 0x080  |          | Subscribe configuration for task <a href="#">STARTRX</a>                                          |
| SUBSCRIBE_STARTTX | 0x088  |          | Subscribe configuration for task <a href="#">STARTTX</a>                                          |
| SUBSCRIBE_STOP    | 0x094  |          | Subscribe configuration for task <a href="#">STOP</a>                                             |
| SUBSCRIBE_SUSPEND | 0x09C  |          | Subscribe configuration for task <a href="#">SUSPEND</a>                                          |
| SUBSCRIBE_RESUME  | 0x0A0  |          | Subscribe configuration for task <a href="#">RESUME</a>                                           |
| EVENTS_STOPPED    | 0x104  |          | TWI stopped                                                                                       |
| EVENTS_ERROR      | 0x124  |          | TWI error                                                                                         |
| EVENTS_SUSPENDED  | 0x148  |          | Last byte has been sent out after the SUSPEND task has been issued, TWI traffic is now suspended. |
| EVENTS_RXSTARTED  | 0x14C  |          | Receive sequence started                                                                          |
| EVENTS_TXSTARTED  | 0x150  |          | Transmit sequence started                                                                         |
| EVENTS_LASTRX     | 0x15C  |          | Byte boundary, starting to receive the last byte                                                  |
| EVENTS_LASTTX     | 0x160  |          | Byte boundary, starting to transmit the last byte                                                 |
| PUBLISH_STOPPED   | 0x184  |          | Publish configuration for event <a href="#">STOPPED</a>                                           |
| PUBLISH_ERROR     | 0x1A4  |          | Publish configuration for event <a href="#">ERROR</a>                                             |
| PUBLISH_SUSPENDED | 0x1C8  |          | Publish configuration for event <a href="#">SUSPENDED</a>                                         |
| PUBLISH_RXSTARTED | 0x1CC  |          | Publish configuration for event <a href="#">RXSTARTED</a>                                         |
| PUBLISH_TXSTARTED | 0x1D0  |          | Publish configuration for event <a href="#">TXSTARTED</a>                                         |
| PUBLISH_LASTRX    | 0x1DC  |          | Publish configuration for event <a href="#">LASTRX</a>                                            |
| PUBLISH_LASTTX    | 0x1E0  |          | Publish configuration for event <a href="#">LASTTX</a>                                            |
| SHORTS            | 0x200  |          | Shortcuts between local events and tasks                                                          |
| INTEN             | 0x300  |          | Enable or disable interrupt                                                                       |
| INTENSET          | 0x304  |          | Enable interrupt                                                                                  |
| INTENCLR          | 0x308  |          | Disable interrupt                                                                                 |
| ERRORSRC          | 0x4C4  |          | Error source                                                                                      |
| ENABLE            | 0x500  |          | Enable TWIM                                                                                       |
| PSEL.SCL          | 0x508  |          | Pin select for SCL signal                                                                         |
| PSEL.SDA          | 0x50C  |          | Pin select for SDA signal                                                                         |
| FREQUENCY         | 0x524  |          | TWI frequency. Accuracy depends on the HFCLK source selected.                                     |
| RXD.PTR           | 0x534  |          | Data pointer                                                                                      |
| RXD.MAXCNT        | 0x538  |          | Maximum number of bytes in receive buffer                                                         |
| RXD.AMOUNT        | 0x53C  |          | Number of bytes transferred in the last transaction                                               |
| RXD.LIST          | 0x540  |          | EasyDMA list type                                                                                 |
| TXD.PTR           | 0x544  |          | Data pointer                                                                                      |
| TXD.MAXCNT        | 0x548  |          | Maximum number of bytes in transmit buffer                                                        |

| Register                   | Offset | Security | Description                                         |
|----------------------------|--------|----------|-----------------------------------------------------|
| <a href="#">TXD.AMOUNT</a> | 0x54C  |          | Number of bytes transferred in the last transaction |
| <a href="#">TXD.LIST</a>   | 0x550  |          | EasyDMA list type                                   |
| <a href="#">ADDRESS</a>    | 0x588  |          | Address used in the TWI transfer                    |

Table 167: Register overview

### 7.1.37.8.1 TASKS\_STARTTRX

Address offset: 0x000

Start TWI receive sequence

|                  |            |               |       |    |    |    |                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|---------------|-------|----|----|----|----------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |               | 31    | 30 | 29 | 28 | 27                         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |               | A     |    |    |    |                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |               | 0     | 0  | 0  | 0  | 0                          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID      | Value |    |    |    | Description                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_STARTRX |       |    |    |    | Start TWI receive sequence |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Trigger       | 1     |    |    |    | Trigger task               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 7.1.37.8.2 TASKS\_STARTTX

Address offset: 0x008

Start TWI transmit sequence

|                  |            |               |                                                                                       |  |       |  |              |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|---------------|---------------------------------------------------------------------------------------|--|-------|--|--------------|-----------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |               | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |       |  |              |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |               | A                                                                                     |  |       |  |              |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |               | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |  |       |  |              |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field |               | Value ID                                                                              |  | Value |  | Description  |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W          | TASKS_STARTTX |                                                                                       |  |       |  |              | Start TWI transmit sequence |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |               | Trigger                                                                               |  | 1     |  | Trigger task |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.37.8.3 TASKS\_STOP

Address offset: 0x014

Stop TWI transaction. Must be issued while the TWI master is not suspended.

|                  |            |            |       |    |    |    |    |                                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|------------------|------------|------------|-------|----|----|----|----|-----------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|
| Bit number       |            |            | 31    | 30 | 29 | 28 | 27 | 26                                                                          | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |
| ID               |            |            | A     |    |    |    |    |                                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
| Reset 0x00000000 |            |            | 0     | 0  | 0  | 0  | 0  | 0                                                                           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |
| ID               | Acce Field | Value ID   | Value |    |    |    |    | Description                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
| A                | W          | TASKS_STOP |       |    |    |    |    | Stop TWI transaction. Must be issued while the TWI master is not suspended. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            | Trigger    | 1     |    |    |    |    | Trigger task                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |

#### 7.1.37.8.4 TASKS SUSPEND

Address offset: 0x01C

## Suspend TWI transaction



|                  |            |          |          |    |    |    |                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|----|----|----|-------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          | 31       | 30 | 29 | 28 | 27                                              | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |          | B        |    |    |    |                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   |   |   |   |   |   |   |   | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |          | 0        |    |    |    |                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID | Value    |    |    |    | Description                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] |    |    |    | Channel that task <b>STOP</b> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |    |    |    |                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        |    |    |    | Disable subscription                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        |    |    |    | Enable subscription                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.37.8.9 SUBSCRIBE\_SUSPEND

Address offset: 0x09C

Subscribe configuration for task **SUSPEND**

|                  |            |  |          |  |          |  |                                                          |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|--|----------|--|----------------------------------------------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          |  |          |  |                                                          |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |
| ID               |            |  |          |  |          |  |                                                          |  |  | B  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  |    |    |    |   |   |   |   |   |   | A | A | A | A | A | A | A |   |
| Reset 0x00000000 |            |  |          |  |          |  |                                                          |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID |  | Value    |  | Description                                              |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          |  | [255..0] |  | Channel that task <span>SUSPEND</span> will subscribe to |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |  |          |  |                                                          |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled |  | 0        |  | Disable subscription                                     |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  |  | 1        |  | Enable subscription                                      |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.37.8.10 SUBSCRIBE\_RESUME

Address offset: 0x0A0

Subscribe configuration for task **RESUME**

|                  |            |  |          |                                                                         |    |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|-------------------------------------------------------------------------|----|---------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31                                                                      | 30 | 29                                                | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |  |          | B                                                                       |    |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |    |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field |  | Value ID | Value                                                                   |    | Description                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          | [255..0]                                                                |    | Channel that task <b>RESUME</b> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |                                                                         |    |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled | 0                                                                       |    | Disable subscription                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  | 1                                                                       |    | Enable subscription                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.37.8.11 EVENTS\_STOPPED

Address offset: 0x104

TWI stopped

|                  |            |                |       |    |                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|------------------|------------|----------------|-------|----|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|--|--|
| Bit number       |            |                | 31    | 30 | 29                  | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |  |  |
| ID               |            |                | A     |    |                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| Reset 0x00000000 |            |                | 0     | 0  | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |  |
| ID               | Acce Field | Value ID       | Value |    | Description         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| A                | RW         | EVENTS_STOPPED |       |    | TWI stopped         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | NotGenerated   | 0     |    | Event not generated |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | Generated      | 1     |    | Event generated     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |  |

### 7.1.37.8.12 EVENTS\_ERROR

Address offset: 0x124

TWI error

|                  |                 |              |                                                                                       |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|-----------------|--------------|---------------------------------------------------------------------------------------|---------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |                 |              | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |                 |              | A                                                                                     |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |                 |              | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field      | Value ID     | Value                                                                                 | Description         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW EVENTS_ERROR |              |                                                                                       | TWI error           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                 | NotGenerated | 0                                                                                     | Event not generated |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                 | Generated    | 1                                                                                     | Event generated     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.37.8.13 EVENTS\_SUSPENDED

Address offset: 0x148

Last byte has been sent out after the SUSPEND task has been issued, TWI traffic is now suspended.

| Bit number       |            |                  | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|------------------|---------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |            |                  | A                                                                                     |                                                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |                  | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |                                                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID         | Value                                                                                 | Description                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | EVENTS_SUSPENDED |                                                                                       | Last byte has been sent out after the SUSPEND task has been issued, TWI traffic is now suspended. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | NotGenerated     | 0                                                                                     | Event not generated                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Generated        | 1                                                                                     | Event generated                                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.37.8.14 EVENTS\_RXSTARTED

Address offset: 0x14C

Receive sequence started

|                  |            |                  |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|------------------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |                  |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |                  |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |                  |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID         | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | EVENTS_RXSTARTED |       | Receive sequence started                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | NotGenerated     | 0     | Event not generated                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Generated        | 1     | Event generated                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.37.8.15 EVENTS\_TXSTARTED

Address offset: 0x150

Transmit sequence started



|                  |            |                  |       |                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|------------------|------------|------------------|-------|---------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|---|
| Bit number       |            |                  |       | 31                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |   |
| ID               |            |                  |       |                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | A |
| Reset 0x00000000 |            |                  |       | 0                         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |   |
| ID               | Acce Field | Value ID         | Value | Description               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
| A                | RW         | EVENTS_TXSTARTED |       | Transmit sequence started |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | NotGenerated     | 0     | Event not generated       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | Generated        | 1     | Event generated           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |

#### 7.1.37.8.16 EVENTS\_LASTRX

Address offset: 0x15C

Byte boundary, starting to receive the last byte

|                  |            |               |       |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|---------------|-------|--------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |               |       | 31                                               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |               |       |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |
| Reset 0x00000000 |            |               |       | 0                                                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID      | Value | Description                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | EVENTS_LASTRX |       | Byte boundary, starting to receive the last byte |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | NotGenerated  | 0     | Event not generated                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Generated     | 1     | Event generated                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.37.8.17 EVENTS\_LASTTX

Address offset: 0x160

Byte boundary, starting to transmit the last byte

|                  |            |               |       |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|------------------|------------|---------------|-------|---------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|---|
| Bit number       |            |               |       | 31                                                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |   |
| ID               |            |               |       |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | A |
| Reset 0x00000000 |            |               |       | 0                                                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |   |
| ID               | Acce Field | Value ID      | Value | Description                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
| A                | RW         | EVENTS_LASTTX |       | Byte boundary, starting to transmit the last byte |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | NotGenerated  | 0     | Event not generated                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | Generated     | 1     | Event generated                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |

#### 7.1.37.8.18 PUBLISH\_STOPPED

Address offset: 0x184

Publish configuration for event STOPPED

|                  |            |  |          |                                                                         |    |                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
|------------------|------------|--|----------|-------------------------------------------------------------------------|----|---------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|-----------------|---|---|---|---|---|---|---|--|--|--|--|
| Bit number       |            |  |          | 31                                                                      | 30 | 29                                          | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |
| ID               |            |  |          | B                                                                       |    |                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A A A A A A A A |   |   |   |   |   |   |   |  |  |  |  |
| Reset 0x00000000 |            |  |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |    |                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
| ID               | Acce Field |  | Value ID | Value                                                                   |    | Description                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
| A                | RW CHIDX   |  |          | [255..0]                                                                |    | Channel that event STOPPED will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
| B                | RW EN      |  |          |                                                                         |    |                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
|                  |            |  | Disabled | 0                                                                       |    | Disable publishing                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
|                  |            |  | Enabled  | 1                                                                       |    | Enable publishing                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |

#### 7.1.37.8.19 PUBLISH\_ERROR

Address offset: 0x1A4

Publish configuration for event ERROR

|                  |            |          |          |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|--------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                                               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |          |          | B                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |          | 0                                                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce Field | Value ID | Value    | Description                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] | Channel that event <b>ERROR</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        | Disable publishing                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        | Enable publishing                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.37.8.20 PUBLISH\_SUSPENDED

Address offset: 0x1C8

Publish configuration for event **SUSPENDED**

|                  |            |  |  |          |    |    |          |    |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |   |   |   |   |   |   |
|------------------|------------|--|--|----------|----|----|----------|----|----|------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|--|---|---|---|---|---|---|---|
| Bit number       |            |  |  | 31       | 30 | 29 | 28       | 27 | 26 | 25                                                   | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |  |   |   |   |   |   |   |   |
| ID               |            |  |  | B        |    |    |          |    |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   |   |   |   |   |  |  |  | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |  | 0        | 0  | 0  | 0        | 0  | 0  | 0                                                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |   |   |   |   |   |   |   |
| ID               | Acce Field |  |  | Value ID |    |    | Value    |    |    | Description                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |  |          |    |    | [255..0] |    |    | Channel that event <b>SUSPENDED</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |   |   |   |   |   |   |
| B                | RW EN      |  |  |          |    |    |          |    |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |   |   |   |   |   |   |
|                  |            |  |  | Disabled |    |    | 0        |    |    | Disable publishing                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |   |   |   |   |   |   |
|                  |            |  |  | Enabled  |    |    | 1        |    |    | Enable publishing                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |   |   |   |   |   |   |

### 7.1.37.8.21 PUBLISH\_RXSTARTED

Address offset: 0x1CC

Publish configuration for event **RXSTARTED**

|                  |            |  |          |          |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|----------|----|------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31       | 30 | 29                                                   | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |  |          | B        |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   |   |   |   |   |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |          | 0        |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID | Value    |    | Description                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          | [255..0] |    | Channel that event <b>RXSTARTED</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  | Disabled | 0        |    | Disable publishing                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  | 1        |    | Enable publishing                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.37.8.22 PUBLISH\_TXSTARTED

Address offset: 0x1D0

Publish configuration for event **TXSTARTED**

|                  |            |          |          |          |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|----------|----|------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31       | 30 | 29                                                   | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |          |          | B        |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   |   |   |   |   |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |          |          | 0        |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |          | Value ID | Value    |    | Description                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          |          | [255..0] |    | Channel that event <b>TXSTARTED</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |          |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled |          | 0        |    | Disable publishing                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  |          | 1        |    | Enable publishing                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.37.8.23 PUBLISH\_LASTRX

Address offset: 0x1DC

Publish configuration for event [LASTRX](#)

|                  |            |          |                                                                                       |                    |                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|--------------------|---------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                    |                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |          | B                                                                                     |                    |                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                    |                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 |                    | Description                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                              |                    | Channel that event <span>LASTRX</span> will publish to. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |                                                                                       |                    |                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Disable publishing |                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Enable publishing  |                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

### 7.1.37.8.24 PUBLISH\_LASTTX

Address offset: 0x1E0

Publish configuration for event [LASTTX](#)

|                  |            |          |                                                                                       |                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|---------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |          | B                                                                                     |                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                              | Channel that event <span>LASTTX</span> will publish to. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |                                                                                       |                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Disable publishing                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Enable publishing                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

### 7.1.37.8.25 SHORTS

Address offset: 0x200

Shortcuts between local events and tasks

| Bit number       |      |                | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|----------------|---------------------------------------------------------------------------------------|-------|--------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |      |                | F E D C B A                                                                           |       |                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |                | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |       |                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field          | Value ID                                                                              | Value | Description                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW   | LASTTX_STARTRX |                                                                                       |       | Shortcut between event <span>LASTTX</span> and task <span>STARTRX</span> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                | Disabled                                                                              | 0     | Disable shortcut                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                | Enabled                                                                               | 1     | Enable shortcut                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW   | LASTTX_SUSPEND |                                                                                       |       | Shortcut between event <span>LASTTX</span> and task <span>SUSPEND</span> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                | Disabled                                                                              | 0     | Disable shortcut                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                | Enabled                                                                               | 1     | Enable shortcut                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW   | LASTTX_STOP    |                                                                                       |       | Shortcut between event <span>LASTTX</span> and task <span>STOP</span>    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                | Disabled                                                                              | 0     | Disable shortcut                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                | Enabled                                                                               | 1     | Enable shortcut                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| D                | RW   | LASTRX_STARTTX |                                                                                       |       | Shortcut between event <span>LASTRX</span> and task <span>STARTTX</span> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                | Disabled                                                                              | 0     | Disable shortcut                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                | Enabled                                                                               | 1     | Enable shortcut                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| E                | RW   | LASTRX_SUSPEND |                                                                                       |       | Shortcut between event <span>LASTRX</span> and task <span>SUSPEND</span> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                | Disabled                                                                              | 0     | Disable shortcut                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                | Enabled                                                                               | 1     | Enable shortcut                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

|                  |                |          |       |    |                                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
|------------------|----------------|----------|-------|----|-----------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|
| Bit number       |                |          | 31    | 30 | 29                                                                          | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |
| ID               |                |          |       |    |                                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | F | E | D | C | B | A |   |   |  |  |
| Reset 0x00000000 |                |          | 0     | 0  | 0                                                                           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |
| ID               | Acce Field     | Value ID | Value |    | Description                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
| F                | RW LASTRX_STOP |          |       |    | Shortcut between event <a href="#">LASTRX</a> and task <a href="#">STOP</a> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |                | Disabled | 0     |    | Disable shortcut                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |                | Enabled  | 1     |    | Enable shortcut                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |

### 7.1.37.8.26 INTEN

Address offset: 0x300

Enable or disable interrupt

| Bit number       |      |           |          | 31    | 30                                                              | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |
|------------------|------|-----------|----------|-------|-----------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|
| ID               |      |           |          | J     |                                                                 |    |    |    |    |    |    |    |    | I  | H  |    |    | G  | F  | D  |    |    |    |    |    |   |   |   |   | A |   |   |   |   |   |   |  |  |
| Reset 0x00000000 |      |           |          | 0     | 0                                                               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |
| ID               | Acce | Field     | Value ID | Value | Description                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
| A                | RW   | STOPPED   |          |       | Enable or disable interrupt for event <a href="#">STOPPED</a>   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |           | Disabled | 0     | Disable                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |           | Enabled  | 1     | Enable                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
| D                | RW   | ERROR     |          |       | Enable or disable interrupt for event <a href="#">ERROR</a>     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |           | Disabled | 0     | Disable                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |           | Enabled  | 1     | Enable                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
| F                | RW   | SUSPENDED |          |       | Enable or disable interrupt for event <a href="#">SUSPENDED</a> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |           | Disabled | 0     | Disable                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |           | Enabled  | 1     | Enable                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
| G                | RW   | RXSTARTED |          |       | Enable or disable interrupt for event <a href="#">RXSTARTED</a> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |           | Disabled | 0     | Disable                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |           | Enabled  | 1     | Enable                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
| H                | RW   | TXSTARTED |          |       | Enable or disable interrupt for event <a href="#">TXSTARTED</a> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |           | Disabled | 0     | Disable                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |           | Enabled  | 1     | Enable                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
| I                | RW   | LASTRX    |          |       | Enable or disable interrupt for event <a href="#">LASTRX</a>    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |           | Disabled | 0     | Disable                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |           | Enabled  | 1     | Enable                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
| J                | RW   | LASTTX    |          |       | Enable or disable interrupt for event <a href="#">LASTTX</a>    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |           | Disabled | 0     | Disable                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |      |           | Enabled  | 1     | Enable                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |

### 7.1.37.8.27 INTENSET

Address offset: 0x304

Enable interrupt

|                  |            |          |                                                                                       |                                                 |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|-------------------------------------------------|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                 |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          | J I H G F                                                                             |                                                 |  |  |  |  |  |  |  |  | D |  |  |  |  |  |  |  |  |  | A |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                   |                                                 |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                     |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW STOPPED |          |                                                                                       | Write '1' to enable interrupt for event STOPPED |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Set      | 1                                                                                     | Enable                                          |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Read: Disabled                                  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Read: Enabled                                   |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |
| D                | RW ERROR   |          |                                                                                       | Write '1' to enable interrupt for event ERROR   |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |

| Bit number       |              |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|--------------|----------|---------------------------------------------------------------------------------------|-------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |              |          | J I H G F D A                                                                         |                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |              |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field   | Value ID | Value                                                                                 | Description                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Set      | 1                                                                                     | Enable                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Disabled | 0                                                                                     | Read: Disabled                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Enabled  | 1                                                                                     | Read: Enabled                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| F                | RW SUSPENDED |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">SUSPENDED</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Set      | 1                                                                                     | Enable                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Disabled | 0                                                                                     | Read: Disabled                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Enabled  | 1                                                                                     | Read: Enabled                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| G                | RW RXSTARTED |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">RXSTARTED</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Set      | 1                                                                                     | Enable                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Disabled | 0                                                                                     | Read: Disabled                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Enabled  | 1                                                                                     | Read: Enabled                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| H                | RW TXSTARTED |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">TXSTARTED</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Set      | 1                                                                                     | Enable                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Disabled | 0                                                                                     | Read: Disabled                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Enabled  | 1                                                                                     | Read: Enabled                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| I                | RW LASTRX    |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">LASTRX</a>    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Set      | 1                                                                                     | Enable                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Disabled | 0                                                                                     | Read: Disabled                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Enabled  | 1                                                                                     | Read: Enabled                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| J                | RW LASTTX    |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">LASTTX</a>    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Set      | 1                                                                                     | Enable                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Disabled | 0                                                                                     | Read: Disabled                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Enabled  | 1                                                                                     | Read: Enabled                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.37.8.28 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number       |              |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|--------------|----------|---------------------------------------------------------------------------------------|----------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |              |          | J I H G F D A                                                                         |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |              |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field   | Value ID | Value                                                                                 | Description                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW STOPPED   |          |                                                                                       | Write '1' to disable interrupt for event STOPPED   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Clear    | 1                                                                                     | Disable                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Disabled | 0                                                                                     | Read: Disabled                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Enabled  | 1                                                                                     | Read: Enabled                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| D                | RW ERROR     |          |                                                                                       | Write '1' to disable interrupt for event ERROR     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Clear    | 1                                                                                     | Disable                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Disabled | 0                                                                                     | Read: Disabled                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Enabled  | 1                                                                                     | Read: Enabled                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| F                | RW SUSPENDED |          |                                                                                       | Write '1' to disable interrupt for event SUSPENDED |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Clear    | 1                                                                                     | Disable                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Disabled | 0                                                                                     | Read: Disabled                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Enabled  | 1                                                                                     | Read: Enabled                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| G                | RW RXSTARTED |          |                                                                                       | Write '1' to disable interrupt for event RXSTARTED |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Clear    | 1                                                                                     | Disable                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Disabled | 0                                                                                     | Read: Disabled                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Enabled  | 1                                                                                     | Read: Enabled                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

| Bit number       |              |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|--------------|----------|---------------------------------------------------------------------------------------|--------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |              |          | J I H G F D A                                                                         |                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |              |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field   | Value ID | Value                                                                                 | Description                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| H                | RW TXSTARTED |          |                                                                                       | Write '1' to disable interrupt for event <a href="#">TXSTARTED</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Clear    | 1                                                                                     | Disable                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Disabled | 0                                                                                     | Read: Disabled                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Enabled  | 1                                                                                     | Read: Enabled                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| I                | RW LASTRX    |          |                                                                                       | Write '1' to disable interrupt for event <a href="#">LASTRX</a>    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Clear    | 1                                                                                     | Disable                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Disabled | 0                                                                                     | Read: Disabled                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Enabled  | 1                                                                                     | Read: Enabled                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| J                | RW LASTTX    |          |                                                                                       | Write '1' to disable interrupt for event <a href="#">LASTTX</a>    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Clear    | 1                                                                                     | Disable                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Disabled | 0                                                                                     | Read: Disabled                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Enabled  | 1                                                                                     | Read: Enabled                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.37.8.29 ERRORSRC

Address offset: 0x4C4

Error source

| Bit number       |            |             | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|-------------|---------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |            |             | C B A                                                                                 |                                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |             | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID    | Value                                                                                 | Description                                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW OVERRUN |             |                                                                                       | Overrun error                                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |             |                                                                                       | A new byte was received before previous byte got transferred into RXD buffer. (Previous data is lost) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | NotReceived | 0                                                                                     | Error did not occur                                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Received    | 1                                                                                     | Error occurred                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW ANACK   |             |                                                                                       | NACK received after sending the address (write '1' to clear)                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | NotReceived | 0                                                                                     | Error did not occur                                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Received    | 1                                                                                     | Error occurred                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW DNACK   |             |                                                                                       | NACK received after sending a data byte (write '1' to clear)                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | NotReceived | 0                                                                                     | Error did not occur                                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Received    | 1                                                                                     | Error occurred                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.37.8.30 ENABLE

Address offset: 0x500

Enable TWIM

|                  |            |        |          |                                                                                       |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|--------|----------|---------------------------------------------------------------------------------------|------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |        |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |        |          | A A A A                                                                               |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |        |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field |        | Value ID | Value                                                                                 | Description            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | ENABLE |          |                                                                                       | Enable or disable TWIM |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |        | Disabled | 0                                                                                     | Disable TWIM           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |        | Enabled  | 6                                                                                     | Enable TWIM            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.37.8.31 PSEL.SCL

Address offset: 0x508

### Pin select for SCL signal

|                  |            |              |                                                                       |    |    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------------|-----------------------------------------------------------------------|----|----|----|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |              | 31                                                                    | 30 | 29 | 28 | 27          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |              | C                                                                     |    |    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Reset 0xFFFFFFFF |            |              | 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 |    |    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field | Value ID     | Value                                                                 |    |    |    | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW PIN     |              | [0..31]                                                               |    |    |    | Pin number  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| B                | RW PORT    |              | [0..1]                                                                |    |    |    | Port number |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| C                | RW CONNECT |              |                                                                       |    |    |    | Connection  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disconnected | 1                                                                     |    |    |    | Disconnect  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Connected    | 0                                                                     |    |    |    | Connect     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 7.1.37.8.32 PSEL.SDA

Address offset: 0x50C

### Pin select for SDA signal

|                  |            |              |         |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------------|---------|----|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |              | 31      | 30 | 29          | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |              | C       |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | B |   |   |   | A | A | A | A | A |
| Reset 0xFFFFFFFF |            |              | 1       | 1  | 1           | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |   |
| ID               | Acce Field | Value ID     | Value   |    | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW PIN     |              | [0..31] |    | Pin number  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW PORT    |              | [0..1]  |    | Port number |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| C                | RW CONNECT |              |         |    | Connection  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disconnected | 1       |    | Disconnect  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Connected    | 0       |    | Connect     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.37.8.33 FREQUENCY

Address offset: 0x524

TWI frequency. Accuracy depends on the HFCLK source selected.

|                  |            |  |           |  |            |  |  |  |  |                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|-----------|--|------------|--|--|--|--|----------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |           |  |            |  |  |  |  | 31                         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |  |           |  |            |  |  |  |  | A                          | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A | A |   |
| Reset 0x04000000 |            |  |           |  |            |  |  |  |  | 0                          | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID  |  | Value      |  |  |  |  | Description                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         |  | FREQUENCY |  |            |  |  |  |  | TWI master clock frequency |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | K100      |  | 0x01980000 |  |  |  |  | 100 kbps                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | K250      |  | 0x04000000 |  |  |  |  | 250 kbps                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | K400      |  | 0x06400000 |  |  |  |  | 400 kbps                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | K1000     |  | 0x0FF00000 |  |  |  |  | 1000 kbps                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.37.8.34 RXD.PTR

Address offset: 0x534

Data pointer

|                  |            |  |          |  |       |  |  |  |  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|--|-------|--|--|--|--|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          |  |       |  |  |  |  | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |  |          |  |       |  |  |  |  | A            | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |          |  |       |  |  |  |  | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID |  | Value |  |  |  |  | Description  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW PTR     |  |          |  |       |  |  |  |  | Data pointer |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

**Note:** See the memory chapter for details about which memories are available for EasyDMA.

### 7.1.37.8.35 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in receive buffer

|                  |            |        |          |             |    |    |    |                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------|----------|-------------|----|----|----|-------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |        |          | 31          | 30 | 29 | 28 | 27                                        | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |        |          |             |    |    |    |                                           |    |    |    |    |    |    |    |    |    |    |    | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |        |          | 0           | 0  | 0  | 0  | 0                                         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |
| ID               | Acce Field |        | Value ID | Value       |    |    |    | Description                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | MAXCNT |          | [1..0xFFFF] |    |    |    | Maximum number of bytes in receive buffer |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.37.8.36 RXD.AMOUNT

Address offset: 0x53C

Number of bytes transferred in the last transaction

|                  |            |        |          |             |    |                                                                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------|----------|-------------|----|--------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |        |          | 31          | 30 | 29                                                                                                     | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |        |          |             |    |                                                                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |        |          | 0           | 0  | 0                                                                                                      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |
| ID               | Acce Field |        | Value ID | Value       |    | Description                                                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | R          | AMOUNT |          | [1..0xFFFF] |    | Number of bytes transferred in the last transaction. In case of NACK error, includes the NACK'ed byte. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.37.8.37 RXD.LIST

Address offset: 0x540

EasyDMA list type

|                  |            |           |       |    |                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-----------|-------|----|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |           | 31    | 30 | 29                   | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |           | A A A |    |                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |           | 0     | 0  | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID  | Value |    | Description          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | LIST      |       |    | List type            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled  | 0     |    | Disable EasyDMA list |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | ArrayList | 1     |    | Use array list       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.37.8.38 TXD.PTR

Address offset: 0x544

Data pointer



|                  |            |  |          |  |       |  |  |  |  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|--|-------|--|--|--|--|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          |  |       |  |  |  |  | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |  |          |  |       |  |  |  |  | A            | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |          |  |       |  |  |  |  | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID |  | Value |  |  |  |  | Description  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW PTR     |  |          |  |       |  |  |  |  | Data pointer |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

**Note:** See the memory chapter for details about which memories are available for EasyDMA.

### 7.1.37.8.39 TXD.MAXCNT

Address offset: 0x548

Maximum number of bytes in transmit buffer

|                  |            |        |          |                                                                                       |  |  |  |  |  |  |  |                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|--------|----------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |        |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |        |          | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A                           |  |  |  |  |  |  |  |                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |        |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                   |  |  |  |  |  |  |  |                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field |        | Value ID | Value                                                                                 |  |  |  |  |  |  |  | Description                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | MAXCNT |          | [1..0xFFFF]                                                                           |  |  |  |  |  |  |  | Maximum number of bytes in transmit buffer |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.37.8.40 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transferred in the last transaction

|                  |            |          |             |                                                                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|-------------|--------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |             | 31                                                                                                     | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |          |             |                                                                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |             | 0                                                                                                      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |
| ID               | Acce Field | Value ID | Value       | Description                                                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | R          | AMOUNT   | [1..0xFFFF] | Number of bytes transferred in the last transaction. In case of NACK error, includes the NACK'ed byte. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.37.8.41 TXD.LIST

Address offset: 0x550

EasyDMA list type

|                  |            |           |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|-----------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |           |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |           |       | A A A                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |           |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID  | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | LIST      |       | List type                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled  | 0     | Disable EasyDMA list                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | ArrayList | 1     | Use array list                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.37.8.42 ADDRESS

Address offset: 0x588

Address used in the TWI transfer

|                  |            |  |  |          |  |  |                                  |  |  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|--|----------|--|--|----------------------------------|--|--|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |  |          |  |  |                                  |  |  | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |  |  |          |  |  |                                  |  |  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  | A  | A | A | A | A | A | A |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |  |          |  |  |                                  |  |  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  |  | Value ID |  |  | Value                            |  |  | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW ADDRESS |  |  |          |  |  | Address used in the TWI transfer |  |  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

## 7.1.37.9 Electrical specification

### 7.1.37.9.1 TWIM interface electrical specifications

| Symbol                  | Description                                            | Min. | Typ. | Max. | Units |
|-------------------------|--------------------------------------------------------|------|------|------|-------|
| f <sub>TWIM,SCL</sub>   | Bit rates for TWIM <sup>25</sup>                       | ..   | ..   | ..   | kbps  |
| t <sub>TWIM,START</sub> | Time from STARTRX/STARTTX task to transmission started | ..   | ..   | ..   | µs    |

### 7.1.37.9.2 Two Wire Interface Master (TWIM) timing specifications

| Symbol                            | Description                                                             | Min. | Typ. | Max. | Units |
|-----------------------------------|-------------------------------------------------------------------------|------|------|------|-------|
| t <sub>TWIM,SU_DAT</sub>          | Data setup time before positive edge on SCL – all modes                 | ..   | ..   | ..   | ns    |
| t <sub>TWIM,HD_DAT</sub>          | Data hold time after negative edge on SCL – all modes                   | ..   | ..   | ..   | ns    |
| t <sub>TWIM,HD_STA,100kbps</sub>  | TWIM master hold time for START and repeated START condition, 100 kbps  | ..   | ..   | ..   | ns    |
| t <sub>TWIM,HD_STA,250kbps</sub>  | TWIM master hold time for START and repeated START condition, 250kbps   | ..   | ..   | ..   | ns    |
| t <sub>TWIM,HD_STA,400kbps</sub>  | TWIM master hold time for START and repeated START condition, 400 kbps  | ..   | ..   | ..   | ns    |
| t <sub>TWIM,HD_STA,1000kbps</sub> | TWIM master hold time for START and repeated START condition, 1000 kbps | ..   | ..   | ..   | ns    |
| t <sub>TWIM,SU_STO,100kbps</sub>  | TWIM master setup time from SCL high to STOP condition, 100 kbps        | ..   | ..   | ..   | ns    |
| t <sub>TWIM,SU_STO,250kbps</sub>  | TWIM master setup time from SCL high to STOP condition, 250 kbps        | ..   | ..   | ..   | ns    |
| t <sub>TWIM,SU_STO,400kbps</sub>  | TWIM master setup time from SCL high to STOP condition, 400 kbps        | ..   | ..   | ..   | ns    |
| t <sub>TWIM,SU_STO,1000kbps</sub> | TWIM master setup time from SCL high to STOP condition, 1000 kbps       | ..   | ..   | ..   | ns    |
| t <sub>TWIM,BUF,100kbps</sub>     | TWIM master bus free time between STOP and START conditions, 100 kbps   | ..   | ..   | ..   | ns    |
| t <sub>TWIM,BUF,250kbps</sub>     | TWIM master bus free time between STOP and START conditions, 250 kbps   | ..   | ..   | ..   | ns    |
| t <sub>TWIM,BUF,400kbps</sub>     | TWIM master bus free time between STOP and START conditions, 400 kbps   | ..   | ..   | ..   | ns    |
| t <sub>TWIM,BUF,1000kbps</sub>    | TWIM master bus free time between STOP and START conditions, 1000 kbps  | ..   | ..   | ..   | ns    |

<sup>25</sup> High bit rates or stronger pull-ups may require GPIOs to be set as High Drive, see GPIO chapter for more details.

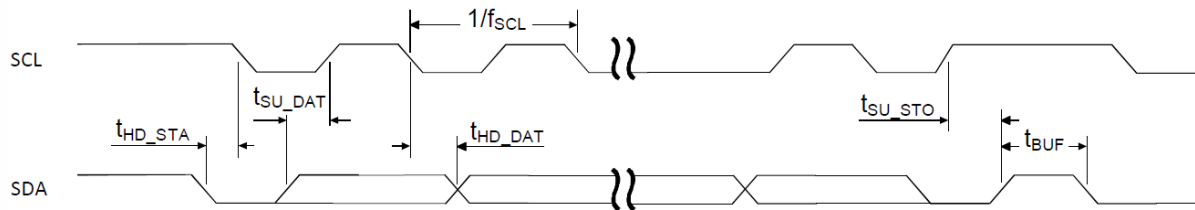


Figure 213: TWIM timing diagram, 1 byte transaction

### 7.1.37.10 Pullup resistor

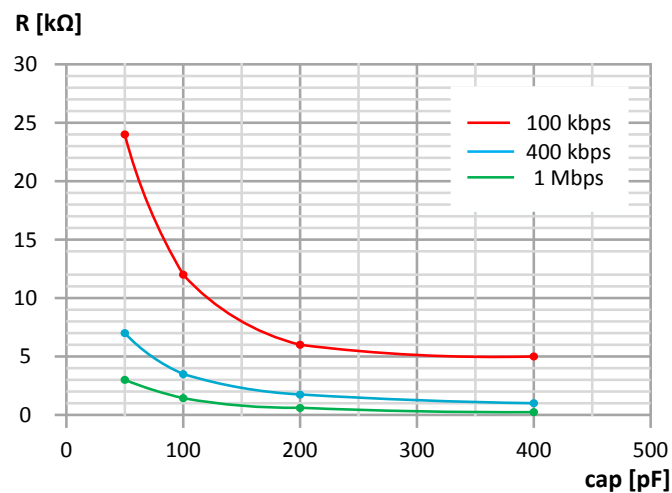


Figure 214: Recommended TWIM pullup value vs. line capacitance

- The I2C specification allows a line capacitance of 400 pF at most.
- The value of internal pullup resistor ( $R_{PU}$ ) for nRF5340 can be found in [GPIO — General purpose input/output](#) on page 209.

## 7.1.38 TWIS — I<sup>2</sup>C compatible two-wire interface slave with EasyDMA

TWI slave with EasyDMA (TWIS) is compatible with I<sup>2</sup>C operating at 100 kHz and 400 kHz. The TWI transmitter and receiver implement EasyDMA.

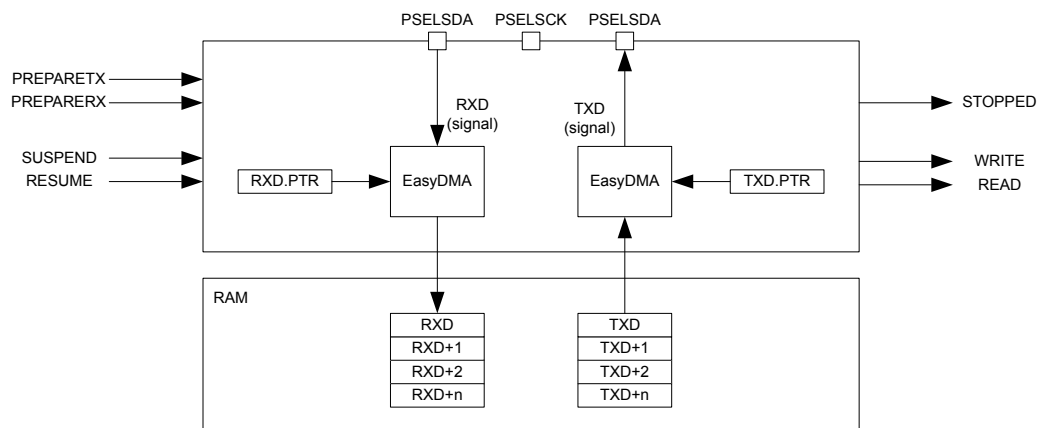


Figure 215: TWI slave with EasyDMA

A typical TWI setup consists of one master and one or more slaves. For an example, see [Figure 216: A typical TWI setup comprising one master and three slaves](#) on page 632. TWIS is only able to operate with a single master on the TWI bus.

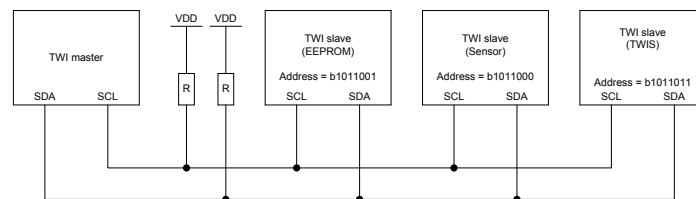


Figure 216: A typical TWI setup comprising one master and three slaves

The TWI slave state machine is illustrated in [Figure 217: TWI slave state machine](#) on page 633 and [Table 168: TWI slave state machine symbols](#) on page 633 is explaining the different symbols used in the state machine.

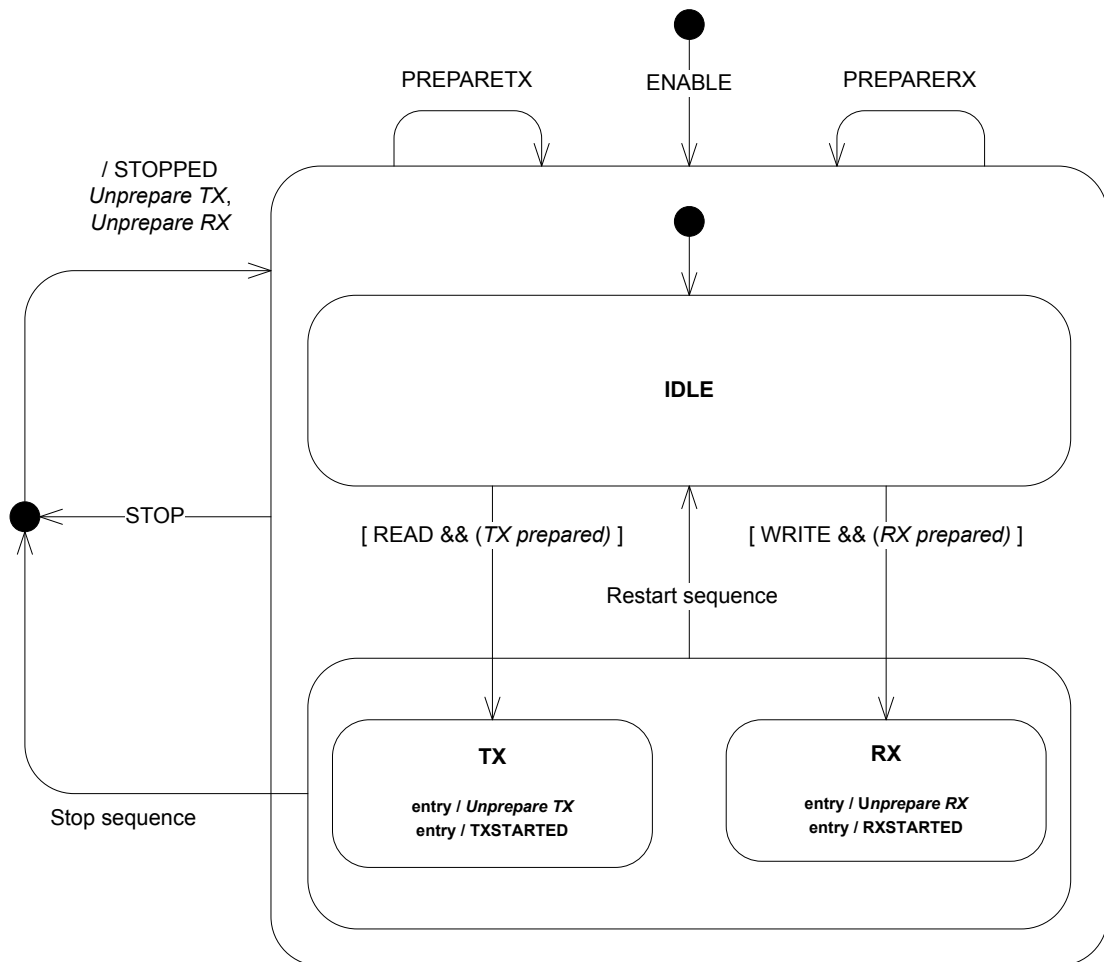


Figure 217: TWI slave state machine

| Symbol           | Type         | Description                                                                                                                    |
|------------------|--------------|--------------------------------------------------------------------------------------------------------------------------------|
| ENABLE           | Register     | The TWI slave has been enabled via the <a href="#">ENABLE</a> register                                                         |
| PREPARETX        | Task         | The <a href="#">TASKS_PREPARETX</a> task has been triggered                                                                    |
| STOP             | Task         | The <a href="#">TASKS_STOP</a> task has been triggered                                                                         |
| PREPARERX        | Task         | The <a href="#">TASKS_PREPARERX</a> task has been triggered                                                                    |
| STOPPED          | Event        | The <a href="#">EVENTS_STOPPED</a> event was generated                                                                         |
| RXSTARTED        | Event        | The <a href="#">EVENTS_RXSTARTED</a> event was generated                                                                       |
| TXSTARTED        | Event        | The <a href="#">EVENTS_TXSTARTED</a> event was generated                                                                       |
| TX prepared      | Internal     | Internal flag indicating that a <a href="#">TASKS_PREPARETX</a> task has been triggered. This flag is not visible to the user. |
| RX prepared      | Internal     | Internal flag indicating that a <a href="#">TASKS_PREPARERX</a> task has been triggered. This flag is not visible to the user. |
| Unprepare TX     | Internal     | Clears the internal 'TX prepared' flag until next <a href="#">TASKS_PREPARETX</a> task.                                        |
| Unprepare RX     | Internal     | Clears the internal 'RX prepared' flag until next <a href="#">TASKS_PREPARERX</a> task.                                        |
| Stop sequence    | TWI protocol | A TWI stop sequence was detected                                                                                               |
| Restart sequence | TWI protocol | A TWI restart sequence was detected                                                                                            |

Table 168: TWI slave state machine symbols

The TWI slave supports clock stretching performed by the master.

The TWI slave operates in a low power mode while waiting for a TWI master to initiate a transfer. As long as the TWI slave is not addressed, it will remain in this low power mode.

To secure correct behaviour of the TWI slave, PSEL.SCL, PSEL.SDA, CONFIG and the ADDRESS[n] registers, must be configured prior to enabling the TWI slave through the ENABLE register. Similarly, changing these settings must be performed while the TWI slave is disabled. Failing to do so may result in unpredictable behaviour.

### 7.1.38.1 Shared resources

The TWI slave shares registers and other resources with other peripherals that have the same ID as the TWI slave.

Therefore, you must disable all peripherals that have the same ID as the TWI slave before the TWI slave can be configured and used. Disabling a peripheral that has the same ID as the TWI slave will not reset any of the registers that are shared with the TWI slave. It is therefore important to configure all relevant registers explicitly to secure that the TWI slave operates correctly.

The Instantiation table in [Instantiation](#) on page 136 shows which peripherals have the same ID as the TWI slave.

### 7.1.38.2 EasyDMA

The TWIS implements EasyDMA for accessing RAM without CPU involvement.

The TWIS peripheral implements the following EasyDMA channels:

| Channel | Type   | Register Cluster |
|---------|--------|------------------|
| TXD     | READER | TXD              |
| RXD     | WRITER | RXD              |

Table 169: TWIS EasyDMA Channels

For detailed information regarding the use of EasyDMA, see [EasyDMA](#) on page 140.

The STOPPED event indicates that EasyDMA has finished accessing the buffer in RAM.

### 7.1.38.3 TWI slave responding to a read command

Before the TWI slave can respond to a read command the TWI slave must be configured correctly and enabled via the ENABLE register. When enabled the TWI slave will be in its IDLE state where it will consume  $I_{IDLE}$ .

A read command is started when the TWI master generates a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 1 (WRITE=0, READ=1). The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK=1) response from the TWI slave.

The TWI slave is able to listen for up to two addresses at the same time. Which addresses to listen for is configured in the ADDRESS registers and the CONFIG register.

The TWI slave will only acknowledge (ACK) the read command if the address presented by the master matches one of the addresses the slave is configured to listen for. The TWI slave will generate a READ event when it acknowledges the read command.

The TWI slave is only able to detect a read command from the IDLE state.

The TWI slave will set an internal 'TX prepared' flag when the PREPARETX task is triggered.

When the read command is received the TWI slave will enter the TX state if the internal 'TX prepared' flag is set.

If the internal 'TX prepared' flag is not set when the read command is received, the TWI slave will stretch the master's clock until the PREPARETX task is triggered and the internal 'TX prepared' flag is set.

The TWI slave will generate the TXSTARTED event and clear the 'TX prepared' flag ('unprepare TX') when it enters the TX state. In this state the TWI slave will send the data bytes found in the transmit buffer to the master using the master's clock. The TWI slave will consume  $I_{TX}$  in this mode.

The TWI slave will go back to the IDLE state if the TWI slave receives a restart command when it is in the TX state.

The TWI slave is stopped when it receives the stop condition from the TWI master. A STOPPED event will be generated when the transaction has stopped. The TWI slave will clear the 'TX prepared' flag ('unprepare TX') and go back to the IDLE state when it has stopped.

The transmit buffer is located in RAM at the address specified in the TXD.PTR register. The TWI slave will only be able to send TXD.MAXCNT bytes from the transmit buffer for each transaction. If the TWI master forces the slave to send more than TXD.MAXCNT bytes, the slave will send the byte specified in the ORC register to the master instead. If this happens, an ERROR event will be generated.

The EasyDMA configuration registers, see TXD.PTR etc., are latched when the TXSTARTED event is generated.

The TWI slave can be forced to stop by triggering the STOP task. A STOPPED event will be generated when the TWI slave has stopped. The TWI slave will clear the 'TX prepared' flag and go back to the IDLE state when it has stopped, see also [Terminating an ongoing TWI transaction](#) on page 637.

Each byte sent from the slave will be followed by an ACK/NACK bit sent from the master. The TWI master will generate a NACK following the last byte that it wants to receive to tell the slave to release the bus so that the TWI master can generate the stop condition. The TXD.AMOUNT register can be queried after a transaction to see how many bytes were sent.

A typical TWI slave read command response is illustrated in [Figure 218: The TWI slave responding to a read command](#) on page 635. Occurrence 2 in the figure illustrates clock stretching performed by the TWI slave following a SUSPEND task.

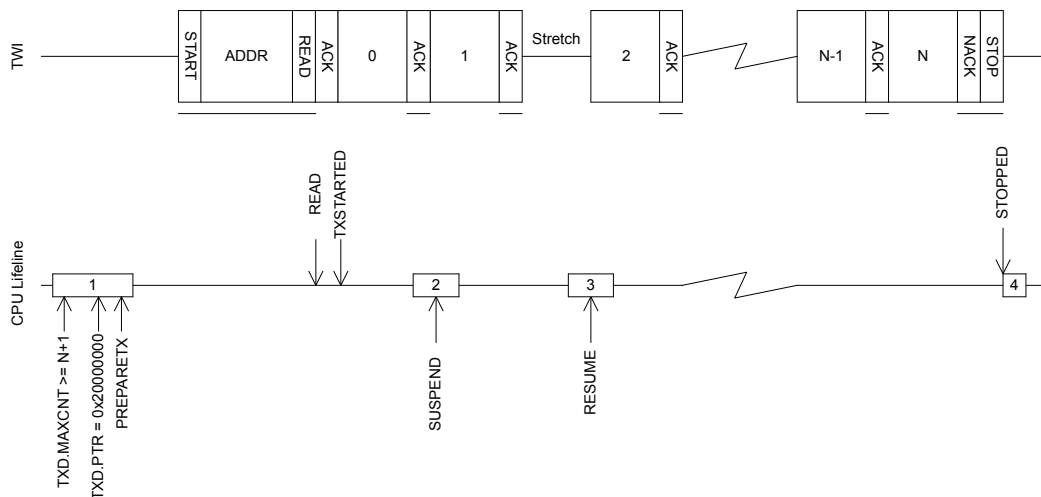


Figure 218: The TWI slave responding to a read command

#### 7.1.38.4 TWI slave responding to a write command

Before the TWI slave can respond to a write command the TWI slave must be configured correctly and enabled via the ENABLE register. When enabled the TWI slave will be in its IDLE state where it will consume  $I_{IDLE}$ .

A write command is started when the TWI master generates a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 0 (WRITE=0, READ=1). The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK=1) response from the slave.

The TWI slave is able to listen for up to two addresses at the same time. Which addresses to listen for is configured in the ADDRESS registers and the CONFIG register.

The TWI slave will only acknowledge (ACK) the write command if the address presented by the master matches one of the addresses the slave is configured to listen for. The TWI slave will generate a WRITE event if it acknowledges the write command.

The TWI slave is only able to detect a write command from the IDLE state.

The TWI slave will set an internal 'RX prepared' flag when the PREPARERX task is triggered.

When the write command is received the TWI slave will enter the RX state if the internal 'RX prepared' flag is set.

If the internal 'RX prepared' flag is not set when the write command is received, the TWI slave will stretch the master's clock until the PREPARERX task is triggered and the internal 'RX prepared' flag is set.

The TWI slave will generate the RXSTARTED event and clear the internal 'RX prepared' flag ('unprepare RX') when it enters the RX state. In this state the TWI slave will be able to receive the bytes sent by the TWI master. The TWI slave will consume I<sub>RX</sub> in this mode.

The TWI slave will go back to the IDLE state if the TWI slave receives a restart command when it is in the RX state.

The TWI slave is stopped when it receives the stop condition from the TWI master. A STOPPED event will be generated when the transaction has stopped. The TWI slave will clear the internal 'RX prepared' flag ('unprepare RX') and go back to the IDLE state when it has stopped.

The receive buffer is located in RAM at the address specified in the TXD.PTR register. The TWI slave will only be able to receive as many bytes as specified in the RXD.MAXCNT register. If the TWI master tries to send more bytes to the slave than the slave is able to receive, these bytes will be discarded and the bytes will be NACKed by the slave. If this happens, an ERROR event will be generated.

The EasyDMA configuration registers, see RXD.PTR etc., are latched when the RXSTARTED event is generated.

The TWI slave can be forced to stop by triggering the STOP task. A STOPPED event will be generated when the TWI slave has stopped. The TWI slave will clear the internal 'RX prepared' flag and go back to the IDLE state when it has stopped, see also [Terminating an ongoing TWI transaction](#) on page 637.

The TWI slave will generate an ACK after every byte received from the master. The RXD.AMOUNT register can be queried after a transaction to see how many bytes were received.

A typical TWI slave write command response is illustrated in [Figure 219: The TWI slave responding to a write command](#) on page 637. Occurrence 2 in the figure illustrates clock stretching performed by the TWI slave following a SUSPEND task.



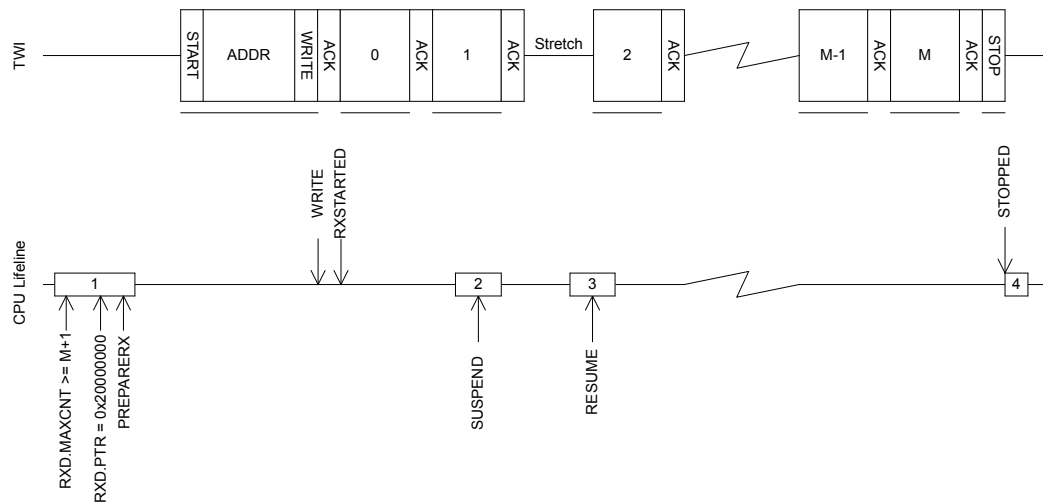


Figure 219: The TWI slave responding to a write command

### 7.1.38.5 Master repeated start sequence

An example of a repeated start sequence is one in which the TWI master writes two bytes to the slave followed by reading four bytes from the slave.

This is illustrated in [Figure 220: A repeated start sequence, where the TWI master writes two bytes followed by reading four bytes from the slave](#) on page 637.

It is here assumed that the receiver does not know in advance what the master wants to read, and that this information is provided in the first two bytes received in the write part of the repeated start sequence. To guarantee that the CPU is able to process the received data before the TWI slave starts to reply to the read command, the SUSPEND task is triggered via a shortcut from the READ event generated when the read command is received. When the CPU has processed the incoming data and prepared the correct data response, the CPU will resume the transaction by triggering the RESUME task.

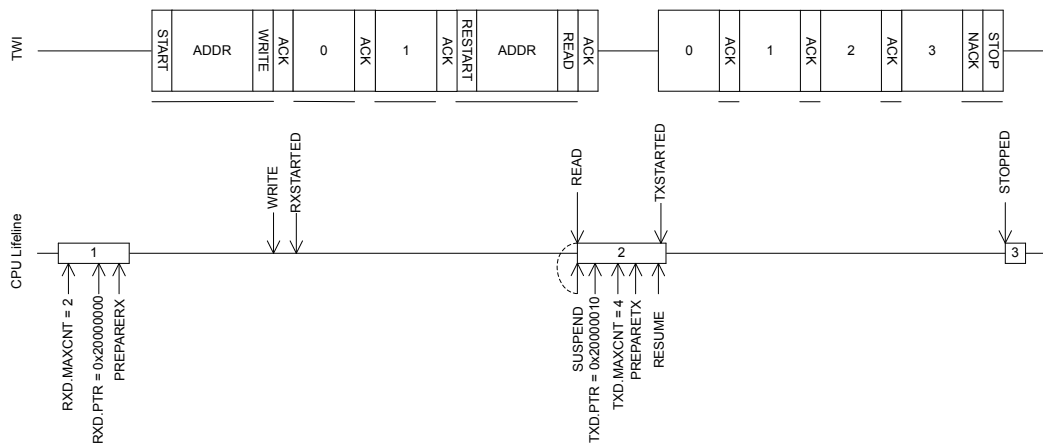


Figure 220: A repeated start sequence, where the TWI master writes two bytes followed by reading four bytes from the slave

### 7.1.38.6 Terminating an ongoing TWI transaction

In some situations, e.g. if the external TWI master is not responding correctly, it may be required to terminate an ongoing transaction.

This can be achieved by triggering the STOP task. In this situation a STOPPED event will be generated when the TWI has stopped independent of whether or not a STOP condition has been generated on the TWI bus. The TWI slave will release the bus when it has stopped and go back to its IDLE state.

### 7.1.38.7 Low power

When putting the system in low power and the peripheral is not needed, lowest possible power consumption is achieved by stopping, and then disabling the peripheral.

The STOP task may not be always needed (the peripheral might already be stopped), but if it is sent, software shall wait until the STOPPED event was received as a response before disabling the peripheral through the ENABLE register.

### 7.1.38.8 Slave mode pin configuration

The SCL and SDA signals associated with the TWI slave are mapped to physical pins according to the configuration specified in the PSEL.SCL and PSEL.SDA registers respectively.

The PSEL.SCL and PSEL.SDA registers and their configurations are only used as long as the TWI slave is enabled, and retained only as long as the device is in ON mode. When the peripheral is disabled, the pins will behave as regular GPIOs, and use the configuration in their respective OUT bit field and PIN\_CNF[n] register. PSEL.SCL and PSEL.SDA must only be configured when the TWI slave is disabled.

To secure correct signal levels on the pins used by the TWI slave when the system is in OFF mode, and when the TWI slave is disabled, these pins must be configured in the GPIO peripheral as described in [Table 170: GPIO configuration before enabling peripheral](#) on page 638.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

| TWI slave signal | TWI slave pin            | Direction | Output value   | Drive strength |
|------------------|--------------------------|-----------|----------------|----------------|
| SCL              | As specified in PSEL.SCL | Input     | Not applicable | S0D1           |
| SDA              | As specified in PSEL.SDA | Input     | Not applicable | S0D1           |

Table 170: GPIO configuration before enabling peripheral

### 7.1.38.9 Registers

| Base address | Domain      | Peripheral | Instance   | Secure mapping | DMA security | Description                | Configuration |
|--------------|-------------|------------|------------|----------------|--------------|----------------------------|---------------|
| 0x50008000   | APPLICATION | TWIS       | TWIS0 : S  | US             | SA           | Two-wire interface slave 0 |               |
| 0x40008000   |             |            | TWIS0 : NS |                |              |                            |               |
| 0x50009000   | APPLICATION | TWIS       | TWIS1 : S  | US             | SA           | Two-wire interface slave 1 |               |
| 0x40009000   |             |            | TWIS1 : NS |                |              |                            |               |
| 0x41013000   | NETWORK     | TWIS       | TWIS0      | NS             | NA           | Two-wire interface slave 0 |               |

Table 171: Instances

| Register            | Offset | Security | Description                                                |
|---------------------|--------|----------|------------------------------------------------------------|
| TASKS_STOP          | 0x014  |          | Stop TWI transaction                                       |
| TASKS_SUSPEND       | 0x01C  |          | Suspend TWI transaction                                    |
| TASKS_RESUME        | 0x020  |          | Resume TWI transaction                                     |
| TASKS_PREPARERX     | 0x030  |          | Prepare the TWI slave to respond to a write command        |
| TASKS_PREPARETX     | 0x034  |          | Prepare the TWI slave to respond to a read command         |
| SUBSCRIBE_STOP      | 0x094  |          | Subscribe configuration for task <a href="#">STOP</a>      |
| SUBSCRIBE_SUSPEND   | 0x09C  |          | Subscribe configuration for task <a href="#">SUSPEND</a>   |
| SUBSCRIBE_RESUME    | 0x0A0  |          | Subscribe configuration for task <a href="#">RESUME</a>    |
| SUBSCRIBE_PREPARERX | 0x0B0  |          | Subscribe configuration for task <a href="#">PREPARERX</a> |
| SUBSCRIBE_PREPARETX | 0x0B4  |          | Subscribe configuration for task <a href="#">PREPARETX</a> |
| EVENTS_STOPPED      | 0x104  |          | TWI stopped                                                |
| EVENTS_ERROR        | 0x124  |          | TWI error                                                  |

| Register          | Offset | Security | Description                                                                             |
|-------------------|--------|----------|-----------------------------------------------------------------------------------------|
| EVENTS_RXSTARTED  | 0x14C  |          | Receive sequence started                                                                |
| EVENTS_TXSTARTED  | 0x150  |          | Transmit sequence started                                                               |
| EVENTS_WRITE      | 0x164  |          | Write command received                                                                  |
| EVENTS_READ       | 0x168  |          | Read command received                                                                   |
| PUBLISH_STOPPED   | 0x184  |          | Publish configuration for event STOPPED                                                 |
| PUBLISH_ERROR     | 0x1A4  |          | Publish configuration for event ERROR                                                   |
| PUBLISH_RXSTARTED | 0x1CC  |          | Publish configuration for event RXSTARTED                                               |
| PUBLISH_TXSTARTED | 0x1D0  |          | Publish configuration for event TXSTARTED                                               |
| PUBLISH_WRITE     | 0x1E4  |          | Publish configuration for event WRITE                                                   |
| PUBLISH_READ      | 0x1E8  |          | Publish configuration for event READ                                                    |
| SHORTS            | 0x200  |          | Shortcuts between local events and tasks                                                |
| INTEN             | 0x300  |          | Enable or disable interrupt                                                             |
| INTENSET          | 0x304  |          | Enable interrupt                                                                        |
| INTENCLR          | 0x308  |          | Disable interrupt                                                                       |
| ERRORSRC          | 0x4D0  |          | Error source                                                                            |
| MATCH             | 0x4D4  |          | Status register indicating which address had a match                                    |
| ENABLE            | 0x500  |          | Enable TWIS                                                                             |
| PSEL_SCL          | 0x508  |          | Pin select for SCL signal                                                               |
| PSEL_SDA          | 0x50C  |          | Pin select for SDA signal                                                               |
| RXD.PTR           | 0x534  |          | RXD Data pointer                                                                        |
| RXD.MAXCNT        | 0x538  |          | Maximum number of bytes in RXD buffer                                                   |
| RXD.AMOUNT        | 0x53C  |          | Number of bytes transferred in the last RXD transaction                                 |
| RXD.LIST          | 0x540  |          | EasyDMA list type                                                                       |
| TXD.PTR           | 0x544  |          | TXD Data pointer                                                                        |
| TXD.MAXCNT        | 0x548  |          | Maximum number of bytes in TXD buffer                                                   |
| TXD.AMOUNT        | 0x54C  |          | Number of bytes transferred in the last TXD transaction                                 |
| TXD.LIST          | 0x550  |          | EasyDMA list type                                                                       |
| ADDRESS[n]        | 0x588  |          | TWI slave address n                                                                     |
| CONFIG            | 0x594  |          | Configuration register for the address match mechanism                                  |
| ORC               | 0x5C0  |          | Over-read character. Character sent out in case of an over-read of the transmit buffer. |

Table 172: Register overview

### 7.1.38.9.1 TASKS\_STOP

Address offset: 0x014

Stop TWI transaction

| Bit number |            | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |         |    |       |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
|------------|------------|---------------------------------------------------------------------------------------|---------|----|-------|----------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|
| ID         |            |                                                                                       |         |    |       |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A |
| Reset      | 0x00000000 | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |         |    |       |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| ID         | Acce       | Field                                                                                 | Value   | ID | Value | Description          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| A          | W          | TASKS_STOP                                                                            |         |    |       | Stop TWI transaction |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
|            |            |                                                                                       | Trigger |    | 1     | Trigger task         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |

### 7.1.38.9.2 TASKS\_SUSPEND

Address offset: 0x01C

Suspend TWI transaction

|                  |            |               |  |          |         |  |       |   |  |              |                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|---------------|--|----------|---------|--|-------|---|--|--------------|-------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |               |  |          |         |  |       |   |  | 31           | 30                      | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |               |  |          |         |  |       |   |  |              |                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |
| Reset 0x00000000 |            |               |  |          |         |  |       |   |  | 0            | 0                       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |               |  | Value ID |         |  | Value |   |  | Description  |                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_SUSPEND |  |          | Trigger |  |       | 1 |  |              | Suspend TWI transaction |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |               |  |          |         |  |       |   |  | Trigger task |                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.38.9.3 TASKS\_RESUME

Address offset: 0x020

Resume TWI transaction

|                  |            |              |  |          |         |  |       |   |  |              |                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------------|--|----------|---------|--|-------|---|--|--------------|------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |              |  |          |         |  |       |   |  | 31           | 30                     | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |              |  |          |         |  |       |   |  |              |                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |
| Reset 0x00000000 |            |              |  |          |         |  |       |   |  | 0            | 0                      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |              |  | Value ID |         |  | Value |   |  | Description  |                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_RESUME |  |          | Trigger |  |       | 1 |  |              | Resume TWI transaction |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |              |  |          |         |  |       |   |  | Trigger task |                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.38.9.4 TASKS\_PREPARERX

Address offset: 0x030

Prepare the TWI slave to respond to a write command

|                  |            |                 |  |          |         |  |       |   |  |              |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-----------------|--|----------|---------|--|-------|---|--|--------------|-----------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                 |  |          |         |  |       |   |  | 31           | 30                                                  | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |                 |  |          |         |  |       |   |  |              |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |
| Reset 0x00000000 |            |                 |  |          |         |  |       |   |  | 0            | 0                                                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |                 |  | Value ID |         |  | Value |   |  | Description  |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_PREPARERX |  |          | Trigger |  |       | 1 |  |              | Prepare the TWI slave to respond to a write command |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |                 |  |          |         |  |       |   |  | Trigger task |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.38.9.5 TASKS\_PREPARETX

Address offset: 0x034

Prepare the TWI slave to respond to a read command

|                  |            |                 |  |          |         |  |       |   |  |              |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-----------------|--|----------|---------|--|-------|---|--|--------------|----------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                 |  |          |         |  |       |   |  | 31           | 30                                                 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |                 |  |          |         |  |       |   |  |              |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |
| Reset 0x00000000 |            |                 |  |          |         |  |       |   |  | 0            | 0                                                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |                 |  | Value ID |         |  | Value |   |  | Description  |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_PREPARETX |  |          | Trigger |  |       | 1 |  |              | Prepare the TWI slave to respond to a read command |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |                 |  |          |         |  |       |   |  | Trigger task |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.38.9.6 SUBSCRIBE\_STOP

Address offset: 0x094

Subscribe configuration for task STOP

|                  |            |          |          |                                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|-------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                                                                      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |          |          | B                                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field | Value ID | Value    | Description                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] | Channel that task <span>STOP</span> will subscribe to                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |                                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        | Disable subscription                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        | Enable subscription                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.38.9.7 SUBSCRIBE\_SUSPEND

Address offset: 0x09C

Subscribe configuration for task **SUSPEND**

|                  |            |  |          |  |          |  |                                                          |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|--|----------|--|----------------------------------------------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          |  |          |  |                                                          |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |  |          |  |          |  |                                                          |  |  | B  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  | A  | A | A | A | A | A | A |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |          |  |          |  |                                                          |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID |  | Value    |  | Description                                              |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          |  | [255..0] |  | Channel that task <span>SUSPEND</span> will subscribe to |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |  |          |  |                                                          |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled |  | 0        |  | Disable subscription                                     |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  |  | 1        |  | Enable subscription                                      |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.38.9.8 SUBSCRIBE\_RESUME

Address offset: 0x0A0

Subscribe configuration for task **RESUME**

|                  |            |  |          |                                                                         |                      |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|-------------------------------------------------------------------------|----------------------|---------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31                                                                      | 30                   | 29                                                | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |  |          | B                                                                       |                      |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |                      |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field |  | Value ID | Value                                                                   |                      | Description                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          | [255..0]                                                                |                      | Channel that task <b>RESUME</b> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |                                                                         |                      |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled | 0                                                                       | Disable subscription |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  | 1                                                                       | Enable subscription  |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.38.9.9 SUBSCRIBE\_PREPARERX

Address offset: 0x0B0

Subscribe configuration for task **PREPARERX**

|                  |            |  |          |  |          |  |                                                      |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|--|----------|--|------------------------------------------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          |  |          |  |                                                      |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |  |          |  |          |  |                                                      |  |  | B  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  | A  | A | A | A | A | A | A |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |          |  |          |  |                                                      |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID |  | Value    |  | Description                                          |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          |  | [255..0] |  | Channel that task <b>PREPARERX</b> will subscribe to |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |  |          |  |                                                      |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled |  | 0        |  | Disable subscription                                 |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  |  | 1        |  | Enable subscription                                  |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.38.9.10 SUBSCRIBE\_PREPARETX

Address offset: 0x0B4

Subscribe configuration for task [PREPARETX](#)

|                  |            |          |                                                                                       |                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|---------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |          | B                                                                                     |                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                   |                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                              | Channel that task <a href="#">PREPARETX</a> will subscribe to |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |                                                                                       |                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Disable subscription                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Enable subscription                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

### 7.1.38.9.11 EVENTS\_STOPPED

Address offset: 0x104

TWI stopped

|                  |                   |              |                                                                                       |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|-------------------|--------------|---------------------------------------------------------------------------------------|---------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |                   |              | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |                   |              | A                                                                                     |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |                   |              | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field        | Value ID     | Value                                                                                 | Description         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW EVENTS_STOPPED |              |                                                                                       | TWI stopped         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                   | NotGenerated | 0                                                                                     | Event not generated |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                   | Generated    | 1                                                                                     | Event generated     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.38.9.12 EVENTS\_ERROR

Address offset: 0x124

TWI error

|                  |            |              |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|--------------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |              |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |              |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |              |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID     | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | EVENTS_ERROR |       | TWI error                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | NotGenerated | 0     | Event not generated                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Generated    | 1     | Event generated                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.38.9.13 EVENTS\_RXSTARTED

Address offset: 0x14C

Receive sequence started

|                  |            |                  |       |                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|------------------|------------|------------------|-------|--------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|---|
| Bit number       |            |                  |       | 31                       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |   |
| ID               |            |                  |       |                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | A |
| Reset 0x00000000 |            |                  |       | 0                        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |   |
| ID               | Acce Field | Value ID         | Value | Description              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
| A                | RW         | EVENTS_RXSTARTED |       | Receive sequence started |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | NotGenerated     | 0     | Event not generated      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | Generated        | 1     | Event generated          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |

#### 7.1.38.9.14 EVENTS\_TXSTARTED

Address offset: 0x150

Transmit sequence started

|                  |            |                  |       |                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|------------------|-------|---------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                  |       | 31                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |                  |       |                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |
| Reset 0x00000000 |            |                  |       | 0                         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID         | Value | Description               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | EVENTS_TXSTARTED |       | Transmit sequence started |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | NotGenerated     | 0     | Event not generated       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Generated        | 1     | Event generated           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.38.9.15 EVENTS\_WRITE

Address offset: 0x164

Write command received

|                  |            |              |       |                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|------------------|------------|--------------|-------|------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|---|
| Bit number       |            |              |       | 31                     | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |   |
| ID               |            |              |       |                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | A |
| Reset 0x00000000 |            |              |       | 0                      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |   |
| ID               | Acce Field | Value ID     | Value | Description            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
| A                | RW         | EVENTS_WRITE |       | Write command received |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | NotGenerated | 0     | Event not generated    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | Generated    | 1     | Event generated        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |

#### 7.1.38.9.16 EVENTS\_READ

Address offset: 0x168

Read command received

|                  |            |              |       |                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|------------------|------------|--------------|-------|-----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|---|
| Bit number       |            |              |       | 31                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |   |
| ID               |            |              |       |                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | A |
| Reset 0x00000000 |            |              |       | 0                     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |   |
| ID               | Acce Field | Value ID     | Value | Description           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
| A                | RW         | EVENTS_READ  |       | Read command received |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | NotGenerated | 0     | Event not generated   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |
|                  |            | Generated    | 1     | Event generated       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |

#### 7.1.38.9.17 PUBLISH\_STOPPED

Address offset: 0x184

Publish configuration for event STOPPED

|                  |            |  |          |          |                    |                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|----------|--------------------|---------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31       | 30                 | 29                                          | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |  |          | B        |                    |                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |          | 0        | 0                  | 0                                           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce Field |  | Value ID | Value    |                    | Description                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          | [255..0] |                    | Channel that event STOPPED will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |          |                    |                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled | 0        | Disable publishing |                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  | 1        | Enable publishing  |                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.38.9.18 PUBLISH\_ERROR

Address offset: 0x1A4

Publish configuration for event **ERROR**

|                  |            |  |          |  |          |  |                                                  |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|--|----------|--|--------------------------------------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          |  |          |  |                                                  |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |
| ID               |            |  |          |  |          |  |                                                  |  |  | B  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  |    |    |    |   |   |   |   |   |   | A | A | A | A | A | A | A |   |
| Reset 0x00000000 |            |  |          |  |          |  |                                                  |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID |  | Value    |  | Description                                      |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          |  | [255..0] |  | Channel that event <b>ERROR</b> will publish to. |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |  |          |  |                                                  |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled |  | 0        |  | Disable publishing                               |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  |  | 1        |  | Enable publishing                                |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.38.9.19 PUBLISH\_RXSTARTED

Address offset: 0x1CC

Publish configuration for event **RXSTARTED**

|                  |            |          |          |          |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|----------|----|------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31       | 30 | 29                                                   | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |          |          | B        |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |          | 0        | 0  | 0                                                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce Field |          | Value ID | Value    |    | Description                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          |          | [255..0] |    | Channel that event <b>RXSTARTED</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |          |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled |          | 0        |    | Disable publishing                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  |          | 1        |    | Enable publishing                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.38.9.20 PUBLISH\_TXSTARTED

Address offset: 0x1D0

Publish configuration for event **TXSTARTED**

|                  |            |  |          |          |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|----------|----|------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31       | 30 | 29                                                   | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |  |          | B        |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |          | 0        |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID | Value    |    | Description                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          | [255..0] |    | Channel that event <b>TXSTARTED</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |          |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled | 0        |    | Disable publishing                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  | 1        |    | Enable publishing                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |





| Bit number       |              |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                 |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|------------------|--------------|----------|---------------------------------------------------------------------------------------|-------------------------------------------------|--|--|--|--|--|--|-----|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|
| ID               |              |          | H G                                                                                   |                                                 |  |  |  |  |  |  | F E |  |  |  |  |  |  |  | B |  |  |  |  |  |  |  | A |  |  |  |  |  |  |  |
| Reset 0x00000000 |              |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                 |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
| ID               | Acce Field   | Value ID | Value                                                                                 | Description                                     |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
| A                | RW STOPPED   |          |                                                                                       | Enable or disable interrupt for event STOPPED   |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |              | Disabled | 0                                                                                     | Disable                                         |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |              | Enabled  | 1                                                                                     | Enable                                          |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
| B                | RW ERROR     |          |                                                                                       | Enable or disable interrupt for event ERROR     |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |              | Disabled | 0                                                                                     | Disable                                         |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |              | Enabled  | 1                                                                                     | Enable                                          |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
| E                | RW RXSTARTED |          |                                                                                       | Enable or disable interrupt for event RXSTARTED |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |              | Disabled | 0                                                                                     | Disable                                         |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |              | Enabled  | 1                                                                                     | Enable                                          |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
| F                | RW TXSTARTED |          |                                                                                       | Enable or disable interrupt for event TXSTARTED |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |              | Disabled | 0                                                                                     | Disable                                         |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |              | Enabled  | 1                                                                                     | Enable                                          |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
| G                | RW WRITE     |          |                                                                                       | Enable or disable interrupt for event WRITE     |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |              | Disabled | 0                                                                                     | Disable                                         |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |              | Enabled  | 1                                                                                     | Enable                                          |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
| H                | RW READ      |          |                                                                                       | Enable or disable interrupt for event READ      |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |              | Disabled | 0                                                                                     | Disable                                         |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |              | Enabled  | 1                                                                                     | Enable                                          |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |

### 7.1.38.9.25 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number       |              |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                   |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|------------------|--------------|----------|---------------------------------------------------------------------------------------|---------------------------------------------------|--|--|--|--|--|--|-----|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|
| ID               |              |          | H G                                                                                   |                                                   |  |  |  |  |  |  | F E |  |  |  |  |  |  |  | B |  |  |  |  |  |  |  | A |  |  |  |  |  |  |  |
| Reset 0x00000000 |              |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                   |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
| ID               | Acce Field   | Value ID | Value                                                                                 | Description                                       |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
| A                | RW STOPPED   |          |                                                                                       | Write '1' to enable interrupt for event STOPPED   |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |              | Set      | 1                                                                                     | Enable                                            |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |              | Disabled | 0                                                                                     | Read: Disabled                                    |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |              | Enabled  | 1                                                                                     | Read: Enabled                                     |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
| B                | RW ERROR     |          |                                                                                       | Write '1' to enable interrupt for event ERROR     |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |              | Set      | 1                                                                                     | Enable                                            |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |              | Disabled | 0                                                                                     | Read: Disabled                                    |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |              | Enabled  | 1                                                                                     | Read: Enabled                                     |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
| E                | RW RXSTARTED |          |                                                                                       | Write '1' to enable interrupt for event RXSTARTED |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |              | Set      | 1                                                                                     | Enable                                            |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |              | Disabled | 0                                                                                     | Read: Disabled                                    |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |              | Enabled  | 1                                                                                     | Read: Enabled                                     |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
| F                | RW TXSTARTED |          |                                                                                       | Write '1' to enable interrupt for event TXSTARTED |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |              | Set      | 1                                                                                     | Enable                                            |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |              | Disabled | 0                                                                                     | Read: Disabled                                    |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |              | Enabled  | 1                                                                                     | Read: Enabled                                     |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
| G                | RW WRITE     |          |                                                                                       | Write '1' to enable interrupt for event WRITE     |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |              | Set      | 1                                                                                     | Enable                                            |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |              | Disabled | 0                                                                                     | Read: Disabled                                    |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |              | Enabled  | 1                                                                                     | Read: Enabled                                     |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
| H                | RW READ      |          |                                                                                       | Write '1' to enable interrupt for event READ      |  |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |

| Bit number       |            |          | 31    | 30 | 29 | 28 | 27             | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |  |   |  |  |  |
|------------------|------------|----------|-------|----|----|----|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|--|---|--|--|--|
| ID               |            |          |       |    |    |    | H              |    |    |    | G  |    |    |    |    |    |    |    | F  |    |    |    | E  |    |   |   |   |   |   |   | B |   |   |   |   |  |  |  | A |  |  |  |
| Reset 0x00000000 |            |          | 0     | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |   |  |  |  |
| ID               | Acce Field | Value ID | Value |    |    |    | Description    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |  |  |
|                  |            | Set      | 1     |    |    |    | Enable         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |  |  |
|                  |            | Disabled | 0     |    |    |    | Read: Disabled |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |  |  |
|                  |            | Enabled  | 1     |    |    |    | Read: Enabled  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |  |  |

### 7.1.38.9.26 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number       |      |           | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                                    |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|------------------|------|-----------|---------------------------------------------------------------------------------------|-------|--------------------------------------------------------------------|--|--|--|--|--|-----|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|
| ID               |      |           | H G                                                                                   |       |                                                                    |  |  |  |  |  | F E |  |  |  |  |  |  |  | B |  |  |  |  |  |  |  | A |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |           | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |       |                                                                    |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
| ID               | Acce | Field     | Value ID                                                                              | Value | Description                                                        |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
| A                | RW   | STOPPED   |                                                                                       |       | Write '1' to disable interrupt for event <a href="#">STOPPED</a>   |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |      |           | Clear                                                                                 | 1     | Disable                                                            |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |      |           | Disabled                                                                              | 0     | Read: Disabled                                                     |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |      |           | Enabled                                                                               | 1     | Read: Enabled                                                      |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
| B                | RW   | ERROR     |                                                                                       |       | Write '1' to disable interrupt for event <a href="#">ERROR</a>     |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |      |           | Clear                                                                                 | 1     | Disable                                                            |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |      |           | Disabled                                                                              | 0     | Read: Disabled                                                     |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |      |           | Enabled                                                                               | 1     | Read: Enabled                                                      |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
| E                | RW   | RXSTARTED |                                                                                       |       | Write '1' to disable interrupt for event <a href="#">RXSTARTED</a> |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |      |           | Clear                                                                                 | 1     | Disable                                                            |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |      |           | Disabled                                                                              | 0     | Read: Disabled                                                     |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |      |           | Enabled                                                                               | 1     | Read: Enabled                                                      |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
| F                | RW   | TXSTARTED |                                                                                       |       | Write '1' to disable interrupt for event <a href="#">TXSTARTED</a> |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |      |           | Clear                                                                                 | 1     | Disable                                                            |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |      |           | Disabled                                                                              | 0     | Read: Disabled                                                     |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |      |           | Enabled                                                                               | 1     | Read: Enabled                                                      |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
| G                | RW   | WRITE     |                                                                                       |       | Write '1' to disable interrupt for event <a href="#">WRITE</a>     |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |      |           | Clear                                                                                 | 1     | Disable                                                            |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |      |           | Disabled                                                                              | 0     | Read: Disabled                                                     |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |      |           | Enabled                                                                               | 1     | Read: Enabled                                                      |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
| H                | RW   | READ      |                                                                                       |       | Write '1' to disable interrupt for event <a href="#">READ</a>      |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |      |           | Clear                                                                                 | 1     | Disable                                                            |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |      |           | Disabled                                                                              | 0     | Read: Disabled                                                     |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                  |      |           | Enabled                                                                               | 1     | Read: Enabled                                                      |  |  |  |  |  |     |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |

### 7.1.38.9.27 ERRORSRC

Address offset: 0x4D0

Error source

| Bit number       |             |             | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |
|------------------|-------------|-------------|---------------------------------------------------------------------------------------|---------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|---|---|
| ID               |             |             |                                                                                       |                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | C | B | A |
| Reset 0x00000000 |             |             | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |
| ID               | Acce Field  | Value ID    | Value                                                                                 | Description                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |
| A                | RW OVERFLOW |             |                                                                                       | RX buffer overflow detected, and prevented  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |
|                  |             | NotDetected | 0                                                                                     | Error did not occur                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |
|                  |             | Detected    | 1                                                                                     | Error occurred                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |
| B                | RW DNACK    |             |                                                                                       | NACK sent after receiving a data byte       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |
|                  |             | NotReceived | 0                                                                                     | Error did not occur                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |
|                  |             | Received    | 1                                                                                     | Error occurred                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |
| C                | RW OVERREAD |             |                                                                                       | TX buffer over-read detected, and prevented |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |
|                  |             | NotDetected | 0                                                                                     | Error did not occur                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |
|                  |             | Detected    | 1                                                                                     | Error occurred                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |

### 7.1.38.9.28 MATCH

Address offset: 0x4D4

Status register indicating which address had a match

|                  |            |       |          |                                                                                       |                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
|------------------|------------|-------|----------|---------------------------------------------------------------------------------------|------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|
| Bit number       |            |       |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| ID               |            |       |          |                                                                                       |                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A |
| Reset 0x00000000 |            |       |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0             |                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| ID               | Acce Field |       | Value ID | Value                                                                                 | Description                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| A                | R          | MATCH |          | [0..1]                                                                                | Which of the addresses in {ADDRESS} matched the incoming address |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |

### 7.1.38.9.29 ENABLE

Address offset: 0x500

Enable TWIS

|                  |            |          |                                                                                       |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          | A A A A                                                                               |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW ENABLE  |          |                                                                                       | Enable or disable TWIS |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Disable TWIS           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 9                                                                                     | Enable TWIS            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.38.9.30 PSEL.SCL

Address offset: 0x508

Pin select for SCL signal

|                  |            |              |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |             |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |              | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15          | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |              | C       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |             |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Reset 0xFFFFFFFF |            |              | 1       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |             |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field | Value ID     | Value   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | Description |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW PIN     |              | [0..31] |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | Pin number  |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| B                | RW PORT    |              | [0..1]  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | Port number |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| C                | RW CONNECT |              |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | Connection  |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disconnected | 1       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | Disconnect  |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Connected    | 0       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | Connect     |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.38.9.31 PSEL.SDA

Address offset: 0x50C

### Pin select for SDA signal

|                  |            |              |                                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |             |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------------|-----------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |              | 31                                                                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15          | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |              | C                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |             |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Reset 0xFFFFFFFF |            |              | 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |             |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field | Value ID     | Value                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | Description |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW PIN     |              | [0..31]                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | Pin number  |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| B                | RW PORT    |              | [0..1]                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | Port number |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| C                | RW CONNECT |              |                                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | Connection  |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disconnected | 1                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | Disconnect  |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Connected    | 0                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | Connect     |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.38.9.32 RXD.PTR

Address offset: 0x534

RXD Data pointer

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A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**Note:** See the memory chapter for details about which memories are available for EasyDMA.

#### 7.1.38.9.33 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in RXD buffer

[illegible]

### 7.1.38.9.34 RXD.AMOUNT

Address offset: 0x53C

Number of bytes transferred in the last RXD transaction

|                  |            |          |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Description                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | R          | AMOUNT   | [1..0xFFFF]                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Number of bytes transferred in the last RXD transaction |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.38.9.35 RXD.LIST

Address offset: 0x540

EasyDMA list type

|                  |            |           |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|-----------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |           |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |           |       | A A                                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |           |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID  | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | LIST      |       | List type                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled  | 0     | Disable EasyDMA list                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | ArrayList | 1     | Use array list                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.38.9.36 TXD.PTR

Address offset: 0x544

TXD Data pointer

|                  |            |          |                                                                                       |  |  |  |                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|--|--|--|------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A                           |  |  |  |                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |  |  |  |                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 |  |  |  | Description      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW PTR     |          |                                                                                       |  |  |  | TXD Data pointer |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**Note:** See the memory chapter for details about which memories are available for EasyDMA.

### 7.1.38.9.37 TXD.MAXCNT

Address offset: 0x548

Maximum number of bytes in TXD buffer

|                  |            |          |                                                                                       |                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|---------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A                           |                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW MAXCNT  |          | [1..0xFFFF]                                                                           | Maximum number of bytes in TXD buffer |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.38.9.38 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transferred in the last TXD transaction

|                  |            |          |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Description                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | R          | AMOUNT   | [1..0xFFFF]                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Number of bytes transferred in the last TXD transaction |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.38.9.39 TXD.LIST

Address offset: 0x550

EasyDMA list type

|                  |      |       |           |                                                                                       |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|-------|-----------|---------------------------------------------------------------------------------------|----------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |       |           | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |       |           | A A                                                                                   |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |       |           | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field | Value ID  | Value                                                                                 | Description          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW   | LIST  |           |                                                                                       | List type            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | Disabled  | 0                                                                                     | Disable EasyDMA list |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |       | ArrayList | 1                                                                                     | Use array list       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.38.9.40 ADDRESS[n] (n=0..1)

Address offset: 0x588 + (n × 0x4)

TWI slave address n

|                  |            |  |          |                                                                                       |  |  |  |                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|--|----------|---------------------------------------------------------------------------------------|--|--|--|-------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |  |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |  |          | A A A A A A A A                                                                       |  |  |  |                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |  |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0           |  |  |  |                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field |  | Value ID | Value                                                                                 |  |  |  | Description       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW ADDRESS |  |          |                                                                                       |  |  |  | TWI slave address |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.38.9.41 CONFIG

Address offset: 0x594

Configuration register for the address match mechanism

|                  |            |                     |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|---------------------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |                     |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |                     |       | B A                                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000001 |            |                     |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID            | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A-B              | RW         | ADDRESS[i] (i=0..1) |       | Enable or disable address matching on ADDRESS[i]                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled            | 0     | Disabled                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled             | 1     | Enabled                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.38.9.42 ORC

Address offset: 0x5C0

Over-read character. Character sent out in case of an over-read of the transmit buffer.

|                  |      |       |       |    |                                                                                         |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------|-------|-------|----|-----------------------------------------------------------------------------------------|----|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |      |       |       | 31 | 30                                                                                      | 29 | 28          | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |      |       |       |    |                                                                                         |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A | A | A | A | A | A | A |   |   |
| Reset 0x00000000 |      |       |       | 0  | 0                                                                                       | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce | Field | Value | ID | Value                                                                                   |    | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW   | ORC   |       |    | Over-read character. Character sent out in case of an over-read of the transmit buffer. |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

## 7.1.38.10 Electrical specification

### 7.1.38.10.1 TWIS slave timing specifications

| Symbol                     | Description                                                                 | Min. | Typ. | Max. | Units   |
|----------------------------|-----------------------------------------------------------------------------|------|------|------|---------|
| $f_{TWIS,SCL}$             | Bit rates for TWIS <sup>26</sup>                                            | ..   | ..   | ..   | kbps    |
| $t_{TWIS,START}$           | Time from PREPARERX/PREPARETX task to ready to receive/transmit             | ..   | ..   | ..   | $\mu$ s |
| $t_{TWIS,SU\_DAT}$         | Data setup time before positive edge on SCL – all modes                     | ..   | ..   | ..   | ns      |
| $t_{TWIS,HD\_DAT}$         | Data hold time after negative edge on SCL – all modes                       | ..   | ..   | ..   | ns      |
| $t_{TWIS,HD\_STA,100kbps}$ | TWI slave hold time from for START condition (SDA low to SCL low), 100 kbps | ..   | ..   | ..   | ns      |
| $t_{TWIS,HD\_STA,400kbps}$ | TWI slave hold time from for START condition (SDA low to SCL low), 400 kbps | ..   | ..   | ..   | ns      |
| $t_{TWIS,SU\_STO,100kbps}$ | TWI slave setup time from SCL high to STOP condition, 100 kbps              | ..   | ..   | ..   | ns      |
| $t_{TWIS,SU\_STO,400kbps}$ | TWI slave setup time from SCL high to STOP condition, 400 kbps              | ..   | ..   | ..   | ns      |
| $t_{TWIS,BUF,100kbps}$     | TWI slave bus free time between STOP and START conditions, 100 kbps         | ..   | ..   | ..   | ns      |
| $t_{TWIS,BUF,400kbps}$     | TWI slave bus free time between STOP and START conditions, 400 kbps         | ..   | ..   | ..   | ns      |

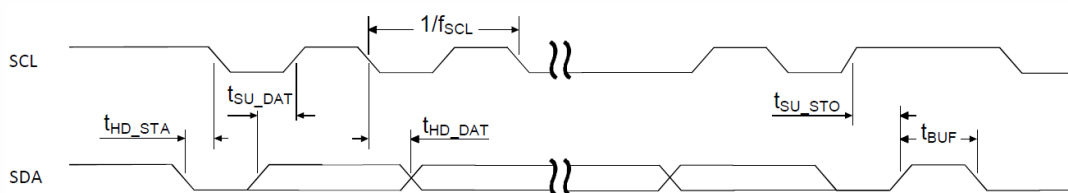


Figure 221: TWIS timing diagram, 1 byte transaction

## 7.1.39 UARTE — Universal asynchronous receiver/transmitter with EasyDMA

The Universal asynchronous receiver/transmitter with EasyDMA (UARTE) offers fast, full-duplex, asynchronous serial communication with built-in flow control (CTS, RTS) support in hardware at a rate up to 1 Mbps, and EasyDMA data transfer from/to RAM.

<sup>26</sup> High bit rates or stronger pull-ups may require GPIOs to be set as High Drive, see GPIO chapter for more details.



Listed here are the main features for UARTE:

- Full-duplex operation
- Automatic hardware flow control
- Optional even parity bit checking and generation
- EasyDMA
- Up to 1 Mbps baudrate
- Return to IDLE between transactions supported (when using HW flow control)
- One or two stop bit
- Least significant bit (LSB) first

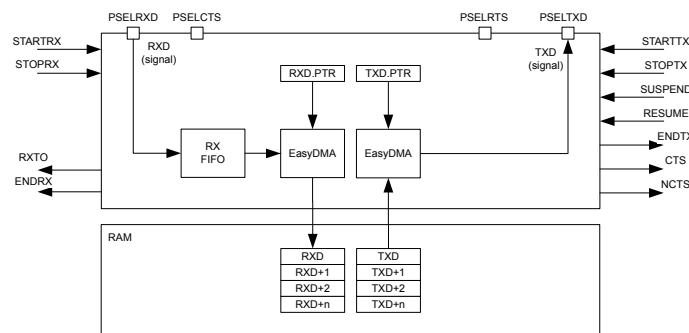


Figure 222: UARTE configuration

The GPIOs used for each UART interface can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pinout and efficient use of board space and signal routing.

**Note:** External crystal oscillator must be enabled to obtain sufficient clock accuracy for stable communication. See [CLOCK — Clock control](#) on page 61 for more information.

### 7.1.39.1 EasyDMA

The UARTE implements EasyDMA for reading and writing to and from the RAM.

If the TXD.PTR and the RXD.PTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See [Memory](#) on page 18 for more information about the different memory regions.

The .PTR and .MAXCNT registers are double-buffered. They can be updated and prepared for the next RX/TX transmission immediately after having received the RXSTARTED/TXSTARTED event.

The ENDRX/ENDTX event indicates that EasyDMA has finished accessing respectively the RX/TX buffer in RAM.

### 7.1.39.2 Transmission

The first step of a DMA transmission is storing bytes in the transmit buffer and configuring EasyDMA. This is achieved by writing the initial address pointer to TXD.PTR, and the number of bytes in the RAM buffer to TXD.MAXCNT. The UARTE transmission is started by triggering the STARTTX task.

After each byte has been sent over the TXD line, a TXDRDY event will be generated.

When all bytes in the TXD buffer, as specified in the TXD.MAXCNT register, have been transmitted, the UARTE transmission will end automatically and an ENDTX event will be generated.

A UARTE transmission sequence is stopped by triggering the STOPTX task, a TXSTOPPED event will be generated when the UARTE transmitter has stopped.

If the ENDTX event has not already been generated when the UARTE transmitter has come to a stop, the UARTE will generate the ENDTX event explicitly even though all bytes in the TXD buffer, as specified in the TXD.MAXCNT register, have not been transmitted.

If flow control is enabled through the HWFC field in the CONFIG register, a transmission will be automatically suspended when CTS is deactivated and resumed when CTS is activated again, as illustrated in [Figure 223: UARTE transmission](#) on page 654. A byte that is in transmission when CTS is deactivated will be fully transmitted before the transmission is suspended.

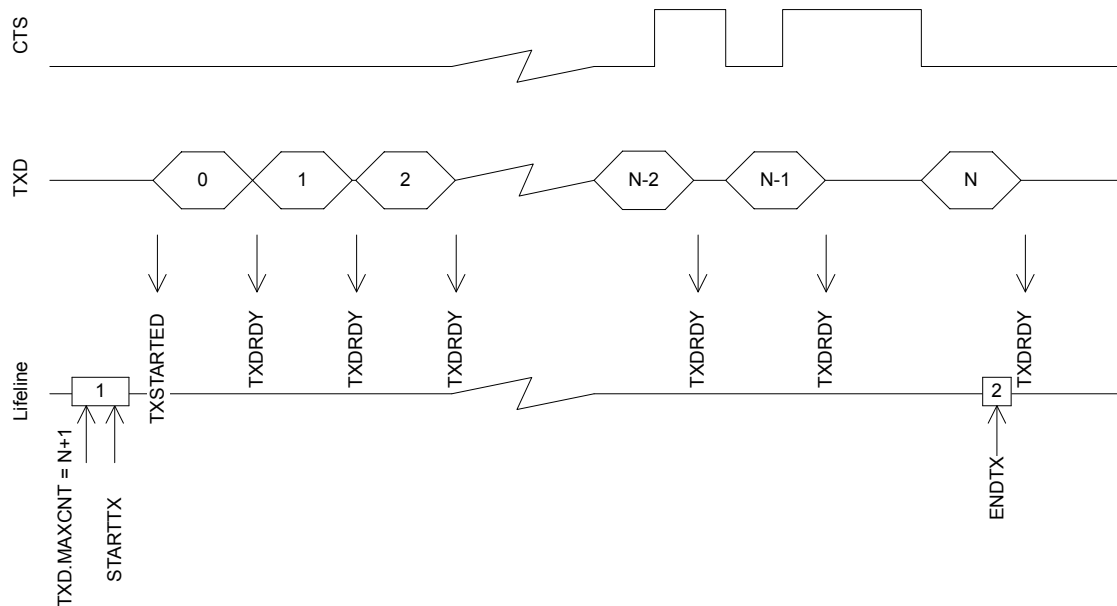


Figure 223: UARTE transmission

The UARTE transmitter will be in its lowest activity level, and consume the least amount of energy, when it is stopped, i.e. before it is started via STARTTX or after it has been stopped via STOPTX and the TXSTOPPED event has been generated. See [POWER — Power control](#) on page 36 for more information about power modes.

### 7.1.39.3 Reception

The UARTE receiver is started by triggering the STARTRX task. The UARTE receiver is using EasyDMA to store incoming data in an RX buffer in RAM.

The RX buffer is located at the address specified in the RXD.PTR register. The RXD.PTR register is double-buffered and it can be updated and prepared for the next STARTRX task immediately after the RXSTARTED event is generated. The size of the RX buffer is specified in the RXD.MAXCNT register and the UARTE will generate an ENDRX event when it has filled up the RX buffer, see [Figure 224: UARTE reception](#) on page 655.

For each byte received over the RXD line, an RXDRDY event will be generated. This event is likely to occur before the corresponding data has been transferred to Data RAM.

The RXD.AMOUNT register can be queried following an ENDRX event to see how many new bytes have been transferred to the RX buffer in RAM since the previous ENDRX event.

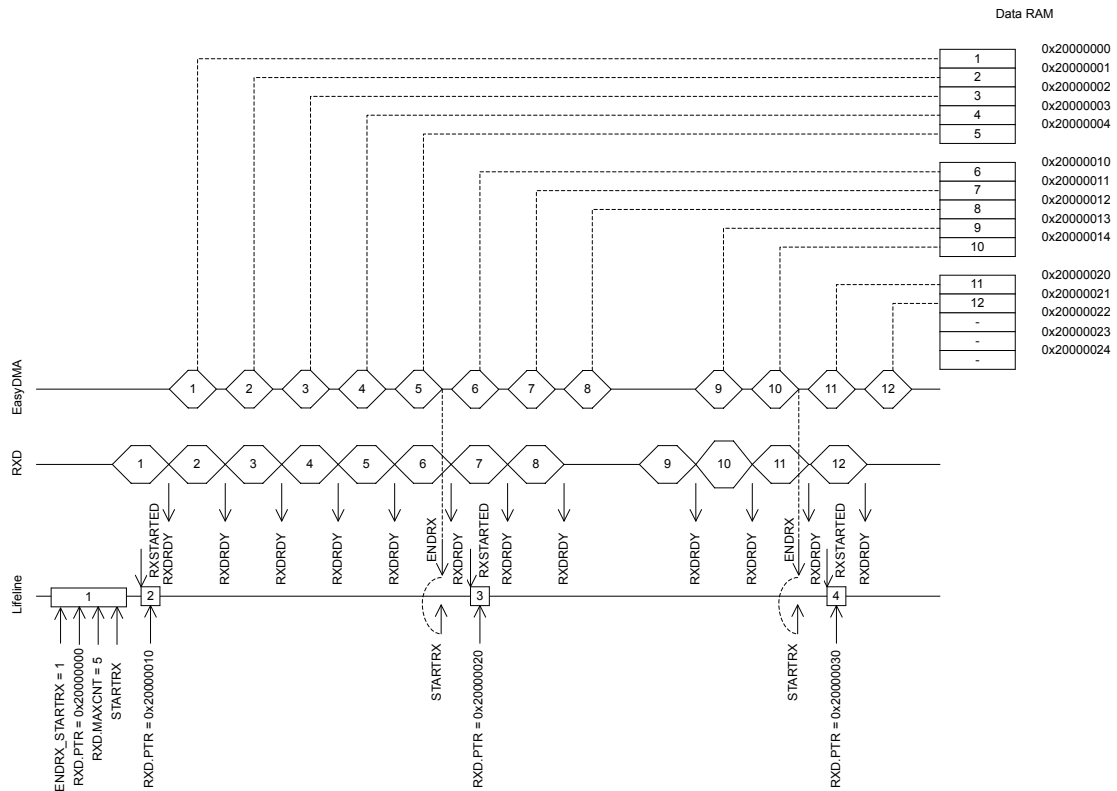


Figure 224: UARTE reception

The UARTE receiver is stopped by triggering the STOPRX task. An RXTO event is generated when the UARTE has stopped. The UARTE will make sure that an impending ENDRX event will be generated before the RXTO event is generated. This means that the UARTE will guarantee that no ENDRX event will be generated after RXTO, unless the UARTE is restarted or a FLUSHRX command is issued after the RXTO event is generated.

**Important:** If the ENDRX event has not already been generated when the UARTE receiver has come to a stop, which implies that all pending content in the RX FIFO has been moved to the RX buffer, the UARTE will generate the ENDRX event explicitly even though the RX buffer is not full. In this scenario the ENDRX event will be generated before the RXTO event is generated.

To be able to know how many bytes have actually been received into the RX buffer, the CPU can read the RXD.AMOUNT register following the ENDRX event or the RXTO event.

The UARTE is able to receive up to four bytes after the STOPRX task has been triggered as long as these are sent in succession immediately after the RTS signal is deactivated. This is possible because after the RTS is deactivated the UARTE is able to receive bytes for an extended period equal to the time it takes to send 4 bytes on the configured baud rate.

After the RXTO event is generated the internal RX FIFO may still contain data, and to move this data to RAM the FLUSHRX task must be triggered. To make sure that this data does not overwrite data in the RX buffer, the RX buffer should be emptied or the RXD.PTR should be updated before the FLUSHRX task is triggered. To make sure that all data in the RX FIFO is moved to the RX buffer, the RXD.MAXCNT register must be set to  $RXD.MAXCNT > 4$ , see [Figure 225: UARTE reception with forced stop via STOPRX](#) on page 656. The UARTE will generate the ENDRX event after completing the FLUSHRX task even if the RX FIFO was empty or if the RX buffer does not get filled up. To be able to know how many bytes have actually been received into the RX buffer in this case, the CPU can read the RXD.AMOUNT register following the ENDRX event.

If HW flow control is enabled through the HWFC field in the CONFIG register, the RTS signal will be deactivated when the receiver is stopped via the STOPRX task or when the UARTE is only able to receive four more bytes in its internal RX FIFO.

The UARTE receiver will be in its lowest activity level, and consume the least amount of energy, when it is stopped, i.e. before it is started via STARTRX or after it has been stopped via STOPRX and the RXTO event has been generated. See [POWER — Power control](#) on page 36 for more information about power modes.

An ERROR event, in the form of a framing error, will be generated if a valid stop bit is not detected in a frame. Another ERROR event, in the form of a break condition, will be generated if the RXD line is held active low for longer than the length of a data frame. Effectively, a framing error is always generated before a break condition occurs.

### 7.1.39.5 Using the UARTE without flow control

### 7.1.39.6 Parity and stop bit configuration

The amount of stop bits can also be configured through the register [CONFIG](#) on page 675.

When putting the system in low power and the peripheral is not needed, lowest possible power consumption is achieved by stopping, and then disabling the peripheral.

The STOPTX and STOPRX tasks may not be always needed (the peripheral might already be stopped), but if STOPTX and/or STOPRX is sent, software shall wait until the TXSTOPPED and/or RXTO event is received in response, before disabling the peripheral through the ENABLE register.

### 7.1.39.8 Pin configuration

The different signals RXD, CTS (Clear To Send, active low), RTS (Request To Send, active low), and TXD associated with the UARTE are mapped to physical pins according to the configuration specified in the PSEL.RXD, PSEL.CTS, PSEL.RTS, and PSEL.TXD registers respectively.

The PSEL.RXD, PSEL.CTS, PSEL.RTS, and PSEL.TXD registers and their configurations are only used as long as the UARTE is enabled, and retained only for the duration the device is in ON mode. PSEL.RXD, PSEL.RTS, PSEL.RTS and PSEL.TXD must only be configured when the UARTE is disabled.

To secure correct signal levels on the pins by the UARTE when the system is in OFF mode, the pins must be configured in the GPIO peripheral as described in [Table 173: GPIO configuration before enabling peripheral](#) on page 657.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

| UARTE signal | UARTE pin                | Direction | Output value   |
|--------------|--------------------------|-----------|----------------|
| RXD          | As specified in PSEL.RXD | Input     | Not applicable |
| CTS          | As specified in PSEL.CTS | Input     | Not applicable |
| RTS          | As specified in PSEL.RTS | Output    | 1              |
| TXD          | As specified in PSEL.TXD | Output    | 1              |

Table 173: GPIO configuration before enabling peripheral

### 7.1.39.9 Registers

| Base address             | Domain      | Peripheral | Instance                  | Secure mapping | DMA security | Description                                                | Configuration |
|--------------------------|-------------|------------|---------------------------|----------------|--------------|------------------------------------------------------------|---------------|
| 0x50008000<br>0x40008000 | APPLICATION | UARTE      | UARTE0 : S<br>UARTE0 : NS | US             | SA           | Universal asynchronous receiver/transmitter with EasyDMA 0 |               |
| 0x50009000<br>0x40009000 |             |            | UARTE1 : S<br>UARTE1 : NS |                |              |                                                            |               |
| 0x41013000               | NETWORK     | UARTE      | UARTE0                    | NS             | NA           | Universal asynchronous receiver/transmitter                |               |

Table 174: Instances

| Register          | Offset | Security | Description                                                            |
|-------------------|--------|----------|------------------------------------------------------------------------|
| TASKS_STARTRX     | 0x000  |          | Start UART receiver                                                    |
| TASKS_STOPRX      | 0x004  |          | Stop UART receiver                                                     |
| TASKS_STARTTX     | 0x008  |          | Start UART transmitter                                                 |
| TASKS_STOPTX      | 0x00C  |          | Stop UART transmitter                                                  |
| TASKS_FLUSHRX     | 0x02C  |          | Flush RX FIFO into RX buffer                                           |
| SUBSCRIBE_STARTRX | 0x080  |          | Subscribe configuration for task <a href="#">STARTRX</a>               |
| SUBSCRIBE_STOPRX  | 0x084  |          | Subscribe configuration for task <a href="#">STOPRX</a>                |
| SUBSCRIBE_STARTTX | 0x088  |          | Subscribe configuration for task <a href="#">STARTTX</a>               |
| SUBSCRIBE_STOPTX  | 0x08C  |          | Subscribe configuration for task <a href="#">STOPTX</a>                |
| SUBSCRIBE_FLUSHRX | 0x0AC  |          | Subscribe configuration for task <a href="#">FLUSHRX</a>               |
| EVENTS_CTS        | 0x100  |          | CTS is activated (set low). Clear To Send.                             |
| EVENTS_NCTS       | 0x104  |          | CTS is deactivated (set high). Not Clear To Send.                      |
| EVENTS_RXDRDY     | 0x108  |          | Data received in RXD (but potentially not yet transferred to Data RAM) |
| EVENTS_ENDRX      | 0x110  |          | Receive buffer is filled up                                            |
| EVENTS_TXDRDY     | 0x11C  |          | Data sent from TXD                                                     |

| Register          | Offset | Security | Description                                               |
|-------------------|--------|----------|-----------------------------------------------------------|
| EVENTS_ENDTX      | 0x120  |          | Last TX byte transmitted                                  |
| EVENTS_ERROR      | 0x124  |          | Error detected                                            |
| EVENTS_RXTO       | 0x144  |          | Receiver timeout                                          |
| EVENTS_RXSTARTED  | 0x14C  |          | UART receiver has started                                 |
| EVENTS_TXSTARTED  | 0x150  |          | UART transmitter has started                              |
| EVENTS_TXSTOPPED  | 0x158  |          | Transmitter stopped                                       |
| PUBLISH_CTS       | 0x180  |          | Publish configuration for event CTS                       |
| PUBLISH_NCTS      | 0x184  |          | Publish configuration for event NCTS                      |
| PUBLISH_RXDRDY    | 0x188  |          | Publish configuration for event RXDRDY                    |
| PUBLISH_ENDRX     | 0x190  |          | Publish configuration for event ENDRX                     |
| PUBLISH_TXDRDY    | 0x19C  |          | Publish configuration for event TXDRDY                    |
| PUBLISH_ENDTX     | 0x1A0  |          | Publish configuration for event ENDTX                     |
| PUBLISH_ERROR     | 0x1A4  |          | Publish configuration for event ERROR                     |
| PUBLISH_RXTO      | 0x1C4  |          | Publish configuration for event RXTO                      |
| PUBLISH_RXSTARTED | 0x1CC  |          | Publish configuration for event RXSTARTED                 |
| PUBLISH_TXSTARTED | 0x1D0  |          | Publish configuration for event TXSTARTED                 |
| PUBLISH_TXSTOPPED | 0x1D8  |          | Publish configuration for event TXSTOPPED                 |
| SHORTS            | 0x200  |          | Shortcuts between local events and tasks                  |
| INTEN             | 0x300  |          | Enable or disable interrupt                               |
| INTENSET          | 0x304  |          | Enable interrupt                                          |
| INTENCLR          | 0x308  |          | Disable interrupt                                         |
| ERRORSRC          | 0x480  |          | Error source                                              |
|                   |        |          | Note : this register is read / write one to clear.        |
| ENABLE            | 0x500  |          | Enable UART                                               |
| PSEL.RTS          | 0x508  |          | Pin select for RTS signal                                 |
| PSEL.TXD          | 0x50C  |          | Pin select for TXD signal                                 |
| PSEL.CTS          | 0x510  |          | Pin select for CTS signal                                 |
| PSEL.RXD          | 0x514  |          | Pin select for RXD signal                                 |
| BAUDRATE          | 0x524  |          | Baud rate. Accuracy depends on the HFCLK source selected. |
| RXD.PTR           | 0x534  |          | Data pointer                                              |
| RXD.MAXCNT        | 0x538  |          | Maximum number of bytes in receive buffer                 |
| RXD.AMOUNT        | 0x53C  |          | Number of bytes transferred in the last transaction       |
| TXD.PTR           | 0x544  |          | Data pointer                                              |
| TXD.MAXCNT        | 0x548  |          | Maximum number of bytes in transmit buffer                |
| TXD.AMOUNT        | 0x54C  |          | Number of bytes transferred in the last transaction       |
| CONFIG            | 0x56C  |          | Configuration of parity and hardware flow control         |

Table 175: Register overview

### 7.1.39.9.1 TASKS\_STARTRX

Address offset: 0x000

Start UART receiver

|                  |            |  |  |               |  |  |       |  |  |                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|--|---------------|--|--|-------|--|--|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |  |               |  |  |       |  |  | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |  |  |               |  |  |       |  |  | A                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |  |               |  |  |       |  |  | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  |  | Value ID      |  |  | Value |  |  | Description         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          |  |  | TASKS_STARTRX |  |  |       |  |  | Start UART receiver |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  |  | Trigger       |  |  | 1     |  |  | Trigger task        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.39.9.2 TASKS\_STOPRX

Address offset: 0x004

Stop UART receiver

|                  |                |          |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|----------------|----------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |                |          |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |                |          |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |                |          |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field     | Value ID | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W TASKS_STOPRX |          |       | Stop UART receiver                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                | Trigger  | 1     | Trigger task                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.39.9.3 TASKS\_STARTTX

Address offset: 0x008

Start UART transmitter

|                  |                 |          |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|-----------------|----------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |                 |          |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |                 |          |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |                 |          |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field      | Value ID | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W TASKS_STARTTX |          |       | Start UART transmitter                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                 | Trigger  | 1     | Trigger task                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.39.9.4 TASKS\_STOPTX

Address offset: 0x00C

Stop UART transmitter

|                  |                |          |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|----------------|----------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |                |          |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |                |          |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |                |          |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field     | Value ID | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W TASKS_STOPTX |          |       | Stop UART transmitter                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                | Trigger  | 1     | Trigger task                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.39.9.5 TASKS\_FLUSHRX

Address offset: 0x02C

Flush RX FIFO into RX buffer

|                  |            |               |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|---------------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |               |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |               |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |               |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID      | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W          | TASKS_FLUSHRX |       | Flush RX FIFO into RX buffer                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Trigger       | 1     | Trigger task                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.39.9.6 SUBSCRIBE\_STARTRX

Address offset: 0x080

Subscribe configuration for task **STARTRX**

|                  |            |          |          |                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|-------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                                                          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |          |          | B                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |          | 0                                                           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |
| ID               | Acce Field | Value ID | Value    | Description                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] | Channel that task <a href="#">STARTRX</a> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        | Disable subscription                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        | Enable subscription                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

## 7.1.39.9.7 SUBSCRIBE\_STOPRX

Address offset: 0x084

Subscribe configuration for task **STOPRX**

|                  |      |       |          |                                                                         |                      |                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------|-------|----------|-------------------------------------------------------------------------|----------------------|---------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |      |       |          | 31                                                                      | 30                   | 29                                                      | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |      |       |          | B                                                                       |                      |                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A |
| Reset 0x00000000 |      |       |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |                      |                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce | Field | Value    | ID                                                                      | Value                | Description                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW   | CHIDX |          |                                                                         | [255..0]             | Channel that task <span>STOPRX</span> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW   | EN    |          |                                                                         |                      |                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |       | Disabled | 0                                                                       | Disable subscription |                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |       | Enabled  | 1                                                                       | Enable subscription  |                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

## 7.1.39.9.8 SUBSCRIBE\_STARTTX

Address offset: 0x088

Subscribe configuration for task **STARTTX**

|                  |            |          |          |                      |    |                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|----------------------|----|----------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                   | 30 | 29                                                       | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |          |          | B                    |    |                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |          | 0                    | 0  | 0                                                        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce Field |          | Value ID | Value                |    | Description                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          |          | [255..0]             |    | Channel that task <span>STARTTX</span> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |                      |    |                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        | Disable subscription |    |                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        | Enable subscription  |    |                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

## 7.1.39.9.9 SUBSCRIBE\_STOPTX

Address offset: 0x08C

Subscribe configuration for task **STOPTX**



|                  |            |          |                                                                         |    |    |    |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
|------------------|------------|----------|-------------------------------------------------------------------------|----|----|----|---------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|-----------------|---|---|---|---|---|---|---|--|--|--|--|
| Bit number       |            |          | 31                                                                      | 30 | 29 | 28 | 27                                                | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |
| ID               |            |          | B                                                                       |    |    |    |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A A A A A A A A |   |   |   |   |   |   |   |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |    |    |    |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                   |    |    |    | Description                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                |    |    |    | Channel that task <b>STOPTX</b> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
| B                | RW EN      |          |                                                                         |    |    |    |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | Disabled | 0                                                                       |    |    |    | Disable subscription                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | Enabled  | 1                                                                       |    |    |    | Enable subscription                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |

### 7.1.39.9.10 SUBSCRIBE\_FLUSHRX

Address offset: 0x0AC

Subscribe configuration for task **FLUSHRX**

|                  |            |  |          |  |          |  |                                                    |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|--|----------|--|----------------------------------------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          |  |          |  |                                                    |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |  |          |  |          |  |                                                    |  |  | B  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  | A  | A | A | A | A | A | A |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |          |  |          |  |                                                    |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID |  | Value    |  | Description                                        |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          |  | [255..0] |  | Channel that task <b>FLUSHRX</b> will subscribe to |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |  |          |  |                                                    |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled |  | 0        |  | Disable subscription                               |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  |  | 1        |  | Enable subscription                                |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.39.9.11 EVENTS\_CTS

Address offset: 0x100

CTS is activated (set low). Clear To Send.

|                  |            |              |       |                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------------|-------|--------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |              |       | 31                                         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |              |       |                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |
| Reset 0x00000000 |            |              |       | 0                                          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |
| ID               | Acce Field | Value ID     | Value | Description                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | EVENTS_CTS   |       | CTS is activated (set low). Clear To Send. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | NotGenerated | 0     | Event not generated                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Generated    | 1     | Event generated                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.39.9.12 EVENTS\_NCTS

Address offset: 0x104

CTS is deactivated (set high). Not Clear To Send.

|                  |                |              |       |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|------------------|----------------|--------------|-------|---------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|--|
| Bit number       |                |              | 31    | 30                                                | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |
| ID               |                |              | A     |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| Reset 0x00000000 |                |              | 0     | 0                                                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |  |
| ID               | Acce Field     | Value ID     | Value | Description                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| A                | RW EVENTS_NCTS |              |       | CTS is deactivated (set high). Not Clear To Send. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |                | NotGenerated | 0     | Event not generated                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |                | Generated    | 1     | Event generated                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |

### 7.1.39.9.13 EVENTS\_RXDRDY

Address offset: 0x108

Data received in RXD (but potentially not yet transferred to Data RAM)

|                  |            |  |               |  |       |  |                                                                        |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|---------------|--|-------|--|------------------------------------------------------------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |               |  |       |  |                                                                        |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |  |               |  |       |  |                                                                        |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |
| Reset 0x00000000 |            |  |               |  |       |  |                                                                        |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID      |  | Value |  | Description                                                            |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         |  | EVENTS_RXDRDY |  |       |  | Data received in RXD (but potentially not yet transferred to Data RAM) |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | NotGenerated  |  | 0     |  | Event not generated                                                    |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Generated     |  | 1     |  | Event generated                                                        |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.39.9.14 EVENTS\_ENDRX

Address offset: 0x110

Receive buffer is filled up

|                  |            |              |       |                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|------------------|------------|--------------|-------|-----------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|---|
| Bit number       |            |              |       | 31                          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |   |
| ID               |            |              |       |                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  | A |
| Reset 0x00000000 |            |              |       | 0                           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |   |
| ID               | Acce Field | Value ID     | Value | Description                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
| A                | RW         | EVENTS_ENDRX |       | Receive buffer is filled up |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|                  |            | NotGenerated | 0     | Event not generated         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |
|                  |            | Generated    | 1     | Event generated             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |

#### 7.1.39.9.15 EVENTS\_TXDRDY

Address offset: 0x11C

Data sent from TXD

|                  |            |               |       |                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|------------------|------------|---------------|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|--|
| Bit number       |            |               | 31    | 30                  | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |
| ID               |            |               | A     |                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| Reset 0x00000000 |            |               | 0     | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |  |
| ID               | Acce Field | Value ID      | Value | Description         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| A                | RW         | EVENTS_TXDRDY |       | Data sent from TXD  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | NotGenerated  | 0     | Event not generated |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | Generated     | 1     | Event generated     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |

#### 7.1.39.9.16 EVENTS\_ENDTX

Address offset: 0x120

Last TX byte transmitted

|                  |            |              |       |                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------------|-------|--------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |              |       | 31                       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |              |       | A                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |              |       | 0                        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID     | Value | Description              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | EVENTS_ENDTX |       | Last TX byte transmitted |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | NotGenerated | 0     | Event not generated      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Generated    | 1     | Event generated          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.39.9.17 EVENTS\_ERROR

Address offset: 0x124

Error detected

|                  |                 |              |                                                                                       |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|-----------------|--------------|---------------------------------------------------------------------------------------|---------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |                 |              | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |                 |              | A                                                                                     |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |                 |              | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                   |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field      | Value ID     | Value                                                                                 | Description         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW EVENTS_ERROR |              |                                                                                       | Error detected      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                 | NotGenerated | 0                                                                                     | Event not generated |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                 | Generated    | 1                                                                                     | Event generated     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.39.9.18 EVENTS\_RXTO

Address offset: 0x144

Receiver timeout

|                  |                |              |                                                                                       |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|----------------|--------------|---------------------------------------------------------------------------------------|---------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |                |              | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |                |              | A                                                                                     |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |                |              | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field     | Value ID     | Value                                                                                 | Description         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW EVENTS_RXTO |              |                                                                                       | Receiver timeout    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                | NotGenerated | 0                                                                                     | Event not generated |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                | Generated    | 1                                                                                     | Event generated     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.39.9.19 EVENTS\_RXSTARTED

Address offset: 0x14C

UART receiver has started

|                  |                     |              |                                                                                       |                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|---------------------|--------------|---------------------------------------------------------------------------------------|---------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |                     |              | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |                     |              | A                                                                                     |                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |                     |              | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field          | Value ID     | Value                                                                                 | Description               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW EVENTS_RXSTARTED |              |                                                                                       | UART receiver has started |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                     | NotGenerated | 0                                                                                     | Event not generated       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |                     | Generated    | 1                                                                                     | Event generated           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.39.9.20 EVENTS\_TXSTARTED

Address offset: 0x150

UART transmitter has started

|                  |            |                  |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|------------------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |                  |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |                  |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |                  |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID         | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | EVENTS_TXSTARTED |       | UART transmitter has started                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | NotGenerated     | 0     | Event not generated                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Generated        | 1     | Event generated                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.39.9.21 EVENTS\_TXSTOPPED

Address offset: 0x158

Transmitter stopped

|                  |            |                  |       |    |                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|------------------|-------|----|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                  | 31    | 30 | 29                  | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |                  | A     |    |                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |                  | 0     | 0  | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID         | Value |    | Description         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | EVENTS_TXSTOPPED |       |    | Transmitter stopped |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | NotGenerated     | 0     |    | Event not generated |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Generated        | 1     |    | Event generated     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.39.9.22 PUBLISH\_CTS

Address offset: 0x180

Publish configuration for event CTS

|                  |            |  |  |          |  |  |          |  |  |                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|--|----------|--|--|----------|--|--|-----------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |  |          |  |  |          |  |  | 31                                      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |  |  |          |  |  |          |  |  | B                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  |    |    |    |   |   |   |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |  |          |  |  |          |  |  | 0                                       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  |  | Value ID |  |  | Value    |  |  | Description                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |  |          |  |  | [255..0] |  |  | Channel that event CTS will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |  |          |  |  |          |  |  |                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  |  | Disabled |  |  | 0        |  |  | Disable publishing                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  |  | Enabled  |  |  | 1        |  |  | Enable publishing                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.39.9.23 PUBLISH\_NCTS

Address offset: 0x184

Publish configuration for event NCTS

|                  |            |  |          |                                                                         |    |                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
|------------------|------------|--|----------|-------------------------------------------------------------------------|----|-------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|-----------------|---|---|---|---|---|---|---|--|--|--|--|
| Bit number       |            |  |          | 31                                                                      | 30 | 29                                              | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |
| ID               |            |  |          | B                                                                       |    |                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A A A A A A A A |   |   |   |   |   |   |   |  |  |  |  |
| Reset 0x00000000 |            |  |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |    |                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
| ID               | Acce Field |  | Value ID | Value                                                                   |    | Description                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
| A                | RW CHIDX   |  |          | [255..0]                                                                |    | Channel that event <b>NCTS</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
| B                | RW EN      |  |          |                                                                         |    |                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
|                  |            |  | Disabled | 0                                                                       |    | Disable publishing                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
|                  |            |  | Enabled  | 1                                                                       |    | Enable publishing                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |

### 7.1.39.9.24 PUBLISH\_RXDRDY

Address offset: 0x188

Publish configuration for event RXDRDY

|                  |            |          |          |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|---------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                                                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |          |          | B                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   |   |   |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |          |          | 0                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID | Value    | Description                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] | Channel that event <b>RXDRDY</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        | Disable publishing                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        | Enable publishing                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.39.9.25 PUBLISH\_ENDRX

Address offset: 0x190

Publish configuration for event **ENDRX**

|                  |            |  |          |          |                    |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|----------|--------------------|--------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31       | 30                 | 29                                               | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |  |          | B        |                    |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   |   |   |   |   |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |          | 0        |                    |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID | Value    |                    | Description                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          | [255..0] |                    | Channel that event <b>ENDRX</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |          |                    |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled | 0        | Disable publishing |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  | 1        | Enable publishing  |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.39.9.26 PUBLISH\_TXDRDY

Address offset: 0x19C

Publish configuration for event **TXDRDY**

|                  |            |  |          |          |    |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|----------|----|---------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31       | 30 | 29                                                | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |  |          | B        |    |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |          | 0        | 0  | 0                                                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce Field |  | Value ID | Value    |    | Description                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          | [255..0] |    | Channel that event <b>TXDRDY</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |          |    |                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled | 0        |    | Disable publishing                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  | 1        |    | Enable publishing                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.39.9.27 PUBLISH\_ENDTX

Address offset: 0x1A0

Publish configuration for event **ENDTX**

|                  |            |  |  |          |    |          |    |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|--|----------|----|----------|----|--------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |  | 31       | 30 | 29       | 28 | 27                                               | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |  |  | B        |    |          |    |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   |   |   |   |   |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |  | 0        |    |          |    |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  |  | Value ID |    | Value    |    | Description                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |  |          |    | [255..0] |    | Channel that event <b>ENDTX</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |  |          |    |          |    |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  |  | Disabled |    | 0        |    | Disable publishing                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  |  | Enabled  |    | 1        |    | Enable publishing                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |



|                  |            |          |          |    |    |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|----|----|----|------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          | 31       | 30 | 29 | 28 | 27                                                   | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |          | B        |    |    |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   |   |   |   |   |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |          | 0        |    |    |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID | Value    |    |    |    | Description                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] |    |    |    | Channel that event <b>TXSTARTED</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |    |    |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        |    |    |    | Disable publishing                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        |    |    |    | Enable publishing                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.39.9.32 PUBLISH\_TXSTOPPED

Address offset: 0x1D8

Publish configuration for event **TXSTOPPED**

|                  |            |  |          |          |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|----------|----|------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31       | 30 | 29                                                   | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |  |          | B        |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   |   |   |   |   |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |          | 0        |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID | Value    |    | Description                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          | [255..0] |    | Channel that event <b>TXSTOPPED</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |          |    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled | 0        |    | Disable publishing                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  | 1        |    | Enable publishing                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.39.9.33 SHORTS

Address offset: 0x200

Shortcuts between local events and tasks

|                  |                  |          |       |                  |                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------------|----------|-------|------------------|-----------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |                  |          | 31    | 30               | 29                                            | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |                  |          | D C   |                  |                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |                  |          | 0     | 0                | 0                                             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field       | Value ID | Value |                  | Description                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| C                | RW ENDRX_STARTRX |          |       |                  | Shortcut between event ENDRX and task STARTRX |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |                  | Disabled | 0     | Disable shortcut |                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |                  | Enabled  | 1     | Enable shortcut  |                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| D                | RW ENDRX_STOPRX  |          |       |                  | Shortcut between event ENDRX and task STOPRX  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |                  | Disabled | 0     | Disable shortcut |                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |                  | Enabled  | 1     | Enable shortcut  |                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.39.9.34 INTEN

Address offset: 0x300

Enable or disable interrupt

|                  |            |          |                                                                         |    |                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
|------------------|------------|----------|-------------------------------------------------------------------------|----|--------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|--|
| Bit number       |            |          | 31                                                                      | 30 | 29                                         | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |  |
| ID               |            |          |                                                                         |    |                                            |    |    |    |    |    |    |    | L  | J  | I  | H  |    |    |    |    |    |    |    |    |   |   | G | F | E |   |   |   |   | D | C | B | A |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |    |                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| ID               | Acce Field | Value ID | Value                                                                   |    | Description                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| A                | RW CTS     |          |                                                                         |    | Enable or disable interrupt for event CTS  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | Disabled | 0                                                                       |    | Disable                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | Enabled  | 1                                                                       |    | Enable                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| B                | RW NCTS    |          |                                                                         |    | Enable or disable interrupt for event NCTS |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |  |

| Bit number       |      |           |                                                                 | 31    | 30          | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
|------------------|------|-----------|-----------------------------------------------------------------|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| ID               |      |           |                                                                 | L     |             |    |    |    |    |    |    |    |    |    |    |    |    | J  | I  | H  |    |    |    | G  |    |   |   | F | E | D |   |   |   | C | B | A |
| Reset 0x00000000 |      |           |                                                                 | 0     | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce | Field     | Value ID                                                        | Value | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| C                | RW   | RXDRDY    | Disabled                                                        | 0     | Disable     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | Enabled                                                         | 1     | Enable      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | Enable or disable interrupt for event <a href="#">RXDRDY</a>    |       |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| D                | RW   | ENDRX     | Disabled                                                        | 0     | Disable     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | Enabled                                                         | 1     | Enable      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | Enable or disable interrupt for event <a href="#">ENDRX</a>     |       |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| E                | RW   | TXDRDY    | Disabled                                                        | 0     | Disable     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | Enabled                                                         | 1     | Enable      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | Enable or disable interrupt for event <a href="#">TXDRDY</a>    |       |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| F                | RW   | ENDTX     | Disabled                                                        | 0     | Disable     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | Enabled                                                         | 1     | Enable      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | Enable or disable interrupt for event <a href="#">ENDTX</a>     |       |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| G                | RW   | ERROR     | Disabled                                                        | 0     | Disable     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | Enabled                                                         | 1     | Enable      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | Enable or disable interrupt for event <a href="#">ERROR</a>     |       |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| H                | RW   | RXTO      | Disabled                                                        | 0     | Disable     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | Enabled                                                         | 1     | Enable      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | Enable or disable interrupt for event <a href="#">RXTO</a>      |       |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| I                | RW   | RXSTARTED | Disabled                                                        | 0     | Disable     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | Enabled                                                         | 1     | Enable      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | Enable or disable interrupt for event <a href="#">RXSTARTED</a> |       |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| J                | RW   | TXSTARTED | Disabled                                                        | 0     | Disable     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | Enabled                                                         | 1     | Enable      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | Enable or disable interrupt for event <a href="#">TXSTARTED</a> |       |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| L                | RW   | TXSTOPPED | Disabled                                                        | 0     | Disable     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | Enabled                                                         | 1     | Enable      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |           | Enable or disable interrupt for event <a href="#">TXSTOPPED</a> |       |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.39.9.35 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|----------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |            |          | L J I H                                                                               |                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  | G F E D C B A |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW CTS     |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">CTS</a>    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Set      | 1                                                                                     | Enable                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Read: Disabled                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Read: Enabled                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW NCTS    |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">NCTS</a>   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Set      | 1                                                                                     | Enable                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Read: Disabled                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Read: Enabled                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW RXDRDY  |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">RXDRDY</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Set      | 1                                                                                     | Enable                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |



| Bit number       |      |                |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                |  |  |                                                                   |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|----------------|----------|---------------------------------------------------------------------------------------|----------------------------------------------------------------|--|--|-------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|---------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |      |                |          | L J I H                                                                               |                                                                |  |  |                                                                   |  |  |  |  |  |  |  |  |  |  |  | G F E D C B A |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |                |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                |  |  |                                                                   |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field          | Value ID | Value                                                                                 | Description                                                    |  |  |                                                                   |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| D                | RW   | ENDRX          | Disabled | 0                                                                                     | Read: Disabled                                                 |  |  |                                                                   |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                | Enabled  | 1                                                                                     | Read: Enabled                                                  |  |  |                                                                   |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">ENDRX</a>  |  |  |                                                                   |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                | Set      | 1                                                                                     | Enable                                                         |  |  |                                                                   |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                | Disabled | 0                                                                                     | Read: Disabled                                                 |  |  |                                                                   |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| E                | RW   | TXDRDY         | Enabled  | 1                                                                                     | Read: Enabled                                                  |  |  |                                                                   |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">TXDRDY</a> |  |  |                                                                   |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                | Set      | 1                                                                                     | Enable                                                         |  |  |                                                                   |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                | Disabled | 0                                                                                     | Read: Disabled                                                 |  |  |                                                                   |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                | Enabled  | 1                                                                                     | Read: Enabled                                                  |  |  |                                                                   |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| F                | RW   | ENDTX          |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">ENDTX</a>  |  |  |                                                                   |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                | Set      | 1                                                                                     | Enable                                                         |  |  |                                                                   |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                | Disabled | 0                                                                                     | Read: Disabled                                                 |  |  |                                                                   |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                | Enabled  | 1                                                                                     | Read: Enabled                                                  |  |  |                                                                   |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                | G        | RW                                                                                    | ERROR                                                          |  |  | Write '1' to enable interrupt for event <a href="#">ERROR</a>     |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Set              | 1    | Enable         |          |                                                                                       |                                                                |  |  |                                                                   |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Disabled         | 0    | Read: Disabled |          |                                                                                       |                                                                |  |  |                                                                   |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Enabled          | 1    | Read: Enabled  |          |                                                                                       |                                                                |  |  |                                                                   |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| H                | RW   | RXTO           |          |                                                                                       |                                                                |  |  | Write '1' to enable interrupt for event <a href="#">RXTO</a>      |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                | Set      | 1                                                                                     | Enable                                                         |  |  |                                                                   |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                | Disabled | 0                                                                                     | Read: Disabled                                                 |  |  |                                                                   |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                | Enabled  | 1                                                                                     | Read: Enabled                                                  |  |  |                                                                   |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                | I        | RW                                                                                    | RXSTARTED                                                      |  |  | Write '1' to enable interrupt for event <a href="#">RXSTARTED</a> |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Set              | 1    | Enable         |          |                                                                                       |                                                                |  |  |                                                                   |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Disabled         | 0    | Read: Disabled |          |                                                                                       |                                                                |  |  |                                                                   |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Enabled          | 1    | Read: Enabled  |          |                                                                                       |                                                                |  |  |                                                                   |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| J                | RW   | TXSTARTED      |          |                                                                                       |                                                                |  |  | Write '1' to enable interrupt for event <a href="#">TXSTARTED</a> |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                | Set      | 1                                                                                     | Enable                                                         |  |  |                                                                   |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                | Disabled | 0                                                                                     | Read: Disabled                                                 |  |  |                                                                   |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                | Enabled  | 1                                                                                     | Read: Enabled                                                  |  |  |                                                                   |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                | L        | RW                                                                                    | TXSTOPPED                                                      |  |  | Write '1' to enable interrupt for event <a href="#">TXSTOPPED</a> |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Set              | 1    | Enable         |          |                                                                                       |                                                                |  |  |                                                                   |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Disabled         | 0    | Read: Disabled |          |                                                                                       |                                                                |  |  |                                                                   |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Enabled          | 1    | Read: Enabled  |          |                                                                                       |                                                                |  |  |                                                                   |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.39.9.36 INTENCLR

Address offset: 0x308

Disable interrupt

|                  |            |          |                                                                                       |                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|---------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          | L J I H                                                                               |                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  | G F E D C B A |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW CTS     |          |                                                                                       | Write '1' to disable interrupt for event <a href="#">CTS</a>  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Clear    | 1                                                                                     | Disable                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Read: Disabled                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Read: Enabled                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW NCTS    |          |                                                                                       | Write '1' to disable interrupt for event <a href="#">NCTS</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

| Bit number       |              |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|--------------|----------|---------------------------------------------------------------------------------------|--------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |              |          | L J I H                                                                               |                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  | G F E D C B A |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |              |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field   | Value ID | Value                                                                                 | Description                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Clear    | 1                                                                                     | Disable                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Disabled | 0                                                                                     | Read: Disabled                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Enabled  | 1                                                                                     | Read: Enabled                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW RXDRDY    |          |                                                                                       | Write '1' to disable interrupt for event <a href="#">RXDRDY</a>    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Clear    | 1                                                                                     | Disable                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Disabled | 0                                                                                     | Read: Disabled                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Enabled  | 1                                                                                     | Read: Enabled                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| D                | RW ENDRX     |          |                                                                                       | Write '1' to disable interrupt for event <a href="#">ENDRX</a>     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Clear    | 1                                                                                     | Disable                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Disabled | 0                                                                                     | Read: Disabled                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Enabled  | 1                                                                                     | Read: Enabled                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| E                | RW TXDRDY    |          |                                                                                       | Write '1' to disable interrupt for event <a href="#">TXDRDY</a>    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Clear    | 1                                                                                     | Disable                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Disabled | 0                                                                                     | Read: Disabled                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Enabled  | 1                                                                                     | Read: Enabled                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| F                | RW ENDTX     |          |                                                                                       | Write '1' to disable interrupt for event <a href="#">ENDTX</a>     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Clear    | 1                                                                                     | Disable                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Disabled | 0                                                                                     | Read: Disabled                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Enabled  | 1                                                                                     | Read: Enabled                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| G                | RW ERROR     |          |                                                                                       | Write '1' to disable interrupt for event <a href="#">ERROR</a>     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Clear    | 1                                                                                     | Disable                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Disabled | 0                                                                                     | Read: Disabled                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Enabled  | 1                                                                                     | Read: Enabled                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| H                | RW RXTO      |          |                                                                                       | Write '1' to disable interrupt for event <a href="#">RXTO</a>      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Clear    | 1                                                                                     | Disable                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Disabled | 0                                                                                     | Read: Disabled                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Enabled  | 1                                                                                     | Read: Enabled                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| I                | RW RXSTARTED |          |                                                                                       | Write '1' to disable interrupt for event <a href="#">RXSTARTED</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Clear    | 1                                                                                     | Disable                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Disabled | 0                                                                                     | Read: Disabled                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Enabled  | 1                                                                                     | Read: Enabled                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| J                | RW TXSTARTED |          |                                                                                       | Write '1' to disable interrupt for event <a href="#">TXSTARTED</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Clear    | 1                                                                                     | Disable                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Disabled | 0                                                                                     | Read: Disabled                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Enabled  | 1                                                                                     | Read: Enabled                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| L                | RW TXSTOPPED |          |                                                                                       | Write '1' to disable interrupt for event <a href="#">TXSTOPPED</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Clear    | 1                                                                                     | Disable                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Disabled | 0                                                                                     | Read: Disabled                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |              | Enabled  | 1                                                                                     | Read: Enabled                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.39.9.37 ERRORSRC

Address offset: 0x480

Error source

Note : this register is read / write one to clear.

| Bit number       |      |         | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                                                                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|---------|---------------------------------------------------------------------------------------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |      |         | D C B A                                                                               |       |                                                                                                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |         | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |       |                                                                                                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field   | Value ID                                                                              | Value | Description                                                                                                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW   | OVERRUN |                                                                                       |       | Overrun error                                                                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |         |                                                                                       |       | A start bit is received while the previous data still lies in RXD. (Previous data is lost.)                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |         | NotPresent                                                                            | 0     | Read: error not present                                                                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |         | Present                                                                               | 1     | Read: error present                                                                                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW   | PARITY  |                                                                                       |       | Parity error                                                                                                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |         |                                                                                       |       | A character with bad parity is received, if HW parity check is enabled.                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |         | NotPresent                                                                            | 0     | Read: error not present                                                                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |         | Present                                                                               | 1     | Read: error present                                                                                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW   | FRAMING |                                                                                       |       | Framing error occurred                                                                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |         |                                                                                       |       | A valid stop bit is not detected on the serial data input after all bits in a character have been received.                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |         | NotPresent                                                                            | 0     | Read: error not present                                                                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |         | Present                                                                               | 1     | Read: error present                                                                                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| D                | RW   | BREAK   |                                                                                       |       | Break condition                                                                                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |         |                                                                                       |       | The serial data input is '0' for longer than the length of a data frame. (The data frame length is 10 bits without parity bit, and 11 bits with parity bit.). |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |         | NotPresent                                                                            | 0     | Read: error not present                                                                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |         | Present                                                                               | 1     | Read: error present                                                                                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.39.9.38 ENABLE

Address offset: 0x500

Enable UART

|                  |            |          |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          |       | A A A A                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | ENABLE   |       | Enable or disable UARTE                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0     | Disable UARTE                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 8     | Enable UARTE                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.39.9.39 PSEL.RTS

Address offset: 0x508

Pin select for RTS signal

|                  |      |         |              |    |         |    |    |    |    |    |    |    |    |    |             |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |             |  |  |  |   |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|---------|--------------|----|---------|----|----|----|----|----|----|----|----|----|-------------|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------------|--|--|--|---|---|---|---|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |         |              | 31 | 30      | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20          | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |             |  |  |  |   |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |         |              | C  |         |    |    |    |    |    |    |    |    |    |             |    |    |    |    |    |    |    |    |    |    |   |   | B |   |   |   |   |   |   |   |             |  |  |  | A | A | A | A | A |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0xFFFFFFFF |      |         |              | 1  | 1       | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1           | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1           |  |  |  |   |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field   | Value        | ID | Value   |    |    |    |    |    |    |    |    |    |             |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | Description |  |  |  |   |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW   | PIN     |              |    | [0..31] |    |    |    |    |    |    |    |    |    | Pin number  |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |             |  |  |  |   |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW   | PORT    |              |    | [0..1]  |    |    |    |    |    |    |    |    |    | Port number |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |             |  |  |  |   |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW   | CONNECT |              |    |         |    |    |    |    |    |    |    |    |    |             |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | Connection  |  |  |  |   |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |         | Disconnected |    | 1       |    |    |    |    |    |    |    |    |    | Disconnect  |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |             |  |  |  |   |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |         | Connected    |    | 0       |    |    |    |    |    |    |    |    |    | Connect     |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |             |  |  |  |   |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

#### 7.1.39.9.40 PSEL.TXD

Address offset: 0x50C

Pin select for TXD signal

|                  |      |         |              |    |         |            |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |   |   |   |   |
|------------------|------|---------|--------------|----|---------|------------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|--|---|---|---|---|---|
| Bit number       |      |         |              | 31 | 30      | 29         | 28          | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |  |   |   |   |   |   |
| ID               |      |         |              | C  |         |            |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | B |   |   |   |   |   |   |   |   |  |  |  | A | A | A | A | A |
| Reset 0xFFFFFFFF |      |         |              | 1  | 1       | 1          | 1           | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  |  |  |   |   |   |   |   |
| ID               | Acce | Field   | Value        | ID | Value   |            | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |   |   |   |   |
| A                | RW   | PIN     |              |    | [0..31] |            | Pin number  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |   |   |   |   |
| B                | RW   | PORT    |              |    | [0..1]  |            | Port number |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |   |   |   |   |
| C                | RW   | CONNECT |              |    |         |            | Connection  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |   |   |   |   |
|                  |      |         | Disconnected |    | 1       | Disconnect |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |   |   |   |   |
|                  |      |         | Connected    |    | 0       | Connect    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |   |   |   |   |

#### 7.1.39.9.41 PSEL.CTS

Address offset: 0x510

Pin select for CTS signal

|                  |            |  |  |  |              |  |  |  |         |    |    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|--|--|--------------|--|--|--|---------|----|----|----|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |  |  |              |  |  |  |         | 31 | 30 | 29 | 28          | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |
| ID               |            |  |  |  |              |  |  |  |         | C  |    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | B  |    |   |   |   |   |   |   |   |   | A | A | A | A |   |   |
| Reset 0xFFFFFFFF |            |  |  |  |              |  |  |  |         | 1  | 1  | 1  | 1           | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ID               | Acce Field |  |  |  | Value ID     |  |  |  | Value   |    |    |    | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW PIN     |  |  |  |              |  |  |  | [0..31] |    |    |    | Pin number  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW PORT    |  |  |  |              |  |  |  | [0..1]  |    |    |    | Port number |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| C                | RW CONNECT |  |  |  |              |  |  |  |         |    |    |    | Connection  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  |  |  | Disconnected |  |  |  | 1       |    |    |    | Disconnect  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  |  |  | Connected    |  |  |  | 0       |    |    |    | Connect     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.39.9.42 PSEL.RXD

Address offset: 0x514

Pin select for RXD signal

|                  |      |         |              |    |       |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |             |             |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|---------|--------------|----|-------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|-------------|-------------|---|---|---|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |         |              | 31 | 30    | 29      | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |             |             |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |         |              | C  |       |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | B |   |   |   |   |   |   |   |   |  |  |             | A           | A | A | A | A |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0xFFFFFFFF |      |         |              | 1  | 1     | 1       | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  |  |             |             |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field   | Value        | ID | Value |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | Description |             |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW   | PIN     |              |    |       | [0..31] |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |             | Pin number  |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW   | PORT    |              |    |       | [0..1]  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |             | Port number |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | RW   | CONNECT |              |    |       |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |             | Connection  |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |         | Disconnected |    |       | 1       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |             | Disconnect  |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |         | Connected    |    |       | 0       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |             | Connect     |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.39.9.43 BAUDRATE

Address offset: 0x524

Baud rate. Accuracy depends on the HFCLK source selected.

| Bit number       |      |          | 31         | 30 | 29         | 28                                | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |
|------------------|------|----------|------------|----|------------|-----------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|--|
| ID               |      |          | A          | A  | A          | A                                 | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |  |  |  |  |
| Reset 0x04000000 |      |          | 0          | 0  | 0          | 0                                 | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |  |
| ID               | Acce | Field    | Value      | ID | Value      | Description                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| A                | RW   | BAUDRATE |            |    |            | Baud rate                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |      |          | Baud1200   |    | 0x0004F000 | 1200 baud (actual rate: 1205)     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |      |          | Baud2400   |    | 0x0009D000 | 2400 baud (actual rate: 2396)     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |      |          | Baud4800   |    | 0x0013B000 | 4800 baud (actual rate: 4808)     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |      |          | Baud9600   |    | 0x00275000 | 9600 baud (actual rate: 9598)     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |      |          | Baud14400  |    | 0x003AF000 | 14400 baud (actual rate: 14401)   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |      |          | Baud19200  |    | 0x004EA000 | 19200 baud (actual rate: 19208)   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |      |          | Baud28800  |    | 0x0075C000 | 28800 baud (actual rate: 28777)   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |      |          | Baud31250  |    | 0x00800000 | 31250 baud                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |      |          | Baud38400  |    | 0x009D0000 | 38400 baud (actual rate: 38369)   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |      |          | Baud56000  |    | 0x00E50000 | 56000 baud (actual rate: 55944)   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |      |          | Baud57600  |    | 0x00EB0000 | 57600 baud (actual rate: 57554)   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |      |          | Baud76800  |    | 0x013A9000 | 76800 baud (actual rate: 76923)   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |      |          | Baud115200 |    | 0x01D60000 | 115200 baud (actual rate: 115108) |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |      |          | Baud230400 |    | 0x03B00000 | 230400 baud (actual rate: 231884) |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |      |          | Baud250000 |    | 0x04000000 | 250000 baud                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |      |          | Baud460800 |    | 0x07400000 | 460800 baud (actual rate: 457143) |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |      |          | Baud921600 |    | 0x0F000000 | 921600 baud (actual rate: 941176) |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |      |          | Baud1M     |    | 0x10000000 | 1Mega baud                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |

### 7.1.39.9.44 RXD.PTR

Address offset: 0x534

Data pointer

|                  |            |  |  |  |          |  |  |  |       |    |    |    |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|--|--|----------|--|--|--|-------|----|----|----|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |  |  |          |  |  |  |       | 31 | 30 | 29 | 28           | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |  |  |  |          |  |  |  |       | A  | A  | A  | A            | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |  |  |          |  |  |  |       | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  |  |  | Value ID |  |  |  | Value |    |    |    | Description  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW PTR     |  |  |  |          |  |  |  |       |    |    |    | Data pointer |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

**Note:** See the memory chapter for details about which memories are available for EasyDMA.

### 7.1.39.9.45 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in receive buffer

|                  |            |          |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          | A A A A A A A A A A A A A A A A                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Description                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW MAXCNT  |          | [1..0xFFFF]                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Maximum number of bytes in receive buffer |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.39.9.46 RXD.AMOUNT

Address offset: 0x53C

Number of bytes transferred in the last transaction

|                  |            |        |          |                                                                                       |                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                 |  |  |  |
|------------------|------------|--------|----------|---------------------------------------------------------------------------------------|-----------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---------------------------------|--|--|--|
| Bit number       |            |        |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                 |  |  |  |
| ID               |            |        |          |                                                                                       |                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A A A A A A A A A |  |  |  |
| Reset 0x00000000 |            |        |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                 |  |  |  |
| ID               | Acce Field |        | Value ID | Value                                                                                 | Description                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                 |  |  |  |
| A                | R          | AMOUNT |          | [1..0xFFFF]                                                                           | Number of bytes transferred in the last transaction |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                 |  |  |  |

### 7.1.39.9.47 TXD.PTR

Address offset: 0x544

Data pointer

| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |            |          | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Description |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | PTR      | Data pointer                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**Note:** See the memory chapter for details about which memories are available for EasyDMA.

### 7.1.39.9.48 TXD.MAXCNT

Address offset: 0x548

Maximum number of bytes in transmit buffer

| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|--------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |            |          | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A                           |                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | MAXCNT   | [1..0xFFFF]                                                                           | Maximum number of bytes in transmit buffer |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.39.9.49 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transferred in the last transaction

|                  |            |        |          |             |    |    |    |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------|----------|-------------|----|----|----|-----------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |        |          | 31          | 30 | 29 | 28 | 27                                                  | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |        |          |             |    |    |    |                                                     |    |    |    |    |    |    |    |    |    |    |    | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |        |          | 0           | 0  | 0  | 0  | 0                                                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |
| ID               | Acce Field |        | Value ID | Value       |    |    |    | Description                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | R          | AMOUNT |          | [1..0xFFFF] |    |    |    | Number of bytes transferred in the last transaction |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.39.9.50 CONFIG

Address offset: 0x56C

Configuration of parity and hardware flow control

| Bit number       |      |            |          | 31    | 30                      | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |  |
|------------------|------|------------|----------|-------|-------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|--|
| ID               |      |            |          |       |                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | D |   |   |   |   | C | B | B | B | A |  |
| Reset 0x00000000 |      |            |          | 0     | 0                       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |  |
| ID               | Acce | Field      | Value ID | Value | Description             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |
| A                | RW   | HWFC       |          |       | Hardware flow control   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |            | Disabled | 0     | Disabled                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |            | Enabled  | 1     | Enabled                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |
| B                | RW   | PARITY     |          |       | Parity                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |            | Excluded | 0x0   | Exclude parity bit      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |            | Included | 0x7   | Include even parity bit |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |
| C                | RW   | STOP       |          |       | Stop bits               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |            | One      | 0     | One stop bit            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |            | Two      | 1     | Two stop bits           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |
| D                | RW   | PARITYTYPE |          |       | Even or odd parity type |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |            | Even     | 0     | Even parity             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |            | Odd      | 1     | Odd parity              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |

## 7.1.39.10 Electrical specification

### 7.1.39.10.1 UARTE electrical specification

| Symbol            | Description                                            | Min. | Typ. | Max. | Units |
|-------------------|--------------------------------------------------------|------|------|------|-------|
| $f_{UARTE}$       | Baud rate for UARTE <sup>27</sup> .                    | ..   | ..   | ..   | kbps  |
| $t_{UARTE,CTSH}$  | CTS high time                                          | ..   | ..   | ..   | μs    |
| $t_{UARTE,START}$ | Time from STARTRX/STARTTX task to transmission started | ..   | ..   | ..   | μs    |

## 7.1.40 USB — Universal serial bus device

The USB device (USB\_D) controller implements a full speed USB device function that meets 2.0 revision of the USB specification.

<sup>27</sup> High baud rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.

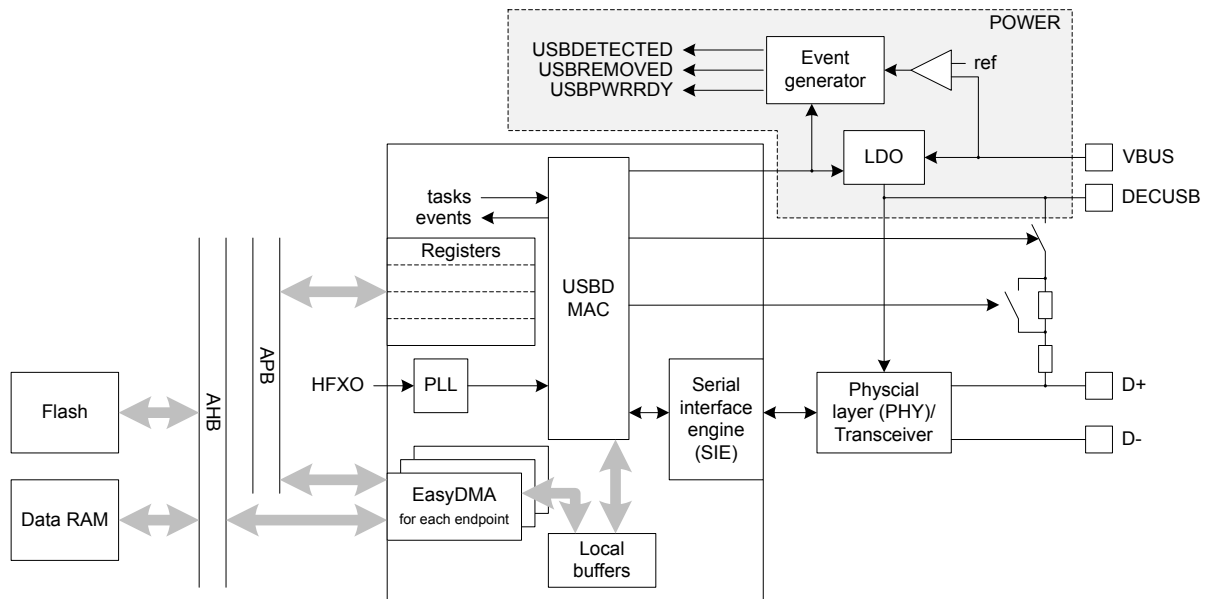


Figure 226: USB device block diagram

Listed here are the main features for USB:

- Implements full-speed (12 Mbps) device fully compliant to [Universal Serial Bus Specification Revision 2.0](#), including following engineering change notices (ECNs) issued by USB Implementers Forum:
  - *Pull-up/pull-down Resistors ECN*
  - *5V Short Circuit Withstand Requirement Change ECN*
- USB device stack available in the Nordic SDK
- Integrated (on-chip) USB transceiver (PHY)
- Software controlled on-chip pull-up on D+
- Endpoints:
  - 2 control (1 IN, 1 OUT)
  - 14 bulk/interrupt (7 IN, 7 OUT)
  - 2 isochronous (1 IN, 1 OUT)
- Supports double buffering for isochronous (ISO) endpoints (IN/OUT)
- Supports USB suspend, resume, and remote wake-up
- 64 bytes buffer size for each bulk/interrupt endpoint
- Up to 1023 bytes buffer size for ISO endpoints
- EasyDMA for all data transfers

#### 7.1.40.1 USB device states

The behavior of a USB device can be modelled through a state diagram.

The USB specification revision 2.0 (see *Chapter 9 USB Device Framework*) defines a number of states for a USB device, as illustrated below.



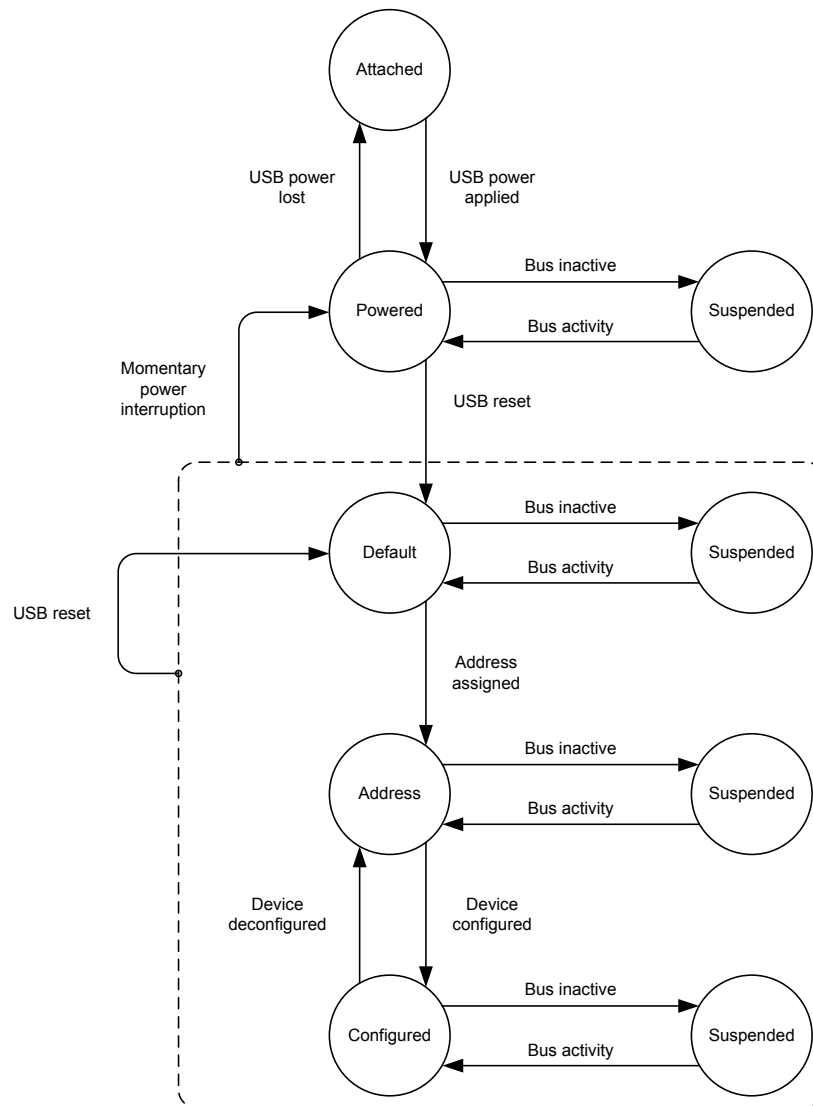


Figure 227: Device state diagram

The device must change state according to host-initiated traffic and USB bus states. It is up to the software to implement a state machine that matches the above definition. To detect the presence or absence of USB supply (VBUS), the **POWER** chapter defines two events, USBDETECTED and USBREMOVED, which can be used to implement the state machine.

As a general rule when implementing the software, the host behavior shall never be assumed to be predictable. In particular the sequence of commands received during an enumeration. The software shall always react to the current bus conditions or commands sent by the host.

#### 7.1.40.2 USB terminology

The USB specification defines bus states, rather than logic levels on the D+ and D- lines.

For a full speed device, the bus state where the D+ line is high and the D- line is low is defined as the J state. The bus state where D+ is low and D- high is called the K state.

An idle bus, where D+ and D- lines are only polarized through the pull-up on D+ and pull-downs on the host side, will be in J state.

Both lines low are called SE0 (single-ended 0), and both lines high SE1 (single-ended 1).

### 7.1.40.3 USB pins

The USB peripheral features a number of dedicated pins.

The dedicated USB pins can be grouped in two categories, signal and power. The signal pins consist of the D+ and D- pins, which are to be connected to the USB host. They are dedicated pins, and not available as standard GPIOs. The USB implements the *5V Short Circuit Withstand ECU* meaning that these two pins are not 5 V tolerant.

The signal pins and the pull-up will operate only while VBUS is in its valid voltage range, and USB is enabled through the **ENABLE** register. For details on the USB power supply and VBUS detection, see **POWER**.

See **Pin assignments** on page 764 for more information about the pinout.

### 7.1.40.4 USB power-up sequence

The physical layer interface (PHY)/USB transceiver is powered separately from the rest of the device (VBUS pin), which has some implications on the USB power-up sequence.

The device is not able to properly signal its presence to the USB host and handle traffic from the host, unless the PHY's power supply is enabled and stable. Turning the PHY's power supply on/off is directly linked to register **ENABLE**. The device provides events that help synchronizing software to the various steps during the power-up sequence.

To make sure that all resources in USB are available and the dedicated USB voltage regulator stabilized, the following is recommended:

- Enable USB after VBUS has been detected only
- Turn the USB pull-up on after:
  - USBPWRDY event has occurred
  - USBEVENT has occurred, with the READY condition flagged in **EVENTCAUSE**

The following sequence chart illustrates a typical handling of VBUS power-up:

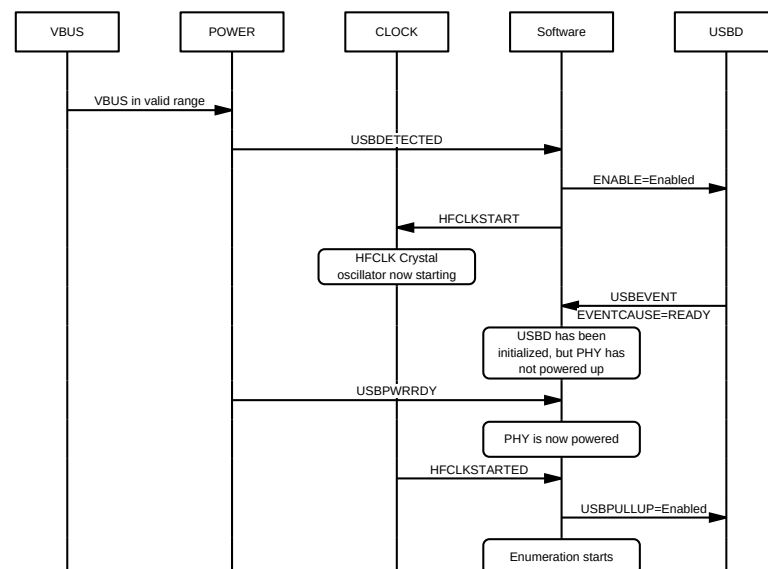


Figure 228: VBUS power-up sequence

Upon VBUS removal detection, signalled by the USBREMOVED event described in **POWER**, it is recommended to let on-going EasyDMA transfers finish (wait for the relevant ENDEPIN[n], ENDISOIN, ENDEPOUT[n] or ENDISOOUT event, see **EasyDMA** on page 681), before disabling USB (by writing **ENABLE=Disabled**). Reading the **ENABLE** register will return Enabled until USB is completely disabled.

### 7.1.40.5 USB pull-up

The USB pull-up serves two purposes - it indicates to the host that the device is connected to the USB bus, and it indicates the device's speed capability.

When no pull-up is connected to the USB bus, the host sees both D+ and D- lines low, as they are pulled down on the host side by 15 k $\Omega$  resistors. The device is not seen by the host and hence in detached state, even though it could be physically connected to the host. USB specification does not allow to draw any current on VBUS in that situation.

When a full-speed device connects its 1.5 k $\Omega$  pull-up to D+, the host sees the corresponding line high. The device is then in the attached state. During the enumeration process, the host attempts to determine if the full-speed device also supports higher speeds and initiates communication with the device to further identify it. The USB peripheral implemented in this device supports only full-speed (12 Mbps), and thus ignores the negotiation for higher speeds in accordance with the USB specification revision 2.0.

Register [USBPULLUP](#) provides means to connect or disconnect the pull-up on D+ under software control. This allows the software to control when USB enumeration takes place. It also allows to emulate a physical disconnect from the USB bus, for instance when re-enumeration is required. [USBPULLUP](#) has to be enabled to allow the USB peripheral to handle USB traffic and generate appropriate events. This forbids the use of an external pull-up.

Note that disconnecting the pull-up through register [USBPULLUP](#) while connected to a host, will result in both D+ and D- lines to be pulled low by the host's pull-down resistors. However, as mentioned above, this will also inhibit the generation of the USBRESET event. The pull-up is disabled by default after a chip reset.

The pull-up shall only get connected after USB peripheral has been enabled through register [ENABLE](#). The USB pull-up value is automatically changed depending on the bus activity, as specified in *Resistor ECN* which amends the original USB specification version 2.0. The user does not have access to this function, it is handled in hardware.

While they should never be used in normal traffic activity, lines D+ and D- may at any time be forced into state specified in register [DPDMVALUE](#) by the task DPDMDRIVE. The DPDMNODRIVE task stops driving them, and PHY returns to normal operation.

### 7.1.40.6 USB reset

The USB specification defines a USB reset, which is not to be confused with a chip reset. The USB reset is a normal USB bus condition, and is used as part of the enumeration sequence, it does not reset the chip.

The USB reset results from a single-ended low state (SE0) on lines D+/D- for a  $t_{\text{USB,DETRST}}$  amount of time. Only the host is allowed to drive a USB reset condition on the bus. The USB peripheral automatically interprets a SE0 longer than  $t_{\text{USB,DETRST}}$  as a USB reset. When the device detects a USB reset and generates a USBRESET event, the device USB stack and related parts of the application shall re-initialize themselves, and go back to the default state.

Some of the registers in the USB peripheral get automatically reset to a known state, in particular all data endpoints are disabled and the [USBADDR](#) reset to 0.

After the device has connected to the USB bus (i.e. after VBUS is applied), the device shall not respond to any traffic from the time the pull-up is enabled until it has seen a USB reset condition. This is automatically ensured by the USB peripheral.

After a USB reset, the device shall be fully responsive after at most  $T_{\text{RSTRCY}}$  (according to chapter 7 in the USB specification). Software shall take into account this time that takes the hardware to recover from a USB reset condition.

### 7.1.40.7 USB suspend and resume

Normally, the host will maintain activity on the USB at least every millisecond according to USB specification. A USB device will enter suspend when there is no activity on the bus (idle) for a given time. The device will resume operation when it receives any non idle signalling.

To signal that the device shall go into low power mode (suspend), the host stops activity on the USB bus, which becomes idle. Only the device pull-up and host pull-downs act on D+ and D-, and the bus is thus kept at a constant J state. It is up to the device to detect this lack of activity, and enter the low power mode (suspend) within a specified time.

The USB host can decide to suspend or resume USB activity at any time. If remote wake-up is enabled, the device may signal to the host to resume from suspend.

#### 7.1.40.7.1 Entering suspend

The USB peripheral automatically detects lack of activity for more than a defined amount of time, and performs steps needed to enter suspend.

When no activity has been detected for longer than  $t_{\text{USB,SUSPEND}}$ , the USB peripheral generates the USBEVENT event with SUSPEND bit set in register **EVENTCAUSE**. The software shall ensure that the current drawn from the USB supply line VBUS is within the specified limits before  $T_{2\text{SUSP}}$ , as defined in chapter 7 of the USB specification. In order to reduce idle current of USB peripheral, the software must explicitly place the USB peripheral in low power mode through writing **LowPower** to register **LOWPOWER**.

In order to save power, and provided that no other peripheral needs it, the crystal oscillator (HFXO) in **CLOCK** may be disabled by software during the USB suspend, while the USB pull-up is disconnected, or when VBUS is not present. Software must explicitly enable it at any other time. The USB peripheral will not be able to respond to USB traffic unless HFXO is enabled and stable.

#### 7.1.40.7.2 Host-initiated resume

Once the host resumes the bus activity, it has to be responsive to incoming requests on the USB bus within the time  $T_{\text{RSMRCY}}$  (as defined in chapter 7 of the USB specification) and revert to normal power consumption mode.

If the host resumes bus activity with or without a RESUME condition (in other words: bus activity is defined as any non-J state), the USB peripheral will generate a USBEVENT event, with RESUME bit set in register **EVENTCAUSE**. If the host resumes bus activity simply by restarting sending frames, the USB peripheral will generate SOF events.

#### 7.1.40.7.3 Device-initiated remote wake-up

Assuming the remote wake-up is supported by the device and enabled by the host, the device can request the host to resume from suspend if wake-up condition is met.

To do so, the HFXO needs to be enabled first. After waking up the HFXO, the software must bring USB peripheral out of the low power mode and into the normal power consumption mode through writing **ForceNormal** in register **LOWPOWER**. It can then instruct the USB peripheral to drive a RESUME condition (K state) on the USB bus by triggering the **DPDMDRIVE** task, and hence attempt to wake up the host. By choosing **Resume** in **DPDMVALUE**, the duration of the RESUME state is under hardware control ( $t_{\text{USB,DRIVEK}}$ ). By choosing **J** or **K**, the duration of that state is under software control (the J or K state is maintained until a **DPDMNODRIVE** task is triggered) and has to meet  $T_{\text{DRSMUP}}$  as specified in USB specification chapter 7.

Upon writing the **ForceNormal** in register **LOWPOWER**, a USBEVENT event is generated with the **USBWUALLOWED** bit set in register **EVENTCAUSE**.

The value in register **DPDMVALUE** on page 713 will only be captured and used when the **DPDMDRIVE** task is triggered. This value defines the state the bus will be forced into after the **DPDMDRIVE** task.

Note that the device shall ensure that it does not initiate a remote wake-up request before  $T_{\text{WTRSM}}$  (according to USB specification chapter 7) after the bus has entered idle state. Using the recommended

resume value in [DPDMVALUE](#) (rather than K) takes care of this, and postpones the RESUME state accordingly.

### 7.1.40.8 EasyDMA

The USB peripheral implements EasyDMA for accessing memory without CPU involvement.

Each endpoint has an associated set of registers, tasks and events. EasyDMA and traffic on USB are tightly related. A number of events provide insight of what is happening on the USB bus, and a number of tasks allow to somewhat automate response to the traffic.

**Note:** Endpoint 0 (IN and OUT) are implemented as control endpoint. For more information, see [Control transfers](#) on page 682.

## Registers

Enabling endpoints is controlled through the [EPINEN](#) and [EPOUTEN](#) registers.

The following registers define the memory address of the buffer for a specific IN or OUT endpoint:

- [EPIN\[n\].PTR](#), (n=0..7)
- [EPOUT\[n\].PTR](#), (n=0..7)
- [ISOIN.PTR](#)
- [ISOOUT.PTR](#)

The following registers define the amount of bytes to be sent on USB for next transaction:

- [EPIN\[n\].MAXCNT](#), (n=0..7)
- [ISOIN.MAXCNT](#)

The following registers define the length of the buffer (in bytes) for next transfer of incoming data:

- [EPOUT\[n\].MAXCNT](#), (n=1..7)
- [ISOOUT.MAXCNT](#)

Since the host decides how many bytes are sent over USB, the MAXCNT value can be copied from register [SIZE.EPOUT\[n\]](#) (n=1..7) or register [SIZE.ISOOUT](#).

Register [EPOUT\[0\].MAXCNT](#) defines the length of the OUT buffer (in bytes) for the control endpoint 0. If the USB host does not misbehave, register [SIZE.EPOUT\[0\]](#) will indicate the same value as `MaxPacketSize` from the device descriptor or `wLength` from the SETUP command, whichever the smallest.

The [.AMOUNT](#) registers indicate how many bytes actually have been transferred over EasyDMA during the last transfer.

Stalling bulk/interrupt endpoints is controlled through the [EPSTALL](#) register.

**Note:** Due to USB specification requirements, the effect of the stalling control endpoint 0 may be overridden by hardware, in particular when a new SETUP token is received.

EasyDMA will not copy the SETUP data to memory (it will only transfer data from the data stage). Setup data is available as separate registers in the USB peripheral:

- [BMREQUESTTYPE](#)
- [BREQUEST](#)
- [WVALUEL](#)
- [WVALUEH](#)
- [WINDEXL](#)
- [WINDEXH](#)

- [WLENGTHL](#)
- [WLENGTHH](#)

[EVENTCAUSE](#) register provides details on what caused a given USBEVENT event, for instance if a CRC error is detected during a transaction, or if bus activity stops or resumes.

## Tasks

Tasks [STARTEPIN\[n\]](#), [STARTEPOUT\[n\]](#) (n=0..7), [STARTISOIN](#) and [STARTISOOUT](#) capture the values for .PTR and .MAXCNT registers. For IN endpoints, a transaction over USB gets automatically triggered when the EasyDMA transfer is complete. For OUT endpoints, it is up to software to allow the next transaction over USB. See the examples in [Control transfers](#) on page 682, [Bulk and interrupt transactions](#) on page 685 and [Isochronous transactions](#) on page 688.

For the control endpoint 0, OUT transactions are allowed through the EPORCVOUT task. The EPOSTATUS task allows a status stage to be initiated, and the EPOSTALL task allows stalling further traffic (data or status stage) on the control endpoint.

## Events

The [STARTED](#) event confirms that the values of the .PTR and .MAXCNT registers of the endpoints flagged in register [EPSTATUS](#) have been captured. Those can then be modified by software for the next transfer.

Events [ENDEPIN\[n\]](#), [ENDEPOUT\[n\]](#) (n=0..7), [ENDISOIN](#) and [ENDISOOUT](#) events indicate that the whole buffer has been consumed. The buffer can be accessed safely by the software.

Only a single EasyDMA transfer can take place in USB0 at any time. Software must ensure that tasks [STARTEPIN\[n\]](#) (n=0..7), [STARTISOIN](#), [STARTEPOUT\[n\]](#) (n=0..7) or [STARTISOOUT](#) are not triggered before events [ENDEPIN\[n\]](#) (n=0..7), [ENDISOIN](#), [ENDEPOUT\[n\]](#) (n=0..7) or [ENDISOOUT](#) are received from an on-going transfer.

The [EPDATA](#) event indicates that a successful (acknowledged) data transaction has occurred on the data endpoint(s) flagged in register [EPDATASTATUS](#). A successful (acknowledged) data transaction on endpoint 0 is signalled by the [EPODATADONE](#) event.

At any time a [USBEVENT](#) event may be sent, with details provided in [EVENTCAUSE](#) register.

[EPOSETUP](#) event indicates that a SETUP token has been received on the control endpoint 0, and that the setup data is available in [registers](#).

### 7.1.40.9 Control transfers

The USB specification mandates every USB device to implement endpoint 0 IN and OUT as control endpoints.

A control transfer consists of two or three stages:

- Setup stage
- Data stage (optional)
- Status stage

Each control transfer can be one of following types:

- Control read
- Control read no data
- Control write
- Control write no data

An EPOSETUP event indicates that the data in the setup stage (following the SETUP token) is available in [registers](#).

The data in the data stage (following the IN or OUT token) is transferred from or to the desired location using EasyDMA.

The control endpoint buffer can be of any size.

After receiving the SETUP token, the USB controller will not accept (NAK) any incoming IN or OUT tokens until the software has finished decoding the command, determining the type of transfer, and preparing for the next stage (data or status) appropriately.

The software can choose to stall a command (in both data and status stages) through the EPOSTALL task, for instance if the command is not supported, or its wValue, wIndex or wLength parameters are wrong. A stalled control read transfer is illustrated below, but the same mechanism (same tasks) applies to stalling a control write transfer (not illustrated):

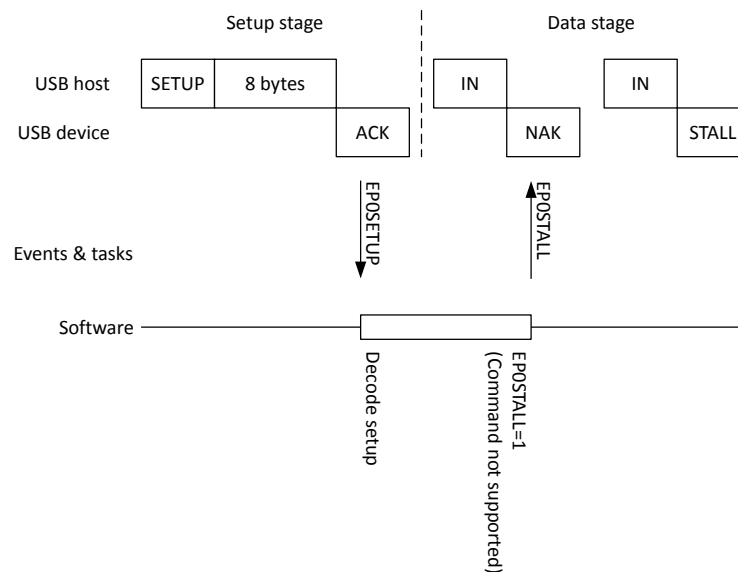


Figure 229: Control read gets stalled

See chapter 9 of the USB specification and relevant class specifications for rules on when to stall a command.

**Note:** The USB peripheral handles the SetAddress transfer by itself. As a consequence, the software shall not process this command other than updating its state machine (see [Device state diagram](#)), nor initiate a status stage. If necessary, the address assigned by the host can be read out from the USBADDR register after the command has been processed.

#### 7.1.40.9.1 Control read transfer

This section describes how the software behaves to respond to a control read transfer.

As mentioned earlier, the USB controller will not accept (NAK) any incoming IN tokens until software has finished decoding the command, determining the type of transfer, and preparing for the next stage (data or status) appropriately.

For a control read, transferring the data from memory into USB will trigger a valid, acknowledged (ACK) IN transaction on USB.

The software has to prepare EasyDMA by pointing to the buffer containing the data to be transferred. If no other EasyDMA transfers are on-going with USB, the software can send the STARTEPIN0 task, which will initiate the data transfer and transaction on USB.

A STARTED event (with EPIN0 bit set in the [EPSTATUS](#) register) will be generated as soon as the EPIN[0].PTR and .MAXCNT registers have been captured. Software may then prepare them for the next data transaction.

An ENDEPIN[0] event will be generated when the data has been transferred from memory to the USBD peripheral.

Finally, an EP0DATADONE event will be generated when the data has been transmitted over USB and acknowledged by the host.

The software can then either prepare and transmit the next data transaction by repeating the above sequence, or initiate the status stage through the EPOSTATUS task.

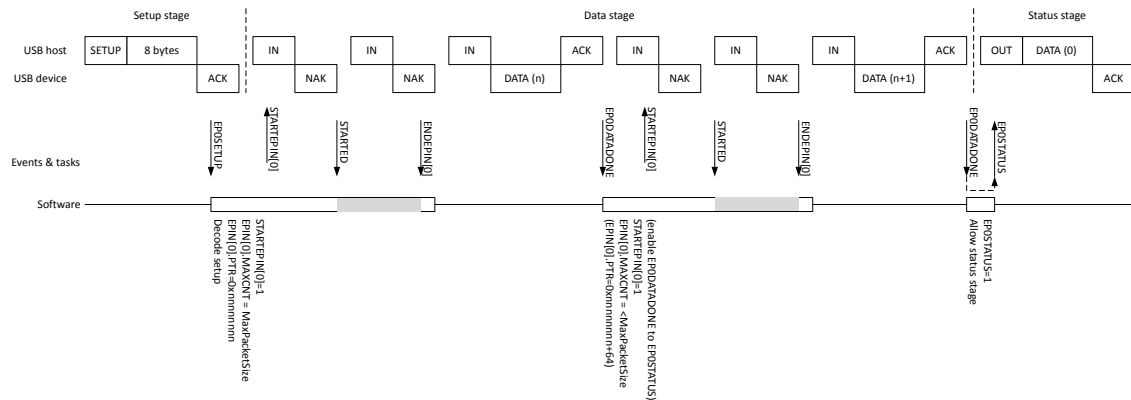


Figure 230: Control read transfer

Note the possibility to enable a shortcut from the EP0DATADONE event to the EPOSTATUS task, typically if the data stage is expected to take a single transfer. If there is no data stage, the software can initiate the status stage through the EPOSTATUS task right away, as illustrated below:

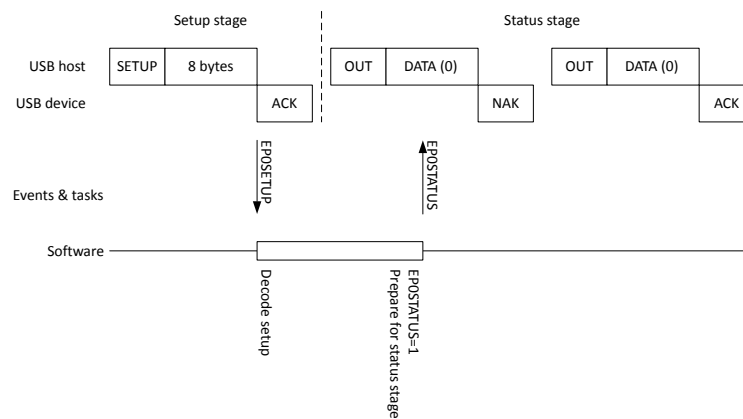


Figure 231: Control read no data transfer

#### 7.1.40.9.2 Control write transfer

This section describes how the software responds to a control write transfer.

The software has to prepare EasyDMA by pointing to the buffer in memory that shall contain the incoming data. If no other EasyDMA transfers are on-going with USB, the software can then send the EP0RCVOUT task, which will make USB acknowledge (ACK) the first OUT+DATA transaction from the host.

An EP0DATADONE event will be generated when a new OUT+DATA has been transmitted over USB, and is about to get acknowledged by the device.



A STARTED event (with EPOUT0 bit set in the EPSTATUS register) will be generated as soon as the EPOUT[0].PTR and .MAXCNT registers have been captured, after receiving the first transaction. Software may then prepare them for the next data transaction.

An ENDEPOUT[0] event will be generated when the data has been transferred from the USB peripheral to memory. The software can then either prepare to receive the next data transaction by repeating the above sequence, or initiate the status stage through the EPOSTATUS task. Until then, further incoming OUT +DATA transactions get a NAK response by the device.

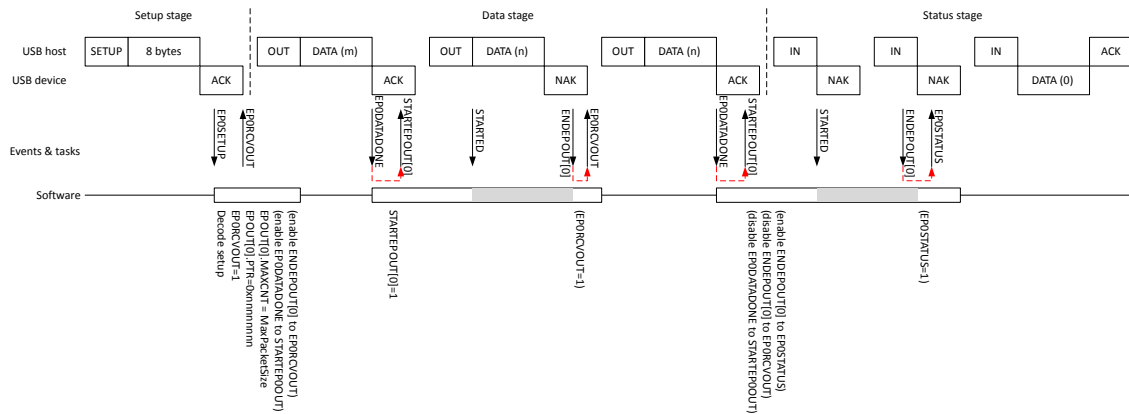


Figure 232: Control write transfer

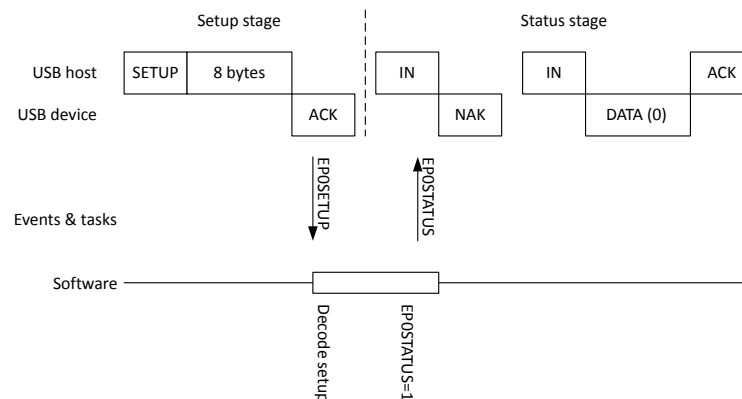


Figure 233: Control write no data transfer

#### 7.1.40.10 Bulk and interrupt transactions

The USB peripheral implements seven pairs of bulk/interrupt endpoints.

The bulk/interrupt endpoints have a fixed USB endpoint number, summarized in the table below.

| Bulk endpoint # | USB IN endpoint | USB OUT endpoint |
|-----------------|-----------------|------------------|
| [1]             | 0x81            | 0x01             |
| [2]             | 0x82            | 0x02             |
| [3]             | 0x83            | 0x03             |
| [4]             | 0x84            | 0x04             |
| [5]             | 0x85            | 0x05             |
| [6]             | 0x86            | 0x06             |
| [7]             | 0x87            | 0x07             |

Table 176: Bulk/interrupt endpoint numbering

A bulk/interrupt transaction consists of a single data stage. Two consecutive, successful transactions are distinguished through alternating leading process ID (PID): DATA0 follows DATA1, DATA1 follows DATA0,

etc. A repeated transaction is detected by re-using the same PID as previous transaction, i.e DATA0 follows DATA0, or DATA1 follows DATA1.

The USB controller automatically toggles DATA0/DATA1 PIDs for every bulk/interrupt transaction, and in general software does not need to care about it.

If an incoming data is corrupted (CRC does not match), the USB controller automatically prevents DATA0/DATA1 from toggling, to request the host to resend the data.

In some specific cases, the software may want to force a data toggle (usually reset) on a specific IN endpoint, or force the expected toggle on an OUT endpoint, for instance as a consequence of the host issuing **ClearFeature**, **SetInterface** or selecting an alternate setting. Controlling the data toggle of data IN or OUT endpoint  $n$  ( $n=1..7$ ) is done through register **DTOGGLE**.

The bulk/interrupt transaction in USB full-speed can be of any size up to 64 bytes, and it has to be a multiple of 4 bytes and 32-bit aligned in memory.

When the transaction is done over USB, an EPDATA event is generated. The hardware will then automatically respond with NAK to all incoming IN tokens until the software is ready to send more data and has finished configuring the EasyDMA, started it, and the whole buffer content has been moved to USB controller (signalled by the ENDEPIN[n] event).

Each IN or OUT data endpoint has to be explicitly enabled by software through register **EPINEN** or **EPOUTEN**, according to the configuration declared by the device and selected by the host through the **SetConfig** command.

A disabled data endpoint will not respond to any traffic from the host. An enabled data endpoint will normally respond NAK or ACK (depending on the readiness of the buffers), or STALL (if configured in register **EPSTALL**), in which case the endpoint is asked to halt). The halted (or not) state of a given endpoint can be read back from register **HALTED.EPIN[n]** or **HALTED.EPOUT[n]**. The format of the returned 16-bit value can be copied as is as response to a **GetStatusEndpoint** request from the host.

Note that enabling or disabling an endpoint will not change its halted state. However, a USB reset will disable and clear the halted state of all data endpoints.

The control endpoint 0 IN and OUT can also be enabled and/or halted using the same mechanisms, but due to USB specification, receiving a SETUP will override its state.

#### 7.1.40.10.1 Bulk and interrupt IN transaction

The host issues IN tokens to receive bulk/interrupt data. In order to send data, the software has to enable the endpoint and prepare an EasyDMA transfer on the desired endpoint.

Bulk/interrupt IN endpoints are enabled or disabled through their respective INN bit ( $n=1..7$ ) in **EPINEN** register.

It is also possible to stall or un-stall an endpoint through the **EPSTALL** register.

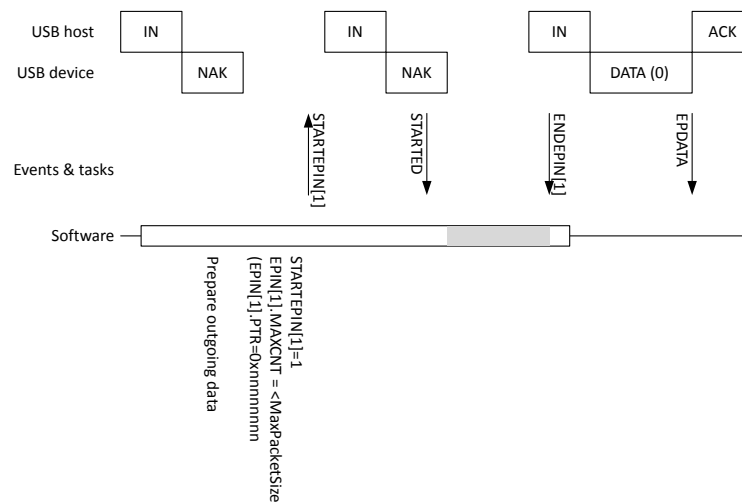


Figure 234: Bulk/interrupt IN transaction

It is possible (and in some situations it is required) to respond to an IN token with a zero-length data packet.

**Note:** On many USB hosts, not responding (DATA+ACK or NAK) to three IN tokens on an interrupt endpoint would have the host disable that endpoint as a consequence. Re-enumerating the device (unplug-replug) may be required to restore functionality. Make sure that the relevant data endpoints are enabled for normal operation as soon as the device gets configured through a **SetConfig** request.

#### 7.1.40.10.2 Bulk and interrupt OUT transaction

When the host wants to transmit bulk/interrupt data, it issues an OUT token (packet) followed by a DATA packet on a given endpoint  $n$  ( $n=1..7$ ).

A NAK is returned until the software writes any value to register [SIZE.EPOUT\[n\]](#), indicating that the content of the local buffer can be overwritten. Upon receiving the next OUT+DATA transaction, an ACK is returned to the host while an EPDATA event is generated (and the [EPDATASTATUS](#) register flags are set to indicate on which endpoint this happened). Once the EasyDMA is prepared and enabled, by writing the [EPOUT\[n\]](#) registers and triggering the [STARTEPOUT\[n\]](#) task, the incoming data will be transferred to memory. Until that transfer is finished, the hardware will automatically NAK any other incoming OUT+DATA packets. Only when the EasyDMA transfer is done (signalled by the [ENDEPOUT\[n\]](#) event), or as soon as any values are written by the software in register [SIZE.EPOUT\[n\]](#), the endpoint  $n$  will accept incoming OUT+DATA again.

It is allowed for the host to send zero-length data packets.

Bulk/interrupt OUT endpoints are enabled or disabled through their respective OUTn bit ( $n=1..7$ ) in the [EPOUTEN](#) register. It is also possible to stall or un-stall an endpoint through the [EPSTALL](#) register.

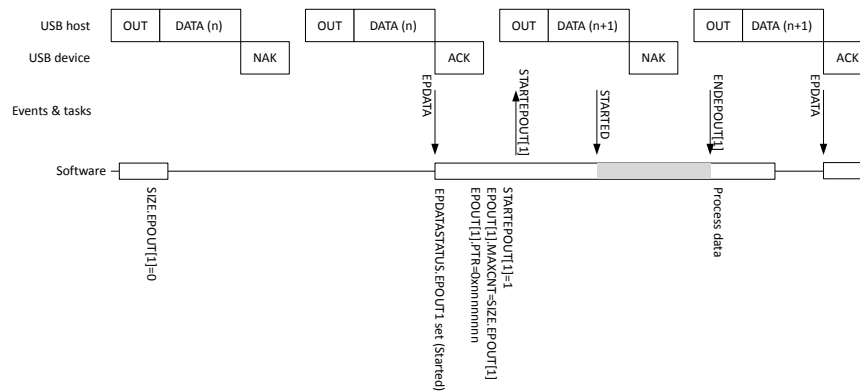


Figure 235: Bulk/interrupt OUT transaction

### 7.1.40.11 Isochronous transactions

The USB peripheral implements isochronous (ISO) endpoints.

The ISO endpoints have a fixed USB endpoint number, summarized in the table below.

| ISO endpoint # | USB IN endpoint | USB OUT endpoint |
|----------------|-----------------|------------------|
| [0]            | 0x88            | 0x08             |

Table 177: Isochronous endpoint numbering

An isochronous transaction consists of a single, non-acknowledged data stage. The host sends out a start of frame at a regular interval (1 ms), and data follows IN or OUT tokens within each frame.

EasyDMA allows transferring ISO data directly from and to memory. EasyDMA transfers must be initiated by the software, which can synchronize with the SOF (start of frame) events.

Because the timing of the start of frame is very accurate, the SOF event can be used for instance to synchronize a local timer through the SOF event and PPI. The SOF event gets synchronized to the 16 MHz clock prior to being made available to the PPI.

Every start of frame increments a free-running counter, which can be read by software through the [FRAMECNT](#) register.

Each IN or OUT ISO data endpoint has to be explicitly enabled by software through register [EPINEN](#) or [EPOUTEN](#), according to the configuration declared by the device and selected by the host through the **SetConfig** command. A disabled ISO IN data endpoint will not respond to any traffic from the host. A disabled ISO OUT data endpoint will ignore any incoming traffic from the host.

The USB peripheral has an internal 1 kB buffer associated with ISO endpoints. The user can either allocate the full amount to the IN or the OUT endpoint, or split the buffer allocation between the two using register [ISOSPLIT](#).

The internal buffer also sets the maximum size of the ISO OUT and ISO IN transfers: 1023 bytes when the full buffer is dedicated to either ISO OUT or ISO IN, and half when the buffer is split between the two.

#### 7.1.40.11.1 Isochronous IN transaction

When the host wants to receive isochronous (ISO) data, it issues an IN token on the isochronous endpoint.

After the data has been transferred using the EasyDMA, the USB controller on the isochronous IN endpoint responds to the IN token with the transferred data using the [ISOIN.MAXCNT](#) for the size of the packet.

The ISO IN data endpoint has to be explicitly enabled by software through the ISOIN0 bit in register [EPINEN](#).

When an ISO IN endpoint is enabled and no data transferred with EasyDMA, the response of the USB device depends on the setting of the RESPONSE field in register [ISOINCONFIG](#) - it can either provide no response to an IN token or respond with a zero-length data.

If the EasyDMA transfer on the isochronous endpoint is not completed before the next SOF event, the result of the transfer is undefined.

The maximum size of an ISO IN transfer in USB full-speed is 1023 bytes, and the data buffer has to be a multiple of 4 bytes 32-bit aligned in memory. However, the amount of bytes transferred on the USB data endpoint can be of any size (up to 1023 bytes, if not shared with an OUT ISO endpoint).

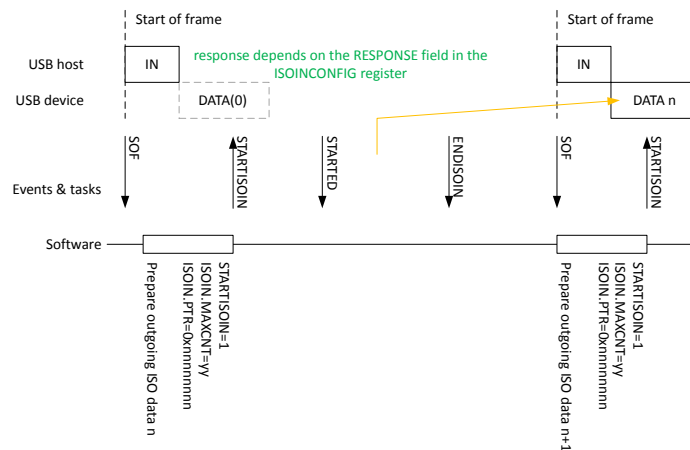


Figure 236: Isochronous IN transfer

#### 7.1.40.11.2 Isochronous OUT transaction

When the host wants to send isochronous (ISO) data, it issues an OUT token on the isochronous endpoint, followed by data.

The ISO OUT data endpoint has to be explicitly enabled by software through the ISOOUT0 bit in register [EPOUTEN](#).

The amount of last received ISO OUT data is provided in the [SIZE.ISOOUT](#) register. Software shall interpret the ZERO and SIZE fields as follows:

| ZERO     | SIZE              | Last received data size          |
|----------|-------------------|----------------------------------|
| Normal   | 0                 | No data received at all          |
| Normal   | 1..1023           | 1..1023 bytes of data received   |
| ZeroData | (not of interest) | Zero-length data packet received |

Table 178: ISO OUT incoming data size

When EasyDMA is prepared and started, triggering a STARTISOOUT task initiates an EasyDMA transfer to memory. Software shall synchronize ISO OUT transfers with the SOF events. EasyDMA uses the address in [ISOOUT.PTR](#) and size in [ISOOUT.MAXCNT](#) for every new transfer.

If the EasyDMA transfer on the isochronous endpoint is not completed before the next SOF event, the result of the transfer is undefined.

The maximum size of an isochronous OUT transfer in USB full-speed is 1023 bytes, and the data buffer has to be a multiple of 4 bytes and 32-bit aligned in Data RAM. However, the amount of bytes transferred on the USB data endpoint can be of any size (up to 1023 bytes if not shared with an IN ISO endpoint).

If the last received ISO data packet is corrupted (wrong CRC), the USB controller generates an USBEVENT event (at the same time as SOF) and indicates a CRC error on ISOOUTCRC in register [EVENTCAUSE](#). EasyDMA will transfer the data anyway if it has been set up properly.

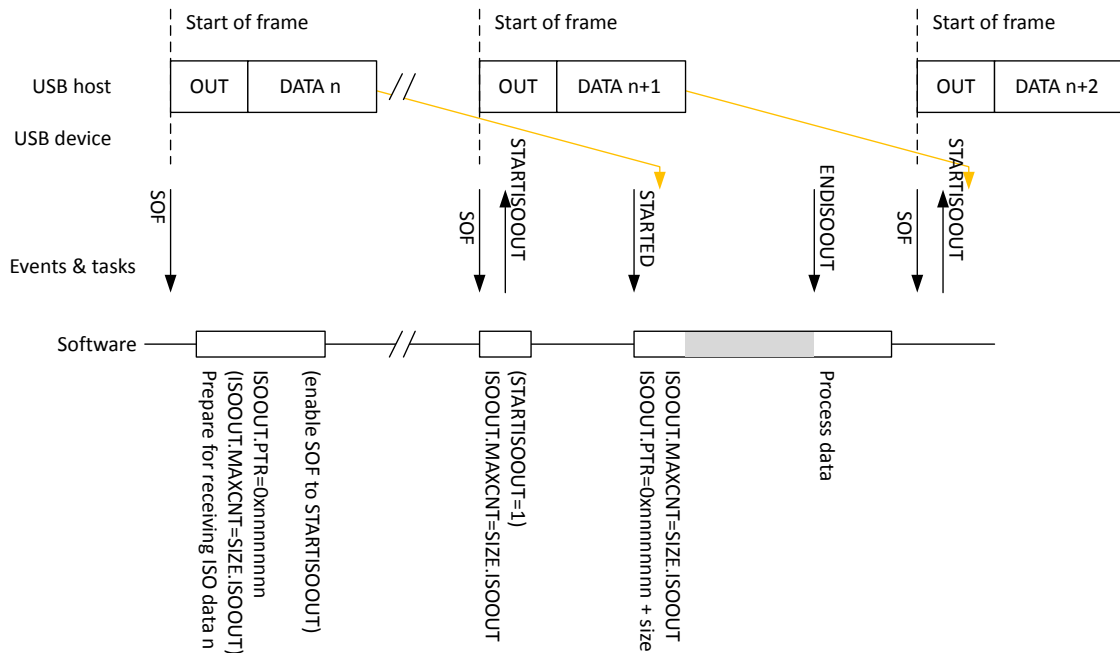


Figure 237: Isochronous OUT transfer

#### 7.1.40.12 USB register access limitations

Some of the registers in USBBD cannot be accessed in specific conditions.

This may be the case when USBBD is not enabled (using the [ENABLE](#) register) and ready (signalled by the READY bit in [EVENTCAUSE](#) after a USBEVENT event), or when USBBD is in low power mode while the USB bus is suspended.

Triggering any tasks, including the tasks triggered through the PPI, is affected by this behavior. In addition, the following registers are affected:

- HALTED.EPIN[0..7]
- HALTED.EPOUT[0..7]
- USBADDR
- BMREQUESTTYPE
- BREQUEST
- WVALUEL
- WVALUEH
- WINDEXL
- WINDEXH
- WLENGTHL
- WLENGTHH
- SIZE.EPOUT[0..7]
- SIZE.ISOOUT
- USBPULLUP
- DTOGGLE

- EPINEN
- EPOUTEN
- EPSTALL
- ISOSPLIT
- FRAMECNTR

### 7.1.40.13 Registers

| Base address | Domain      | Peripheral | Instance  | Secure mapping | DMA security | Description                 | Configuration |
|--------------|-------------|------------|-----------|----------------|--------------|-----------------------------|---------------|
| 0x50036000   | APPLICATION | USB0       | USB0 : S  | US             | SA           | Universal serial bus device |               |
| 0x40036000   |             |            | USB0 : NS |                |              |                             |               |

Table 179: Instances

| Register                | Offset | Security | Description                                                                                                                                                           |
|-------------------------|--------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TASKS_STARTEPIN[n]      | 0x004  |          | Captures the EPIN[n].PTR and EPIN[n].MAXCNT registers values, and enables endpoint IN n to respond to traffic from host                                               |
| TASKS_STARTISOIN        | 0x024  |          | Captures the ISOIN.PTR and ISOIN.MAXCNT registers values, and enables sending data on ISO endpoint                                                                    |
| TASKS_STARTEPOUT[n]     | 0x028  |          | Captures the EPOUT[n].PTR and EPOUT[n].MAXCNT registers values, and enables endpoint n to respond to traffic from host                                                |
| TASKS_STARTISOOOUT      | 0x048  |          | Captures the ISOOOUT.PTR and ISOOOUT.MAXCNT registers values, and enables receiving of data on ISO endpoint                                                           |
| TASKS_EPORCVOUT         | 0x04C  |          | Allows OUT data stage on control endpoint 0                                                                                                                           |
| TASKS_EPOSTATUS         | 0x050  |          | Allows status stage on control endpoint 0                                                                                                                             |
| TASKS_EPOSTALL          | 0x054  |          | Stalls data and status stage on control endpoint 0                                                                                                                    |
| TASKS_DPDMDRIVE         | 0x058  |          | Forces D+ and D- lines into the state defined in the DPDMVALUE register                                                                                               |
| TASKS_DPDMNODRIVE       | 0x05C  |          | Stops forcing D+ and D- lines into any state (USB engine takes control)                                                                                               |
| SUBSCRIBE_STARTEPIN[n]  | 0x084  |          | Subscribe configuration for task <a href="#">STARTEPIN[n]</a>                                                                                                         |
| SUBSCRIBE_STARTISOIN    | 0x0A4  |          | Subscribe configuration for task <a href="#">STARTISOIN</a>                                                                                                           |
| SUBSCRIBE_STARTEPOUT[n] | 0x0A8  |          | Subscribe configuration for task <a href="#">STARTEPOUT[n]</a>                                                                                                        |
| SUBSCRIBE_STARTISOOOUT  | 0x0C8  |          | Subscribe configuration for task <a href="#">STARTISOOOUT</a>                                                                                                         |
| SUBSCRIBE_EPORCVOUT     | 0x0CC  |          | Subscribe configuration for task <a href="#">EPORCVOUT</a>                                                                                                            |
| SUBSCRIBE_EPOSTATUS     | 0x0D0  |          | Subscribe configuration for task <a href="#">EPOSTATUS</a>                                                                                                            |
| SUBSCRIBE_EPOSTALL      | 0x0D4  |          | Subscribe configuration for task <a href="#">EPOSTALL</a>                                                                                                             |
| SUBSCRIBE_DPDMDRIVE     | 0x0D8  |          | Subscribe configuration for task <a href="#">DPDMDRIVE</a>                                                                                                            |
| SUBSCRIBE_DPDMNODRIVE   | 0x0DC  |          | Subscribe configuration for task <a href="#">DPDMNODRIVE</a>                                                                                                          |
| EVENTS_USBRESET         | 0x100  |          | Signals that a USB reset condition has been detected on USB lines                                                                                                     |
| EVENTS_STARTED          | 0x104  |          | Confirms that the EPIN[n].PTR and EPIN[n].MAXCNT, or EPOUT[n].PTR and EPOUT[n].MAXCNT registers have been captured on all endpoints reported in the EPSTATUS register |
| EVENTS_ENDEPIN[n]       | 0x108  |          | The whole EPIN[n] buffer has been consumed. The buffer can be accessed safely by software.                                                                            |
| EVENTS_EPODATADONE      | 0x128  |          | An acknowledged data transfer has taken place on the control endpoint                                                                                                 |
| EVENTS_ENDISOIN         | 0x12C  |          | The whole ISOIN buffer has been consumed. The buffer can be accessed safely by software.                                                                              |
| EVENTS_ENDEPOUT[n]      | 0x130  |          | The whole EPOUT[n] buffer has been consumed. The buffer can be accessed safely by software.                                                                           |
| EVENTS_ENDISOOOUT       | 0x150  |          | The whole ISOOOUT buffer has been consumed. The buffer can be accessed safely by software.                                                                            |
| EVENTS_SOF              | 0x154  |          | Signals that a SOF (start of frame) condition has been detected on USB lines                                                                                          |
| EVENTS_USBEVENT         | 0x158  |          | An event or an error not covered by specific events has occurred. Check EVENTCAUSE register to find the cause.                                                        |

| Register            | Offset | Security | Description                                                                                                                                    |
|---------------------|--------|----------|------------------------------------------------------------------------------------------------------------------------------------------------|
| EVENTS_EPOSETUP     | 0x15C  |          | A valid SETUP token has been received (and acknowledged) on the control endpoint                                                               |
| EVENTS_EPDATA       | 0x160  |          | A data transfer has occurred on a data endpoint, indicated by the EPDATASTATUS register                                                        |
| PUBLISH_USBRESET    | 0x180  |          | Publish configuration for event <b>USBRESET</b>                                                                                                |
| PUBLISH_STARTED     | 0x184  |          | Publish configuration for event <b>STARTED</b>                                                                                                 |
| PUBLISH_ENDEPIN[n]  | 0x188  |          | Publish configuration for event <b>ENDEPIN[n]</b>                                                                                              |
| PUBLISH_EP0DATADONE | 0x1A8  |          | Publish configuration for event <b>EP0DATADONE</b>                                                                                             |
| PUBLISH_ENDISOIN    | 0x1AC  |          | Publish configuration for event <b>ENDISOIN</b>                                                                                                |
| PUBLISH_ENDEPOUT[n] | 0x1B0  |          | Publish configuration for event <b>ENDEPOUT[n]</b>                                                                                             |
| PUBLISH_ENDISOOOUT  | 0x1D0  |          | Publish configuration for event <b>ENDISOOOUT</b>                                                                                              |
| PUBLISH_SOF         | 0x1D4  |          | Publish configuration for event <b>SOF</b>                                                                                                     |
| PUBLISH_USBEVENT    | 0x1D8  |          | Publish configuration for event <b>USBEVENT</b>                                                                                                |
| PUBLISH_EPOSETUP    | 0x1DC  |          | Publish configuration for event <b>EPOSETUP</b>                                                                                                |
| PUBLISH_EPDATA      | 0x1E0  |          | Publish configuration for event <b>EPDATA</b>                                                                                                  |
| SHORTS              | 0x200  |          | Shortcuts between local events and tasks                                                                                                       |
| INTEN               | 0x300  |          | Enable or disable interrupt                                                                                                                    |
| INTENSET            | 0x304  |          | Enable interrupt                                                                                                                               |
| INTENCLR            | 0x308  |          | Disable interrupt                                                                                                                              |
| EVENTCAUSE          | 0x400  |          | Details on what caused the USBEVENT event                                                                                                      |
| HALTED.EPIN[n]      | 0x420  |          | IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.                                                 |
| HALTED.EPOUT[n]     | 0x444  |          | OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.                                                |
| EPSTATUS            | 0x468  |          | Provides information on which endpoint's EasyDMA registers have been captured                                                                  |
| EPDATASTATUS        | 0x46C  |          | Provides information on which endpoint(s) an acknowledged data transfer has occurred (EPDATA event)                                            |
| USBADDR             | 0x470  |          | Device USB address                                                                                                                             |
| BMREQUESTTYPE       | 0x480  |          | SETUP data, byte 0, bmRequestType                                                                                                              |
| BREQUEST            | 0x484  |          | SETUP data, byte 1, bRequest                                                                                                                   |
| WVALUEL             | 0x488  |          | SETUP data, byte 2, LSB of wValue                                                                                                              |
| WVALUEH             | 0x48C  |          | SETUP data, byte 3, MSB of wValue                                                                                                              |
| WINDEXL             | 0x490  |          | SETUP data, byte 4, LSB of wIndex                                                                                                              |
| WINDEXH             | 0x494  |          | SETUP data, byte 5, MSB of wIndex                                                                                                              |
| WLENGTHL            | 0x498  |          | SETUP data, byte 6, LSB of wLength                                                                                                             |
| WLENGTHH            | 0x49C  |          | SETUP data, byte 7, MSB of wLength                                                                                                             |
| SIZE.EPOUT[n]       | 0x4A0  |          | Number of bytes received last in the data stage of this OUT endpoint                                                                           |
| SIZE.ISOOUT         | 0x4C0  |          | Number of bytes received last on this ISO OUT data endpoint                                                                                    |
| ENABLE              | 0x500  |          | Enable USB                                                                                                                                     |
| USBPULLUP           | 0x504  |          | Control of the USB pull-up                                                                                                                     |
| DPDMVALUE           | 0x508  |          | State D+ and D- lines will be forced into by the DPDMDRIVE task. The DPDMNODRIVE task reverts the control of the lines to MAC IP (no forcing). |
| DTOGGLE             | 0x50C  |          | Data toggle control and status                                                                                                                 |
| EPINEN              | 0x510  |          | Endpoint IN enable                                                                                                                             |
| EPOUTEN             | 0x514  |          | Endpoint OUT enable                                                                                                                            |
| EPSTALL             | 0x518  |          | STALL endpoints                                                                                                                                |
| ISOSPLIT            | 0x51C  |          | Controls the split of ISO buffers                                                                                                              |
| FRAMECNTR           | 0x520  |          | Returns the current value of the start of frame counter                                                                                        |
| LOWPOWER            | 0x52C  |          | Controls USB peripheral low power mode during USB suspend                                                                                      |
| ISOINCONFIG         | 0x530  |          | Controls the response of the ISO IN endpoint to an IN token when no data is ready to be sent                                                   |
| EPIN[n].PTR         | 0x600  |          | Data pointer                                                                                                                                   |
| EPIN[n].MAXCNT      | 0x604  |          | Maximum number of bytes to transfer                                                                                                            |



| Register        | Offset | Security | Description                                         |
|-----------------|--------|----------|-----------------------------------------------------|
| EPIN[n].AMOUNT  | 0x608  |          | Number of bytes transferred in the last transaction |
| ISOIN.PTR       | 0x6A0  |          | Data pointer                                        |
| ISOIN.MAXCNT    | 0x6A4  |          | Maximum number of bytes to transfer                 |
| ISOIN.AMOUNT    | 0x6A8  |          | Number of bytes transferred in the last transaction |
| EPOUT[n].PTR    | 0x700  |          | Data pointer                                        |
| EPOUT[n].MAXCNT | 0x704  |          | Maximum number of bytes to transfer                 |
| EPOUT[n].AMOUNT | 0x708  |          | Number of bytes transferred in the last transaction |
| ISOOUT.PTR      | 0x7A0  |          | Data pointer                                        |
| ISOOUT.MAXCNT   | 0x7A4  |          | Maximum number of bytes to transfer                 |
| ISOOUT.AMOUNT   | 0x7A8  |          | Number of bytes transferred in the last transaction |

Table 180: Register overview

### 7.1.40.13.1 TASKS\_STARTEPIN[n] (n=0..7)

Address offset:  $0x004 + (n \times 0x4)$

Captures the EPIN[n].PTR and EPIN[n].MAXCNT registers values, and enables endpoint IN n to respond to traffic from host

|                  |            |                 |       |                                                                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|-----------------|-------|-------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |                 |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |                 |       | A                                                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |                 |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID        | Value | Description                                                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W          | TASKS_STARTEPIN |       | Captures the EPIN[n].PTR and EPIN[n].MAXCNT registers values, and enables endpoint IN n to respond to traffic from host |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Trigger         | 1     | Trigger task                                                                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.40.13.2 TASKS\_STARTISOIN

Address offset: 0x024

Captures the ISOIN.PTR and ISOIN.MAXCNT registers values, and enables sending data on ISO endpoint

|                  |            |                  |                                                                                       |                                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|------------------|---------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |                  | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |                  | A                                                                                     |                                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |                  | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0           |                                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID         | Value                                                                                 | Description                                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W          | TASKS_STARTISOIN |                                                                                       | Captures the ISOIN.PTR and ISOIN.MAXCNT registers values,<br>and enables sending data on ISO endpoint |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Trigger          | 1                                                                                     | Trigger task                                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.40.13.3 TASKS\_STARTEPOUT[n] (n=0..7)

Address offset:  $0x028 + (n \times 0x4)$

Captures the EPOUT[n].PTR and EPOUT[n].MAXCNT registers values, and enables endpoint n to respond to traffic from host



|                  |            |                |          |   |       |              |             |                                                    |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------------|----------|---|-------|--------------|-------------|----------------------------------------------------|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                |          |   |       |              |             |                                                    |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |                |          |   |       |              |             |                                                    |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |   |
| Reset 0x00000000 |            |                |          |   |       |              |             |                                                    |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |                | Value ID |   | Value |              | Description |                                                    |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TASKS_EPOSTALL |          |   |       |              |             | Stalls data and status stage on control endpoint 0 |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Trigger        |          | 1 |       | Trigger task |             |                                                    |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.40.13.8 TASKS\_DPDMDRIVE

Address offset: 0x058

Forces D+ and D- lines into the state defined in the DPDMVALUE register

|                  |            |                 |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|-----------------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |                 |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |                 |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |                 |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID        | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W          | TASKS_DPDMDRIVE |       | Forces D+ and D- lines into the state defined in the DPDMVALUE register               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Trigger         | 1     | Trigger task                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.40.13.9 TASKS\_DPDMNODRIVE

Address offset: 0x05C

Stops forcing D+ and D- lines into any state (USB engine takes control)

|                  |      |                   |         |    |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|-------------------|---------|----|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|-------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |                   |         | 31 | 30    | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |                   |         |    |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |                   |         | 0  | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field             | Value   | ID | Value |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   | Description                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W    | TASKS_DPDMNODRIVE |         |    |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   | Stops forcing D+ and D- lines into any state (USB engine takes control) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                   | Trigger | 1  |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   | Trigger task                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.40.13.10 SUBSCRIBE\_STARTEPIN[n] (n=0..7)

Address offset: 0x084 + (n × 0x4)

Subscribe configuration for task [STARTEPIN\[n\]](#)

|                  |            |          |  |          |    |                      |    |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|--|----------|----|----------------------|----|------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |  | 31       | 30 | 29                   | 28 | 27                                                               | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |          |  | B        |    |                      |    |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |          |  | 0        |    |                      |    |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |          |  | Value ID |    | Value                |    | Description                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | CHIDX    |  |          |    | [255..0]             |    | Channel that task <a href="#">STARTEPIN[n]</a> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW         | EN       |  |          |    |                      |    |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled |  | 0        |    | Disable subscription |    |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  |  | 1        |    | Enable subscription  |    |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.40.13.11 SUBSCRIBE\_STARTISOIN

Address offset: 0x0A4

Subscribe configuration for task [STARTISOIN](#)

|                  |            |  |          |          |    |                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|----------|----|----------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31       | 30 | 29                                                             | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |  |          | B        |    |                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |          | 0        | 0  | 0                                                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |
| ID               | Acce Field |  | Value ID | Value    |    | Description                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          | [255..0] |    | Channel that task <a href="#">STARTISOIN</a> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |          |    |                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled | 0        |    | Disable subscription                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  | 1        |    | Enable subscription                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.40.13.12 SUBSCRIBE\_STARTEPOUT[n] (n=0..7)

Address offset: 0x0A8 + (n × 0x4)

Subscribe configuration for task [STARTEPOUT\[n\]](#)

|                  |            |  |          |  |          |  |                                                                   |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|--|----------|--|-------------------------------------------------------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          |  |          |  |                                                                   |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |
| ID               |            |  |          |  |          |  |                                                                   |  |  | B  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  |    |    |    |   |   |   |   |   |   | A | A | A | A | A | A | A |   |
| Reset 0x00000000 |            |  |          |  |          |  |                                                                   |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID |  | Value    |  | Description                                                       |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          |  | [255..0] |  | Channel that task <a href="#">STARTEPOUT[n]</a> will subscribe to |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |  |          |  |                                                                   |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled |  | 0        |  | Disable subscription                                              |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  |  | 1        |  | Enable subscription                                               |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.40.13.13 SUBSCRIBE\_STARTISOOUT

Address offset: 0x0C8

Subscribe configuration for task [STARTISOOUT](#)

|                  |            |          |          |                                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|-------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                                                                      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |          |          | B                                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field | Value ID | Value    | Description                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] | Channel that task <a href="#">STARTISOOUT</a> will subscribe to         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |                                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        | Disable subscription                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        | Enable subscription                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.40.13.14 SUBSCRIBE\_EPORCVOUT

Address offset: 0x0CC

Subscribe configuration for task [EPORCVOUT](#)

|                  |            |  |          |  |          |  |                                                               |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|--|----------|--|---------------------------------------------------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          |  |          |  |                                                               |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |  |          |  |          |  |                                                               |  |  | B  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  |    |    |    |   |   |   |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |  |          |  |          |  |                                                               |  |  | 0  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID |  | Value    |  | Description                                                   |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          |  | [255..0] |  | Channel that task <a href="#">EPORCVOUT</a> will subscribe to |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |  |          |  |                                                               |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled |  | 0        |  | Disable subscription                                          |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  |  | 1        |  | Enable subscription                                           |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.40.13.15 SUBSCRIBE\_EPOSTATUS

Address offset: 0x0D0

Subscribe configuration for task [EPOSTATUS](#)

|                  |            |          |                                                                                       |  |  |  |                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|--|--|--|------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |          | B                                                                                     |  |  |  |                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                   |  |  |  |                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 |  |  |  | Description                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                              |  |  |  | Channel that task <span>EPOSTATUS</span> will subscribe to |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |                                                                                       |  |  |  |                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     |  |  |  | Disable subscription                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     |  |  |  | Enable subscription                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

### 7.1.40.13.16 SUBSCRIBE\_EPOSTALL

Address offset: 0x0D4

Subscribe configuration for task [EPOSTALL](#)

|                  |            |          |                                                                                       |                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|-----------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |          | B                                                                                     |                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                              | Channel that task <span>EPOSTALL</span> will subscribe to |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |                                                                                       |                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Disable subscription                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Enable subscription                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

### 7.1.40.13.17 SUBSCRIBE\_DPDMDRIVE

Address offset: 0x0D8

Subscribe configuration for task [DPDMDRIVE](#)

|                  |            |          |                                                                                       |                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |          | B                                                                                     |                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | RW CHIDX   |          | [255..0]                                                                              | Channel that task <b>DPDMDRIVE</b> will subscribe to |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | RW EN      |          |                                                                                       |                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Disable subscription                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Enable subscription                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

### 7.1.40.13.18 SUBSCRIBE\_DPDMNODRIVE

Address offset: 0x0DC

Subscribe configuration for task [DPDMNODRIVE](#)

|                  |            |  |          |          |    |                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|----------|----|-----------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31       | 30 | 29                                                              | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |  |          | B        |    |                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |          | 0        | 0  | 0                                                               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce Field |  | Value ID | Value    |    | Description                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          | [255..0] |    | Channel that task <a href="#">DPDMNODRIVE</a> will subscribe to |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |          |    |                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled | 0        |    | Disable subscription                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  | 1        |    | Enable subscription                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.40.13.19 EVENTS\_USBRESET

Address offset: 0x100

Signals that a USB reset condition has been detected on USB lines

|                  |            |  |                 |  |              |   |                                                                   |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|-----------------|--|--------------|---|-------------------------------------------------------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |                 |  |              |   |                                                                   |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |  |                 |  |              |   |                                                                   |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |   |
| Reset 0x00000000 |            |  |                 |  |              |   |                                                                   |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID        |  | Value        |   | Description                                                       |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         |  | EVENTS_USBRESET |  |              |   | Signals that a USB reset condition has been detected on USB lines |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  |                 |  | NotGenerated | 0 | Event not generated                                               |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  |                 |  | Generated    | 1 | Event generated                                                   |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.40.13.20 EVENTS\_STARTED

Address offset: 0x104

Confirms that the EPIN[n].PTR and EPIN[n].MAXCNT, or EPOUT[n].PTR and EPOUT[n].MAXCNT registers have been captured on all endpoints reported in the EPSTATUS register

|                  |            |                |       |    |                                                                                                                                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |  |
|------------------|------------|----------------|-------|----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|---|--|
| Bit number       |            |                | 31    | 30 | 29                                                                                                                                                                    | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |   |  |
| ID               |            |                |       |    |                                                                                                                                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | A |  |
| Reset 0x00000000 |            |                | 0     | 0  | 0                                                                                                                                                                     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |   |  |
| ID               | Acce Field | Value ID       | Value |    | Description                                                                                                                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |  |
| A                | RW         | EVENTS_STARTED |       |    | Confirms that the EPIN[n].PTR and EPIN[n].MAXCNT, or EPOUT[n].PTR and EPOUT[n].MAXCNT registers have been captured on all endpoints reported in the EPSTATUS register |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |  |
|                  |            | NotGenerated   | 0     |    | Event not generated                                                                                                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |  |
|                  |            | Generated      | 1     |    | Event generated                                                                                                                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |  |

### 7.1.40.13.21 EVENTS\_ENDEPIN[n] (n=0..7)

Address offset: 0x108 + (n × 0x4)

The whole EPIN[n] buffer has been consumed. The buffer can be accessed safely by software.

|                  |            |                |       |                                                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------------|-------|--------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                | 31    | 30                                                                                         | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |                | A     |                                                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |                | 0     | 0                                                                                          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID       | Value | Description                                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | EVENTS_ENDEPIN |       | The whole EPIN[n] buffer has been consumed. The buffer can be accessed safely by software. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | NotGenerated   | 0     | Event not generated                                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Generated      | 1     | Event generated                                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 7.1.40.13.22 EVENTS\_EP0DATADONE

Address offset: 0x128

An acknowledged data transfer has taken place on the control endpoint

|                  |            |  |                    |  |       |  |                                                                       |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|--------------------|--|-------|--|-----------------------------------------------------------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |                    |  |       |  |                                                                       |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |  |                    |  |       |  |                                                                       |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |   |
| Reset 0x00000000 |            |  |                    |  |       |  |                                                                       |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID           |  | Value |  | Description                                                           |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         |  | EVENTS_EP0DATADONE |  |       |  | An acknowledged data transfer has taken place on the control endpoint |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | NotGenerated       |  | 0     |  | Event not generated                                                   |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Generated          |  | 1     |  | Event generated                                                       |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.40.13.23 EVENTS\_ENDISOIN

Address offset: 0x12C

The whole ISOIN buffer has been consumed. The buffer can be accessed safely by software.

|                  |            |                 |       |                                                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-----------------|-------|------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                 |       | 31                                                                                       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |                 |       | A                                                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |                 |       | 0                                                                                        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID        | Value | Description                                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | EVENTS_ENDISOIN |       | The whole ISOIN buffer has been consumed. The buffer can be accessed safely by software. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | NotGenerated    | 0     | Event not generated                                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Generated       | 1     | Event generated                                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.40.13.24 EVENTS\_ENDEPOUT[n] (n=0..7)

Address offset: 0x130 + (n × 0x4)

The whole EPOUT[n] buffer has been consumed. The buffer can be accessed safely by software.

|                  |            |                 |       |                                                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|------------------|------------|-----------------|-------|---------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|--|
| Bit number       |            |                 | 31    | 30                                                                                          | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |
| ID               |            |                 | A     |                                                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| Reset 0x00000000 |            |                 | 0     | 0                                                                                           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |  |
| ID               | Acce Field | Value ID        | Value | Description                                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| A                | RW         | EVENTS_ENDEPOUT |       | The whole EPOUT[n] buffer has been consumed. The buffer can be accessed safely by software. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | NotGenerated    | 0     | Event not generated                                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | Generated       | 1     | Event generated                                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |

### 7.1.40.13.25 EVENTS\_ENDISOOUT

Address offset: 0x150

The whole ISOOUT buffer has been consumed. The buffer can be accessed safely by software.

|                  |      |                  |              |    |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   |                                                                                           |
|------------------|------|------------------|--------------|----|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|---|-------------------------------------------------------------------------------------------|
| Bit number       |      |                  |              | 31 | 30    | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |   |                                                                                           |
| ID               |      |                  |              |    |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  | A |                                                                                           |
| Reset 0x00000000 |      |                  |              | 0  | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |   |                                                                                           |
| ID               | Acce | Field            | Value        | ID | Value |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   | Description                                                                               |
| A                | RW   | EVENTS_ENDISOOUT |              |    |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   | The whole ISOOUT buffer has been consumed. The buffer can be accessed safely by software. |
|                  |      |                  | NotGenerated | 0  |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   | Event not generated                                                                       |
|                  |      |                  | Generated    | 1  |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |   | Event generated                                                                           |

### 7.1.40.13.26 EVENTS\_SOF

Address offset: 0x154

Signals that a SOF (start of frame) condition has been detected on USB lines

|                  |            |              |       |                                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|------------------|------------|--------------|-------|------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|--|
| Bit number       |            |              | 31    | 30                                                                           | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |
| ID               |            |              | A     |                                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| Reset 0x00000000 |            |              | 0     | 0                                                                            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |  |
| ID               | Acce Field | Value ID     | Value | Description                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| A                | RW         | EVENTS_SOF   |       | Signals that a SOF (start of frame) condition has been detected on USB lines |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | NotGenerated | 0     | Event not generated                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | Generated    | 1     | Event generated                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |

### 7.1.40.13.27 EVENTS\_USBEVENT

Address offset: 0x158

An event or an error not covered by specific events has occurred. Check EVENTCAUSE register to find the cause.

|                  |            |                 |       |    |                                                                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |
|------------------|------------|-----------------|-------|----|----------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|--|--|
| Bit number       |            |                 | 31    | 30 | 29                                                                                                             | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |  |
| ID               |            |                 | A     |    |                                                                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |
| Reset 0x00000000 |            |                 | 0     | 0  | 0                                                                                                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |  |  |
| ID               | Acce Field | Value ID        | Value |    | Description                                                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |
| A                | RW         | EVENTS_USBEVENT |       |    | An event or an error not covered by specific events has occurred. Check EVENTCAUSE register to find the cause. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |
|                  |            | NotGenerated    | 0     |    | Event not generated                                                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |
|                  |            | Generated       | 1     |    | Event generated                                                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |

### 7.1.40.13.28 EVENTS\_EPOSETUP

Address offset: 0x15C

A valid SETUP token has been received (and acknowledged) on the control endpoint



|                  |            |                 |       |                                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-----------------|-------|----------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                 |       | 31                                                                               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |                 |       | A                                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |                 |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field | Value ID        | Value | Description                                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | EVENTS_EP0SETUP |       | A valid SETUP token has been received (and acknowledged) on the control endpoint |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | NotGenerated    | 0     | Event not generated                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | Generated       | 1     | Event generated                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.40.13.29 EVENTS\_EPDATA

Address offset: 0x160

A data transfer has occurred on a data endpoint, indicated by the EPDATASTATUS register

|                  |            |  |               |  |       |  |                                                                                         |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|---------------|--|-------|--|-----------------------------------------------------------------------------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |               |  |       |  |                                                                                         |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |  |               |  |       |  |                                                                                         |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |
| Reset 0x00000000 |            |  |               |  |       |  |                                                                                         |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID      |  | Value |  | Description                                                                             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         |  | EVENTS_EPDATA |  |       |  | A data transfer has occurred on a data endpoint, indicated by the EPDATASTATUS register |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | NotGenerated  |  | 0     |  | Event not generated                                                                     |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Generated     |  | 1     |  | Event generated                                                                         |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.40.13.30 PUBLISH\_USBRESET

Address offset: 0x180

Publish configuration for event USBRESET

|                  |            |  |          |                                                                             |    |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|-----------------------------------------------------------------------------|----|-----------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31                                                                          | 30 | 29                                                  | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |  |          | B                                                                           |    |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |    |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field |  | Value ID | Value                                                                       |    | Description                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          | [255..0]                                                                    |    | Channel that event <b>USBRESET</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |                                                                             |    |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled | 0                                                                           |    | Disable publishing                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  | 1                                                                           |    | Enable publishing                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.40.13.31 PUBLISH\_STARTED

Address offset: 0x184

Publish configuration for event STARTED

|                  |            |       |          |                                                                         |    |    |    |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
|------------------|------------|-------|----------|-------------------------------------------------------------------------|----|----|----|----------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|-----------------|---|---|---|---|---|---|---|--|--|--|--|
| Bit number       |            |       |          | 31                                                                      | 30 | 29 | 28 | 27                                                 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |
| ID               |            |       |          | B                                                                       |    |    |    |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A A A A A A A A |   |   |   |   |   |   |   |  |  |  |  |
| Reset 0x00000000 |            |       |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |    |    |    |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
| ID               | Acce Field |       | Value ID | Value                                                                   |    |    |    | Description                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
| A                | RW         | CHIDX |          | [255..0]                                                                |    |    |    | Channel that event <b>STARTED</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
| B                | RW         | EN    |          |                                                                         |    |    |    |                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
|                  |            |       | Disabled | 0                                                                       |    |    |    | Disable publishing                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |
|                  |            |       | Enabled  | 1                                                                       |    |    |    | Enable publishing                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                 |   |   |   |   |   |   |   |  |  |  |  |



|                  |            |          |          |                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|-------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31                                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |          |          | B                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |          | 0                                               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce Field | Value ID | Value    | Description                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |          | [255..0] | Channel that event ENDEPOUT[n] will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |          |          |                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled | 0        | Disable publishing                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  | 1        | Enable publishing                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.40.13.36 PUBLISH\_ENDISOOUT

Address offset: 0x1D0

Publish configuration for event **ENDISOOUT**

|                  |            |  |          |  |          |  |                                                      |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|--|----------|--|------------------------------------------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          |  |          |  |                                                      |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |  |          |  |          |  |                                                      |  |  | B  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  |    |    |    |   |   |   |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |          |  |          |  |                                                      |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID |  | Value    |  | Description                                          |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          |  | [255..0] |  | Channel that event <b>ENDISOOUT</b> will publish to. |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |  |          |  |                                                      |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled |  | 0        |  | Disable publishing                                   |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  |  | 1        |  | Enable publishing                                    |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.40.13.37 PUBLISH\_SOF

Address offset: 0x1D4

Publish configuration for event **SOF**

|                  |            |  |          |          |                    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|----------|--------------------|------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31       | 30                 | 29                                                   | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |  |          | B        |                    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |          | 0        | 0                  | 0                                                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce Field |  | Value ID | Value    |                    | Description                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW CHIDX   |  |          | [255..0] |                    | Channel that event <span>SOF</span> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW EN      |  |          |          |                    |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Disabled | 0        | Disable publishing |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |  | Enabled  | 1        | Enable publishing  |                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.40.13.38 PUBLISH\_USBEVENT

Address offset: 0x1D8

Publish configuration for event **USBEVENT**

|                  |            |       |          |          |                    |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-------|----------|----------|--------------------|-----------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |       |          | 31       | 30                 | 29                                                  | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |       |          | B        |                    |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   |   |   |   | A | A | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |       |          | 0        |                    |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |       | Value ID | Value    |                    | Description                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | CHIDX |          | [255..0] |                    | Channel that event <b>USBEVENT</b> will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW         | EN    |          |          |                    |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |       | Disabled | 0        | Disable publishing |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |       | Enabled  | 1        | Enable publishing  |                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |



Address offset: 0x300

Enable or disable interrupt

### 7.1.40.13.43 INTENSET

4406\_456 v0.5

|                  |            |                      |          |                                                                         |                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------------------|----------|-------------------------------------------------------------------------|---------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                      |          | 31                                                                      | 30                                                                  | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |                      |          | Y X W V U T S R Q P O N M L K J I H G F E D C B A                       |                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |                      |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field |                      | Value ID | Value                                                                   | Description                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | USBRESET             |          |                                                                         | Write '1' to enable interrupt for event <a href="#">USBRESET</a>    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |                      | Set      | 1                                                                       | Enable                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |                      | Disabled | 0                                                                       | Read: Disabled                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |                      | Enabled  | 1                                                                       | Read: Enabled                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| B                | RW         | STARTED              |          |                                                                         | Write '1' to enable interrupt for event <a href="#">STARTED</a>     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |                      | Set      | 1                                                                       | Enable                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |                      | Disabled | 0                                                                       | Read: Disabled                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |                      | Enabled  | 1                                                                       | Read: Enabled                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| C-J              | RW         | ENDEPIN[i] (i=0..7)  |          |                                                                         | Write '1' to enable interrupt for event <a href="#">ENDEPIN[i]</a>  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |                      | Set      | 1                                                                       | Enable                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |                      | Disabled | 0                                                                       | Read: Disabled                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |                      | Enabled  | 1                                                                       | Read: Enabled                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| K                | RW         | EPODATADONE          |          |                                                                         | Write '1' to enable interrupt for event <a href="#">EPODATADONE</a> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |                      | Set      | 1                                                                       | Enable                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |                      | Disabled | 0                                                                       | Read: Disabled                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |                      | Enabled  | 1                                                                       | Read: Enabled                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| L                | RW         | ENDISOIN             |          |                                                                         | Write '1' to enable interrupt for event <a href="#">ENDISOIN</a>    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |                      | Set      | 1                                                                       | Enable                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |                      | Disabled | 0                                                                       | Read: Disabled                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |                      | Enabled  | 1                                                                       | Read: Enabled                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| M-T              | RW         | ENDEPOUT[i] (i=0..7) |          |                                                                         | Write '1' to enable interrupt for event <a href="#">ENDEPOUT[i]</a> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |                      | Set      | 1                                                                       | Enable                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |                      | Disabled | 0                                                                       | Read: Disabled                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |                      | Enabled  | 1                                                                       | Read: Enabled                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| U                | RW         | ENDISOOOT            |          |                                                                         | Write '1' to enable interrupt for event <a href="#">ENDISOOOT</a>   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |                      | Set      | 1                                                                       | Enable                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |                      | Disabled | 0                                                                       | Read: Disabled                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |                      | Enabled  | 1                                                                       | Read: Enabled                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| V                | RW         | SOF                  |          |                                                                         | Write '1' to enable interrupt for event <a href="#">SOF</a>         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |                      | Set      | 1                                                                       | Enable                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |                      | Disabled | 0                                                                       | Read: Disabled                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |                      | Enabled  | 1                                                                       | Read: Enabled                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| W                | RW         | USBEVENT             |          |                                                                         | Write '1' to enable interrupt for event <a href="#">USBEVENT</a>    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |                      | Set      | 1                                                                       | Enable                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |                      | Disabled | 0                                                                       | Read: Disabled                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |                      | Enabled  | 1                                                                       | Read: Enabled                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| X                | RW         | EPOSETUP             |          |                                                                         | Write '1' to enable interrupt for event <a href="#">EPOSETUP</a>    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |                      | Set      | 1                                                                       | Enable                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |                      | Disabled | 0                                                                       | Read: Disabled                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |                      | Enabled  | 1                                                                       | Read: Enabled                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Y                | RW         | EPDATA               |          |                                                                         | Write '1' to enable interrupt for event <a href="#">EPDATA</a>      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |                      | Set      | 1                                                                       | Enable                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |                      | Disabled | 0                                                                       | Read: Disabled                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |                      | Enabled  | 1                                                                       | Read: Enabled                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 7.1.40.13.44 INTENCLR

Address offset: 0x308

|                  |      |                      |          |                                                                         |                                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|------------------|------|----------------------|----------|-------------------------------------------------------------------------|----------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| Bit number       |      |                      |          | 31                                                                      | 30                                                                   | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| ID               |      |                      |          | Y X W V U T S R Q P O N M L K J I H G F E D C B A                       |                                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| Reset 0x00000000 |      |                      |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |                                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| ID               | Acce | Field                | Value ID | Value                                                                   | Description                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| A                | RW   | USBRESET             |          |                                                                         | Write '1' to disable interrupt for event <a href="#">USBRESET</a>    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                      | Clear    | 1                                                                       | Disable                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                      | Disabled | 0                                                                       | Read: Disabled                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                      | Enabled  | 1                                                                       | Read: Enabled                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| B                | RW   | STARTED              |          |                                                                         | Write '1' to disable interrupt for event <a href="#">STARTED</a>     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                      | Clear    | 1                                                                       | Disable                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                      | Disabled | 0                                                                       | Read: Disabled                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                      | Enabled  | 1                                                                       | Read: Enabled                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| C-J              | RW   | ENDEPIN[i] (i=0..7)  |          |                                                                         | Write '1' to disable interrupt for event <a href="#">ENDEPIN[i]</a>  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                      | Clear    | 1                                                                       | Disable                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                      | Disabled | 0                                                                       | Read: Disabled                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                      | Enabled  | 1                                                                       | Read: Enabled                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| K                | RW   | EPODATADONE          |          |                                                                         | Write '1' to disable interrupt for event <a href="#">EPODATADONE</a> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                      | Clear    | 1                                                                       | Disable                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                      | Disabled | 0                                                                       | Read: Disabled                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                      | Enabled  | 1                                                                       | Read: Enabled                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| L                | RW   | ENDISOIN             |          |                                                                         | Write '1' to disable interrupt for event <a href="#">ENDISOIN</a>    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                      | Clear    | 1                                                                       | Disable                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                      | Disabled | 0                                                                       | Read: Disabled                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                      | Enabled  | 1                                                                       | Read: Enabled                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| M-T              | RW   | ENDEPOUT[i] (i=0..7) |          |                                                                         | Write '1' to disable interrupt for event <a href="#">ENDEPOUT[i]</a> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                      | Clear    | 1                                                                       | Disable                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                      | Disabled | 0                                                                       | Read: Disabled                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                      | Enabled  | 1                                                                       | Read: Enabled                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| U                | RW   | ENDISOOUT            |          |                                                                         | Write '1' to disable interrupt for event <a href="#">ENDISOOUT</a>   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                      | Clear    | 1                                                                       | Disable                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                      | Disabled | 0                                                                       | Read: Disabled                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                      | Enabled  | 1                                                                       | Read: Enabled                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| V                | RW   | SOF                  |          |                                                                         | Write '1' to disable interrupt for event <a href="#">SOF</a>         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                      | Clear    | 1                                                                       | Disable                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                      | Disabled | 0                                                                       | Read: Disabled                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                      | Enabled  | 1                                                                       | Read: Enabled                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| W                | RW   | USBEVENT             |          |                                                                         | Write '1' to disable interrupt for event <a href="#">USBEVENT</a>    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                      | Clear    | 1                                                                       | Disable                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                      | Disabled | 0                                                                       | Read: Disabled                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                      | Enabled  | 1                                                                       | Read: Enabled                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| X                | RW   | EPOSETUP             |          |                                                                         | Write '1' to disable interrupt for event <a href="#">EPOSETUP</a>    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                      | Clear    | 1                                                                       | Disable                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                      | Disabled | 0                                                                       | Read: Disabled                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                      | Enabled  | 1                                                                       | Read: Enabled                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| Y                | RW   | EPDATA               |          |                                                                         | Write '1' to disable interrupt for event <a href="#">EPDATA</a>      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                      | Clear    | 1                                                                       | Disable                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                      | Disabled | 0                                                                       | Read: Disabled                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |                      | Enabled  | 1                                                                       | Read: Enabled                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

### 7.1.40.13.45 EVENTCAUSE

Address offset: 0x400

## Details on what caused the USBEVENT event

| Bit number       |      |              | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |         |  |  |  |   |
|------------------|------|--------------|---------------------------------------------------------------------------------------|-------|-------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---------|--|--|--|---|
| ID               |      |              |                                                                                       |       |                                                                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | E D C B |  |  |  | A |
| Reset 0x00000000 |      |              | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |       |                                                                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |         |  |  |  |   |
| ID               | Acce | Field        | Value ID                                                                              | Value | Description                                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |         |  |  |  |   |
| A                | RW   | ISOOUTCRC    |                                                                                       |       | CRC error was detected on isochronous OUT endpoint 8.<br>Write '1' to clear.                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |         |  |  |  |   |
|                  |      |              | NotDetected                                                                           | 0     | No error detected                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |         |  |  |  |   |
|                  |      |              | Detected                                                                              | 1     | Error detected                                                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |         |  |  |  |   |
| B                | RW   | SUSPEND      |                                                                                       |       | Signals that USB lines have been idle long enough for the device to enter suspend. Write '1' to clear.            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |         |  |  |  |   |
|                  |      |              | NotDetected                                                                           | 0     | Suspend not detected                                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |         |  |  |  |   |
|                  |      |              | Detected                                                                              | 1     | Suspend detected                                                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |         |  |  |  |   |
| C                | RW   | RESUME       |                                                                                       |       | Signals that a RESUME condition (K state or activity restart) has been detected on USB lines. Write '1' to clear. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |         |  |  |  |   |
|                  |      |              | NotDetected                                                                           | 0     | Resume not detected                                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |         |  |  |  |   |
|                  |      |              | Detected                                                                              | 1     | Resume detected                                                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |         |  |  |  |   |
| D                | RW   | USBWUALLOWED |                                                                                       |       | USB MAC has been woken up and operational. Write '1' to clear.                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |         |  |  |  |   |
|                  |      |              | NotAllowed                                                                            | 0     | Wake up not allowed                                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |         |  |  |  |   |
|                  |      |              | Allowed                                                                               | 1     | Wake up allowed                                                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |         |  |  |  |   |
| E                | RW   | READY        |                                                                                       |       | USB device is ready for normal operation. Write '1' to clear.                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |         |  |  |  |   |
|                  |      |              | NotDetected                                                                           | 0     | USBEVENT was not issued due to USB peripheral ready                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |         |  |  |  |   |
|                  |      |              | Ready                                                                                 | 1     | USB peripheral is ready                                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |         |  |  |  |   |

## 7.1.40.13.46 HALTED.EPIN[n] (n=0..7)

Address offset: 0x420 + (n × 0x4)

IN endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.

|                  |            |           |           |                                                                                                   |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|-----------|-----------|---------------------------------------------------------------------------------------------------|------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |           |           | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0             |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |           |           |                                                                                                   |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A A A A A A A A A |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |           |           | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                                   |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID  | Value     | Description                                                                                       |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | R          | GETSTATUS |           | IN endpoint halted status. Can be used as is as response to a<br>GetStatus() request to endpoint. |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |           | NotHalted | 0                                                                                                 | Endpoint is not halted |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |           | Halted    | 1                                                                                                 | Endpoint is halted     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

## 7.1.40.13.47 HALTED.EPOUT[n] (n=0..7)

Address offset: 0x444 + (n × 0x4)

OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint.



|                  |      |           |           |       |                                                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |
|------------------|------|-----------|-----------|-------|-------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|--|
| Bit number       |      |           |           | 31    | 30                                                                                              | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |  |
| ID               |      |           |           |       |                                                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A | A | A |  |
| Reset 0x00000000 |      |           |           | 0     | 0                                                                                               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |  |
| ID               | Acce | Field     | Value ID  | Value | Description                                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |
| A                | R    | GETSTATUS |           |       | OUT endpoint halted status. Can be used as is as response to a GetStatus() request to endpoint. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |           | NotHalted | 0     | Endpoint is not halted                                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |           | Halted    | 1     | Endpoint is halted                                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |  |

### 7.1.40.13.48 EPSTATUS

Address offset: 0x468

Provides information on which endpoint's EasyDMA registers have been captured

| Bit number       |      |                   | 31                | 30    | 29                                                                  | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |
|------------------|------|-------------------|-------------------|-------|---------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|--|
| ID               |      |                   | R Q P O N M L K J |       |                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    | I H G F E D C B A |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| Reset 0x00000000 |      |                   | 0                 | 0     | 0                                                                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |  |
| ID               | Acce | Field             | Value ID          | Value | Description                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |                   |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| A-I              | RW   | EPIN[i] (i=0..8)  |                   |       | Captured state of endpoint's EasyDMA registers. Write '1' to clear. |    |    |    |    |    |    |    |    |    |    |    |    |    |                   |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |      |                   | NoData            | 0     | EasyDMA registers have not been captured for this endpoint          |    |    |    |    |    |    |    |    |    |    |    |    |    |                   |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |      |                   | DataDone          | 1     | EasyDMA registers have been captured for this endpoint              |    |    |    |    |    |    |    |    |    |    |    |    |    |                   |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| J-R              | RW   | EPOUT[i] (i=0..8) |                   |       | Captured state of endpoint's EasyDMA registers. Write '1' to clear. |    |    |    |    |    |    |    |    |    |    |    |    |    |                   |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |      |                   | NoData            | 0     | EasyDMA registers have not been captured for this endpoint          |    |    |    |    |    |    |    |    |    |    |    |    |    |                   |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |      |                   | DataDone          | 1     | EasyDMA registers have been captured for this endpoint              |    |    |    |    |    |    |    |    |    |    |    |    |    |                   |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |

### 7.1.40.13.49 EPDATASTATUS

Address offset: 0x46C

Provides information on which endpoint(s) an acknowledged data transfer has occurred (EPDATA event)

| Bit number       |            |                   | 31            | 30                                                                   | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15            | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
|------------------|------------|-------------------|---------------|----------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| ID               |            |                   | N M L K J I H |                                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    | G F E D C B A |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| Reset 0x00000000 |            |                   | 0             | 0                                                                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |
| ID               | Acce Field | Value ID          | Value         | Description                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |               |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| A-G              | RW         | EPIN[i] (i=1..7)  |               | Acknowledged data transfer on this IN endpoint. Write '1' to clear.  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |               |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | NotDone           | 0             | No acknowledged data transfer on this endpoint                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |               |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | DataDone          | 1             | Acknowledged data transfer on this endpoint has occurred             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |               |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| H-N              | RW         | EPOUT[i] (i=1..7) |               | Acknowledged data transfer on this OUT endpoint. Write '1' to clear. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |               |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | NotStarted        | 0             | No acknowledged data transfer on this endpoint                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |               |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|                  |            | Started           | 1             | Acknowledged data transfer on this endpoint has occurred             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |               |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

### 7.1.40.13.50 USBADDR

Address offset: 0x470

Device USB address

|                  |            |      |          |                                                                                       |  |  |  |                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------------|------|----------|---------------------------------------------------------------------------------------|--|--|--|--------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |            |      |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |            |      |          |                                                                                       |  |  |  |                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |      |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |  |  |  |                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce Field |      | Value ID | Value                                                                                 |  |  |  | Description        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | R          | ADDR |          |                                                                                       |  |  |  | Device USB address |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

### 7.1.40.13.51 BMREQUESTTYPE

Address offset: 0x480

SETUP data, byte 0, bmRequestType

| Bit number       |      |           |              | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------|-----------|--------------|---------------------------------------------------------------------------------------|-------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| ID               |      |           |              |                                                                                       |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | C B B A A A A A |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |           |              | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce | Field     | Value ID     | Value                                                                                 | Description             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | R    | RECIPIENT |              |                                                                                       | Data transfer type      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |           | Device       | 0                                                                                     | Device                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |           | Interface    | 1                                                                                     | Interface               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |           | Endpoint     | 2                                                                                     | Endpoint                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |           | Other        | 3                                                                                     | Other                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | R    | TYPE      |              |                                                                                       | Data transfer type      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |           | Standard     | 0                                                                                     | Standard                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |           | Class        | 1                                                                                     | Class                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |           | Vendor       | 2                                                                                     | Vendor                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| C                | R    | DIRECTION |              |                                                                                       | Data transfer direction |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |           | HostToDevice | 0                                                                                     | Host-to-device          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |           | DeviceToHost | 1                                                                                     | Device-to-host          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

### 7.1.40.13.52 BREQUEST

Address offset: 0x484

SETUP data, byte 1, bRequest

| Bit number       |      |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |
|------------------|------|----------|---------------------------------------------------------------------------------------|-------|------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|
| ID               |      |          |                                                                                       |       |                                                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A |  |  |  |  |  |
| Reset 0x00000000 |      |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |       |                                                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |
| ID               | Acce | Field    | Value ID                                                                              | Value | Description                                                                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |
| A                | R    | BREQUEST |                                                                                       |       | SETUP data, byte 1, bRequest. Values provided for standard requests only, user must implement class and vendor values. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |
|                  |      |          | STD_GET_STATUS                                                                        | 0     | Standard request GET_STATUS                                                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |
|                  |      |          | STD_CLEAR_FEATURE                                                                     | 1     | Standard request CLEAR_FEATURE                                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |
|                  |      |          | STD_SET_FEATURE                                                                       | 3     | Standard request SET_FEATURE                                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |
|                  |      |          | STD_SET_ADDRESS                                                                       | 5     | Standard request SET_ADDRESS                                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |
|                  |      |          | STD_GET_DESCRIPTOR                                                                    | 6     | Standard request GET_DESCRIPTOR                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |
|                  |      |          | STD_SET_DESCRIPTOR                                                                    | 7     | Standard request SET_DESCRIPTOR                                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |
|                  |      |          | STD_GET_CONFIGURATION                                                                 | 8     | Standard request GET_CONFIGURATION                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |
|                  |      |          | STD_SET_CONFIGURATION                                                                 | 9     | Standard request SET_CONFIGURATION                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |
|                  |      |          | STD_GET_INTERFACE                                                                     | 10    | Standard request GET_INTERFACE                                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |
|                  |      |          | STD_SET_INTERFACE                                                                     | 11    | Standard request SET_INTERFACE                                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |
|                  |      |          | STD_SYNCH_FRAME                                                                       | 12    | Standard request SYNCH_FRAME                                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |

### 7.1.40.13.53 WVALUEL

Address offset: 0x488

SETUP data, byte 2, LSB of wValue

|                  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  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 |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  | 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| Reset 0x00000000 |  |  |  |  |  |  |  |  |  | 0  |    |    |    |    |    |    |    |    |    | 0  |    |    |    |    |    |    |    |    |    | 0  |    |   |   |   |   |   |   |   |   | 0 |   |   |   |   |   |   |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  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|  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |

### 7.1.40.13.54 WVALUEH

Address offset: 0x48C

SETUP data, byte 3, MSB of wValue

|            |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |
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| Bit number       |      |         |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |         |       | A A A A A A A A                                                                       |       |                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |         |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |       |                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field   | Value | ID                                                                                    | Value | Description                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | R    | WINDEXL |       |                                                                                       |       | SETUP data, byte 4, LSB of windex |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.40.13.56 WINDEXH

Address offset: 0x494

SETUP data, byte 5, MSB of wIndex

|                  |      |         |       |    |       |                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------|---------|-------|----|-------|-----------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |      |         |       | 31 | 30    | 29                                | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |      |         |       |    |       |                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |      |         |       | 0  | 0     | 0                                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce | Field   | Value | ID | Value | Description                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | R    | WINDEXH |       |    |       | SETUP data, byte 5, MSB of wIndex |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.40.13.57 WLENGTHL

Address offset: 0x498

SETUP data, byte 6, LSB of wLength

|            |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
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| Bit number |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID         |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |

### 7.1.40.13.58 WLENGTHH

Address offset: 0x49C

SETUP data, byte 7, MSB of wLength

|                  |            |          |  |          |  |  |       |                                    |  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|--|----------|--|--|-------|------------------------------------|--|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |  |          |  |  |       |                                    |  | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |
| ID               |            |          |  |          |  |  |       |                                    |  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  | A  | A  | A  | A | A | A | A | A |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |          |  |          |  |  |       |                                    |  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |          |  | Value ID |  |  | Value |                                    |  | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | R          | WLENGTHH |  |          |  |  |       | SETUP data, byte 7, MSB of wLength |  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.40.13.59 SIZE.EPOUT[n] (n=0..7)

Address offset: 0x4A0 + (n × 0x4)

Number of bytes received last in the data stage of this OUT endpoint

Write to any value to accept further OUT traffic on this endpoint, and overwrite the intermediate buffer

|                  |  |  |  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            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| Bit number       |  |  |  | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      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| ID               |  |  |  | A A A A A A A A                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            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### 7.1.40.13.60 SIZE.ISOOUT

Address offset: 0x4C0

Number of bytes received last on this ISO OUT data endpoint

|                  |            |      |  |          |          |  |       |                                  |                                                 |             |                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|------|--|----------|----------|--|-------|----------------------------------|-------------------------------------------------|-------------|-------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |      |  |          |          |  |       |                                  |                                                 | 31          | 30                                                          | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |
| ID               |            |      |  |          |          |  |       |                                  |                                                 |             |                                                             |    |    |    |    |    |    |    |    | B  |    |    |    |    |    |    |    |    |    |    |    |   |   |   | A | A | A | A | A | A | A | A | A |   |   |
| Reset 0x00010000 |            |      |  |          |          |  |       |                                  |                                                 | 0           | 0                                                           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |      |  | Value ID |          |  | Value |                                  |                                                 | Description |                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | R          | SIZE |  |          |          |  |       |                                  |                                                 |             | Number of bytes received last on this ISO OUT data endpoint |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | R          | ZERO |  |          |          |  |       | Zero-length data packet received |                                                 |             |                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |      |  |          | Normal   |  |       | 0                                | No zero-length data received, use value in SIZE |             |                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |      |  |          | ZeroData |  |       | 1                                | Zero-length data received, ignore value in SIZE |             |                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.40.13.61 ENABLE

Address offset: 0x500

Enable USB

After writing Disabled to this register, reading the register will return Enabled until USB is completely disabled.

|                  |            |          |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | ENABLE   |       | Enable USB                                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0     | USB peripheral is disabled                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1     | USB peripheral is enabled                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.40.13.62 USBPULLUP

Address offset: 0x504

Control of the USB pull-up

|                  |            |  |          |                                                                                       |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|--|----------|---------------------------------------------------------------------------------------|-------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |  |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |  |          | A                                                                                     |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |  |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field |  | Value ID | Value                                                                                 | Description                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW CONNECT |  |          |                                                                                       | Control of the USB pull-up on the D+ line |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |  | Disabled | 0                                                                                     | Pull-up is disconnected                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |  | Enabled  | 1                                                                                     | Pull-up is connected to D+                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.40.13.63 DPDMVALUE

Address offset: 0x508

State D+ and D- lines will be forced into by the DPDMDRIVE task. The DPDMNODRIVE task reverts the control of the lines to MAC IP (no forcing).

|                  |            |          |                                                                                       |                                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          | A A A A A                                                                             |                                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |                                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW STATE   |          |                                                                                       | State D+ and D- lines will be forced into by the DPDMDRIVE task                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Resume   | 1                                                                                     | D+ forced low, D- forced high (K state) for a timing preset in hardware (50 μs or 5 ms, depending on bus state) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | J        | 2                                                                                     | D+ forced high, D- forced low (J state)                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | K        | 4                                                                                     | D+ forced low, D- forced high (K state)                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.40.13.64 DTOGGLE

Address offset: 0x50C

Data toggle control and status

Write this register first with VALUE=Nop to select the endpoint; then read it to get the status from VALUE, or write it again with VALUE=Data0 or Data1

|                  |      |                |       |    |       |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------|----------------|-------|----|-------|--------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |      |                |       | 31 | 30    | 29                                               | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |      |                |       |    |       |                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | I | H | G | F | E | D | C | B | A |
| Reset 0x00000001 |      |                |       | 0  | 0     | 0                                                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |   |
| ID               | Acce | Field          | Value | ID | Value | Description                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A-H              | RW   | IN[i] (i=0..7) |       |    |       | Enable IN endpoint i                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      | Disable        | 0     |    |       | Disable endpoint IN i (no response to IN tokens) |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      | Enable         | 1     |    |       | Enable endpoint IN i (response to IN tokens)     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| I                | RW   | ISOIN          |       |    |       | Enable ISO IN endpoint                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      | Disable        | 0     |    |       | Disable ISO IN endpoint 8                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      | Enable         | 1     |    |       | Enable ISO IN endpoint 8                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

|                  |      |                 |       |                                                    |       |                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------|-----------------|-------|----------------------------------------------------|-------|---------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |      |                 |       |                                                    | 31    | 30                        | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |      |                 |       |                                                    |       |                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | I | H | G | F | E | D | C | B | A |
| Reset 0x00000001 |      |                 |       |                                                    | 0     | 0                         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |   |
| ID               | Acce | Field           | Value | ID                                                 | Value | Description               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A-H              | RW   | OUT[i] (i=0..7) |       |                                                    |       | Enable OUT endpoint i     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      | Disable         | 0     | Disable endpoint OUT i (no response to OUT tokens) |       |                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      | Enable          | 1     | Enable endpoint OUT i (response to OUT tokens)     |       |                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| I                | RW   | ISOOUT          |       |                                                    |       | Enable ISO OUT endpoint 8 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      | Disable         | 0     | Disable ISO OUT endpoint 8                         |       |                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      | Enable          | 1     | Enable ISO OUT endpoint 8                          |       |                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

| Bit number       |      |       |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |       |  |
|------------------|------|-------|----------|---------------------------------------------------------------------------------------|-------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----|--|-------|--|
| ID               |      |       |          |                                                                                       |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | C B |  | A A A |  |
| Reset 0x00000000 |      |       |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |       |  |
| ID               | Acce | Field | Value ID | Value                                                                                 | Description                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |       |  |
| A                | W    | EP    |          |                                                                                       | Select endpoint number        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |       |  |
| B                | W    | IO    |          |                                                                                       | Selects IN or OUT endpoint    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |       |  |
|                  |      |       | Out      | 0                                                                                     | Selects OUT endpoint          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |       |  |
|                  |      |       | In       | 1                                                                                     | Selects IN endpoint           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |       |  |
| C                | W    | STALL |          |                                                                                       | Stall selected endpoint       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |       |  |
|                  |      |       | UnStall  | 0                                                                                     | Don't stall selected endpoint |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |       |  |
|                  |      |       | Stall    | 1                                                                                     | Stall selected endpoint       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |  |       |  |

### 7.1.40.13.68 ISOSPLIT

Address offset: 0x51C

Controls the split of ISO buffers

|                  |            |          |        |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|--------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          |        | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          |        |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | A A A A A A A A A A A A A A A A |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          |        | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value  | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW SPLIT   |          |        | Controls the split of ISO buffers                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | OneDir   | 0x0000 | Full buffer dedicated to either iso IN or OUT                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | HalfIN   | 0x0080 | Lower half for IN, upper half for OUT                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.40.13.69 FRAMECNTR

Address offset: 0x520

Returns the current value of the start of frame counter

|                  |            |           |          |                                                                                       |                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|-----------|----------|---------------------------------------------------------------------------------------|---------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |           |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |           |          | A A A A A A A A A A A A A A A A                                                       |                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |           |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field |           | Value ID | Value                                                                                 | Description                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | R          | FRAMECNTR |          |                                                                                       | Returns the current value of the start of frame counter |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.40.13.70 LOWPOWER

Address offset: 0x52C

Controls USB peripheral low power mode during USB suspend

| Bit number       |            |             | 31    | 30                                                                                                                              | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------|------------|-------------|-------|---------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| ID               |            |             |       |                                                                                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | A |
| Reset 0x00000000 |            |             | 0     | 0                                                                                                                               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID    | Value | Description                                                                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | LOWPOWER    |       | Controls USB peripheral low-power mode during USB suspend                                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | ForceNormal | 0     | Software must write this value to exit low power mode and before performing a remote wake-up                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            | LowPower    | 1     | Software must write this value to enter low power mode after DMA and software have finished interacting with the USB peripheral |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.40.13.71 ISOINCONFIG

Address offset: 0x530

Controls the response of the ISO IN endpoint to an IN token when no data is ready to be sent

|                  |            |          |          |                                                                                       |                                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|----------|---------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          |          | A                                                                                     |                                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field |          | Value ID | Value                                                                                 | Description                                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | RESPONSE |          |                                                                                       | Controls the response of the ISO IN endpoint to an IN token when no data is ready to be sent |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | NoResp   | 0        | Endpoint does not respond in that case                                                |                                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | ZeroData | 1        | Endpoint responds with a zero-length data packet in that case                         |                                                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.40.13.72 EPIN[n].PTR (n=0..7)

Address offset: 0x600 + (n × 0x14)

Data pointer

|                  |            |          |       |    |    |                                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|------------------|------------|----------|-------|----|----|------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|--|
| Bit number       |            |          | 31    | 30 | 29 | 28                                                                                 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |
| ID               |            |          | A     | A  | A  | A                                                                                  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |  |  |  |  |
| Reset 0x00000000 |            |          | 0     | 0  | 0  | 0                                                                                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |  |
| ID               | Acce Field | Value ID | Value |    |    | Description                                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| A                | RW         | PTR      |       |    |    | Data pointer                                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            |          |       |    |    | See the memory chapter for details about which memories are available for EasyDMA. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |

### 7.1.40.13.73 EPIN[n].MAXCNT (n=0..7)

Address offset: 0x604 + (n × 0x14)

Maximum number of bytes to transfer

|                  |            |          |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          | A A A A A A A                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Description                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | MAXCNT   | [64..0]                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Maximum number of bytes to transfer |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |



### 7.1.40.13.74 EPIN[n].AMOUNT (n=0..7)

Address offset:  $0x608 + (n \times 0x14)$

Number of bytes transferred in the last transaction

|                  |            |        |          |  |       |                                                     |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------|----------|--|-------|-----------------------------------------------------|-------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |        |          |  |       |                                                     |             |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |        |          |  |       |                                                     |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  | A  | A | A | A | A | A | A |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |        |          |  |       |                                                     |             |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |        | Value ID |  | Value |                                                     | Description |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | R          | AMOUNT |          |  |       | Number of bytes transferred in the last transaction |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.40.13.75 ISOIN.PTR

Address offset: 0x6A0

Data pointer

|                  |            |  |  |          |  |  |              |  |  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|--|----------|--|--|--------------|--|--|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |  |          |  |  |              |  |  | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |
| ID               |            |  |  |          |  |  |              |  |  | A           | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A | A | A | A |   |
| Reset 0x00000000 |            |  |  |          |  |  |              |  |  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  |  | Value ID |  |  | Value        |  |  | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW PTR     |  |  |          |  |  | Data pointer |  |  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

See the memory chapter for details about which memories are available for EasyDMA.

### 7.1.40.13.76 ISOIN.MAXCNT

Address offset: 0x6A4

Maximum number of bytes to transfer

|                  |            |        |          |           |    |                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------|----------|-----------|----|-------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |        |          | 31        | 30 | 29                                  | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               |            |        |          |           |    |                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |        |          | 0         | 0  | 0                                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| ID               | Acce Field |        | Value ID | Value     |    | Description                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | MAXCNT |          | [1023..1] |    | Maximum number of bytes to transfer |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.40.13.77 ISOIN.AMOUNT

Address offset: 0x6A8

Number of bytes transferred in the last transaction

|                  |  |  |  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            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 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| Bit number       |  |  |  | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      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 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |  |  |  | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                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 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |  |  |  | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 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### 7.1.40.13.78 EPOUT[n].PTR (n=0..7)

Address offset:  $0x700 + (n \times 0x14)$

Data pointer

|                  |            |  |          |                                                                                    |    |    |    |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|------------------------------------------------------------------------------------|----|----|----|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31                                                                                 | 30 | 29 | 28 | 27           | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |  |          | A                                                                                  | A  | A  | A  | A            | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |          | 0                                                                                  | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID | Value                                                                              |    |    |    | Description  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW PTR     |  |          |                                                                                    |    |    |    | Data pointer |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |  |          | See the memory chapter for details about which memories are available for EasyDMA. |    |    |    |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 7.1.40.13.79 EPOUT[n].MAXCNT (n=0..7)

Address offset: 0x704 + (n × 0x14)

Maximum number of bytes to transfer

|                  |            |        |          |         |    |                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------|----------|---------|----|-------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |        |          | 31      | 30 | 29                                  | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |        |          |         |    |                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A | A | A | A | A | A | A |   |
| Reset 0x00000000 |            |        |          | 0       | 0  | 0                                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |        | Value ID | Value   |    | Description                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | MAXCNT |          | [64..0] |    | Maximum number of bytes to transfer |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 7.1.40.13.80 EPOUT[n].AMOUNT (n=0..7)

Address offset: 0x708 + (n × 0x14)

Number of bytes transferred in the last transaction

|                  |  |  |  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| Bit number       |  |  |  | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      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| ID               |  |  |  | A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                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| Reset 0x00000000 |  |  |  | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 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#### 7.1.40.13.81 ISOOUT.PTR

Address offset: 0x7A0

Data pointer

|                  |            |  |  |          |  |  |              |  |  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|--|----------|--|--|--------------|--|--|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |  |          |  |  |              |  |  | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |  |  |          |  |  |              |  |  | A           | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |  |          |  |  |              |  |  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  |  | Value ID |  |  | Value        |  |  | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW PTR     |  |  |          |  |  | Data pointer |  |  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

See the memory chapter for details about which memories are available for EasyDMA.

#### 7.1.40.13.82 ISOOUT.MAXCNT

Address offset: 0x7A4

Maximum number of bytes to transfer

|                  |            |          |       |    |    |    |    |    |    |    |    |    |                                     |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|-------|----|----|----|----|----|----|----|----|----|-------------------------------------|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          | 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21                                  | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |
| ID               |            |          |       |    |    |    |    |    |    |    |    |    |                                     |    |    |    |    |    |    |    |    |    |    |    |   | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |   |   |   |   |   |
| ID               | Acce Field | Value ID | Value |    |    |    |    |    |    |    |    |    | Description                         |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | MAXCNT   |       |    |    |    |    |    |    |    |    |    | Maximum number of bytes to transfer |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.40.13.83 ISOOUT.AMOUNT

Address offset: 0x7A8

Number of bytes transferred in the last transaction

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## 7.1.40.14 Electrical specification

### 7.1.40.14.1 USB Electrical Specification

| Symbol              | Description                                                              | Min. | Typ. | Max. | Units    |
|---------------------|--------------------------------------------------------------------------|------|------|------|----------|
| $R_{USB,PU,ACTIVE}$ | Value of pull-up on D+, bus active (upstream device transmitting)        | ..   | ..   | ..   | $\Omega$ |
| $R_{USB,PU,IDLE}$   | Value of pull-up on D+, bus idle                                         | ..   | ..   | ..   | $\Omega$ |
| $t_{USB,DETRST}$    | Minimum duration of an SE0 state to be detected as a USB reset condition | ..   | ..   | ..   | $\mu s$  |
| $f_{USB,CLK}$       | Frequency of local clock, USB active                                     | ..   | ..   | ..   | MHz      |
| $f_{USB,TOL}$       | Accuracy of local clock, USB active <sup>28</sup>                        | ..   | ..   | ..   | ppm      |
| $T_{USB,JITTER}$    | Jitter on USB local clock, USB active                                    | ..   | ..   | ..   | ns       |

## 7.1.41 VMC — Volatile memory controller

The VMC provides power control of RAM blocks.

Each of the available RAM blocks, which each may contain multiple RAM sections, can power up and down independently in both System ON and System OFF mode, using the RAM[n] registers. See [Memory](#) chapter for more information about RAM blocks and sections.

### 7.1.41.1 RAM power states

In System OFF, retention of a RAM section is configured in the RETENTION field of the corresponding register [RAM\[n\].POWER \(n=0..7\)](#) on page 720.

In System ON, retention and accessibility for a RAM section is configured in the RETENTION and POWER fields of the corresponding register [RAM\[n\].POWER \(n=0..7\)](#) on page 720.

The following table summarizes the behavior of these registers.

<sup>28</sup> The local clock can be stopped during USB suspend

| Configuration |                    |                        | RAM section status |          |
|---------------|--------------------|------------------------|--------------------|----------|
| System on/off | RAM[n].POWER.POWER | RAM[n].POWER.RETENTION | Accessible         | Retained |
| Off           | x                  | Off                    | No                 | No       |
| Off           | x                  | On                     | No                 | Yes      |
| On            | Off                | Off                    | No                 | No       |
| On            | Off <sup>1</sup>   | On                     | No                 | Yes      |
| On            | On                 | x                      | Yes                | Yes      |

Table 181: RAM section configuration. x = don't care.

The advantage of not retaining RAM contents is that the overall current consumption is reduced.

See chapter [Memory](#) on page 18 for more information on RAM sections.

### 7.1.41.2 Registers

| Base address | Domain      | Peripheral | Instance | Secure mapping | DMA security | Description                | Configuration            |
|--------------|-------------|------------|----------|----------------|--------------|----------------------------|--------------------------|
| 0x50081000   | APPLICATION | VMC        | VMC : S  | US             | NA           | Volatile memory controller |                          |
| 0x40081000   |             |            | VMC : NS |                |              |                            |                          |
| 0x41081000   | NETWORK     | VMC        | VMC      | NS             | NA           | Volatile memory controller | 4 RAM slaves implemented |
|              |             |            |          |                |              |                            | 4 RAM slaves implemented |

Table 182: Instances

| Register        | Offset | Security | Description                         |
|-----------------|--------|----------|-------------------------------------|
| RAM[n].POWER    | 0x600  |          | RAM[n] power control register       |
| RAM[n].POWERSET | 0x604  |          | RAM[n] power control set register   |
| RAM[n].POWERCLR | 0x608  |          | RAM[n] power control clear register |

Table 183: Register overview

#### 7.1.41.2.1 RAM[n].POWER (n=0..7)

Address offset: 0x600 + (n × 0x10)

RAM[n] power control register

| Bit number       |            | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |       |  |                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|---------------------------------------------------------------------------------------|--|-------|--|-----------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |            | f e d c b a Z Y X W V U T S R Q P O N M L K J I H G F E D C B A                       |  |       |  |                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x0000FFFF |            | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1                         |  |       |  |                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID                                                                              |  | Value |  | Description                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A-P              | RW         | S[i]POWER (i=0..15)                                                                   |  |       |  | Keep RAM section Si of RAM[n] on or off in System ON mode                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Off                                                                                   |  | 0     |  | Off                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | On                                                                                    |  | 1     |  | On                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Q-f              | RW         | S[i]RETENTION (i=0..15)                                                               |  |       |  | Keep retention on RAM section Si of RAM[n] when RAM section is switched off |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Off                                                                                   |  | 0     |  | Off                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | On                                                                                    |  | 1     |  | On                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

<sup>1</sup> Not useful setting. RAM section power off gives negligible reduction in current consumption when retention is on.

### 7.1.41.2.2 RAM[n].POWERSET (n=0..7)

Address offset:  $0x604 + (n \times 0x10)$

RAM[n] power control set register

When read, this register will return the value of the RAM[n].POWER register.

|                  |      |                         |       |    |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|-------------------------|-------|----|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|-----------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |                         |       | 31 | 30    | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |                         |       | f  | e     | d  | c  | b  | a  | z  | y  | x  | w  | v  | u  | t  | s  | r  | q  | p  | o  | n  | m  | l  | k  | j | i | h | g | f | e | d | c | b | a |  |  |  |                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x0000FFFF |      |                         |       | 0  | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  |  |  |                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field                   | Value | ID | Value |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  | Description                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A-P              | RW   | S[i]POWER (i=0..15)     |       |    |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  | Keep RAM section Si of RAM[n] on or off in System ON mode                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                         | On    |    | 1     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  | On                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Q-f              | RW   | S[i]RETENTION (i=0..15) |       |    |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  | Keep retention on RAM section Si of RAM[n] when RAM section is switched off |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |                         | On    |    | 1     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  | On                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.41.2.3 RAM[n].POWERCLR (n=0..7)

Address offset:  $0x608 + (n \times 0x10)$

RAM[n] power control clear register

When read, this register will return the value of the RAM[n].POWER register.

| Bit number       |      |                         | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |    |       |                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|-------------------------|---------------------------------------------------------------------------------------|----|-------|-----------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |      |                         | f e d c b a Z Y X W V U T S R Q P O N M L K J I H G F E D C B A                       |    |       |                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x0000FFFF |      |                         | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1                       |    |       |                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field                   | Value                                                                                 | ID | Value | Description                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A-P              | RW   | S[i]POWER (i=0..15)     |                                                                                       |    |       | Keep RAM section Si of RAM[n] on or off in System ON mode                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Off                     | 1                                                                                     |    |       | Off                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Q-f              | RW   | S[i]RETENTION (i=0..15) |                                                                                       |    |       | Keep retention on RAM section Si of RAM[n] when RAM section is switched off |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      | Off                     | 1                                                                                     |    |       | Off                                                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

## 7.1.42 WDT — Watchdog timer

A countdown watchdog timer using the low-frequency clock source (LFCLK) offers configurable and robust protection against application lock-up.

The watchdog must be configured before it is started.

After configuration, the watchdog is started by triggering the START task.

After it is started, the watchdog's configuration registers, which comprise registers CRV, RREN, and CONFIG, will be blocked for further configuration.

The watchdog can be paused during long CPU sleep periods for low power applications and when the debugger has halted the CPU. The watchdog is implemented as a down-counter that generates a TIMEOUT event when it wraps over after counting down to 0. When the watchdog timer is started through the START task, the watchdog counter is loaded with the value specified in the CRV register. This counter is also reloaded with the value specified in the CRV register when a reload request is granted.

The watchdog's timeout period is given by:

$$\text{timeout [s]} = ( \text{CRV} + 1 ) / 32768$$

When started, the watchdog will automatically force the 32.768 kHz RC oscillator on as long as no other 32.768 kHz clock source is running and generating the 32.768 kHz system clock, see chapter [CLOCK — Clock control](#) on page 61.

#### 7.1.42.1 Reload criteria

The watchdog has eight separate reload request registers, which shall be used to request the watchdog to reload its counter with the value specified in the CRV register. To reload the watchdog counter, the special value 0x6E524635 needs to be written to all enabled reload registers.

One or more RR registers can be individually enabled through the RREN register.

#### 7.1.42.2 Temporarily pausing the watchdog

By default, the watchdog will be active counting down the down-counter while the CPU is sleeping. It is however possible to configure the watchdog to automatically pause while the CPU is sleeping as well as when it is halted by the debugger.

Going to system OFF-mode will stop and disable the watchdog.

#### 7.1.42.3 Watchdog reset

A TIMEOUT event will automatically lead to a watchdog reset.

See [RESET - Reset control](#) on page 55 for more information about reset sources. If the watchdog is configured to generate an interrupt on the TIMEOUT event, the watchdog reset will be postponed with two 32.768 kHz clock cycles after the TIMEOUT event has been generated. Once the TIMEOUT event has been generated, and unless the watchdog is stopped, the impending watchdog reset will be effectuated.

The watchdog can be reset from several reset sources, see [Application core reset behavior](#) on page 57. After being reset from these sources, the watchdog configuration registers will be available for configuration again.

#### 7.1.42.4 Stopping the watchdog

By default, the watchdog cannot be stopped. It is however possible to configure the watchdog to allow the STOP task.

To allow stopping the watchdog, the STOPEN field of the [CONFIG](#) register must be set to Enable when configuring the watchdog.

Then, to stop the watchdog,

- the special value 0x6E524635 must be written to the [TSEN](#) register
- the STOP task must be invoked

When all of these conditions are met, the watchdog is stopped. The STOPPED event indicates a successful stopping of the watchdog.

When the watchdog is stopped, the watchdog's configuration registers [CRV](#), [RREN](#) and [CONFIG](#) are no longer blocked.

**Note:** It is recommended to write zeros to [TSEN](#) on page 728 after the watchdog has stopped, to avoid un-intended invocation of the STOP task.

## 7.1.42.5 Registers

| Base address | Domain      | Peripheral | Instance  | Secure mapping | DMA security | Description      | Configuration |
|--------------|-------------|------------|-----------|----------------|--------------|------------------|---------------|
| 0x50018000   | APPLICATION | WDT        | WDT0 : S  | US             | NA           | Watchdog timer 0 |               |
| 0x40018000   |             |            | WDT0 : NS |                |              |                  |               |
| 0x50019000   | APPLICATION | WDT        | WDT1 : S  | US             | NA           | Watchdog timer 1 |               |
| 0x40019000   |             |            | WDT1 : NS |                |              |                  |               |
| 0x4100B000   | NETWORK     | WDT        | WDT       | NS             | NA           | Watchdog timer   |               |

Table 184: Instances

| Register        | Offset | Security | Description                                             |
|-----------------|--------|----------|---------------------------------------------------------|
| TASKS_START     | 0x000  |          | Start the watchdog                                      |
| TASKS_STOP      | 0x004  |          | Stop the watchdog timer.                                |
| SUBSCRIBE_START | 0x080  |          | Subscribe configuration for task <a href="#">START</a>  |
| SUBSCRIBE_STOP  | 0x084  |          | Subscribe configuration for task <a href="#">STOP</a>   |
| EVENTS_TIMEOUT  | 0x100  |          | Watchdog timeout                                        |
| EVENTS_STOPPED  | 0x104  |          | Watchdog stopped                                        |
| PUBLISH_TIMEOUT | 0x180  |          | Publish configuration for event <a href="#">TIMEOUT</a> |
| PUBLISH_STOPPED | 0x184  |          | Publish configuration for event <a href="#">STOPPED</a> |
| INTENSET        | 0x304  |          | Enable interrupt                                        |
| INTENCLR        | 0x308  |          | Disable interrupt                                       |
| NMIENSET        | 0x324  |          | Enable interrupt                                        |
| NMIENCLR        | 0x328  |          | Disable interrupt                                       |
| RUNSTATUS       | 0x400  |          | Run status                                              |
| REQSTATUS       | 0x404  |          | Request status                                          |
| CRV             | 0x504  |          | Counter reload value                                    |
| RREN            | 0x508  |          | Enable register for reload request registers            |
| CONFIG          | 0x50C  |          | Configuration register                                  |
| TSEN            | 0x520  |          | Task Stop Enable                                        |
| RR[n]           | 0x600  |          | Reload request n                                        |

Table 185: Register overview

### 7.1.42.5.1 TASKS\_START

Address offset: 0x000

Start the watchdog

|                  |            |             |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|-------------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |             |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |             |       | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |             |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID    | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W          | TASKS_START |       | Start the watchdog                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Trigger     | 1     | Trigger task                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.42.5.2 TASKS\_STOP

Address offset: 0x004

Stop the watchdog timer.





|                  |            |                |          |              |       |                  |                     |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------------|----------|--------------|-------|------------------|---------------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                |          |              |       |                  |                     |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |                |          |              |       |                  |                     |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |   |
| Reset 0x00000000 |            |                |          |              |       |                  |                     |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |                | Value ID |              | Value |                  | Description         |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | EVENTS_STOPPED |          |              |       | Watchdog stopped |                     |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |                |          | NotGenerated |       | 0                | Event not generated |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |                |          | Generated    |       | 1                | Event generated     |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.42.5.7 PUBLISH\_TIMEOUT

Address offset: 0x180

Publish configuration for event **TIMEOUT**

|                  |            |          |          |          |       |                                                    |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|----------|-------|----------------------------------------------------|-------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          |          |       |                                                    |             |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |
| ID               |            |          |          |          |       |                                                    |             |  |  | B  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  |    |    |    |   |   |   |   |   |   | A | A | A | A | A | A | A |   |
| Reset 0x00000000 |            |          |          |          |       |                                                    |             |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |          | Value ID |          | Value |                                                    | Description |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | CHIDX    |          | [255..0] |       | Channel that event <b>TIMEOUT</b> will publish to. |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW         | EN       |          |          |       |                                                    |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled |          | 0        |       | Disable publishing                                 |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  |          | 1        |       | Enable publishing                                  |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.42.5.8 PUBLISH\_STOPPED

Address offset: 0x184

Publish configuration for event **STOPPED**

|                  |            |          |          |          |    |                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|----------|----|---------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          | 31       | 30 | 29                                          | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |          |          | B        |    |                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A |   |   |   |   | A | A | A | A | A | A |
| Reset 0x00000000 |            |          |          | 0        | 0  | 0                                           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |
| ID               | Acce Field |          | Value ID | Value    |    | Description                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | CHIDX    |          | [255..0] |    | Channel that event STOPPED will publish to. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW         | EN       |          |          |    |                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled |          | 0        |    | Disable publishing                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled  |          | 1        |    | Enable publishing                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

#### 7.1.42.5.9 INTENSET

Address offset: 0x304

Enable interrupt

| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|-----------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |            |          | B A                                                                                   |                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW TIMEOUT |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">TIMEOUT</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Set      | 1                                                                                     | Enable                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Read: Disabled                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Read: Enabled                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW STOPPED |          |                                                                                       | Write '1' to enable interrupt for event <a href="#">STOPPED</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Set      | 1                                                                                     | Enable                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Read: Disabled                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Read: Enabled                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.42.5.10 INTENCLR

Address offset: 0x308

Disable interrupt

| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |            |          | B A                                                                                   |                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW TIMEOUT |          |                                                                                       | Write '1' to disable interrupt for event <a href="#">TIMEOUT</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Clear    | 1                                                                                     | Disable                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Read: Disabled                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Read: Enabled                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW STOPPED |          |                                                                                       | Write '1' to disable interrupt for event <a href="#">STOPPED</a> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Clear    | 1                                                                                     | Disable                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Read: Disabled                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Read: Enabled                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.42.5.11 NMIENSET

Address offset: 0x324

Enable interrupt

|                  |            |          |                                                                                       |                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|-------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          | B A                                                                                   |                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0       |                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW TIMEOUT |          |                                                                                       | Write '1' to enable interrupt for event TIMEOUT |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Set      | 1                                                                                     | Enable                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Read: Disabled                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Read: Enabled                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW STOPPED |          |                                                                                       | Write '1' to enable interrupt for event STOPPED |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Set      | 1                                                                                     | Enable                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | Read: Disabled                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Read: Enabled                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 7.1.42.5.12 NMIENCLR

Address offset: 0x328



|                  |      |       |       |    |                          |                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------|-------|-------|----|--------------------------|------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |      |       |       | 31 | 30                       | 29                                                               | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |      |       |       | A  | A                        | A                                                                | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0xFFFFFFFF |      |       |       | 1  | 1                        | 1                                                                | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ID               | Accs | Field | Value | ID | Value                    | Description                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW   | CRV   |       |    | [0x0000000F..0xFFFFFFFF] | Counter reload value in number of cycles of the 32.768 kHz clock |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.42.5.16 RREN

Address offset: 0x508

Enable register for reload request registers

|                  |       |                |          |    |       |                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|------------------|-------|----------------|----------|----|-------|----------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|--|
| Bit number       |       |                |          | 31 | 30    | 29                               | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |
| ID               |       |                |          |    |       |                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | H | G | F | E | D | C | B | A |  |  |  |  |
| Reset 0x00000001 |       |                |          | 0  | 0     | 0                                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |  |  |  |  |
| ID               | Acces | Field          | Value    | ID | Value | Description                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| A-H              | RW    | RR[i] (i=0..7) |          |    |       | Enable or disable RR[i] register |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |       |                | Disabled |    | 0     | Disable RR[i] register           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |       |                | Enabled  |    | 1     | Enable RR[i] register            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |

### 7.1.42.5.17 CONFIG

Address offset: 0x50C

Configuration register

| Bit number       |            |        |          |       | 31                                                                                                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
|------------------|------------|--------|----------|-------|------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| ID               |            |        |          |       |                                                                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   | F |   |   |   | C |   |   |   | A |
| Reset 0x00000001 |            |        |          |       | 0                                                                                                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |   |
| D                | Acce Field |        | Value ID | Value | Description                                                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | SLEEP  |          |       | Configure the watchdog to either be paused, or kept running, while the CPU is sleeping               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |        | Pause    | 0     | Pause watchdog while the CPU is sleeping                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |        | Run      | 1     | Keep the watchdog running while the CPU is sleeping                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| C                | RW         | HALT   |          |       | Configure the watchdog to either be paused, or kept running, while the CPU is halted by the debugger |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |        | Pause    | 0     | Pause watchdog while the CPU is halted by the debugger                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |        | Run      | 1     | Keep the watchdog running while the CPU is halted by the debugger                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| F                | RW         | STOPEN |          |       | Allow stopping the watchdog                                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |        | Disable  | 0     | Do not allow stopping the watchdog                                                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |        | Enable   | 1     | Allow stopping the watchdog                                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 7.1.42.5.18 TSEN

Address offset: 0x520

Task Stop Enable

|                  |            |      |          |            |    |    |    |                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|------|----------|------------|----|----|----|--------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |      |          | 31         | 30 | 29 | 28 | 27                                   | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |      |          | A          | A  | A  | A  | A                                    | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |      |          | 0          | 0  | 0  | 0  | 0                                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |      | Value ID | Value      |    |    |    | Description                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | W          | TSEN |          |            |    |    |    | Task stop enable register            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |      | Enable   | 0x6E524635 |    |    |    | Value to allow stopping the watchdog |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 7.1.42.5.19 RR[n] (n=0..7)

Address offset: 0x600 + (n × 0x4)

Reload request n

|                  |            |    |          |            |    |    |    |                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----|----------|------------|----|----|----|-------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |    |          | 31         | 30 | 29 | 28 | 27                                              | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |    |          | A          | A  | A  | A  | A                                               | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |    |          | 0          | 0  | 0  | 0  | 0                                               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |    | Value ID | Value      |    |    |    | Description                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | W          | RR |          |            |    |    |    | Reload request register                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |    | Reload   | 0x6E524635 |    |    |    | Value to request a reload of the watchdog timer |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

## 7.1.42.6 Electrical specification

### 7.1.42.6.1 Watchdog Timer Electrical Specification

| Symbol | Description       | Min. | Typ. | Max. | Units |
|--------|-------------------|------|------|------|-------|
| twDT   | Time out interval | ..   | ..   | ..   |       |

## 8 Debug and trace

## 8.1 Overview

The debug and trace system offers a flexible and powerful mechanism for non-intrusive debugging.

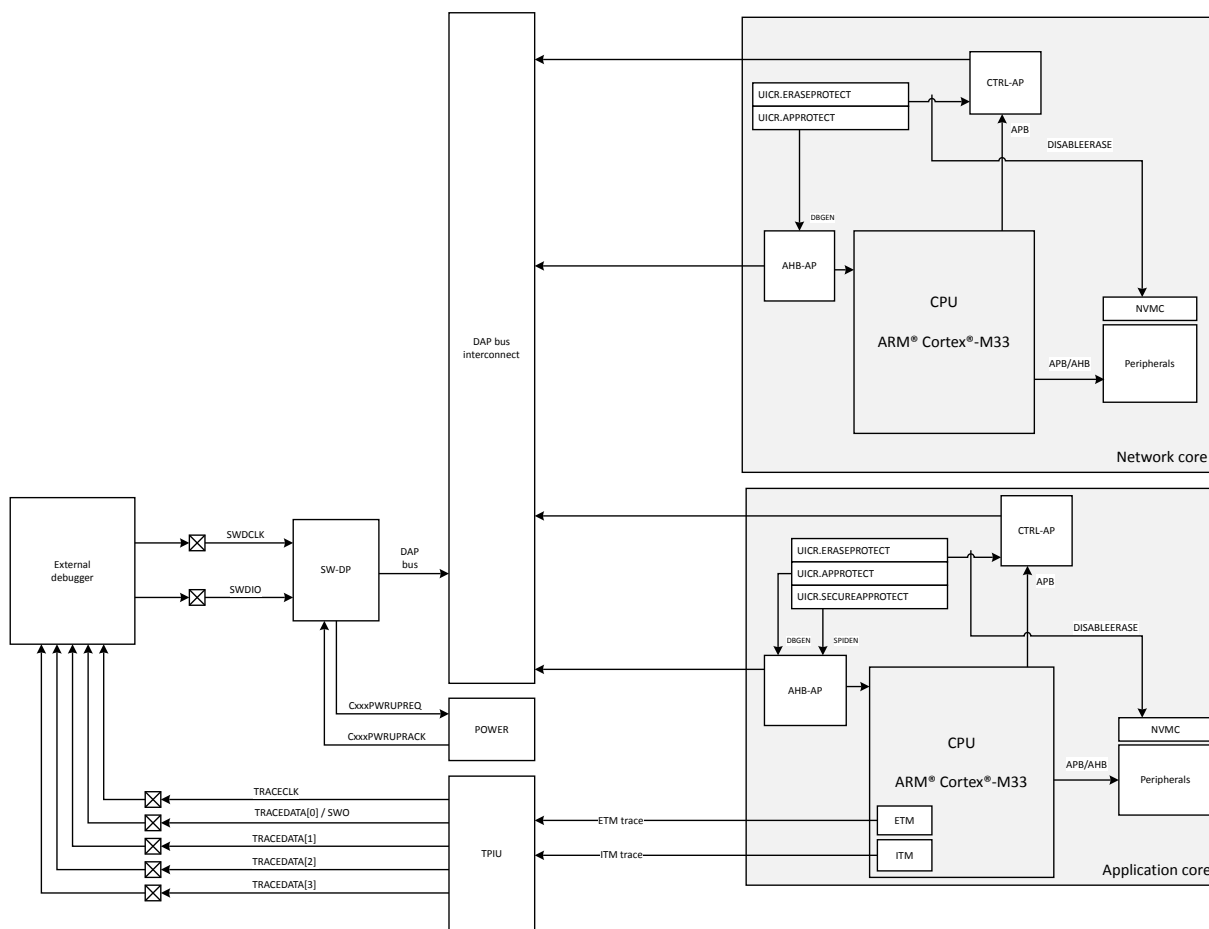


Figure 238: Debug and trace overview

The main features of the debug and trace system are:

- Access port connection to application core ARM Cortex-M33
  - Eight breakpoints
  - Four watchpoint comparators
  - Instrumentation trace macrocell (ITM)
  - Embedded trace macrocell (ETM)
  - Access protection through APPROTECT, ERASEPROTECT and SECUREAPPROTECT
- Access port connection to network core ARM Cortex-M33
  - Eight breakpoints
  - Four watchpoints
  - Access protection through APPROTECT and ERASEPROTECT
- Serial wire debug (SWD) interface, protocol version 2 with multidrop support
- Trace port interface unit (TPIU)

- 4-bit parallel trace of ITM and ETM trace data
- Serial wire output (SWO) trace of ITM data

### 8.1.1 DAP - Debug access port

An external debugger can access the device via the debug access port (DAP).

The DAP implements a standard ARM CoreSight serial wire debug port (SW-DP). The SW-DP implements the serial wire debug (SWD) protocol that is a two-pin serial interface, see SWDCLK and SWDIO in figure [Figure 238: Debug and trace overview](#) on page 730.

**Note:**

- The SWDIO line has an internal pull-up resistor.
- The SWDCLK line has an internal pull-down resistor.

There are several access ports that connect to different parts of the system. An overview is given in the table below.

| AP ID | Type    | Description                               |
|-------|---------|-------------------------------------------|
| 0     | AHB-AP  | Application subsystem access port         |
| 1     | AHB-AP  | Network subsystem access port             |
| 2     | CTRL-AP | Application subsystem control access port |
| 3     | CTRL-AP | Network subsystem control access port     |

Table 186: Access port overview

The AHB-AP and APB-AP are standard ARM components, and documented in *ARM CoreSight SoC-400 Technical Reference Manual*, revision r3p2. The control access port (CTRL-AP) is proprietary, and described in more detail in [CTRL-AP - Control access port](#) on page 739.

### 8.1.2 Access port protection

Debugger transactions through an access port can be protected in different ways.

An overview of the access port protection schemes is given in the table below.

| Register                         | Description                                                                                                                                                                                                                                                                                                                                            |
|----------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Application UICR.APPROTECT       | Blocks all access through the application AHB-AP. This can be used to provide read-back protection of the application. Note that the network core may be able to access non-secure memory of the application core as defined in <a href="#">SPU — System protection unit</a> on page 568. This can be prevented by using the network core's APPROTECT. |
| Application UICR.SECUREAPPROTECT | Blocks all secure transfers through the application AHB-AP. This means that only the non-secure code can be debugged and accessed.                                                                                                                                                                                                                     |
| Application UICR.ERASEPROTECT    | Disables the application core CTRL-AP.ERASEALL and NVMC ERASEALL functionality. This can be used together with APPROTECT to provide read-back and re-purposing protection.                                                                                                                                                                             |
| Network UICR.APPROTECT           | Blocks all access through the network AHB-AP.                                                                                                                                                                                                                                                                                                          |
| Network UICR.ERASEPROTECT        | Disables the network core CTRL-AP.ERASEALL and NVMC ERASEALL functionality. This can be used together with APPROTECT to provide read-back and re-purposing protection.                                                                                                                                                                                 |

Table 187: Access port protection overview

### 8.1.3 Debug interface mode

Before the external debugger can access any of the access ports, the debugger must first request the device to power up via CxxxPWRUPREQ in the SWJ-DP.

As long as the debugger is requesting power via CxxxPWRUPREQ, the device will be in debug interface mode. Otherwise, the device is in normal mode. When a debug session is over, the external debugger must make sure to put the device back into normal mode and then a pin reset should be performed. The reason is that the overall power consumption is higher in debug interface mode compared to normal mode.

Some peripherals behave differently in debug interface mode compared to normal mode. These differences are described in more detail in the chapters of the peripherals that are affected.

For details on how to use the debug capabilities, read the debug documentation of your IDE.

If the device is in System OFF when power is requested via CxxxPWRUPREQ, the system will wake up and the DIF flag in [RESETREAS](#) on page 59 will be set.

### 8.1.4 Real-time debug

The device supports real-time debugging, which allows interrupts to execute to completion in real time when breakpoints are set in thread mode or lower priority interrupts.

Real-time debugging enables the developer to set a breakpoint and single-step through their code without a failure of the real-time event-driven threads running at higher priority. For example, this enables the device to continue to service the high-priority interrupts of an external controller or sensor without failure or loss of state synchronization while the developer steps through code in a low-priority thread.

### 8.1.5 ROM tables

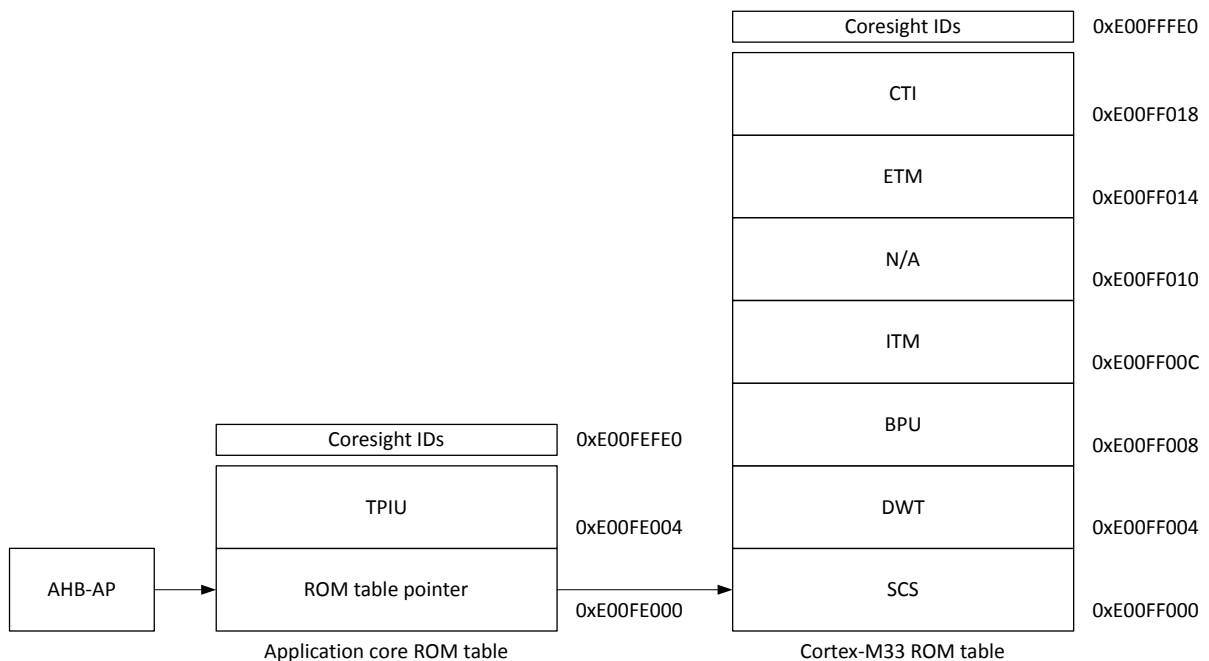


Figure 239: Application core ROM table overview



| Address    | Component | Value                                                           |
|------------|-----------|-----------------------------------------------------------------|
| 0xE00FEFFC | CIDR3     | 0x000000B1                                                      |
| 0xE00FEFF8 | CIDR2     | 0x00000005                                                      |
| 0xE00FEFF4 | CIDR1     | 0x00000010                                                      |
| 0xE00FEFF0 | CIDR0     | 0x0000000D                                                      |
| 0xE00FEFDC | PIDR7     | 0x00000000                                                      |
| 0xE00FEFD8 | PIDR6     | 0x00000000                                                      |
| 0xE00FEFD4 | PIDR5     | 0x00000000                                                      |
| 0xE00FEFD0 | PIDR4     | 0x00000002                                                      |
| 0xE00FEFEC | PIDR3     | 0x00000000                                                      |
| 0xE00FEFE8 | PIDR2     | 1. 0x0000002C nRF5340 limited sampling<br>2. 0x0000003C nRF5340 |
| 0xE00FEFE4 | PIDR1     | 0x00000040                                                      |
| 0xE00FEFE0 | PIDR0     | 0x00000007                                                      |
| 0xE00FEFCC | MEMTYPE   | 0x00000001                                                      |
| 0xE00FE004 | TPIU      | 0xFFFF42003                                                     |
| 0xE00FE000 | ROM table | 0x00001003                                                      |

Table 188: Application core ROM table entries

| Address    | Component             | Value       |
|------------|-----------------------|-------------|
| 0xE00FF01C | MTB (not implemented) | 0xFFFF44002 |
| 0xE00FF018 | CTI                   | 0xFFFF43003 |
| 0xE00FF014 | ETM                   | 0xFFFF42003 |
| 0xE00FF00C | ITM                   | 0xFFFF01003 |
| 0xE00FF008 | BPU                   | 0xFFFF03003 |
| 0xE00FF004 | DWT                   | 0xFFFF02003 |
| 0xE00FF000 | SCS                   | 0xFFFF0F003 |

Table 189: Application ARM Cortex-M33 ROM table entries

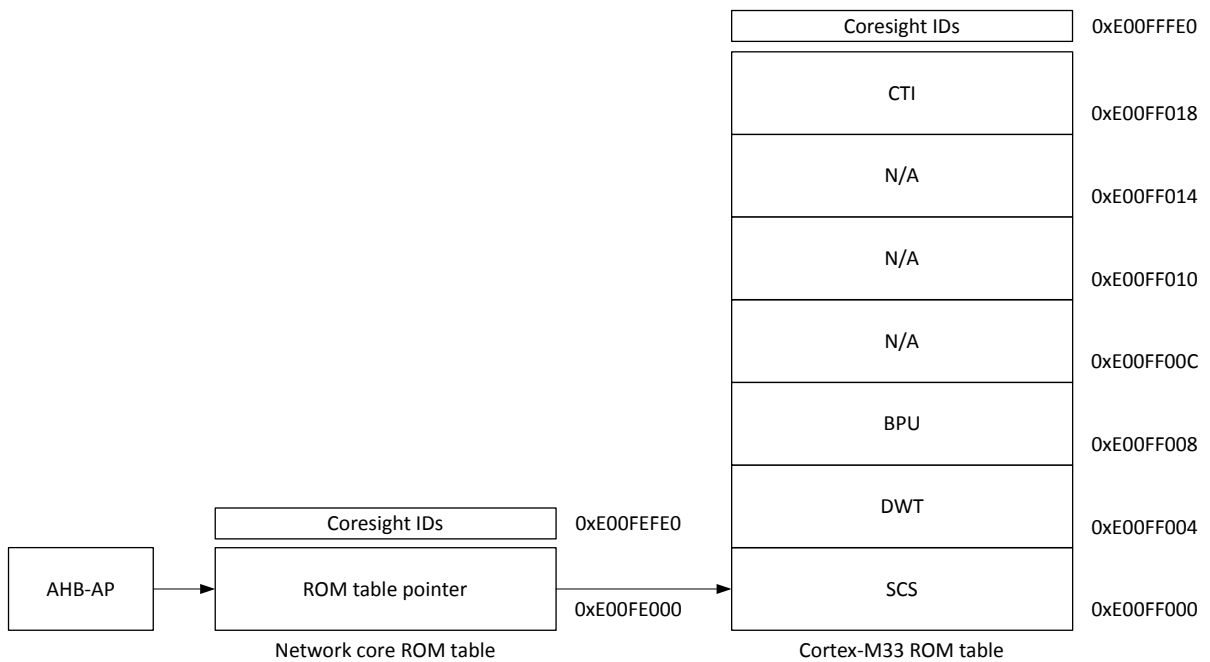


Figure 240: Network core ROM table overview

| Address    | Component | Value                                                               |
|------------|-----------|---------------------------------------------------------------------|
| 0xE00EFFF8 | CIDR3     | 0x000000B1                                                          |
| 0xE00EFFF4 | CIDR2     | 0x00000005                                                          |
| 0xE00EFFF0 | CIDR1     | 0x00000010                                                          |
| 0xE00EFFF0 | CIDR0     | 0x0000000D                                                          |
| 0xE00FEFDC | PIDR7     | 0x00000000                                                          |
| 0xE00FEFD8 | PIDR6     | 0x00000000                                                          |
| 0xE00FEFD4 | PIDR5     | 0x00000000                                                          |
| 0xE00FEFD0 | PIDR4     | 0x00000002                                                          |
| 0xE00FEFEC | PIDR3     | 0x00000000                                                          |
| 0xE00FEFE8 | PIDR2     | 1. 0x0000002C - nRF5340 limited sampling<br>2. 0x0000003C - nRF5340 |
| 0xE00FEFE4 | PIDR1     | 0x00000040                                                          |
| 0xE00FEFE0 | PIDR0     | 0x00000007                                                          |
| 0xE00FEFCC | MEMTYPE   | 0x00000001                                                          |
| 0xE00FE000 | ROM table | 0x00001003                                                          |

Table 190: Network core ROM table entries

| Address    | Component             | Value       |
|------------|-----------------------|-------------|
| 0xE00FF01C | MTB (not implemented) | 0xFFFF4402  |
| 0xE00FF018 | CTI                   | 0xFFFF43003 |
| 0xE00FF014 | ETM (not implemented) | 0xFFFF42002 |
| 0xE00FF00C | ITM (not implemented) | 0xFFFF01002 |
| 0xE00FF008 | BPU                   | 0xFFFF03003 |
| 0xE00FF004 | DWT                   | 0xFFFF02003 |
| 0xE00FF000 | SCS                   | 0xFFFF0F003 |

Table 191: Network ARM Cortex-M33 ROM table entries

### 8.1.6 Cross-trigger network

The debug system features a cross-trigger network that can be used for simultaneous starting and halting of the cores in the system. An overview of the cross-trigger connections is given in figure below.

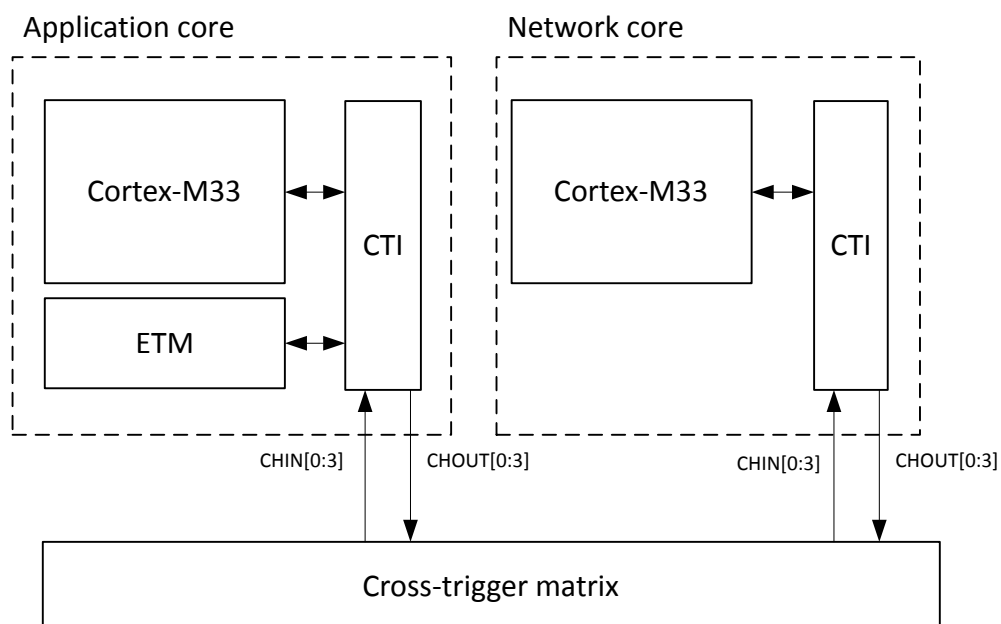


Figure 241: Cross-trigger network overview

Both the application and network core have a cross-trigger interface (CTI) peripheral that can trigger, or get triggered, by signals in the processor or debug blocks. The CTI can be configured to route trigger in-signals to trigger out-signals within the CTI or the cross-trigger matrix. The cross-trigger matrix has four channels in total that can be used to communicate trigger signals between cores.

It is possible to halt the network core when the application is halted (either because of a breakpoint or a stopped debug session). This can be done in the following way:

1. Configure application CTI to generate an event on channel 0 for CTITRIGIN[0] (processor halted) using CTIINEN[0].
2. Configure network CTI to trigger CTITRIGOUT[0] (processor debug request) on channel 0 using CTIOUTEN[0].

### Configuring the cross-trigger interface

In this example, the following CTI channels are used:

- Channel 0 is used to relay debug requests from the application to the network domain.
- Channel 1 is used to relay debug requests from the network to the application domain.
- Channel 2 is used by the debugger to send a common trigger for restarting both domains after a breakpoint.

For the application core, add the following code:

```
#define CTI_TRIGIN_CPUHALTED    0
#define CTI_TRIGOUT_DEBUGREQ    0
#define CTI_TRIGOUT_CPURESTART  1
...
// Enable global CTI routing
NRF_CTI_S->CTICONTROL = CTI_CTICONTROL_GLBEN_Enabled;
// Connect the CPU halted trigger of this domain to debug request of the other domain
NRF_CTI_S->CTIINEN[CTI_TRIGIN_CPUHALTED]    = CTI_CTIINEN_TRIGINEN_0_Msk;
NRF_CTI_S->CTIOUTEN[CTI_TRIGOUT_DEBUGREQ]    = CTI_CTIOUTEN_TRIGOUTEN_1_Msk;
NRF_CTI_S->CTIOUTEN[CTI_TRIGOUT_CPURESTART] = CTI_CTIOUTEN_TRIGOUTEN_2_Msk;
```

For the network core, add the following code:

```
#define CTI_TRIGIN_CPUHALTED    0
#define CTI_TRIGOUT_DEBUGREQ    0
#define CTI_TRIGOUT_CPURESTART  1
...
// Enable global CTI routing
NRF_CTI_NS->CTICONTROL = CTI_CTICONTROL_GLBEN_Enabled;
// Connect the CPU halted trigger of this domain to debug request of the other domain
NRF_CTI_NS->CTIINEN[CTI_TRIGIN_CPUHALTED]    = CTI_CTIINEN_TRIGINEN_1_Msk;
NRF_CTI_NS->CTIOUTEN[CTI_TRIGOUT_DEBUGREQ]    = CTI_CTIOUTEN_TRIGOUTEN_0_Msk;
NRF_CTI_NS->CTIOUTEN[CTI_TRIGOUT_CPURESTART] = CTI_CTIOUTEN_TRIGOUTEN_2_Msk;
```

For more information about the trigger connections to and from the CTI, see the tables below.

| Signal       | Description             |
|--------------|-------------------------|
| CTITRIGIN[0] | Processor halted        |
| CTITRIGIN[1] | DWT comparator output 0 |
| CTITRIGIN[2] | DWT comparator output 1 |
| CTITRIGIN[3] | DWT comparator output 2 |
| CTITRIGIN[4] | ETM event output 0      |
| CTITRIGIN[5] | ETM event output 1      |

Table 192: Application core triggers to CTI

| Signal        | Description             |
|---------------|-------------------------|
| CTITRIGOUT[0] | Processor debug request |
| CTITRIGOUT[1] | Processor restart       |
| CTITRIGOUT[2] | N/A                     |
| CTITRIGOUT[3] | N/A                     |
| CTITRIGOUT[4] | ETM event input 0       |
| CTITRIGOUT[5] | ETM event input 1       |
| CTITRIGOUT[6] | ETM event input 2       |
| CTITRIGOUT[7] | ETM event input 3       |

Table 193: Application core triggers from CTI

| Signal       | Description             |
|--------------|-------------------------|
| CTITRIGIN[0] | Processor halted        |
| CTITRIGIN[1] | DWT comparator output 0 |
| CTITRIGIN[2] | DWT comparator output 1 |
| CTITRIGIN[3] | DWT comparator output 2 |

Table 194: Network core triggers to CTI

| Signal        | Description             |
|---------------|-------------------------|
| CTITRIGOUT[0] | Processor debug request |
| CTITRIGOUT[1] | Processor restart       |

Table 195: Network core triggers from CTI

## 8.1.7 Multidrop SWD

Multidrop SWD allows simultaneous access to an unlimited number of devices through a single connection. This is useful for connectivity-constrained products that contain multiple chips with multidrop support.

In order to select a target in a multidrop capable product, the debugger must write the correct TINSTANCE, TPARTNO and TDESIGNER fields into the SW-DP TARGETSEL register. Values for these fields are located in and fetched from two registers, [TARGETID](#) on page 738 and [DLPIDR](#) on page 738.

For more information about multidrop SWD, see *ARM Debug Interface Architecture Specification*, ADIv5.0 to ADIv5.2.

## 8.1.8 Trace

The device supports ETM and ITM trace.

Trace data from the ETM and the ITM is sent to an external debugger via a 4-bit wide parallel trace port (TPIU), see TRACEDATA[0] through TRACEDATA[3], and TRACECLK in figure [Figure 238: Debug and trace overview](#) on page 730.

In addition to parallel trace, the TPIU supports serial trace via the serial wire output (SWO) trace protocol. Parallel and serial trace cannot be used at the same time. ETM trace is supported in parallel trace mode only, while both parallel and serial trace modes support the ITM trace. For details on how to use the trace capabilities, please read the debug documentation of your IDE.

TPIU's trace pins are multiplexed with GPIOs. SWO and TRACEDATA[0] use the same GPIO. See [Pin assignments](#) on page 764 for more information.

Trace speed is configured in the [TRACEPORTSPEED](#) on page 763 register. The speed of the trace pins depends on the drive setting of the GPIOs that the trace pins are multiplexed with. See [GPIO — General purpose input/output](#) on page 209 for information about how to set drive settings. Only S0S1 and H0H1 drives are suitable for debugging. S0S1 is the default drive at reset. If parallel or serial trace port signals are not fast enough in the debugging conditions, all GPIOs in use for tracing should be set to high drive (H0H1). The user shall make sure that these GPIOs' drive setting is not overwritten by software during the debugging session.

### 8.1.9 Enabling the trace port

A specific sequence of operations must be performed to enable the trace port.

1. Enable the debug master by using the code below.

```
NRF_TAD_S->ENABLE = TAD_ENABLE_ENABLE_Msk;
```

2. Request clock startup.

```
NRF_TAD_S->CLOCKSTART = TAD_CLOCKSTART_START_Msk;
```

3. Configure TPIU port to pads.

```
NRF_TAD_S->PSEL.TRACECLK = TAD_PSEL_TRACECLK_PIN_Traceclk;
NRF_TAD_S->PSEL.TRACEDATA0 = TAD_PSEL_TRACEDATA0_PIN_Tracedata0;
NRF_TAD_S->PSEL.TRACEDATA1 = TAD_PSEL_TRACEDATA1_PIN_Tracedata1;
NRF_TAD_S->PSEL.TRACEDATA2 = TAD_PSEL_TRACEDATA2_PIN_Tracedata2;
NRF_TAD_S->PSEL.TRACEDATA3 = TAD_PSEL_TRACEDATA3_PIN_Tracedata3;
```

4. Hand over control of the GPIO pads to the trace and debug subsystem, and set high drive strength to ensure sufficiently fast operation. Do this for all trace pins that should be used.

```
// Clear the bitfields before configuring to make sure the correct value is written
NRF_P0_S->PIN_CNF[TAD_PSEL_TRACECLK_PIN_Traceclk]
    &= ~(GPIO_PIN_CNF_MCUSEL_Msk | GPIO_PIN_CNF_DRIVE_Msk);
NRF_P0_S->PIN_CNF[TAD_PSEL_TRACECLK_PIN_Traceclk]
    |= (GPIO_PIN_CNF_MCUSEL_TND << GPIO_PIN_CNF_MCUSEL_Pos)
    | (GPIO_PIN_CNF_DRIVE_H0H1 << GPIO_PIN_CNF_DRIVE_Pos);
```

5. Set trace port speed to 64 MHz.

```
NRF_TAD_S->TRACEPORTSPEED = TAD_TRACEPORTSPEED_TRACEPORTSPEED_64MHz;
```

**Note:** Although possible, it is not recommended to run the trace port at less than half the CPU frequency, as it risks dropping some trace packets.

6. Configure ARM CoreSight components (see ARM CoreSight documents for more information).

## 8.1.10 Registers

| Register | Offset | Security | Description                                                                                                                                                                                                                                          |
|----------|--------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TARGETID | 0x042  |          | <p>The TARGETID register provides information about the target when the host is connected to a single device.</p> <p>The TARGETID register is accessed by a read of DP register 0x4 when the DPBANKSEL bit in the SELECT register is set to 0x2.</p> |
| DLPIDR   | 0x043  |          | <p>The DLPIDR register provides information about the serial wire debug protocol version.</p> <p>Accessed by a read of DP register 0x4 when the DPBANKSEL bit in the SELECT register is set to 0x3.</p>                                              |

Table 196: Register overview

### 8.1.10.1 TARGETID

Address offset: 0x042

The TARGETID register provides information about the target when the host is connected to a single device.

The TARGETID register is accessed by a read of DP register 0x4 when the DPBANKSEL bit in the SELECT register is set to 0x2.

|                  |            |            |       |    |    |                                                                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|------------------|------------|------------|-------|----|----|--------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|--|
| Bit number       |            |            | 31    | 30 | 29 | 28                                                                                                           | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |
| ID               |            |            | C     | C  | C  | C                                                                                                            | B  | B  | B  | B  | B  | B  | B  | B  | B  | B  | B  | B  | B  | B  | B  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |  |  |  |  |
| Reset 0x30070289 |            |            | 0     | 0  | 1  | 1                                                                                                            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |  |  |  |  |
| ID               | Acce Field | Value ID   | Value |    |    | Description                                                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| A                | R          | TDESIGNER  |       |    |    | An 11-bit code JEDEC JEP106 continuation code and identity code. The ID identifies the designer of the part. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | NordicSemi | 0x44  |    |    | Nordic Semiconductor ASA.                                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| B                | R          | TPARTNO    |       |    |    | Part number.                                                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | nRF53      | 7     |    |    | nRF53 Series.                                                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
| C                | R          | TREVISION  |       |    |    | Target revision.                                                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | nRF5340LS  | 2     |    |    | nRF5340 limited sampling.                                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |
|                  |            | nRF5340    | 3     |    |    | nRF5340.                                                                                                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |

### 8.1.10.2 DLPIDR

Address offset: 0x043

The DLPIDR register provides information about the serial wire debug protocol version.

Accessed by a read of DP register 0x4 when the DPBANKSEL bit in the SELECT register is set to 0x3.

|                  |            |           |          |    |    |    |       |    |                        |    |                                                   |                   |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-----------|----------|----|----|----|-------|----|------------------------|----|---------------------------------------------------|-------------------|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |           | 31       | 30 | 29 | 28 | 27    | 26 | 25                     | 24 | 23                                                | 22                | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |           | B        | B  | B  | B  |       |    |                        |    |                                                   |                   |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | A | A | A | A |
| Reset 0x00000001 |            |           | 0        | 0  | 0  | 0  | 0     | 0  | 0                      | 0  | 0                                                 | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| ID               | Acce Field |           | Value ID |    |    |    | Value |    |                        |    | Description                                       |                   |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | R          | PROTVSN   |          |    |    |    |       |    |                        |    |                                                   | Protocol version. |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |           | SWDPv2   |    | 1  |    |       |    | SW protocol version 2. |    |                                                   |                   |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| B                | R          | TINSTANCE |          |    |    |    |       |    |                        |    |                                                   | Target instance.  |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |           |          |    |    |    |       |    |                        |    | This value is set by the UICR.TINSTANCE register. |                   |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

## 8.1.11 Electrical specification

### 8.1.11.1 SW-DP

| Symbol       | Description                                       | Min. | Typ. | Max. | Units      |
|--------------|---------------------------------------------------|------|------|------|------------|
| $R_{pull}$   | Internal SWDIO and SWDCLK pull up/down resistance | ..   | ..   | ..   | k $\Omega$ |
| $f_{SWDCLK}$ | SWDCLK frequency                                  | ..   | ..   | ..   | MHz        |

### 8.1.11.2 Trace port

| Symbol    | Description                                                                                                                                                 | Min. | Typ. | Max. | Units |
|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|-------|
| $T_{cyc}$ | Clock period, as defined by ARM in Embedded Trace Macrocell Architecture Specification (see Timing specifications in Trace Port Physical Interface section) | ..   | ..   | ..   | ns    |

## 8.2 CTRL-AP - Control access port

The control access port (CTRL-AP) is a custom access port that enables control of the device when other debug access ports (DAP) have been disabled by the access port protection.

For an overview of the other debug access ports, see [DAP - Debug access port](#) on page 731.

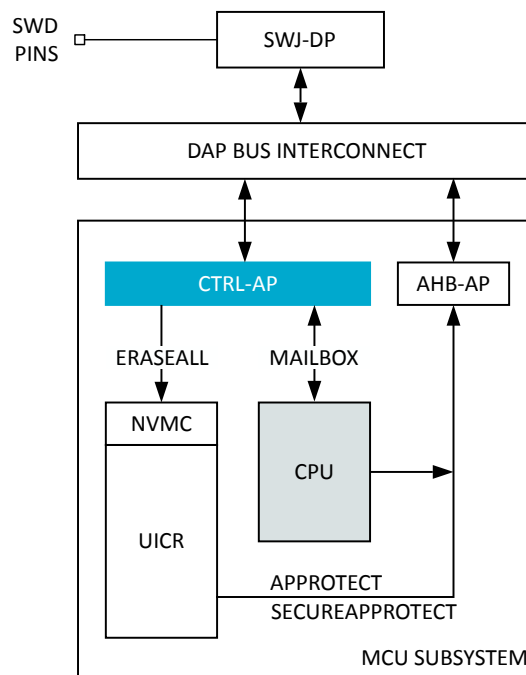


Figure 242: Control access port details

Access port protection (APPROTECT) blocks the debugger access to the AHB-AP, and prevents read and write access to all CPU registers and memory-mapped addresses. It is possible to enable access port protection for both secure and non-secure mode, using registers UICR.SECUREAPPROTECT and UICR.APPROTECT respectively. The debugger can use register [APPROTECT.STATUS](#) on page 743 to read the status of secure and non-secure access port protection.

CTRL-AP has the following features:

- Soft reset
- Erase all

- Mailbox interface
- Debug of protected devices

### 8.2.1 Reset request

The debugger can request the device to perform a soft reset.

Register [RESET](#) on page 742 is used to request the soft reset. Once the soft reset is performed, the reset reason is accessible to on-chip firmware through register [RESETREAS](#). For more information about the soft reset, see [RESET - Reset control](#) on page 55.

### 8.2.2 Erase all

Erase all function gives debugger the possibility of triggering an erase of flash, user information configuration registers (UICR), RAM, including all peripheral settings, as well as removing the access port protection.

To trigger an erase all function, the debugger can write to register [ERASEALL](#) on page 743. Register [ERASEALLSTATUS](#) on page 743 will read as busy for the duration of the operation. After the next reset, the access port protection is removed.

If the debugger performs an erase all function on a slave MCU, the erase sequence will always erase the application MCU first, independently of how the application is protected, before erasing the slave MCU.

#### Erase all protection

It is possible to prevent debugger from performing an erase all operation by writing to the [UICR.ERASEPROTECT](#) register. Once the register is configured and the device reset, the CTRL-AP [ERASEALL](#) operation is disabled, and all flash write and erase operations are restricted to firmware. In addition, it is still possible to write/erase from debugger as long as [UICR.APPROTECT](#) is not set.

**Note:** Setting [UICR.ERASEPROTECT](#) has no effect on debugger access, only on erase all operation.

Register [ERASEPROTECT.STATUS](#) on page 744 holds the status for erase protection.

### 8.2.3 Mailbox interface

CTRL-AP implements a mailbox interface which enables the CPU to communicate with a debugger over the SWD interface.

The mailbox interface consists of a transmit register [MAILBOX.TXDATA](#) on page 745 with its corresponding status register [MAILBOX.TXSTATUS](#) on page 745, and a receive register [MAILBOX.RXDATA](#) on page 746 with its corresponding status register [MAILBOX.RXSTATUS](#) on page 746. Status bits in registers [TXSTATUS](#)/[RXSTATUS](#) will be set and cleared automatically when registers [TXDATA](#)/[RXDATA](#) are written to and read from, independently of the direction.



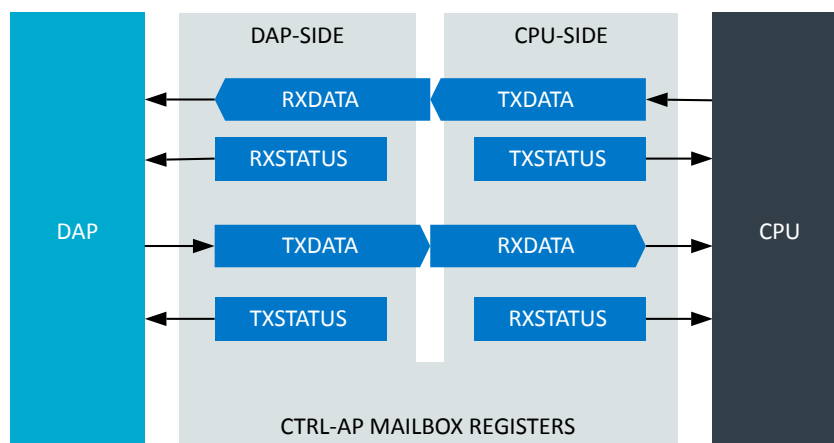


Figure 243: Mailbox register interface

### Mailbox transfer sequence

1. Sender writes TXDATA
2. Hardware sets sender's TXSTATUS to DataPending
3. Hardware sets receiver's RXSTATUS to DataPending
4. Receiver reads RXDATA
5. Hardware sets receiver's RXSTATUS to NoDataPending
6. Hardware sets sender's TXSTATUS to NoDataPending

### 8.2.4 Disabling erase protection

The erase protection mechanism can be disabled in order to return a device to factory default settings upon next reset.

The debugger can read the erase protection status in register [ERASEPROTECT.STATUS](#) on page 744.

If ERASEPROTECT has been enabled, both the debugger and on-chip firmware must write the same non-zero 32-bit KEY value into their respective ERASEPROTECT.DISABLE registers in order to disable the erase protection. As soon as both registers have been written with the same non-zero 32-bit KEY value, the device is automatically erased as described in [Erase all](#) on page 740. The access ports will be re-enabled on next reset once the secure erase sequence has completed.

Write-once register [ERASEPROTECT.LOCK](#) on page 748 should be set to 'Locked' as early as possible in the start-up sequence, preferably as soon as on-chip firmware has determined it does not need to communicate with a debugger over the CTRL-AP mailbox interface. Once written, it will not be possible to remove the erase protection until next reset.

### 8.2.5 Disabling access port protection

The access port protection mechanisms can be temporarily disabled to erase or debug the device.

The debugger can read the access port protection status in register [APPROTECT.STATUS](#) on page 743.

### Disabling non-secure access port protection

If APPROTECT has been enabled from UICR, both the debugger and on-chip firmware must write the same 32-bit KEY value into their respective APPROTECT.DISABLE registers in order to disable the access port protection to non-secure mode. The access port protection remain disabled until a non-equal KEY value is written or until a pin reset is performed, allowing non-secure mode to be debugged through a reset.

Write-once register [APPROTECT.LOCK](#) on page 748 should be set to 'Locked' as early as possible in the start-up sequence, preferably as soon as on-chip firmware has determined it does not need to

communicate with a debugger over the CTRL-AP mailbox interface. Once written, it will not be possible to remove the non-secure mode access port protection until next reset.

## Disabling secure access port protection

If SECUREAPPROTECT has been enabled from UICR, both the debugger and on-chip firmware must write the same 32-bit KEY value into their respective SECUREAPPROTECT.DISABLE registers in order to disable the access port protection to secure mode. The access port protection remain disabled until a non-equal KEY value is written or until a pin reset is performed, allowing secure mode to be debugged through a reset.

Write-once register [SECUREAPPROTECT.LOCK](#) on page 749 should be set to 'Locked' as early as possible in the start-up sequence, preferably as soon as on-chip firmware has determined it does not need to communicate with a debugger over the CTRL-AP mailbox interface. Once written, it will not be possible to remove the secure mode access port protection until next reset.

**Note:** If secure mode debug is enabled, an ERASEALL sequence can also be initiated by writing the same 32-bit KEY value into the respective ERASEPROTECT.DISABLE registers

## 8.2.6 Debugger registers

The CTRL-AP has a set of registers that can only be accessed from the debugger over the SWD interface. These are not accessible from the CPU.

### 8.2.6.1 Registers

| Register                | Offset | Security | Description                                                                                                                                                           |
|-------------------------|--------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RESET                   | 0x000  |          | System reset request.                                                                                                                                                 |
| ERASEALL                | 0x004  |          | Perform a secure erase of the device, where flash, SRAM and UICR will be erased in sequence. The device will be returned to factory default settings upon next reset. |
| ERASEALLSTATUS          | 0x008  |          | Status register for the ERASEALL operation                                                                                                                            |
| APPROTECT.STATUS        | 0x00C  |          | Status register for UICR APPROTECT and SECUREAPPROTECT configuration                                                                                                  |
| APPROTECT.DISABLE       | 0x010  |          | Disable APPROTECT and enable debug access to non-secure mode                                                                                                          |
| SECUREAPPROTECT.DISABLE | 0x014  |          | Disable SECUREAPPROTECT and enable debug access to secure mode                                                                                                        |
| ERASEPROTECT.STATUS     | 0x018  |          | Status register for UICR ERASEPROTECT configuration                                                                                                                   |
| ERASEPROTECT.DISABLE    | 0x01C  |          | Disable ERASEPROTECT and perform ERASEALL                                                                                                                             |
| MAILBOX.TXDATA          | 0x020  |          | Data sent from the debugger to the CPU                                                                                                                                |
| MAILBOX.TXSTATUS        | 0x024  |          | Status to indicate if data sent from the debugger to the CPU has been read                                                                                            |
| MAILBOX.RXDATA          | 0x028  |          | Data sent from the CPU to the debugger                                                                                                                                |
| MAILBOX.RXSTATUS        | 0x02C  |          | Status to indicate if data sent from the CPU to the debugger has been read                                                                                            |
| IDR                     | 0x0FC  |          | CTRL-AP Identification Register, IDR                                                                                                                                  |

Table 197: Register overview

#### 8.2.6.1.1 RESET

Address offset: 0x000

System reset request.

This register is automatically deactivated during ERASEALL operation.

| Bit number       |      |       | 31       | 30 | 29                              | 28 | 27                                    | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |  |
|------------------|------|-------|----------|----|---------------------------------|----|---------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|--|
| ID               |      |       |          |    |                                 |    |                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |  |  |  |
| Reset 0x00000000 |      |       | 0        | 0  | 0                               | 0  | 0                                     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |  |  |  |
| ID               | Acce | Field | Value ID |    | Value                           |    | Description                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
| A                | RW   | RESET |          |    | System reset request and status |    |                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |       | NoReset  |    | 0                               |    | Write to release reset                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |       |          |    |                                 |    | Reading '0' means reset is not active |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |       | Reset    |    | 1                               |    | Write to hold reset                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |      |       |          |    |                                 |    | Reading '1' means reset is active     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |

### 8.2.6.1.2 ERASEALL

Address offset: 0x004

Perform a secure erase of the device, where flash, SRAM and UICR will be erased in sequence. The device will be returned to factory default settings upon next reset.

|                  |            |          |          |             |       |   |  |  |                                           |             |                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|----------|-------------|-------|---|--|--|-------------------------------------------|-------------|----------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          |          |             |       |   |  |  |                                           | 31          | 30                                     | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |          |          |             |       |   |  |  |                                           |             |                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |   |
| Reset 0x00000000 |            |          |          |             |       |   |  |  |                                           | 0           | 0                                      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |          | Value ID |             | Value |   |  |  |                                           | Description |                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | ERASEALL |          |             |       |   |  |  | Return device to factory default settings |             |                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |          |          | NoOperation |       | 0 |  |  |                                           |             | No operation                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |          |          | Erase       |       | 1 |  |  |                                           |             | Erase flash, SRAM and UICR in sequence |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 8.2.6.1.3 ERASEALLSTATUS

Address offset: 0x008

Status register for the ERASEALL operation

|                  |            |                                                                                       |       |                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|---------------------------------------------------------------------------------------|-------|---------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            | A                                                                                     |       |                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |       |                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID                                                                              | Value | Description                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | R          | ERASEALLSTATUS                                                                        |       | Status bit for the ERASEALL operation |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Ready                                                                                 | 0     | ERASEALL is ready                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Busy                                                                                  | 1     | ERASEALL is busy (on-going)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 8.2.6.1.4 APPROTECT.STATUS

Address offset: 0x00C

Status register for UICR APPROTECT and SECUREAPPROTECT configuration



| Bit number       |            |          | 31       | 30 | 29                                                                                      | 28                                                        | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |
|------------------|------------|----------|----------|----|-----------------------------------------------------------------------------------------|-----------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|
| ID               |            |          |          |    |                                                                                         |                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |  |  |
| Reset 0x00000000 |            |          | 0        | 0  | 0                                                                                       | 0                                                         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |
| ID               | Acce Field | Value ID | Value    |    | Description                                                                             |                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
| A                | R          | PALL     |          |    | Status bit for erase protection                                                         |                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            |          |          |    | <div><b>Note:</b> Reset value is auto read from the ERASEPROTECT register in UICR</div> |                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            |          | Enabled  |    | 0                                                                                       | ERASEPROTECT is enabled                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |
|                  |            |          | Disabled |    | 1                                                                                       | ERASEPROTECT is not enabled and ERASEALL can be performed |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |

**Note:** Reset value is auto read from the ERASEPROTECT register in UICR

### 8.2.6.1.8 ERASEPROTECT.DISABLE

Address offset: 0x01C

Disable ERASEPROTECT and perform ERASEALL

|                  |            |          |       |    |    |    |                                                                                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|-------|----|----|----|--------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          | 31    | 30 | 29 | 28 | 27                                                                                                                             | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |          | A     | A  | A  | A  | A                                                                                                                              | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          | 0     | 0  | 0  | 0  | 0                                                                                                                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID | Value |    |    |    | Description                                                                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | KEY      |       |    |    |    | The ERASEALL sequence will be initiated if value of KEY fields are non-zero and KEY fields match on both CPU and debugger side |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 8.2.6.1.9 MAILBOX.TXDATA

Address offset: 0x020

Data sent from the debugger to the CPU

Writing to this register will automatically set field DataPending in register TXSTATUS

|                  |            |  |          |  |       |  |                         |  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|--|-------|--|-------------------------|--|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          |  |       |  |                         |  |             | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |  |          |  |       |  |                         |  |             | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |          |  |       |  |                         |  |             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID |  | Value |  |                         |  | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW Data    |  |          |  |       |  | Data sent from debugger |  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

### 8.2.6.1.10 MAILBOX.TXSTATUS

Address offset: 0x024

Status to indicate if data sent from the debugger to the CPU has been read

|                  |            |        |  |               |  |  |       |  |  |                                    |                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------|--|---------------|--|--|-------|--|--|------------------------------------|-------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |        |  |               |  |  |       |  |  | 31                                 | 30                      | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |        |  |               |  |  |       |  |  |                                    |                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |
| Reset 0x00000000 |            |        |  |               |  |  |       |  |  | 0                                  | 0                       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |        |  | Value ID      |  |  | Value |  |  | Description                        |                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | R          | Status |  |               |  |  |       |  |  |                                    | Status of register DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |        |  | NoDataPending |  |  | 0     |  |  | No data pending in register TXDATA |                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |        |  | DataPending   |  |  | 1     |  |  | Data pending in register TXDATA    |                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 8.2.6.1.11 MAILBOX.RXDATA

Address offset: 0x028

Data sent from the CPU to the debugger

Reading from this register will automatically set field NoDataPending in register RXSTATUS

| Bit number       | 31   | 30    | 29    | 28 | 27    | 26                 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------|------|-------|-------|----|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| ID               | A    | A     | A     | A  | A     | A                  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 | 0    | 0     | 0     | 0  | 0     | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce | Field | Value | ID | Value | Description        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | R    | Data  |       |    |       | Data sent from CPU |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 8.2.6.1.12 MAILBOX.RXSTATUS

Address offset: 0x02C

Status to indicate if data sent from the CPU to the debugger has been read

|                  |      |        |               |       |    |                                    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------|--------|---------------|-------|----|------------------------------------|----|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |      |        |               |       | 31 | 30                                 | 29 | 28          | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |      |        |               |       |    |                                    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |
| Reset 0x00000000 |      |        |               |       | 0  | 0                                  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce |        | Field         | Value | ID | Value                              |    | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | R    | Status |               |       |    | Status of register DATA            |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |        | NoDataPending | 0     |    | No data pending in register RXDATA |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |        | DataPending   | 1     |    | Data pending in register RXDATA    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

### 8.2.6.1.13 IDR

Address offset: 0x0FC

CTRL-AP Identification Register, IDR

| Bit number       | 31   | 30         | 29         | 28 | 27    | 26                             | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------|------|------------|------------|----|-------|--------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| ID               | E    | E          | E          | E  | D     | D                              | D  | D  | C  | C  | C  | C  | C  | C  | B  | B  | B  | B  |    |    |    |    |   |   |   |   | A | A | A | A | A | A |
| Reset 0x12880000 | 0    | 0          | 0          | 1  | 0     | 0                              | 1  | 0  | 1  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce | Field      | Value      | ID | Value | Description                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | R    | APID       |            |    |       | AP Identification              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| B                | R    | CLASS      |            |    |       | Access Port (AP) class         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |            | NotDefined |    | 0x0   | No defined class               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |      |            | MEMAP      |    | 0x8   | Memory Access Port             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| C                | R    | JEP106ID   |            |    |       | JEDEC JEP106 identity code     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| D                | R    | JEP106CONT |            |    |       | JEDEC JEP106 continuation code |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| E                | R    | REVISION   |            |    |       | Revision                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

## 8.2.7 Registers

| Base address | Domain      | Peripheral | Instance    | Secure mapping | DMA security | Description             | Configuration |
|--------------|-------------|------------|-------------|----------------|--------------|-------------------------|---------------|
| 0x50006000   | APPLICATION | CTRLAPPERI | CTRLAP : S  | US             | NSA          | Control access port CPU |               |
| 0x40006000   |             |            | CTRLAP : NS |                |              | side                    |               |
| 0x41006000   | NETWORK     | CTRLAPPERI | CTRLAP      | NS             | NA           | Control access port CPU | side          |

Table 198: Instances

| Register                | Offset | Security | Description                                                                |
|-------------------------|--------|----------|----------------------------------------------------------------------------|
| MAILBOX.RXDATA          | 0x400  |          | Data sent from the debugger to the CPU                                     |
| MAILBOX.RXSTATUS        | 0x404  |          | Status to indicate if data sent from the debugger to the CPU has been read |
| MAILBOX.TXDATA          | 0x480  |          | Data sent from the CPU to the debugger                                     |
| MAILBOX.TXSTATUS        | 0x484  |          | Status to indicate if data sent from the CPU to the debugger has been read |
| ERASEPROTECT.LOCK       | 0x500  |          | Lock register ERASEPROTECT.DISABLE from being written until next reset     |
| ERASEPROTECT.DISABLE    | 0x504  |          | Disable ERASEPROTECT and perform ERASEALL                                  |
| APPROTECT.LOCK          | 0x540  |          | Lock register APPROTECT.DISABLE from being written to until next reset     |
| APPROTECT.DISABLE       | 0x544  |          | Disable APPROTECT and enable debug access to non-secure mode               |
| SECUREAPPROTECT.LOCK    | 0x548  |          | Lock register SECUREAPPROTECT.DISABLE from being written until next reset  |
| SECUREAPPROTECT.DISABLE | 0x54C  |          | Disable SECUREAPPROTECT and enable debug access to secure mode             |
| STATUS                  | 0x600  |          | Status bits for CTRL-AP peripheral                                         |

Table 199: Register overview

### 8.2.7.1 MAILBOX.RXDATA

Address offset: 0x400

Data sent from the debugger to the CPU

Reading from this register will automatically set field NoDataPending in register RXSTATUS

|                  |            |        |          |       |    |    |    |                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------|----------|-------|----|----|----|-----------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |        |          | 31    | 30 | 29 | 28 | 27                          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |        |          | A     | A  | A  | A  | A                           | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |        |          | 0     | 0  | 0  | 0  | 0                           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |        | Value ID | Value |    |    |    | Description                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | R          | RXDATA |          |       |    |    |    | Data received from debugger |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 8.2.7.2 MAILBOX.RXSTATUS

Address offset: 0x404

Status to indicate if data sent from the debugger to the CPU has been read

|                  |      |          |                                                                                       |    |       |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|----------|---------------------------------------------------------------------------------------|----|-------|------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |    |       |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |          | A                                                                                     |    |       |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |      |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |    |       |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field    | Value                                                                                 | ID | Value | Description                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | R    | RXSTATUS |                                                                                       |    |       | Status of data in register RXDATA  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |          | NoDataPending                                                                         |    | 0     | No data pending in register RXDATA |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |          | DataPending                                                                           |    | 1     | Data pending in register RXDATA    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 8.2.7.3 MAILBOX.TXDATA

Address offset: 0x480

Data sent from the CPU to the debugger

Writing to this register will automatically set field DataPending in register TXSTATUS

|                  |            |  |          |       |    |    |    |                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--|----------|-------|----|----|----|-----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |  |          | 31    | 30 | 29 | 28 | 27                    | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |  |          | A     | A  | A  | A  | A                     | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |  |          | 0     | 0  | 0  | 0  | 0                     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |  | Value ID | Value |    |    |    | Description           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW TXDATA  |  |          |       |    |    |    | Data sent to debugger |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 8.2.7.4 MAILBOX.TXSTATUS

Address offset: 0x484

Status to indicate if data sent from the CPU to the debugger has been read

|                  |      |          |               |    |       |                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |
|------------------|------|----------|---------------|----|-------|------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|
| Bit number       |      |          |               | 31 | 30    | 29                                 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |
| ID               |      |          |               |    |       |                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |  |
| Reset 0x00000000 |      |          |               | 0  | 0     | 0                                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |  |
| ID               | Acce | Field    | Value         | ID | Value | Description                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |
| A                | R    | TXSTATUS |               |    |       | Status of data in register TXDATA  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |          | NoDataPending | 0  |       | No data pending in register TXDATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |      |          | DataPending   | 1  |       | Data pending in register TXDATA    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |

### 8.2.7.5 ERASEPROTECT.LOCK

Address offset: 0x500

Lock register ERASEPROTECT.DISABLE from being written until next reset

|                  |            |          |       |                                                                         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|------------------|------------|----------|-------|-------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|
| Bit number       |            |          |       | 31                                                                      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |
| ID               |            |          |       | A                                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
| Reset 0x00000000 |            |          |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
| ID               | Acce Field | Value ID | Value | Description                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
| A                | RW1 LOCK   |          |       | Lock register ERASEPROTECT.DISABLE from being written until next reset  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            | Unlocked | 0     | Register ERASEPROTECT.DISABLE is writeable                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|                  |            | Locked   | 1     | Register ERASEPROTECT.DISABLE is read-only                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |

### 8.2.7.6 ERASEPROTECT.DISABLE

Address offset: 0x504

Disable ERASEPROTECT and perform ERASEALL

|                  |      |       |       |    |       |                                                                                                                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------|-------|-------|----|-------|--------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |      |       |       | 31 | 30    | 29                                                                                                                             | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |      |       |       | A  | A     | A                                                                                                                              | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |      |       |       | 0  | 0     | 0                                                                                                                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce | Field | Value | ID | Value | Description                                                                                                                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW   | KEY   |       |    |       | The ERASEALL sequence will be initiated if value of KEY fields are non-zero and KEY fields match on both CPU and debugger side |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 8.2.7.7 APPROTECT.LOCK

Address offset: 0x540

Lock register APPROTECT.DISABLE from being written to until next reset



| Bit number       |            |          |       | 31                                                                     | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
|------------------|------------|----------|-------|------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| ID               |            |          |       |                                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |
| Reset 0x00000000 |            |          |       | 0                                                                      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |
| ID               | Acce Field | Value ID | Value | Description                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW1 LOCK   |          |       | Lock register APPROTECT.DISABLE from being written to until next reset |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Unlocked | 0     | Register APPROTECT.DISABLE is writeable                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Locked   | 1     | Register APPROTECT.DISABLE is read-only                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

### 8.2.7.8 APPROTECT.DISABLE

Address offset: 0x544

Disable APPROTECT and enable debug access to non-secure mode

|                  |            |          |       |    |    |    |                                                                                                                                                        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|----------|-------|----|----|----|--------------------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |          | 31    | 30 | 29 | 28 | 27                                                                                                                                                     | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ID               |            |          | A     | A  | A  | A  | A                                                                                                                                                      | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            |          | 0     | 0  | 0  | 0  | 0                                                                                                                                                      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID | Value |    |    |    | Description                                                                                                                                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW KEY     |          |       |    |    |    | Disable APPROTECT and enable debug access to non-secure mode until next pin reset if KEY fields match                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |          |       |    |    |    | The current APPROTECT value as configured from UICR is bypassed if value of KEY fields are non-zero and KEY fields match on both CPU and debugger side |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 8.2.7.9 SECUREAPPROTECT.LOCK

Address offset: 0x548

Lock register SECUREAPPROTECT.DISABLE from being written until next reset

|                  |            |  |  |          |    |    |       |    |    |                                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |
|------------------|------------|--|--|----------|----|----|-------|----|----|---------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|
| Bit number       |            |  |  | 31       | 30 | 29 | 28    | 27 | 26 | 25                                                                        | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |
| ID               |            |  |  |          |    |    |       |    |    |                                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A |  |
| Reset 0x00000000 |            |  |  | 0        | 0  | 0  | 0     | 0  | 0  | 0                                                                         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |  |
| ID               | Acce Field |  |  | Value ID |    |    | Value |    |    | Description                                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |
| A                | RW1 LOCK   |  |  |          |    |    |       |    |    | Lock register SECUREAPPROTECT.DISABLE from being written until next reset |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |            |  |  | Unlocked |    |    | 0     |    |    | Register SECUREAPPROTECT.DISABLE is writeable                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |
|                  |            |  |  | Locked   |    |    | 1     |    |    | Register SECUREAPPROTECT.DISABLE is read-only                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |

### 8.2.7.10 SECUREAPPROTECT.DISABLE

Address offset: 0x54C

Disable SECUREAPPROTECT and enable debug access to secure mode

| Bit number       |            | 31       | 30 | 29    | 28 | 27                                                                                                                                                           | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------|------------|----------|----|-------|----|--------------------------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| ID               |            | A        | A  | A     | A  | A                                                                                                                                                            | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A  | A | A | A | A | A | A | A | A | A | A |
| Reset 0x00000000 |            | 0        | 0  | 0     | 0  | 0                                                                                                                                                            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field | Value ID |    | Value |    | Description                                                                                                                                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | RW         | KEY      |    |       |    | Disable SECUREAPPROTECT and enable debug of secure mode until next pin reset if KEY fields match                                                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|                  |            |          |    |       |    | The current SECUREAPPROTECT value as configured from UICR is bypassed if value of KEY fields are non-zero and KEY fields match on both CPU and debugger side |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### 8.2.7.11 STATUS

Address offset: 0x600

### Status bits for CTRL-AP peripheral

| Bit number       |      |                 | 31       | 30 | 29                                                           | 28                                                       | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |   |   |   |
|------------------|------|-----------------|----------|----|--------------------------------------------------------------|----------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|---|---|---|
| ID               |      |                 |          |    |                                                              |                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  | C | B | A |
| Reset 0x00000000 |      |                 | 0        | 0  | 0                                                            | 0                                                        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |   |   |   |
| ID               | Acce | Field           | Value    | ID | Value                                                        | Description                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |   |   |
| A                | R    | DBGIFACEMODE    |          |    |                                                              | Status bit for device debug interface mode               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |   |   |
|                  |      |                 | Disabled | 0  | No debugger attached                                         |                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |   |   |
|                  |      |                 | Enabled  | 1  | Debugger is attached and device is in debug interface mode   |                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |   |   |
| B                | R    | APPROTECT       |          |    |                                                              | Status bit for access port protection in non-secure mode |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |   |   |
|                  |      |                 | Disabled | 0  | Non-secure mode access port protection is currently disabled |                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |   |   |
|                  |      |                 | Enabled  | 1  | Non-secure mode access port protection is currently enabled  |                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |   |   |
| C                | R    | SECUREAPPROTECT |          |    |                                                              | Status bit for access port protection in secure mode     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |   |   |
|                  |      |                 | Disabled | 0  | Secure mode access port protection is currently disabled     |                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |   |   |
|                  |      |                 | Enabled  | 1  | Secure mode access port protection is currently enabled      |                                                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |   |   |   |

### 8.3 CTI - Cross Trigger Interface

## Configuration interface for the Cross Trigger Interface

Please refer to the [CTI](#) section for more information about how to configure the Cross Trigger Interface.

### 8.3.1 Registers

| Base address | Domain      | Peripheral | Instance | Secure mapping | DMA security | Description             | Configuration        |
|--------------|-------------|------------|----------|----------------|--------------|-------------------------|----------------------|
| 0xE0042000   | APPLICATION | CTI        | CTI      | S              | NA           | Cross-trigger interface | Application core CTI |
| 0xE0042000   | NETWORK     | CTI        | CTI      | NS             | NA           | Cross-trigger interface | Network core CTI     |

Table 200: Instances

| Register    | Offset | Security | Description                            |
|-------------|--------|----------|----------------------------------------|
| CTICONTROL  | 0x000  |          | CTI Control register                   |
| CTIINTACK   | 0x010  |          | CTI Interrupt Acknowledge register     |
| CTIAPPSET   | 0x014  |          | CTI Application Trigger Set register   |
| CTIAPPCLEAR | 0x018  |          | CTI Application Trigger Clear register |
| CTIAPPULSE  | 0x01C  |          | CTI Application Pulse register         |

| Register         | Offset | Security | Description                            |
|------------------|--------|----------|----------------------------------------|
| CTIINEN[n]       | 0x020  |          | CTI Trigger to Channel Enable register |
| CTIOUTEN[n]      | 0x0A0  |          | CTI Channel to Trigger Enable register |
| CTITRIGINSTATUS  | 0x130  |          | CTI Trigger In Status register         |
| CTITRIGOUTSTATUS | 0x134  |          | CTI Trigger Out Status register        |
| CTICHINSTATUS    | 0x138  |          | CTI Channel In Status register         |
| CTIGATE          | 0x140  |          | Enable CTI Channel Gate register       |
| DEVARCH          | 0xFBC  |          | Device Architecture register           |
| DEVID            | 0xFC8  |          | Device Configuration register          |
| DEVTYPE          | 0xFCC  |          | Device Type Identifier register        |
| PIDR4            | 0xFD0  |          | Peripheral ID4 Register                |
| PIDR5            | 0xFD4  |          | Peripheral ID5 register                |
| PIDR6            | 0xFD8  |          | Peripheral ID6 register                |
| PIDR7            | 0xFDC  |          | Peripheral ID7 register                |
| PIDR0            | 0xFE0  |          | Peripheral ID0 Register                |
| PIDR1            | 0xFE4  |          | Peripheral ID1 Register                |
| PIDR2            | 0xFE8  |          | Peripheral ID2 Register                |
| PIDR3            | 0xFEC  |          | Peripheral ID3 Register                |
| CIDR0            | 0xFF0  |          | Component ID0 Register                 |
| CIDR1            | 0xFF4  |          | Component ID1 Register                 |
| CIDR2            | 0xFF8  |          | Component ID2 Register                 |
| CIDR3            | 0xFFC  |          | Component ID3 Register                 |

Table 201: Register overview

### 8.3.1.1 CTICONTROL

Address offset: 0x000

CTI Control register

The CTICONTROL register enables the CTI.

|                  |            |          |                                                                                       |                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|---------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          | A                                                                                     |                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW GLBEN   |          |                                                                                       | Enables or disables the CTI                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled | 0                                                                                     | All cross-triggering mapping logic functionality is disabled. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled  | 1                                                                                     | Cross-triggering mapping logic functionality is enabled.      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 8.3.1.2 CTIINTACK

Address offset: 0x010

CTI Interrupt Acknowledge register

The CTIINTACK register is a software acknowledge for a trigger output. This register is used when **ctitrigout** is used as a sticky output. That is, no hardware acknowledge is available and software acknowledge is required.

|                  |            |                    |          |   |       |  |             |                                       |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------------------|----------|---|-------|--|-------------|---------------------------------------|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                    |          |   |       |  |             |                                       |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |                    |          |   |       |  |             |                                       |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | H  | G  | F | E | D | C | B | A |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |                    |          |   |       |  |             |                                       |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |                    | Value ID |   | Value |  | Description |                                       |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A-H              | W          | INTACK[i] (i=0..7) |          |   |       |  |             | Acknowledges the ctitrigout i output. |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Acknowledge        |          | 1 |       |  |             | Clears the ctitrigout                 |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 8.3.1.3 CTIAPPSET

Address offset: 0x014

CTI Application Trigger Set register

Writing to the CTIAPPSET register causes a channel event to be raised, corresponding to the bit written to.

|                  |            |                    |                                                                                       |                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|--------------------|---------------------------------------------------------------------------------------|-----------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |                    | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |                    | D C B A                                                                               |                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |                    | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                   |                                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID           | Value                                                                                 | Description                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A-D              | RW         | APPSET[i] (i=0..3) |                                                                                       | Application trigger event for channel i |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Inactive           | 0                                                                                     | Application trigger i is inactive.      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Active             | 1                                                                                     | Application trigger i is active.        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Activate           | 1                                                                                     | Generate channel event for channel i.   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 8.3.1.4 CTIAPPCLEAR

Address offset: 0x018

CTI Application Trigger Clear register

Writing to a bit in the CTIAPPCLEAR register clears the corresponding channel event.

|                  |            |                      |       |                                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------------------|-------|-------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |                      |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |                      |       | D C B A                                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |                      |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID             | Value | Description                                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A-D              | W          | APPCLEAR[i] (i=0..3) |       | Sets the corresponding bits in the CTIAPPSET to 0. There is one bit of the register for each channel. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Clear                | 1     | Clears the event for channel i                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 8.3.1.5 CTIAPPPULSE

Address offset: 0x01C

CTI Application Pulse register

A write to this register causes a channel event pulse, one ctick period, to be generated, corresponding to the bit written to. The pulse external to the CTI can be extended to multi-cycle by the handshaking interface circuits. This register clears itself immediately, so it can be repeatedly written to without software having to clear it.

|                  |            |                     |                                                                                       |                                                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|---------------------|---------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |                     | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |                     | D C B A                                                                               |                                                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |                     | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID            | Value                                                                                 | Description                                                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A-D              | W          | APPULSE[i] (i=0..3) |                                                                                       | Setting a bit HIGH generates a channel event pulse for the selected channel. There is one bit of the register for each channel. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Generate            | 1                                                                                     | Generates an event pulse on channel i                                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 8.3.1.6 CTIINEN[n] (n=0..7)

Address offset: 0x020 + (n × 0x4)

CTI Trigger to Channel Enable register

The CTIINENn register enables the signaling of an event on CTM channels when a trigger event is received by the CTI. There is a bit for each of the four channels implemented. This register does not affect the application trigger operations.

|                  |            |                      |       |                                                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------------------|-------|--------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |                      |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |                      |       | D C B A                                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |                      |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID             | Value | Description                                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A-D              | RW         | TRIGINEN[i] (i=0..3) |       | Enables a cross trigger event to channel i when a ctitrigin input is activated             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disabled             | 0     | Input trigger n events are ignored by channel i                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Enabled              | 1     | When an event is received on input trigger n (ctitrigin[n]) generate an event on channel i |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 8.3.1.7 CTIOUTEN[n] (n=0..7)

Address offset: 0x0A0 + (n × 0x4)

CTI Channel to Trigger Enable register

The CTIOUTENn register defines which channels can generate a ctitrigin[n] output. There is a bit for each of the four channels implemented. This register affects the mapping from application trigger to trigger outputs.

|                  |            |                       |       |                                                                                          |                                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-----------------------|-------|------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                       |       | 31                                                                                       | 30                                                                              | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |
| ID               |            |                       |       |                                                                                          |                                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | D | C | B | A |
| Reset 0x00000000 |            |                       |       | 0                                                                                        | 0                                                                               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |   |
| ID               | Acce Field | Value ID              | Value | Description                                                                              |                                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A-D              | RW         | TRIGOUTEN[i] (i=0..3) |       |                                                                                          | Enables a cross trigger event to ctitrigout when channel i<br>when is activated |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled              | 0     | Channel i is ignored by output trigger n                                                 |                                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled               | 1     | When an event occur on channel i, generate an event on<br>output event n (ctitrigout[n]) |                                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 8.3.1.8 CTITRIGINSTATUS

Address offset: 0x130

CTI Trigger In Status register

The CTITRIGINSTATUS register provides the status of the ctitrigin inputs.

|                  |  |  |  |  |  |  |  |  |  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          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| Bit number       |  |  |  |  |  |  |  |  |  | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |  |  |  |  |  |  |  |  |  | H G F E D C B A                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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### 8.3.1.9 CTTRIGOUTSTATUS

Address offset: 0x134

CTI Trigger Out Status register

The CTTRIGOUTSTATUS register provides the status of the cttrigout outputs.

|                  |            |                  |          |   |       |                                       |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|------------------|----------|---|-------|---------------------------------------|-------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                  |          |   |       |                                       |             |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |
| ID               |            |                  |          |   |       |                                       |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | H  | G  | F | E | D | C | B | A |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000000 |            |                  |          |   |       |                                       |             |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |                  | Value ID |   | Value |                                       | Description |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A-H              | R          | TRIGOUTSTATUS[i] |          |   |       | Shows the status of cttrigouti output |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | (i=0..7)         |          |   |       |                                       |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |                  | Active   | 1 |       | Cttrigout i is active                 |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |                  | Inactive | 0 |       | Cttrigout i is inactive               |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 8.3.1.10 CTICHINSTATUS

Address offset: 0x138

CTI Channel In Status register

The CTICHINSTATUS register provides the status of the ctichin inputs.

|                  |            |                              |       |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|------------------------------|-------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |                              |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |                              |       | D C B A                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |                              |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID                     | Value | Description                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A-D              | R          | CTICHINSTATUS[i]<br>(i=0..3) |       | Shows the status of the cttrigin i input.                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Active                       | 1     | Ctichin i is active                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Inactive                     | 0     | Ctichin i is inactive                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 8.3.1.11 CTIGATE

Address offset: 0x140

Enable CTI Channel Gate register

The CTIGATE register prevents the channels from propagating through the CTM to other CTIs. This enables local cross-triggering, for example for causing an interrupt when the ETM trigger occurs. It can be used effectively with CTIAPPSET, CTIAPPCLEAR, and CTIAPPULSE for asserting trigger outputs by asserting channels, without affecting the rest of the system. On reset, this register is 0xF, and channel propagation is enabled.

|                  |            |                       |          |   |       |                                        |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|-----------------------|----------|---|-------|----------------------------------------|-------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |                       |          |   |       |                                        |             |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |                       |          |   |       |                                        |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | D | C | B | A |   |   |   |
| Reset 0x0000000F |            |                       |          |   |       |                                        |             |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| ID               | Acce Field |                       | Value ID |   | Value |                                        | Description |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A-D              | RW         | CTIGATEEN[i] (i=0..3) |          |   |       | Enable ctichouti                       |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Enabled               |          | 1 |       | Enable ctichout channel i propagation  |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Disabled              |          | 0 |       | Disable ctichout channel i propagation |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 8.3.1.12 DEVARCH

Address offset: 0xFBC

Device Architecture register

| Bit number       |            | 31           | 30 | 29    | 28 | 27                                   | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------|------------|--------------|----|-------|----|--------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| ID               |            |              |    |       |    |                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | A |
| Reset 0x47701A14 |            | 0            | 1  | 0     | 0  | 0                                    | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| ID               | Acce Field | Value ID     |    | Value |    | Description                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| A                | R          | Architecture |    |       |    | Contains the CTI device architecture |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 8.3.1.13 DEVID

Address offset: 0xFC8

Device Configuration register

The DEVID register indicates the capabilities of the component.

|                  |      |           |  |          |    |       |    |                                                                                                                                                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------|-----------|--|----------|----|-------|----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |      |           |  | 31       | 30 | 29    | 28 | 27                                                                                                                                                                                    | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |      |           |  |          |    |       |    |                                                                                                                                                                                       |    |    |    |    |    |    |    | C  | C  | C  | C  | B  | B  | B  | B  | B  | B  | B | B | B | B |   |   | A | A | A | A |   |
| Reset 0x00040800 |      |           |  | 0        | 0  | 0     | 0  | 0                                                                                                                                                                                     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce | Field     |  | Value ID |    | Value |    | Description                                                                                                                                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | R    | EXTMUXNUM |  |          |    |       |    | Indicates the number of multiplexers available on Trigger Inputs and Trigger Outputs that are using asicctl. The default value of 0b000000 indicates that no multiplexing is present. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| B                | R    | NUMTRIG   |  |          |    |       |    | Number of ECT triggers available                                                                                                                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| C                | R    | NUMCH     |  |          |    |       |    | Number of ECT channels available                                                                                                                                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

### 8.3.1.14 DEVTYPE

Address offset: 0xFCC

Device Type Identifier register

The DEVTYPE register provides a debugger with information about the component when the Part Number field is not recognized. The debugger can then report this information.

| Bit number       |            |              | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                                                                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |
|------------------|------------|--------------|---------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|
| ID               |            |              |                                                                                       |                                                                                                                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | B B B B A A A A |  |  |  |  |  |
| Reset 0x00000014 |            |              | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 0                 |                                                                                                                                                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |
| ID               | Acce Field | Value ID     | Value                                                                                 | Description                                                                                                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |
| A                | R          | MAJOR        |                                                                                       | Major classification of the type of the debug component as specified in the ARM Architecture Specification for this debug and trace component                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |
|                  |            | Controller   | 0b0100                                                                                | Indicates that this component allows a debugger to control other components in a CoreSight SoC-400 system                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |
| B                | R          | SUB          |                                                                                       | Sub-classification of the type of the debug component as specified in the ARM Architecture Specification within the major classification as specified in the MAJOR field. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |
|                  |            | Crosstrigger | 0b0001                                                                                | Indicates that this component is a sub-triggering component                                                                                                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |

### 8.3.1.15 PIDR4

Address offset: 0xFD0

Peripheral ID4 Register

The PIDR4 register is part of the set of peripheral identification registers. Contains part of the designer identity and the memory size.

|                  |      |       |                                                                                       |        |                                                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|------------------|------|-------|---------------------------------------------------------------------------------------|--------|--------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|
| Bit number       |      |       | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |        |                                                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               |      |       |                                                                                       |        |                                                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | B B B B A A A A |  |  |  |  |  |  |  |
| Reset 0x00000004 |      |       | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0                 |        |                                                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| ID               | Acce | Field | Value ID                                                                              | Value  | Description                                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| A                | R    | DES_2 |                                                                                       |        | Together, PIDR1.DES_0, PIDR2.DES_1, and PIDR4.DES_2 identify the designer of the component |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
|                  |      |       | Code                                                                                  | 0b0100 | JEDEC continuation code                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |
| B                | R    | SIZE  |                                                                                       |        | Always 0b0000. Indicates that the device only occupies 4KB of memory                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |

### 8.3.1.16 PIDR5

Address offset: 0xFD4

Peripheral ID5 register

|                  |            |          |                                                                                       |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|-------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          |                                                                                       |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 8.3.1.17 PIDR6

Address offset: 0xFD8

Peripheral ID6 register

|                  |            |          |                                                                                       |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|-------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          |                                                                                       |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                   |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 | Description |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |



### 8.3.1.18 PIDR7

Address offset: 0xFDC

Peripheral ID7 register

|                  |            |  |          |       |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
|------------------|------------|--|----------|-------|----|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|
| Bit number       |            |  |          | 31    | 30 | 29          | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |
| ID               |            |  |          |       |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
| Reset 0x00000000 |            |  |          | 0     | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |
| ID               | Acce Field |  | Value ID | Value |    | Description |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |

### 8.3.1.19 PIDR0

Address offset: 0xFE0

Peripheral ID0 Register

The PIDR0 register is part of the set of peripheral identification registers. Contains part of the designer-specific part number.

|                  |            |        |             |  |                     |                                                         |             |                                                                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|--------|-------------|--|---------------------|---------------------------------------------------------|-------------|--------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |        |             |  | 31                  | 30                                                      | 29          | 28                                                                                                           | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| ID               |            |        |             |  | A A A A A A A A A A |                                                         |             |                                                                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| Reset 0x00000021 |            |        |             |  | 0                   | 0                                                       | 0           | 0                                                                                                            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| ID               | Acce Field |        | Value ID    |  | Value               |                                                         | Description |                                                                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | R          | PART_0 |             |  |                     |                                                         |             | Bits[7:0] of the 12-bit part number of the component. The designer of the component assigns this part number |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |            |        | PartnumberL |  | 0x21                | Indicates bits[7:0] of the part number of the component |             |                                                                                                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

| Bit number       |      |          |        | 31 | 30     | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |                                                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|----------|--------|----|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |      |          |        |    |        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |                                                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x0000000B |      |          |        | 0  | 0      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |  |                                                                                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field    | Value  | ID | Value  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  | Description                                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | R    | DES_1    |        |    |        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  | Together, PIDR1.DES_0, PIDR2.DES_1, and PIDR4.DES_2 identify the designer of the component |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |          | Arm    |    | 0b011  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  | ARM. Bits[6:4] of the JEDEC JEP106 Identity Code                                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | R    | JEDEC    |        |    |        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  | Always 1. Indicates that the JEDEC-assigned designer ID is used                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C                | R    | REVISION |        |    |        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  | Peripheral revision                                                                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |          | Rev0p0 |    | 0b0000 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  | This device is at r0p0                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

|                  |            |        |                                                                                       |  |       |  |                                                                                                                                                                                                                                                                                                                                                                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|--------|---------------------------------------------------------------------------------------|--|-------|--|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |        | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |       |  |                                                                                                                                                                                                                                                                                                                                                                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |        |                                                                                       |  |       |  |                                                                                                                                                                                                                                                                                                                                                                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |        | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0               |  |       |  |                                                                                                                                                                                                                                                                                                                                                                                                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field |        | Value ID                                                                              |  | Value |  | Description                                                                                                                                                                                                                                                                                                                                                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | R          | CMOD   | Unmodified                                                                            |  | 0b000 |  | Customer Modified. Indicates whether the customer has modified the behavior of the component. In most cases, this field is 0b0000. Customers change this value when they make authorized modifications to this component.<br><br>Indicates that the customer has not modified this component                                                                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | R          | REVAND | NoErrata                                                                              |  | 0b000 |  | Indicates minor errata fixes specific to the revision of the component being used, for example metal fixes after implementation. In most cases, this field is 0b0000. ARM recommends that the component designers ensure that a metal fix can change this field if required, for example, by driving it from registers that reset to 0b0000.<br><br>Indicates that there are no errata fixes to this component |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

|                  |            |         |          |      |       |                                                                      |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|---------|----------|------|-------|----------------------------------------------------------------------|-------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |         |          |      |       |                                                                      |             |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |
| ID               |            |         |          |      |       |                                                                      |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A | A | A | A | A | A | A | A |   |   |   |
| Reset 0x0000000D |            |         |          |      |       |                                                                      |             |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| ID               | Acce Field |         | Value ID |      | Value |                                                                      | Description |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | R          | PRMBL_0 |          |      |       | Preamble[0]. Contains bits[7:0] of the component identification code |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Value   |          | 0x0D |       | Bits[7:0] of the identification code                                 |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |

### 8.3.1.24 CIDR1

Address offset: 0xFF4

Component ID1 Register

The CIDR1 register is a component identification register that indicates the presence of identification registers. This register also indicates the component class.

| Bit number       |      |         |           | 31     | 30 | 29                                                                                                                                                                    | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
|------------------|------|---------|-----------|--------|----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| ID               |      |         |           |        |    |                                                                                                                                                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | B | B | B | B | A | A | A | A |   |
| Reset 0x00000090 |      |         |           | 0      | 0  | 0                                                                                                                                                                     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| ID               | Acce | Field   | Value ID  | Value  |    | Description                                                                                                                                                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| A                | R    | PRMBL_1 |           |        |    | Preamble[1]. Contains bits[11:8] of the component identification code                                                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |         | Value     | 0b0000 |    | Bits[11:8] of the identification code                                                                                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| B                | R    | CLASS   |           |        |    | Class of the component, for example, whether the component is a ROM table or a generic CoreSight component. Contains bits[15:12] of the component identification code |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |         | Coresight | 0b1001 |    | Indicates that the component is a CoreSight component                                                                                                                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

### 8.3.1.25 CIDR2

Address offset: 0xFF8

Component ID2 Register

The CIDR2 register is a component identification register that indicates the presence of identification registers.

|                  |            |         |          |      |       |                                        |             |                                                                        |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|---------|----------|------|-------|----------------------------------------|-------------|------------------------------------------------------------------------|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |         |          |      |       |                                        |             |                                                                        |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |         |          |      |       |                                        |             |                                                                        |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | A  | A  | A | A | A | A | A | A | A |   |   |   |   |   |
| Reset 0x00000005 |            |         |          |      |       |                                        |             |                                                                        |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| ID               | Acce Field |         | Value ID |      | Value |                                        | Description |                                                                        |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | R          | PRMBL_2 |          |      |       |                                        |             | Preamble[2]. Contains bits[23:16] of the component identification code |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Value   |          | 0x05 |       | Bits[23:16] of the identification code |             |                                                                        |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 8.3.1.26 CIDR3

Address offset: 0xFFC

Component ID3 Register

The CIDR3 register is a component identification register that indicates the presence of identification registers.

|                  |            |         |          |      |       |                                                                        |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|---------|----------|------|-------|------------------------------------------------------------------------|-------------|--|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |         |          |      |       |                                                                        |             |  |  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |
| ID               |            |         |          |      |       |                                                                        |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | A | A | A | A | A | A | A | A |   |   |   |   |
| Reset 0x000000B1 |            |         |          |      |       |                                                                        |             |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| ID               | Acce Field |         | Value ID |      | Value |                                                                        | Description |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | R          | PRMBL_3 |          |      |       | Preamble[3]. Contains bits[31:24] of the component identification code |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |            | Value   |          | 0xB1 |       | Bits[31:24] of the identification code                                 |             |  |  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

## 8.4 TAD - Trace and debug control

Configuration interface for trace and debug

Please refer to the [Trace](#) section for more information about how to configure the trace and debug interface.

**Note:** Although there are [PSEL](#) registers for the trace port, each function can only be mapped to a single pin due to pin speed requirements. Setting the PIN field to anything else will not have any effect. See [Pin assignment chapter](#) for more information

### 8.4.1 Registers

| Base address | Domain      | Peripheral | Instance | Secure mapping | DMA security | Description             | Configuration |
|--------------|-------------|------------|----------|----------------|--------------|-------------------------|---------------|
| 0xE0080000   | APPLICATION | TAD        | TAD      | S              | NA           | Trace and debug control |               |

Table 202: Instances

| Register        | Offset | Security | Description                                          |
|-----------------|--------|----------|------------------------------------------------------|
| CLOCKSTART      | 0x004  |          | Start all trace and debug clocks.                    |
| CLOCKSTOP       | 0x008  |          | Stop all trace and debug clocks.                     |
| ENABLE          | 0x500  |          | Enable debug domain and aquire selected GPIOs        |
| PSEL.TRACECLK   | 0x504  |          | Pin configuration for TRACECLK                       |
| PSEL.TRACEDATA0 | 0x508  |          | Pin configuration for TRACEDATA[0] and SWO           |
| PSEL.TRACEDATA1 | 0x50C  |          | Pin configuration for TRACEDATA[1]                   |
| PSEL.TRACEDATA2 | 0x510  |          | Pin configuration for TRACEDATA[2]                   |
| PSEL.TRACEDATA3 | 0x514  |          | Pin configuration for TRACEDATA[3]                   |
| TRACEPORTSPEED  | 0x518  |          | Clocking options for the Trace Port debug interface. |

Table 203: Register overview

#### 8.4.1.1 CLOCKSTART

Address offset: 0x004

Start all trace and debug clocks.

|                  |            |          |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |          | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |          | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID | Value                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Description                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | W          | START    | Start                                                                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 1 Start all trace and debug clocks. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 8.4.1.2 CLOCKSTOP

Address offset: 0x008

Stop all trace and debug clocks.

|                  |            |      |  |          |      |  |       |   |  |             |                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|------------|------|--|----------|------|--|-------|---|--|-------------|----------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit number       |            |      |  |          |      |  |       |   |  | 31          | 30                               | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |
| ID               |            |      |  |          |      |  |       |   |  |             |                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | A |   |   |   |
| Reset 0x00000000 |            |      |  |          |      |  |       |   |  | 0           | 0                                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID               | Acce Field |      |  | Value ID |      |  | Value |   |  | Description |                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | W          | STOP |  |          | Stop |  |       | 1 |  |             | Stop all trace and debug clocks. |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |

### 8.4.1.3 ENABLE

Address offset: 0x500

Enable debug domain and aquire selected GPIOs

|                  |            |        |          |  |       |  |                                                 |  |  |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|--------|----------|--|-------|--|-------------------------------------------------|--|--|---------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |            |        |          |  |       |  |                                                 |  |  | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |            |        |          |  |       |  |                                                 |  |  | A                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |        |          |  |       |  |                                                 |  |  | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field |        | Value ID |  | Value |  | Description                                     |  |  |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | ENABLE | DISABLED |  | 0     |  | Disable debug domain and release selected GPIOs |  |  |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            |        | ENABLED  |  | 1     |  | Enable debug domain and aquire selected GPIOs   |  |  |                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 8.4.1.4 PSEL.TRACECLK

Address offset: 0x504

Pin configuration for TRACECLK

| Bit number       |      |         |              | 31    | 30                           | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |
|------------------|------|---------|--------------|-------|------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ID               |      |         |              | B     |                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | A | A | A | A |
| Reset 0xFFFFFFFF |      |         |              | 1     | 1                            | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |   |   |   |   |
| ID               | Acce | Field   | Value ID     | Value | Description                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A                | RW   | PIN     | Traceclk     | 12    | Pin number<br>TRACECLK pin   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |         |              |       | Note: Only this pin is valid |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B                | RW   | CONNECT | Disconnected | 1     | Connection<br>Disconnect     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                  |      |         | Connected    | 0     | Connect                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

**Note:** Only this pin is valid

### 8.4.1.5 PSEL.TRACEDATA0

Address offset: 0x508

Pin configuration for TRACEDATA[0] and SWO

|                  |      |         |              |    |       |    |                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |
|------------------|------|---------|--------------|----|-------|----|------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|--|--|---|--|--|--|---|--|--|--|---|--|--|--|---|--|--|--|---|--|--|--|---|--|--|--|
| Bit number       |      |         | 31           | 30 | 29    | 28 | 27                           | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |
| ID               |      |         | B            |    |       |    |                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | A |   |   |   | A | A | A | A |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |
| Reset 0xFFFFFFFF |      |         | 1            |    |       |    |                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | 1 |   |   |   | 1 |   |   |   | 1 |  |  |  | 1 |  |  |  | 1 |  |  |  | 1 |  |  |  | 1 |  |  |  | 1 |  |  |  | 1 |  |  |  |
| ID               | Acce | Field   | Value ID     |    | Value |    | Description                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |
| A                | RW   | PIN     |              |    |       |    | Pin number                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |
|                  |      |         | Tracedata0   |    | 11    |    | TRACEDATA0/SWO pin           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |
|                  |      |         |              |    |       |    | Note: Only this pin is valid |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |
| B                | RW   | CONNECT |              |    |       |    | Connection                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |
|                  |      |         | Disconnected |    | 1     |    | Disconnect                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |
|                  |      |         | Connected    |    | 0     |    | Connect                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |   |  |  |  |

#### 8.4.1.6 PSEL.TRACEDATA1

Address offset: 0x50C

### Pin configuration for TRACEDATA[1]

|                  |      |         |                                                                                       |    |       |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|---------|---------------------------------------------------------------------------------------|----|-------|------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |         | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |    |       |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |         | B                                                                                     |    |       |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0xFFFFFFFF |      |         | 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1               |    |       |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field   | Value                                                                                 | ID | Value | Description                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW   | PIN     |                                                                                       |    |       | Pin number                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |         | Tracedata1                                                                            | 10 |       | TRACEDATA1 pin               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |         |                                                                                       |    |       | Note: Only this pin is valid |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW   | CONNECT |                                                                                       |    |       | Connection                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |         | Disconnected                                                                          | 1  |       | Disconnect                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |         | Connected                                                                             | 0  |       | Connect                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

#### 8.4.1.7 PSEL.TRACEDATA2

Address offset: 0x510

## Pin configuration for TRACEDATA[2]

|                  |      |         |              |                                                                                       |       |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------|---------|--------------|---------------------------------------------------------------------------------------|-------|------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Bit number       |      |         |              | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |       |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               |      |         |              | B                                                                                     |       |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0xFFFFFFFF |      |         |              | 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1                       |       |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce | Field   | Value        | ID                                                                                    | Value | Description                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW   | PIN     |              |                                                                                       |       | Pin number                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |         | Tracedata2   | 9                                                                                     |       | TRACEDATA2 pin               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |         |              |                                                                                       |       | Note: Only this pin is valid |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW   | CONNECT |              |                                                                                       |       | Connection                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |         | Disconnected | 1                                                                                     |       | Disconnect                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |      |         | Connected    | 0                                                                                     |       | Connect                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

#### 8.4.1.8 PSEL.TRACEDATA3

Address offset: 0x514

### Pin configuration for TRACEDATA[3]

| Bit number       |            |                              | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|------------------------------|---------------------------------------------------------------------------------------|----------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |            |                              | B                                                                                     |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0xFFFFFFFF |            |                              | 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1   |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID                     | Value                                                                                 | Description    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | PIN                          |                                                                                       | Pin number     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Tracedata3                   | 8                                                                                     | TRACEDATA3 pin |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Note: Only this pin is valid |                                                                                       |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B                | RW         | CONNECT                      |                                                                                       | Connection     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Disconnected                 | 1                                                                                     | Disconnect     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | Connected                    | 0                                                                                     | Connect        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

### 8.4.1.9 TRACEPORTSPEED

Address offset: 0x518

Clocking options for the Trace Port debug interface.

This register is a retained register. Reset behavior is the same as debug components.

| Bit number       |            |                | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |                                                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|----------------|---------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| ID               |            |                | A A                                                                                   |                                                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset 0x00000000 |            |                | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0                       |                                                                                                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ID               | Acce Field | Value ID       | Value                                                                                 | Description                                                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A                | RW         | TRACEPORTSPEED |                                                                                       | Speed of Trace Port clock. Note that the TRACECLK pin output will be divided again by two from the Trace Port clock. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | 64MHz          | 0                                                                                     | Trace Port clock is:<br><br>64MHz                                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | 32MHz          | 1                                                                                     | Trace Port clock is:<br><br>32MHz                                                                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | 8MHz           | 2                                                                                     | Trace Port clock is:<br><br>8MHz                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                  |            | 4MHz           | 3                                                                                     | Trace Port clock is:<br><br>4MHz                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

# 9 Hardware and layout

## 9.1 Pin assignments

This section describes the pin assignment and the pin functions.

This device provides flexibility when it comes to routing and configuration of the GPIO pins. However, some pins have recommendations for how the pin should be configured or what it should be used for.

In addition to the information in the pin-out tables for the respective packages, the following peripherals have dedicated pins that should be used for proper operation:

- TWI - In 1 Mbps mode, the two high-speed TWI pins must be configured in the TWI peripheral's PSEL registers
- QSPI - For the fastest QSPI mode, the special purpose GPIO pins are enabled using the PIN\_CNF[p].MCUSEL register
- SPIM2 - For the fastest SPI mode, the special purpose GPIO pins are enabled using the PIN\_CNF[p].MCUSEL register

For all high-speed signals, printed circuit board (PCB) layout must ensure that connections are made using short PCB traces. Refer to the manufacturer's PCB design recommendations for additional information.

### 9.1.1 aQFN94 pin assignments

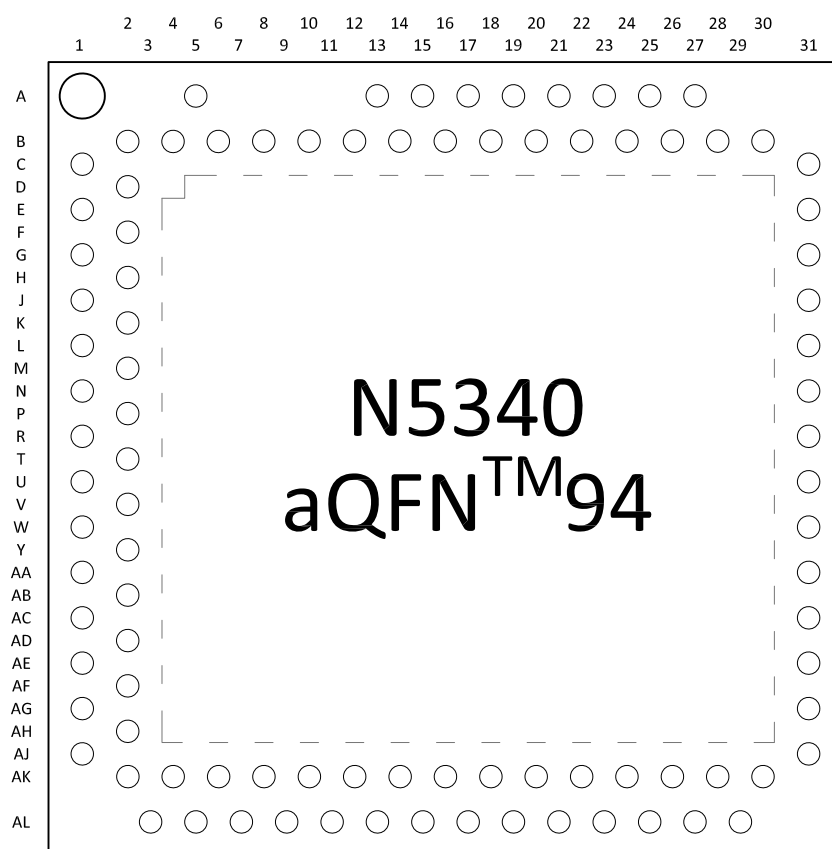


Figure 244: aQFN94 pin assignments, top view



| Pin  | Name   | Function     | Description                                             |
|------|--------|--------------|---------------------------------------------------------|
| A5   | VBUS   | Power        | 5 V input for USB 3.3 V regulator                       |
| A13  | DECA   | Power        | Analog regulator supply decoupling                      |
| A15  | DECD   | Power        | Digital regulator supply decoupling                     |
| A17  | P1.13  | Digital I/O  | General purpose I/O                                     |
| A19  | VDD    | Power        | Power supply                                            |
| A21  | DCCR   | Power        | DC/DC converter output                                  |
| A23  | DECN   | Power        | Regulator supply decoupling                             |
| A27  | DECR   | Power        | Regulator supply decoupling                             |
| B2   | D+     | Digital I/O  | USB D+                                                  |
| B4   | D-     | Digital I/O  | USB D-                                                  |
| B6   | DECUSB | Power        | USB 3.3 V regulator supply decoupling                   |
| B8   | VDD    | Power        | Power supply                                            |
| B10  | DCCD   | Power        | DC/DC converter output                                  |
| B14  | P1.15  | Digital I/O  | General purpose I/O                                     |
| B16  | P1.14  | Digital I/O  | General purpose I/O                                     |
| B18  | P1.12  | Digital I/O  | General purpose I/O                                     |
| B20  | P1.11  | Digital I/O  | General purpose I/O                                     |
| B22  | P0.31  | Digital I/O  | General purpose I/O                                     |
| B24  | P0.30  | Digital I/O  | General purpose I/O                                     |
| B28  | VDD    | Power        | Power supply                                            |
| B30  | XC2    | Analog input | Connection for 32 MHz crystal                           |
| C1   | VDD    | Power        | Power supply                                            |
| C31  | XC1    | Analog input | Connection for 32 MHz crystal                           |
| E1   | VDDH   | Power        | Power supply                                            |
| E31  | VDD    | Power        | Power supply                                            |
| G31  | DECRF  | Power        | RADIO power supply decoupling                           |
| J1   | DCCH   | Power        | DC/DC converter output                                  |
| L1   | VDD    | Power        | Power supply                                            |
| L31  | ANT    | RF           | Single-ended antenna connection                         |
| M2   | P1.00  | Digital I/O  | General purpose I/O                                     |
| N1   | P0.00  | Digital I/O  | General purpose I/O                                     |
|      | XL1    | Analog input | Connection for 32 kHz crystal                           |
| N31  | VDD    | Power        | Power supply                                            |
| P2   | P1.01  | Digital I/O  | General purpose I/O                                     |
| R1   | P0.01  | Digital I/O  | General purpose I/O                                     |
|      | XL2    | Analog input | Connection for 32 kHz crystal                           |
| R31  | P1.10  | Digital I/O  | General purpose I/O                                     |
| U1   | VDD    | Power        | Power supply                                            |
| U31  | P0.29  | Digital I/O  | General purpose I/O                                     |
| V2   | P0.04  | Digital I/O  | General purpose I/O                                     |
|      | AIN0   | Analog input | Analog input                                            |
| W1   | P0.02  | Digital I/O  | General purpose I/O                                     |
|      | NFC1   | NFC input    | NFC antenna connection                                  |
| W31  | SWDCLK | Debug        | Serial wire debug clock input for debug and programming |
| Y2   | P0.05  | Digital I/O  | General purpose I/O                                     |
|      | AIN1   | Analog input | Analog input                                            |
| AA1  | P0.03  | Digital I/O  | General purpose I/O                                     |
|      | NFC2   | NFC input    | NFC antenna connection                                  |
| AA31 | SWDIO  | Debug        | Serial wire debug I/O for debug and programming         |
| AB2  | P0.06  | Digital I/O  | General purpose I/O                                     |
|      | AIN2   | Analog input | Analog input                                            |
| AC1  | VDD    | Power        | Power supply                                            |
| AC31 | nRESET | Reset        | Pin RESET with internal pull-up resistor                |

| Pin  | Name       | Function       | Description                      |
|------|------------|----------------|----------------------------------|
| AD2  | P0.07      | Digital I/O    | General purpose I/O              |
|      | AIN3       | Analog input   | Analog input                     |
| AE1  | P1.02      | Digital I/O    | General purpose I/O              |
|      | TWI        | TWI 1 Mbps     | High-speed pin for 1 Mbps TWI    |
| AE31 | P0.28      | Digital I/O    | General purpose I/O              |
|      | AIN7       | Analog input   | Analog input                     |
| AF2  | P1.03      | Digital I/O    | General purpose I/O              |
|      | TWI        | TWI 1 Mbps     | High-speed pin for 1 Mbps TWI    |
| AG1  | VDD        | Power          | Power supply                     |
| AG31 | DECF       | Power          | Regulator supply decoupling      |
| AH2  | P0.08      | Digital I/O    | General purpose I/O              |
|      | TRACEDATA3 | Trace data     | Trace buffer TRACEDATA[3]        |
|      | SCK        | SCK for SPIM2  | Dedicated pin for high-speed SPI |
| AJ1  | P0.09      | Digital I/O    | General purpose I/O              |
|      | TRACEDATA2 | Trace data     | Trace buffer TRACEDATA[2]        |
|      | MOSI       | MOSI for SPIM2 | Dedicated pin for high-speed SPI |
| AJ31 | VDD        | Power          | Power supply                     |
| AK2  | P0.10      | Digital I/O    | General purpose I/O              |
|      | TRACEDATA1 | Trace data     | Trace buffer TRACEDATA[1]        |
|      | MISO       | MISO for SPIM2 | Dedicated pin for high-speed SPI |
| AK4  | P0.11      | Digital I/O    | General purpose I/O              |
|      | TRACEDATA0 | Trace data     | Trace buffer TRACEDATA[0]        |
| AK6  | P0.12      | Digital I/O    | General purpose I/O              |
|      | TRACECLK   | Trace clock    | Trace buffer clock               |
| AK8  | P0.14      | Digital I/O    | General purpose I/O              |
|      | IO1        | IO1 for QSPI   | Dedicated pin for Quad SPI       |
| AK10 | P0.15      | Digital I/O    | General purpose I/O              |
|      | IO2        | IO2 for QSPI   | Dedicated pin for Quad SPI       |
| AK12 | P0.17      | Digital I/O    | General purpose I/O              |
|      | SCK        | SCK for QSPI   | Dedicated pin for Quad SPI       |
| AK14 | P0.18      | Digital I/O    | General purpose I/O              |
|      | CSN        | CSN for QSPI   | Dedicated pin for Quad SPI       |
| AK16 | P0.20      | Digital I/O    | General purpose I/O              |
| AK18 | P0.22      | Digital I/O    | General purpose I/O              |
| AK20 | P0.23      | Digital I/O    | General purpose I/O              |
| AK22 | P1.05      | Digital I/O    | General purpose I/O              |
| AK24 | P1.07      | Digital I/O    | General purpose I/O              |
| AK26 | P1.09      | Digital I/O    | General purpose I/O              |
| AK28 | P0.25      | Digital I/O    | General purpose I/O              |
|      | AIN4       | Analog input   | Analog input                     |
| AK30 | P0.27      | Digital I/O    | General purpose I/O              |
|      | AIN6       | Analog input   | Analog input                     |
| AL3  | VDD        | Power          | Power supply                     |
| AL5  | P0.13      | Digital I/O    | General purpose I/O              |
|      | IO0        | IO0 for QSPI   | Dedicated pin for Quad SPI       |
| AL7  | VDD        | Power          | Power supply                     |
| AL9  | P0.16      | Digital I/O    | General purpose I/O              |
|      | IO3        | IO3 for QSPI   | Dedicated pin for Quad SPI       |
| AL11 | VDD        | Power          | Power supply                     |
| AL13 | P0.19      | Digital I/O    | General purpose I/O              |
| AL15 | P0.21      | Digital I/O    | General purpose I/O              |
| AL17 | VDD        | Power          | Power supply                     |
| AL19 | P1.04      | Digital I/O    | General purpose I/O              |

| Pin                   | Name  | Function     | Description                                                                                |
|-----------------------|-------|--------------|--------------------------------------------------------------------------------------------|
| AL21                  | P1.06 | Digital I/O  | General purpose I/O                                                                        |
| AL23                  | P1.08 | Digital I/O  | General purpose I/O                                                                        |
| AL25                  | VDD   | Power        | Power supply                                                                               |
| AL27                  | P0.24 | Digital I/O  | General purpose I/O                                                                        |
| AL29                  | P0.26 | Digital I/O  | General purpose I/O                                                                        |
|                       | AIN5  | Analog input | Analog input                                                                               |
| <b>Bottom of chip</b> |       |              |                                                                                            |
| Die pad               | VSS   | Power        | Ground pad. Exposed die pad must be connected to ground (VSS) for proper device operation. |

Table 204: aQFN94 pin assignments

## 9.2 Mechanical specifications

The mechanical specifications for the packages show the dimensions in millimeters.

### 9.2.1 aQFN94 7 x 7 mm package

Dimensions in millimeters for the aQFN94 7 x 7 mm package.

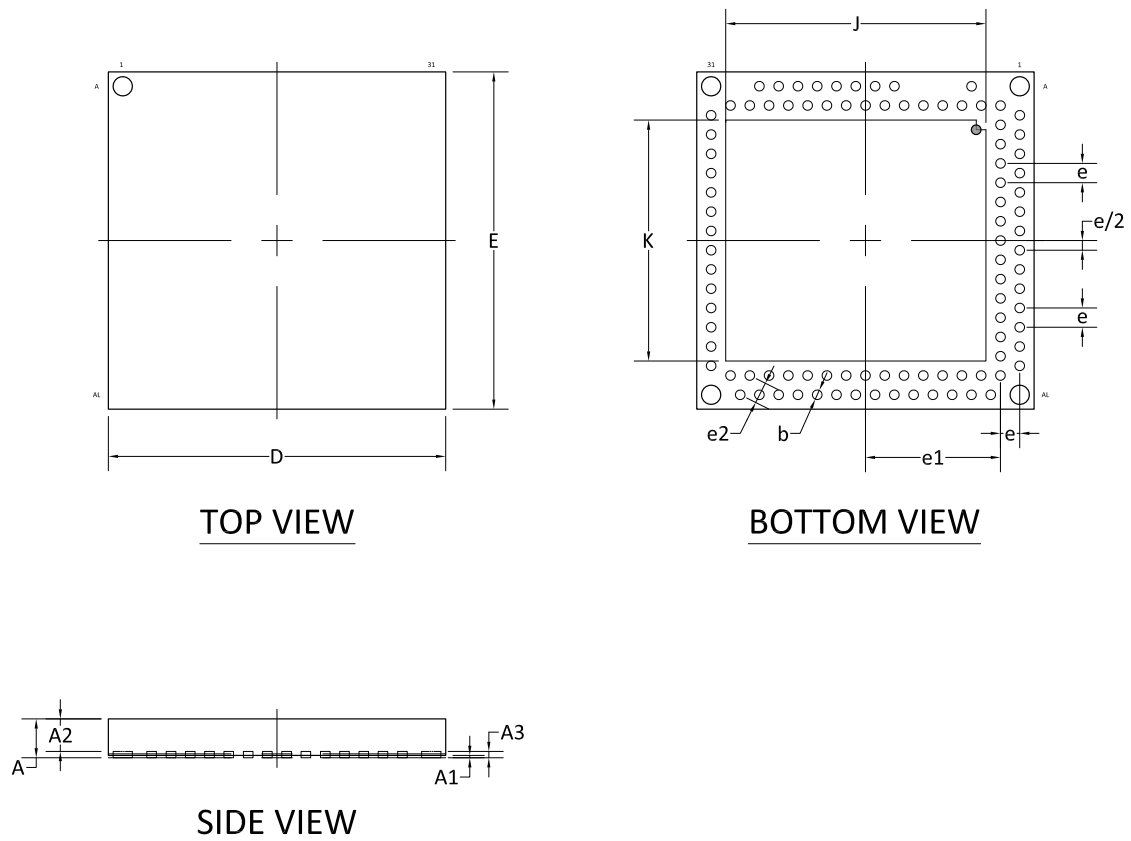


Figure 245: aQFN94 7 x 7 mm package

|                        |   | Symbol | Min   | Nom  | Max  |
|------------------------|---|--------|-------|------|------|
| Total thickness        |   | A      |       |      | 0.85 |
| Stand off              |   | A1     | 0.02  | 0.05 | 0.08 |
| Mold thickness         |   | A2     | 0.675 |      |      |
| L/F thickness          |   | A3     | 0.13  |      |      |
| Lead width             |   | b      | 0.15  | 0.2  | 0.25 |
| Body size              | X | D      | 7.00  |      |      |
|                        | Y | E      | 7.00  |      |      |
| Lead pitch             |   | e      | 0.4   |      |      |
|                        |   | e1     | 2.8   |      |      |
|                        |   | e2     | 0.447 |      |      |
| EP Size                | X | J      | 5.3   | 5.4  | 5.5  |
|                        | Y | K      | 4.9   | 5    | 5.1  |
| Package edge tolerance |   | aaa    | 0.05  |      |      |
| Mold flatness          |   | bbb    | 0.08  |      |      |
| Coplanarity            |   | ccc    | 0.08  |      |      |
| Lead offset            |   | ddd    | 0.08  |      |      |
| Exposed pad offset     |   | eee    | 0.1   |      |      |

Table 205: aQFN94 dimensions in millimeters

## 9.3 Reference circuitry

To ensure good RF performance when designing PCBs, it is highly recommended to use the PCB layouts and component values provided by Nordic Semiconductor.

Documentation for the different package reference circuits, including Altium Designer files, PCB layout files, and PCB production files can be downloaded from [www.nordicsemi.com](http://www.nordicsemi.com).

In this section, there is a reference circuit for QKAA aQFN94, showing the components and component values to support on-chip features in a design.

Some general guidance is summarized here:

- When supplying power from a USB source only, VBUS must be connected to VDDH if USB is to be used.
- Components required for DC/DC function are only needed if DC/DC mode is enabled for that regulator.
- NFC can be used in any configuration.
- USB can be used in any configuration as long as VBUS is supplied by the USB host.
- The schematics include an optional, but recommended, series resistor on the USB supply for improved immunity to transient over-voltage during VBUS connection.

### 9.3.1 Circuit configuration no. 1

Circuit configuration number 1 for QKAA aQFN94, showing the schematic and the bill of materials table.

| Config no. | Supply configuration |     | Enabled features |     |
|------------|----------------------|-----|------------------|-----|
|            | VDDH                 | VDD | USB              | NFC |
| Config. 1  | USB                  | N/A | Yes              | No  |

Table 206: Configuration summary for circuit configuration no. 1

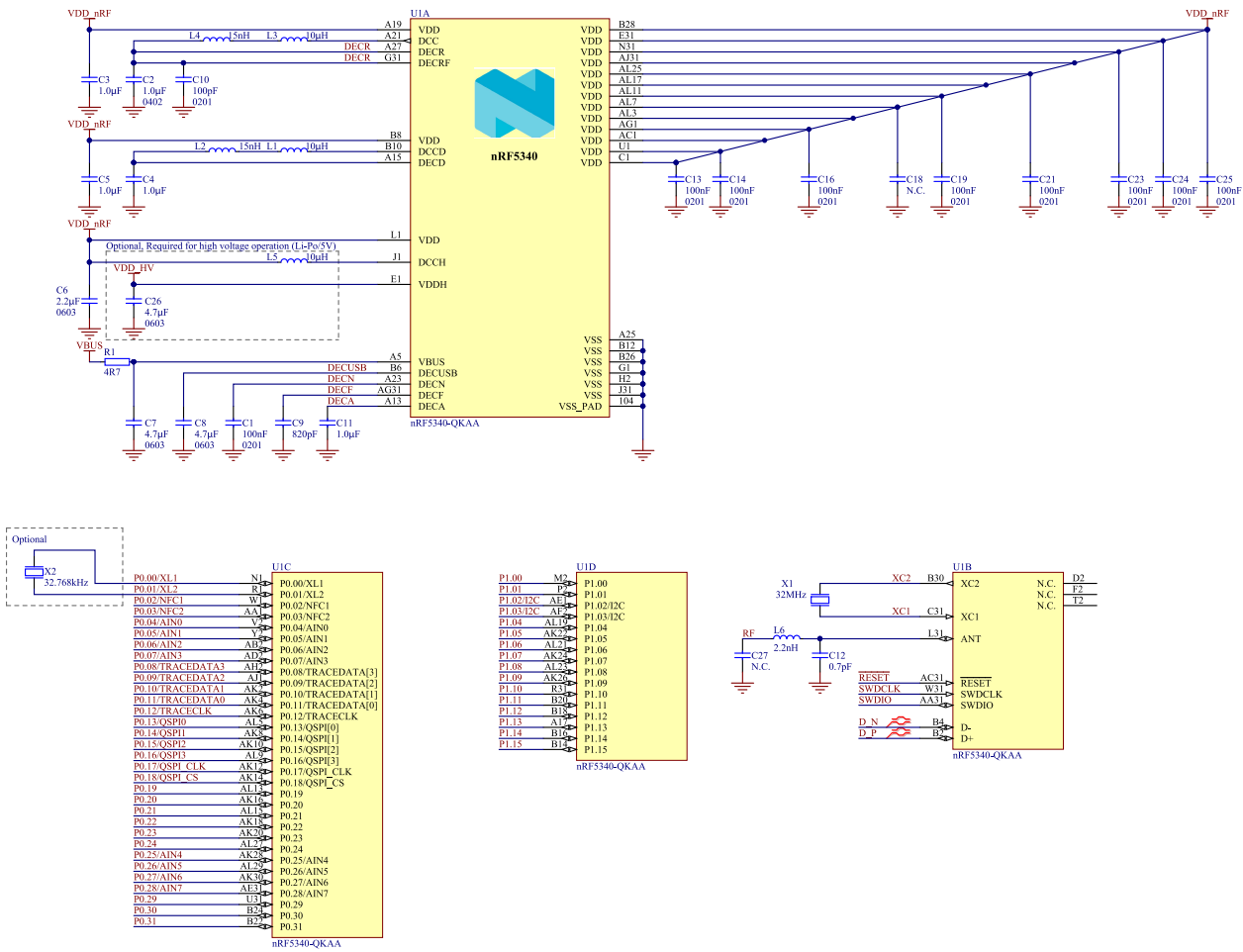


Figure 246: Circuit configuration no. 1 schematic

**Note:** For PCB reference layouts, see the product page for the nRF5340 on [www.nordicsemi.com](http://www.nordicsemi.com).

| Designator                                 | Value        | Description                                                                                   | Footprint |
|--------------------------------------------|--------------|-----------------------------------------------------------------------------------------------|-----------|
| C1, C13, C14, C16, C19, C21, C23, C24, C25 | 100 nF       | Capacitor, X5R, $\pm 10\%$                                                                    | 0201      |
| C2, C3, C4, C5, C11                        | 1.0 $\mu$ F  | Capacitor, X5R, $\pm 5\%$ , 6.3 V                                                             | 0402      |
| C6                                         | 2.2 $\mu$ F  | Capacitor, X7R, $\pm 10\%$                                                                    | 0603      |
| C7                                         | 4.7 $\mu$ F  | Capacitor, X7R, $\pm 10\%$                                                                    | 0603      |
| C8, C26                                    | 4.7 $\mu$ F  | Capacitor, X7S, $\pm 10\%$                                                                    | 0603      |
| C9                                         | 820 pF       | Capacitor, X7R, $\pm 10\%$                                                                    | 0201      |
| C10                                        | 100 pF       | Capacitor, NP0, $\pm 2\%$                                                                     | 0201      |
| C12                                        | 0.7 pF       | Capacitor, NP0, $\pm 0.05$ pF                                                                 | 0201      |
| C18, C27                                   | N.C.         | Not mounted                                                                                   | 0201      |
| L1, L3, L5                                 | 10 $\mu$ H   | Inductor, 250 mA, $\pm 20\%$ , 1.05 $\Omega$                                                  | 0603      |
| L2, L4                                     | 15 nH        | Inductor, 250 mA, $\pm 5\%$                                                                   | 0201      |
| L6                                         | 2.2 nH       | High frequency chip inductor, $\pm 5\%$                                                       | 0201      |
| R1                                         | 4.7 $\Omega$ | Resistor, $\pm 1\%$ , 0.05 W                                                                  | 0201      |
| U1                                         | nRF5340-QKAA | Multi-protocol Bluetooth Low Energy, IEEE 802.15.4, ANT and 2.4GHz proprietary system-on-chip | AQFN-94   |
| X1                                         | 32 MHz       | XTAL SMD 2016, 32 MHz, CI=8 pF, $\pm 40$ ppm                                                  | XTAL_2016 |
| X2                                         | 32.768 kHz   | XTAL SMD 2012, 32.768 kHz, CI=9 pF, Total Tol: $\pm 50$ ppm                                   | XTAL_2012 |

Table 207: Bill of material for circuit configuration no. 1

### 9.3.2 PCB layout example

The PCB layout shown below is a reference layout for the aQFN package with internal LDO setup and VBUS supply.

**Note:** Pay attention to how the capacitor C12 is grounded. It is not directly connected to the ground plane, but grounded via pin J31 and to the VSS die pad. This is done to create additional filtering of harmonic components.

For all available reference layouts, see the product page for the nRF5340 on [www.nordicsemi.com](http://www.nordicsemi.com).

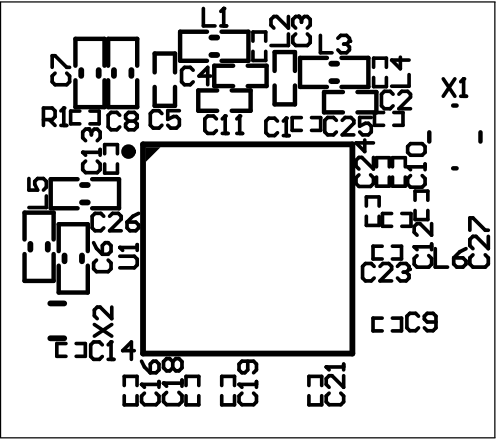


Figure 247: Top silk layer

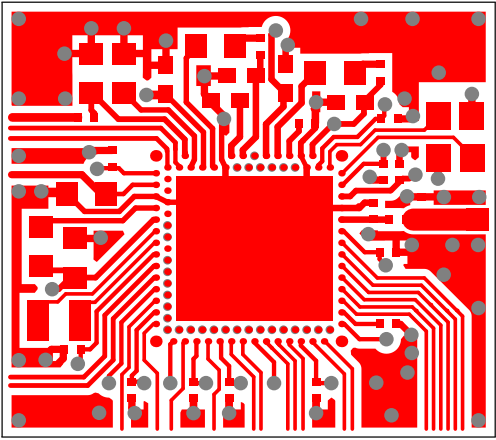


Figure 248: Top layer

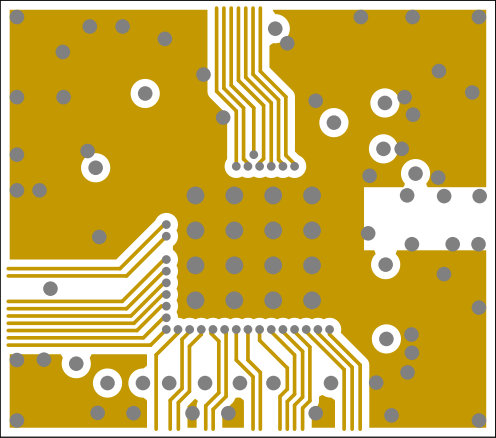


Figure 249: Mid layer 1

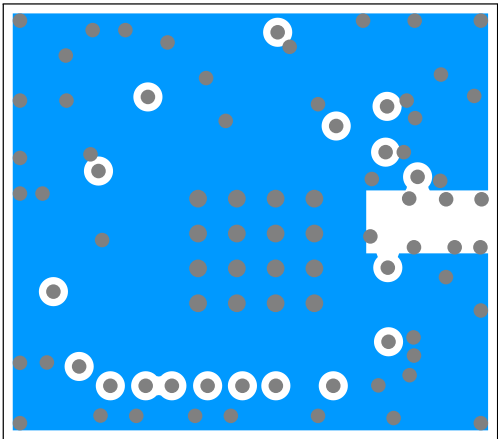


Figure 250: Mid layer 2

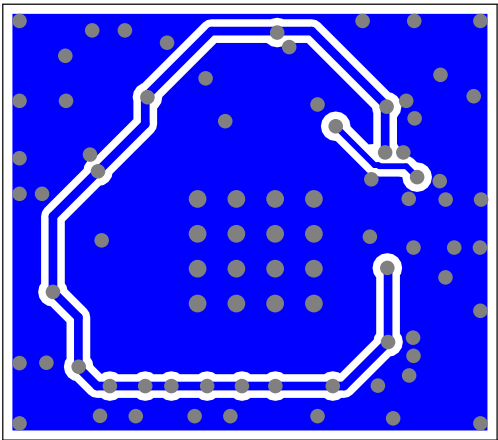


Figure 251: Bottom layer



# 10 Recommended operating conditions

The operating conditions are the physical parameters that the chip can operate within.

| Symbol              | Parameter                                       | Notes | Min. | Nom. | Max. | Units |
|---------------------|-------------------------------------------------|-------|------|------|------|-------|
| VDD                 | VDD supply voltage, independent of DCDC enable  |       | 1.7  | 3.0  | 3.6  | V     |
| VDDH                | VDDH supply voltage, independent of DCDC enable |       | 2.5  | 3.7  | 5.5  | V     |
| t <sub>R_VDD</sub>  | Supply rise time (0 V to 1.7 V)                 |       |      |      | tbd  | ms    |
| t <sub>R_VDDH</sub> | Supply rise time (0 V to 3.7 V)                 |       |      |      | tbd  | ms    |
| TA                  | Operating temperature                           |       | -40  | 25   | 105  | °C    |

Table 208: Recommended operating conditions

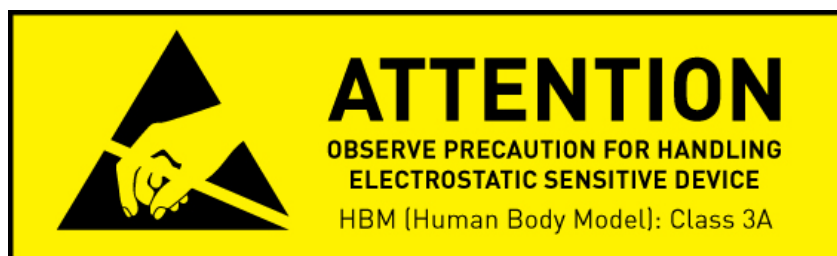
**Important:** The on-chip power-on reset circuitry may not function properly for rise times longer than the specified maximum.

# 11 Absolute maximum ratings

Maximum ratings are the extreme limits to which the chip can be exposed for a limited amount of time without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect the reliability of the device.

|                                   | Note                       | Min.             | Max.        | Unit               |
|-----------------------------------|----------------------------|------------------|-------------|--------------------|
| <b>Supply voltages</b>            |                            |                  |             |                    |
| VDD                               |                            | -0.3             | +3.9        | V                  |
| VDDH                              |                            | -0.3             | +5.8        | V                  |
| VBUS                              |                            | -0.3             | +5.8        | V                  |
| VSS                               |                            |                  | 0           | V                  |
| <b>I/O pin voltage</b>            |                            |                  |             |                    |
| $V_{I/O}$ , VDD $\leq$ 3.6 V      |                            | -0.3             | VDD + 0.3 V | V                  |
| $V_{I/O}$ , VDD > 3.6 V           |                            | -0.3             | 3.9 V       | V                  |
| <b>Environmental aQFN package</b> |                            |                  |             |                    |
| Storage temperature               |                            | -40              | +125        | °C                 |
| MSL                               | Moisture Sensitivity Level |                  | 2           |                    |
| ESD HBM                           | Human Body Model           |                  | 2           | kV                 |
| ESD CDM                           | Charged Device Model       |                  | 500         | V                  |
| <b>Flash memory</b>               |                            |                  |             |                    |
| Endurance                         |                            | 10 000           |             | Write/erase cycles |
| Retention                         |                            | 10 years at 40°C |             |                    |

Table 209: Absolute maximum ratings



# 12 Ordering information

This chapter contains information on IC marking, ordering codes, and container sizes.

## 12.1 IC marking

The nRF5340 SoC package is marked as shown in the following figure.

|     |    |    |    |     |     |
|-----|----|----|----|-----|-----|
| N   | 5  | 3  | 4  | 0   |     |
| <P> | P> | <V | V> | <H> | <P> |
| <Y  | Y> | <W | W> | <L  | L>  |

Figure 252: IC marking

## 12.2 Box labels

The following figures define the box labels used for the nRF5340.

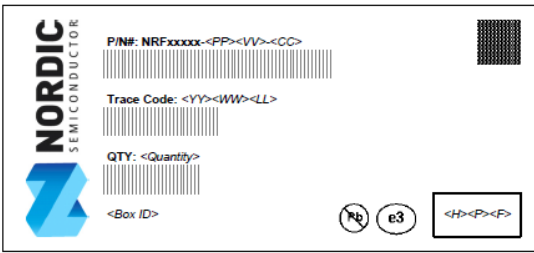


Figure 253: Inner box label

FROM:

TO:

DEVICE: NRFxxxx-<PP>-<VV>-<CC>

Rd

<H>-<P>-<F>

S/O No.: <Nordic Sales Order>

CUSTOMER PO No.: <Customer Purchase Order>

WF LOT No.: <Wafer Lot Number>

Trace Code: <YY>-<WW>-<LL>

QTY: <Quantity>

PACKAGE COUNT:

of

PACKAGE WEIGHT: 

KGS

COUNTRY OF ORIGIN: <Country>

Figure 254: Outer box label

### 12.3 Order code

The following tables define the nRF5340 order codes and definitions.

|   |   |   |   |   |   |   |   |    |    |    |    |   |    |    |
|---|---|---|---|---|---|---|---|----|----|----|----|---|----|----|
| n | R | F | 5 | 3 | 4 | 0 | - | <P | P> | <V | V> | - | <C | C> |
|---|---|---|---|---|---|---|---|----|----|----|----|---|----|----|

Figure 255: Order code

4406\_456 v0.5

776

| Abbreviation | Definition and implemented codes                                                                                                                                             |
|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| N53/nRF53    | nRF53 series product                                                                                                                                                         |
| 40           | Part code                                                                                                                                                                    |
| <PP>         | Package variant code                                                                                                                                                         |
| <VV>         | Function variant code                                                                                                                                                        |
| <H><P><F>    | Build code<br>H - Hardware version code<br>P - Production configuration code (production site, etc.)<br>F - Firmware version code (only visible on shipping container label) |
| <YY><WW><LL> | Tracking code<br>YY - Year code<br>WW - Assembly week number<br>LL - Wafer lot code                                                                                          |
| <CC>         | Container code                                                                                                                                                               |

Table 210: Abbreviations

## 12.4 Code ranges and values

The following tables define the nRF5340 code ranges and values.

| <PP> | Package | Size (mm) | Pin/Ball count | Pitch (mm) |
|------|---------|-----------|----------------|------------|
| QK   | AQFN    | 7 x 7     | 94             | 0.4        |

Table 211: Package variant codes

| <VV> | Flash (kB) | RAM (kB) |
|------|------------|----------|
| AA   | 1024       | 512      |

Table 212: Function variant codes

| <H>       | Description                                        |
|-----------|----------------------------------------------------|
| [A . . Z] | Hardware version/revision identifier (incremental) |

Table 213: Hardware version codes

| <P>       | Description                                 |
|-----------|---------------------------------------------|
| [0 . . 9] | Production device identifier (incremental)  |
| [A . . Z] | Engineering device identifier (incremental) |

Table 214: Production configuration codes

| <F>                | Description                              |
|--------------------|------------------------------------------|
| [A . . N, P . . Z] | Version of preprogrammed firmware        |
| [0]                | Delivered without preprogrammed firmware |

Table 215: Production version codes

| <YY>        | Description                   |
|-------------|-------------------------------|
| [16 . . 99] | Production year: 2016 to 2099 |

Table 216: Year codes

| <WW>       | Description        |
|------------|--------------------|
| [1 . . 52] | Week of production |

Table 217: Week codes

| <LL>        | Description                     |
|-------------|---------------------------------|
| [AA . . ZZ] | Wafer production lot identifier |

Table 218: Lot codes

| <CC> | Description |
|------|-------------|
| R7   | 7" Reel     |
| R    | 13" Reel    |
| T    | Tray        |

Table 219: Container codes

## 12.5 Product options

The following tables define the nRF5340 product options.

| Order code      | MOQ <sup>29</sup> | Comment                       |
|-----------------|-------------------|-------------------------------|
| nRF5340-QKAA-R7 | 800               | Availability to be announced. |
| nRF5340-QKAA-R  | 3000              |                               |
| nRF5340-QKAA-T  | 260               |                               |

*Table 220: nRF5340 order codes*

| Order code         | Description                     |
|--------------------|---------------------------------|
| nRF5340-PREVIEW-DK | nRF5340 Preview Development Kit |

*Table 221: Development tools order code*

<sup>29</sup> Minimum Ordering Quantity

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