



# NJG1135MD7

## ■ ABSOLUTE MAXIMUM RATINGS

( $T_a=+25^{\circ}\text{C}$ ,  $Z_s=Z_l=50\Omega$ )

PARAMETERS	SYMBOL	CONDITIONS	RATINGS	UNITS
Supply voltage	$V_{DD}$		5.0	V
Control voltage	$V_{CTL}$	VCTL1, VCTL2 terminal	5.0	V
Input power	$P_{in}$	$V_{DD}=2.8\text{V}$	+15	dBm
Power dissipation	$P_D$	4-layer FR4 PCB with through-hole (74.2x74.2mm), $T_j=150^{\circ}\text{C}$	1300	mW
Operating temperature	$T_{opr}$		-40~+85	$^{\circ}\text{C}$
Storage temperature	$T_{stg}$		-55~+150	$^{\circ}\text{C}$

## ■ ELECTRICAL CHARACTERISTICS 1 (DC CHARACTERISTICS)

(General Conditions:  $V_{DD}=2.8\text{V}$ ,  $T_a=+25^{\circ}\text{C}$ ,  $Z_s=Z_l=50\Omega$ )

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating voltage	$V_{DD}$		2.65	2.8	2.95	V
Control voltage (High)	$V_{CTL(H)}$		1.8	2.8	2.95	V
Control voltage (Low)	$V_{CTL(L)}$		-0.3	0	0.3	V
Operating current1 (Cellular Band High Gain mode)	$I_{DD1}$	RF OFF, $V_{CTL1}=0\text{V}$ , $V_{CTL2}=2.8\text{V}$	-	10	14	mA
Operating current2 (PCS Band High Gain mode)	$I_{DD2}$	RF OFF, $V_{CTL1}=2.8\text{V}$ , $V_{CTL2}=0\text{V}$	-	10	14	mA
Operating current3 (LNA all off mode)	$I_{DD3}$	RF OFF, $V_{CTL1}=0\text{V}$ , $V_{CTL2}=0\text{V}$	-	30	60	$\mu\text{A}$
Control current1	$I_{CTL1}$	RF OFF, $V_{CTL1}=2.8\text{V}$	-	17	30	$\mu\text{A}$
Control current2	$I_{CTL2}$	RF OFF, $V_{CTL2}=2.8\text{V}$	-	17	30	$\mu\text{A}$

## ■ ELECTRICAL CHARACTERISTICS 2 (Cellular Band: LNA High Gain Mode)

(General Conditions:  $V_{DD}=2.8V$ ,  $V_{CTL1}=0V$ ,  $V_{CTL2}=2.8V$ ,  $f_{RF}=880MHz$ ,  $T_a=+25^{\circ}C$ ,  $Z_s=Z_l=50\Omega$ , with application circuit)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small signal gain 1	Gain1	Exclude PCB, Connector Losses (input and output) 0.11dB	14.5	16.0	-	dB
Noise figure 1	NF1	Exclude PCB, Connector Losses (input) 0.06dB	-	1.4	1.8	dB
1dB gain compression input power 1	P-1dB_1		-8	-4	-	dBm
3rd order input intercept point 1	IIP3_1	$f1=f_{RF}$ , $f2=f_{RF}+100kHz$ , $P_{in}=-25dBm$	+7	+10	-	dBm
RF IN VSWR 1	VSWR <sub>i</sub> _1		-	1.5	2.0	
RF OUT VSWR 1	VSWR <sub>o</sub> _1		-	1.5	2.0	

## ■ ELECTRICAL CHARACTERISTICS 3 (Cellular Band: LNA Low Gain Mode)

(General Conditions:  $V_{DD}=2.8V$ ,  $V_{CTL1}=0V$ ,  $V_{CTL2}=0V$ ,  $f_{RF}=880MHz$ ,  $T_a=+25^{\circ}C$ ,  $Z_s=Z_l=50\Omega$ , with application circuit)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small signal gain 2	Gain2	Exclude PCB, Connector Losses (input and output) 0.11dB	-4.0	-2.5	-	dB
Noise figure 2	NF2	Exclude PCB, Connector Losses (input and output) 0.11dB	-	2.5	5.0	dB
1dB gain compression input power 2	P-1dB_2		+3.5	+10.5	-	dBm
3rd order input intercept point 2	IIP3_2	$f1=f_{RF}$ , $f2=f_{RF}+100kHz$ , $P_{in}=-12dBm$	+15	+19	-	dBm
RF IN VSWR 2	VSWR <sub>i</sub> _2		-	2.0	2.5	
RF OUT VSWR 2	VSWR <sub>o</sub> _2		-	1.5	2.0	

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## ■ ELECTRICAL CHARACTERISTICS 4 (PCS Band: LNA High Gain Mode)

(General Conditions:  $V_{DD}=2.8V$ ,  $V_{CTL1}=2.8V$ ,  $V_{CTL2}=0V$ ,  $f_{RF}=1960MHz$ ,  $T_a=+25^{\circ}C$ ,  $Z_s=Z_l=50\Omega$ , with application circuit)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small signal gain 3	Gain3	Exclude PCB, Connector Losses (input and output) 0.22dB	14.5	16.0	-	dB
Noise figure 3	NF3	Exclude PCB, Connector Losses (input) 0.12dB	-	1.4	1.8	dB
1dB gain compression input power 3	P-1dB_3		-10	-6	-	dBm
3rd order input intercept point 3	IIP3_3	$f1=f_{RF}$ , $f2=f_{RF}+100kHz$ , $P_{in}=-25dBm$	+5	+8	-	dBm
RF IN VSWR 3	VSWR <sub>i</sub> _3		-	2.3	3.1	
RF OUT VSWR 3	VSWR <sub>o</sub> _3		-	1.5	2.2	

## ■ ELECTRICAL CHARACTERISTICS 5 (PCS Band: LNA Low Gain Mode)

(General Conditions:  $V_{DD}=2.8V$ ,  $V_{CTL1}=0V$ ,  $V_{CTL2}=0V$ ,  $f_{RF}=1960MHz$ ,  $T_a=+25^{\circ}C$ ,  $Z_s=Z_l=50\Omega$ , with application circuit)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small signal gain 4	Gain4	Exclude PCB, Connector Losses (input and output) 0.22dB	-5.0	-3.5	-	dB
Noise figure 4	NF4	Exclude PCB, Connector Losses (input and output) 0.22dB	-	4.0	5.5	dB
1dB gain compression input power 4	P-1dB_4		+1.5	+8.5	-	dBm
3rd order input intercept point 4	IIP3_4	$f1=f_{RF}$ , $f2=f_{RF}+100kHz$ , $P_{in}=-12dBm$	+13	+17	-	dBm
RF IN VSWR 4	VSWR <sub>i</sub> _4		-	2.3	2.9	
RF OUT VSWR 4	VSWR <sub>o</sub> _4		-	1.5	2.0	

## ■ TERMINAL INFORMATION

No.	SYMBOL	DESCRIPTION
1	GND	Ground terminal.
2	VCTL2	Control port 2. This terminal is set to more than +1.8V~+2.95V of logical high level for high gain mode of cellular band LNA, and set to -0.3V~+0.3V of logical low level for low gain mode of cellular band LNA.
3	VCTL1	Control port 1. This terminal is set to more than +1.8V~+2.95V of logical high level for high gain mode of PCS band LNA, and set to -0.3V~+0.3V of logical low level for low gain mode of PCS band LNA.
4	GND	Ground terminal.
5	RFOUT1	RF output terminal of PCS band signal. RF signal and DC power is input through external matching circuit connected to this terminal. External matching circuit and DC blocking capacitor are required.
6	RFOUT2	RF output terminal of cellular band signal. RF signal and DC power is input through external matching circuit connected to this terminal. External matching circuit and DC blocking capacitor are required.
7	GND	Ground terminal. This terminal is not connected with internal circuit.
8	GND	Ground terminal.
9	GND	Ground terminal. This terminal is not connected with internal circuit.
10	GND	Ground terminal. This terminal is not connected with internal circuit.
11	GND	Ground terminal.
12	RFIN2	RF input terminal of cellular band signal. RF signal is input through external matching circuit connected to this terminal. A DC blocking capacitor is not required.
13	RFIN1	RF input terminal of PCS band signal. RF signal is input through external matching circuit connected to this terminal. A DC blocking capacitor is not required.
14	GND	Ground terminal. This terminal is not connected with internal circuit.

Notes:

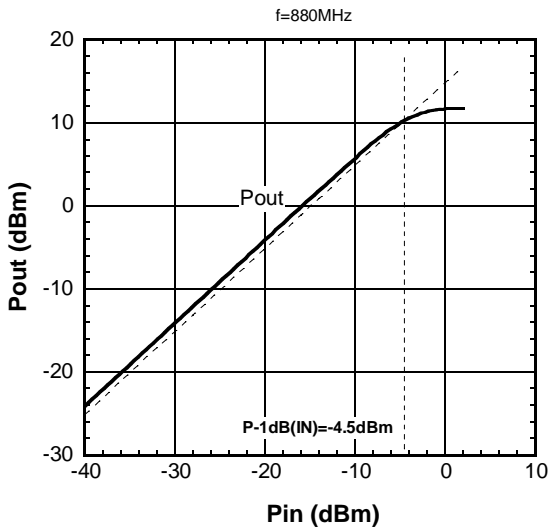
- 1) Ground terminal (No.1, 4, 8, and 11) should be connected with the ground plane as close as possible for good RF performance, because distance to GND makes parasitic inductance.

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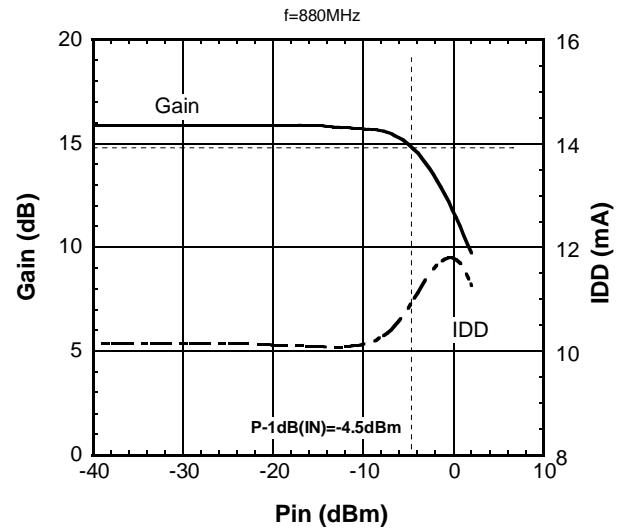
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(General Conditions:  $V_{DD}=2.8V$ ,  $V_{CTL1}=0V$ ,  $V_{CTL2}=2.8V$ ,  $f_{RF}=880MHz$ ,  $T_a=+25^\circ C$ ,  $Z_s=Z_l=50\Omega$ , with application circuit)

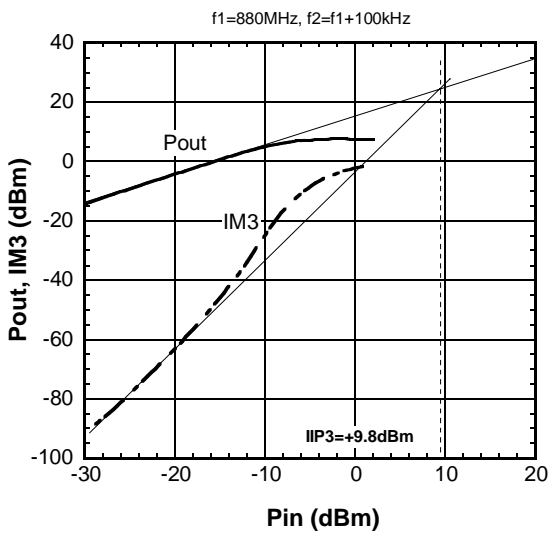
**Pout vs. Pin**



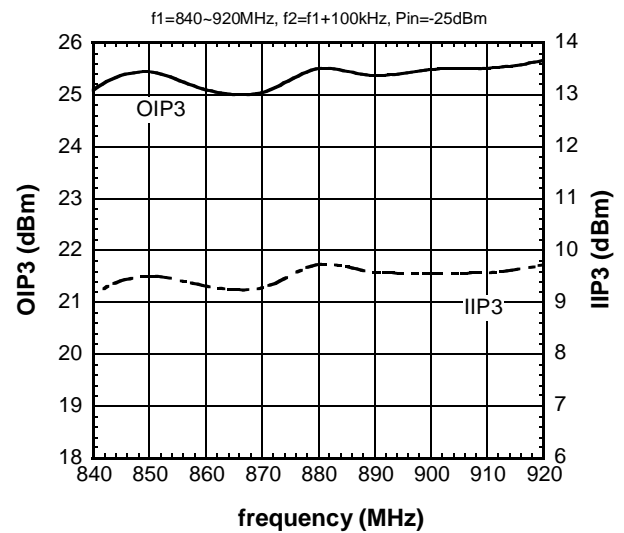
**Gain, IDD vs. Pin**



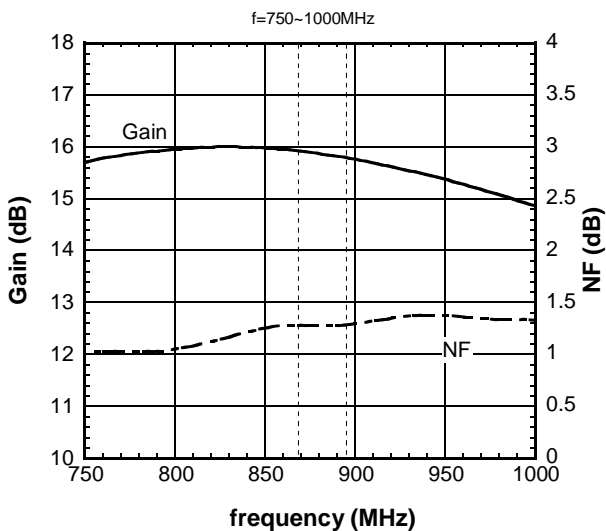
**Pout, IM3 vs. Pin**



**OIP3, IIP3 vs. frequency**

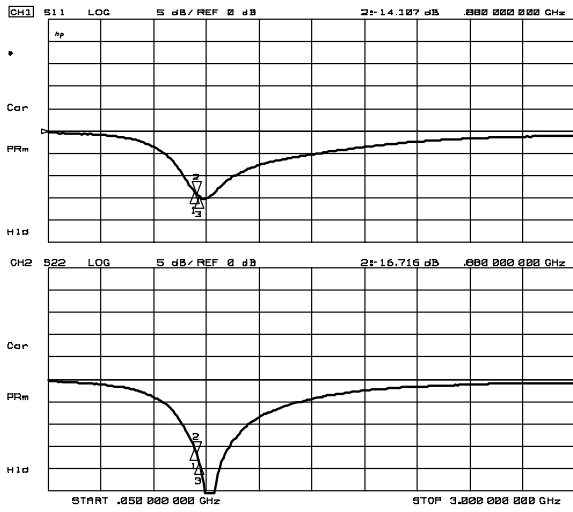


**Gain, NF vs. frequency**

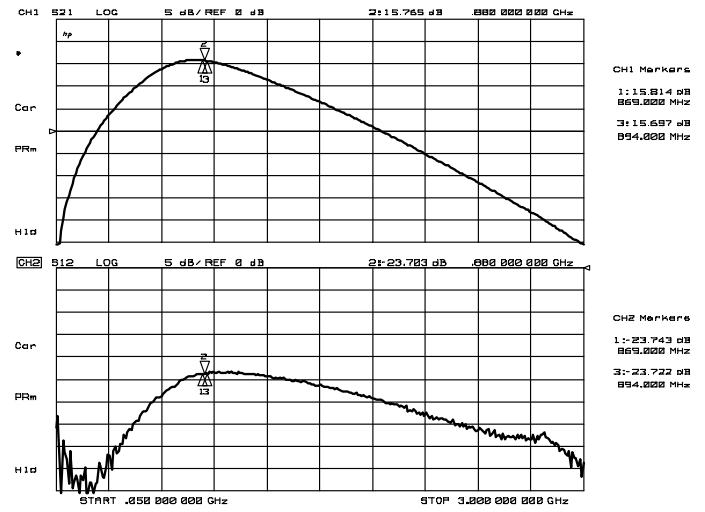


## ELECTRICAL CHARACTERISTICS (Cellular Band: LNA High Gain Mode)

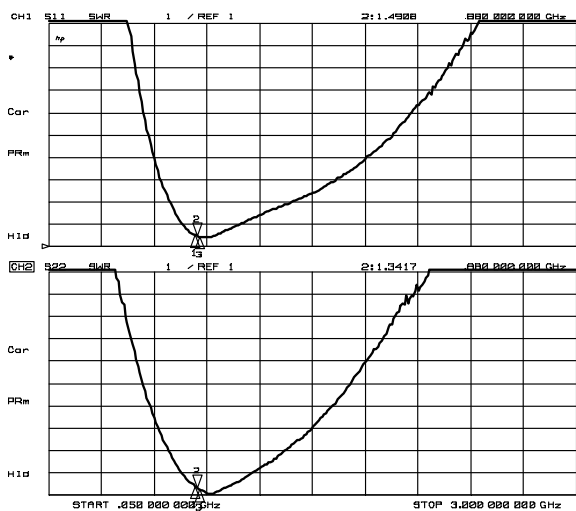
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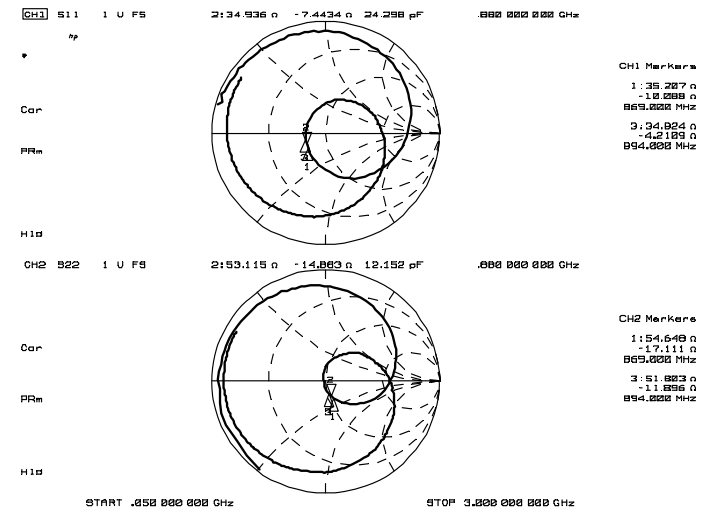
S11, S22



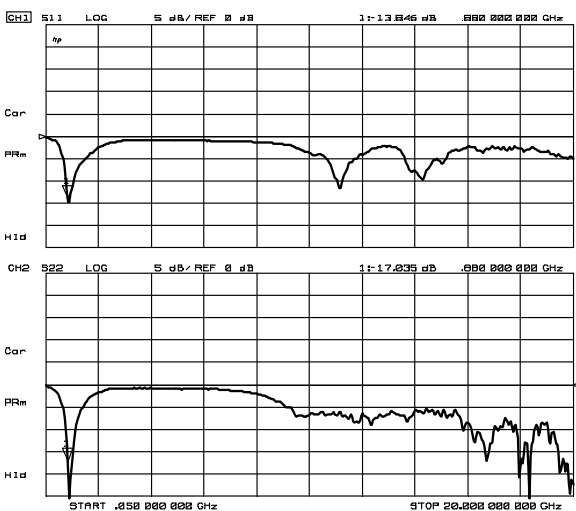
S21, S12



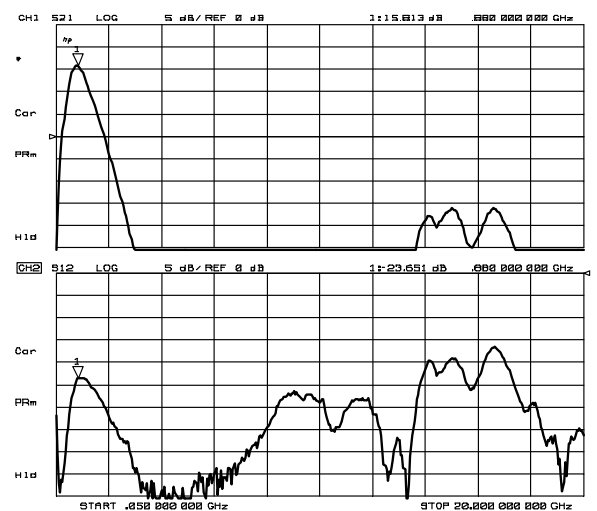
VSWR



Zin, Zout



S11, S22 (~20GHz)



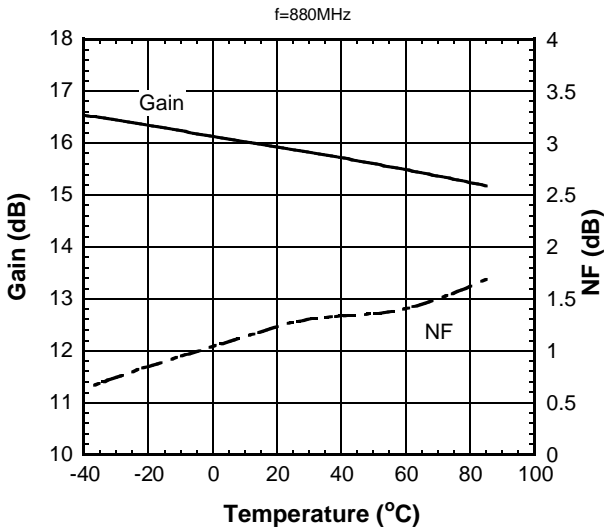
S21, S12 (~20GHz)

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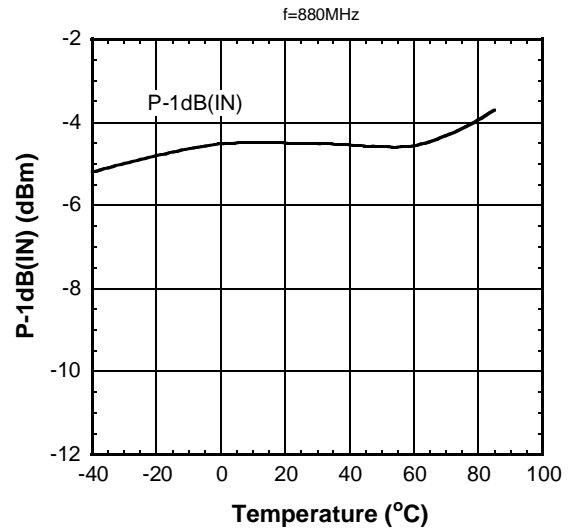
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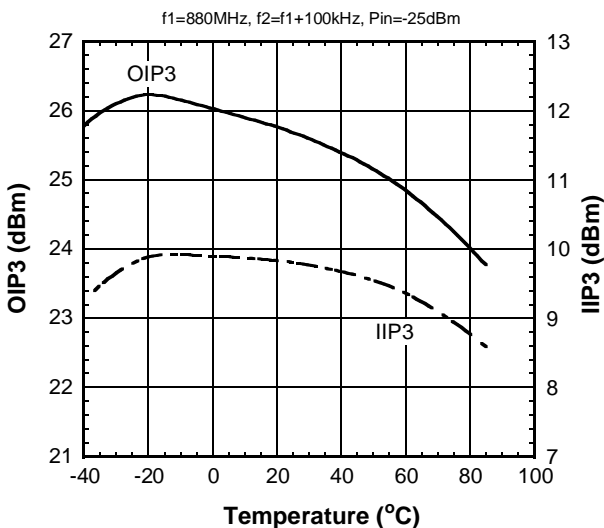
Gain, NF vs. Temperature



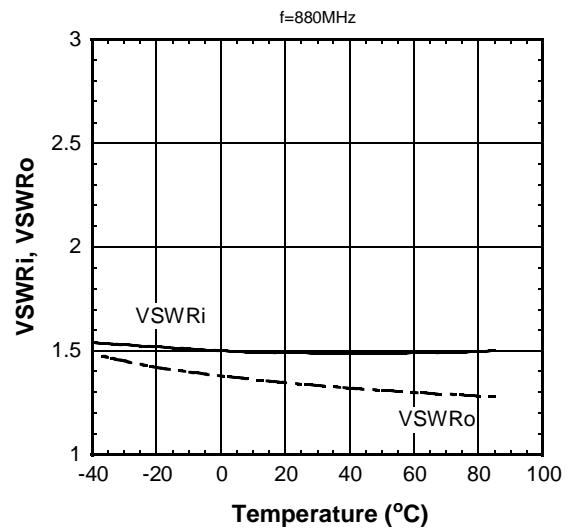
P-1dB(IN) vs. Temperature



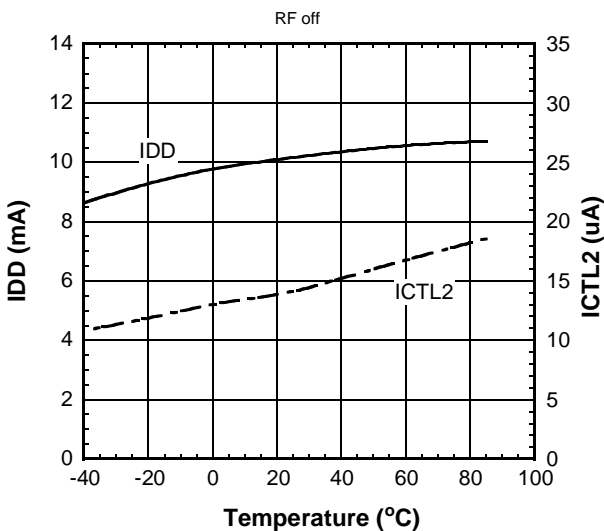
OIP3, IIP3 vs. Temperature



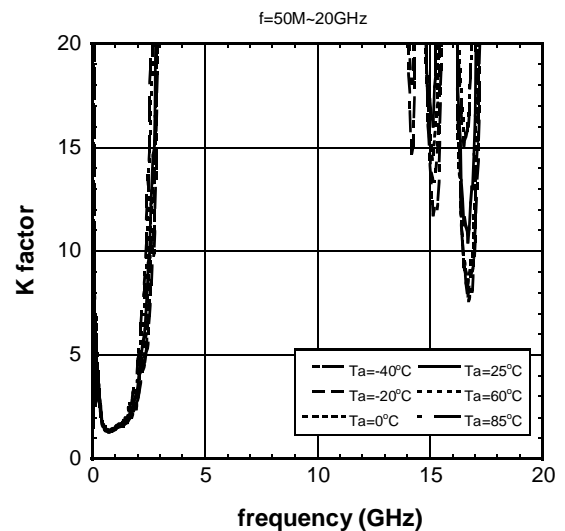
VSWRi, VSWRo vs. Temperature



IDD, ICTL2 vs. Temperature



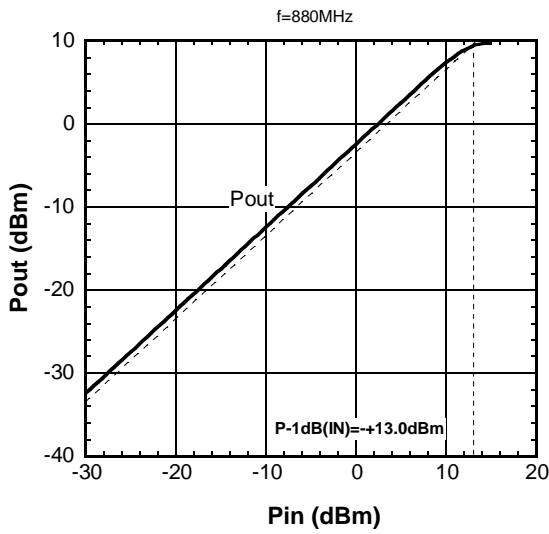
K factor vs. frequency



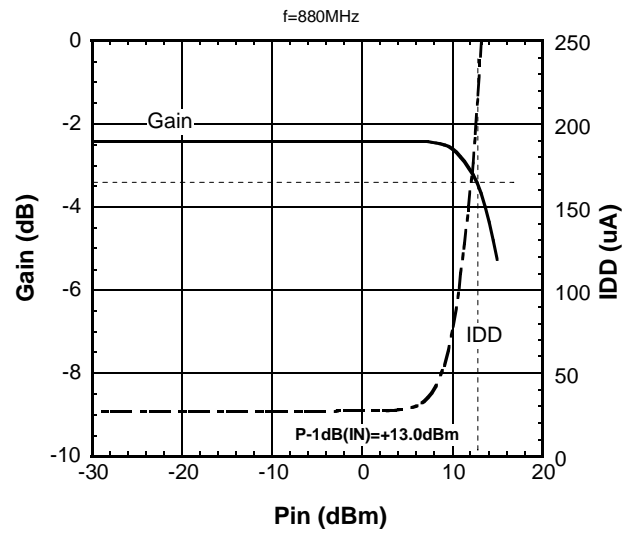
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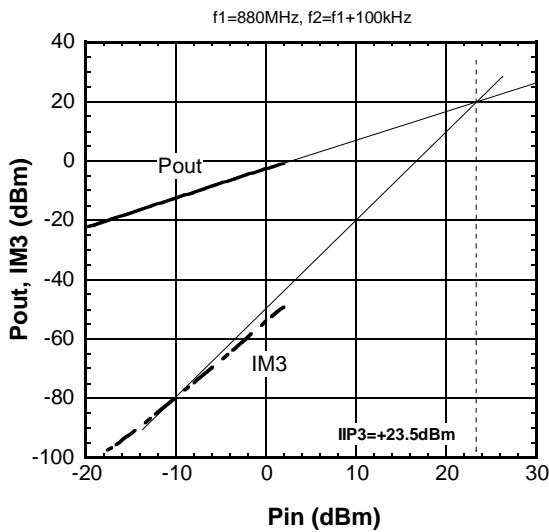
### Pout vs. Pin



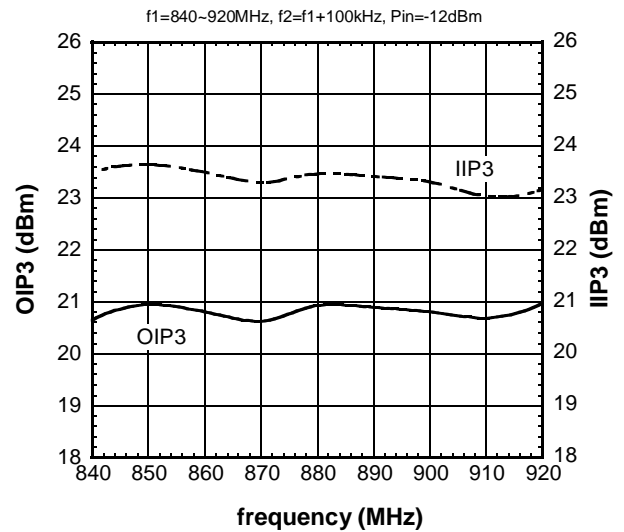
### Gain, IDD vs. Pin



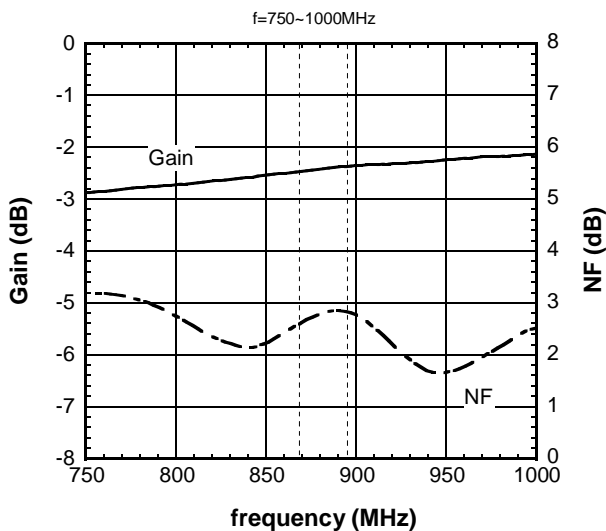
### Pout, IM3 vs. Pin



### OIP3, IIP3 vs. frequency



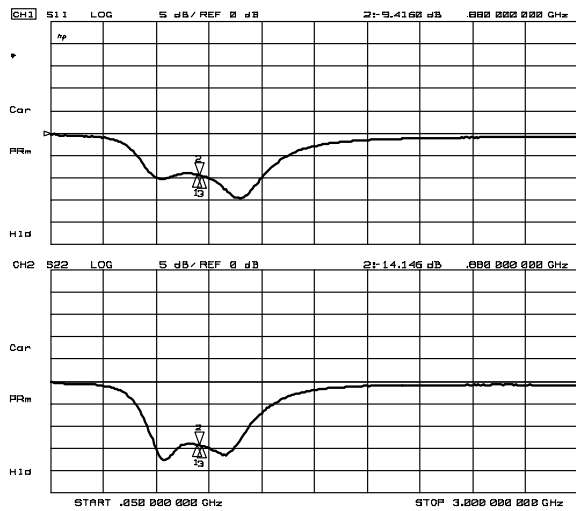
### Gain, NF vs. frequency



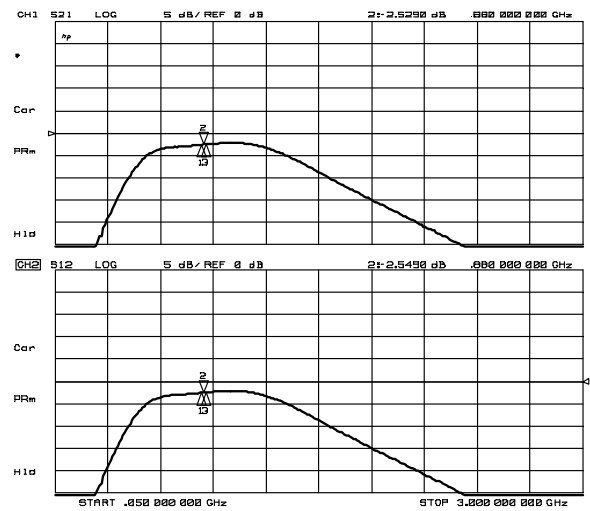
# NJG1135MD7

## ■ ELECTRICAL CHARACTERISTICS (Cellular Band: LNA Low Gain Mode)

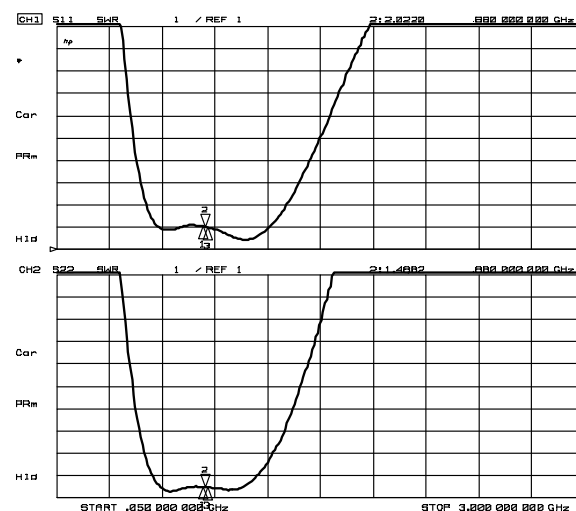
(General Conditions:  $V_{DD}=2.8V$ ,  $V_{CTL1}=0V$ ,  $V_{CTL2}=2.8V$ ,  $f_{RF}=880MHz$ ,  $T_a=+25^{\circ}C$ ,  $Z_s=Z_l=50\Omega$ , with application circuit)



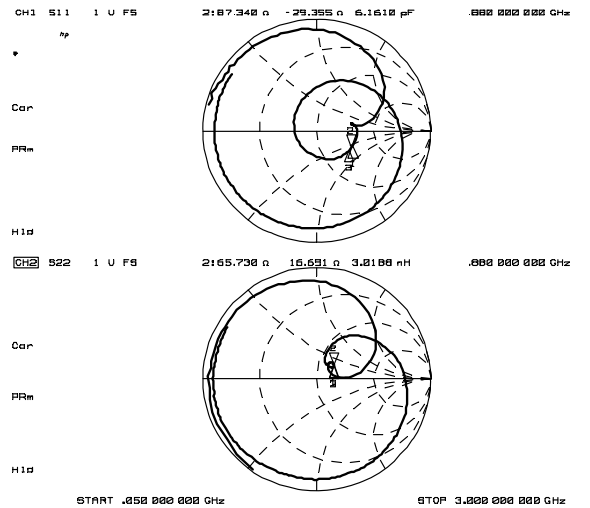
S11, S22



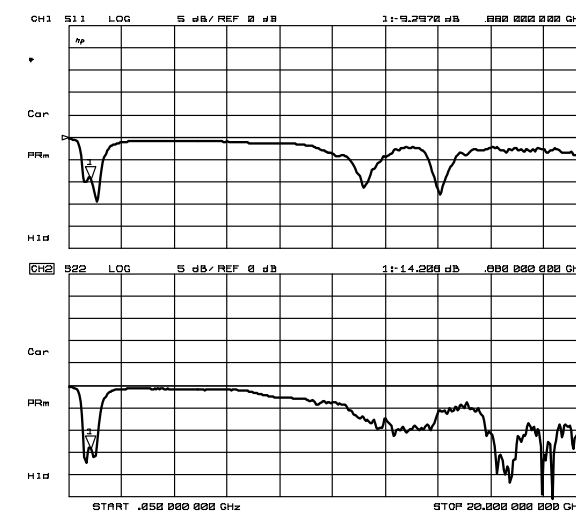
S21, S12



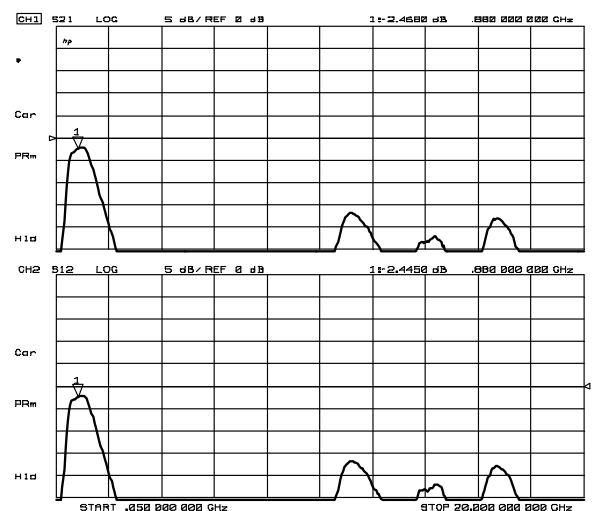
VSWR



Zin, Zout



S11, S22 (~20GHz)

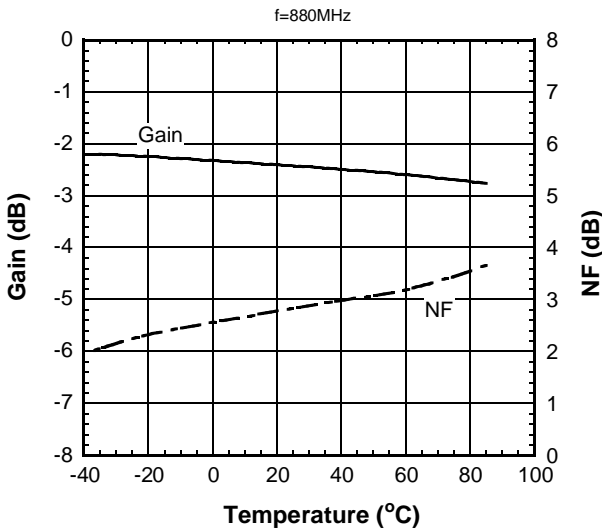


S21, S12 (~20GHz)

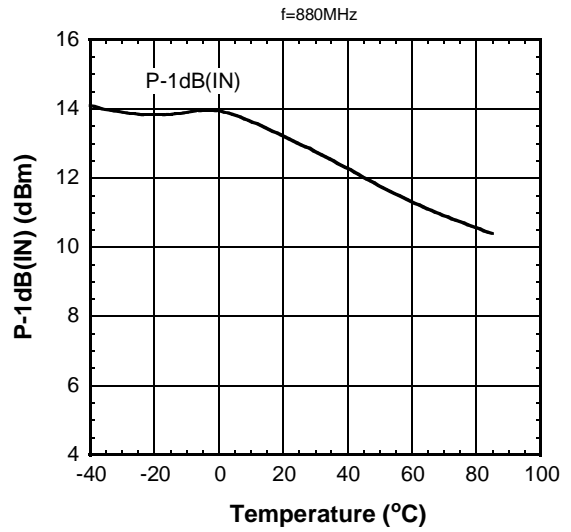
## ■ ELECTRICAL CHARACTERISTICS (Cellular Band: LNA Low Gain Mode)

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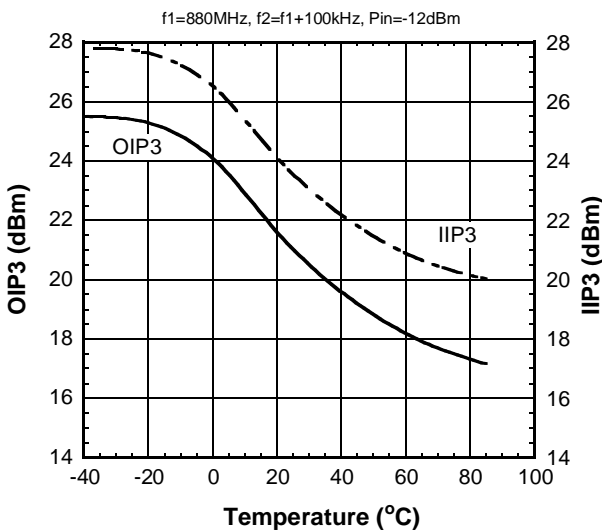
### Gain, NF vs. Temperature



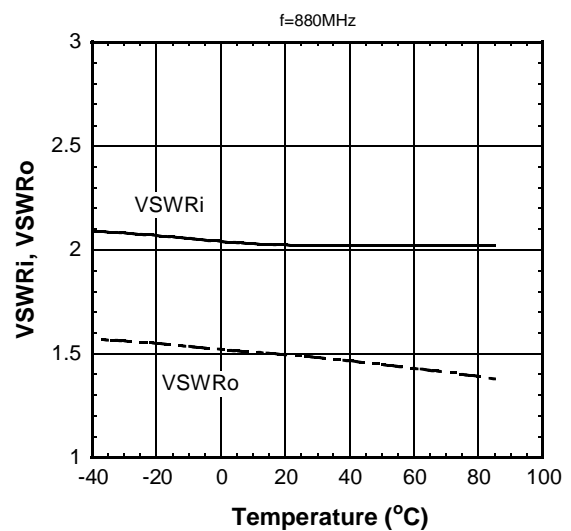
### P-1dB(IN) vs. Temperature



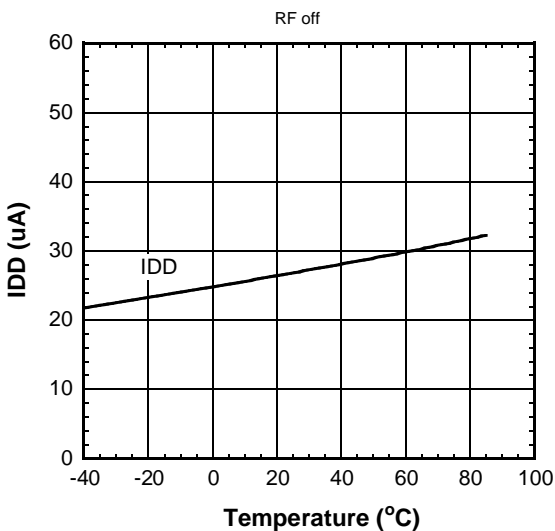
### OIP3, IIP3 vs. Temperature



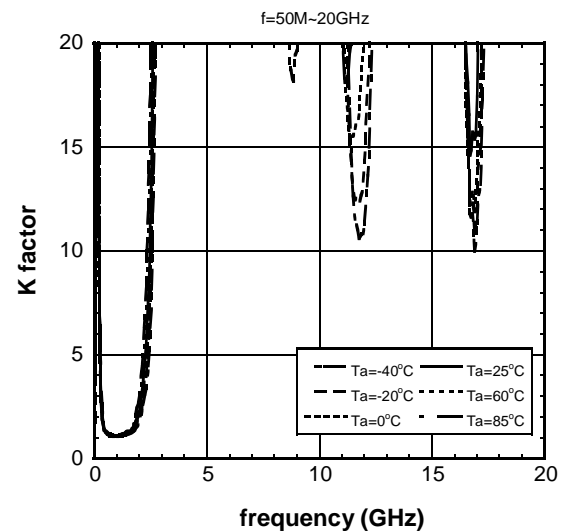
### VSWRi, VSWRo vs. Temperature



### IDD vs. Temperature



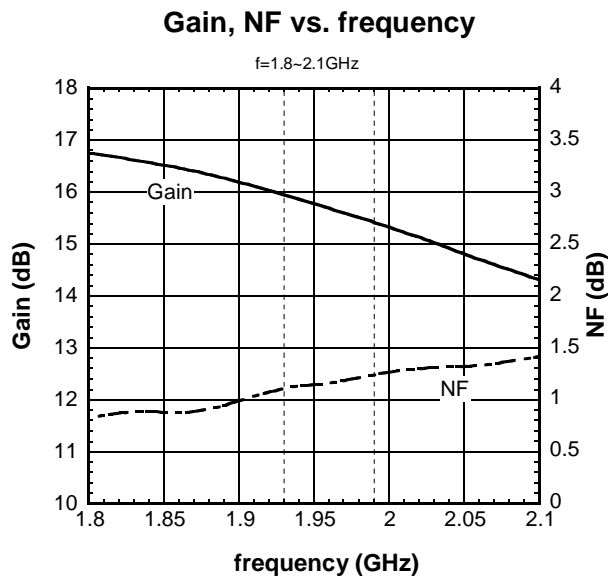
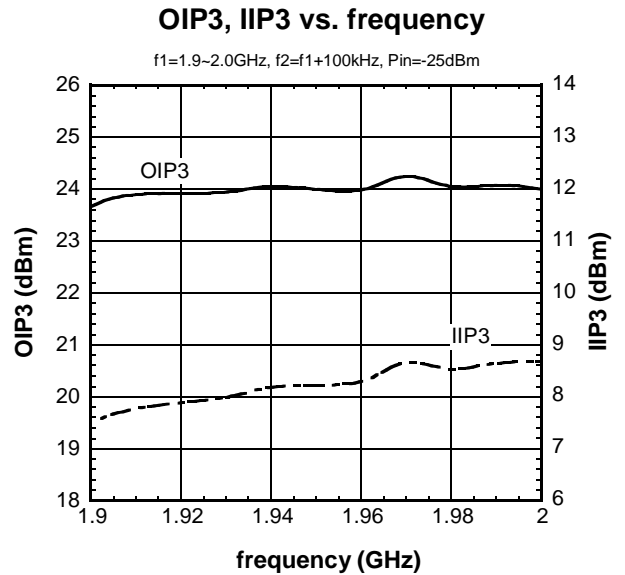
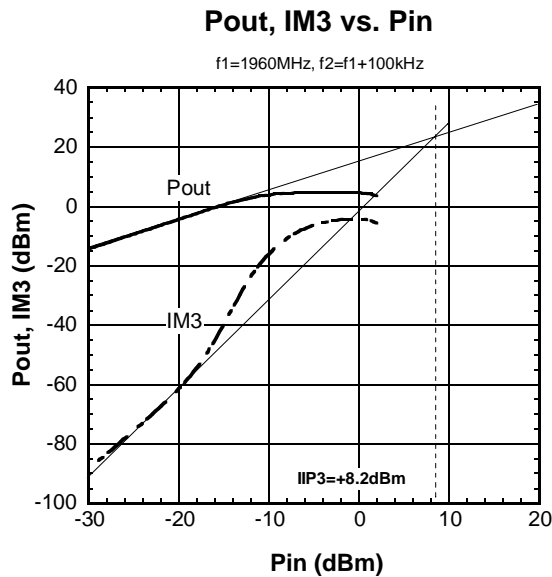
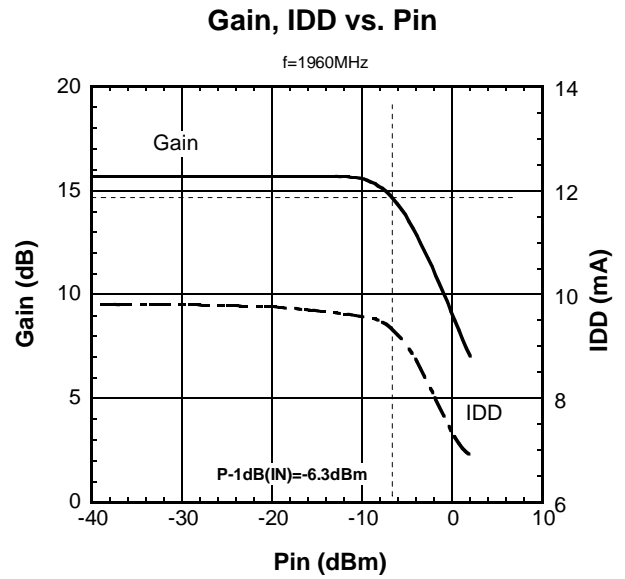
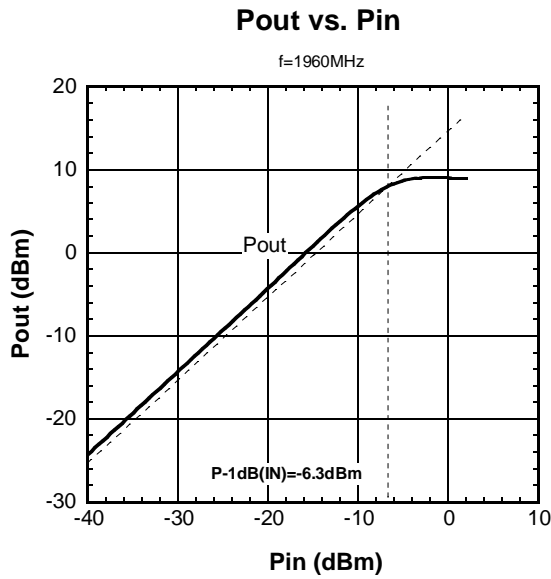
### K factor vs. frequency



# NJG1135MD7

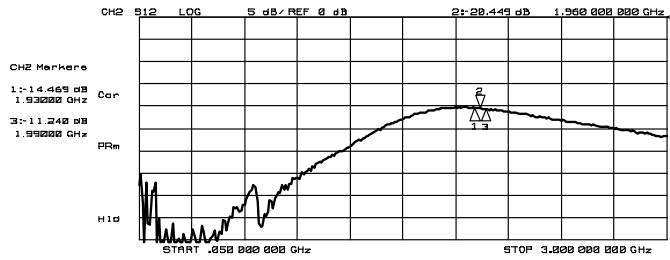
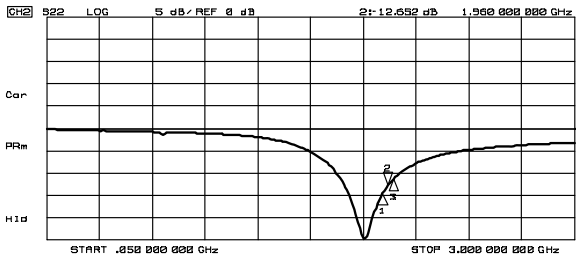
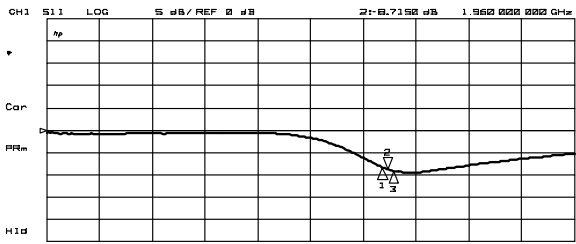
## ■ ELECTRICAL CHARACTERISTICS (PCS Band: LNA High Gain Mode)

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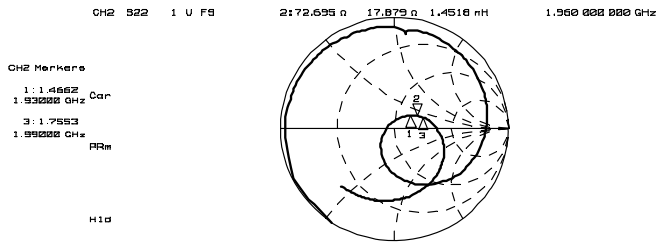
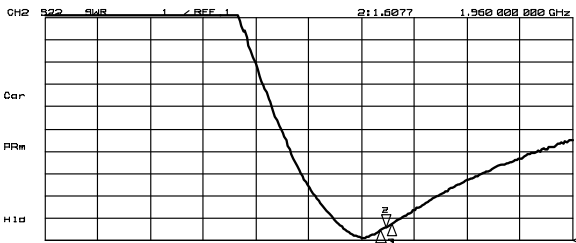
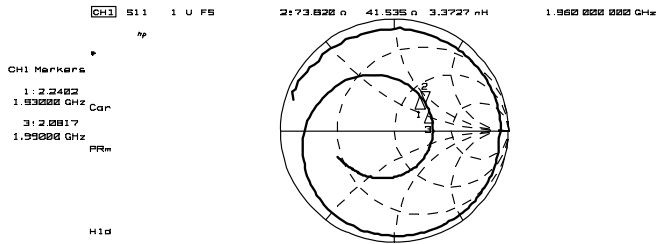
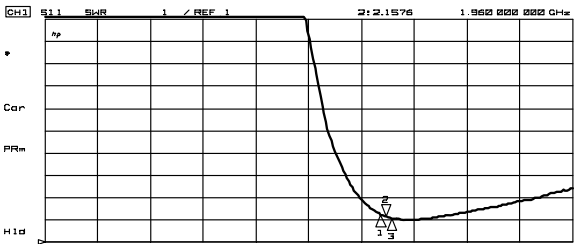
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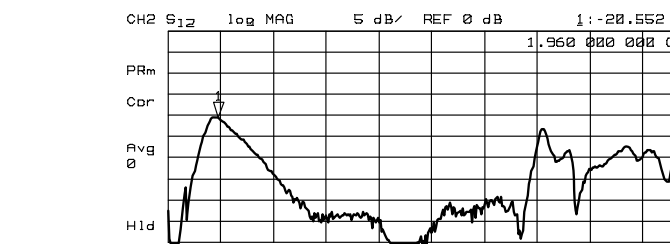
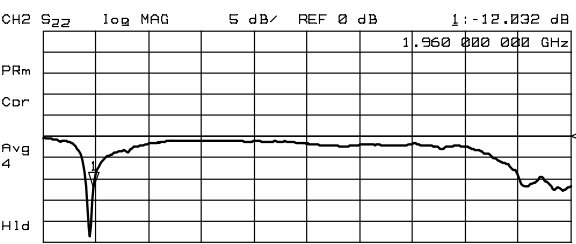
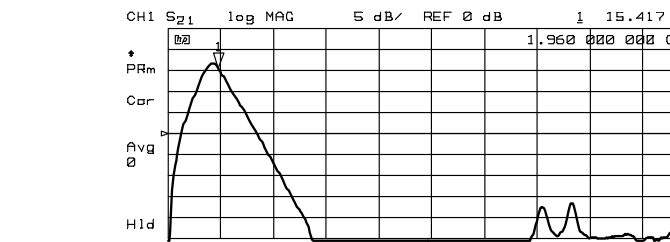
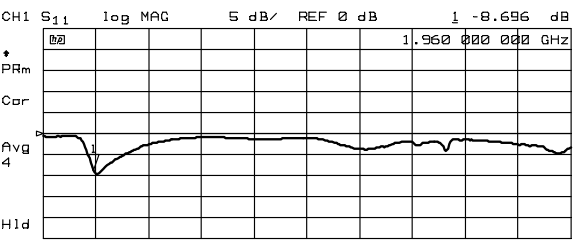
S11, S22

S21, S12



VSWR

Zin, Zout



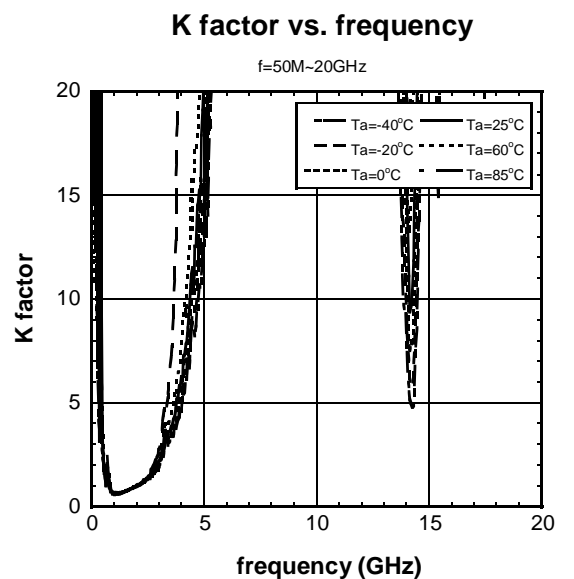
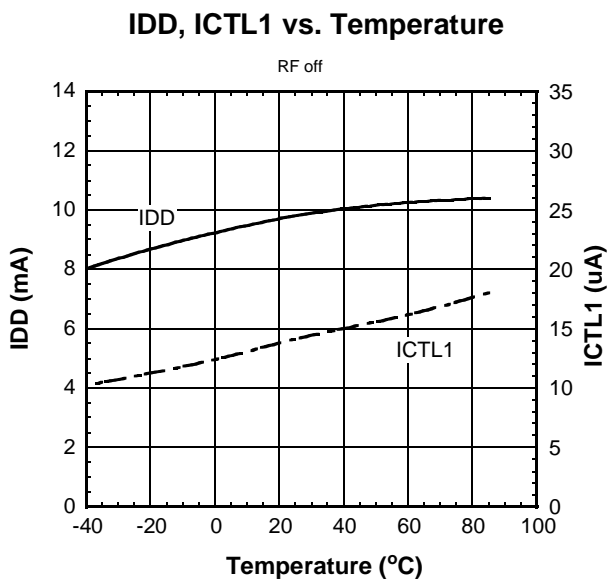
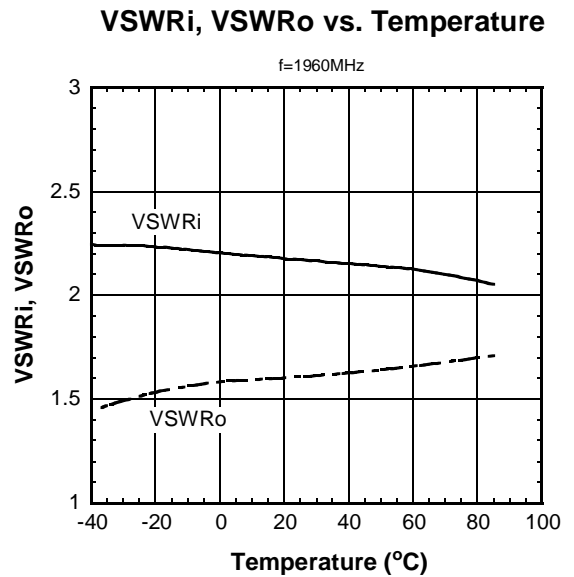
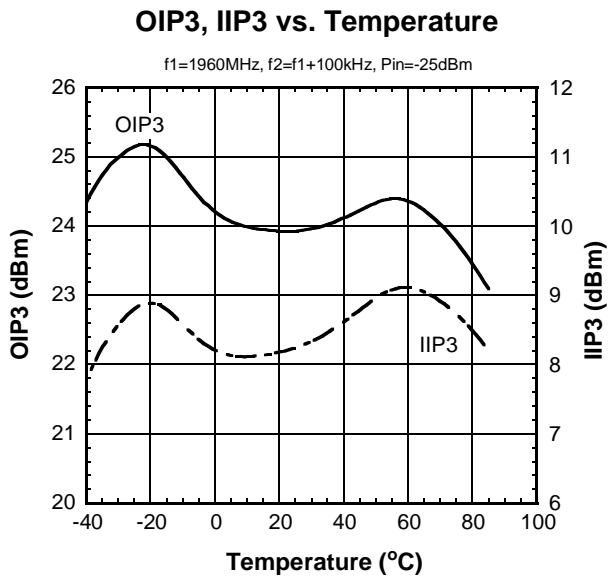
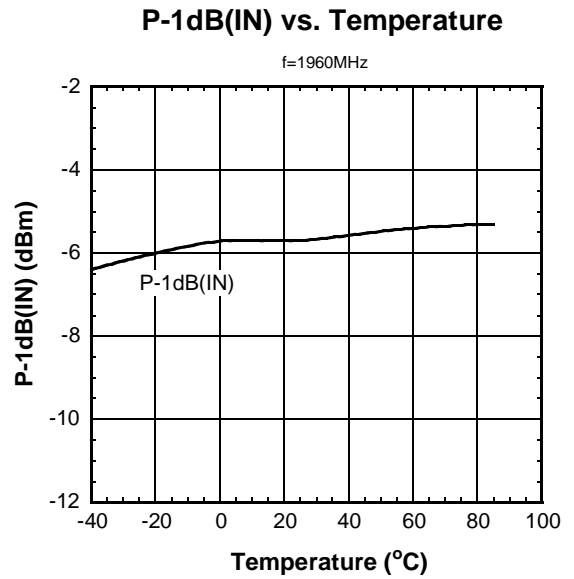
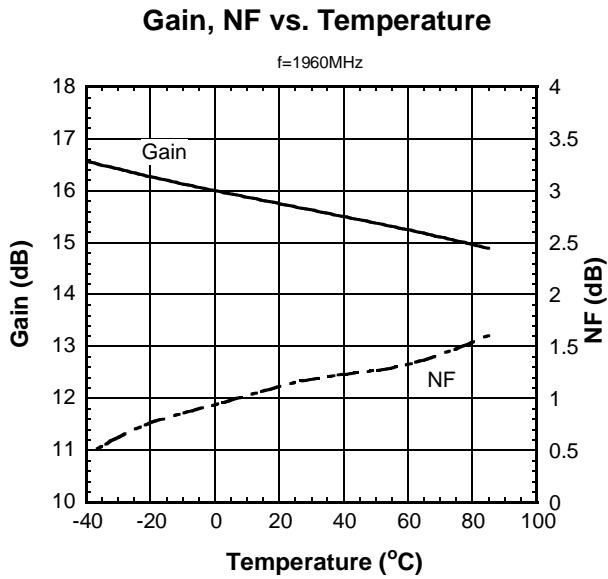
S11, S22 (~20GHz)

S21, S12 (~20GHz)

# NJG1135MD7

## ■ ELECTRICAL CHARACTERISTICS (PCS Band: LNA High Gain Mode)

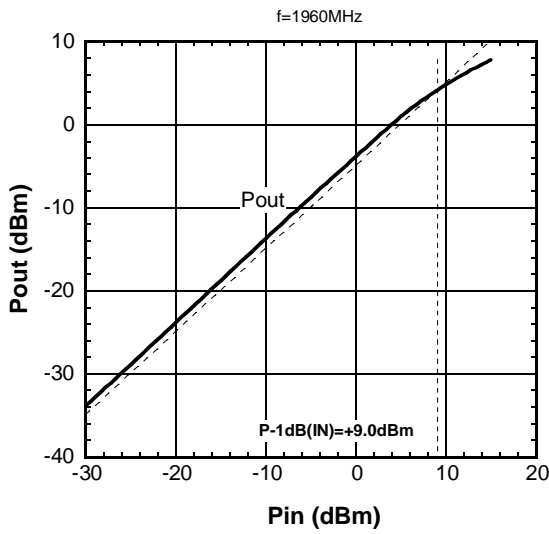
(General Conditions:  $V_{DD}=2.8V$ ,  $V_{CTL1}=0V$ ,  $V_{CTL2}=2.8V$ ,  $f_{RF}=1960MHz$ ,  $Z_S=Z_L=50\Omega$ , with application circuit)



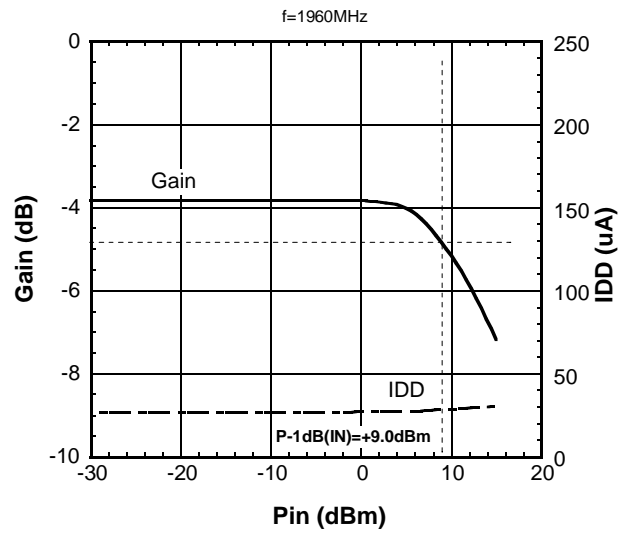
## ■ ELECTRICAL CHARACTERISTICS (PCS Band: LNA Low Gain Mode)

(General Conditions:  $V_{DD}=2.8V$ ,  $V_{CTL1}=0V$ ,  $V_{CTL2}=2.8V$ ,  $f_{RF}=1960MHz$ ,  $T_a=+25^{\circ}C$ ,  $Z_s=Z_l=50\Omega$ , with application circuit)

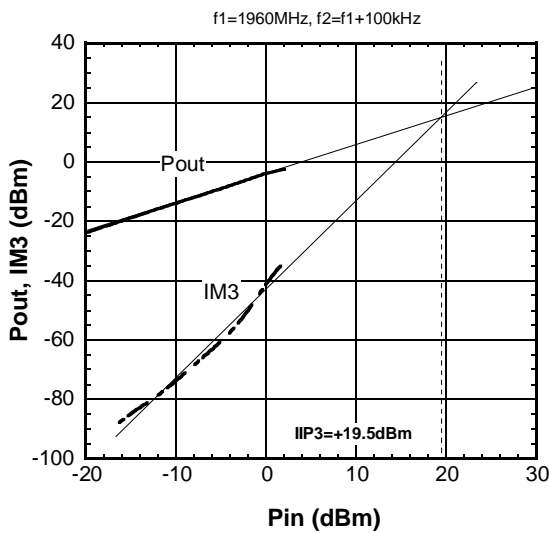
**Pout vs. Pin**



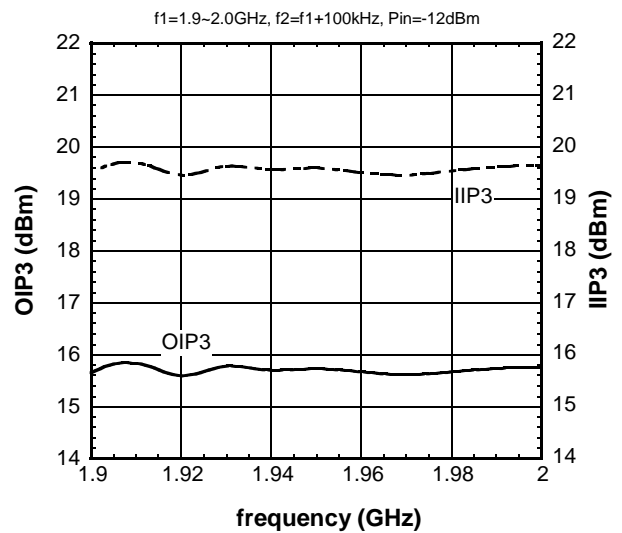
**Gain, IDD vs. Pin**



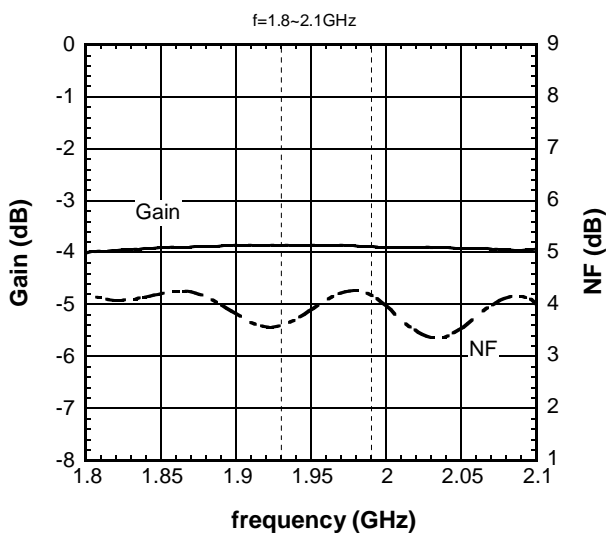
**Pout, IM3 vs. Pin**



**OIP3, IIP3 vs. frequency**



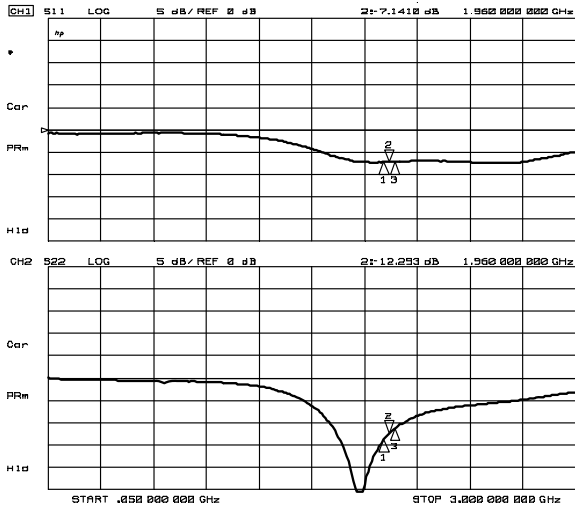
**Gain, NF vs. frequency**



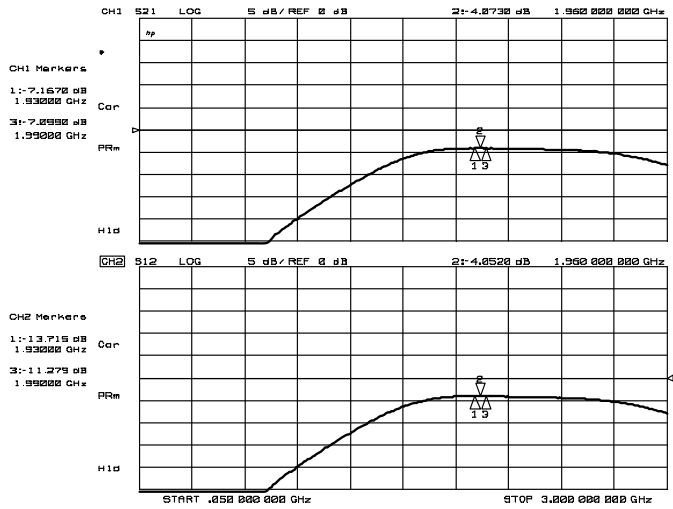
# NJG1135MD7

## ELECTRICAL CHARACTERISTICS (PCS Band: LNA Low Gain Mode)

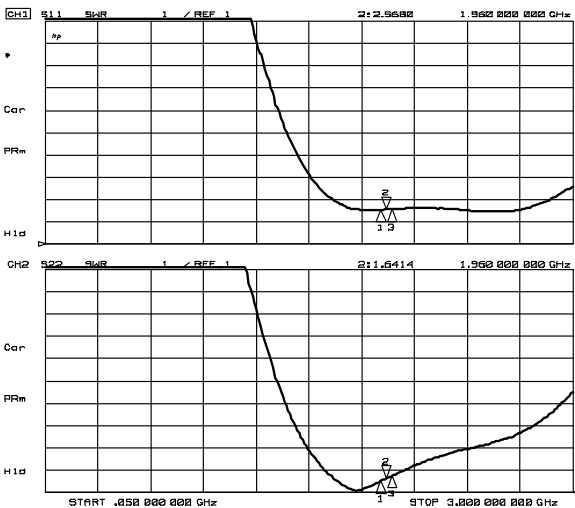
(General Conditions:  $V_{DD}=2.8V$ ,  $V_{CTL1}=0V$ ,  $V_{CTL2}=2.8V$ ,  $f_{RF}=1960MHz$ ,  $T_a=+25^{\circ}C$ ,  $Z_s=Z_l=50\Omega$ , with application circuit)



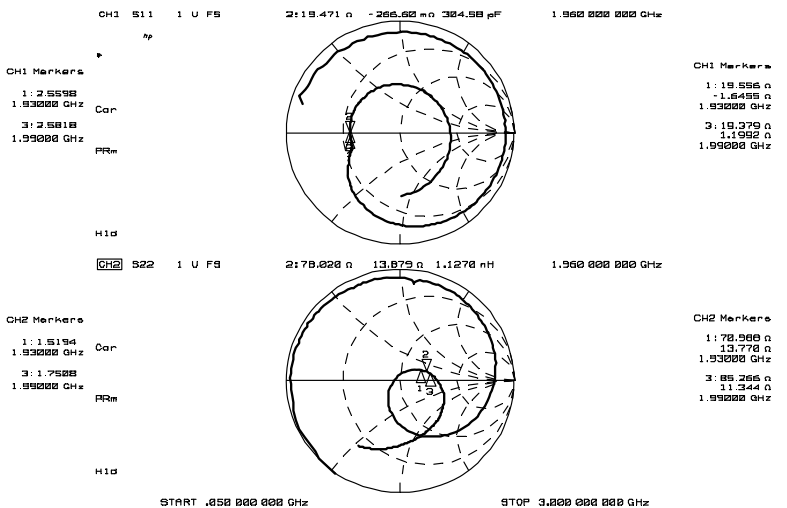
S11, S22



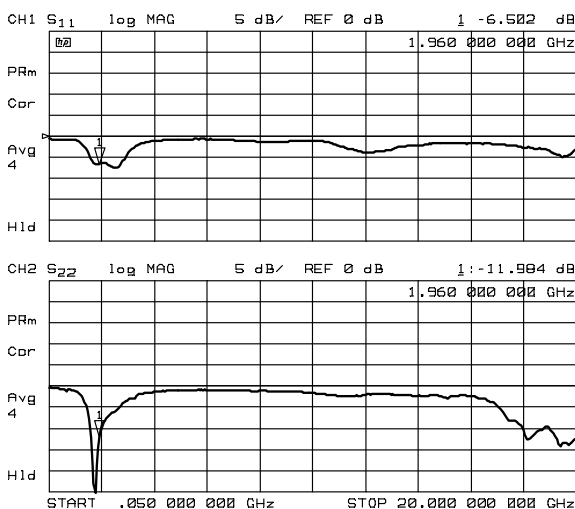
S21, S12



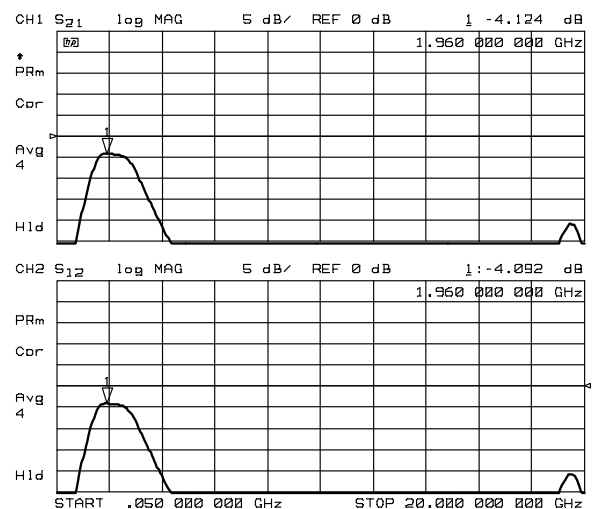
VSWR



Zin, Zout



S11, S22 (~20GHz)

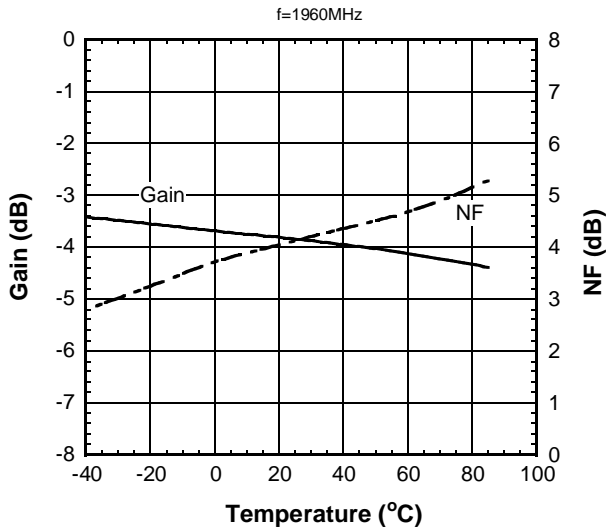


S21, S12 (~20GHz)

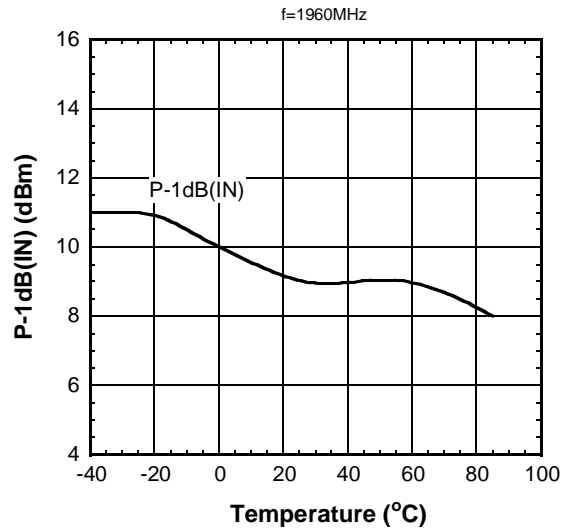
## ■ ELECTRICAL CHARACTERISTICS (PCS Band: LNA Low Gain Mode)

(General Conditions:  $V_{DD}=2.8V$ ,  $V_{CTL1}=0V$ ,  $V_{CTL2}=2.8V$ ,  $f_{RF}=1960MHz$ ,  $Z_s=Z_l=50\Omega$ , with application circuit)

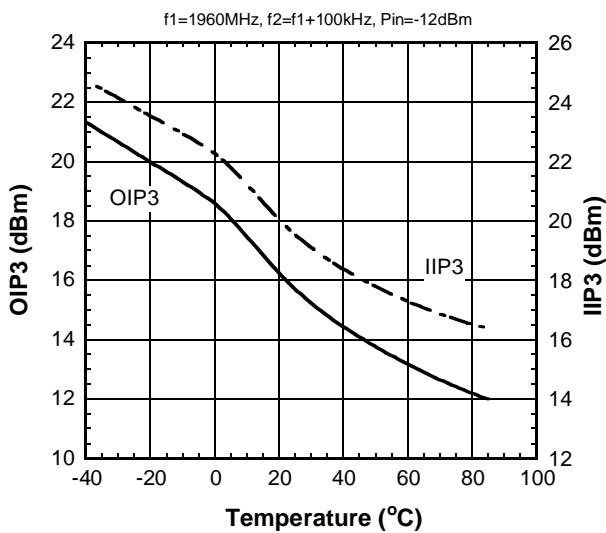
### Gain, NF vs. Temperature



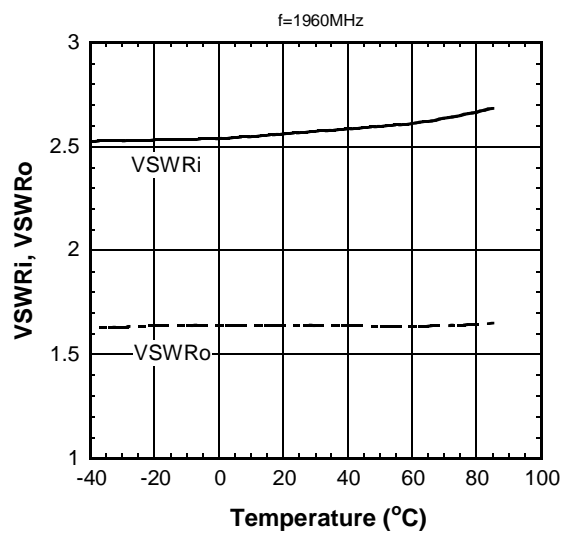
### P-1dB(IN) vs. Temperature



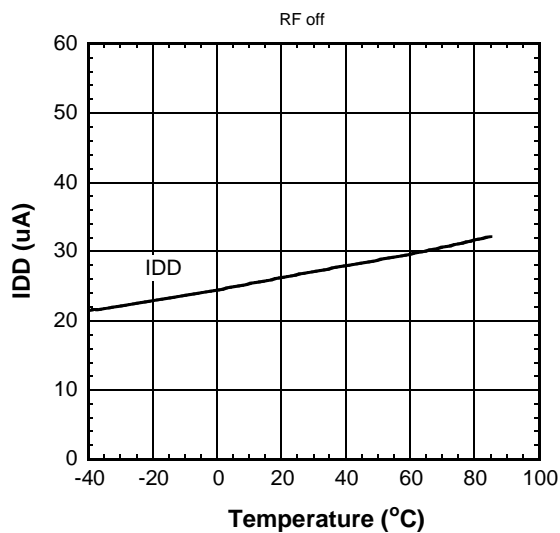
### OIP3, IIP3 vs. Temperature



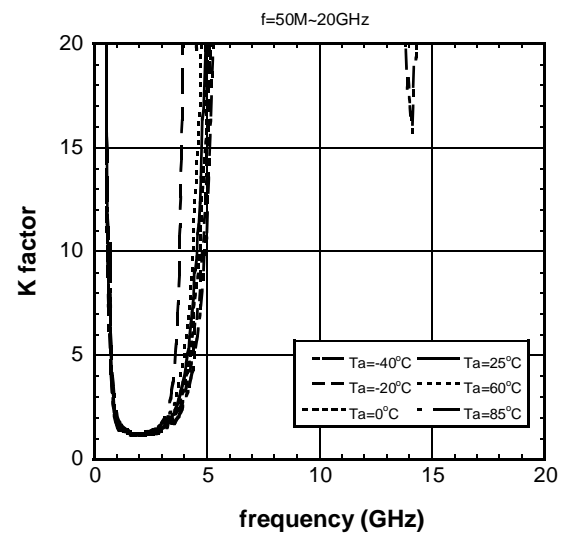
### VSWRi, VSWRo vs. Temperature



### IDD vs. Temperature

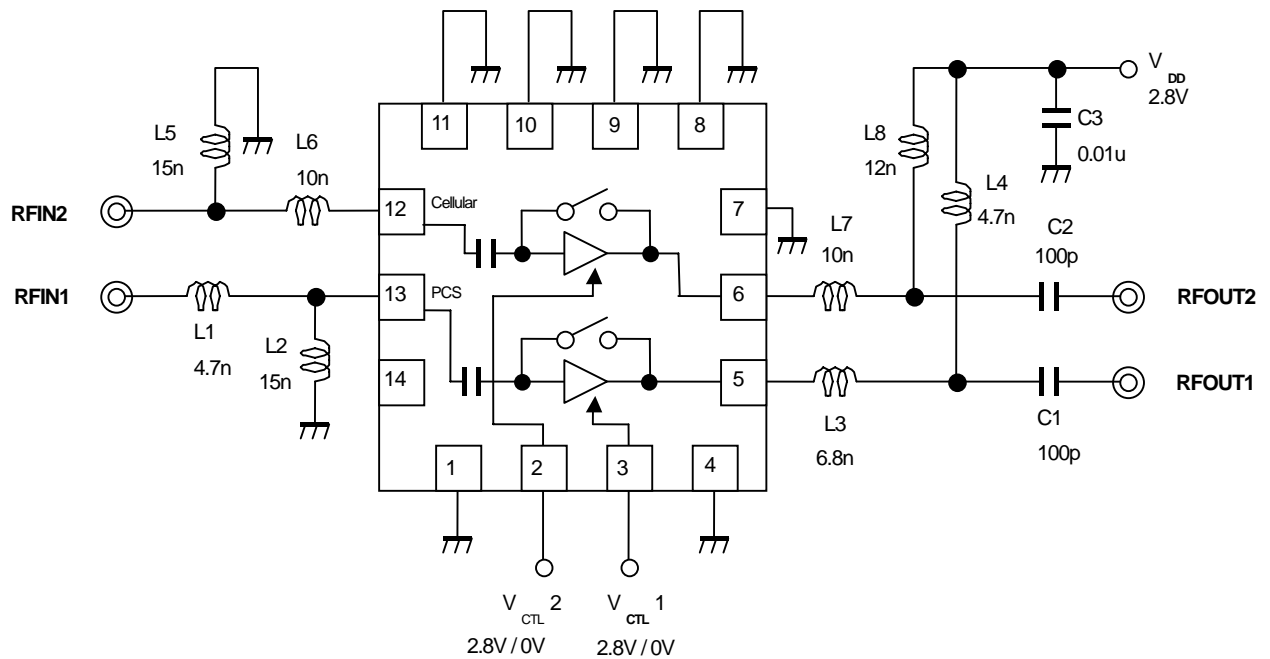


### K factor vs. frequency



# NJG1135MD7

## APPLICATION CIRCUIT

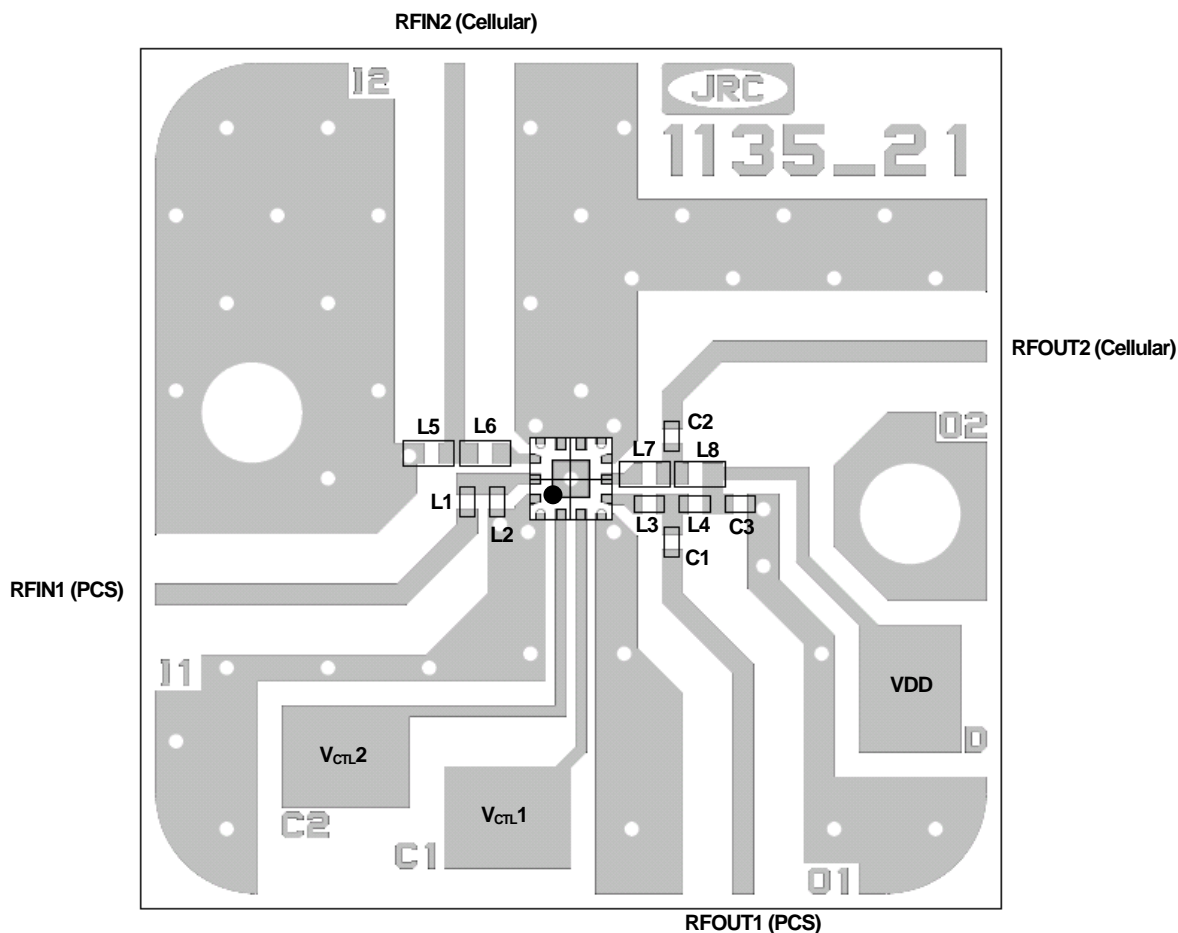


### Parts list

Parts ID	Comments
L1, L2, L4	MURATA (LQP03T Series)
L3	TDK (MLK0603 Series)
L5~L8	TAIYO-YUDEN (HK1005 Series)
C1~C3	MURATA (GRM03 Series)

## TEST PCB LAYOUT

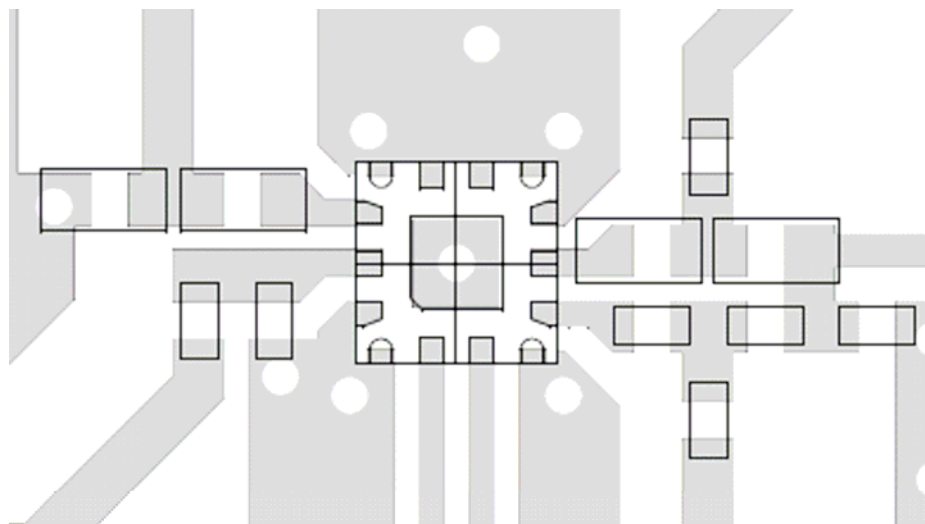
(TOP VIEW)



PCB (FR-4):  
 t=0.2mm  
 MICROSTRIP LINE WIDTH=0.4mm ( $Z_0=50\text{ohm}$ )  
 PCB SIZE=17.0mm x 17.0mm

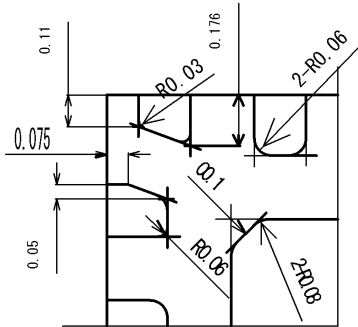
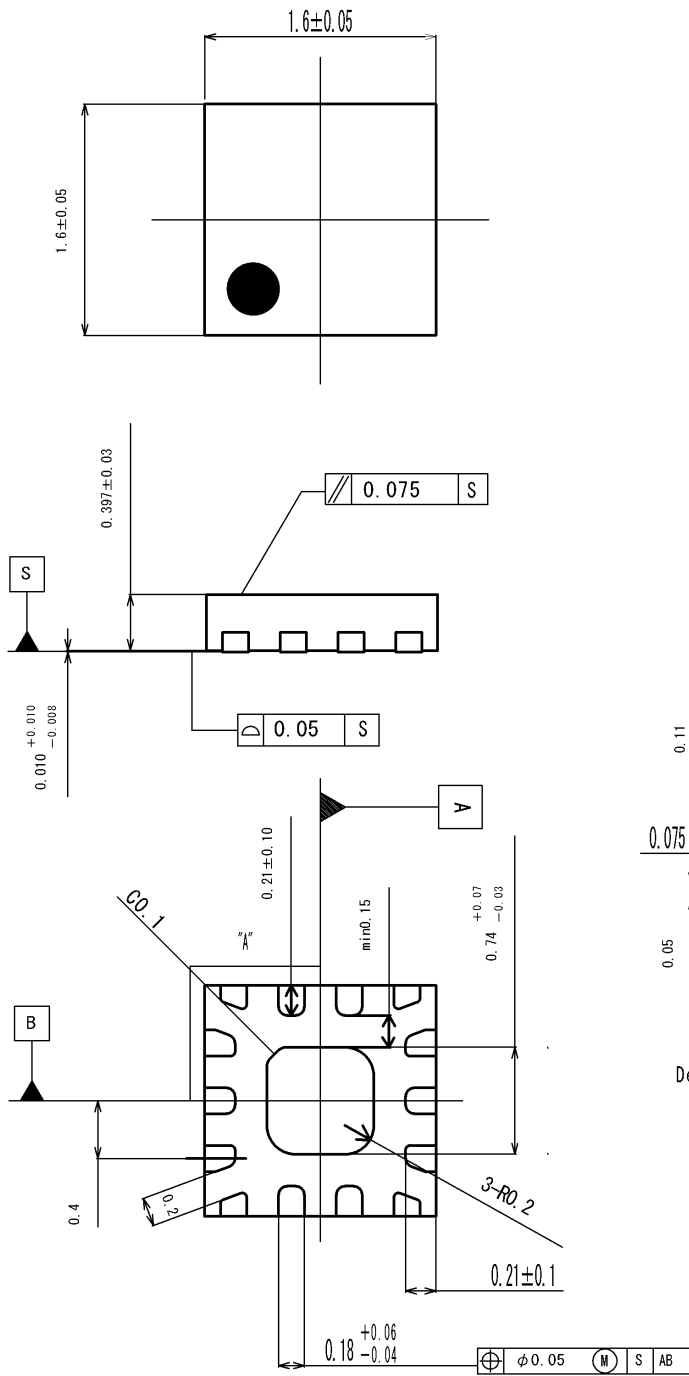
### PRECAUTION:

In order not to couple with terminal RFIN and RFOUT, please layout ground pattern under the IC.



# NJG1135MD7

## PACKAGE OUTLINE (EQFN14-D7)



Details of "A" part (x 2)

UNIT : mm

SUBSTRATE MATERIAL : Copper  
 TERMINAL FINISH : Sn-Bi plating  
 MOLDE MATERIAL : Epoxy resin  
 MASS (TYP.) : 0.0034 (g)

**Cautions on using this product**  
 This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.

**[CAUTION]**  
 The specifications on this databook are only given for information, without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.