

# Linear Voltage Regulator 3 A for DDR1, DDR2, DDR3, LPDDR3, DDR4 $V_{TT}$ Termination

## NCP51200, NCV51200

The NCP/NCV51200 is a source/sink Double Data Rate (DDR) termination regulator specifically designed for low input voltage and low-noise systems where space is a key consideration.

The NCP/NCV51200 maintains a fast transient response and only requires a minimum output capacitance of 20  $\mu$ F. The NCP/NCV51200 supports a remote sensing function and all power requirements for DDR  $V_{TT}$  bus termination. The NCP/NCV51200 can also be used in low-power chipsets and graphics processor cores that require dynamically adjustable output voltages.

The NCP/NCV51200 is available in the thermally-efficient DFN10 Exposed Pad wettable flank package, and is rated both Green and Pb-free.

### Features

- For Automotive Applications
- Input Voltage Rails: Supports 2.5 V, 3.3 V and 5 V Rails
- $PV_{CC}$  Voltage Range: 1.1 to 3.5 V
- Integrated Power MOSFETs
- Fast Load-Transient Response
- $P_{GOOD}$  – Logic output pin to Monitor  $V_{TT}$  Regulation
- EN – Logic input pin for Shutdown mode
- $V_{RI}$  – Reference Input Allows for Flexible Input Tracking Either Directly or Through Resistor Divider
- Remote Sensing ( $V_{TTS}$ )
- Built-in Soft Start, Under Voltage Lockout and Over Current Limit
- Thermal Shutdown
- Small, Low-Profile 10-pin, 3x3 DFN Package
- NCV51200MWTXG (SFS), NCV51200MLTXG (SLP); – Wettable Flank Options for Enhanced Optical Inspection
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable\*
- These Devices are Pb-Free and are RoHS Compliant

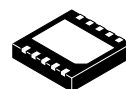
### Applications

- DDR Memory Termination
- Desktop PC's, Notebooks, and Workstations
- Servers and Networking equipment
- Telecom/Datacom, GSM Base Station
- Graphics Processor Core Supplies
- Set Top Boxes, LCD-TV/PDP-TV, Copier/Printers
- Chipset/RAM Supplies as Low as 0.5 V
- Active Bus Termination

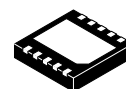


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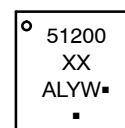


DFN10  
CASE 485C



DFNW10  
CASE 507AM

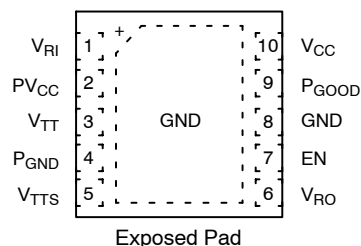
### MARKING DIAGRAMS



|    |                                  |
|----|----------------------------------|
| XX | = Specific Device Code           |
| A  | = Assembly Location              |
| L  | = Wafer Lot (Optional character) |
| Y  | = Year                           |
| W  | = Work Week                      |
| ▪  | = Pb-Free Package                |

(Note: Microdot may be in either location)

### PIN CONNECTION



### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 8 of this data sheet.

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## PIN FUNCTION DESCRIPTION

| Pin Number | Pin Name          | Pin Function                                                                                                                                                                                   |
|------------|-------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1          | V <sub>RI</sub>   | V <sub>TT</sub> External Reference Input ( set to V <sub>DDQ</sub> / 2 thru resistor network ).                                                                                                |
| 2          | PV <sub>CC</sub>  | Power input. Internally connected to the output source MOSFET.                                                                                                                                 |
| 3          | V <sub>TT</sub>   | Power Output of the Linear Regulator.                                                                                                                                                          |
| 4          | P <sub>GND</sub>  | Power Ground. Internally connected to the output sink MOSFET.                                                                                                                                  |
| 5          | V <sub>TTS</sub>  | V <sub>TT</sub> Sense Input. The V <sub>TTS</sub> pin provides accurate remote feedback sensing of V <sub>TT</sub> . Connect V <sub>TTS</sub> to the remote DDR termination bypass capacitors. |
| 6          | V <sub>RO</sub>   | Independent Buffered V <sub>TT</sub> Reference Output. Sources and sinks over 5 mA. Connect to GND thru 0.1 $\mu$ F ceramic capacitor.                                                         |
| 7          | EN                | Shutdown Control Input. CMOS compatible input. Logic high = enable, logic low = shutdown. Connect to V <sub>DDQ</sub> for normal operation.                                                    |
| 8          | GND               | Common Ground.                                                                                                                                                                                 |
| 9          | P <sub>GOOD</sub> | Power Good (Open Drain output).                                                                                                                                                                |
| 10         | V <sub>CC</sub>   | Analog power supply input. Connect to GND thru a 1 – 4.7 $\mu$ F ceramic capacitor.                                                                                                            |
|            | THERMAL PAD       | Pad for thermal connection. The exposed pad must be connected to the ground plane using multiple vias for maximum power dissipation performance.                                               |

## ABSOLUTE MAXIMUM RATINGS

| Rating                                                                                                               | Symbol             | Value        | Unit |
|----------------------------------------------------------------------------------------------------------------------|--------------------|--------------|------|
| V <sub>CC</sub> , PV <sub>CC</sub> , V <sub>TT</sub> , V <sub>TTS</sub> , V <sub>RI</sub> , V <sub>RO</sub> (Note 1) |                    | –0.3 to 6.0  | V    |
| EN, P <sub>GOOD</sub> (Note 1)                                                                                       |                    | –0.3 to 6.0  | V    |
| P <sub>GND</sub> to GND (Note 1)                                                                                     |                    | –0.3 to +0.3 | V    |
| Storage Temperature                                                                                                  | T <sub>STG</sub>   | –55 to 150   | °C   |
| Operating Junction Temperature Range                                                                                 | T <sub>J</sub>     | 150          | °C   |
| ESD Capability, Human Body Model (Note 2)                                                                            | ESD <sub>HBM</sub> | 2000         | V    |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following method:  
 ESD Human Body Model tested per AEC–Q100–002 (EIA/JESD22–A114)  
 ESD Machine Model tested per AEC–Q100–003 (EIA/JESD22–A115)  
 Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

## DISSIPATION RATINGS

| Package    | T <sub>A</sub> = 25°C Power Rating | Derating Factor above T <sub>A</sub> = 25°C | T <sub>A</sub> = +85°C Power Rating |
|------------|------------------------------------|---------------------------------------------|-------------------------------------|
| 10–Pin DFN | 1.92 W                             | 19 mW/°C                                    | 0.79 W                              |

## THERMAL INFORMATION

| Symbol                | Thermal Metric                                          | NCP51200 (*)<br>DFN 3x3mm<br>10 pins | Unit |
|-----------------------|---------------------------------------------------------|--------------------------------------|------|
| R <sub>θJA</sub>      | Junction–to–ambient thermal resistance                  | 53.9                                 | °C/W |
| R <sub>θJC(top)</sub> | Junction–to–case (top) thermal resistance               | 95.5                                 | °C/W |
| R <sub>θJB</sub>      | Junction–to–board thermal resistance (1mm from package) | 32.3                                 | °C/W |
| Ψ <sub>JT</sub>       | Junction–to–top thermal resistance                      | 4.3                                  | °C/W |
| Ψ <sub>JB</sub>       | Junction–to–board thermal resistance (1mm from package) | 32.3                                 | °C/W |
| R <sub>θJC(bot)</sub> | Junction–to–case (bot) thermal resistance               | 14.2                                 | °C/W |

\*1S2P JEDEC JESD51–7 PCB with 240 sqmm, 2 oz copper heat spreader.

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## RECOMMENED OPERATING CONDITIONS

| Rating                         | Symbol                                            | Value        | Unit |
|--------------------------------|---------------------------------------------------|--------------|------|
| Supply Voltage                 | $V_{CC}$                                          | 2.375 to 5.5 | V    |
| Voltage Range                  | $V_{RO}$                                          | -0.1 to 1.8  | V    |
|                                | $V_{RI}$                                          | 0.5 to 1.8   |      |
|                                | $PV_{CC}$ , $V_{TT}$ , $V_{TTS}$ , EN, $P_{GOOD}$ | -0.1 to 3.5  |      |
|                                | $P_{GND}$                                         | -0.1 to +0.1 |      |
| Operating Free-Air Temperature | $T_A$                                             | -40 to +125  | °C   |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## ELECTRICAL CHARACTERISTICS

-40°C ≤  $T_A$  ≤ 125°C;  $V_{CC}$  = 3.3 V;  $PV_{CC}$  = 1.8 V;  $V_{RI}$  =  $V_{TTS}$  = 0.9 V; EN =  $V_{CC}$ ;  $C_{OUT}$  = 3 x 10 μF (Ceramic); unless otherwise noted.

| Parameter | Conditions | Symbol | Min | Typ | Max | Units |
|-----------|------------|--------|-----|-----|-----|-------|
|-----------|------------|--------|-----|-----|-----|-------|

### Supply Current

|                            |                                                    |                |      |     |       |    |
|----------------------------|----------------------------------------------------|----------------|------|-----|-------|----|
| $V_{CC}$ Supply Current    | $T_A$ = +25°C, EN = 3.3 V, No Load                 | $I_{VCC}$      |      | 0.7 | 1     | mA |
| $V_{CC}$ Shutdown Current  | $T_A$ = +25°C, EN = 0 V, $V_{RI}$ = 0 V, No Load   | $I_{VCC SHD}$  |      | 65  | 80    | μA |
|                            | $T_A$ = +25°C, EN = 0 V, $V_{RI}$ > 0.4 V, No Load |                |      | 200 | 400   |    |
| $V_{CC}$ UVLO Threshold    | Wake-up, $T_A$ = +25°C                             | $V_{UVLO}$     | 2.15 | 2.3 | 2.375 | V  |
|                            | Hysteresis                                         |                |      | 50  |       | mV |
| $PV_{CC}$ Supply Current   | $T_A$ = +25°C, EN = 3.3 V, No Load                 | $I_{PVCC}$     |      | 1   | 50    | μA |
| $PV_{CC}$ Shutdown Current | $T_A$ = +25°C, EN = 0 V, No Load                   | $I_{PVCC SHD}$ |      | 0.1 | 50    | μA |

### $V_{TT}$ Output

|                                        |                                                             |           |     |     |     |    |
|----------------------------------------|-------------------------------------------------------------|-----------|-----|-----|-----|----|
| $V_{TT}$ Output Offset Voltage         | $V_{RO}$ = 1.25 V (DDR1), $I_{TT}$ = 0 A                    | $V_{OS}$  | -15 |     | +15 | mV |
|                                        | $V_{RO}$ = 0.9 V (DDR2), $I_{TT}$ = 0 A                     |           | -15 |     | +15 |    |
|                                        | AMN suffix, $V_{RO}$ = 0.6 V (DDR4), $I_{TT}$ = 0 A         |           | -15 |     | +15 |    |
|                                        | $PV_{CC}$ = 1.5 V, $V_{RO}$ = 0.75 V (DDR3), $I_{TT}$ = 0 A |           | -15 |     | +15 |    |
| $V_{TT}$ Voltage Tolerance to $V_{RO}$ | -2 A ≤ $I_{TT}$ ≤ +2 A                                      |           | -25 |     | +25 | mV |
| Source Current Limit                   | $V_{TTS}$ = 90% * $V_{RO}$                                  |           | 3   |     | 4.5 | A  |
| Sink Current Limit                     | $V_{TTS}$ = 110% * $V_{RO}$                                 |           | 3.5 |     | 5.5 | A  |
| Soft-start Current Limit Timeout       |                                                             | $T_{SS}$  |     | 200 |     | μs |
| Discharge MOSFET On-resistance         | $V_{RI}$ = 0 V, $V_{TT}$ = 0.3 V, EN = 0 V, $T_A$ = +25°C   | $R_{DIS}$ |     | 18  | 25  | Ω  |

### $V_{RI}$ – Input Reference

|                             |                 |               |     |     |     |    |
|-----------------------------|-----------------|---------------|-----|-----|-----|----|
| $V_{RI}$ Voltage Range      |                 | $V_{RI}$      | 0.5 |     | 1.8 | V  |
| $V_{RI}$ Input-bias Current | EN = 3.3 V      | $I_{RI}$      |     |     | +1  | μA |
| $V_{RI}$ UVLO Voltage       | $V_{RI}$ rising | $V_{RI UVLO}$ | 360 | 390 | 435 | mV |
|                             | Hysteresis      | $V_{RI HYS}$  |     | 60  |     |    |

### $V_{RO}$ – Output Reference

|                                        |                                                |  |          |    |     |    |
|----------------------------------------|------------------------------------------------|--|----------|----|-----|----|
| $V_{RO}$ Voltage                       |                                                |  | $V_{RI}$ |    |     | V  |
| $V_{RO}$ Voltage Tolerance to $V_{RI}$ | $I_{RO}$ = ±10 mA, 0.6 V ≤ $V_{RI}$ ≤ 1.25 V   |  | -15      |    | +15 | mV |
|                                        | AMN suffix, $I_{RO}$ = ±1 mA, $V_{RI}$ = 0.6 V |  | -12      |    | +12 |    |
| $V_{RO}$ Source Current Limit          | $V_{RO}$ = 0 V                                 |  | 10       | 40 |     | mA |
| $V_{RO}$ Sink Current Limit            | $V_{RO}$ = 0 V                                 |  | 10       | 40 |     | mA |

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## ELECTRICAL CHARACTERISTICS

$-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ ;  $V_{CC} = 3.3\text{ V}$ ;  $PV_{CC} = 1.8\text{ V}$ ;  $V_{RI} = V_{TTS} = 0.9\text{ V}$ ;  $EN = V_{CC}$ ;  $C_{OUT} = 3 \times 10\text{ }\mu\text{F}$  (Ceramic); unless otherwise noted.

| Parameter                                | Conditions                                                                                                   | Symbol | Min    | Typ  | Max     | Units |
|------------------------------------------|--------------------------------------------------------------------------------------------------------------|--------|--------|------|---------|-------|
| P <sub>GOOD</sub> – Powergood Comparator |                                                                                                              |        |        |      |         |       |
| P <sub>GOOD</sub> Lower Threshold        | (with respect to V <sub>RO</sub> )                                                                           |        | −23.5% | −20% | −17.5 % | V/V   |
| P <sub>GOOD</sub> Upper Threshold        | (with respect to V <sub>RO</sub> )                                                                           |        | 17.5%  | 20%  | 23.5%   |       |
| P <sub>GOOD</sub> Hysteresis             |                                                                                                              |        | 5%     |      |         |       |
| P <sub>GOOD</sub> Start-up Delay         | Start-up rising edge, V <sub>TTS</sub> within 15% of V <sub>RO</sub>                                         |        | 2      |      |         | ms    |
| P <sub>GOOD</sub> Leakage Current        | V <sub>TTS</sub> = V <sub>RI</sub> (P <sub>GOOD</sub> = True)<br>P <sub>GOOD</sub> = V <sub>CC</sub> + 0.2 V |        |        |      | 1       | μA    |
| P <sub>GOOD</sub> = False Delay          | V <sub>TTS</sub> is beyond ±20% P <sub>GOOD</sub> trip thresholds                                            |        | 10     |      |         | μs    |
| P <sub>GOOD</sub> Output Low Voltage     | I <sub>GOOD</sub> = 4 mA                                                                                     |        |        |      | 0.4     | V     |

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## ELECTRICAL CHARACTERISTICS

$-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ ;  $V_{CC} = 3.3\text{ V}$ ;  $PV_{CC} = 1.8\text{ V}$ ;  $V_{RI} = V_{TTS} = 0.9\text{ V}$ ;  $\text{EN} = V_{CC}$ ;  $C_{OUT} = 3 \times 10\text{ }\mu\text{F}$  (Ceramic); unless otherwise noted.

| Parameter             | Conditions                          | Symbol      | Min | Typ | Max | Units         |
|-----------------------|-------------------------------------|-------------|-----|-----|-----|---------------|
| Logic Input Threshold | EN Logic high                       | $V_{IH}$    | 1.7 |     |     | V             |
|                       | EN Logic low                        | $V_{IL}$    |     |     | 0.3 | V             |
| Hysteresis Voltage    | EN pin                              | $V_{ENHYS}$ | 0.5 |     |     | V             |
| Logic Leakage Current | EN pin, $T_A = +25^{\circ}\text{C}$ | $I_{LEAK}$  | -1  |     | +1  | $\mu\text{A}$ |

## Thermal Shutdown

|                              |  |          |     |  |                    |
|------------------------------|--|----------|-----|--|--------------------|
| Thermal Shutdown Temperature |  | $T_{SD}$ | 150 |  | $^{\circ}\text{C}$ |
| Thermal Shutdown Hysteresis  |  | $T_{SH}$ | 25  |  | $^{\circ}\text{C}$ |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

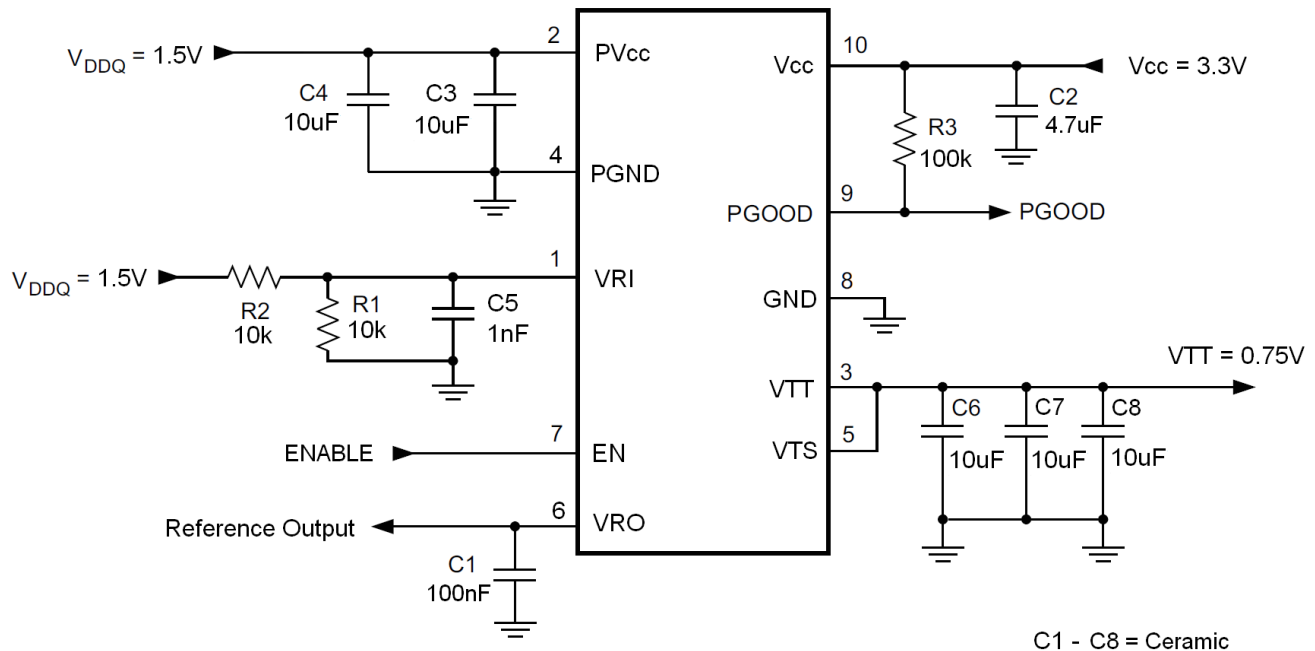


Figure 1. Typical DDR-3 Application Schematic

# NCP51200

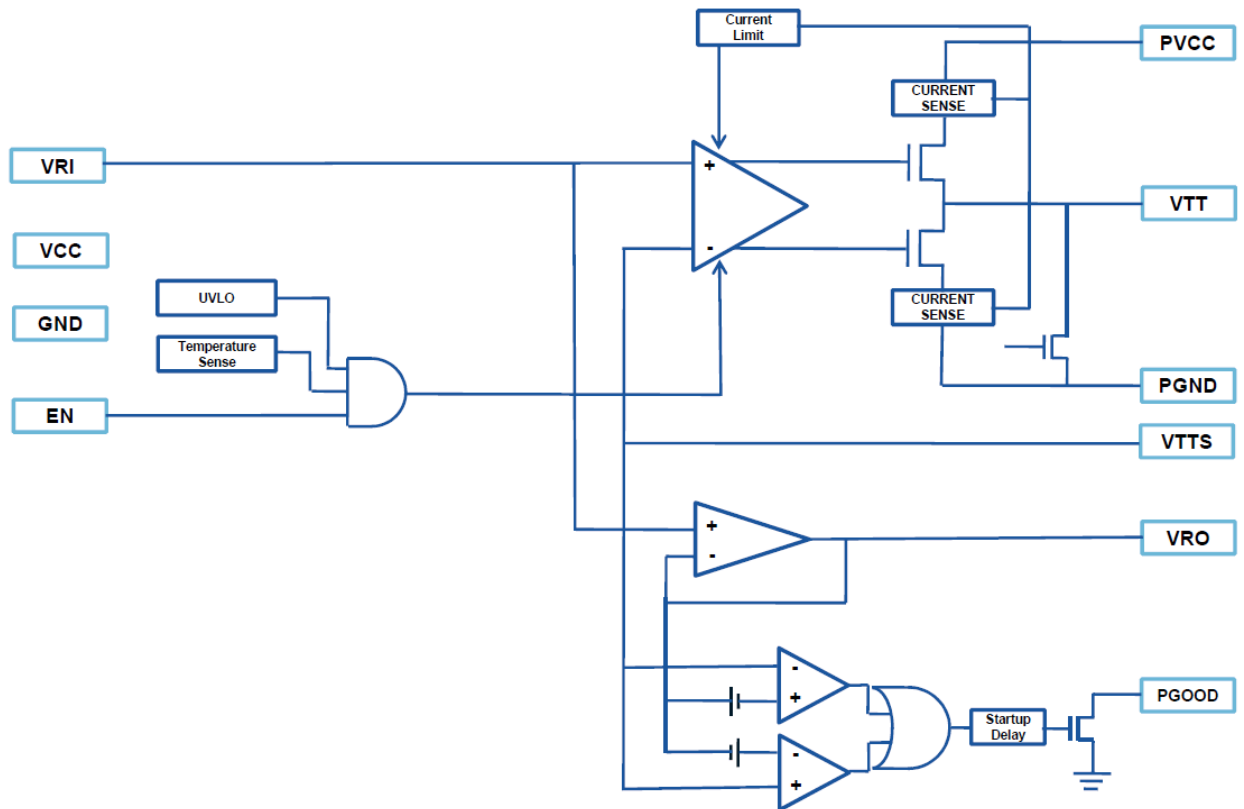


Figure 2. Block Diagram

**General**

The NCP51200 is a sink/source tracking termination regulator specifically designed for low input voltage and low external component count systems where space is a key application parameter. The NCP51200 integrates a high-performance, low-dropout (LDO) linear regulator that is capable of both sourcing and sinking current. The LDO regulator employs a fast feedback loop so that small ceramic capacitors can be used to support the fast load transient response. To achieve tight regulation with minimum effect of trace resistance, a remote sensing terminal,  $V_{TTS}$ , should be connected to the positive terminal of the output capacitors as a separate trace from the high current path from  $V_{TT}$ .

 **$V_{RI}$  – Generation of Internal Voltage Reference**

The output voltage,  $V_{TT}$ , is regulated to  $V_{RO}$ . When  $V_{RI}$  is configured for standard DDR termination applications,  $V_{RI}$  can be set by an external equivalent ratio voltage divider connected to the memory supply bus ( $V_{DDQ}$ ). The NCP51200 supports  $V_{RI}$  voltage from 0.5 V to 1.8 V, making it versatile and ideal for many types of low-power LDO applications.

 **$V_{RO}$  – Reference Output**

When it is configured for DDR termination applications,  $V_{RO}$  generates the DDR  $V_{TT}$  reference voltage for the memory application. It is capable of supporting both a sourcing and sinking load of 10 mA.  $V_{RO}$  becomes active when  $V_{RI}$  voltage rises to 435 mV and  $V_{CC}$  is above the UVLO threshold. When  $V_{RO}$  is less than 360 mV, it is disabled and subsequently discharges to GND through an internal 10 k $\Omega$  MOSFET.  $V_{RO}$  is independent of the EN pin state.

**Soft Start**

The soft-start function of the  $V_{TT}$  pin is achieved via a current clamp. The current clamp allows the output capacitors to be charged with low and constant current, providing a linear ramp-up of the output voltage. When

$V_{TT}$  is outside of the power good window, the current clamp level is one-half of the full over-current limit (OCL) level. When  $V_{TT}$  rises or falls within the  $P_{GOOD}$  window, the current clamp level switches to the full OCL level.

The soft-start function is completely symmetrical; it works not only from GND to the  $V_{RO}$  voltage but also from  $PV_{CC}$  to the  $V_{RO}$  voltage.

**EN – Enable Control**

When EN is driven high, the NCP51200  $V_{TT}$  regulator begins normal operation. When EN is driven low,  $V_{TT}$  is discharged to GND through an internal 18- $\Omega$  MOSFET.  $V_{REF}$  remains on when EN is driven low.

 **$P_{GOOD}$  – PowerGood**

The NCP51200 provides an open-drain  $P_{GOOD}$  output that goes high when the  $V_{TT}$  output is within  $\pm 20\%$  of  $V_{RO}$ .  $P_{GOOD}$  de-asserts within 10  $\mu$ s after the output exceeds the

limits of the PowerGood window. During initial  $V_{TT}$  startup,  $P_{GOOD}$  asserts high 2 ms after the  $V_{TT}$  enters power good window. Because  $P_{GOOD}$  is an open-drain output, a 100 k $\Omega$  pull-up resistor between  $P_{GOOD}$  and a stable active supply voltage rail is required.

The LDO has a constant over-current limit (OCL). Note that the OCL level reduces by one-half when the output voltage is not within the power good window. This reduction is non-latch protection. For  $V_{CC}$  under-voltage lockout (UVLO) protection, the NCP51200 monitors  $V_{CC}$  voltage. When the  $V_{CC}$  voltage is lower than the UVLO threshold voltage, both the  $V_{TT}$  and  $V_{RO}$  regulators are powered off. This shutdown is also non-latch protection.

**Thermal Shutdown with Hysteresis**

If the NCP51200 is to operate in elevated temperatures for long durations, care should be taken to ensure that the maximum operating junction temperature is not exceeded. To guarantee safe operation, the NCP51200 provides on-chip thermal shutdown protection. When the chip junction temperature exceeds 150°C, the part will shutdown. When the junction temperature falls back to 125°C, the device resumes normal operation. If the junction temperature exceeds the thermal shutdown threshold then the  $V_{TT}$  and  $V_{RO}$  regulators are both shut off, discharged by the internal discharge MOSFETs. The shutdown is a non-latch protection.

**Tracking Startup and Shutdown**

The NCP51200 also supports tracking startup and shutdown when EN is tied directly to the system bus and not used to turn on or turn off the device. During tracking startup,  $V_{TT}$  follows  $V_{RO}$  once  $V_{RI}$  voltage is greater than 435 mV.  $V_{RI}$  follows the rise of  $V_{DDQ}$  memory supply rail via a voltage divider. The typical soft-start time for the  $V_{DDQ}$  memory supply rail is approximately 3 ms, however it may vary depending on the system configuration. The SS time of the  $V_{TT}$  output no longer depends on the OCL setting, but it is a function of the SS time of the  $V_{DDQ}$  memory supply rail.  $P_{GOOD}$  is asserted 2 ms after  $V_{TT}$  is within  $\pm 20\%$  of  $V_{RO}$ . During tracking shutdown,  $V_{TT}$  falls following  $V_{RO}$  until  $V_{RO}$  reaches 360 mV. Once  $V_{RO}$  falls below 360 mV, the internal discharge MOSFETs are turned on and quickly discharge both  $V_{RO}$  and  $V_{TT}$  to GND.  $P_{GOOD}$  is de-asserted once  $V_{TT}$  is beyond the  $\pm 20\%$  range of  $V_{RO}$ .

 **$V_{TT}$  Output Capacitor**

The NCP51200 requires the output capacitor connected as close as possible to the  $V_{TT}$  and PGND pins. The regulator has been designed to remain stable with output capacitor's effective capacitance in range from 20  $\mu$ F to 1000  $\mu$ F. The ceramic X7R or X5R type is recommended due to its low capacitance variations over the specified temperature range and low ESR and ESL. When selecting the capacitor value the changes with temperature and DC bias voltage needs to be taken into account. Especially for small package size

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capacitors, the effective capacitance drops rapidly with the applied DC bias voltage (refer the capacitor's datasheet for details). Larger capacitance and lower ESR improves the load transient response and PSRR. In the PCB layout, design the traces short and wide and place the capacitor at the same PCB layer as the device (do not use layers changing for the traces).

### PVCC Input Capacitor

Power input capacitor, connected as close as possible to PVCC and PGND pins, is also necessary to ensure device stability and good transient response. The value of the input capacitor should be 10  $\mu$ F or greater (max. value is not

limited). This capacitor provides needed energy during load transients for output capacitor re-charging and from this point of view, the higher value is better. The good starting value is the half of the output capacitor value. The rules mentioned at VTT capacitor paragraph are applicable for PVCC capacitor as well.

### VCC Input Capacitor

Add a ceramic capacitor, connected as close as possible to VCC and GND pins. The X7R or X5R capacitor should be used with a value in range from 1  $\mu$ F to 10  $\mu$ F is recommended.

### DEVICE ORDERING INFORMATION

| Device         | Marking Code | Package             | Feature                       | Shipping <sup>†</sup> |
|----------------|--------------|---------------------|-------------------------------|-----------------------|
| NCP51200MNTXG  | 51200        | DFN10<br>(Pb-Free)  | Non-Wettable Flank            | 3000 / Tape & Reel    |
| NCV51200MNTXG* | 51200<br>MN  |                     |                               |                       |
| NCV51200MWTXG* | 51200<br>MW  |                     | Wettable Flank<br>SFS Process | 3000 / Tape & Reel    |
| NCV51200MLTXG* | 51200<br>ML  | DFNW10<br>(Pb-Free) | Wettable Flank<br>SLP Process | 3000 / Tape & Reel    |
| NCP51200AMNTXG | 51200<br>A   | DFN10<br>(Pb-Free)  | Non-Wettable Flank            | 3000 / Tape & Reel    |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.



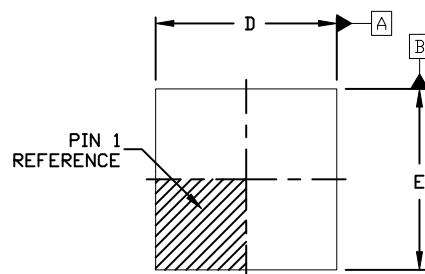
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



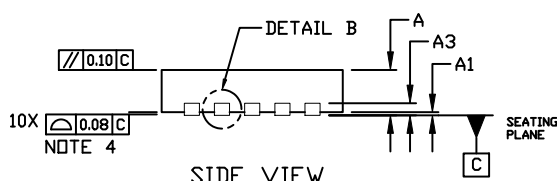
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## DFN10, 3x3, 0.5P CASE 485C ISSUE F

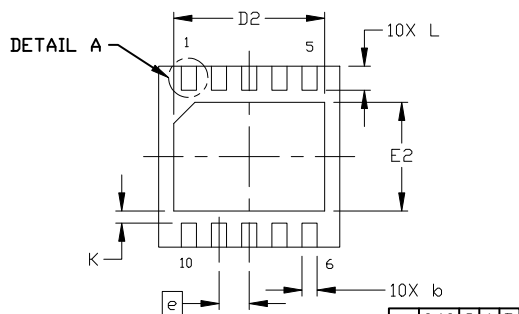
DATE 16 DEC 2021



TOP VIEW

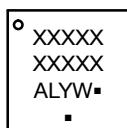


SIDE VIEW



BOTTOM VIEW

### GENERIC MARKING DIAGRAM\*



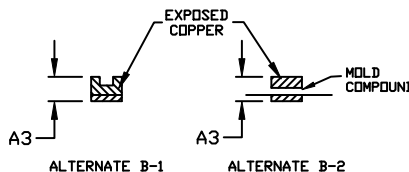
XXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

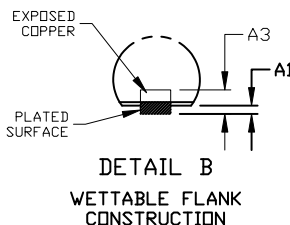
### NOTES:

1. DIMENSION AND TOLERANCING PER ASME Y14.5, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION  $b$  APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TERMINAL  $b$  MAY HAVE MOLD COMPOUND MATERIAL ALONG SIDE EDGE. MOLD FLASH MAY NOT EXCEED 30 MICRONS ONTO BOTTOM SURFACE OF TERMINAL.
6. FOR DEVICE OPN CONTAINING W OPTION, DETAIL A AND DETAIL B ALTERNATE CONSTRUCTIONS ARE NOT APPLICABLE. WETTABLE FLANK CONSTRUCTION IS DETAIL B AS SHOWN ON SIDE VIEW OF PACKAGE.

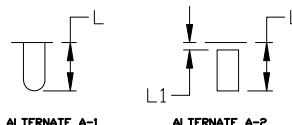


DETAIL B

ALTERNATE CONSTRUCTION



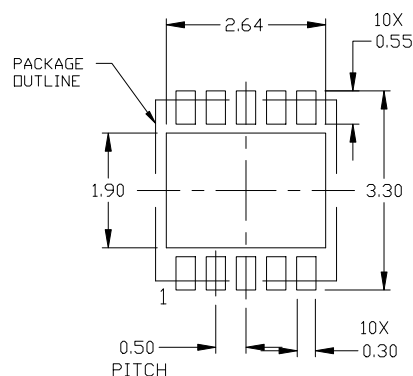
DETAIL B  
WETTABLE FLANK  
CONSTRUCTION



DETAIL A

ALTERNATE CONSTRUCTION

| DIM | MILLIMETERS |      |      |
|-----|-------------|------|------|
|     | MIN.        | NDM. | MAX. |
| A   | 0.80        | 0.90 | 1.00 |
| A1  | 0.00        | ---  | 0.05 |
| A3  | 0.20 REF    |      |      |
| b   | 0.18        | 0.23 | 0.30 |
| D   | 2.90        | 3.00 | 3.10 |
| D2  | 2.40        | 2.50 | 2.60 |
| E   | 2.90        | 3.00 | 3.10 |
| E2  | 1.70        | 1.80 | 1.90 |
| e   | 0.50 BSC    |      |      |
| K   | 0.20 REF    |      |      |
| L   | 0.30        | 0.40 | 0.50 |
| L1  | ---         | ---  | 0.03 |



### RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

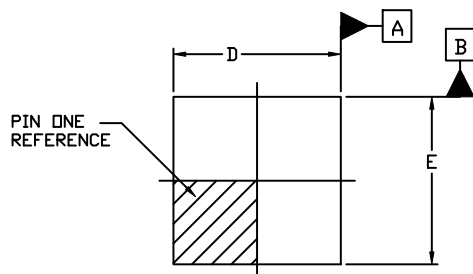
|                  |                             |                                                                                                                                                                                  |
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| DESCRIPTION:     | DFN10, 3X3 MM, 0.5 MM PITCH | PAGE 1 OF 1                                                                                                                                                                      |

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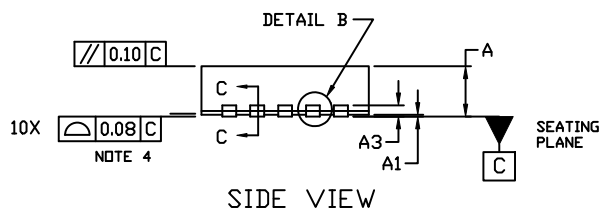


### DFNW10 3x3, 0.5P CASE 507AM ISSUE A

DATE 12 JUN 2018



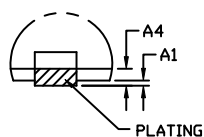
TOP VIEW



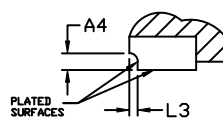
SIDE VIEW

#### NOTES:

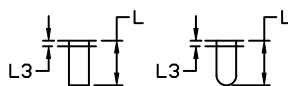
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION  $b$  APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.



DETAIL B



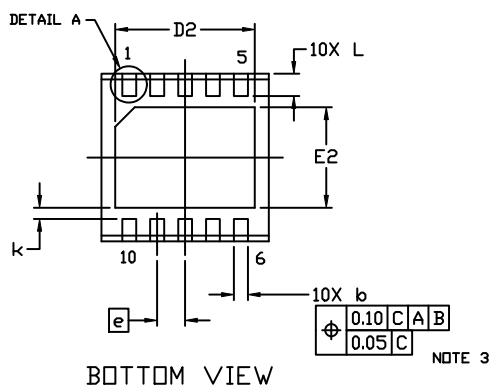
SECTION C-C



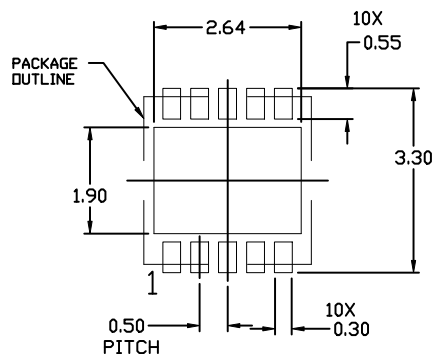
ALTERNATE CONSTRUCTION

DETAIL A

| DIM | MILLIMETERS |      |      |
|-----|-------------|------|------|
|     | MIN.        | NOM. | MAX. |
| A   | 0.80        | 0.90 | 1.00 |
| A1  | 0.00        | ---  | 0.05 |
| A3  | 0.20 REF    |      |      |
| A4  | 0.10        | ---  | ---  |
| b   | 0.20        | 0.25 | 0.30 |
| D   | 2.85        | 3.00 | 3.15 |
| D2  | 2.40        | 2.50 | 2.60 |
| E   | 2.85        | 3.00 | 3.15 |
| E2  | 1.70        | 1.80 | 1.90 |
| e   | 0.50 BSC    |      |      |
| k   | 0.19 REF    |      |      |
| L   | 0.35        | 0.40 | 0.45 |
| L3  | ---         | 0.05 | 0.10 |

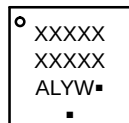


BOTTOM VIEW



RECOMMENDED MOUNTING FOOTPRINT

#### GENERIC MARKING DIAGRAM\*



XXXXX = Specific Device Code  
 A = Assembly Location  
 L = Wafer Lot  
 Y = Year  
 W = Work Week  
 ■ = Pb-Free Package  
 (Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

|                  |                  |                                                                                                                                                                                  |
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| DESCRIPTION:     | DFNW10 3x3, 0.5P | PAGE 1 OF 1                                                                                                                                                                      |

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