

NCV4264

Linear Regulator, 100 mA, Low Dropout

The NCV4264 is a wide input range, precision 3.3 V and 5.0 V fixed output, low dropout integrated voltage regulator with a full load current rating of 100 mA.

The output voltage is accurate within $\pm 2.0\%$, and maximum dropout voltage is 500 mV at 100 mA load current.

It is internally protected against 45 V input transients, input supply reversal, output overcurrent faults, and excess die temperature. No external components are required to enable these features.

Features

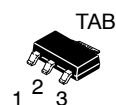
- 3.3 V and 5.0 V Fixed Output
- $\pm 2.0\%$ Output Accuracy, Over Full Temperature Range
- Quiescent Current 400 μA at $I_{\text{OUT}} = 1.0 \text{ mA}$
- 500 mV Maximum Dropout Voltage at 100 mA Load Current
- Wide Input Voltage Operating Range of 4.5 V to 45 V
- Internal Fault Protection
 - ◆ -42 V Reverse Voltage
 - ◆ Short Circuit/Overcurrent
 - ◆ Thermal Overload
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These are Pb-Free Devices



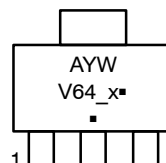
ON Semiconductor®

www.onsemi.com

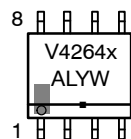
MARKING DIAGRAMS



**SOT-223
ST SUFFIX
CASE 318E**



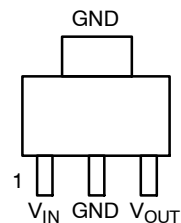
**SO-8
D SUFFIX
CASE 751**



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
x = 3 (3.3 V Version)
= 5 (5.0 V Version)
▪ = Pb-Free Package

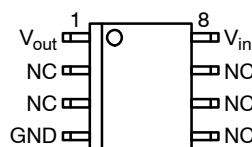
(Note: Microdot may be in either location)

PIN CONNECTIONS



SOT-223

(Top View)



SO-8

(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

NCV4264

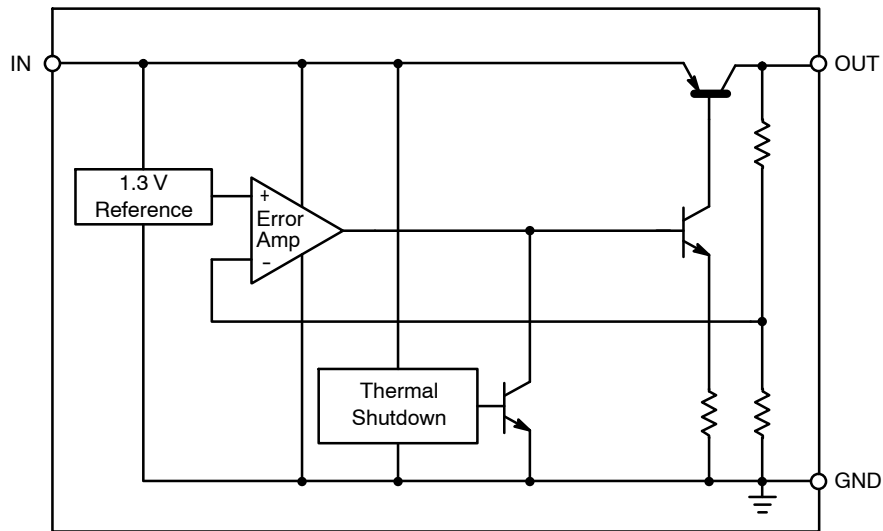


Figure 1. Block Diagram

PIN FUNCTION DESCRIPTION

Pin No. SOT-223	Pin No. SO-8	Symbol	Function
1	8	V_{IN}	Unregulated input voltage; 4.5 V to 45 V.
2	4	GND	Ground; substrate.
3	1	V_{OUT}	Regulated output voltage; collector of the internal PNP pass transistor.
TAB	–	GND	Ground; substrate and best thermal connection to the die.
–	2,3,5,6,7	NC	Not Connected

MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
V_{IN} , DC Input Voltage	V_{IN}	–42	+45	V
V_{OUT} , DC Voltage	V_{OUT}	–0.3	+16	V
Storage Temperature	T_{stg}	–55	+150	°C
Moisture Sensitivity Level	MSL	3	1	–
ESD Capability, Human Body Model (Note 1)	V_{ESDHB}	4000	–	V
ESD Capability, Machine Model (Note 1)	V_{ESDMIM}	200	–	V
Lead Temperature Soldering Reflow (SMD Styles Only), Lead Free (Note 2)	T_{sld}	–	265 pk	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series incorporates ESD protection and is tested by the following methods:

ESD HBM tested per AEC-Q100-002 (EIA/JESD22-A 114C)

ESD MM tested per AEC-Q100-003 (EIA/JESD22-A 115C)

2. Lead Free, 60 sec – 150 sec above 217°C, 40 sec max at peak.

OPERATING RANGE

Pin Symbol, Parameter	Symbol	Min	Max	Unit
V_{IN} , DC Input Operating Voltage	V_{IN}	4.5	+45	V
Junction Temperature Operating Range	T_J	–40	+150	°C

THERMAL RESISTANCE

Parameter	Symbol	Min	Max	Unit
Junction-to-Ambient SOT-223	$R_{\theta JA}$	–	99 (Note 3)	°C/W
Junction-to-Case SOT-223	$R_{\theta JC}$	–	17	
Junction-to-Ambient SO-8	$R_{\theta JA}$	–	162 (Note 3)	°C/W
Junction-to-Lead2 SO-8	Ψ_{JL2}	–	45	

3. 1 oz., 100 mm² copper area.

ELECTRICAL CHARACTERISTICS ($V_{IN} = 13.5\text{ V}$, $T_J = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$, unless otherwise noted.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage 5.0 V Version	V_{OUT}	$5.0\text{ mA} \leq I_{OUT} \leq 100\text{ mA}$ (Note 4) $6.0\text{ V} \leq V_{IN} \leq 28\text{ V}$	4.900	5.000	5.100	V
Output Voltage 3.3 V Version	V_{OUT}	$5.0\text{ mA} \leq I_{OUT} \leq 100\text{ mA}$ (Note 4) $4.5\text{ V} \leq V_{IN} \leq 28\text{ V}$	3.234	3.300	3.366	V
Line Regulation 5.0 V Version	ΔV_{OUT} vs. V_{IN}	$I_{OUT} = 5.0\text{ mA}$ $6.0\text{ V} \leq V_{IN} \leq 28\text{ V}$	–30	5.0	+30	mV
Line Regulation 3.3 V Version	ΔV_{OUT} vs. V_{IN}	$I_{OUT} = 5.0\text{ mA}$ $4.5\text{ V} \leq V_{IN} \leq 28\text{ V}$	–30	5.0	+30	mV
Load Regulation	ΔV_{OUT} vs. I_{OUT}	$5.0\text{ mA} \leq I_{OUT} \leq 100\text{ mA}$ (Note 4)	–40	5.0	+40	mV
Dropout Voltage 5.0 V Version	$V_{IN}-V_{OUT}$	$I_{OUT} = 100\text{ mA}$ (Notes 4 & 5)	–	275	500	mV
Dropout Voltage 3.3 V Version	$V_{IN}-V_{OUT}$	$I_{OUT} = 100\text{ mA}$ (Notes 4 & 7)	–	–	1.266	V
Quiescent Current	I_q	$I_{OUT} = 1.0\text{ mA}$	–	100	400	μA
Active Ground Current	$I_{G(ON)}$	$I_{OUT} = 100\text{ mA}$ (Note 4)	–	4	15	mA
Power Supply Rejection	PSRR	$V_{RIPPLE} = 0.5\text{ V}_{P-P}$, $F = 100\text{ Hz}$	–	67	–	dB
Output Capacitor for Stability 5.0 V Version	C_{OUT} ESR	$I_{OUT} = 1.0\text{ mA}$ to 100 mA (Note 4)	10	–	9.0	μF Ω
Output Capacitor for Stability 3.3 V Version	C_{OUT} ESR	$I_{OUT} = 1.0\text{ mA}$ to 100 mA (Note 4)	22 –	– –	– 16	μF Ω

PROTECTION

Current Limit	$I_{OUT(LIM)}$	$V_{OUT} = 4.5\text{ V}$ (5.0 V Version) (Note 4) $V_{OUT} = 3.0\text{ V}$ (3.3 V Version) (Note 4)	150 150	– –	500 500	mA
Short Circuit Current Limit	$I_{OUT(SC)}$	$V_{OUT} = 0\text{ V}$ (Note 4)	40	–	500	mA
Thermal Shutdown Threshold	T_{TSD}	(Note 6)	150	–	200	°C

4. Use pulse loading to limit power dissipation.

5. Dropout voltage = $(V_{IN}-V_{OUT})$, measured when the output voltage has dropped 100 mV relative to the nominal value obtained with $V_{IN} = 13.5\text{ V}$.

6. Not tested in production. Limits are guaranteed by design.

7. $V_{DO} = V_{IN} - V_{OUT}$. For output voltage set to $< 4.5\text{ V}$, V_{DO} will be constrained by the minimum input voltage.

NCV4264

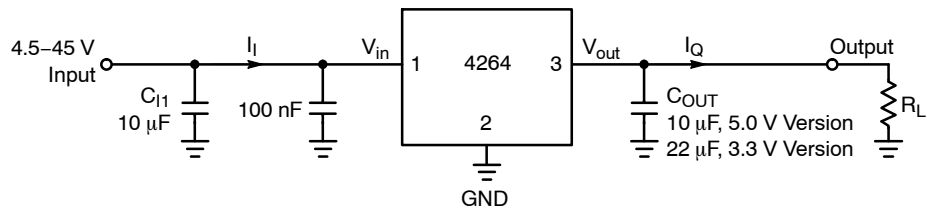


Figure 2. Measurement Circuit

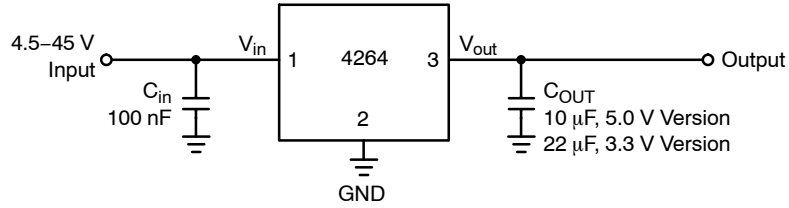
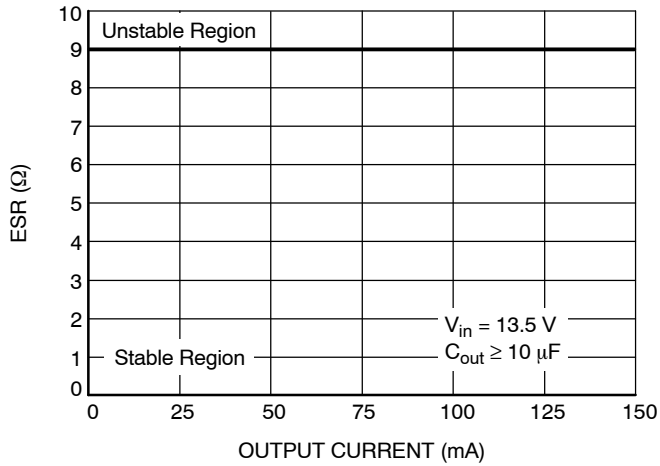
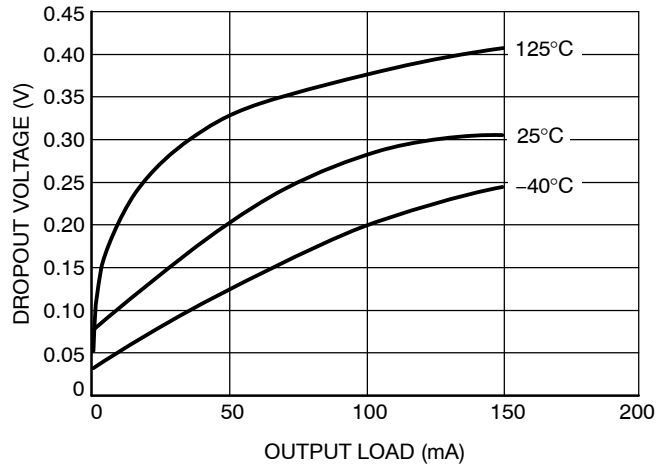


Figure 3. Applications Circuit

TYPICAL CHARACTERISTIC CURVES – 5 V Version



**Figure 4. ESR Characterization
(5 V Version)**



**Figure 5. Dropout Voltage vs. Output Load
(5 V Version)**

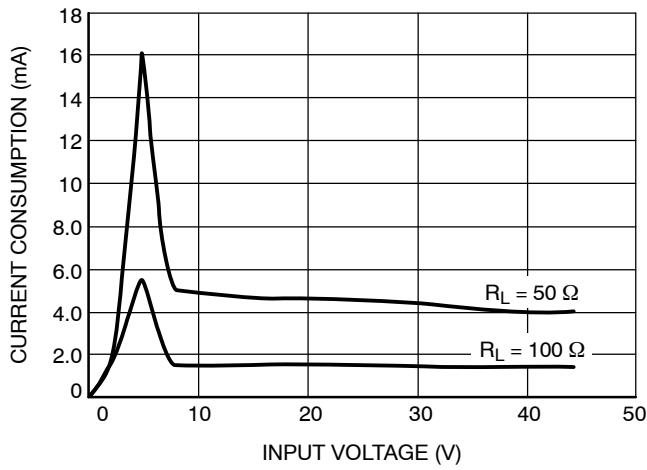


Figure 6. Current Consumption vs. Input Voltage (5 V Version)

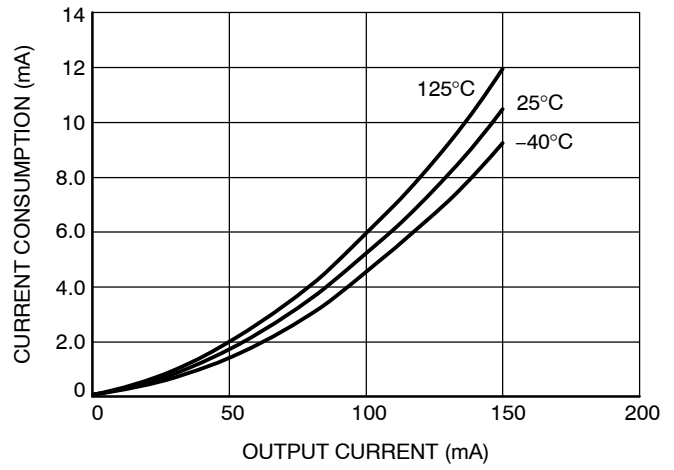


Figure 7. Current Consumption vs. Output Current (5 V Version)

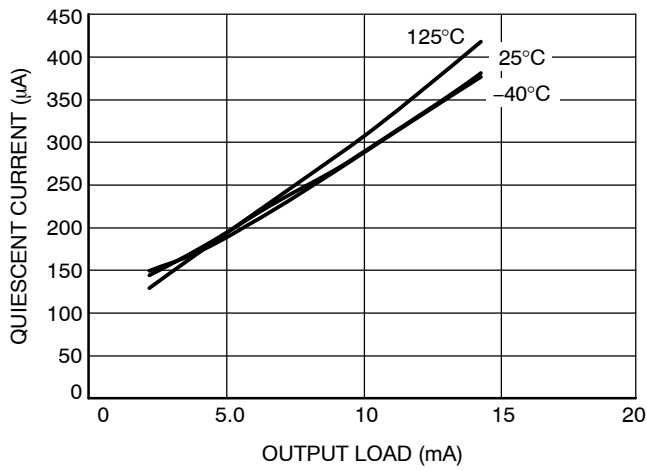


Figure 8. Quiescent Current vs. Output Load (5 V Version)

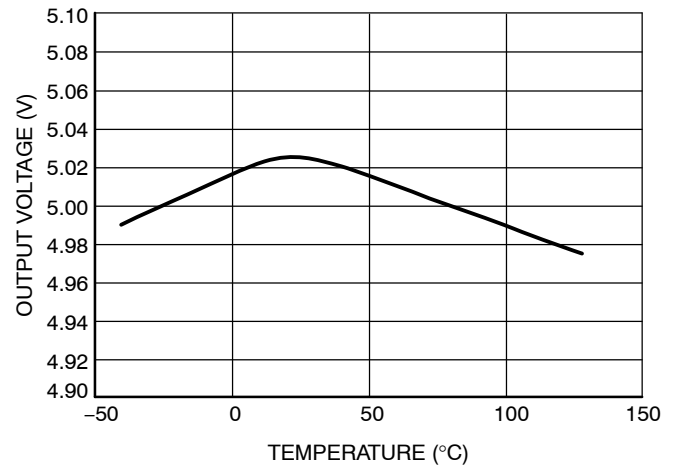


Figure 9. Output Voltage vs. Temperature (5 V Version)

TYPICAL CHARACTERISTIC CURVES – 5 V Version

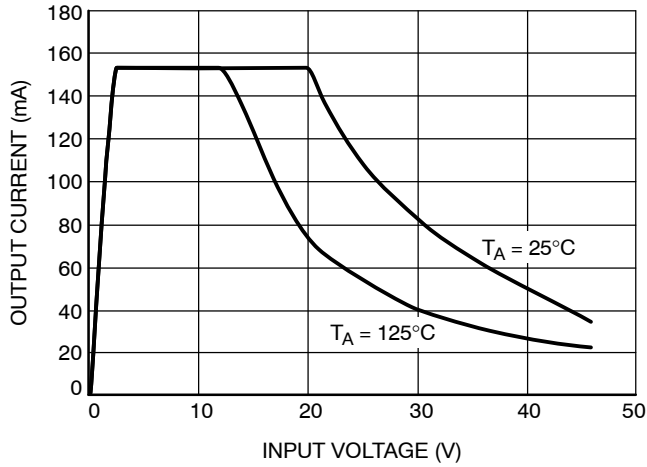


Figure 10. Output Current vs. Input Voltage (5 V Version)

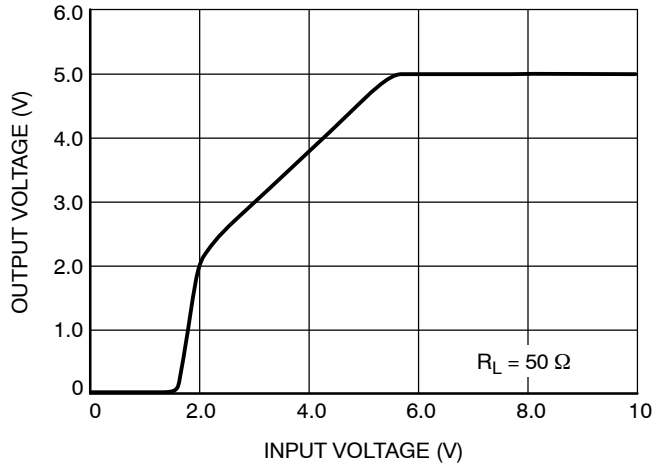


Figure 11. Input Voltage vs. Output Voltage (5 V Version)

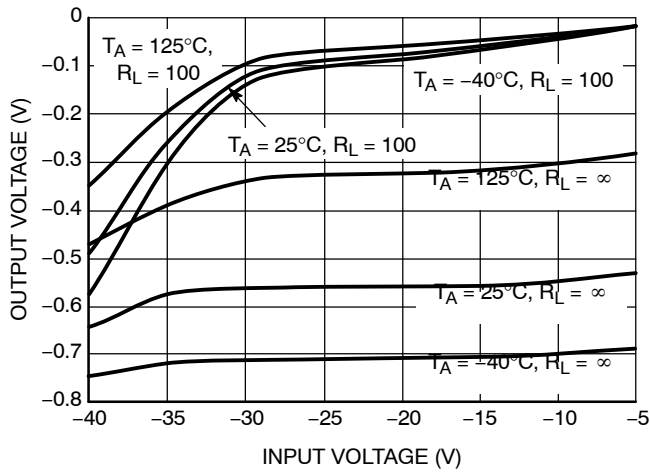
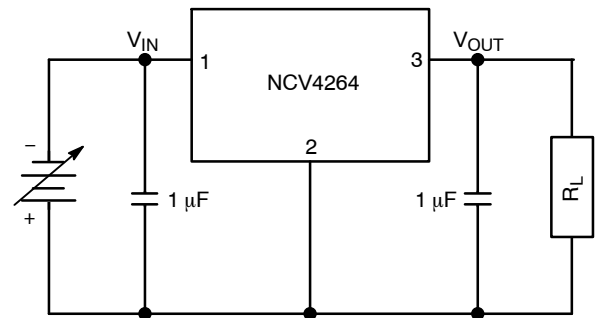


Figure 12. Reverse Voltage Characteristics (5 V Version)



MEASUREMENT CIRCUIT

TYPICAL CHARACTERISTIC CURVES – 3.3 V Version

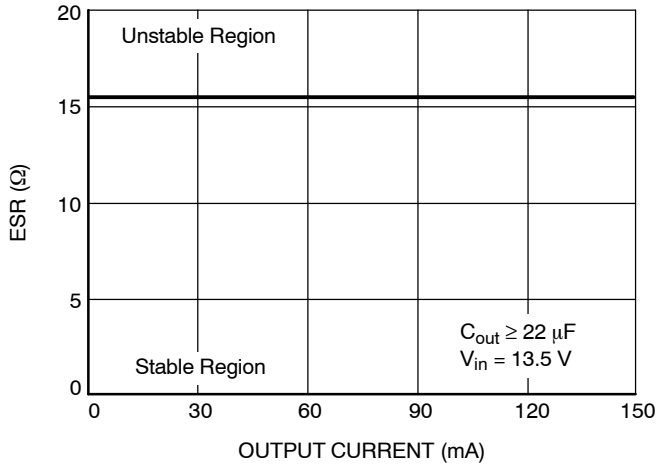


Figure 13. ESR Stability vs. Output Current (3.3 V Version)

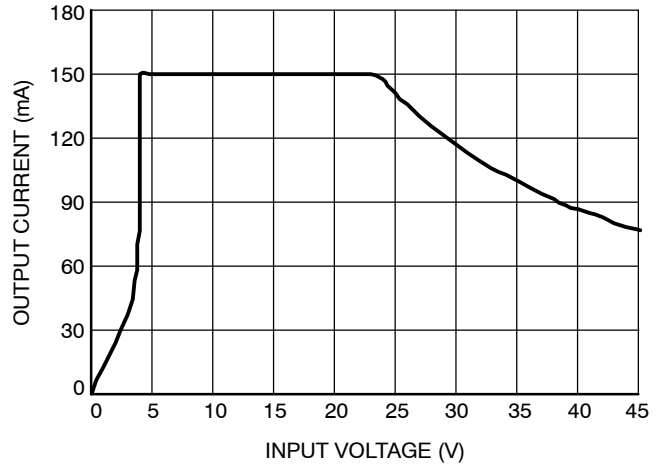


Figure 14. Output Current vs. Input Voltage (3.3 V Version)

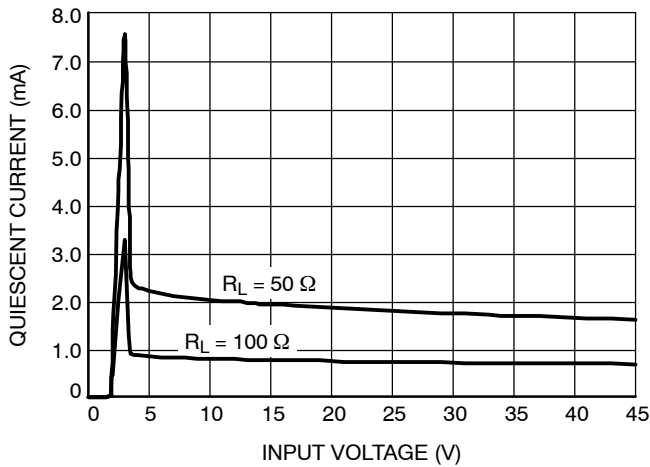


Figure 15. Input Voltage vs. Quiescent Current (3.3 V Version)

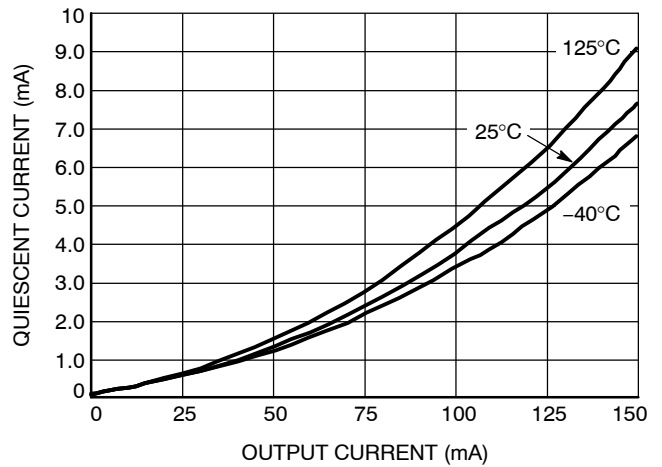


Figure 16. Quiescent Current vs. Output Current (3.3 V Version)

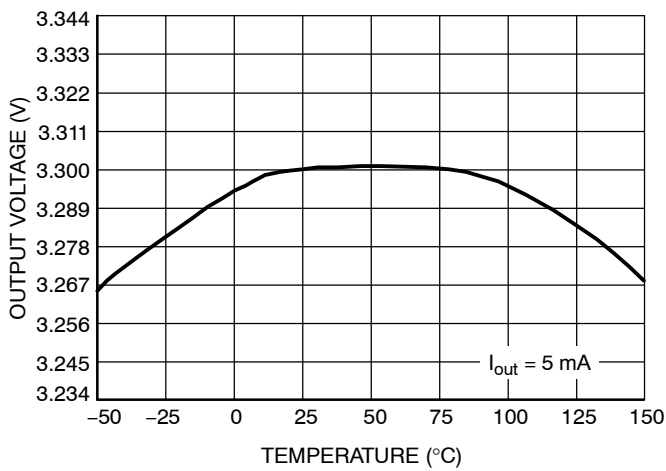


Figure 17. Output Voltage vs. Temperature (3.3 V Version)

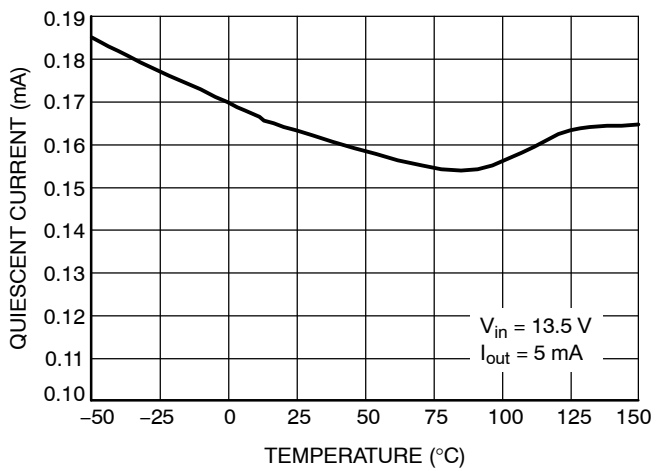


Figure 18. Quiescent Current vs. Temperature (3.3 V Version)

TYPICAL CHARACTERISTIC CURVES – 3.3 V Version

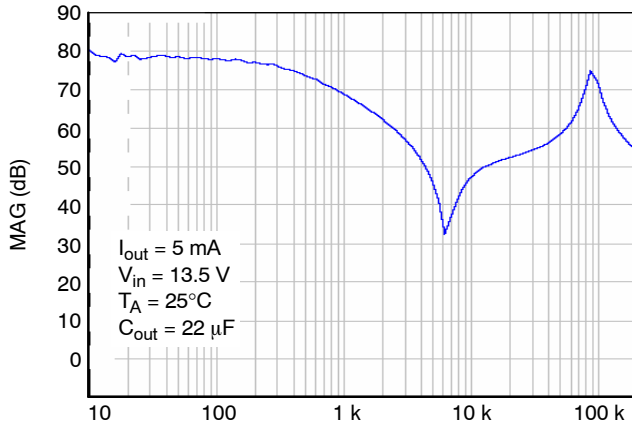


Figure 19. Power Supply Rejection Ratio
(3.3 V Version)

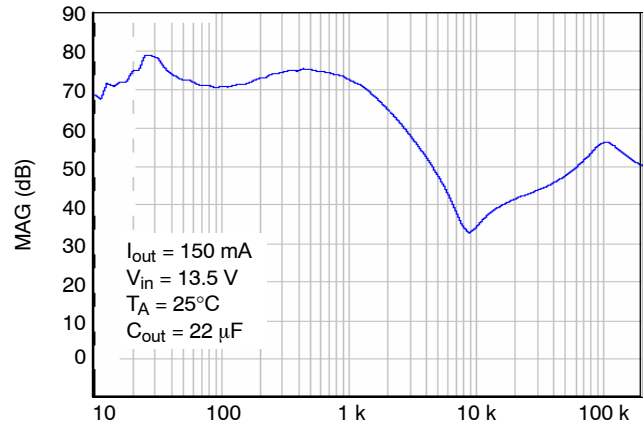


Figure 20. Power Supply Rejection Ratio
(3.3 V Version)

Circuit Description

The NCV4264 is a precision trimmed 5.0 V and 3.3 V fixed output regulator. The device has current capability of 100 mA, with 500 mV of dropout voltage at 100 mA of current. The regulation is provided by a PNP pass transistor controlled by an error amplifier with a bandgap reference. The regulator is protected by both current limit and short circuit protection. Thermal shutdown occurs above 150°C to protect the IC during overloads and extreme ambient temperatures.

Regulator

The error amplifier compares the reference voltage to a sample of the output voltage (V_{out}) and drives the base of a PNP series pass transistor by a buffer. The reference is a bandgap design to give it a temperature-stable output. Saturation control of the PNP is a function of the load current and input voltage. Over saturation of the output power device is prevented, and quiescent current in the ground pin is minimized.

Regulator Stability Considerations

The input capacitor C_{IN1} in Figure 2 is necessary for compensating input line reactance. Possible oscillations caused by input inductance and input capacitance can be damped by using a resistor of approximately 1 Ω in series with C_{IN2} . The output or compensation capacitor, C_{OUT} helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability. The capacitor value and type should be based on cost, availability, size and temperature constraints. Tantalum, aluminum electrolytic, film, or ceramic capacitors are all acceptable solutions, however, attention must be paid to ESR constraints. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (-25°C to -40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet usually provides this information. The value for the output capacitor C_{OUT} shown in Figure 2 should work for most applications; however, it is not necessarily the optimized solution. Stability is guaranteed at values of $C_Q \geq 10 \mu\text{F}$, with an $\text{ESR} \leq 9 \Omega$ for the 5.0 V Version, and $C_Q \geq 22 \mu\text{F}$ with an $\text{ESR} \leq 16 \Omega$ for the 3.3 V Version within the operating temperature range. Actual limits are shown in a graph in the Typical Performance Characteristics section.

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 3) is:

$$P_{D(\text{max})} = \frac{[V_{IN(\text{max})} - V_{OUT(\text{min})}] \cdot I_{Q(\text{max})} + V_{I(\text{max})} \cdot I_q}{1} \quad (\text{eq. 1})$$

Where:

$V_{IN(\text{max})}$ is the maximum input voltage,

$V_{OUT(\text{min})}$ is the minimum output voltage,

$I_{Q(\text{max})}$ is the maximum output current for the application, and I_q is the quiescent current the regulator consumes at $I_{Q(\text{max})}$.

Once the value of $P_{D(\text{Max})}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$P_{\theta JA} = \frac{150^{\circ}\text{C} - T_A}{P_D} \quad (\text{eq. 2})$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$'s less than the calculated value in Equation 2 will keep the die temperature below 150°C. In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heat sink will be required. The current flow and voltages are shown in the Measurement Circuit Diagram.

Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air. Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (\text{eq. 3})$$

Where:

$R_{\theta JC}$ = the junction-to-case thermal resistance,

$R_{\theta CS}$ = the case-to-heat sink thermal resistance, and

$R_{\theta SA}$ = the heat sink-to-ambient thermal resistance.

$R_{\theta JA}$ appears in the package section of the data sheet.

Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heat sink and the interface between them. These values appear in data sheets of heat sink manufacturers. Thermal, mounting, and heat sinking are discussed in the ON Semiconductor application note AN1040/D, available on the ON Semiconductor Website.

NCV4264

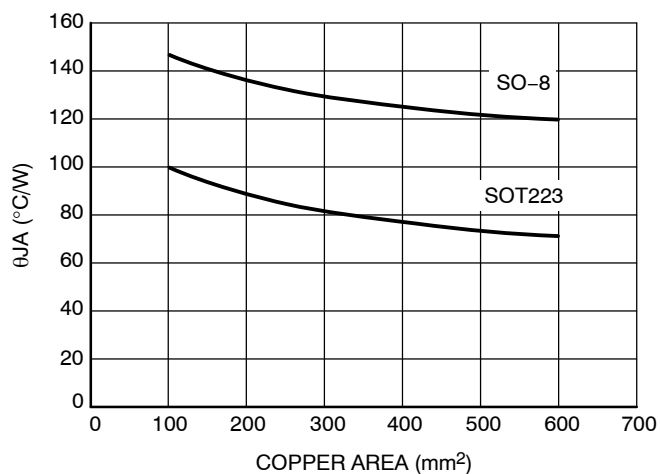


Figure 21.

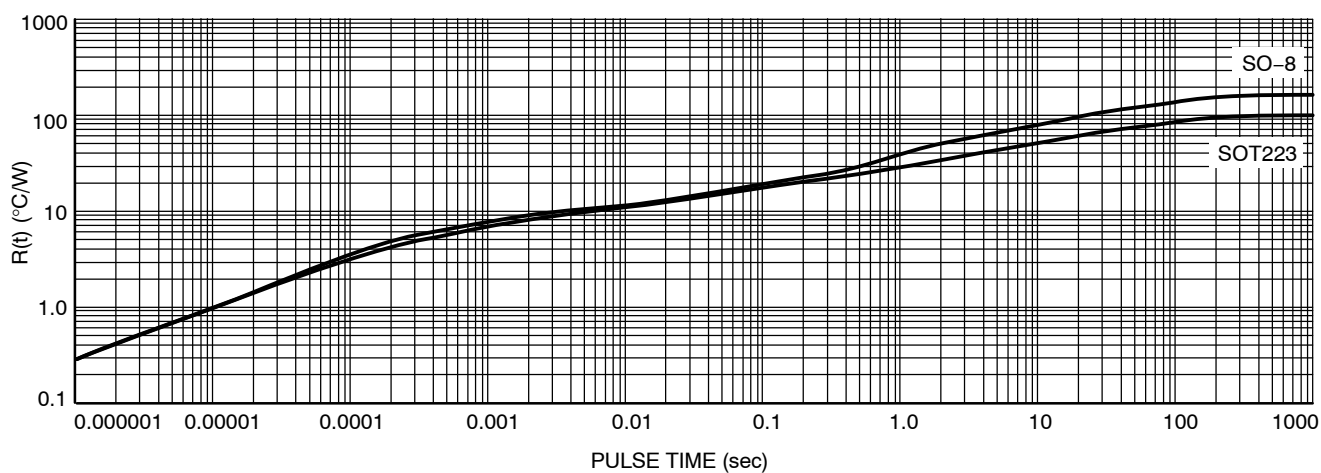


Figure 22.

ORDERING INFORMATION

Device*	Marking	Package	Shipping†
NCV4264ST50T3G	V64_5	SOT-223	4000 / Tape & Reel
NCV4264ST33T3G	V64_3	SOT-223	4000 / Tape & Reel
NCV4264D50R2G	V42645	SO-8	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

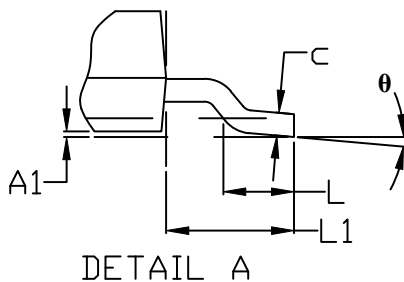
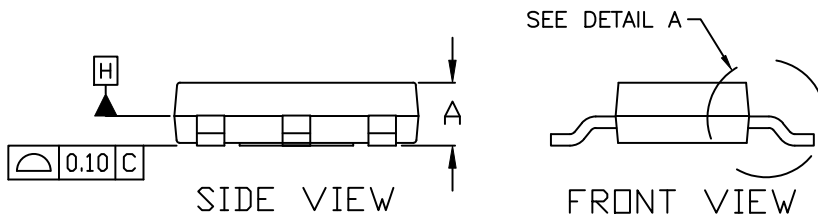
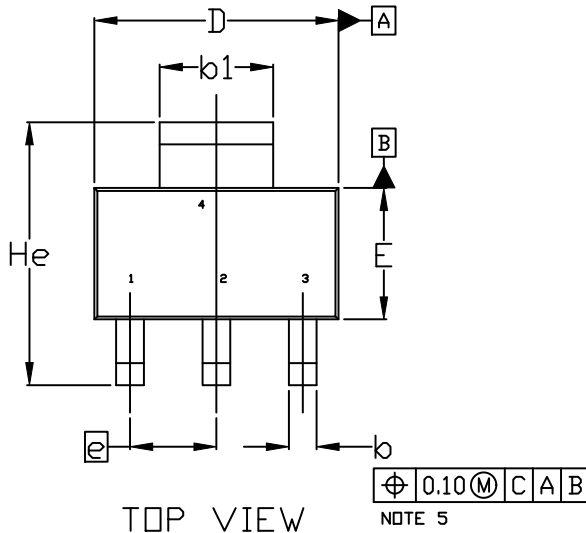
*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.



SCALE 1:1

SOT-223 (TO-261)
CASE 318E-04
ISSUE R

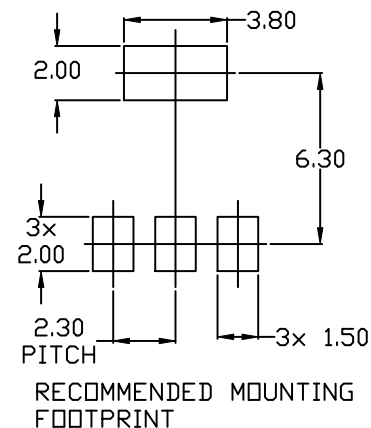
DATE 02 OCT 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

MILLIMETERS			
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



DOCUMENT NUMBER:	98ASB42680B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOT-223 (TO-261)	PAGE 1 OF 2

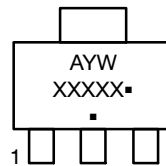
ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

SOT-223 (TO-261)
CASE 318E-04
ISSUE R

DATE 02 OCT 2018

STYLE 1: PIN 1. BASE 2. COLLECTOR 3. EMITTER 4. COLLECTOR	STYLE 2: PIN 1. ANODE 2. CATHODE 3. NC 4. CATHODE	STYLE 3: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN	STYLE 4: PIN 1. SOURCE 2. DRAIN 3. GATE 4. DRAIN	STYLE 5: PIN 1. DRAIN 2. GATE 3. SOURCE 4. GATE
STYLE 6: PIN 1. RETURN 2. INPUT 3. OUTPUT 4. INPUT	STYLE 7: PIN 1. ANODE 1 2. CATHODE 3. ANODE 2 4. CATHODE	STYLE 8: CANCELLED	STYLE 9: PIN 1. INPUT 2. GROUND 3. LOGIC 4. GROUND	STYLE 10: PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE
STYLE 11: PIN 1. MT 1 2. MT 2 3. GATE 4. MT 2	STYLE 12: PIN 1. INPUT 2. OUTPUT 3. NC 4. OUTPUT	STYLE 13: PIN 1. GATE 2. COLLECTOR 3. EMITTER 4. COLLECTOR		

**GENERIC
MARKING DIAGRAM***



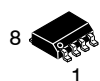
A = Assembly Location
 Y = Year
 W = Work Week
 XXXXX = Specific Device Code
 ■ = Pb-Free Package

(Note: Microdot may be in either location)
 *This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98ASB42680B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOT-223 (TO-261)	PAGE 2 OF 2

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

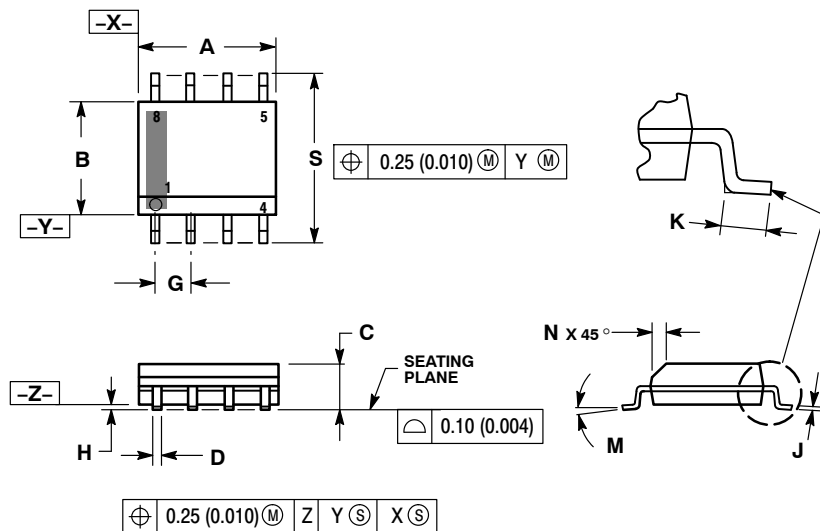
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

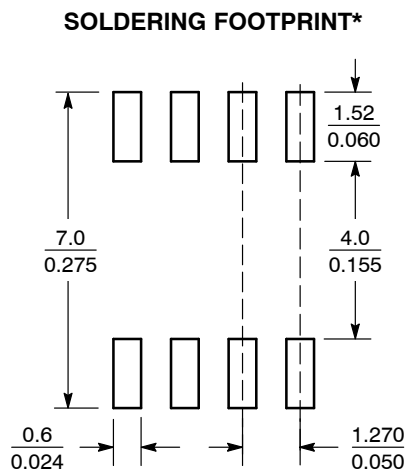


NOTES:

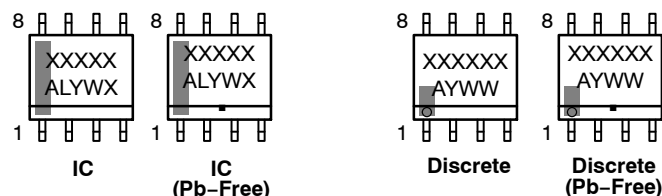
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

GENERIC MARKING DIAGRAM*



SCALE 6:1 (mm/inches)



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-8 NB	PAGE 1 OF 2

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

STYLE 1: PIN 1. EMITTER 2. COLLECTOR 3. COLLECTOR 4. EMITTER 5. EMITTER 6. BASE 7. BASE 8. EMITTER	STYLE 2: PIN 1. COLLECTOR, DIE, #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. BASE, #2 6. EMITTER, #2 7. BASE, #1 8. EMITTER, #1	STYLE 3: PIN 1. DRAIN, DIE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. GATE, #2 6. SOURCE, #2 7. GATE, #1 8. SOURCE, #1	STYLE 4: PIN 1. ANODE 2. ANODE 3. ANODE 4. ANODE 5. ANODE 6. ANODE 7. ANODE 8. COMMON CATHODE
STYLE 5: PIN 1. DRAIN 2. DRAIN 3. DRAIN 4. DRAIN 5. GATE 6. GATE 7. SOURCE 8. SOURCE	STYLE 6: PIN 1. SOURCE 2. DRAIN 3. DRAIN 4. SOURCE 5. SOURCE 6. GATE 7. GATE 8. SOURCE	STYLE 7: PIN 1. INPUT 2. EXTERNAL BYPASS 3. THIRD STAGE SOURCE 4. GROUND 5. DRAIN 6. GATE 3 7. SECOND STAGE Vd 8. FIRST STAGE Vd	STYLE 8: PIN 1. COLLECTOR, DIE #1 2. BASE, #1 3. BASE, #2 4. COLLECTOR, #2 5. COLLECTOR, #2 6. EMITTER, #2 7. EMITTER, #1 8. COLLECTOR, #1
STYLE 9: PIN 1. EMITTER, COMMON 2. COLLECTOR, DIE #1 3. COLLECTOR, DIE #2 4. EMITTER, COMMON 5. EMITTER, COMMON 6. BASE, DIE #2 7. BASE, DIE #1 8. EMITTER, COMMON	STYLE 10: PIN 1. GROUND 2. BIAS 1 3. OUTPUT 4. GROUND 5. GROUND 6. BIAS 2 7. INPUT 8. GROUND	STYLE 11: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1	STYLE 12: PIN 1. SOURCE 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
STYLE 13: PIN 1. N.C. 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN	STYLE 14: PIN 1. N-SOURCE 2. N-GATE 3. P-SOURCE 4. P-GATE 5. P-DRAIN 6. P-DRAIN 7. N-DRAIN 8. N-DRAIN	STYLE 15: PIN 1. ANODE 1 2. ANODE 1 3. ANODE 1 4. ANODE 1 5. CATHODE, COMMON 6. CATHODE, COMMON 7. CATHODE, COMMON 8. CATHODE, COMMON	STYLE 16: PIN 1. EMITTER, DIE #1 2. BASE, DIE #1 3. EMITTER, DIE #2 4. BASE, DIE #2 5. COLLECTOR, DIE #2 6. COLLECTOR, DIE #2 7. COLLECTOR, DIE #1 8. COLLECTOR, DIE #1
STYLE 17: PIN 1. VCC 2. V2OUT 3. V1OUT 4. TXE 5. RXE 6. VEE 7. GND 8. ACC	STYLE 18: PIN 1. ANODE 2. ANODE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. CATHODE 8. CATHODE	STYLE 19: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. MIRROR 2 7. DRAIN 1 8. MIRROR 1	STYLE 20: PIN 1. SOURCE (N) 2. GATE (N) 3. SOURCE (P) 4. GATE (P) 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
STYLE 21: PIN 1. CATHODE 1 2. CATHODE 2 3. CATHODE 3 4. CATHODE 4 5. CATHODE 5 6. COMMON ANODE 7. COMMON ANODE 8. CATHODE 6	STYLE 22: PIN 1. I/O LINE 1 2. COMMON CATHODE/VCC 3. COMMON CATHODE/VCC 4. I/O LINE 3 5. COMMON ANODE/GND 6. I/O LINE 4 7. I/O LINE 5 8. COMMON ANODE/GND	STYLE 23: PIN 1. LINE 1 IN 2. COMMON ANODE/GND 3. COMMON ANODE/GND 4. LINE 2 IN 5. LINE 2 OUT 6. COMMON ANODE/GND 7. COMMON ANODE/GND 8. LINE 1 OUT	STYLE 24: PIN 1. BASE 2. EMITTER 3. COLLECTOR/ANODE 4. COLLECTOR/ANODE 5. CATHODE 6. CATHODE 7. COLLECTOR/ANODE 8. COLLECTOR/ANODE
STYLE 25: PIN 1. VIN 2. N/C 3. REXT 4. GND 5. IOUT 6. IOUT 7. IOUT 8. IOUT	STYLE 26: PIN 1. GND 2. dv/dt 3. ENABLE 4. ILIMIT 5. SOURCE 6. SOURCE 7. SOURCE 8. VCC	STYLE 27: PIN 1. ILIMIT 2. OVLO 3. UVLO 4. INPUT+ 5. SOURCE 6. SOURCE 7. SOURCE 8. DRAIN	STYLE 28: PIN 1. SW_TO_GND 2. DASIC_OFF 3. DASIC_SW_DET 4. GND 5. V_MON 6. VBULK 7. VBULK 8. VIN
STYLE 29: PIN 1. BASE, DIE #1 2. EMITTER, #1 3. BASE, #2 4. EMITTER, #2 5. COLLECTOR, #2 6. COLLECTOR, #2 7. COLLECTOR, #1 8. COLLECTOR, #1	STYLE 30: PIN 1. DRAIN 1 2. DRAIN 1 3. GATE 2 4. SOURCE 2 5. SOURCE 1/DRAIN 2 6. SOURCE 1/DRAIN 2 7. SOURCE 1/DRAIN 2 8. GATE 1		

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-8 NB	PAGE 2 OF 2

onsemi and **onsemi** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT

North American Technical Support:

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative