NCP720

350mA, Very Low Dropout Bias Rail CMOS Voltage Regulator

The NCP720 is a 350 mA VLDO equipped with NMOS pass transistor and a separate bias supply voltage (V_{BIAS}). The device provides very stable, accurate output voltage with low noise suitable for space constrained, noise sensitive applications. In order to optimize performance for battery operated portable applications, the NCP720 features low I_Q consumption. The WDFN6 2 mm x 2 mm package is optimized for use in space constrained applications.

Features

- Input Voltage Range: 0.8 V to 5.5 V
- Bias Voltage Range: 2.4 V to 5.5 V
- Fixed Output Voltage Device
- Output Voltage Range: 0.8 V to 2.1 V
- ±2% Accuracy over Temperature
- Ultra−Low Dropout: 110 mV typically at 350 mA
- Very Low Bias Input Current of Typ. 80 μA
- Very Low Bias Input Current in Disable Mode: Typ. 0.5 μA
- Low Noise, High PSRR
- Built−In Soft−Start with Monotonic V_{OUT} Rise
- Stable with a 2.2 μF Ceramic Capacitor
- Available in WDFN6 − 2 mm x 2 mm Package
- These are Pb−Free Devices

Typical Applications

- Battery−powered Equipment
- Smartphones, Tablets
- Cameras, DVRs, STB and Camcorders

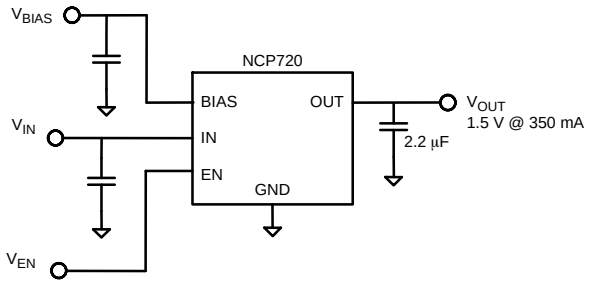

Figure 1. Typical Application Schematics

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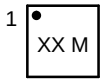
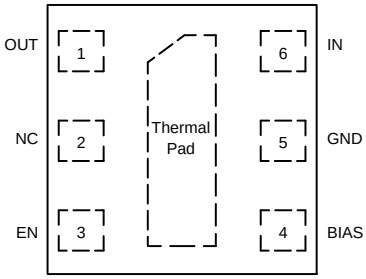
MARKING DIAGRAM

WDFN6
CASE 511BR



XX = Specific Device Code
M = Date Code

PIN CONNECTIONS



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ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 8 of this data sheet.

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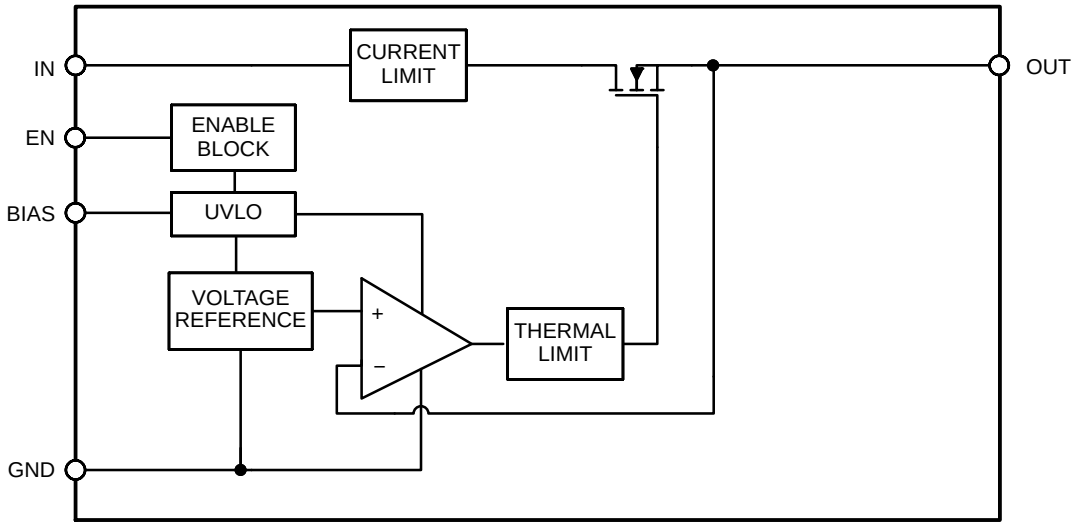


Figure 2. Simplified Schematic Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	OUT	Regulated Output Voltage pin
2	N/C	Not internally connected
3	EN	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode.
4	BIAS	Bias voltage supply for internal control circuits. This pin is monitored by internal Under-Voltage Lockout Circuit.
5	GND	Ground pin
6	IN	Input Voltage Supply pin
Pad		Should be soldered to the ground plane for increased thermal performance.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	−0.3 to 6	V
Output Voltage	V_{OUT}	−0.3 to (V_{IN}+0.3) ≤ 6	V
Chip Enable and Bias Input	V_{EN}, V_{BIAS}	−0.3 to 6	V
Output Short Circuit Duration	t_{SC}	unlimited	s
Maximum Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection (except OUT pin) and is tested by the following methods:
   ESD Human Body Model tested per EIA/JESD22−A114
   ESD Machine Model tested per EIA/JESD22−A115
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, WDFN6 2 mm x 2 mm Thermal Resistance, Junction−to−Air (Note 3)	$R_{\theta JA}$	65	°C/W

3. This data was derived by thermal simulations based on the JEDEC JESD51 series standards methodology. Only a single device mounted at the center of a high − K (2s2p) 3in x 3in multilayer board with 1−ounce internal planes and 2−ounce copper on top and bottom. Top copper layer has a dedicated 125 sqmm copper area.

ELECTRICAL CHARACTERISTICS

Over Operating Temperature Range (T_J = −40°C to +125°C), V_{BIAS} = (V_{OUT} + 1.4 V) or 2.5 V, whichever is greater; $V_{IN} \geq V_{OUT}$ + 0.5 V, I_{OUT} = 1 mA, V_{EN} = 1.1 V, C_{OUT} = 2.2 μF, unless otherwise noted. Typical values are at T_J = +25°C.

Parameter		Test Conditions		Symbol	Min	Typ	Max	Unit
Operating Input Voltage Range				V_{IN}	V_{OUT} + V_{DO_IN}		5.5	V
Operating Bias Voltage Range				V_{BIAS}	(V_{OUT} + 1.4) ≥ 2.4		5.5	V
Output Voltage Range (Note 4)					0.8		2.1	V
Output Voltage Accuracy	Nominal	T_J = +25°C		V_{OUT}		±0.5		%
	Over V_{BIAS}, V_{IN}, I_{OUT}, T_J = –40°C to +125°C	V_{OUT} + 1.4 V ≤ V_{BIAS} ≤ 5.5 V, V_{OUT} + 0.5 V ≤ V_{IN} ≤ 4.5 V, 0mA ≤ I_{OUT} ≤ 350 mA		V_{OUT}	-2		+2	%
V_{IN} Line Regulation		V_{IN} = (V_{OUT} + 0.5 V) to 4.5 V, I_{OUT} = 1mA		$\Delta V_{OUT}/\Delta V_{IN}$		5.0		μV/V
V_{BIAS} Line Regulation		V_{BIAS} = (V_{OUT} + 1.4 V) or 2.5 V (whichever is greater) to 5.5 V, I_{OUT} = 1 mA		$\Delta V_{OUT}/\Delta V_{BIAS}$		16		μV/V
Load Regulation		0 mA ≤ I_{OUT} ≤ 350 mA (no load to full load)		$\Delta V_{OUT}/\Delta I_{OUT}$		–1.0		μV/mA
V_{IN} Dropout Voltage (Note 5)		V_{IN} = $V_{OUT(NOM)}$ – 0.1 V, (V_{BIAS} – $V_{OUT(NOM)}$) = 1.4 V, I_{OUT} = 350 mA		V_{DO_IN}		110	200	mV
V_{BIAS} Dropout Voltage (Note 6)		V_{IN} = $V_{OUT(NOM)}$ + 0.3 V, I_{OUT} = 350 mA		V_{DO_BIAS}		1.15	1.4	V
Output Current Limit		V_{OUT} = 0.9 x $V_{OUT(NOM)}$		I_{CL}	420	525	800	mA
Bias Pin Current		I_{OUT} = 0 mA to 350 mA		I_{BIAS}		80	110	μA
Shutdown Current (I_{GND})		V_{EN} ≤ 0.4 V, T_J = -40°C to +85°C		I_{SHDN}		0.5	2.0	μA
V_{IN} Power-Supply Rejection Ratio		V_{IN} – V_{OUT} ≥ 0.5 V, V_{BIAS} = V_{OUT} + 1.4 V, I_{OUT} = 350 mA	f = 10 Hz	PSRR (V_{IN})		52		dB
			f = 100 Hz			56		
			f = 1 kHz			65		
			f = 10 kHz			46		
			f = 100 kHz			37		
			f = 1 MHz			25		
V_{BIAS} Power-Supply Rejection Ratio		V_{IN} – V_{OUT} ≥ 0.5 V, V_{BIAS} = V_{OUT} + 1.4 V, I_{OUT} = 350 mA	f = 10 Hz	PSRR (V_{BIAS})		65		dB
			f = 100 Hz			65		
			f = 1 kHz			70		
			f = 10 kHz			50		
			f = 100 kHz			35		
			f = 1 MHz			24		
Output Noise Voltage		BW = 10 Hz to 100 kHz		V_N		40		μV_{RMS}
Inrush Current on V_{IN}				I_{VIN_INRUSH}		100 + I_{LOAD}		mA
Startup Time		V_{OUT} = 95% $V_{OUT(NOM)}$, I_{OUT} = 350 mA, C_{OUT} = 2.2 μF		t_{STR}		140		μs
Enable Pin High (enabled)				$V_{EN(HI)}$	1.1			V
Enable Pin Low (disabled)				$V_{EN(LO)}$	0		0.4	V
Enable Pin Current		V_{EN} = 5.5 V		I_{EN}		0.3	1	μA
Undervoltage Lock-out		V_{BIAS} rising		UVLO		1.6		V
Hysteresis		V_{BIAS} falling				0.2		V
Thermal Shutdown Temperature		Shutdown, temperature increasing		T_{SD}		+160		°C
		Reset, temperature decreasing				+140		°C
Operating Junction Temperature				T_J	–40		+125	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. V_{OUT} nominal value is factory programmable.
5. Measured for devices with $V_{OUT(NOM)} \geq 1.2V$.
6. V_{BIAS} – V_{OUT} with V_{OUT} = $V_{OUT(NOM)}$ – 0.1V.

APPLICATIONS INFORMATION

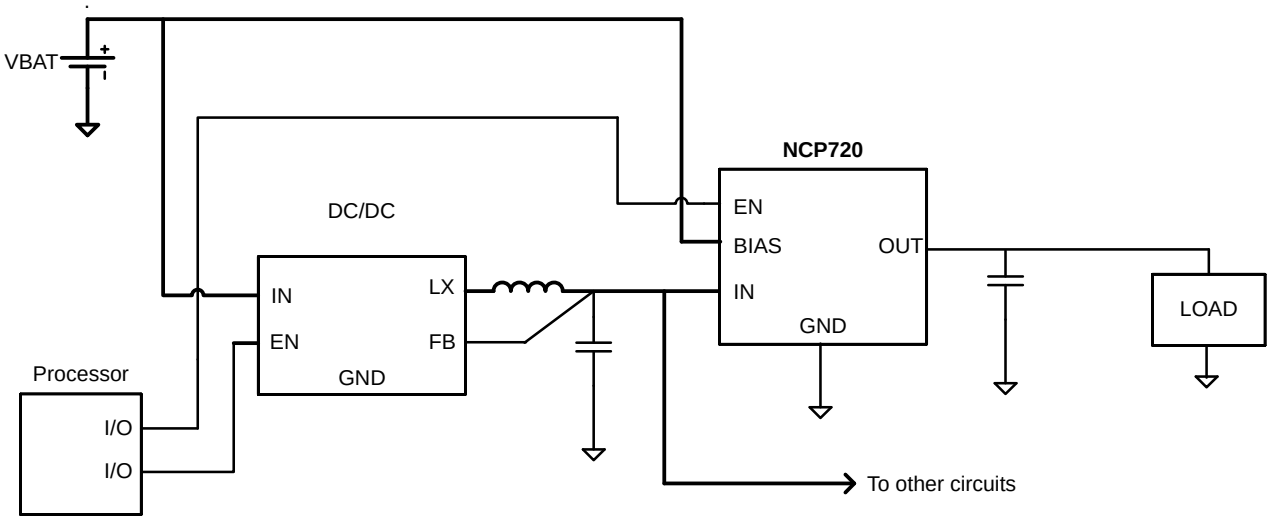


Figure 3. Typical Application: Low−Voltage Post−Regulator with ON/OFF functionality

TYPICAL CHARACTERISTICS

$V_{OUT(NOMINAL)}$ = 1.5 V, V_{BIAS} = (V_{OUT} + 1.4 V) or 2.5 V, whichever is greater, V_{IN} = V_{OUT} + 0.5 V, I_{OUT} = 1 mA, V_{EN} = 1.1 V, C_{OUT} = 2.2 μF, T_J = 25°C unless otherwise noted.

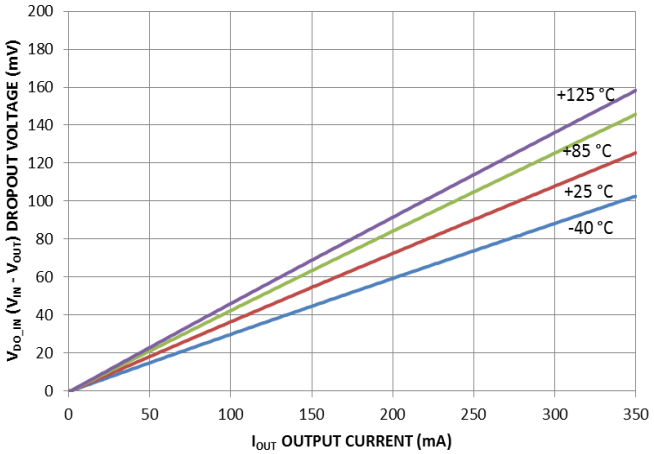


Figure 4. V_{IN} Dropout Voltage vs. Output Current

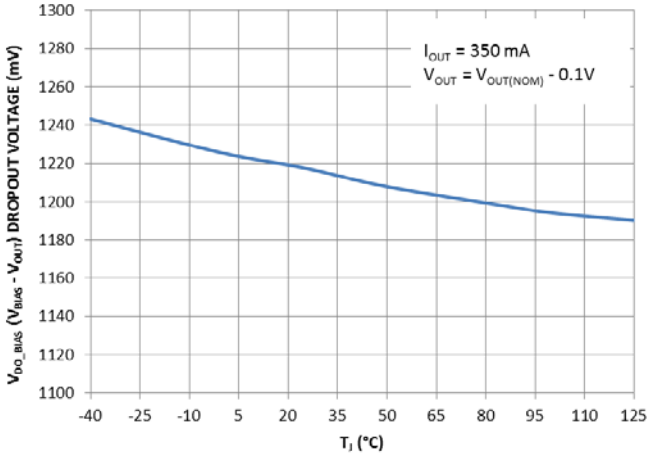


Figure 5. V_{BIAS} Dropout Voltage vs. Temperature

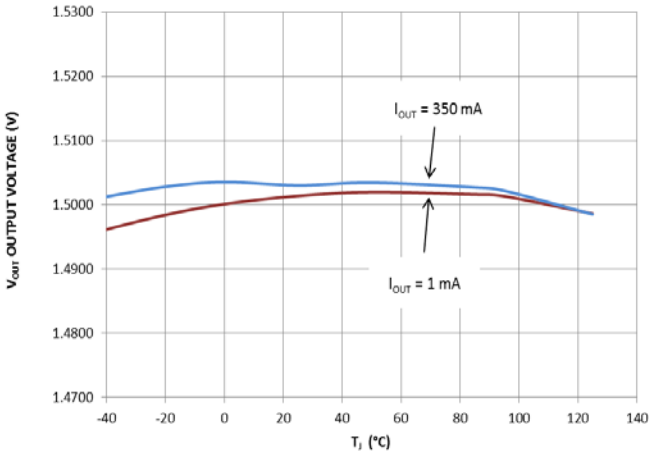


Figure 6. Output Voltage vs. Temperature

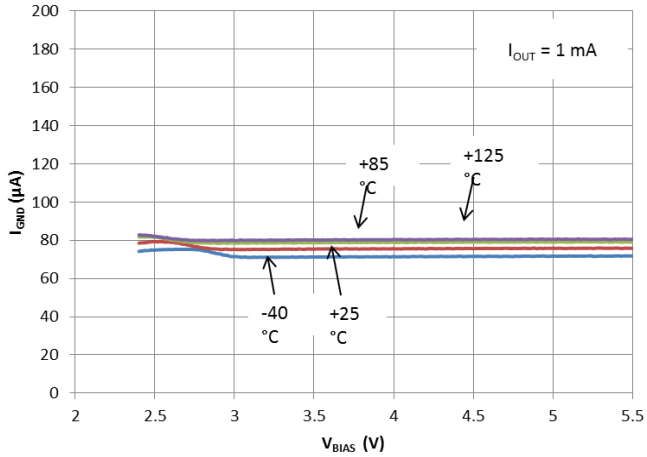


Figure 7. Bias Pin Current vs. V_{BIAS} Input Voltage

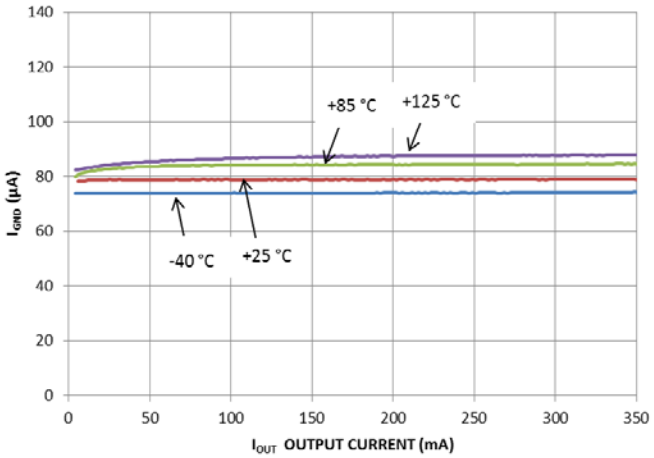


Figure 8. Bias Pin Current vs. Output Current

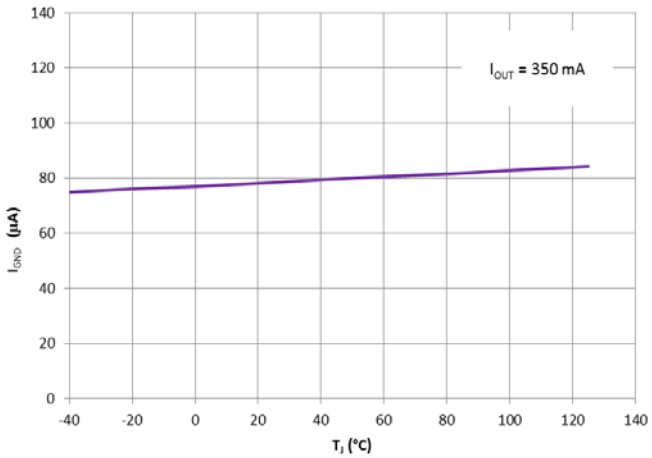


Figure 9. Bias Pin Current vs. Temperature

TYPICAL CHARACTERISTICS

$V_{OUT(NOMINAL)}$ = 1.5 V, V_{BIAS} = (V_{OUT} + 1.4 V) or 2.5 V, whichever is greater, V_{IN} = V_{OUT} + 0.5 V, I_{OUT} = 1 mA, V_{EN} = 1.1 V, C_{OUT} = 2.2 μF, T_J = 25°C unless otherwise noted.

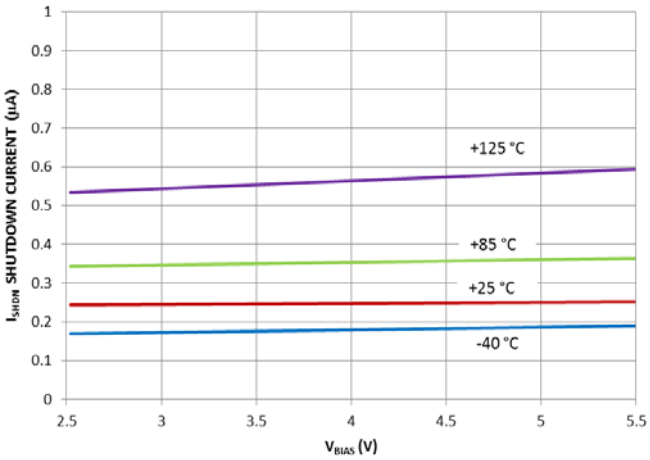


Figure 10. Shutdown Current vs. V_{BIAS} Input Voltage

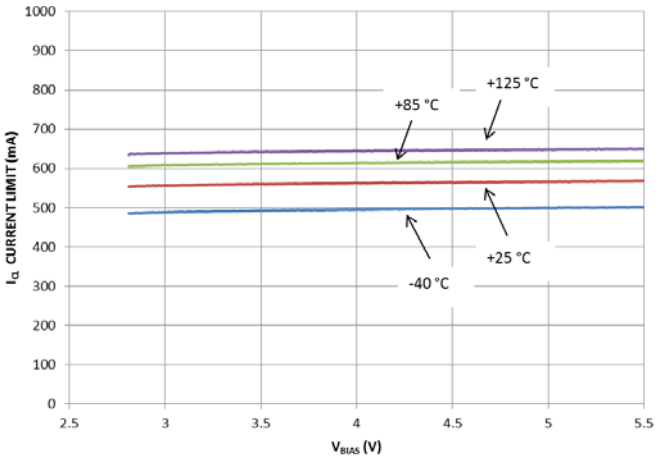


Figure 11. Current Limit vs. V_{BIAS} Input Voltage

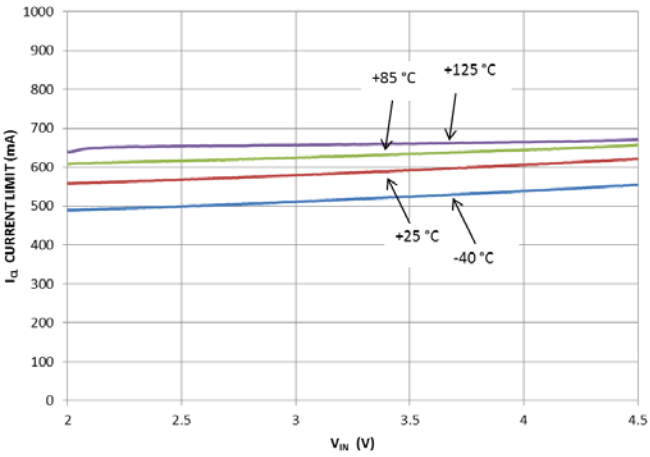


Figure 12. Current Limit vs. V_{IN} Input Voltage

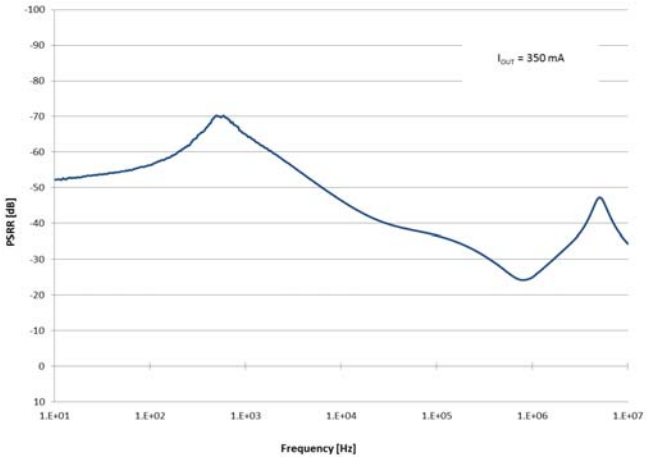


Figure 13. V_{IN} Power Supply Ripple Rejection vs. Frequency

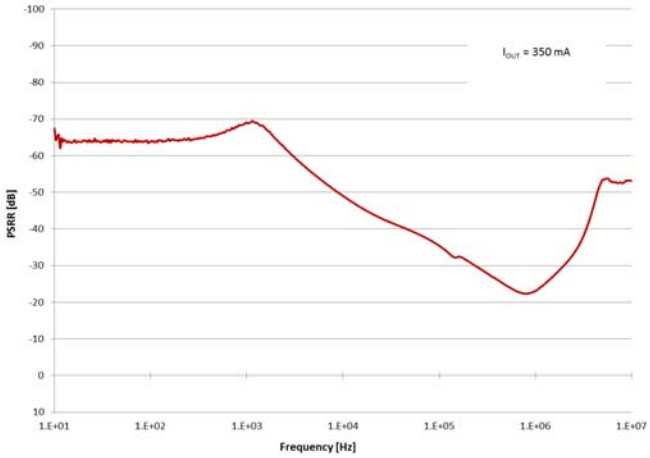


Figure 14. V_{BIAS} Power Supply Ripple Rejection vs. Frequency

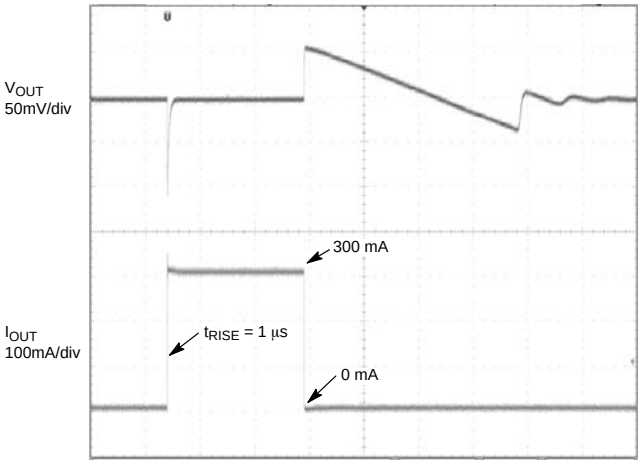


Figure 15. Load Transient Response

APPLICATIONS INFORMATION

The NCP720 dual−rail very low dropout voltage regulator is using NMOS pass transistor for output voltage regulation from V_{IN} voltage. All the low current internal controll circuitry is powered from the V_{BIAS} voltage.

The use of an NMOS pass transistor offers several advantages in applications. Unlike a PMOS topology devices, the output capacitor has reduced impact on loop stability. V_{IN} to V_{OUT} operating voltage difference can be very low compared with standard PMOS regulators in very low V_{IN} applications.

The NCP720 offers built−in Soft−Start with monotonic V_{OUT} rise. The controlled voltage rising limits the inrush current.

The Enable (EN) input is equipped with internal hysteresis.

NCP720 is a Fixed Voltage linear regulator.

Dropout Voltage

Because of two power supply inputs V_{IN} and V_{BIAS} and one V_{OUT} regulator output, there are two Dropout voltages specified.

The first, the V_{IN} Dropout voltage is the voltage difference ($V_{IN} – V_{OUT}$) at which the regulator output no longer maintains regulation against further reductions in input voltage. V_{BIAS} is high enough, specific value is published in the Electrical Characteristics table.

The second, V_{BIAS} dropout voltage is the voltage difference ($V_{BIAS} – V_{OUT}$) at which the regulator output no longer maintains regulation against further reductions in V_{BIAS} voltage. V_{IN} is high enough.

Input and Output Capacitors

The device is designed to be stable for ceramic output capacitors with Effective capacitance in the range from 2.2 μF to 10 μF. The device is also stable with multiple capacitors in parallel, having the total effective capacitance in the specified range.

In applications where no low input supplies impedance available (PCB inductance in V_{IN} and/or V_{BIAS} inputs as example), the recommended C_{IN} = 1 μF and C_{BIAS} = 0.1 μF or greater. Ceramic capacitors are recommended**.** For the best performance all the capacitors should be connected to the NCP720 respective pins directly in the device PCB copper layer, not through vias having not negligible impedance.

When using small ceramic capacitor, their capacitance is not constant but varies with applied DC biasing voltage, temperature and tolerance. The effective capacitance can be much lower than their nominal capacitance value, most importantly in negative temperatures and higher LDO output voltages. That is why the recommended Output capacitor capacitance value is specified as Effective value in the specific application conditions.

Enable Operation

The enable pin will turn the regulator on or off. The threshold limits are covered in the electrical characteristics table in this data sheet. If the enable function is not to be used then the pin should be connected to V_{IN} or V_{BIAS}. When enabled, the device consumes roughly 20 μA from Vin supply per 1 V nominal output voltage. That is why using the enable / disable function in power saving applications is recommended.

Current Limitation

The internal Current Limitation circuitry allows the device to supply the full nominal current and surges but protects the device against Current Overload or Short.

Thermal Protection

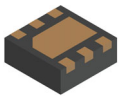
Internal thermal shutdown (TSD) circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When TSD activated , the regulator output turns off. When cooling down under the low temperature threshold, device output is activated again. This TSD feature is provided to prevent failures from accidental overheating.

ORDERING INFORMATION

Device	Nominal Output Voltage	Marking	Package	Shipping†
NCP720BMT100TBG	1.00 V	JC	WDFN6 (Pb−Free)	3000 / Tape & Reel
NCP720BMT105TBG	1.05 V	JD		
NCP720BMT110TBG	1.10 V	JE		
NCP720BMT115TBG	1.15 V	JF		
NCP720BMT120TBG	1.20 V	JG		
NCP720BMT125TBG	1.25 V	JH		
NCP720BMT130TBG	1.30 V	JJ		
NCP720BMT135TBG	1.35 V	JK		
NCP720BMT140TBG	1.40 V	JL		
NCP720BMT145TBG	1.45 V	JM		
NCP720BMT150TBG	1.50 V	JA		
NCP720BMT160TBG	1.60 V	JP		
NCP720BMT170TBG	1.70 V	JQ		
NCP720BMT180TBG	1.80 V	JR		

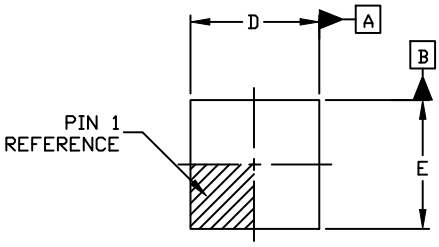
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

To order other package and voltage variants, please contact your ON sales representative

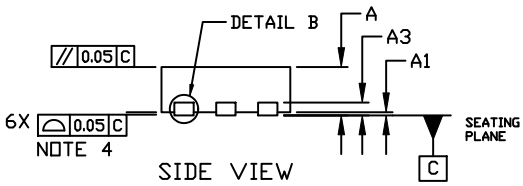


WDFN6 2x2, 0.65P
CASE 511BR
ISSUE C

DATE 01 DEC 2021



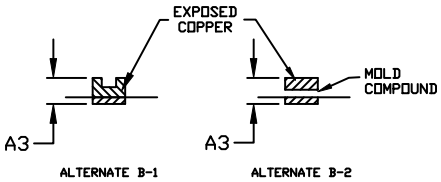
TOP VIEW



SIDE VIEW

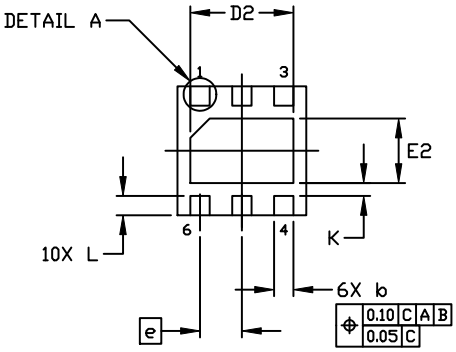
NOTES:

1. DIMENSION AND TOLERANCING PER ASME Y14.5, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

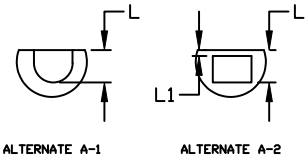


DETAIL B
ALTERNATE CONSTRUCTION

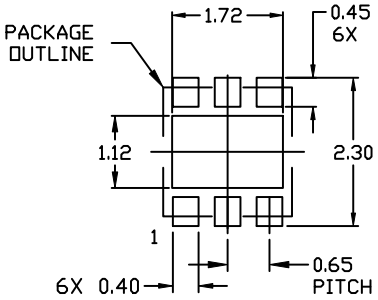
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	---	0.05
A3	0.20 REF		
b	0.25	0.30	0.35
D	1.90	2.00	2.10
D2	1.50	1.60	1.70
E	1.90	2.00	2.10
E2	0.90	1.00	1.10
e	0.65 BSC		
K	0.20 REF		
L	0.20	0.30	0.40
L1	---	---	0.15



BOTTOM VIEW



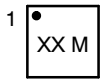
DETAIL A
ALTERNATE CONSTRUCTIONS



RECOMMENDED
MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**WDFN6 2X2, 0.65P**	**PAGE 1 OF 1**

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