



# NCP45750

**Table 1. PIN DESCRIPTION**

Pin	Name	Function
2, 3, 4	V <sub>OUT</sub>	Source of MOSFET connected to load. Includes an internal bleed resistor to GND. – <b>All pins must be connected to provide correct R<sub>ds</sub>, OCP, and current capability.</b>
6	V <sub>SS</sub>	Driver ground
7	SR	Slew Rate control pin. Slew rate adjustment made with an external capacitor to GND; float if not used.
8	PG	Active–high, open–drain output that indicates when the gate of the MOSFET is fully charged, external pull up resistor ≥ 100 kΩ to an external voltage source required; tie to GND if not used.
9	OCP	Over–current protection trip point adjustment made with a resistor to ground; short to ground if over–current protection is not needed.
10	V <sub>CC</sub>	Driver supply voltage (3.0 V – 5.5 V)
11	EN	Active–high digital input used to turn on the MOSFET driver, pin has an internal pull down resistor to GND
12, 13	V <sub>IN</sub>	Input voltage (3 V – 24 V) – <b>Pin 13 should be used for high current (&gt;0.5 A)</b>

**Table 2. ABSOLUTE MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Supply Voltage Range	V <sub>CC</sub>	–0.3 to 6	V
Input Voltage Range	V <sub>IN</sub>	–0.3 to 30	V
Output Voltage Range	V <sub>OUT</sub>	–0.3 to 30	V
EN Input Voltage Range	V <sub>EN</sub>	–0.3 to 6	V
PG Output Voltage Range (Note 1)	V <sub>PG</sub>	–0.3 to 6	V
OCP Input Voltage Range	V <sub>OCP</sub>	–0.3 to 6	V
Thermal Resistance, Junction–to–Ambient, Steady State (Note 2)	R <sub>θJA</sub>	49.7	°C/W
Thermal Resistance, Junction–to–Case (V <sub>IN</sub> Paddle)	R <sub>θJC</sub>	1.7	°C/W
Continuous MOSFET Current @ T <sub>A</sub> = 25°C (Note 2)	I <sub>MAX</sub>	10	A
Load Power Range (Note 5)	P <sub>LOAD</sub>	100	W
Storage Temperature Range	T <sub>STG</sub>	–55 to 150	°C
Lead Temperature, Soldering (10 sec.)	T <sub>SLD</sub>	260	°C
ESD Capability, Human Body Model (Notes 3 and 4)	ESD <sub>HBM</sub>	2	kV
ESD Capability, Charged Device Model (Notes 3 and 4)	ESD <sub>CDM</sub>	0.5	kV
Latch–up Current Immunity (Note 3)	LU	100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- PG is an open drain output that requires an external pull–up resistor > 100 kΩ to an external voltage source.
- Surface–mounted on FR4 board using the minimum recommended pad size, 1 oz Cu. Over current protection will limit maximum realized current to 10 A at highest setting.
- Tested by the following methods @ T<sub>A</sub> = 25°C:  
 ESD Human Body Model tested per JS–001  
 ESD Charged Device Model per ESD JS–002  
 Latch–up Current tested per JESD78  
 PG, OCP, and SR pins must be correctly connected for compliance
- Rating is for all pins except for V<sub>IN</sub> and V<sub>OUT</sub> which are tied to the internal MOSFET’s Drain and Source. Typical MOSFET ESD performance for V<sub>IN</sub> and V<sub>OUT</sub> should be expected and these devices should be treated as ESD sensitive.

# NCP45750

**Table 3. OPERATING RANGES**

Rating	Symbol	Min	Max	Unit
VCC – ( $V_{IN} > 4.5$ V)	$V_{CC}$	3	5.5	V
VCC – ( $V_{IN} < 4.5$ V)	$V_{CC}$	4.5	5.5	V
VIN – ( $V_{CC} > 4.5$ V)	$V_{IN}$	3	24	V
VIN – ( $V_{CC} < 4.5$ V)	$V_{IN}$	4.5	24	V
OCP External Resistor to VSS	$R_{OCP}$	short	open	$\Omega$
OFF to ON Transition Energy Dissipation Limit (See application section)	$E_{TRANS}$		100	mJ
VSS	$V_{SS}$		0	V
Ambient Temperature	$T_A$	-40	85	$^{\circ}$ C
Junction Temperature	$T_J$	-40	125	$^{\circ}$ C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

**Table 4. ELECTRICAL CHARACTERISTICS** ( $T_J = 25^{\circ}$ C,  $V_{CC} = 3$  V – 5.5 V, unless otherwise specified)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
On-Resistance	$V_{CC} = 4.5$ V; $V_{IN} = 3$ V	$R_{ON}$		5.9	7.0	m $\Omega$
	$V_{CC} = 3.3$ V; $V_{IN} = 4.5$ V			5.9	7.0	
	$V_{CC} = 3.3$ V; $V_{IN} = 15$ V			5.9	7.0	
	$V_{CC} = 3.3$ V; $V_{IN} = 24$ V			5.9	7.0	
Leakage Current – $V_{IN}$ to $V_{OUT}$	$V_{EN} = 0$ V; $V_{IN} = 24$ V	$I_{LEAK}$			0.1	$\mu$ A
$V_{IN}$ Control Current – $V_{IN}$ to $V_{SS}$	$V_{EN} = 0$ V; $V_{IN} = 24$ V; $V_{CC} = 3.3$ V	$I_{INCTL}$			1.5	$\mu$ A
$V_{IN}$ Control Current – $V_{IN}$ to $V_{SS}$	$V_{EN} = V_{CC} = 3.3$ V; $V_{IN} = 24$ V	$I_{INCTL\_EN}$			300	$\mu$ A
Supply Standby Current (Note 5)	$V_{EN} = 0$ V; $V_{IN} = 24$ V; $V_{CC} = 3.3$ V	$I_{STBY}$		2.0	5.0	$\mu$ A
Supply Dynamic Current (Note 6)	$V_{EN} = V_{CC} = 3.3$ V; $V_{IN} = 24$ V	$I_{DYN}$			0.5	mA
Bleed Resistance		$R_{BLEED}$	75	104	200	k $\Omega$
EN Input High Voltage		$V_{IH}$	2			V
EN Input Low Voltage		$V_{IL}$			0.8	V
EN Input Leakage Current	$V_{EN} = 0$ V	$I_{IL}$	-1.0		1.0	$\mu$ A
EN Pull Down Resistance		$R_{PD}$	76	100	124	k $\Omega$
PG Output Low Voltage	$I_{SINK} = 100$ $\mu$ A	$V_{OL}$			0.1	V
PG Output Leakage Current	$V_{TERM} = 3.3$ V	$I_{OH}$		3.5	100	nA
Slew Rate Control Constant (Note 7)	SR pin floating (default)	$K_{SR}$	70	99	130	$\mu$ A

## FAULT PROTECTIONS

Thermal Shutdown Threshold (Note 8)		$T_{SDT}$		145		$^{\circ}$ C
Thermal Shutdown Hysteresis (Note 8)		$T_{HYS}$		20		$^{\circ}$ C
$V_{IN}$ Under Voltage Lockout Threshold	$V_{IN}$ rising	$V_{UVLO}$		2.0	2.1	V
$V_{IN}$ Under Voltage Lockout Hysteresis		$V_{HYS}$		220	300	mV
Over-Current Protection Trip (Note 9)	$R_{OCP} = \text{open}$	$I_{TRIP}$	0.85	1.2	1.45	A
	$R_{OCP} = 32$ k $\Omega$			7.5		
	$R_{OCP} = \text{short to GND}$ (Note 10)			12		
Over-Current Protection Blanking Time		$t_{OCP}$		2.25		ms
Short-Circuit Protection Trip Current	Soft Short & Hard Short (Note 11)	$I_{SC}$		12		A

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Average current from  $V_{CC}$  to GND with MOSFET turned off.

6. Average current from  $V_{CC}$  to GND after charge up time of MOSFET.

7. See Applications Information section for details on how to adjust the gate slew rate.

8. Operation above  $T_J = 125^{\circ}$ C is not guaranteed.

9. OCP Trip current limits were verified by bench test and are not guaranteed on every part.

10. Transient currents exceeding the short-circuit protection trip current will cause the device to fault. For OCP settings less than 20 k $\Omega$ , high steady state currents may cause an over temperature lockout before the OCP threshold is reached due to self-heating.

11. Short Circuit Protection protects the device against hard shorts ( $R_{SHORT} \leq 250$  m $\Omega$   $V_{out}$  to Ground) for  $V_{in} < 18$  V, and against soft shorts ( $R_{SHORT} > 250$  m $\Omega$ ) for  $V_{in} < 24$  V. Short circuit protection testing assumed a 100 W supply capability limit on  $V_{in}$ .

# NCP45750

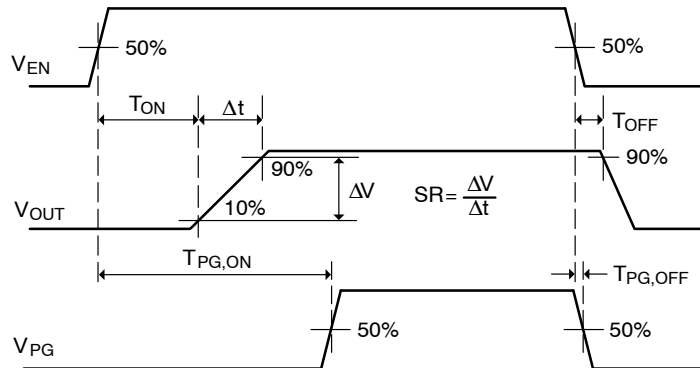
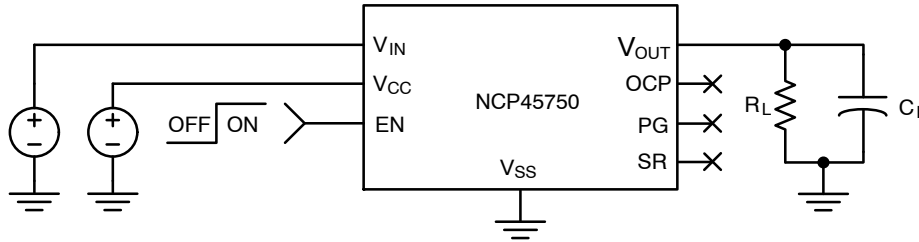
**Table 5. SWITCHING CHARACTERISTICS** ( $T_J = 25^\circ\text{C}$  unless otherwise specified) (Notes 12 and 13)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Output Slew Rate – Default	$V_{CC} = 4.5\text{ V}; V_{IN} = 3\text{ V}$	SR	13	20.3	28	kV/s
	$V_{CC} = 5.0\text{ V}; V_{IN} = 3\text{ V}$		13	20.6	28	
	$V_{CC} = 3.3\text{ V}; V_{IN} = 24\text{ V}$		13	23	28	
	$V_{CC} = 5.0\text{ V}; V_{IN} = 24\text{ V}$		13	23	28	
Output Turn-on Delay	$V_{CC} = 4.5\text{ V}; V_{IN} = 3\text{ V}$	$T_{ON}$	100	162	700	$\mu\text{s}$
	$V_{CC} = 5.0\text{ V}; V_{IN} = 3\text{ V}$		100	161	700	
	$V_{CC} = 3.3\text{ V}; V_{IN} = 24\text{ V}$		100	453	700	
	$V_{CC} = 5.0\text{ V}; V_{IN} = 24\text{ V}$		100	448	700	
Output Turn-off Delay	$V_{CC} = 4.5\text{ V}; V_{IN} = 3\text{ V}$	$T_{OFF}$		60		$\mu\text{s}$
	$V_{CC} = 5.0\text{ V}; V_{IN} = 3\text{ V}$			60		
	$V_{CC} = 3.3\text{ V}; V_{IN} = 24\text{ V}$			40		
	$V_{CC} = 5.0\text{ V}; V_{IN} = 24\text{ V}$			40		
Power Good Turn-on Time	$V_{CC} = 4.5\text{ V}; V_{IN} = 3\text{ V}$	$T_{PG,ON}$	0.25	0.5	2.5	ms
	$V_{CC} = 5.0\text{ V}; V_{IN} = 3\text{ V}$		0.25	0.5	2.5	
	$V_{CC} = 3.3\text{ V}; V_{IN} = 24\text{ V}$		0.25	1.7	2.5	
	$V_{CC} = 5.0\text{ V}; V_{IN} = 24\text{ V}$		0.25	1.5	2.5	
Power Good Turn-off Time (Note 14)	$V_{CC} = 4.5\text{ V}; V_{IN} = 3\text{ V}$	$T_{PG,OFF}$			10	ns
	$V_{CC} = 5.0\text{ V}; V_{IN} = 3\text{ V}$				10	
	$V_{CC} = 3.3\text{ V}; V_{IN} = 24\text{ V}$				10	
	$V_{CC} = 5.0\text{ V}; V_{IN} = 24\text{ V}$				10	

12. See below figure for Test Circuit and Timing Diagram.

13. Tested with the following conditions:  $V_{TERM} = V_{CC}$ ;  $R_{PG} = 100\text{ k}\Omega$ ;  $R_L = 10\ \Omega$ ;  $C_L = 0.1\ \mu\text{F}$ .

14. Power Good Turn-off Time is highly dependent on external pull up resistor value and external capacitive loading. 100 k $\Omega$  pull up to 3.3 V was used in test.



**Figure 2. Switching Characteristics Test Circuit and Timing Diagrams**

TYPICAL CHARACTERISTICS

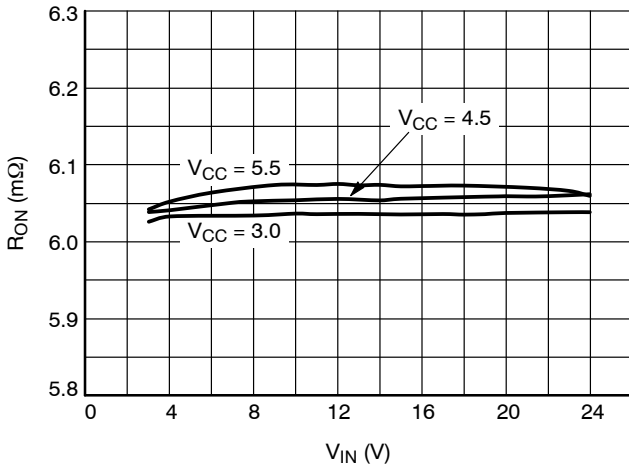


Figure 3. On-Resistance vs. Input Voltage

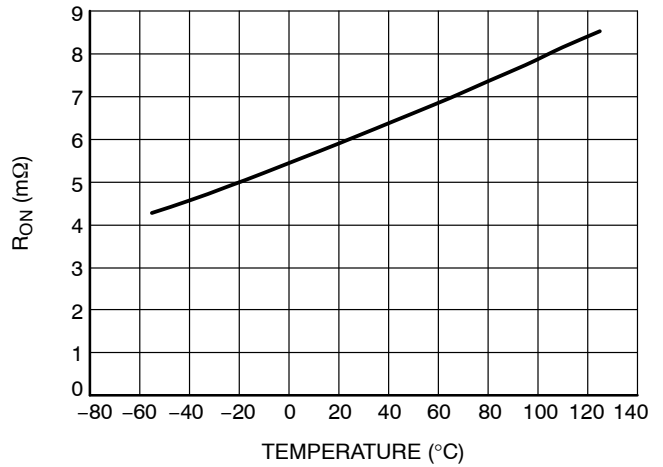


Figure 4. On-Resistance vs. Temperature

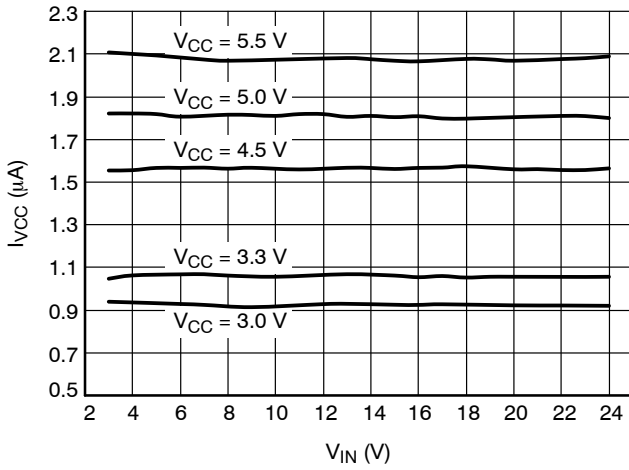


Figure 5. Supply Standby Current vs. Supply Voltage

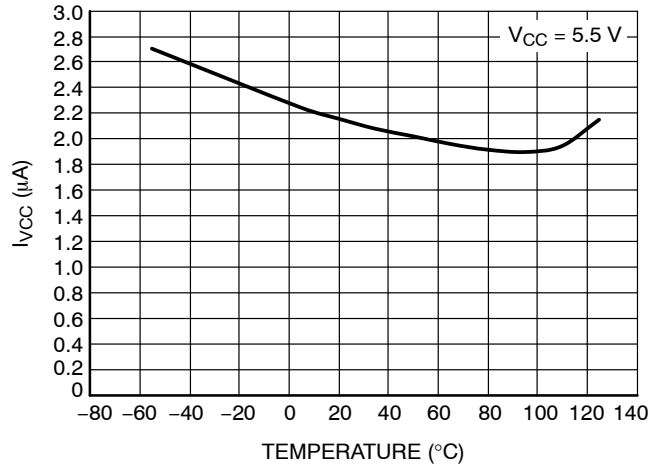


Figure 6. Supply Standby Current vs. Temperature

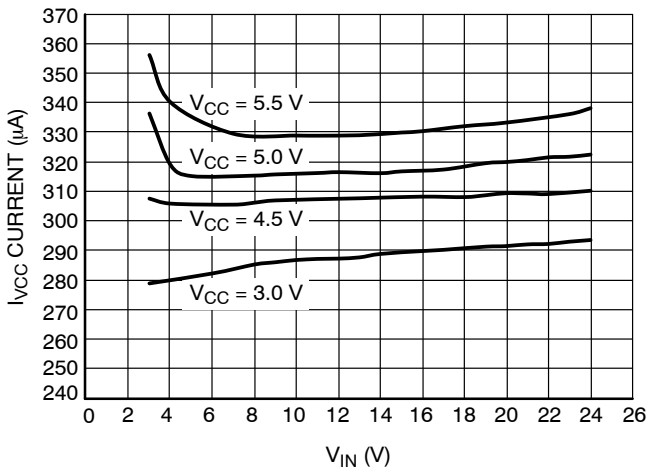


Figure 7. Dynamic Current vs. Input Voltage

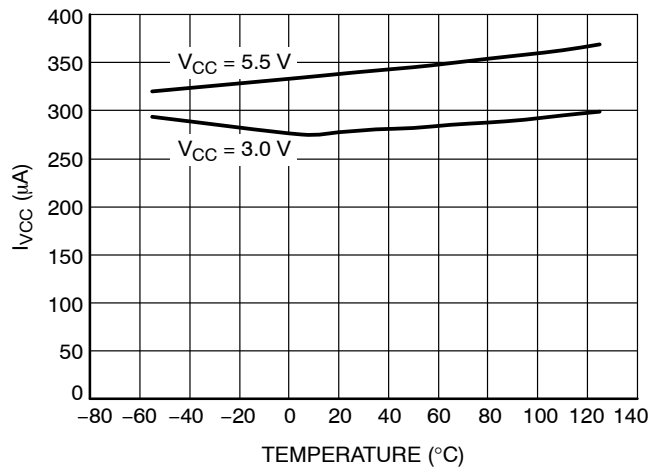


Figure 8. Supply Dynamic Current vs. Temperature

TYPICAL CHARACTERISTICS

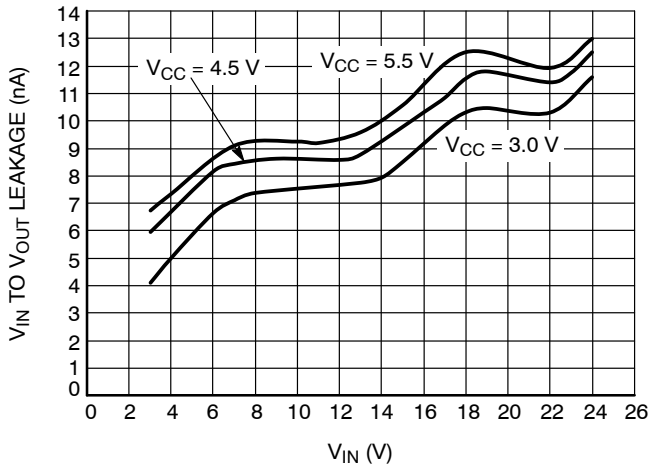


Figure 9. Input to Output Leakage vs. Input Voltage (EN = 0)

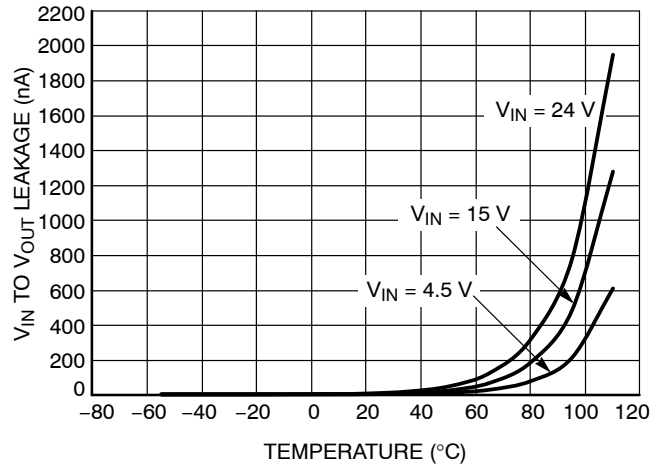


Figure 10. Input to Output Leakage vs. Temperature (EN = 0)

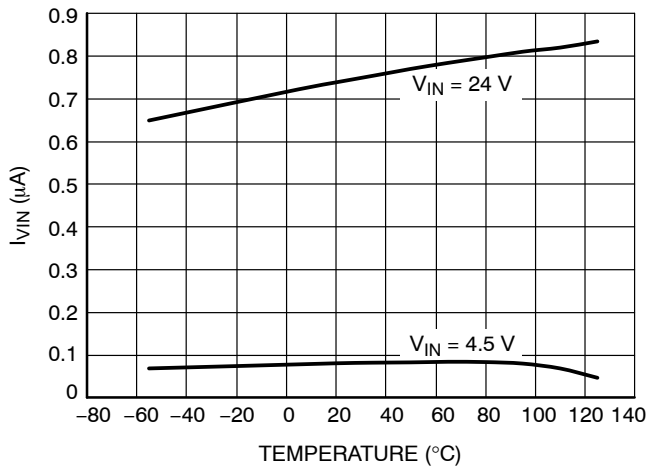


Figure 11. Vin Controller Current vs. Temperature (EN = 0)

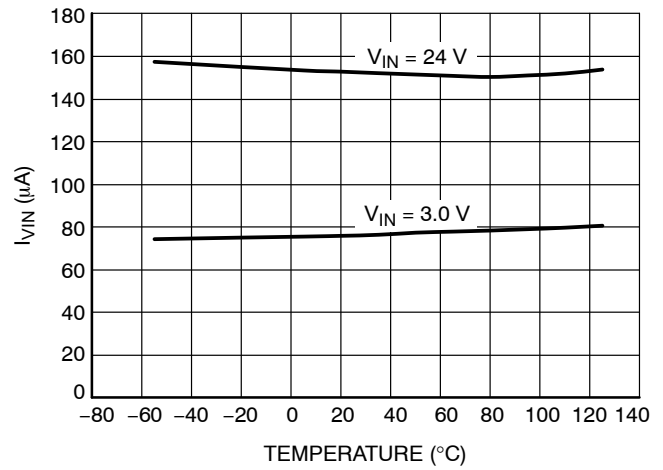


Figure 12. Vin Controller Current vs. Temperature (EN = HIGH)

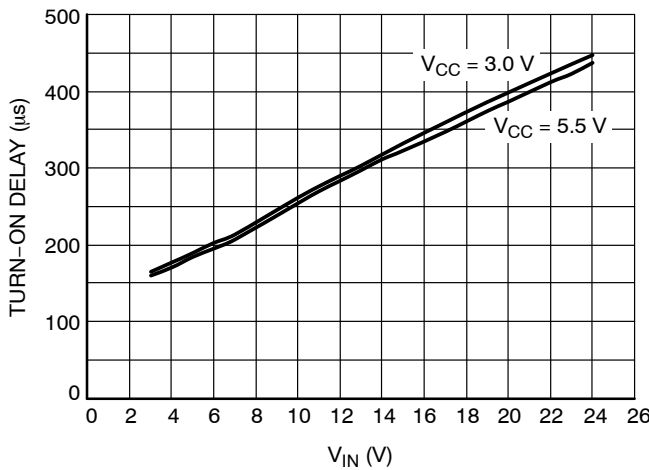


Figure 13. Output Turn-on Delay vs. Input Voltage

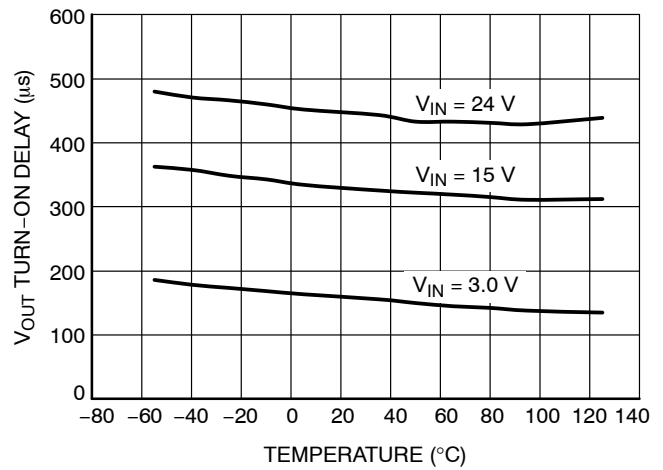


Figure 14. Output Turn-on Delay vs. Temperature

TYPICAL CHARACTERISTICS

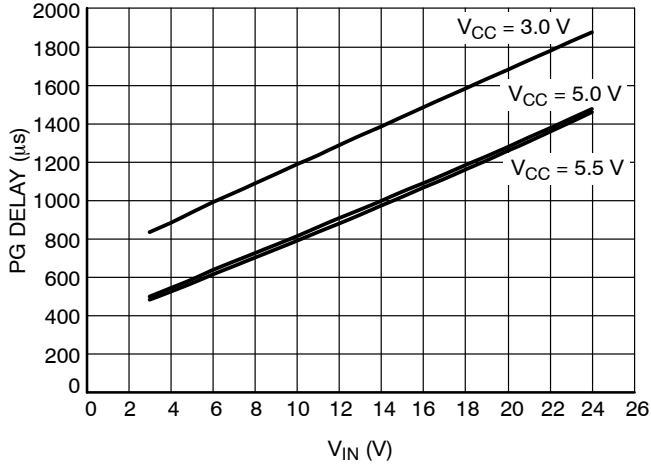


Figure 15. Power Good Turn-on Time vs. Input Voltage

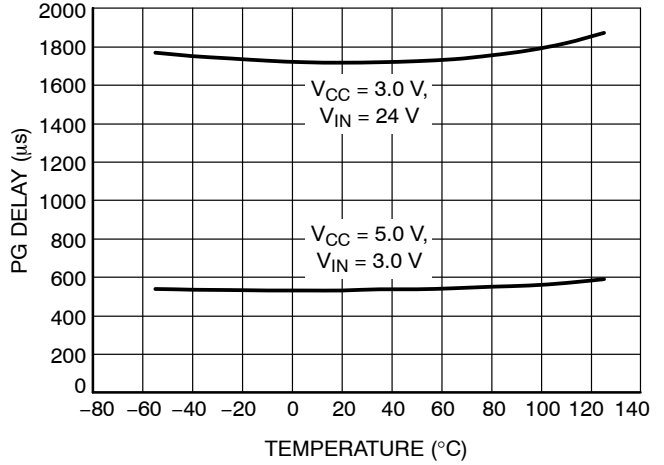


Figure 16. Power Good Turn-on vs. Temperature

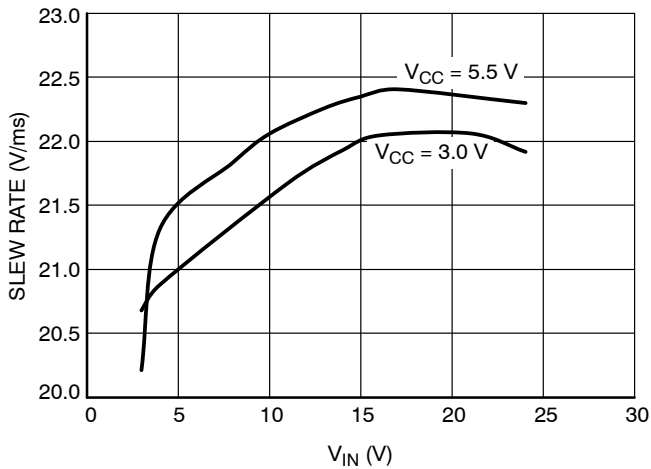


Figure 17. Default Slew Rate vs. Input Voltage

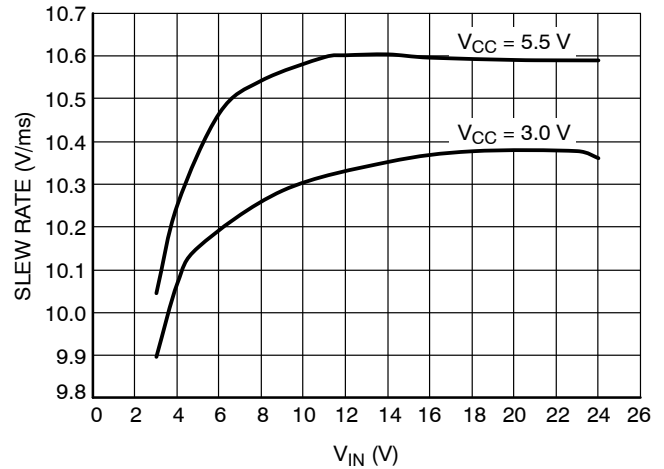


Figure 18. Slew Rate vs. Input Voltage (SR pin = 10 nF to GND)

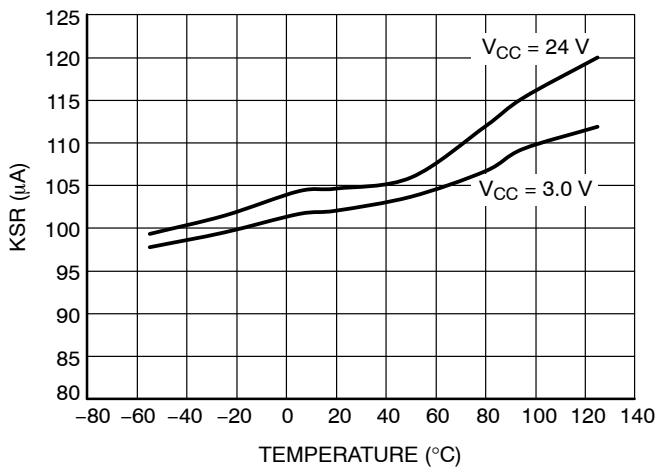


Figure 19. KSR vs. Temperature

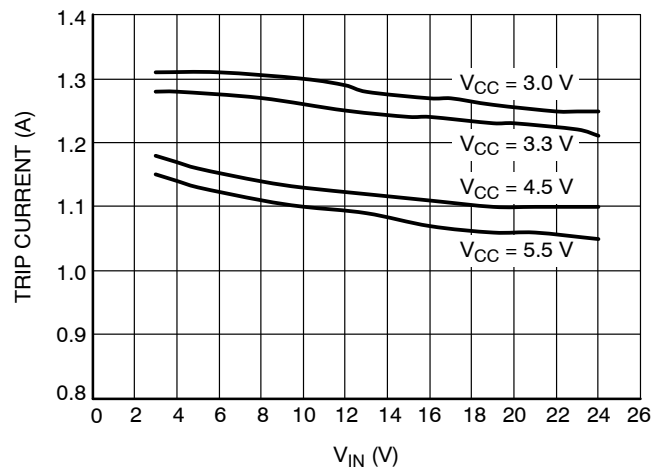


Figure 20. OCP Trip Current vs. Input Voltage (OCP = Float)

# NCP45750

## TYPICAL CHARACTERISTICS

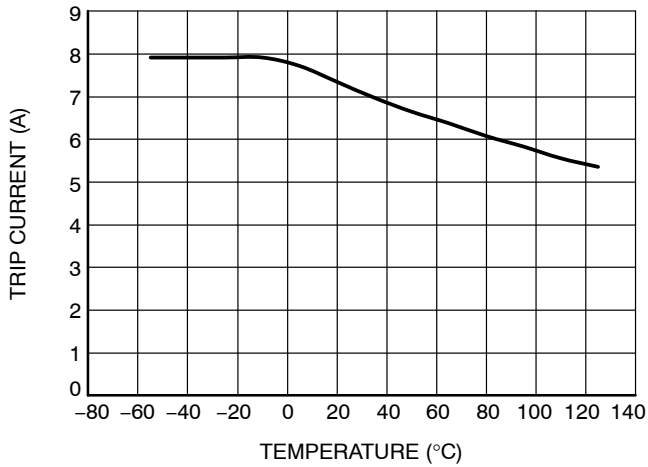


Figure 21. OCP Trip Current vs. Temperature (OCP = 32 kΩ)

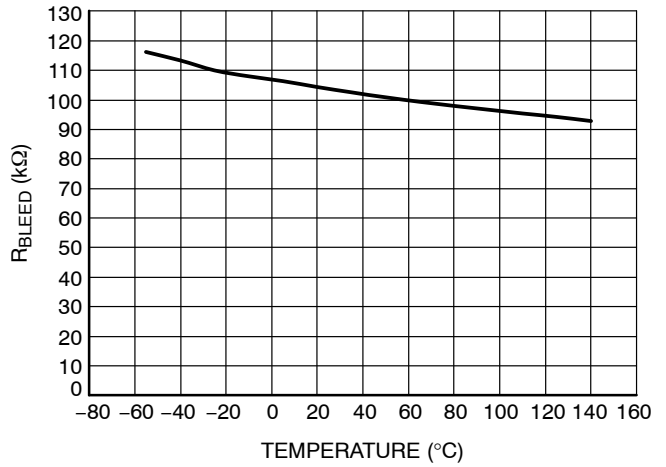


Figure 22. R\_BLEED vs. Temperature

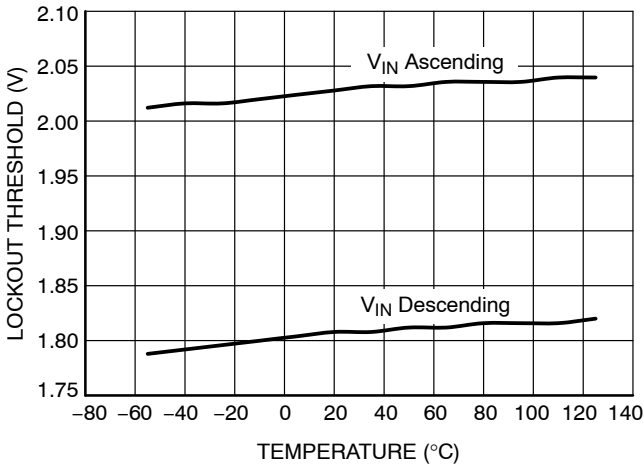


Figure 23. UVLO Trip Voltage vs. Temperature

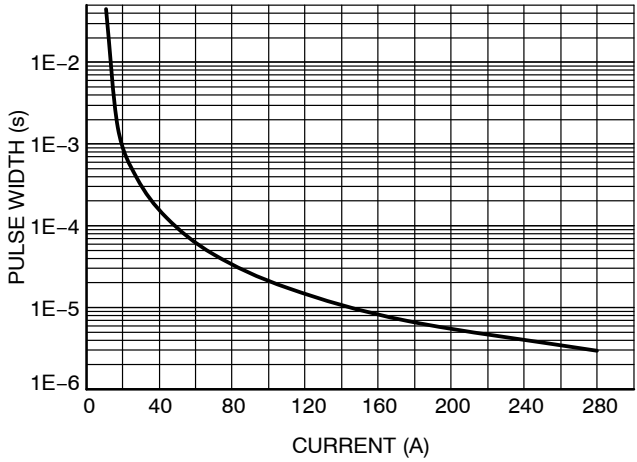


Figure 24. Safe Operating Area Transient Current

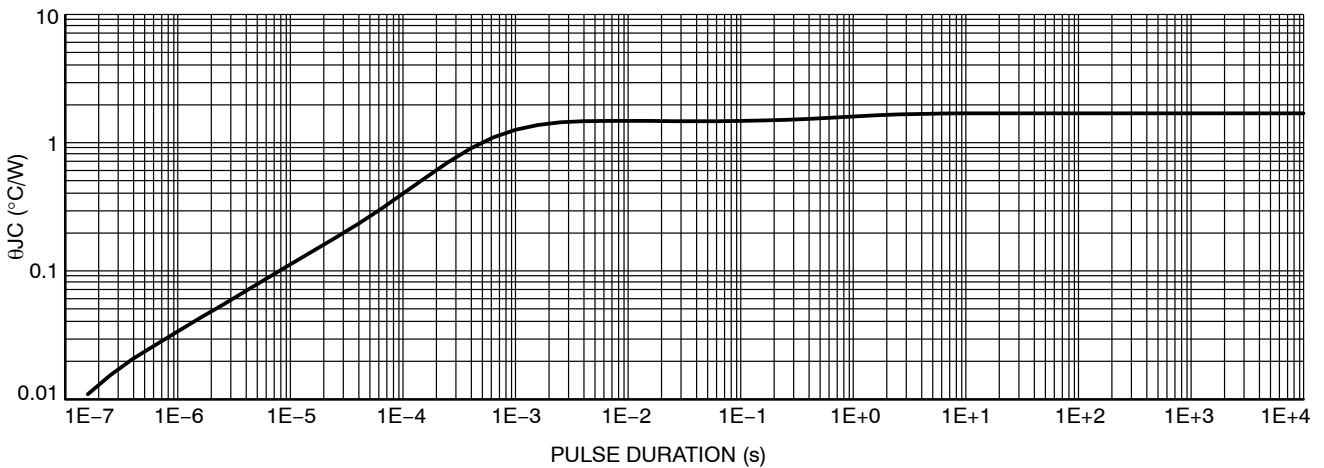


Figure 25. Transient Thermal Response

## APPLICATIONS INFORMATION

**Enable Control**

The NCP45750 part enables the MOSFET in an active-high configuration. When the EN pin is at a logic high level and the  $V_{CC}$  supply pin has an adequate voltage applied, the MOSFET will be enabled. When the EN pin is at a logic low level, the MOSFET will be disabled. An internal pull down resistor to ground on the EN pin ensures that the MOSFET will be disabled when not driven.

**Short-Circuit Protection**

The NCP45750 device is equipped with a short-circuit protection that helps protect the part and the system from a sudden high-current event, such as the output,  $V_{OUT}$ , being hard-shorted to ground.

Once active, the circuitry monitors the voltage difference between the  $V_{IN}$  pin and the  $V_{OUT}$  pin. When the difference is equal to the short-circuit protection threshold voltage, the MOSFET is turned off and the load bleed is activated. The part remains off and is latched in the Fault state until EN is toggled or  $V_{CC}$  supply voltage is cycled, at which point the MOSFET will be turned on in a controlled fashion with the normal output turn-on delay and slew rate. The short circuit protection feature protects the device from hard shorts ( $R_{SHORT} < 250 \text{ m}\Omega$   $V_{OUT}$  to GND) for  $V_{IN} \leq 18 \text{ V}$ . Hard short circuit testing used a  $10 \text{ m}\Omega$  short to ground for this scenario. The short circuit protection circuitry remains active regardless of the EN state to protect against enabling into a short circuit.

**Over-Current Protection**

The NCP45750 device is equipped with an over-current protection (OCP) that helps protect the part and the system from a high current event which exceeds the expected operational current (e.g., a soft short).

In the event that the current from the  $V_{IN}$  pin to the  $V_{OUT}$  pin exceeds the OCP threshold for longer than the blanking time, the MOSFET will shut down and the PG pin is driven low. Like the short-circuit protection, the part remains latched in the Fault state until EN is toggled or  $V_{CC}$  supply voltage is cycled, at which point the MOSFET will be turned on in a controlled fashion with the normal output turn-on delay and slew rate.

The over-current trip point is determined by the resistance between the OCP pin and ground. If no over-current protection is needed, then the OCP pin should be tied to GND; if the OCP protection is disabled in this way, the short-circuit protection will still remain active.

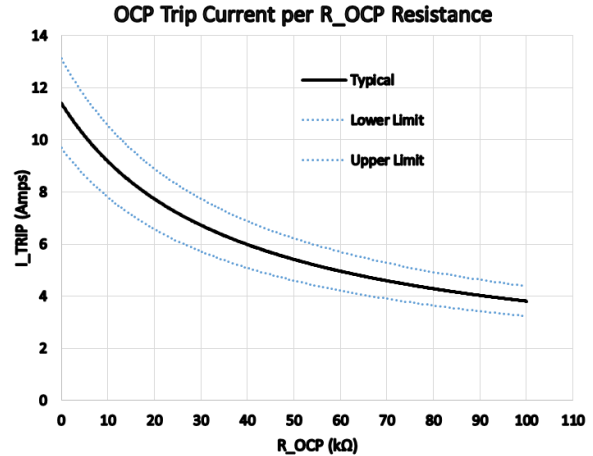


Figure 26. OCP Trip Current Setting

**Thermal Shutdown**

The thermal shutdown of the NCP45750 device protects the part from internally or externally generated excessive temperatures. This circuitry is disabled when EN is not active to reduce standby current. When an over-temperature condition is detected, the MOSFET is turned off and the load bleed is activated.

The part comes out of thermal shutdown when the junction temperature decreases to a safe operating temperature as dictated by the thermal hysteresis. Upon exiting a thermal shutdown state, and if EN remains active, the MOSFET will be turned on in a controlled fashion with the normal output turn-on delay and slew rate.

**Under Voltage Lockout**

The under voltage lockout of the NCP45750 device turns the MOSFET off and activates the load bleed when the input voltage,  $V_{IN}$ , drops below the under voltage lockout threshold. This circuitry is disabled when EN is not active to reduce standby current.

If the  $V_{IN}$  voltage rises above the under voltage lockout threshold, and EN remains active, the MOSFET will be turned on in a controlled fashion with the normal output turn-on delay and slew rate.

**Power Good**

The NCP45750 device has a power good output (PG) that can be used to indicate when the gate of the MOSFET is fully charged. The PG pin is an active-high, open-drain output

that requires an external pull up resistor, RPG, greater than or equal to 100 kΩ to an external voltage source.

The power good output can be used as the enable signal for other active-high devices in the system. This allows for guaranteed by design power sequencing and reduces the number of enable signals needed from the system controller. If the power good feature is not used in the application, the PG pin should be tied to GND.

### Slew Rate Control

The NCP45750 device is equipped with controlled output slew rate which provides soft start functionality. This limits the inrush current caused by capacitor charging and enables these devices to be used in hot swapping applications.

The slew rate can be decreased with an external capacitor added between the SR pin and ground. With an external capacitor present, the slew rate can be determined by the following equation:

$$\text{Slew Rate} = \frac{K_{SR}}{C_{SR}} \left[ \frac{V}{s} \right] \quad (\text{eq. 1})$$

where  $K_{SR}$  is the specified slew rate control constant, found on page 3, and  $C_{SR}$  is the capacitor added between the SR pin and ground. Note that the slew rate of the device will always be the lower of the default slew rate and the adjusted slew rate. Therefore, if the  $C_{SR}$  is not large enough to decrease the slew rate more than the specified default value, the slew rate of the device will be the default value.

### Capacitive Load

The peak in-rush current associated with the initial charging of the application load capacitance needs to stay below the specified  $I_{max}$ .  $C_L$  (capacitive load) should be less than  $C_{max}$  as defined by the following equation:

$$C_{max} = \frac{I_{max}}{SR_{typ}} \quad (\text{eq. 2})$$

where  $I_{max}$  is the maximum load current, and  $SR_{typ}$  is the typical default slew rate when no external load capacitor is added to the SR pin.

### OFF to ON Transition Energy Dissipation

The energy dissipation due to load current traveling from  $V_{IN}$  to  $V_{OUT}$  is very low during steady state operation due

to the low  $R_{ON}$ . When the EN signal is asserted high, the load switch transitions from an OFF state to an ON state. During this time, the resistance from  $V_{IN}$  to  $V_{OUT}$  transitions from high impedance to  $R_{ON}$ , and additional energy is dissipated in the device for a short period of time. The worst case energy dissipated during the OFF to ON transition can be approximated by the following equation:

$$E = 0.5 \cdot V_{IN} \cdot (I_{INRUSH} + 0.8 \cdot I_{LOAD}) \cdot dt \quad (\text{eq. 3})$$

where  $V_{IN}$  is the voltage on the  $V_{IN}$  pin,  $I_{INRUSH}$  is the inrush current caused by capacitive loading on  $V_{OUT}$ , and  $dt$  is the time it takes  $V_{OUT}$  to rise from 0 V to  $V_{IN}$ .  $I_{INRUSH}$  can be calculated using the following equation:

$$I_{INRUSH} = \frac{dv}{dt} \cdot C_L \quad (\text{eq. 4})$$

where  $dv/dt$  is the programmed slew rate, and  $C_L$  is the capacitive loading on  $V_{OUT}$ . To prevent thermal lockout or damage to the device, the energy dissipated during the OFF to ON transition should be limited to  $E_{TRANS}$  listed in operating ranges table.

## ecoSWITCH LAYOUT GUIDELINES

### Electrical Layout Considerations

Correct physical PCB layout is important for proper low noise accurate operation of all ecoSWITCH products.

**Power Planes:** The ecoSWITCH is optimized for extremely low  $R_{on}$  resistance, however, improper PCB layout can substantially increase source to load series resistance by adding PCB board parasitic resistance. Solid connections to the  $V_{IN}$  and  $V_{OUT}$  pins of the ecoSWITCH to copper planes should be used to achieve low series resistance and good thermal dissipation. The ecoSWITCH requires ample heat dissipation for correct thermal lockout operation. The internal FET dissipates load condition dependent amounts of power in the milliseconds following the rising edge of enable, and providing good thermal conduction from the packaging to the board is critical. Direct coupling of  $V_{IN}$  to  $V_{OUT}$  should be avoided, as this will adversely affect slew rates.

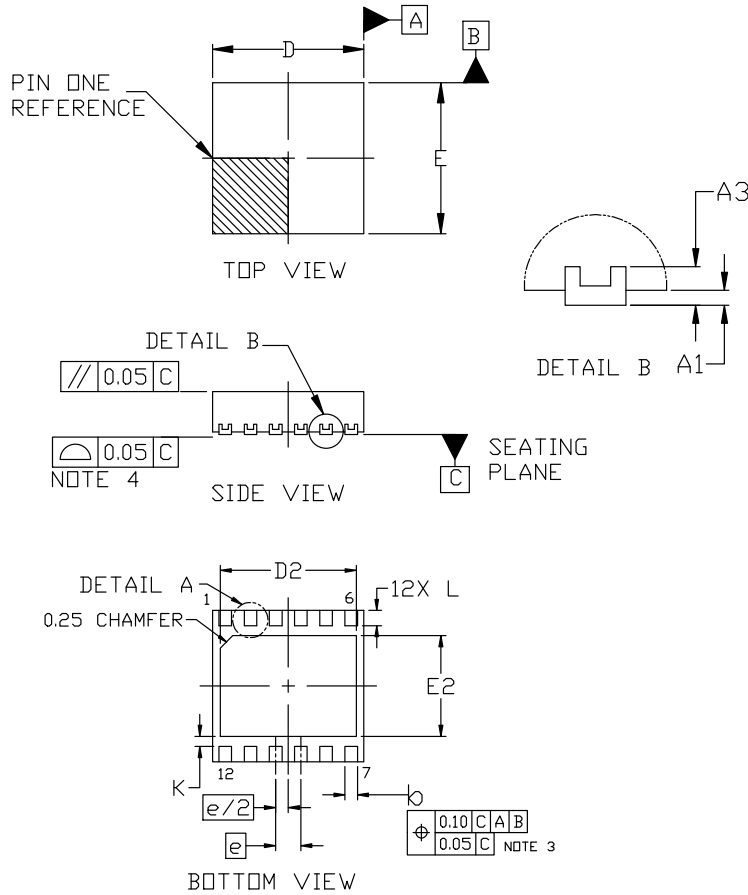
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 2:1

**DFN12 3x3, 0.5P**  
CASE 506DY  
ISSUE A

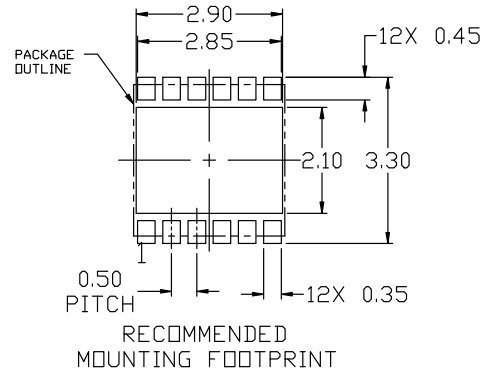
DATE 26 OCT 2022



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION *b* APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	---	---	0.05
A3	0.20 REF		
<i>b</i>	0.20	0.25	0.30
D	2.90	3.00	3.10
D2	2.40	2.50	2.60
E	2.90	3.00	3.10
E2	1.80	1.90	2.00
<i>e</i>	0.50 BSC		
K	0.25 REF		
L	0.20	0.30	0.40



\* For additional information on our Pb-Free strategy and soldering details, please download the DN Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



XXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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<b>DESCRIPTION:</b>	<b>DFN12 3X3, 0.5P</b>	<b>PAGE 1 OF 1</b>

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