

NC7SZ373

TinyLogic UHS D-Type Latch with 3-STATE Output

Description

The NC7SZ373 is a single positive edge-triggered D-type CMOS Latch with 3-STATE output from ON Semiconductor's Ultra High Speed Series of TinyLogic in the space saving SC70 6-lead package. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a very broad V_{CC} operating range. The device is specified to operate over the 1.65 V to 5.5 V V_{CC} range. The inputs and output are high impedance when V_{CC} is 0 V. Inputs tolerate voltages up to 5.5 V independent of V_{CC} operating voltage. The latch appears transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. The output tolerates voltages above V_{CC} in the 3-STATE condition.

Features

- Space Saving SC70 6-Lead Package
- Ultra Small MicroPak™ Leadless Package
- Ultra High Speed: t_{PD} 2.6 ns Typ into 50 pF at 5 V V_{CC}
- High Output Drive: ± 24 mA at 3 V V_{CC}
- Broad V_{CC} Operating Range: 1.65 V to 5.5 V
- Matches the Performance of LCX when Operated at 3.3 V V_{CC}
- Power Down High Impedance Inputs / Output
- Overvoltage Tolerant Inputs Facilitate 5 V to 3 V Translation
- Patented Noise / EMI Reduction Circuitry Implemented
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

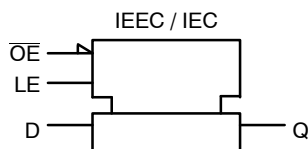


Figure 1. Logic Symbol



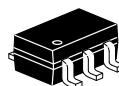
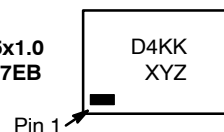
ON Semiconductor®

www.onsemi.com

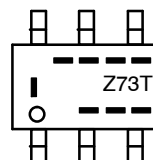
MARKING DIAGRAMS



SIP6 1.45x1.0
CASE 127EB



SC-88
(SC-70 6 Lead)
1.25x2
CASE 419AD-01



D4, Z73	= Specific Device Code
KK	= 2-Digit Lot Run Traceability Code
XY	= 2-Digit Date Code Format
Z	= Assembly Plant Code
----	= Year Coding Scheme
I- -	= Plant Code Identifier
T	= Die Run Code
- - -	= Eight-Week Datacoding Scheme

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 7 of this data sheet.

Connection Diagrams

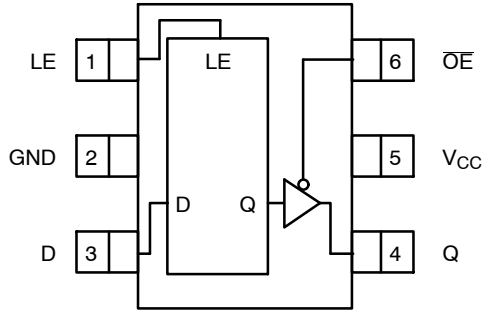


Figure 2. SC70 (Top View)

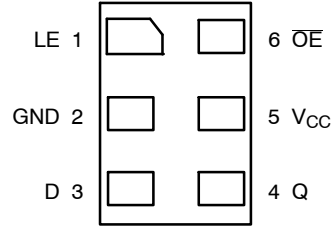
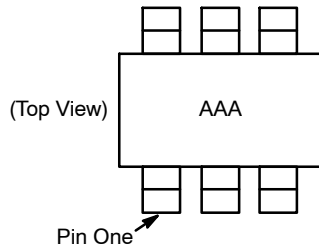


Figure 4. MicroPak (Top Through View)



AAA = Product Code Top Mark – see ordering code

NOTE: Orientation of Top Mark determines Pin One location.
Read the top product code mark left to right, Pin One is the lower left pin (see diagram).

Figure 3. Pin 1 Orientation

PIN DESCRIPTIONS

Pin Name	Description
D	Data Input
CP	Latch Enable Input
OE	Output Enable Input
Q	Latch Output

FUNCTION TABLE

Inputs			Output
LE	D	OE	Q
H	L	L	L
H	H	L	H
L	X	L	Q_{n-1}
X	X	H	Z

H = HIGH Logic Level

L = LOW Logic Level

Q_{n-1} = Previous state prior to HIGH-to-LOW transition of latch enable

X = Immaterial

Z = HIGH Impedance

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V _{CC}	Supply Voltage		–0.5	+6.5	V
V _{IN}	DC Input Voltage		–0.5	+6.5	V
V _{OUT}	DC Output Voltage		–0.5	+6.5	V
I _{IK}	DC Input Diode Current	V _{IN} < 0 V	–	–50	mA
I _{OK}	DC Output Diode Current	V _{OUT} < 0 V	–	–50	mA
I _{OUT}	DC Output Source / Sink Current		–	±50	mA
I _{CC} / I _{GND}	DC V _{CC} / GND Current		–	±50	mA
T _{STG}	Storage Temperature Range		–65	+150	°C
T _J	Junction Temperature under Bias		–	150	°C
T _L	Junction Lead Temperature (Soldering, 10 Seconds)		–	260	°C
P _D	Power Dissipation @ +85°C	SC–70–5	–	190	mW
		MicroPak	–	327	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	Supply Voltage Operating		1.65	5.5	V
	Supply Voltage Data Retention		1.5	5.5	
V _{IN}	Input Voltage		0	5.5	V
V _{OUT}	Output Voltage	Active State	0	V _{CC}	V
		3–STATE	0	5.5	V
t _r , t _f	Input Rise and Fall Time	V _{CC} = 1.8 V, 2.5 V ±0.2 V	0	20	ns/V
		V _{CC} = 3.3 V ±0.3 V	0	10	
		V _{CC} = 5.5 V ±0.5 V	0	5	
T _A	Operating Temperature		–40	+85	°C
θ _{JA}	Thermal Resistance		–	350	°C/W
		SC–70–5	–	659	°C/W
		MicroPak	–	382	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. Unused inputs must be held HIGH or LOW. They may not float.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	Conditions		T _A = +25°C			T _A = -40 to +85°C		Unit
					Min	Typ	Max	Min	Max	
V _{IH}	HIGH Level Control Input Voltage	1.65 to 1.95			0.65 V _{CC}	–	–	0.65 V _{CC}	–	V
		2.3 to 5.5			0.7 V _{CC}	–	–	0.7 V _{CC}	–	
V _{IL}	LOW Level Control Input Voltage	1.65 to 1.95			–	–	0.35 V _{CC}	–	0.35 V _{CC}	V
		2.3 to 5.5			–	–	0.3 V _{CC}	–	0.3 V _{CC}	
V _{OH}	HIGH Level Control Output Voltage	1.65	V _{IN} = V _{IH}	I _{OH} = -100 µA	1.55	1.65	–	1.55	–	V
		1.8			1.7	1.8	–	1.7	–	
		2.3			2.2	2.3	–	2.2	–	
		3.0			2.9	3.0	–	2.9	–	
		4.5			4.4	4.5	–	4.4	–	
		1.65			1.24	1.52	–	1.29	–	
		2.3		I _{OH} = -8 mA	1.9	2.15	–	1.9	–	
		3.0		I _{OH} = -16 mA	2.4	2.8	–	2.4	–	
		3.0		I _{OH} = -24 mA	2.3	2.68	–	2.3	–	
		4.5		I _{OH} = -32 mA	3.8	4.2	–	3.8	–	
V _{OL}	LOW Level Control Output Voltage	1.65	V _{IN} = V _{IL}	I _{OL} = 100 µA	–	0.0	0.08	–	0.0	V
		1.8			–	0.0	0.1	–	0.1	
		2.3			–	0.0	0.1	–	0.1	
		3.0			–	0.0	0.1	–	0.1	
		4.5			–	0.0	0.1	–	0.1	
		1.65		I _{OL} = 4 mA	–	0.08	0.24	–	0.24	
		2.3		I _{OL} = 8 mA	–	0.10	0.3	–	0.3	
		3.0		I _{OL} = 16 mA	–	0.15	0.4	–	0.4	
		3.0		I _{OL} = 24 mA	–	0.22	0.55	–	0.55	
		4.5		I _{OL} = 32 mA	–	0.22	0.55	–	0.55	
I _{IN}	Input Leakage Current	1.65 to 5.5	0 ≤ V _{IN} ≤ 5.5 V		–	–	±0.1	–	±1.0	µA
I _{OZ}	3-STATE Output Leakage	1.65 to 5.5	V _{IN} = V _{IL} or V _{IH} 0 ≤ V _{OUT} ≤ 5.5 V		–	–	±0.5	–	±5.0	µA
I _{OFF}	Power Off Leakage Current	0.0	V _{IN} or V _{OUT} = 5.5 V		–	–	1.0	–	10	µA
I _{CC}	Quiescent Supply Current	1.65 to 5.5	V _{IN} = 5.5 V, GND		–	–	1.0	–	10	µA

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = +25°C			T _A = -40 to +85°C		Unit
				Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay D to Q	1.65	C _L = 15 pF, R _D = 1 MΩ, S ₁ = Open (Figures 5, 7)	–	9.0	15.0	–	16.0	ns
		1.8		–	6.1	10.0	–	10.5	
		2.5 ±0.2		–	3.6	6.5	–	6.8	
		3.3 ±0.3		–	2.7	4.6	–	5.0	
		5.0 ±0.5		–	2.0	3.4	–	3.7	
		3.3 ±0.3	C _L = 50 pF, R _D = 500 Ω, S ₁ = Open (Figures 5, 7)	–	3.3	5.5	–	6.2	
		5.0 ±0.5		–	2.6	4.3	–	4.8	
t _{PLH} t _{PHL}	Propagation Delay LE to Q	1.65	C _L = 15 pF, R _D = 1 MΩ, S ₁ = Open (Figures 5, 7)	–	9.0	1.45	–	15.0	ns
		1.8		–	6.0	9.6	–	10.0	
		2.5 ±0.2		–	3.5	6.1	–	6.6	
		3.3 ±0.3		–	2.6	4.4	–	4.8	
		5.0 ±0.5		–	2.0	3.2	–	3.5	
		3.3 ±0.3	C _L = 50 pF, R _D = 500 Ω, S ₁ = Open (Figures 5, 8)	–	3.3	5.3	–	6.2	
		5.0 ±0.5		–	2.6	4.2	–	4.6	
t _{PZL} t _{PZH}	Output Enable Time	1.65	C _L = 50 pF, V _I = 2 × V _{CC} , R _U , R _D = 500 Ω, S ₁ = GND for t _{PZH} S ₁ = V _I for t _{PZL} (Figures 5, 8)	–	9.0	13.5	–	14.6	ns
		1.8		–	6.0	9.0	–	9.5	
		2.5 ±0.2		–	3.7	6.0	–	6.6	
		3.3 ±0.3		–	2.8	5.0	–	5.3	
		5.0 ±0.5		–	2.2	3.7	–	3.9	
t _{PLZ} t _{PHZ}	Output Disable Time	1.65	C _L = 50 pF, V _I = 2 × V _{CC} , R _U , R _D = 500 Ω, S ₁ = GND for t _{PHZ} S ₁ = V _I for t _{PLZ} (Figures 5, 8)	–	7.7	12.0	–	13.0	ns
		1.8		–	5.1	8.0	–	8.5	
		2.5 ±0.2		–	3.5	6.0	–	6.3	
		3.3 ±0.3		–	2.8	4.5	–	4.7	
		5.0 ±0.5		–	2.3	3.7	–	3.9	
t _S	Setup Time, D to LE	2.5 ±0.2	C _L = 50 pF, R _D = 500 Ω, S ₁ = Open (Figures 5, 9)	–	–	–	2.0	–	ns
		3.3 ±0.3		–	–	–	1.5	–	
		5.0 ±0.5		–	–	–	1.5	–	
t _H	Hold Time, D to LE	2.5 ±0.2	C _L = 50 pF, R _D = 500 Ω, S ₁ = Open (Figures 5, 9)	–	–	–	1.5	–	ns
		3.3 ±0.3		–	–	–	1.5	–	
		5.0 ±0.5		–	–	–	1.5	–	
t _W	Pulse Width, LE	2.5 ±0.2	C _L = 50 pF, R _D = 500 Ω, S ₁ = Open (Figures 5, 9)	–	–	–	3.0	–	ns
		3.3 ±0.3		–	–	–	3.0	–	
		5.0 ±0.5		–	–	–	3.0	–	

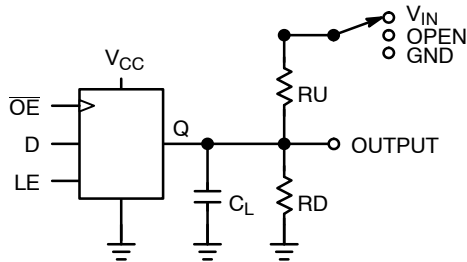
CAPACITANCE ($T_A = +25^\circ\text{C}$, $f = 1\text{ MHz}$)

Symbol	Parameter	Condition	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{CC} = \text{Open}$, $V_{IN} = 0\text{ V or } V_{CC}$	3	–	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3\text{ V}$, $V_{IN} = 0\text{ V or } V_{CC}$	4	–	pF
C_{PD}	Power Dissipation Capacitance (Note 2)	$V_{CC} = 3.3\text{ V}$ $V_{CC} = 5.0\text{ V}$	14 17	– –	pF

2. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 6)

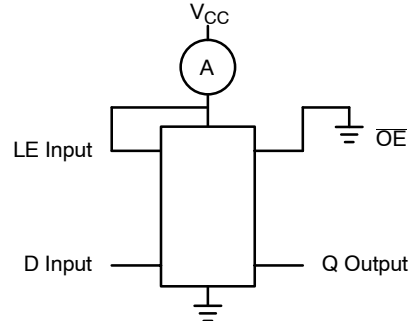
C_{PD} is related to I_{CCD} dynamic operating current by the expression: $I_{CCD} = (C_{PD}) (V_{CC}) (f_{IN}) + (I_{CC\text{static}})$.

AC Loading and Waveforms



C_L includes load and stray capacitance
Input PRR = 1.0 MHz, $t_W = 500\text{ ns}$.

Figure 5. AC Test Circuit



D Input = AC Waveform; $t_r = t_f = 1.8\text{ ns}$;
D Input PRR = 10 MHz; Duty Cycle = 50%.

Figure 6. I_{CCD} Test Circuit

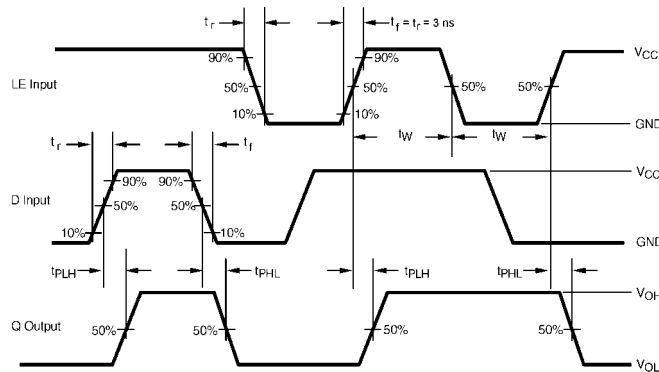


Figure 7. AC Waveforms

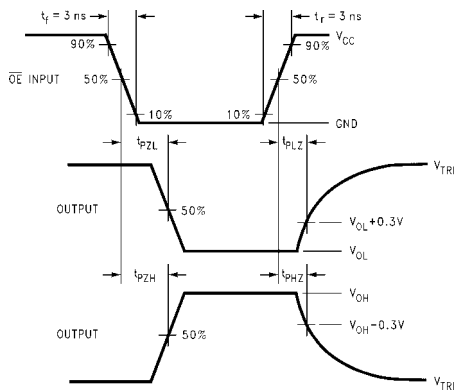


Figure 8. AC Waveforms

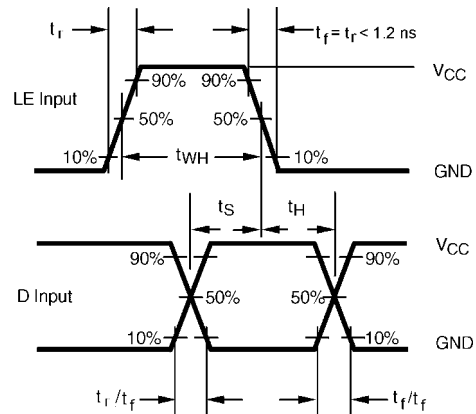


Figure 9. AC Waveforms

NC7SZ373

ORDERING INFORMATION

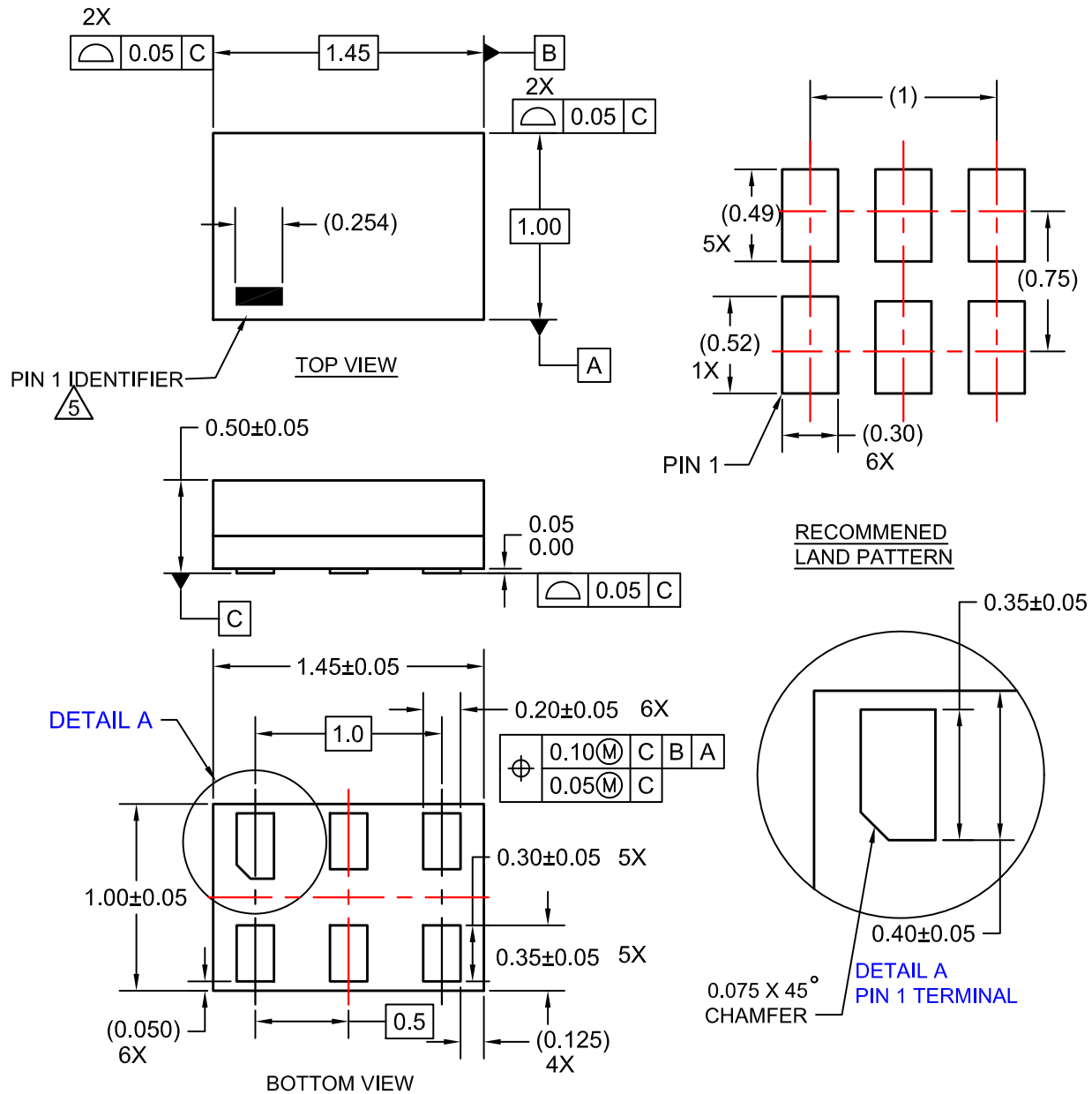
Device	Top Mark	Packages	Shipping [†]
NC7SZ373P6X	Z73	6-Lead SC70, EIAJ SC88, 1.25 mm Wide	3000 / Tape & Reel
NC7SZ373L6X	D4	6-Lead MicroPak, 1.00 mm Wide	5000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MicroPak is trademark of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries.

SIP6 1.45X1.0
CASE 127EB
ISSUE O

DATE 31 AUG 2016



NOTES:

1. CONFORMS TO JEDEC STANDARD MO-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-2009
4. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

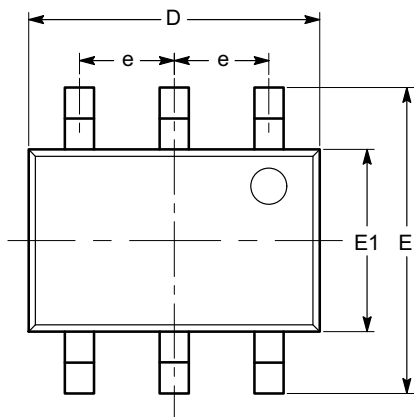
DOCUMENT NUMBER:	98AON13590G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
STATUS:	ON SEMICONDUCTOR STANDARD	
NEW STANDARD:		
DESCRIPTION:	SIP6 1.45X1.0	
		PAGE 1 OF 2

[illegible]

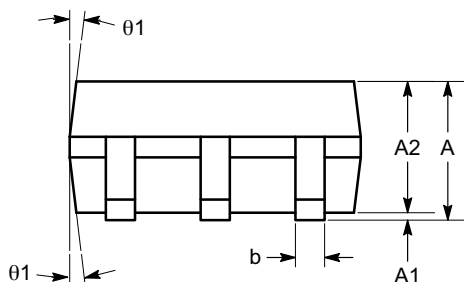
ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

SC-88 (SC-70 6 Lead), 1.25x2
CASE 419AD-01
ISSUE A

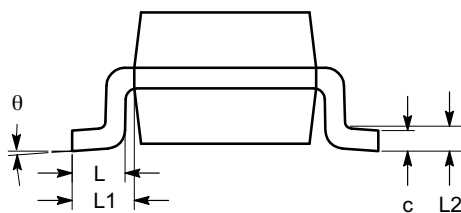
DATE 07 JUL 2010



TOP VIEW



SIDE VIEW



END VIEW

SYMBOL	MIN	NOM	MAX
A	0.80		1.10
A1	0.00		0.10
A2	0.80		1.00
b	0.15		0.30
c	0.10		0.18
D	1.80	2.00	2.20
E	1.80	2.10	2.40
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.26	0.36	0.46
L1	0.42 REF		
L2	0.15 BSC		
θ	0°		8°
θ1	4°		10°

Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-203.

DOCUMENT NUMBER:	98AON34266E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
STATUS:	ON SEMICONDUCTOR STANDARD	
REFERENCE:		
DESCRIPTION:	SC-88 (SC-70 6 LEAD), 1.25X2	PAGE 1 OF 2

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative