NB685A

28 V, 12 A, Low Iq, High Current Synchronous Buck Converter with +/- 1 A LDO and Buffered Reference

DESCRIPTION

The NB685A provides a complete power supply with the highest power density for DDR3, DDR3L, LPDDR3, and DDR4 memory. It integrates a high-frequency, synchronous, rectified, step-down, switch-mode converter (VDDQ) with a 1 A sink/source LDO (VTT) and buffered low noise reference (VTTREF).

The NB685A operates at high efficiency over a wide output current load range based on MPS proprietary switching loss reduction technology and internal low Ron power MOSFETs.

Adaptive constant-on-time (COT) control mode provides fast transient response and eases loop stabilization. The DC auto-tune loop provides good load and line regulation.

The VTT LDO provides 1 A sink/source current capability and requires only a 22 µF ceramic capacitor. The VTTREF tracks VDDQ/2 with excellent 1% accuracy.

Full protection features include OC limit, OVP, UVP, over-temperature warning (OTW), and thermal shutdown.

The converter requires a minimum number of external components and is available in a QFN 3mm x 3mm package.

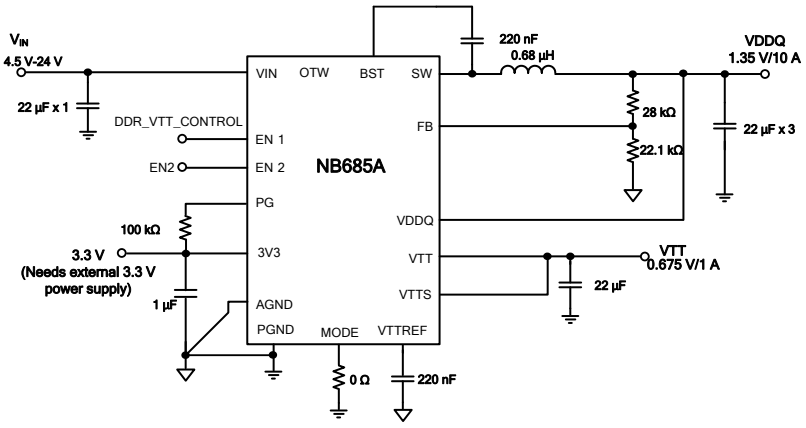
FEATURES

- Wide 4.5 V to 28 V Operating Input Range
- Compatible for IMVP8
- 135 µA Low Quiescent Current
- 12 A Continous Output Current
- 13 A Peak Output Current
- Selectable Ultrasonic Mode
- Selectable 500 k/700 k Switching Frequency
- Built-in +/- 1 A VTTLDO
- 1% Buffered VTTREF Output
- Adaptive COT for Fast Transient
- DC Auto-Tune Loop
- Stable with POSCAP and Ceramic Output Capacitors
- Over-Temperature Warning
- Internal Soft Start
- Output Discharge
- OCL, OVP, UVP, and Thermal Shutdown
- Latch-Off Reset via EN or Power Cycle
- QFN 3mm x 3mm Package

APPLICATIONS

- Laptop Computers
- Networking Systems
- Servers
- Distributed Power Systems

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
NB685AGQ	QFN-16 (3mm x 3mm)	*See Below*

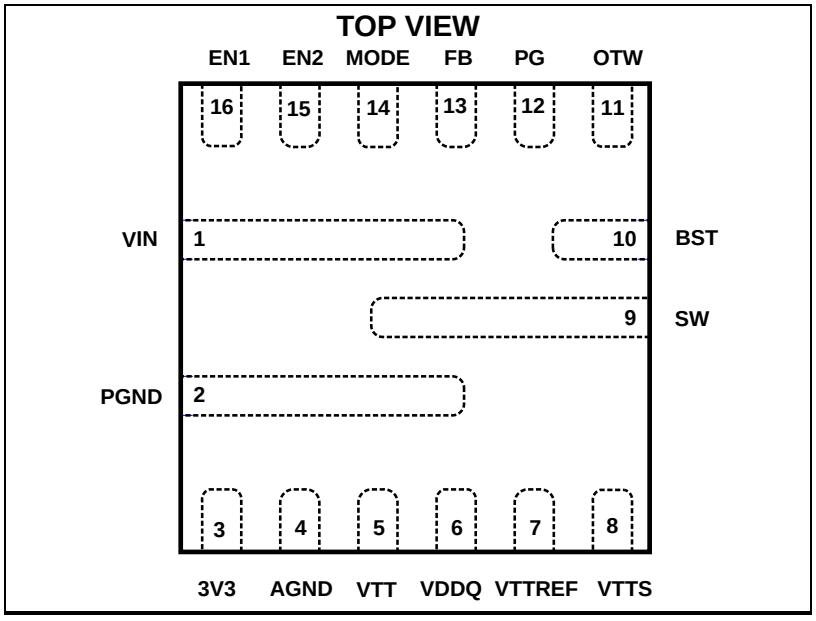
* For Tape & Reel, add suffix –Z (e.g. NB685AGQ–Z)

TOP MARKING

AREY
LLL

ARE: Product code of NB685AGQ
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) ..... 28 V
V_{SW}(DC) ..... -1V to 26 V
V_{SW} (25 ns) ..... -3.6 V to 28 V
V_{BST} ..... V_{SW} + 4.5 V
I_{EN1},I_{EN2} ..... 100 µA
All other pins ..... -0.3 V to +4.5 V
Continuous power dissipation (T_A = +25°C)(2)
QFN-16 (3mm x 3mm) ..... 2.3 W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 4.5 V to 24 V
Supply voltage (V_{CC}) ..... 3.15 V to 3.5 V
Output voltage (V_{DDQ}) ..... 0.6 V to 3.3 V(5)
I_{EN1},I_{EN2} ..... 50 µA
Operating junction temp. (T_J) ..... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

	θ_{JA}	θ_{JC}	
QFN-16 (3mm x 3mm)	55	13	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.
5) For applications that need 3.3 V < Vout < 5.5 V, special design requirements are needed. Please refer to the application information section. VDDQ still needs voltage ≤ 3.3 V.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12 V, 3V3 = 3.3 V, T_J = 25°C, R_{MODE}=0, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply current						
3V3 supply current in normal mode	I_{3V3}	V_{EN1} = V_{EN2} = 3 V, no load		185		µA
3V3 supply current in S3 mode	I_{3V3_S3}	V_{EN1} = 0 V, V_{EN2} = 3 V, no load		135		µA
3V3 shutdown current	I_{3V3_SDN}	V_{EN1} = V_{EN2} = 0 V, no load			1	µA
MOSFET						
High-side switch on resistance	HS_{RDS-ON}	T_J = 25°C		19.5		mΩ
Low-side switch on resistance	LS_{RDS-ON}	T_J = 25°C		6.6		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0 V, V_{SW} = 0 V		0	1	µA
Current limit						
Low-side valley current limit	I_{LIMIT}		12	13	14	A
Switching frequency and minimum off time						
Switching frequency	F_S	R_{MODE} = 0		700		kHz
		R_{MODE} = 150 k		500		kHz
Constant on timer	T_{ON}	Vin = 6 V, V_{OUT} = 3 V, R_{MODE} = 150 k	1100	1200	1300	ns
Minimum on time[6]	T_{ON_MIN}			70		ns
Minimum off time[6]	T_{OFF_MIN}			300		ns
Ultrasonic mode						
Ultrasonic mode operation period	T_{USM}	V_{FB} = 0.62 V		32		µs
Protection						
OVP threshold	V_{OVP}		125	130	135	$\%V_{REF}$
UVP-1 threshold	V_{UVP-1}		70%	75%	80%	V_{REF}
UVP-1 foldback timer[6]	T_{UVP-1}			30		µs
UVP-2 threshold	V_{UVP-2}		45%	50%	55%	V_{REF}
Reference and soft start, soft stop						
Reference voltage	V_{REF}		594	600	606	mV
Feedback current	I_{FB}	V_{FB} = 0.62 V		10	50	nA
Soft-start time	T_{SStart}	EN to PG up	1.8	2.2	2.6	ms
Soft-stop time	T_{SStop}			2		ms

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12 V, 3V3 = 3.3 V, T_J = 25°C, R_{MODE} = 0, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Enable and UVLO						
En1 rising threshold	V_{EN1_TH}		0.54	0.59	0.64	V
En1 hysteresis	$V_{EN1-HYS}$			125		mV
En2 rising threshold	V_{EN2_TH}		1.12	1.22	1.32	V
En2 hysteresis	$V_{EN2-HYS}$			125		mV
Enable input current	$I_{EN1/2}$	$V_{EN1/2}$ = 2 V			5	µA
		$V_{EN1/2}$ = 0 V			1	
VCC under-voltage lockout threshold—rising	VCC_{Vth}		2.9	3.0	3.1	V
VCC under-voltage lockout threshold—hysteresis	VCC_{HYS}			220		mV
VIN under-voltage lockout threshold—rising	VIN_{VTH}			4.2	4.4	V
VIN under-voltage lockout threshold—hysteresis	VIN_{HYS}			360		mV
Power good						
PG when FB rising (good)	$PG_{\_Rising(GOOD)}$	V_{FB} rising, percentage of V_{FB}		95		%
PG when FB falling (fault)	$PG_{\_Falling(Fault)}$	V_{FB} falling, percentage of V_{FB}		90		
PG when FB rising (fault)	$PG_{\_Rising(Fault)}$	V_{FB} rising, percentage of V_{FB}		115		
PG when FB falling (good)	$PG_{\_Falling(GOOD)}$	V_{FB} falling, percentage of V_{FB}		105		
PG low to high delay	PG_{Td}			3		µs
EN low to PG low delay	$PG_{Td\ EN\ low}$				1	µs
Power good sink current capability	V_{PG}	Sink 4 mA			0.4	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12 V, T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
VTTREF output						
VTTREF output voltage	V_{TTREF}			$V_{DDQ}/2$		
Output voltage tolerance to VDDQ	V_{TTREF}/ V_{DDQ}	I_{VTTREF} < 0.1 mA, 1 V < V_{DDQ} < 1.5 V	49.2%	50%	50.8%	
		I_{VTTREF} < 10 mA, 1 V < V_{DDQ} < 1.5 V	49%	50%	51%	
Current limit	I_{LIMIT_VTTREF}		13	15		mA
VTT LDO						
VTT output voltage	V_{TT}			$V_{DDQ}/2$		
VTT tolerance to VTTREF	V_{TT}-V_{TTREF}	-10 mA < I_{VTT} < 10 mA, V_{DDQ} = [1 V-1.5 V]	-15		15	mV
		-0.6 A < I_{VTT} < 0.6 A, V_{DDQ} = [1 V-1.5 V]	-20		20	mV
		-1 A < I_{VTT} < 1 A, V_{DDQ} = [1 V-1.5 V]	-25		25	mV
Source current limit	$I_{LIMIT\ SOURCE}$		1.2	1.5		A
Sink current limit	$I_{LIMIT\ SINK}$		1.2	1.5		A
OTW#						
Over temp warning(6)	$T_{OTW\#}$			130		°C
OTW# hysteresis(6)	$T_{OTW\#\ HYS}$			25		°C
OTW# sink current capability	$V_{OTW\#}$	Sink 4 mA			0.4	V
OTW# leakage current	$I_{OTW\#}$	$V_{OTW\#}$ = 3.3 V			1	µA
OTW# assertion time(6)	$T_{OTW\#}$			32		ms
Thermal protection						
Thermal shutdown(6)	T_{SD}			145		°C
Thermal shutdown hysteresis	T_{SD_HYS}			25		°C

NOTE:

6) Guaranteed by design.

PIN FUNCTIONS

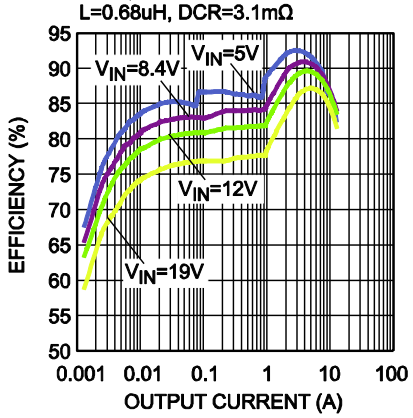
PIN #	Name	Description
1	VIN	**Supply voltage**. VIN supplies power for the internal MOSFET and regulator. The NB685A operates from a +4.5 V to +24 V input rail. An input capacitor is needed to decouple the input rail. Use wide PCB traces and multiple vias to make the connection.
2	PGND	**Power ground**. Use wide PCB traces and multiple vias to make the connection.
3	3V3	**External 3V3 VCC input for control and driver.** Place a 1 µF decoupling capacitor close to 3V3 and AGND. It is recommended to form an RC filter.
4	AGND	**Analog ground**. The internal reference is referred to AGND. Connect the GND of the FB divider resistor to AGND for better load regulation.
5	VTT	**VTT LDO output.** Decouple with a minimum 22 µF ceramic capacitor as close to VTT as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics.
6	VDDQ	**Input of VTTLDO, also used for Vout sense**. Do NOT float VDDQ at any time. Connect VDDQ to the output capacitor of the regulator directly with a thick (>100 mil) trace.
7	VTTREF	**Buffered VTT reference output.** Decouple with a minimum 0.22 µF ceramic capacitor as close to VTTREF as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics.
8	VTTS	**VTT output sense.** Connect VTTS to the output capacitor of the VTT regulator directly.
9	SW	**Switch output.** Connect SW to the inductor and bootstrap capacitor. SW is connected to VIN when the HS-FET is on and to PGND when the LS-FET is on. Use wide and short PCB traces to make the connection. SW is noisy, so keep sensitive traces away from SW.
10	BST	**Bootstrap.** A capacitor connected between SW and BST is required to form a floating supply across the high-side switch driver.
11	OTW#	**Over-temperature status**. Used to indicate that the part is close to the OTP. OTW# is pulled low once the junction temperature is higher than the over-temperature warning threshold. OTW# can be left open if not used.
12	PG	**Power good output.** PG is an open-drain signal. PG is high if the output voltage is within a proper range.
13	FB	**Feedback.** An external resistor divider from the output to GND (tapped to FB) sets the output voltage. Place the resistor divider as close to FB as possible. Avoid vias on the FB traces.
14	MODE	**The switching frequency and ultrasonic mode selection pin.** A 1% pull-down resistor is needed.
15/16	EN2/EN1	**Enable.** EN1 and EN2 are digital inputs, which are used to enable or disable the internal regulators. Once EN1 = EN2 = 1, the VDDQ regulator, VTT LDO, and VTTREF output are turned on; when EN1 = 0 and EN2 = 1, all the regulators are on except VTT LDO. All the regulators are turned off when EN2 = 0 or EN1 = EN2 = 0. Do NOT float EN1 at any time. If the VTT LDO function is not used, tie EN1 to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 20 V, V_{DDQ} = 1.35 V, L = 0.68 µH/3.1 mΩ, F_{SW} = 700 kHz, unless otherwise noted.

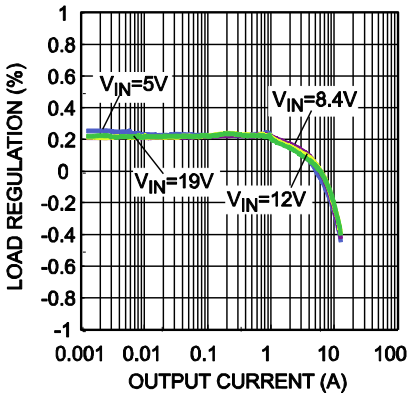
Efficiency vs. Load Current

V_{DDQ}=1.35V, F_{SW}=700kHz, L=0.68uH, DCR=3.1mΩ



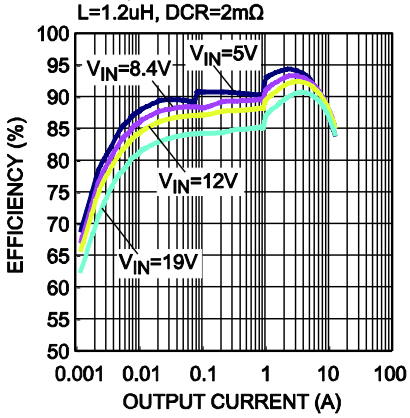
Load Regulation

V_{DDQ}=1.35V, F_{SW}=700kHz, L=0.68µH, DCR=3.1mΩ



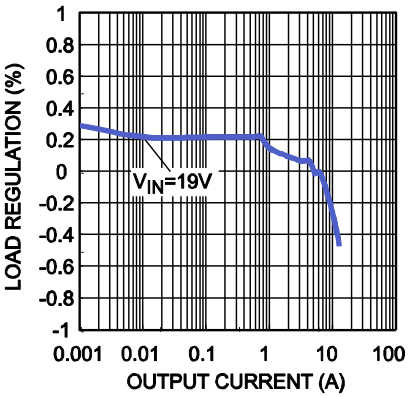
Efficiency vs. Load Current

V_{DDQ}=1.35V, F_{SW}=500kHz, L=1.2uH, DCR=2mΩ



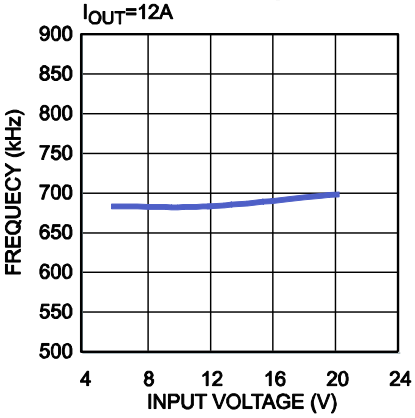
Load Regulation

V_{DDQ}=1.35V, F_{SW}=500kHz, L=1.2uH, DCR=2mΩ



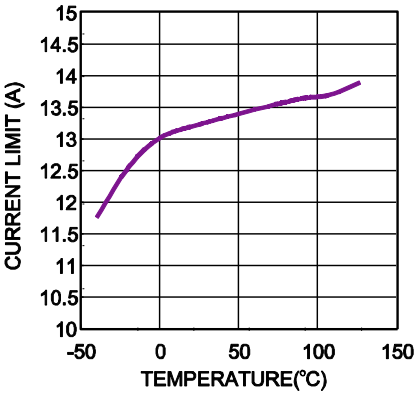
Switch Frequency vs. Input Voltage

I_{OUT}=12A



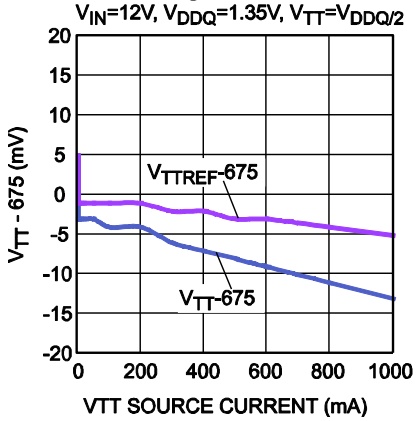
Valley Current Limit vs. Temperature

V_{IN}=12V



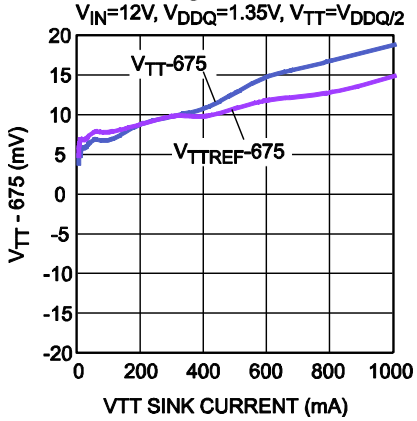
VTT Source Current Load Regulation

V_{IN}=12V, V_{DDQ}=1.35V, V_{TT}=V_{DDQ}/2



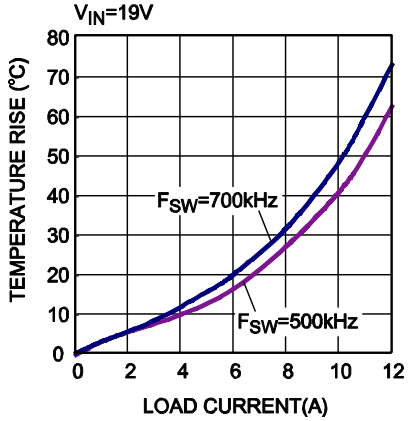
VTT Sink Current Load Regulation

V_{IN}=12V, V_{DDQ}=1.35V, V_{TT}=V_{DDQ}/2



Temperature Rise vs. Load Current

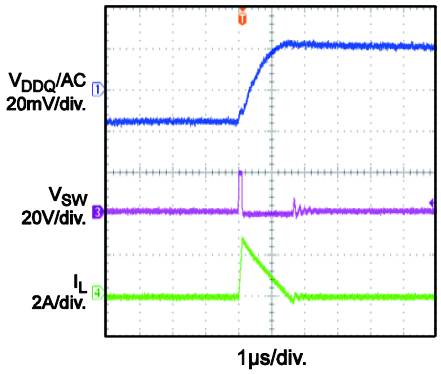
V_{IN}=19V



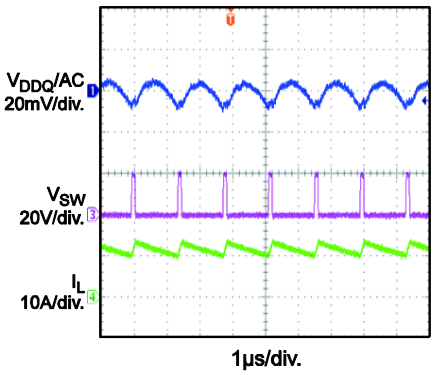
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 20 V, V_{DDQ} = 1.35 V, L = 0.68 µH/3.1 mΩ, F_{SW} = 700 kHz, unless otherwise noted.

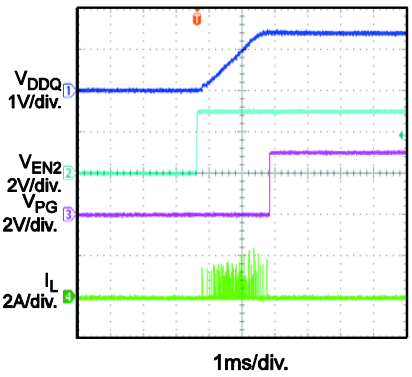
Output Voltage Ripple
I_{OUT} = 0A



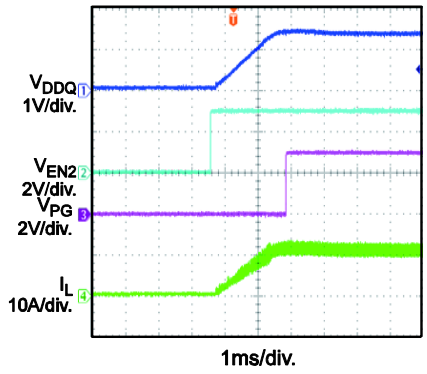
Output Voltage Ripple
I_{OUT} = 12A



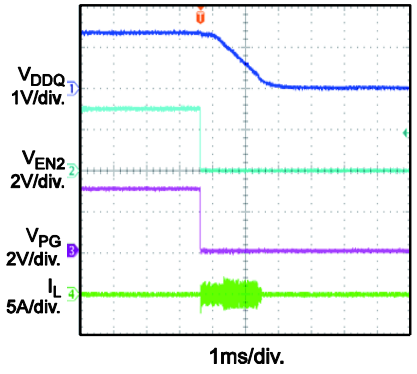
Start-Up through EN2
I_{OUT} = 0A



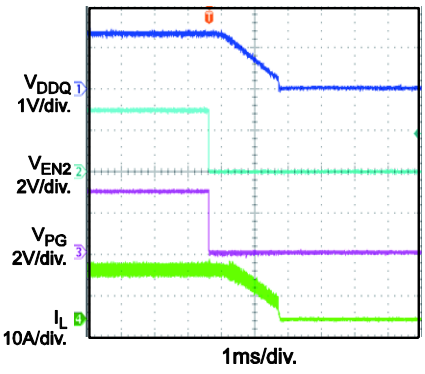
Start-Up through EN2
I_{OUT} = 12A



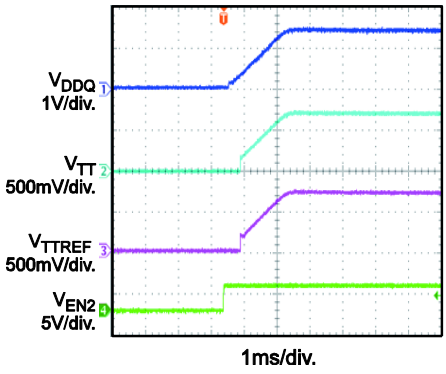
Shutdown through EN2
I_{OUT} = 0A



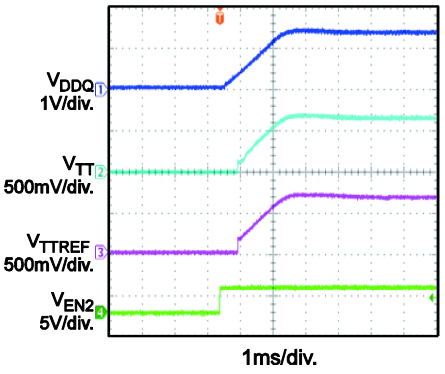
Shutdown through EN2
I_{OUT} = 12A



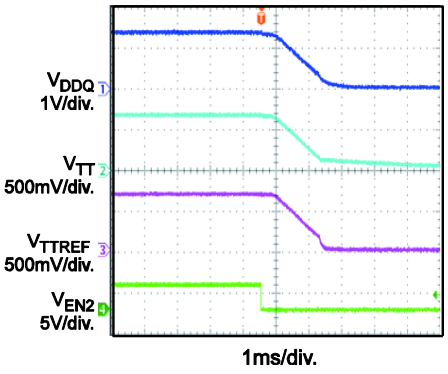
VTT Start-Up through EN2
I_{IVDDQ}=I_{VTT}=I_{VTTREF}=0A



VTT Start-Up through EN2
I_{IVDDQ}=12A, I_{VTT}=1A, I_{VTTREF}=0mA



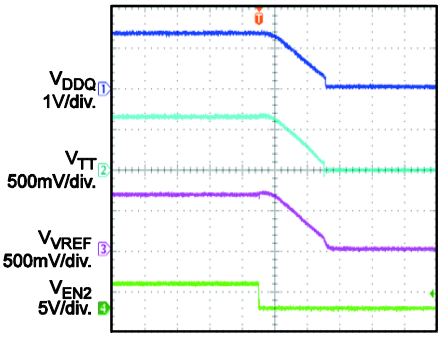
VTT Shutdown through EN2
I_{IVDDQ}=I_{VTT}=I_{VTTREF}=0A



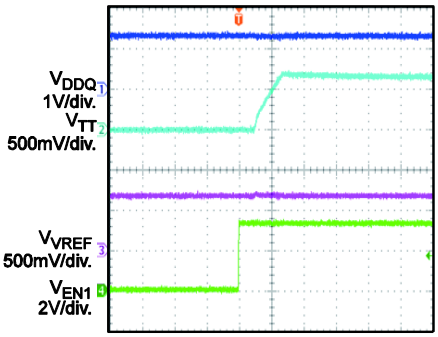
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 20 V, V_{DDQ} = 1.35 V, L = 0.68 µH/3.1 mΩ, F_{SW} = 700 kHz, unless otherwise noted.

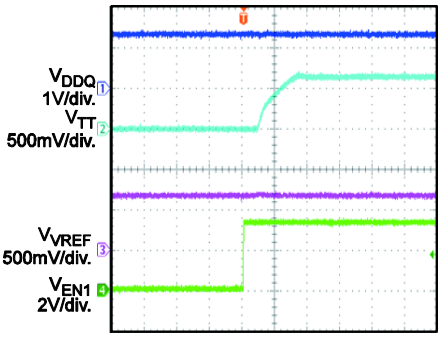
VTT Shutdown through EN2
I_{IVDDQ}=12A, I_{VTT}=1A, I_{VTTREF}=0mA



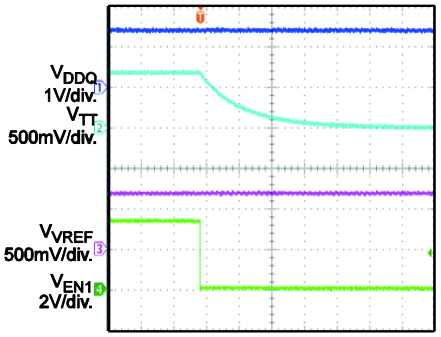
VTT Start-Up through EN1
I_{IVDDQ}=I_{VTT}=I_{VTTREF}=0A



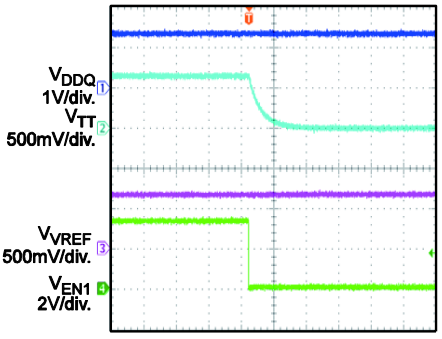
VTT Start-Up through EN1
I_{IVDDQ}=12A, I_{VTT}=1A, I_{VTTREF}=0mA



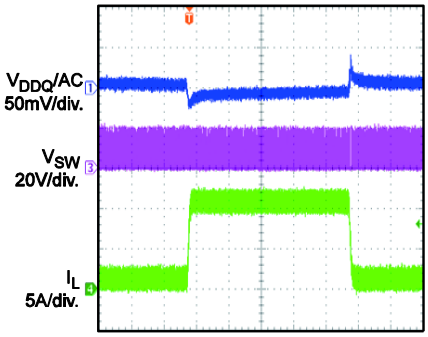
VTT Shutdown through EN1
I_{IVDDQ}=I_{VTT}=I_{VTTREF}=0A



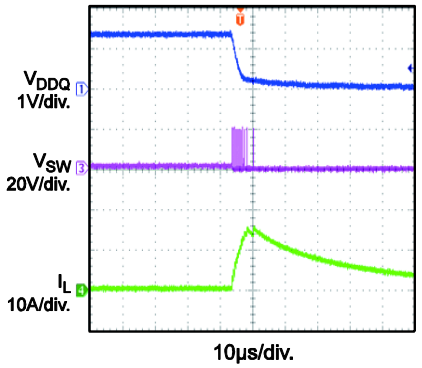
VTT Shutdown through EN1
I_{IVDDQ}=12A, I_{VTT}=1A, I_{VTTREF}=0mA



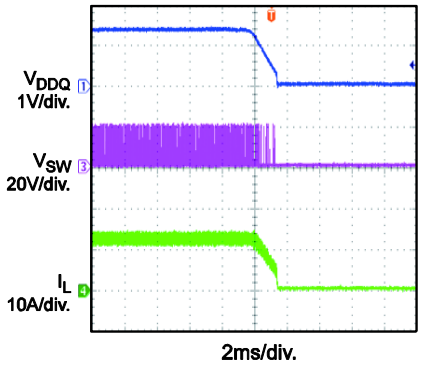
Transient
I_{OUT}=1.2-10.8A@1.6A/µs,
F_{SW}=700kHz,C_{OUT}=66µF



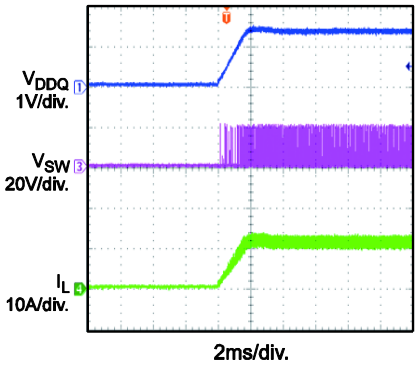
Short-Circuit Protection
I_{OUT} = 0A



Thermal Shutdown
I_{OUT} = 12A in Temp Chamber



Thermal Recovery
I_{OUT} = 12A in Temp Chamber



FUNCTIONAL BLOCK DIAGRAM

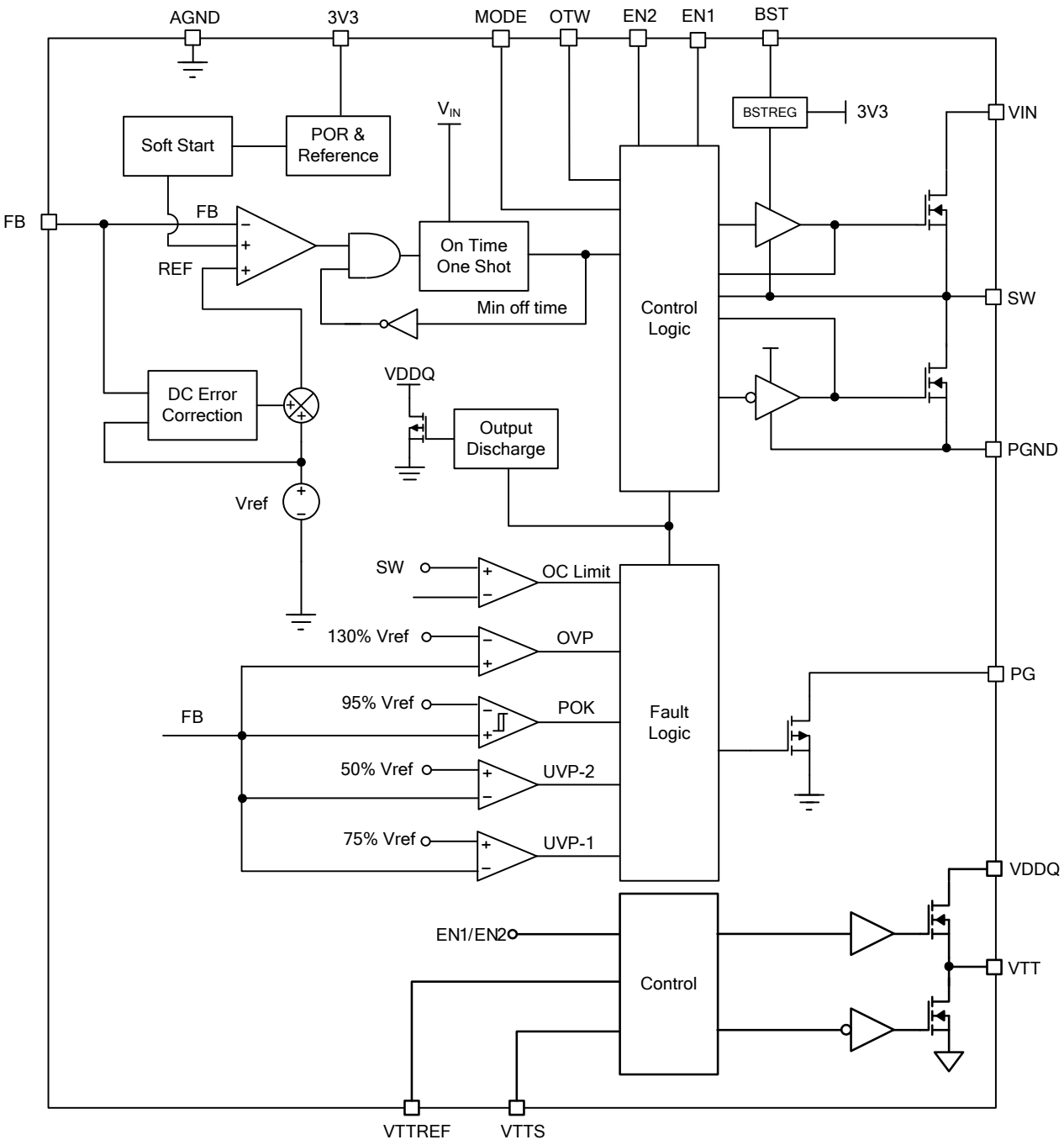


Figure 1—Functional block diagram

OPERATION

PWM Operation

The NB685A is a fully integrated, synchronous, rectified, step-down, switch-mode converter with +/-1 A LDO current. Constant-on-time (COT) control provides fast transient response and eases loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned on when the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}), which indicates insufficient output voltage. The on period is determined by both the output voltage and the input voltage to make the switching frequency fairy constant over the input voltage range.

After the on period elapses, the HS-FET is turned off or enters an off state. It is turned on again when V_{FB} drops below V_{REF}. By repeating operation this way, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) is turned on when the HS-FET is in its off state to minimize the conduction loss. A dead short occurs between the input and GND if both the HS-FET and the LS-FET are turned on at the same time (shoot-through). In order to avoid shoot-through, a dead time (DT) is generated internally between the HS-FET off and the LS-FET on period or the LS-FET off and the HS-FET on period.

Internal compensation is applied for COT control for stable operation even when ceramic capacitors are used as output capacitors. This internal compensation improves the jitter performance without affecting the line or load regulation.

Heavy-Load Operation

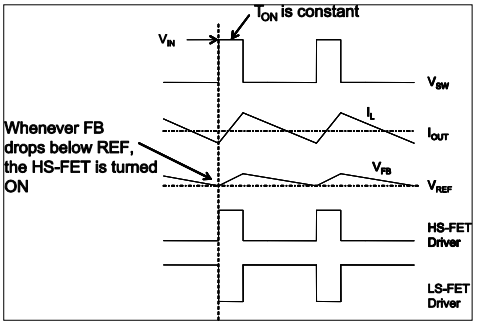


Figure 2—CCM operation

Continuous conduction mode (CCM) occurs when the output current is high, and the inductor current is always above zero amps (see Figure 2). When V_{FB} is below V_{REF}, the HS-FET is turned on for a fixed interval, which is determined by the one-shot on timer. See Equation 1. When the HS-FET is turned off, the LS-FET is turned on until the next period.

In CCM operation, the switching frequency is fairly constant (PWM mode).

Light-Load Operation

When the load decreases, the inductor current will decrease as well. Once the inductor current reaches zero, the part transitions from CCM to discontinuous conduction mode (DCM).

DCM operation is shown in Figure 3. When V_{FB} is below V_{REF}, the HS-FET is turned on for a fixed interval, which is determined by the one-shot on timer. See Equation 1. When the HS-FET is turned off, the LS-FET is turned on until the inductor current reaches zero. In DCM operation, the V_{FB} does not reach V_{REF} when the inductor current is approaching zero. The LS-FET driver turns into tri-state (high Z) when the inductor current reaches zero. A current modulator takes over the control of the LS-FET and limits the inductor current to less than -1 mA. Hence, the output capacitors discharge slowly to GND through the LS-FET. As a result, the efficiency during a light-load condition is improved greatly. The HS-FET does not turn on as frequently during a light-load condition as it does during a heavy-load condition (skip mode).

At a light-load or no-load condition, the output drops very slowly, and the NB685A reduces the switching frequency naturally, achieving high efficiency at light load.

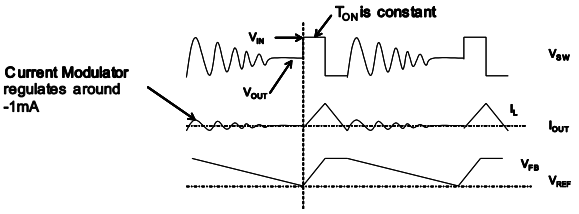


Figure 3—DCM operation

As the output current increases from the light-load condition, the time period within which the current modulator regulates becomes shorter. The HS-FET is turned on more frequently. Hence, the switching frequency increases accordingly. The output current reaches the critical level when the current modulator time is zero. The critical level of the output current is determined with Equation (1):

$$I_{OUT\_Critical} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_S \times V_{IN}} \quad (1)$$

The part enters PWM mode once the output current exceeds the critical level. After that, the switching frequency stays fairly constant over the output current range.

Jitter and FB Ramp

Jitter occurs in both PWM and skip mode when noise in the V_{FB} ripple propagates a delay to the HS-FET driver (see Figure 4 and Figure 5). Jitter affects system stability, with noise immunity proportional to the steepness of V_{FB}'s downward slope, so the jitter in DCM is usually larger than in CCM. However, V_{FB} ripple does not affect noise immunity directly.

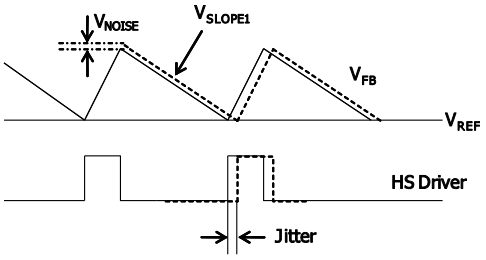


Figure 4—Jitter in PWM mode

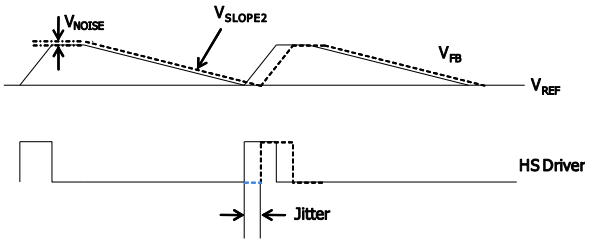


Figure 5—Jitter in skip mode

Operation—No External Ramp Compensation

The traditional constant-on-time control scheme is intrinsically unstable if the output capacitor's ESR is not large enough to act as an effective current-sense resistor.

Usually, ceramic capacitors cannot be used directly as output capacitors.

The NB685A has built-in internal ramp compensation to ensure the system is stable, even without the help of the output capacitor's ESR. Thus, the pure ceramic capacitor solution applies. The pure ceramic capacitor solution reduces significantly the output ripple, the total BOM cost, and the board area.

Figure 6 shows a typical output circuit in PWM mode without an external ramp circuit. Refer to the application information section for design steps without external compensation.

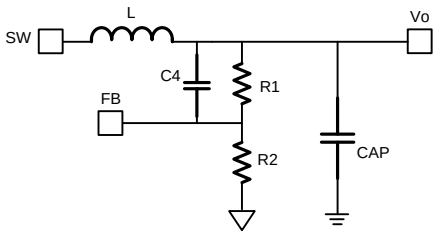


Figure 6—Simplified output circuit

When using a large capacitor (e.g., OSCON) on the output, add a ceramic capacitor with a value >10 µF in parallel to minimize the effect of ESL.

Operating with External Ramp Compensation

Usually, the NB685A is able to support ceramic output capacitors without external ramp. However, in some cases, the internal ramp may not be enough to stabilize the system, or there is too much jitter, which will require external ramp compensation. Refer to the application information section for design steps with external ramp compensation.

VTT and VTTREF

NB685A integrates high performance, low dropout linear regulators (VTT and VTTREF) to provide complete DDR3/DDR3L power solutions. The VTTREF has a 10 mA sink/source current capability and always tracks 1/2 of VDDQ with +/-1% accuracy using an on-chip divider. A minimum 0.22 µF ceramic capacitor must be connected close to the VTTREF terminal for stable operation.

VTT responds quickly to track VTTREF with +/-30 mV in all conditions. The current capability of the VTT regulator is up to 1 A for

both sink and source modes. A minimum 22 µF ceramic capacitor must be connected close to the VTT terminal. VTTS should be connected to the positive node of the remote VTT output capacitor as a separate trace from the high-current line to VTT.

Configuring the EN Control

The NB685A has two enable pins to control the on/off of the internal regulators. VDDQ, VTTREF, and VTT are turned on at S0 state (EN1 = EN2 = high). In S3 mode (EN1 = low, EN2 = high), VDDQ and VTTREF voltages remain on while VTT is turned off and left at a high-impedance state (high-Z). The VTT output floats and does not sink/source current in this state. In S4/S5 mode (EN1 = EN2 = low), all of the regulators remain off and discharge to GND through a soft shutdown. See EN1/EN2 logic details in Table1.

Table 1—EN1/EN2 control

State	EN1	EN2	VDDQ	VTTREF	VTT
S0	High	High	ON	ON	ON
S3	Low	High	ON	ON	OFF(High-Z)
S4/S5	Low	Low	OFF	OFF	OFF
Others	High	Low	OFF	OFF	OFF

Ultrasonic Mode (USM)

Ultrasonic mode (USM) is designed to keep the switching frequency above an audible frequency area during light-load or no-load conditions. Once the part detects that both the HS-FET and the LS-FET are off (for about 32 µs), it forces PWM to initiate Ton, so the switching frequency is out of audio range. To avoid Vout becoming too high, NB685A reduces Ton to control the Vout. If the part's FB is still too high after reducing Ton to the minimum value, the output discharge function is activated and keeps the Vout within a reasonable range. USM is selected by MODE.

MODE Selection

NB685A implements MODE for multiple applications for USM and switching frequency selection. The USM and the switching frequency can be selected by a different resistor on the 3V3 logic mode pin. There are four modes that can be selected for normal application with external resistors. It is recommended to use a 1% accuracy resistor (see Table 2).

Table 2—Mode selection

State	USM	Fs	Resistor to GND
M1	No	700 KHz	0
M2	Yes	700 KHz	90 K
M3	No	500 KHz	150 K
M4	Yes	500 KHz	>230 K or float

VDDQ Power Good (PG)

The NB685A has power good (PG) output used to indicate whether the output voltage of the VDDQ regulator is ready. PG is the open drain of a MOSFET. It should be connected to V_{CC} or another voltage source through a resistor (e.g. 100 k). After the input voltage is applied, the MOSFET is turned on, so PG is pulled to GND before SS is ready. After the FB voltage reaches 95 percent of the REF voltage, PG is pulled high (after a delay time within 10 µs). When the FB voltage drops to 90 percent of the REF voltage, PG is pulled low.

Soft Start (SS)

The NB685A employs a soft-start (SS) mechanism to ensure smooth output during power-up. When EN becomes high, the internal reference voltage ramps up gradually; hence, the output voltage ramps up smoothly as well. Once the reference voltage reaches the target value, the soft start finishes, and the part enters steady-state operation.

The start-up sequence is shown in Figure 7.

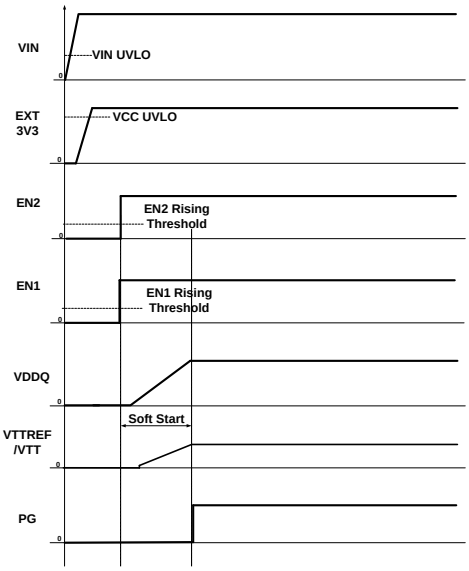


Figure 7—Start-up power sequence

If the output is pre-biased to a certain voltage during start-up, the IC disables the switching of both the high-side and the low-side switches until the voltage on the internal reference exceeds the sensed output voltage at the FB node.

Soft Shutdown

The NB685A employs a soft-shutdown mechanism for DDR to ensure VTTREF and VTT follow exactly half of the VDDQ. When EN2 is low, the internal reference then ramps down gradually, so the output voltage falls linearly. Figure 8 shows the soft-shutdown sequence.

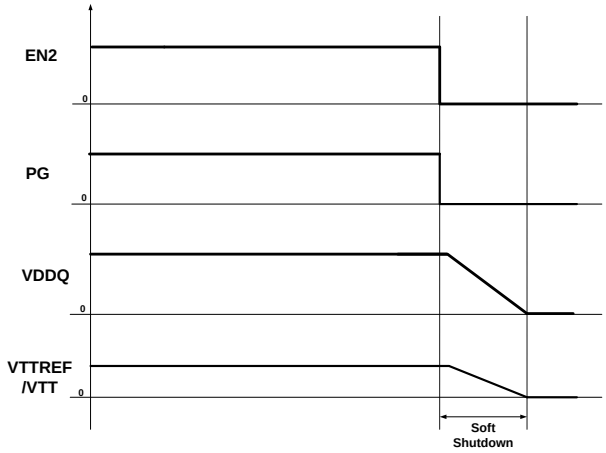


Figure 8—Soft-shutdown sequence

VDDQ Over-Current Limit

NB685A has cycle-by-cycle over-current limiting control. The current-limit circuit employs a "valley" current-sensing algorithm. The part uses the Rds(on) of the LS-FET as a current-sensing element. If the magnitude of the current-sense signal is above the current-limit threshold, the PWM is not allowed to initiate a new cycle, even if FB is lower than the REF. Figure 9 shows the detailed operation of the valley current limit.

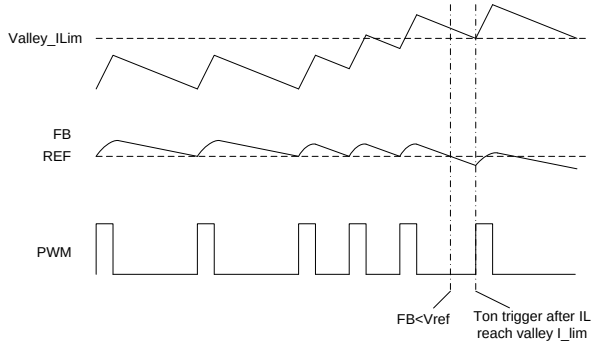


Figure 9—Valley current-limit control

Since the comparison is done during the LS-FET on state, the OC trip level sets the valley level of the inductor current. The maximum load current at the over-current threshold (Ioc) can be calculated using Equation (2):

$$I_{OC} = I\_limit + \frac{\Delta I_{inductor}}{2} \quad (2)$$

The OCL limits the inductor current and does not latch off. In an over-current condition, the current to the load exceeds the current to the output capacitor; thus, the output voltage tends to fall off. Eventually, it ends up crossing the under-voltage protection (UVP) threshold and latches off. Fault latching can be re-set by EN going low or the power cycling of VIN.

VTT/VTTREF Over-Current Protection

The VTT LDO has an internally non latch, fixed current limit of 1.5 A for both sink and source operation. Once the current limit is reached, it adjusts the gate of the sink/source MOSFET to limit the current. Also, VTTREF has an internal non latch 15 mA current limit.

VDDQ Over/Under-Voltage Protection

NB685A monitors a resistor divided feedback voltage to detect over and under voltage. When the feedback voltage becomes higher than 130 percent of the target voltage, the OVP comparator output goes high, and the circuit latches as the HS-FET turns off, and the LS-FET turns on, acting as an -2 A current source.

To protect the part from damage, there is an absolute 3.6 V OVP on VOUT. Once Vout reaches this value, it latches off as well. The LS-FET behaves the same as at 130 percent OVP.

When the feedback voltage drops lower than 75 percent of the Vref but remains higher than 50 percent of the Vref, the UVP-1 comparator output goes high, and the part latches if the FB voltage stays in this range for about 30 µs (latching the HS-FET off and the LS-FET on). The LS-FET remains on until the inductor current hits zero. During this period, the valley current limit helps control the inductor current.

When the feedback voltage drops below 50 percent of the Vref, the UVP-2 comparator output goes high and the part latches off directly after the comparator and logic delay (latching the HS-FET off and the LS-FET on); the LS-FET remains

on until the inductor current hits zero. Fault latching can be re-set by EN going low or the power cycling of VIN.

UVLO Protection

The NB685A has two under-voltage lockout protections: a 3 V VCC UVLO and a 4.2 V Vin UVLO. The part starts up only when both the VCC and Vin exceed their own UVLO. The part shuts down when either the VCC voltage is lower than the UVLO falling threshold voltage (2.8 V, typically), or the VIN is lower than the 3.9 V Vin falling threshold. Both UVLO protections are non-latch off.

If an application requires a higher under-voltage lockout (UVLO), use EN2 to adjust the input voltage UVLO by using two external resistors (see Figure 10).

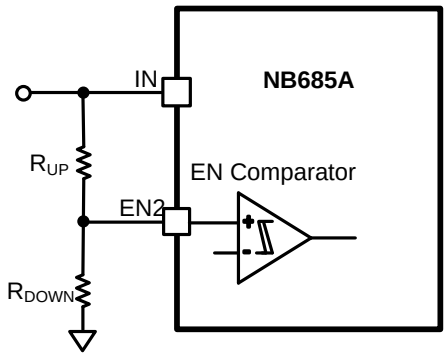


Figure 10—Adjustable UVLO

Over-Temperature Warning (OTW)

An over-temperature warning (OTW) status pin is added on the NB685A acting as a pre-over temperature indicator. When the IC detects the part is close to its OT threshold, OTW pulls low and remains low for at least 10 ms. OTW pulls high again when the device temperature has cooled below the temperature hysteresis. OTW does not trigger any protection.

Thermal Shutdown

Thermal shutdown is employed in the NB685A. The junction temperature of the IC is monitored internally. If the junction temperature exceeds the threshold value (145ºC, typically), the converter shuts off. This is a non-latch protection. There is about 25ºC hysteresis. Once the junction temperature drops to about 120ºC, it initiates a SS.

Output Discharge

NB685A discharges all the outputs including VDDQ, VTTREF, and VTT when the controller is turned off by the protection functions UVP, OCP, OVP, UVLO, and thermal shutdown. The discharge resistor on VDDQ is 3 Ω, typically. Note that the output discharge is not active during the soft shutdown.

APPLICATION INFORMATION

Setting the Output Voltage—No External Ramp

NB685A does not need ramp compensation for applications when POSCAP or ceramic capacitors are set as output capacitors (when Vin is over 6 V), so the external compensation is not needed. The output voltage is then set by feedback resistors R1 and R2 (see Figure 11).

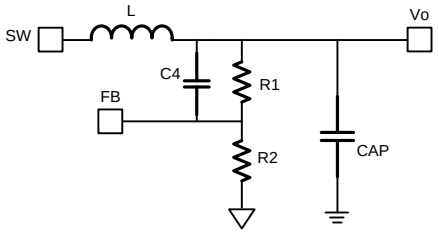


Figure11—Simplified circuit without external ramp

First, choose a value for R2. R2 should be chosen reasonably. A small value for R2 leads to considerable quiescent current loss while too large a value for R2 makes the FB noise sensitive. It is recommended to choose a value within 5 kΩ-50 kΩ for R2. Use a comparatively larger value for R2 when Vo is low and a smaller value for R2 when Vo is high. Considering the output ripple, R1 is determined with Equation (3):

$$R_1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \cdot R_2 \quad (3)$$

C4 acts as a feed-forward capacitor to improve the transient and can be set in the range of 0 pF-1000 pF. A larger value for C4 leads to better transient, but it is more noise sensitive. Reserve room for a noise filter resistor (R9) as shown in Figure 12. The value is calculated with Equation (5).

Setting the Output Voltage—with External Compensation

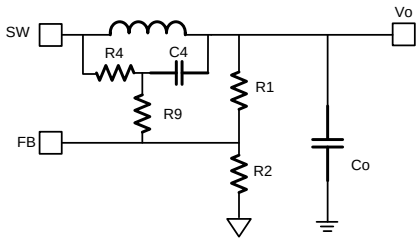


Figure 12—Simplified circuit with external ramp

If the system is not stable enough or there is too much jitter when a ceramic capacitor is used on the output (i.e., with a ceramic Cout and Vin is 5 V or lower), an external voltage ramp should be added to FB through resistor R4 and capacitor C4. Since there is already internal ramp added in the system, a 1 M (R4), 220 pF (C4) ramp should suffice.

Besides the R1 & R2 divider, the output voltage is influenced by R4 (see Figure 12). R2 should be chosen reasonably. A small value for R2 leads to considerable quiescent current loss while too large a value for R2 makes the FB noise sensitive. It is recommended to choose a value within 5 kΩ-50 kΩ for R2. Use a comparatively larger value for R2 when Vo is low and a smaller value for R2 when Vo is high. The value of R1 then is determined with Equation (4):

$$R_1 = \frac{1}{\frac{V_{REF}}{V_{OUT} - V_{REF}} - \frac{R2}{R4}} \cdot R_2 \quad (4)$$

Usually, R9 is set using Equation (5) to get a pole for better noise immunity:

$$R_9 = \frac{1}{2\pi \times C_4 \times 2F_{SW}} \quad (5)$$

It is suggested to set R9 in the range of 100 Ω to 1 kΩ to reduce its influence on the ramp.

Input Capacitor

The input current to the step-down converter is discontinuous, and therefore requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Ceramic capacitors are recommended for best performance and should be placed as close to VIN as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable with temperature fluctuations.

The capacitors must have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated with Equation (6) and Equation (7):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (6)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (7)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an input capacitor that meets the specification.

The input voltage ripple can be estimated with Equation (8) and Equation (9):

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

The worst-case condition occur at $V_{IN} = 2V_{OUT}$, where:

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (9)$$

Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated using Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (10)$$

When using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is caused mainly by the capacitance. For simplification, the output voltage ripple can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (11)$$

The output voltage ripple caused by ESR is very small. Therefore, an external ramp is needed to stabilize the system. The external ramp can be generated through resistor R4 and capacitor C4.

When using POSCAP capacitors, the ESR dominates the impedance at the switching frequency. The ramp voltage generated from the ESR dominates the output ripple. The output ripple can be approximated with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (12)$$

The maximum output capacitor limitation should be considered in design application. NB685A has an around 1.6 ms soft-start time period. If the output capacitor value is too high, the output voltage cannot reach the design value during the soft-start time, causing it to fail to regulate. The maximum output capacitor value (C_{o_max}) can be limited approximately with Equation (13):

$$C_{O\_MAX} = (I_{LIM\_AVG} - I_{OUT}) \times T_{ss} / V_{OUT} \quad (13)$$

Where, I_{LIM_AVG} is the average start-up current during the soft-start period (it can be equivalent to the current limit), and T_{ss} is the soft-start time.

Inductor

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage. A larger value inductor results in less ripple current, resulting in lower output ripple voltage. However, a larger value inductor has a larger physical footprint, a higher series resistance, and/or a lower saturation current. A good rule for determining the inductance value is to design the peak-to-peak ripple current in the inductor in the range of 30 percent to 50 percent of the maximum output current, and the peak inductor current below the maximum switch current limit. The inductance value can be calculated with Equation (14):

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_{L}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (14)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current (including short current), so it is suggested to choose Isat >13 A.

RECOMMENDED LAYOUT

PCB Layout Guidelines

Efficient PCB layout is critical for optimal performance of the IC. For best results, refer to Figure 13 and follow the guidelines below. For more information, refer to AN087.

1. Keep the VDDQ trace width >100 mil to avoid a voltage drop at the input of the VTTLDO.
2. Place the high-current paths (GND, IN, and SW) very close to the device with short, direct, and wide traces. A thick PGND trace under the IC should be the number one priority.
3. Place the input capacitors as close to IN and GND as possible on the same layer as the IC.
4. Place the decoupling capacitor as close to VCC and GND as possible. Keep the switching node (SW) short and away from the feedback network.
5. Place the external feedback resistors next to FB. Make sure that there is no via on the FB trace.
6. Keep the BST voltage path (BST, C3, and SW) as short as possible.
7. Keep the IN and GND pads connected with a large copper plane to achieve better thermal performance. Add several vias with 10 mil drill/18mil copper width close to the IN and GND pads to help thermal dissipation.
8. A 4-layer layout is strongly recommended to achieve better thermal performance.

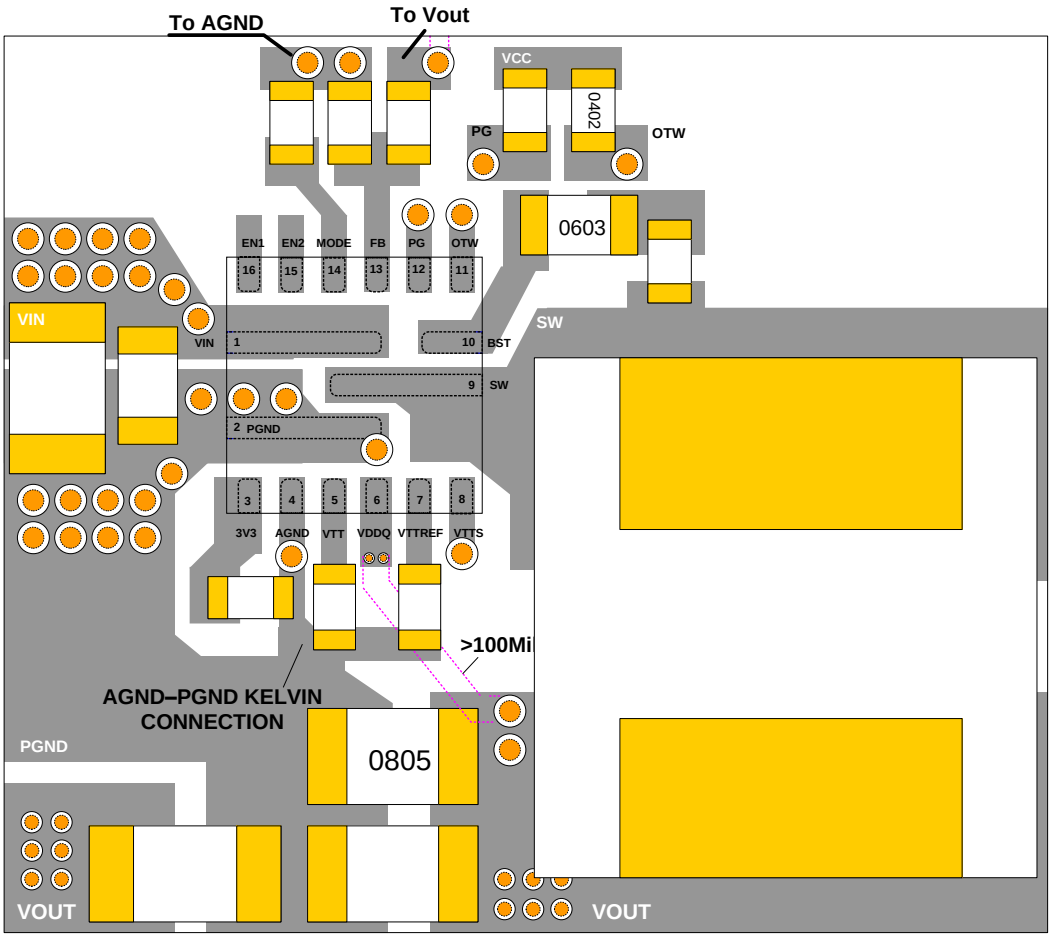


Figure 13—Recommended PCB layout

Recommend Design Example

For applications that need current over 10 A, it is recommended to apply a 500 KHz fsw part for better thermal performance and efficiency (see Table 3.1). Otherwise, 700 kHz fsw operation will make the system more compact with faster transient (see Table 3.2).

There is a resistor from an external 3.3 V to 3V3 acting as a ripple noise filter of the 3.3 V power supply. It is recommended to have a resistor value from 0 Ω-5.1 Ω depending on the noise level. A 0402 sized resistor will suffice if the 3.3 V voltage rises up with SS > 100 µs. Otherwise, a larger sized resistor (e.g., 0603/0805) is needed.

For application when Vin is 5 V or lower, it is recommended to apply the SCH shown in Figure 14 with a proper external ramp.

NB685A also supports non DDR application with very compact external components (see Figure 15).

Some design examples are provided below when ceramic capacitors are applied:

Table 3.1—Design example for 500 kHz fsw

V_{OUT} (V)	Cout (F)	L (µH)	R_{Mode} (Ω)	C4 (pF)	R1 (kΩ)	R2 (kΩ)
1.0	22 µ x 4	1.0	150 K	220	13.3	20
1.2	22 µ x 4	1.0	150 K	220	20	20
1.35	22 µ x 4	1.0	150 K	220	28	22.1
1.5	22 µ x 4	1.2	150 K	220	30.1	20
1.8	22 µ x 4	1.5	150 K	220	40.2	20

Table 3.2—Design example for 700 KHz fsw

V_{OUT} (V)	Cout (F)	L (µH)	R_{Mode} (Ω)	C4 (pF)	R1 (kΩ)	R2 (kΩ)
1	22 µ x 3	0.68	0	220	13.3	20
1.2	22 µ x 3	0.68	0	220	20	20
1.35	22 µ x 3	0.68	0	220	28	22.1
1.5	22 µ x 3	0.68	0	220	30.1	20
1.8	22 µ x 3	0.68	0	220	40.2	20

Additional Design Examples with Higher Vout

NB685A supports designs that need Vout in the range of 3.3 V to 5.5 V. Figure 17 shows a SCH with a 5 V Vout with proper external settings. Please pay attention to the red components, and please note that USM is not allowed for this application.

TYPICAL APPLICATION

DDR Application for Vin >6 V

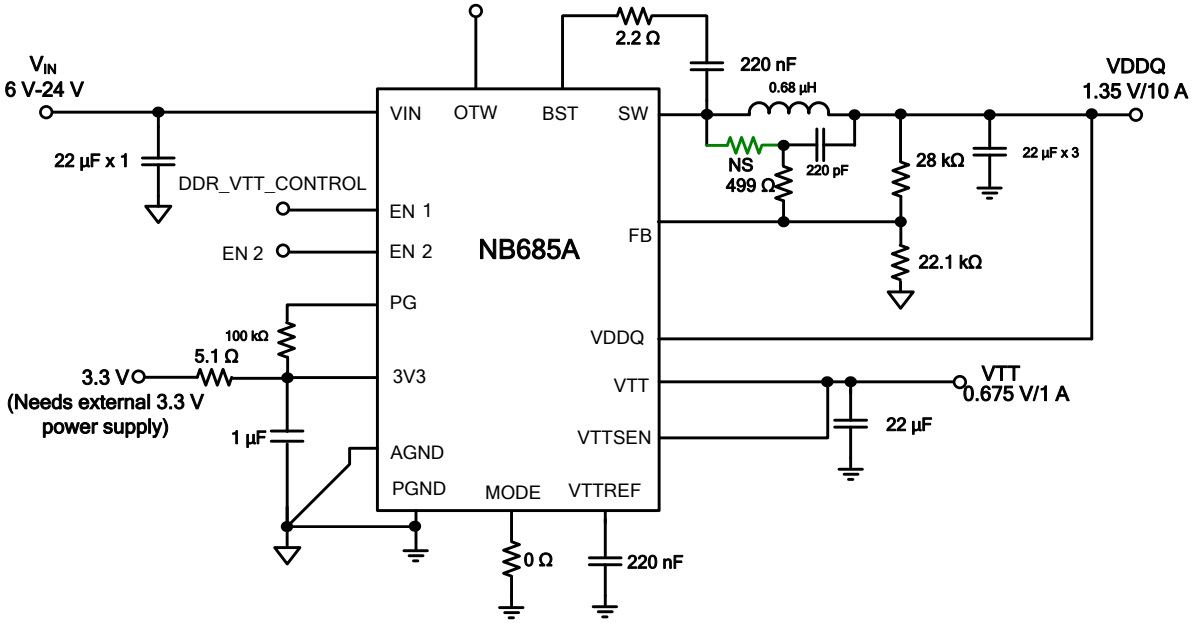


Figure 14—Typical DDR application circuit, V_{IN} = 6 V-24 V, V_{OUT} = 1.35 V, I_{OUT} = 10 A, with VTT fs = 700 kHz.

DDR Application Cover 5 V Vin Application.

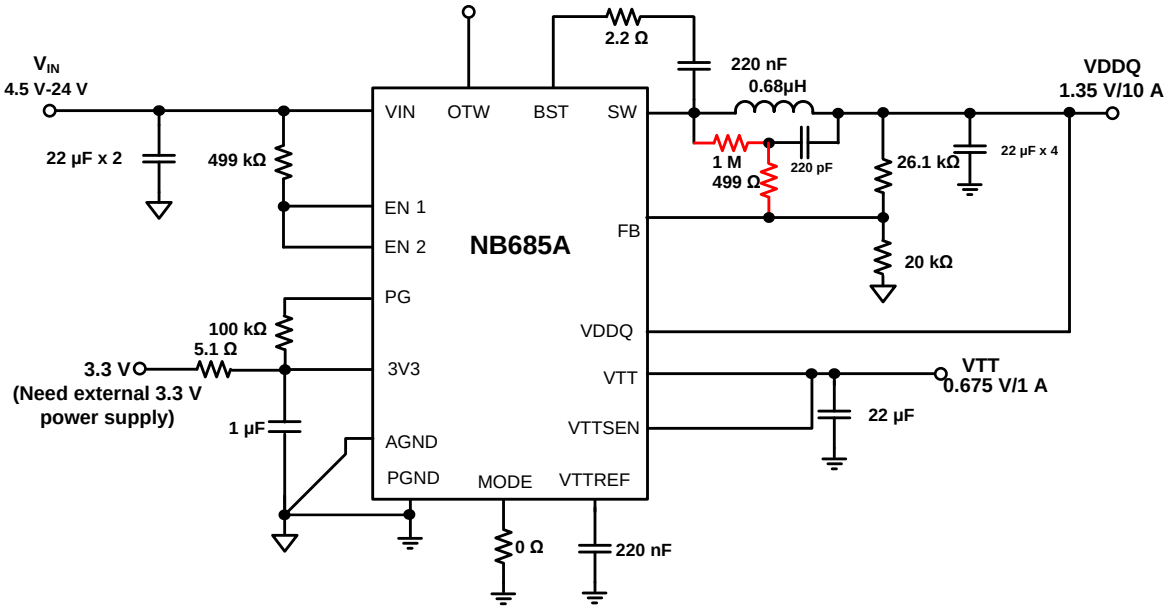


Figure 15—Typical DDR application circuit, V_{IN} = 4.5 V-24 V, V_{OUT} = 1.35 V, I_{OUT} = 10 A, with VTT fs = 700 kHz.

Non DDR Application

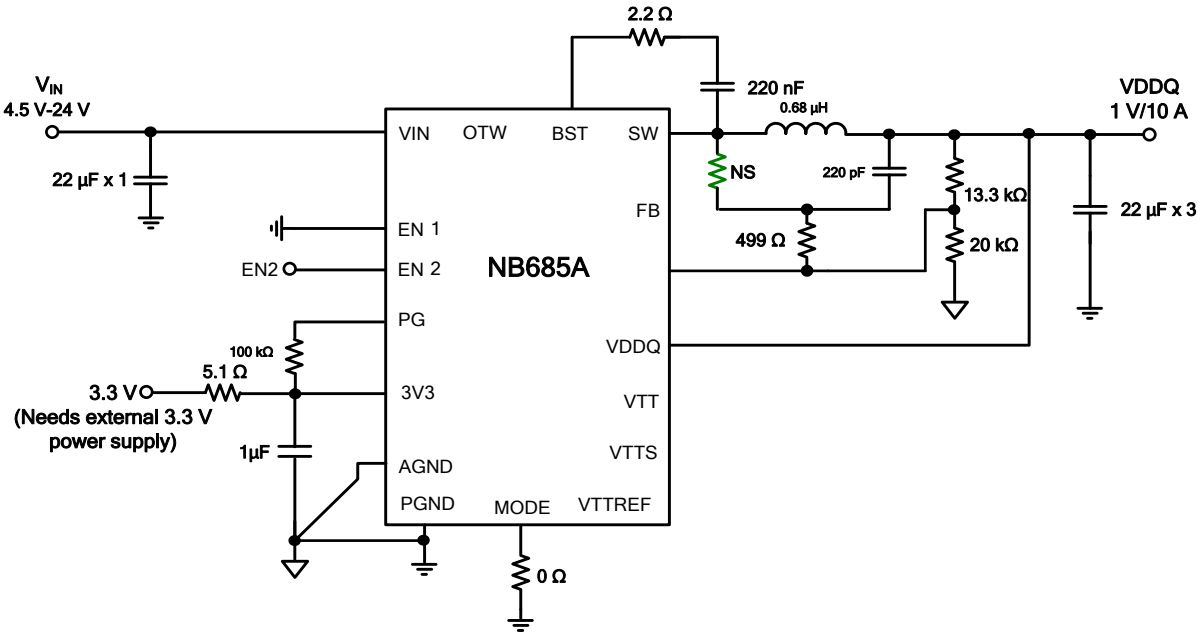
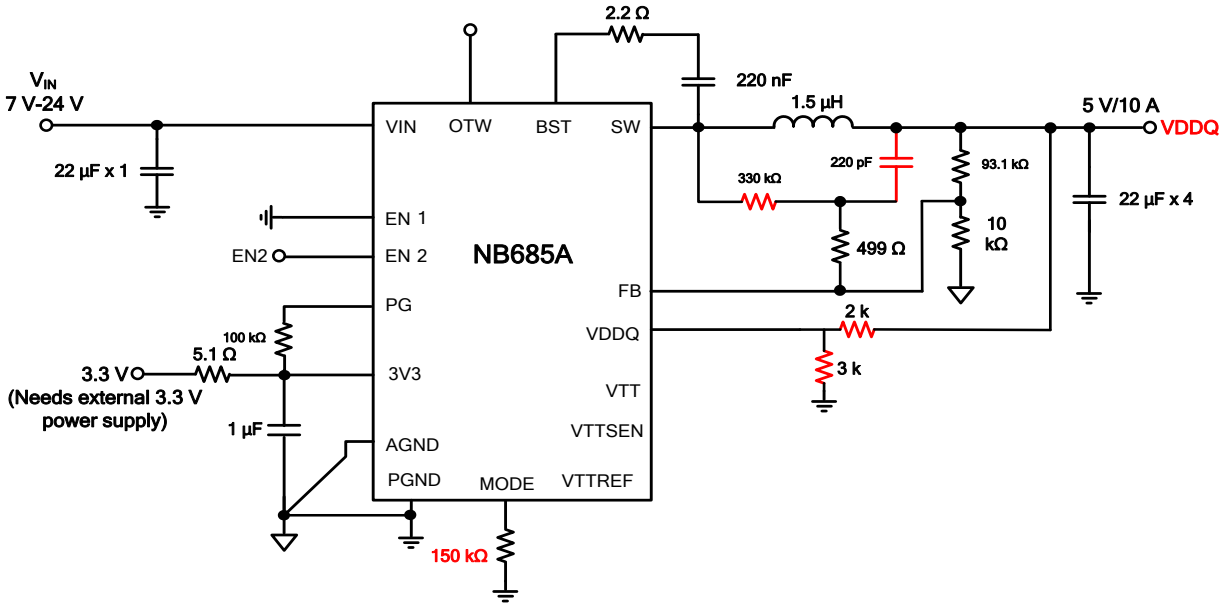


Figure 16 — Normal single buck application circuit, V_{IN} = 4.5 V-24 V, V_{OUT} = 1 V, I_{OUT} = 10 A, without VTT fs = 700 kHz.

SPECIAL APPLICATION—WITH 3.3 V < VOUT < 5.5 V



NOTE 1: Ultrasonic mode is not effective if applied in this SCH.

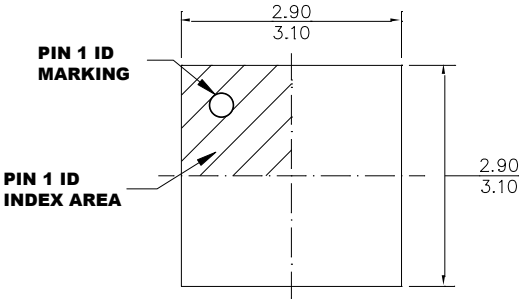
NOTE 2: The maximum load is 10 A in this application. Fs is set with a 500 kHz mode but is actually 700 kHz.

NOTES 3: It is recommended to avoid VDDQ voltage over 3.3 V by using the external resistors setting.

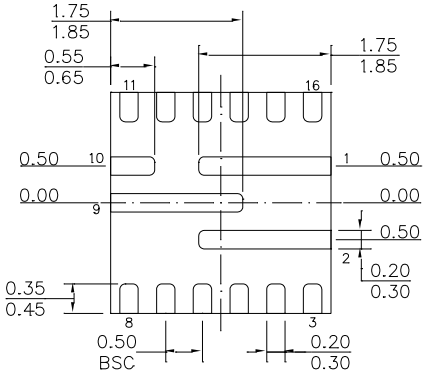
Figure 17 — Special application circuit, V_{IN} = 7 V-24 V, V_{OUT} = 5 V, I_{OUT} = 10 A, fs = 700 kHz.

PACKAGE INFORMATION

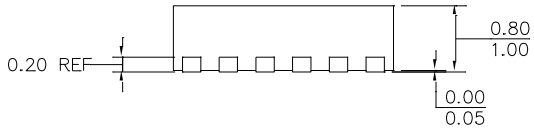
QFN-16 (3mm x 3mm)



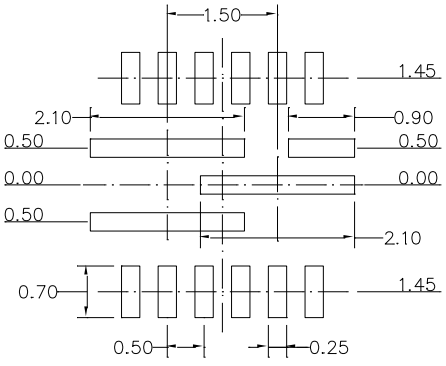
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.