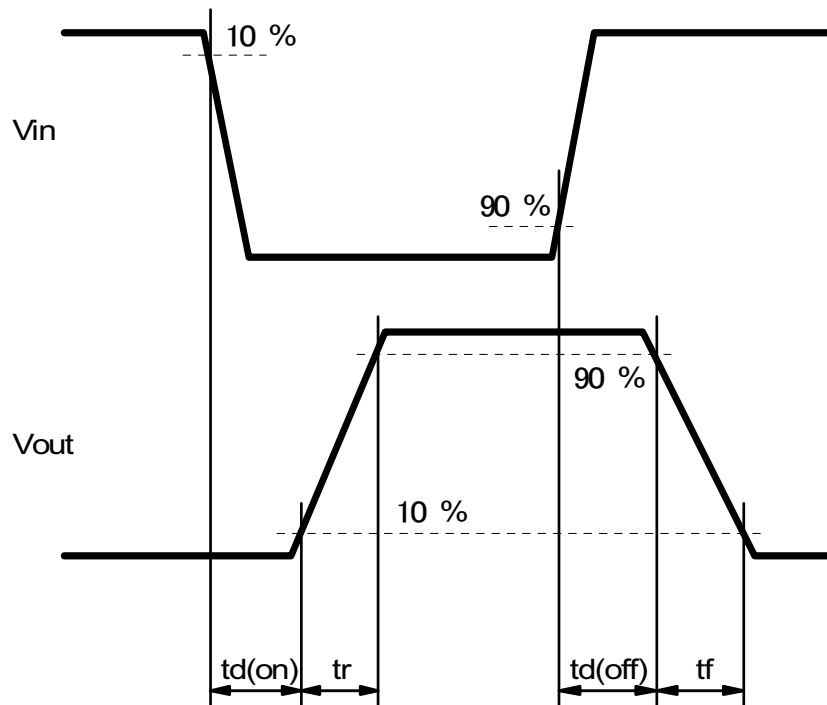
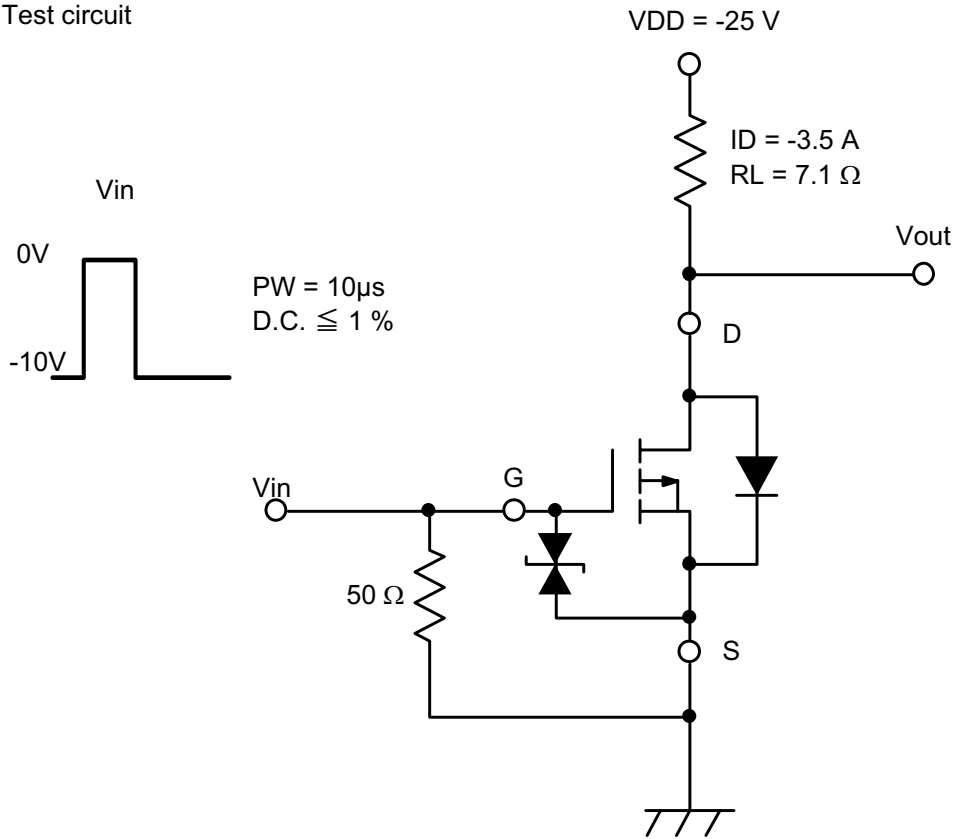


Product Specification Type Number : M T M 9 8 1 4 0 0 B B F *1				Prepared by S.Miyata	Checked by M.Fujisawa	Applied by H.Shidooka	Established by K.Kemichi
Type	Silicon Field Effect Transistors						
Application	Switching						
Structure	P-Channel MOS Type						
Outline	SO8-F1-B				Marking		BA
Absolute Maximum Ratings	VDSS (V)	VGSS (V)	ID (A)	IDp (A)	PD ^{*2} (W)	Tch (°C)	Tstg (°C)
	-40	±20	-7	-28	2	150	-55 to +150
Electrical characteristics (Ta = 25 °C ±3 °C)							
Item	Symbol	Measuring condition	Limit			Unit	
			min.	typ.	max.		
Drain-Source Voltage	VDSS	ID = -1 mA, VGS = 0 V	-40			V	
Drain-Source Cutoff Current	IDSS	VDS = -40 V, VGS = 0 V			-10	μA	
Gate-Source Cutoff Current	IGSS	VGS = ±16 V, VDS = 0 V			±10	μA	
Gate Threshold Voltage	Vth	ID = -1.0 mA, VDS = -10.0 V	-1.0		-2.5	V	
Drain Resistance (ON)	^{*3} RDS(ON)	ID = -7 A, VGS = -10 V		19	25	mΩ	
Drain Resistance (ON)	^{*3} RDS(ON)	ID = -3.5A, VGS = -4.5V		28	45	mΩ	
Forward Transfer Admittance	^{*3} Yfs	ID = -7 A, VDS = -10 V	10			S	
Small-Signal Short-Circuit Input Capacitance	Ciss	VDS = -10 V, VGS = 0 V, f = 1MHz		2700		pF	
Small-Signal Short-Circuit Output Capacitance	Coss	VDS = -10V, VGS = 0V, f = 1MHz		190		pF	
Small-Signal Reverse Transfer Capacitance	Crss	VDS = -10 V, VGS = 0 V, f = 1 MHz		175		pF	
Turn-on Delay Time	^{*3,4} td(on)	VDD = -25 V, VGS = 0 to -10 V, ID = -3.5 A		18		ns	
Rise Time	^{*3,4} tr	VDD = -25 V, VGS = 0 to -10 V, ID = -3.5 A		15		ns	
Turn-off Delay Time	^{*3,4} td(off)	VDD = -25 V, VGS = -10 to 0 V, ID = -3.5 A		230		ns	
Fall Time	^{*3,4} tf	VDD = -25 V, VGS = -10 to 0 V, ID = -3.5 A		70		ns	
<p>Note: Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.</p> <p>*1 Packing Embossed type (thermo-compression sealing)</p> <p>*2 Measuring on ceramic board at 50×50×1.0mm.</p> <p>*3 Pulse test</p> <p>*4 See test circuit</p> <p style="text-align: center;">Internally connected circuit</p> <div style="display: flex; align-items: flex-start;"> <div style="margin-right: 20px;"> <p>1.Source</p> <p>2.Source</p> <p>3.Source</p> <p>4.Gate</p> <p>5.Drain</p> <p>6.Drain</p> <p>7.Drain</p> <p>8.Drain</p> </div> </div>							
2008.01.31							
Established	Revised						

Product Specification
 Type Number : M T M 9 8 1 4 0 0 B B F
 *1

Test circuit



2008.01.31

Established

Revised

PACKAGE STANDARDS

Package Code

SO8-F1-B

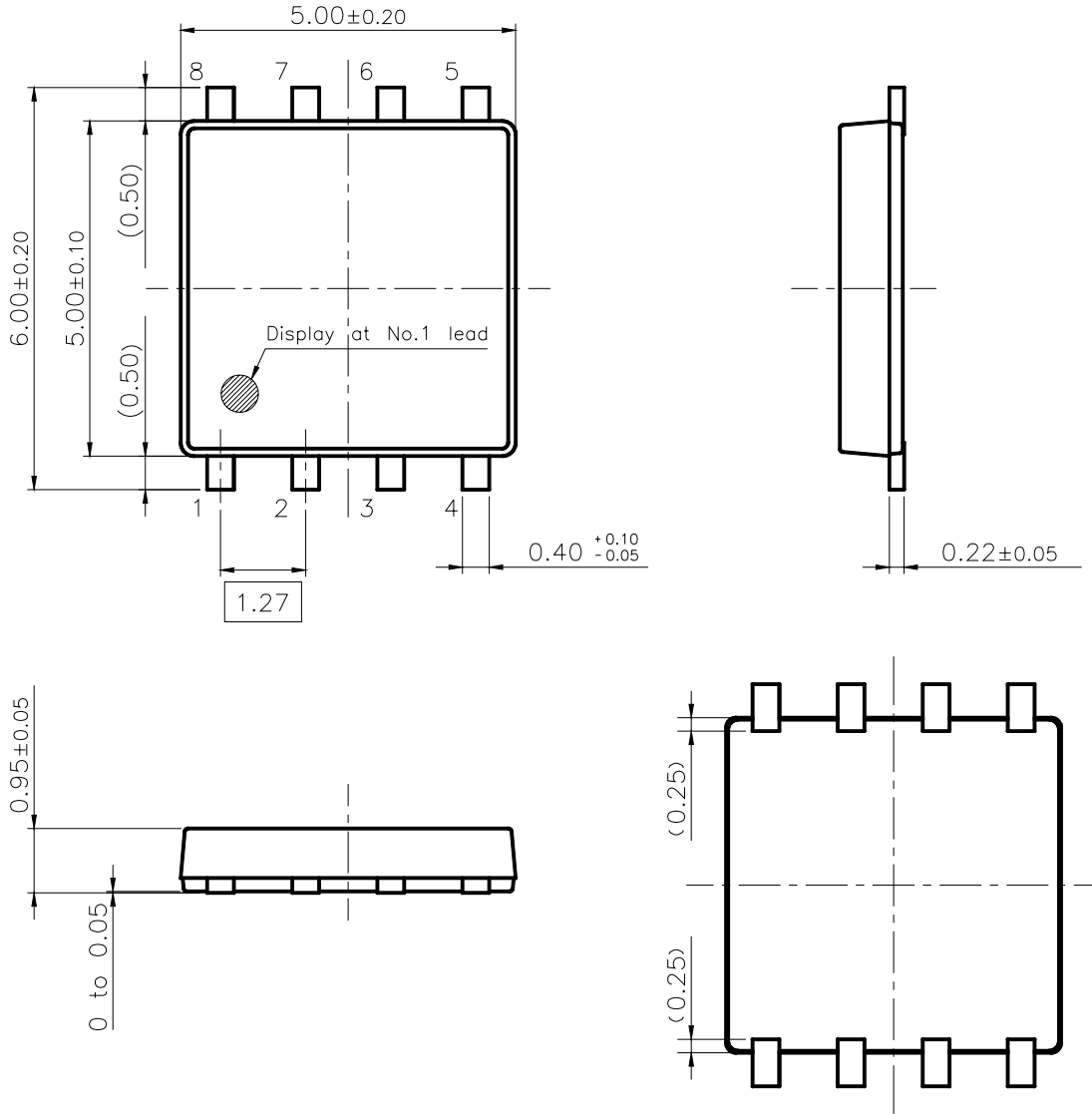
Semiconductor Company
Panasonic Corporation

Established by	Applied by	Checked by	Prepared by
H.Shidooka	H.Yoshida	M.Okajima	M.Kametaka

	PACKAGE STANDARDS SO8-F1-B		
		Total Pages	Page
		3	2

1. Outline Drawing

Unit:mm



Body Material	: Br / Sb Free Epoxy Resin
Lead Material	: Cu Alloy
Lead Finish Method	: SnBi Plating



	PACKAGE STANDARDS SO8-F1-B		
		Total Pages	Page
	3	3	

3. Mark Drawing

