1/2-Inch VGA (with Freeze-Frame) CMOS Image Sensor

MT9V403

For the latest data sheet revision, please refer to Micron's Web site: www.micron.com/imaging

Features

- Output: 10-bit digital through a single port
- Interface Mode: Master/Snapshot/Slave (with simultaneous or sequential exposure/readout)
- Shutter Efficiency: 98.5%
- Shutter Exposure Time:
  - Master Mode or Snapshot Mode: 2 rows to 256 frames (20µs to 1.3 sec with 66 MHz clock)
- Slave Mode: user controlled
- Gain: 1x–18x (step size = 1) or 0.5x–9x (step size = 0.5)
- Control Interface: Two-wire serial interface
- Timing and Control:
  On-chip:
  - ADC controls, output multiplexing, ADC calibration via two-wire serial interface, exposure time, read/write ADC calibration coefficients, window size and location, gain, biases, master vs. snapshot vs. slave, simultaneous vs. continuous exposure/readout, progressive vs. interlace, ADC reference, vertical and horizontal blanking.

  Off-chip:
  - Exposure trigger (snapshot mode), exposure and readout timing (slave mode)

Description

The Micron® Imaging MT9V403 VGA-based CMOS active-pixel sensor has a 1/2-inch optical format and delivers superb resolution at a turbocharged 200 fps, making it the perfect solution for machine vision assembly lines, airbag deployment, golf swing analysis, and special effects in movies. The freeze-frame shutter allows the signal charges of all pixels to be integrated in parallel—all pixels start integrating simultaneously and stop integrating simultaneously.

The charges are then sampled into pixel analog memories (one memory per pixel) and consequently, row by row, are digitized and read out-of-chip. The sensor works in master, snapshot, or slave mode. In master mode it generates the readout timing on-chip.

Table 1: Key Performance Parameters

Parameter	Typical Value
Optical format	1/2-inch (4:3)
Active imager size	6.61mm(H) x 4.97mm(V)
Active pixels	659H x 494V
Pixel size	9.9µm x 9.9µm
Color filter array	RGB Bayer pattern
Shutter type	TrueSNAP™ freeze-frame electronic
Maximum data rate/ master clock	66 MB/s (master clock 66 MHz)
Frame rate	0-200 fps, progressive scan
ADC resolution	10-bit, on-chip
Responsivity	2.0 V/lux-sec (with source illumination at 550nm)
Dynamic range	60dB
SNR	45dB
Supply voltage	+3.3V
Power consumption	130mW at 200 fps
Operating temperature	-5°C to +70°C
Packaging	48-pin CLCC

In snapshot mode it accepts an external trigger and then generates the readout timing. In slave mode the sensor accepts external readout timing. The integration time is programmed through the two-wire serial interface (master or snapshot mode) or controlled via externally-generated control signals (slave mode). The scanning mode can be progressive or interlaced. There is also an option to scan just a window of interest by choosing start row and column and stop row and column. The user can control the frame rate and row rate through the use of vertical and horizontal blanking as well as the master clock frequency.

The readout of the data out of the chip can be done simultaneously with integration and ADC operation due to the two-cell SRAM which allows data from the previously converted row to be shifted into the output memory for readout. The sensor's ADCs contain special self-calibrating circuitry that allow the sensor to reduce its own column-wise fixed pattern noise. The calibration coefficients can be read from, and written to, the sensor.

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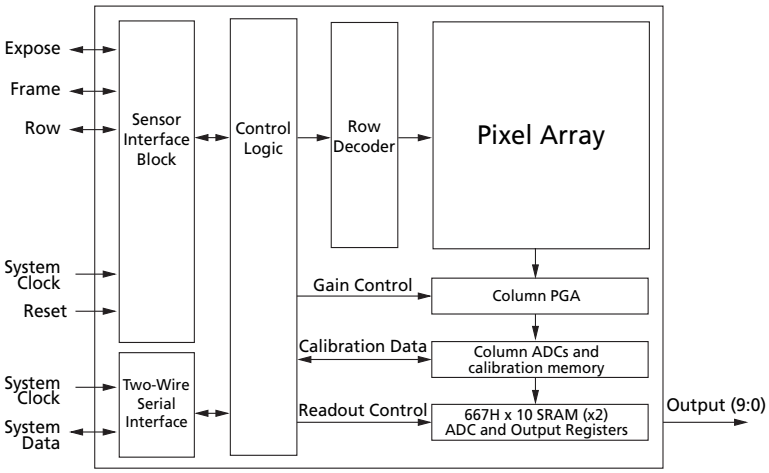
Figure 1: Block Diagram



Pin Description

Table 2: Pin Description

Pin (Ball) Numbers	Symbol	Type	Description
37	SYSCLK	Input	Clock input for entire chip. Maximum design frequency is 66 MHz (50 percent, ±5 percent duty cycle).
39	SDATA	Input/ Output	Serial port data.
38	SCLK	Input	Serial port clock. Maximum frequency is 1 MHz.
33	LRST_N	Input	Global logic RESET function (asynchronous). Active low pulse with minimum duration 200ns.
30[1]	ROW_STRT	Input	Slave mode input signal. Starts row processing sequence of the pixel row (i.e., pixel readout, ADC conversion, and writing of data to ADC registers). The rising edge of ROW_STRT should be synchronous with the falling edge of SYSCLK. A one-clock cycle wide active high pulse. The two-wire serial interface register setting switches this pin between input and output.
31[1]	LD_SHFT_N	Input	Slave mode input signal. An active LOW signal that enables the column counter and initiates the readout process. Causes the 10-bit output port to be updated with data on the rising edge of the system clock. The two-wire serial interface register setting switches this pin between input and output.
26	PG_N	Input	Slave mode input signal. Active low pulse that resets all photodetectors, starting a new integration cycle. No connection should be made in master mode or snapshot mode. Signal is pulled up on-chip.
25	TX_N	Input	Slave mode input signal. Active low pulse that controls transfer of charge from photodetector to memory inside each pixel for the entire pixel array. No connection should be made in master mode or snapshot mode. Signal is pulled up on-chip
24	RESMEM	Input	Slave mode input signal. Active low pulse to reset all pixel memories. No connection should be made in master mode or snapshot mode. Signal is pulled up on-chip.
32	FRAME_SYNC_N	Input	Slave mode input signal. Active low pulse to reset row and column counters, providing frame synchronization. Low duration should be at least two-clock cycles wide. An input that is held LOW also sets the sensor in LOW, per standby mode, until it is released. Signal is pulled up on-chip.
30[1]	FRAME_VALID	Output	Master mode and snapshot mode output signal. Active HIGH during readout. The two-wire serial interface register setting switches this pin between input and output.
31[1]	ROW_VALID	Output	Master mode and snapshot mode output signal. Active HIGH when image data are on data output bus. The two-wire serial interface register setting switches this pin between input and output.
29[1]	EXPOSE	Output	Master mode output signal. Active HIGH during exposure. The two-wire serial interface register setting switches this pin between input and output.
29[1]	EXPOSE	Input	Trigger for snapshot mode. The two-wire serial interface register setting switches this pin between input and output. No connection should be made in slave mode.
18	VLNS	Input	Bias setting voltage for VLN_AMP or VLN_OUT. VLN_AMP and VLN_OUT can be individually disconnected from their internal biases via the two-wire serial interface and driven by this input.
17	VLN1	Input	Bias setting voltage for pixel source following operating current.
19	VLP	Input	Bias setting voltage for the column source follower operating current.
13	VOFF	Input	Dark offset cancellation. Polarity of offset is set via the two-wire serial interface.

Table 2: Pin Description (continued)

Pin (Ball) Numbers	Symbol	Type	Description
16	VREF	Input	Op amp bias.
9	VREF1	Input	ADC reference voltage that sets the maximum input signal level, setting the size of the least significant bit (LSB) in the analog to digital conversion process.
8	VREF1DRV	Input	ADC bias.
7	VREF2	Input	ADC reference used for the calibration operation.
14	VTEST	Input	The user should ground this pin.
23	VRSTLOW	Input	Offset that may be needed for very short exposure conditions.
21	VLN2	Input	Bias setting voltage for the ADC operating current.
41	DATA9	Output	Pixel output data bit 9 (MSB).
40	DATA8	Output	Pixel output data bit 8.
45	DATA7	Output	Pixel output data bit 7.
42	DATA6	Output	Pixel output data bit 6.
46	DATA5	Output	Pixel output data bit 5.
47	DATA4	Output	Pixel output data bit 4.
48	DATA3	Output	Pixel output data bit 3.
1	DATA2	Output	Pixel output data bit 2.
2	DATA1	Output	Pixel output data bit 1.
3	DATA0	Output	Pixel output data bit 0 (LSB).
12, 22	VAA	Power	3.3V power supply for analog signal processing circuitry.
20	VRST_PIX	Power	Power supply for pixel array. Set for 2.5V.
10, 11, 15	AGND	Power	Ground for analog signal processing circuitry.
6, 27, 36, 43	VDD	Power	3.3V digital power supply.
4, 5, 28, 34, 35, 44	DGND	Power	Ground for digital circuitry.

Note: [1]Pins 29, 30, and 31 can be input or output depending on which mode the device is in.

Pixel Data Format

The pixel array descriptions and details are shown below.

Figure 2: Pixel Array Description

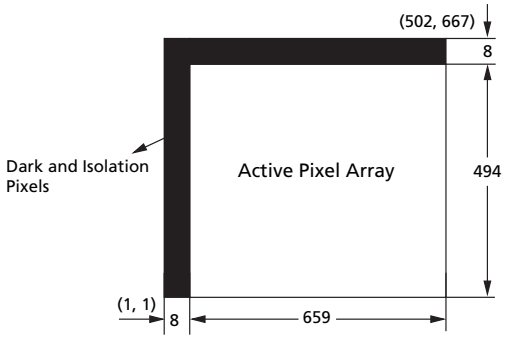
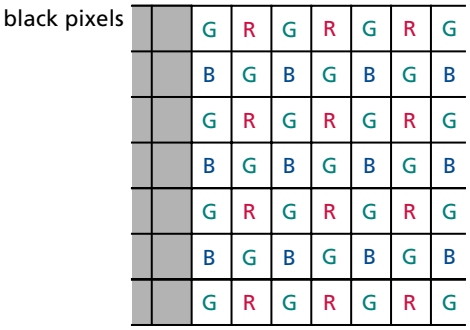


Figure 3: Pixel Color Pattern Detail (Bottom Left Corner)



Output Format and Timing

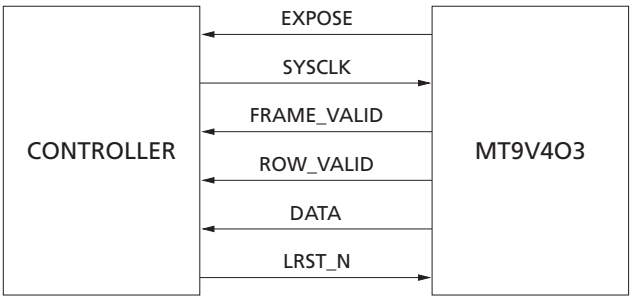
The sensor can operate in three interface modes: master, snapshot, or slave mode. Additionally, master mode can be setup to allow simultaneous integration and readout (simultaneous master mode) or sequential integration and readout (sequential master mode). Mode selection is done via the two-wire serial interface, taking less than one frame time to switch between modes.

The default register settings program the imager to read out the visible pixels. Therefore, the start row is 1, start column is 9, end row is 480 and the end column is 648.

Master Mode

In master mode the sensor internally generates the timing to initiate exposure and readout. The interface signals utilized in master mode are depicted in Figure 4. In master mode, the start of the integration period is determined internal to the MT9V403.

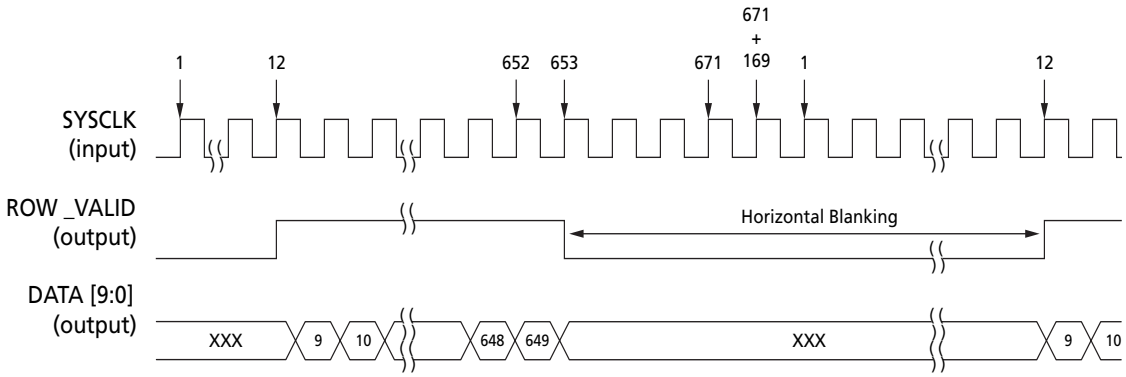
Figure 4: Master Mode Interface Signals



The integration time is pre-programmed via the two-wire serial interface and indicated by the EXPOSE signal going HIGH. When the sensor commences, the readout process the FRAME_VALID, ROW_VALID, and DATA signals are output, as shown in Figure 5 on page 9.

The master mode row synchronization waveform relationships are as shown in Figure 5 on page 9. The FRAME_VALID signal goes HIGH, indicating the start of frame, and 2.5 clock cycles later the ROW_VALID signal goes HIGH, indicating the start of the first row. The first data bit is valid on the first falling edge of SYSCLK after ROW_VALID goes HIGH. The remaining 665 pixels for the row are valid on the subsequent falling edges of SYSCLK, after which ROW_VALID returns to the LOW state. (Please note that in master mode 648 pixels are readout for each row.) The ROW_VALID will then be an active HIGH envelope for subsequent rows and the FRAME_VALID signal will be an active HIGH envelope for subsequent frames. The time required for one complete row operation is 671 clock cycles: 1 clock cycle delay + 666 columns + 4 clock cycles when ROW_VALID is LOW. With a SYSCLK of 66 MHz, this translates into a row time of 10.2µs and a frame time of 5.1ms for full resolution (502 rows). This assumes there is no vertical blanking or horizontal blanking and that the exposure time is less than 5.1ms. If exposure time becomes greater than 5.1ms, the frame time then becomes the inverse of the exposure time (1/[exposure time]).

Figure 5: Master Mode Row Timing Diagram



Note: Horizontal blanking is nominally 35 rows, and may be increased using register 5.

In master mode the frame rate is controlled by inserting vertical and/or horizontal blanking periods during readout, or by changing the input master clock (SYSCLK) frequency (i.e., slowing the sensor down), or by changing the number of rows being readout (i.e., window size). Table 3 shows some examples of how the frame rate changes with window resolution and clock speed.

Table 3: Frame Rate vs. Resolution and Clock Speed
No blanking, Exposure < Readout

Resolution (# rows)	Clock Speed (sysclk)	Frame Rate (frames/second)
502 (full resolution)	66 MHz	196
251	66 MHz	392
125	66 MHz	784
63	66 MHz	1568
502 (full resolution)	24 MHz	70
251	24MHz	140
125	24 MHz	280
63	24 MHz	560
502 (full resolution)	10 MHz	30

When horizontal blanking is utilized, the ROW_VALID stays LOW for an additional user-programmable number of clock cycles after each row readout. As a result the row time becomes:

$$RT = (1 + 66\ 6+ 4 + HB) \times (1/fsysclk)$$

where HB is the horizontal blanking in SYSCLK cycles (255 clock maximum) specified in register 5.

When vertical blanking is utilized, the FRAME_ VALID signal stays LOW for an additional user programmable number of rows after the frame is readout (if exposure time < readout time) or exposed (if exposure time > readout time). Table 4 on page 10 shows the various scenarios for calculating the frame time, where VB is the vertical blanking in rows (255 rows maximum) specified in register 6. The default vertical blanking is one SYSCLK cycle, so the true vertical blanking time is the number of blanking rows programmed plus one clock cycle.

Table 4: Determination of Frame Timing

	Exposure TIme > Readout Time	Readout Time> Exposure Time
No Blanking	Frame Time = Exposure Time	Frame Time = N x RT
With Vertical Blanking	Frame Time = Exposure Time + VB	Frame Time = (N + VB) x RT

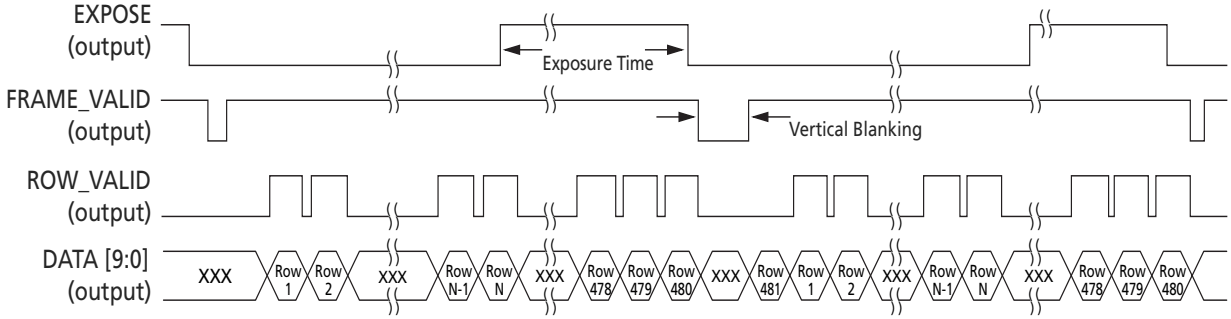
Note: N = number of rows in image
RT = row time
VB = vertical blanking rows (255 rows maximum); set in register 6
HB = horizontal blanking in SYSCLK cycles (255 maximum); set forth in register 6

Simultaneous Master Mode

There are two possible operation methods for master mode: simultaneous master mode and sequential master mode. One of these operation modes must be selected via the two-wire serial interface. In simultaneous master mode the exposure period occurs during readout. The frame synchronization waveforms are shown in Figure 6 and Figure 7. This is the fastest mode of operation since the exposure and readout are happening in parallel rather than sequentially. Please note that with this speed optimized timing the first row readout is the last row of the previous frame that is still in the row memory.

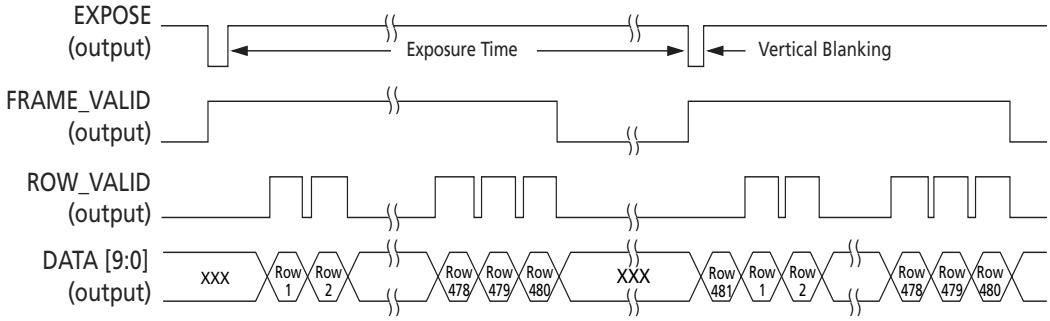
Note: In simultaneous master mode, when integration time is less than frame time, noise generated from global signals can degrade image quality. The section of the image that degrades tracks the integration time.

Figure 6: Simultaneous Master Mode Frame Synchronization Waveforms Readout Time > Exposure Time



Note: Vertical blanking is nominally 1 SYSCLK and 0 row times, and may be increased by using register 6.

Figure 7: Simultaneous Master Mode Frame Synchronization Waveforms Exposure Time > Readout Time

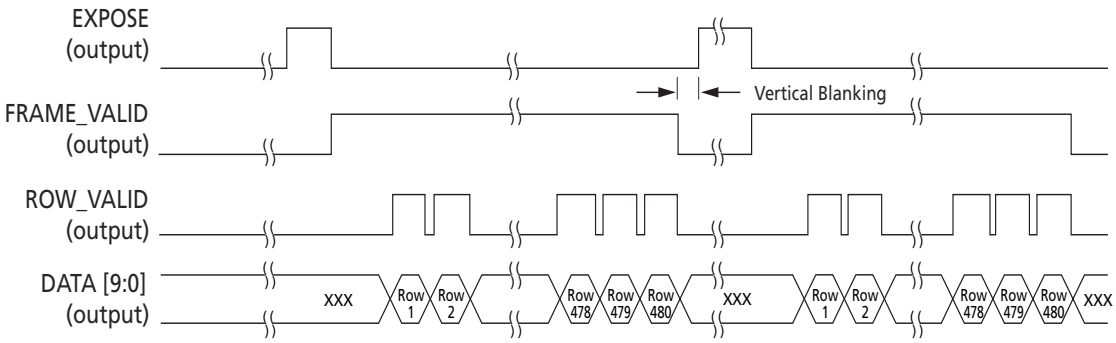


Note: Vertical blanking is nominally 1 SYSCLK and 0 row times, and may be increased by using register 6.

Sequential Master Mode

In sequential master mode the exposure period is followed by readout. The frame synchronization waveforms for sequential master mode are shown in Figure 8.

Figure 8: Sequential Master Mode Frame Synchronization Waveforms



Note: Vertical blanking is nominally 1 SYSCLK and 0 row times, and may be increased by using register 6.

Snapshot Mode

In snapshot mode the sensor accepts an input trigger signal that initiates exposure, which is immediately followed by readout. The interface signals utilized in snapshot mode are depicted in Figure 9. In snapshot mode the start of the integration period is determined by the externally applied EXPOSE pulse that the user inputs to the MT9V403. The integration time is preprogrammed via the two-wire interface. After each frame's integration period is complete, the readout process commences and the FRAME_VALID, ROW_ VALID, and DATA signals are output.

Snapshot mode can be used to capture a single image or a sequence of images. The frame rate is controlled only by changing the period of the user supplied EXPOSE pulse train. The frame synchronization waveforms for snapshot mode are shown in Figure 9. Insertion of horizontal blanking periods (specified via the two-wire serial interface register) during readout is allowed, but the user controls the vertical blanking by controlling the input EXPOSE pulse.

Figure 9: Snapshot Mode Interface Signals

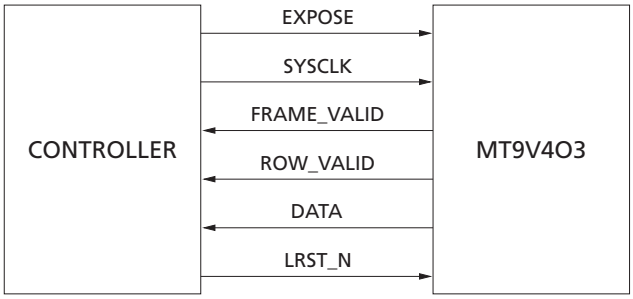
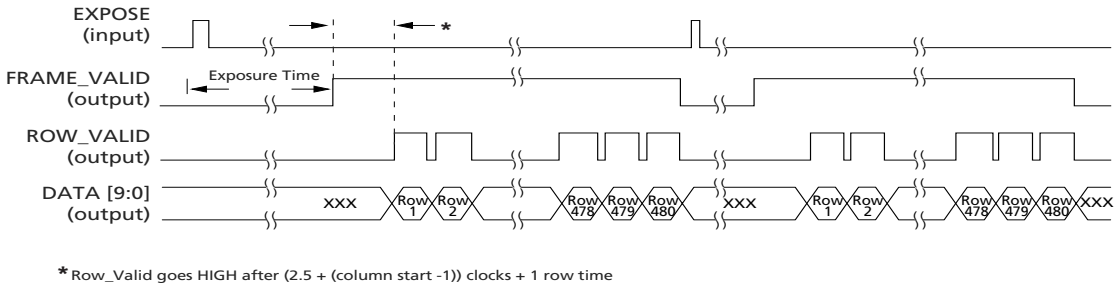


Figure 10: Snapshot Mode Frame Synchronization Waveforms



* Row_Valid goes HIGH after (2.5 + (column start -1)) clocks + 1 row time

Slave Mode

Slave mode allows the user much greater control of the sensor. The interface signals utilized in slave mode are depicted in Figure 11. The user can start and stop integration through the use of PG_N and TX_N, respectively. The use of the RESMEM signal to reset pixel memories prior to ending exposure (TX_N) is optional. The readout process is controlled by user-supplied row control signals (ROW_STRT and LD_SHFT_N). Additionally, the FRAME_SYNC _N signal may be used for frame synchronization.

Figure 11: Slave Mode Interface Signals

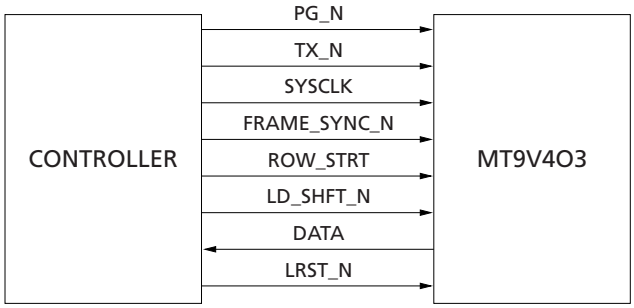


Figure 12 on page 14 shows the block diagram of the sensor for slave mode operation, where the sensor's digital block requires external synchronization inputs to trigger generation of the row conversion and readout sequence. The internal structure of the digital block in slave mode includes row counter, column counter, and row sequencer. The rising edge of the ROW_STRT signal increments the row counter to the next value and triggers the row sequencer. The row sequence duration is always equal to 671 clocks, which is fixed by the column parallel architecture. The duration of the ROW_STRT signal should be one clock cycle.

The column counter selects the column output SRAM cells for off-chip readout at the speed of SYSCLK. LD_SHFT_N enables the column counter when LOW. Data is output 3.5 clocks after LD_SHFT_N goes LOW. The column counter is zeroed when LD_SHFT_N is HIGH; if LD_SHFT is not high the counter will continue.

The row counter and column counter may be zeroed using the CLEAR signal, which is driven by register 14. The user can set the CLEAR signal by writing to this register through the two-wire serial interface or by pulling down the FRAME_SYNC_N signal for two clock cycles.

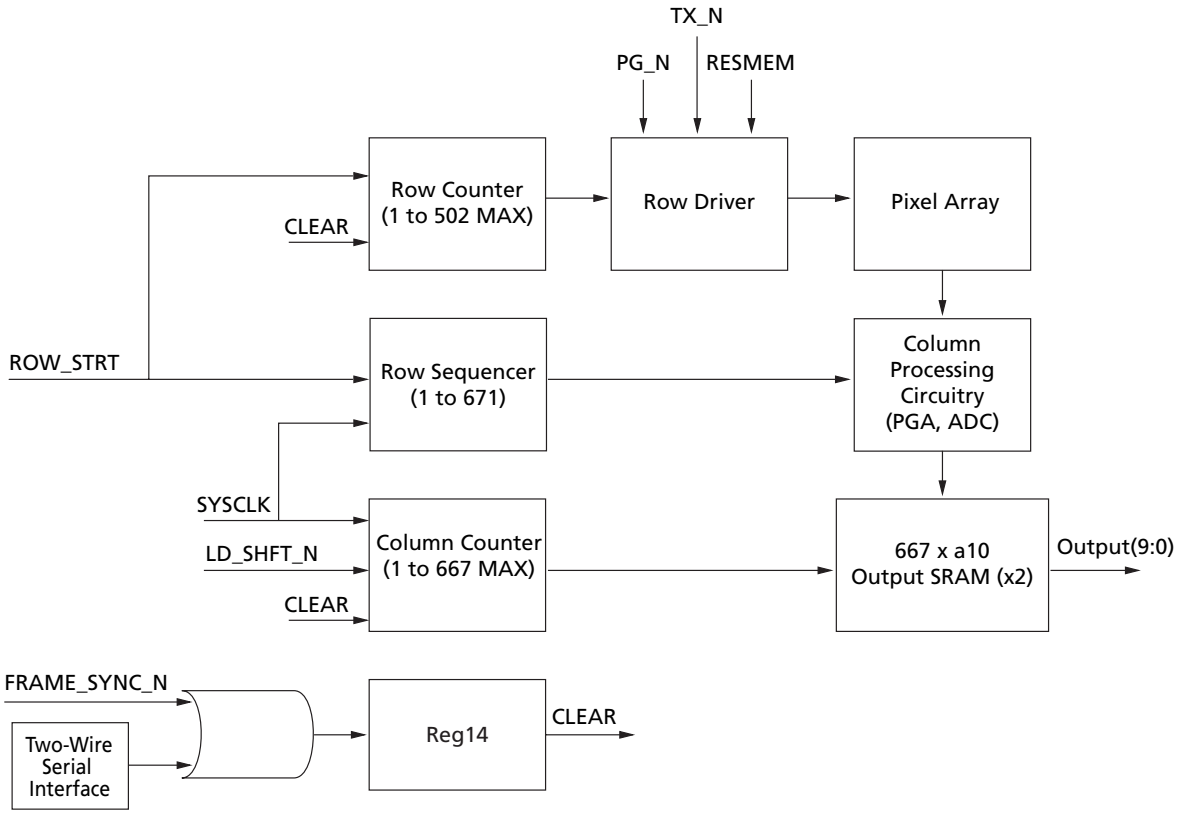
When operating in slave mode, the user should keep in mind that both the row and column counters count between the START and STOP values, which are set in registers 1–4 via the two-wire serial interface. Sufficient time should be allocated to allow the

counters to complete. It must also be emphasized that the row sequencer always requires 671 clock cycles independent of the START and STOP values (i.e., window size). Horizontal blanking may be achieved between rows by holding LD_SHFT_N HIGH and delaying the application of the ROW_STRT rising edge.

Additionally, it is possible to operate the sensor in a pipelined manner or non-pipelined manner in slave mode (master mode is always pipelined). Pipelined operation means that a row of data is read out of the sensor at the same time that a new row is converted. This is accomplished through the dual SRAM banks that store one row for readout in one bank while the other bank is being filled with a newly converted row. As mentioned above, the ROW_STRT triggers the row conversion and LD_SHFT_N enables the data output. These can be applied nearly simultaneously to achieve pipelined operation or applied sequentially, offset by the row processing time, for non-pipelined operation.

Note: To reduce horizontal temporal noise in slave mode, delay readout by 80 SYSCLK.

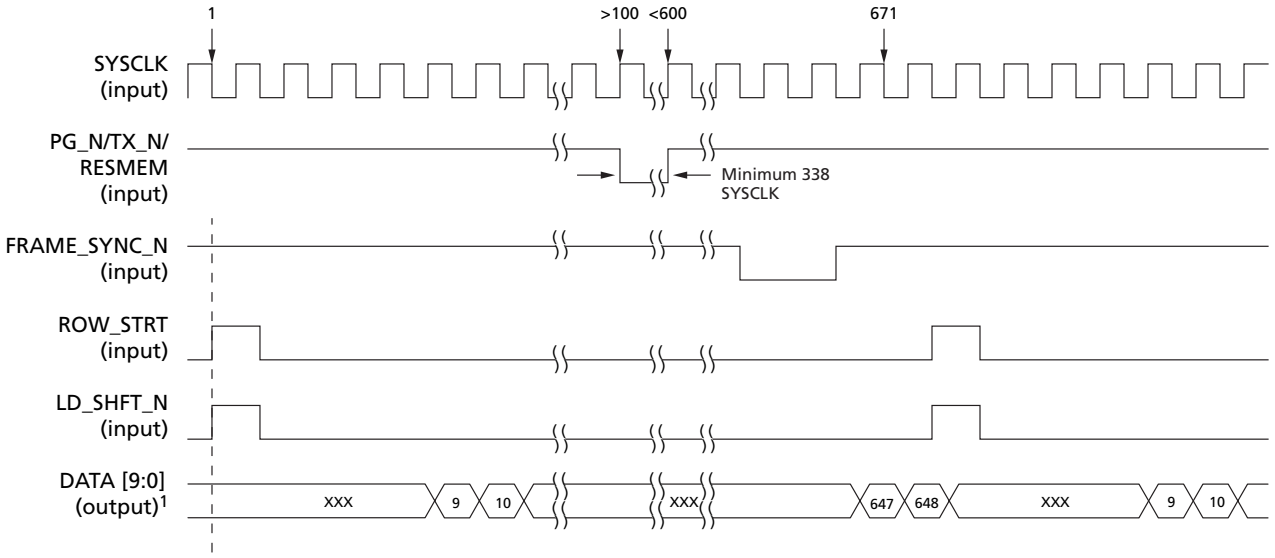
Figure 12: Slave Mode Block Diagram



Simultaneous Slave Mode

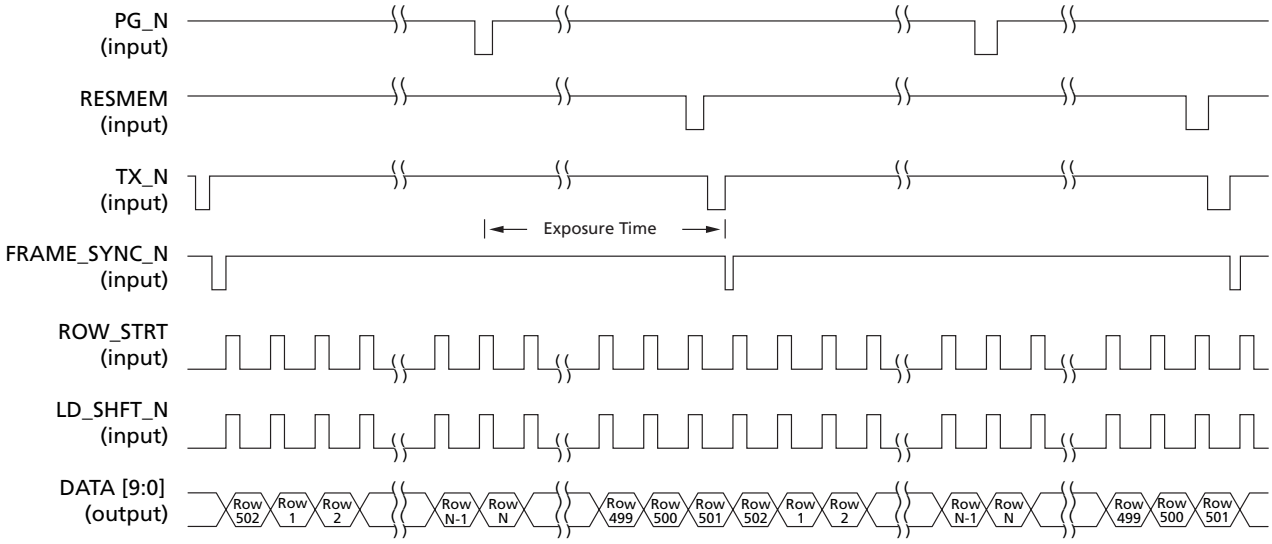
There are two possible operation methods for slave mode: simultaneous slave and sequential slave mode. The method of operation selected is determined by the means in which the user supplies the control signals. In simultaneous slave mode the exposure period occurs during readout. The row and frame synchronization waveforms are shown in Figures 13 and 14, respectively. This is the fastest mode of operation since the exposure and readout are happening in parallel rather than sequentially. The PG_N, TX_N, and RESMEM pulses should have a minimum duration of 338 clock cycles and be applied between the 100th and 600th clocks of a given row.

Figure 13: Simultaneous Slave Mode Row Timing Diagram Example (Default Settings)



Note: [1]Starts with col 9 with default register settings.

Figure 14: Simultaneous Slave Mode Frame Synchronization Waveforms Example



Sequential Slave Mode

In sequential slave mode the exposure period is followed by readout. The row and frame synchronization waveforms are shown in Figures 15 and 16, respectively.

Figure 15: Sequential Slave Mode Row Timing Diagram Example

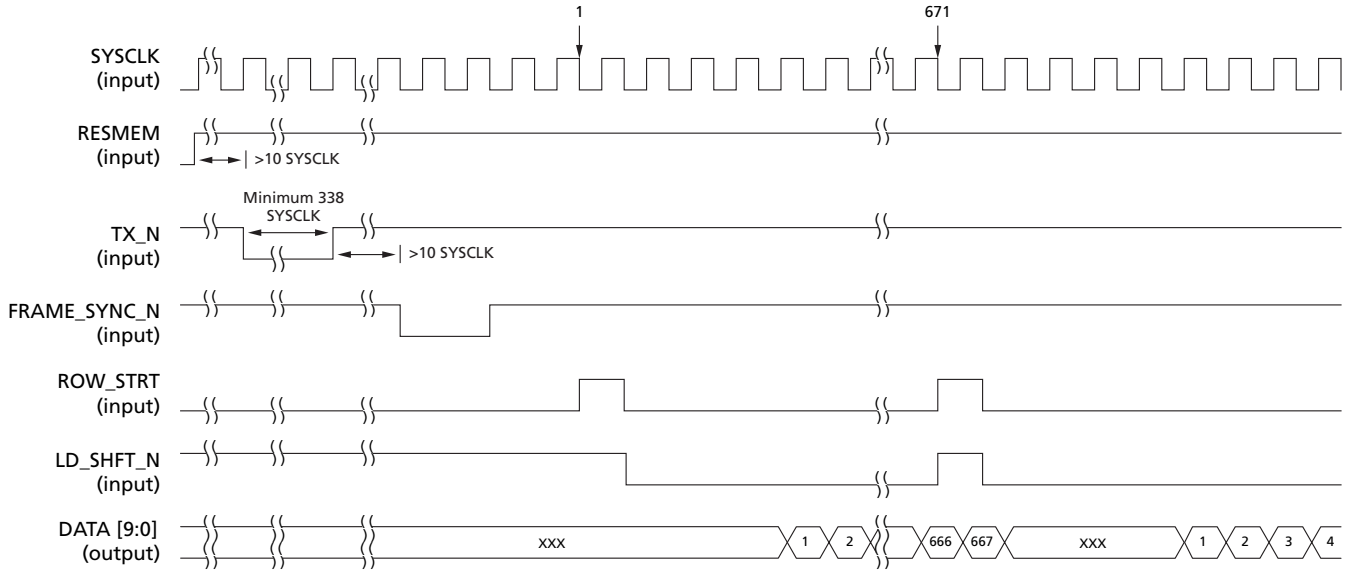
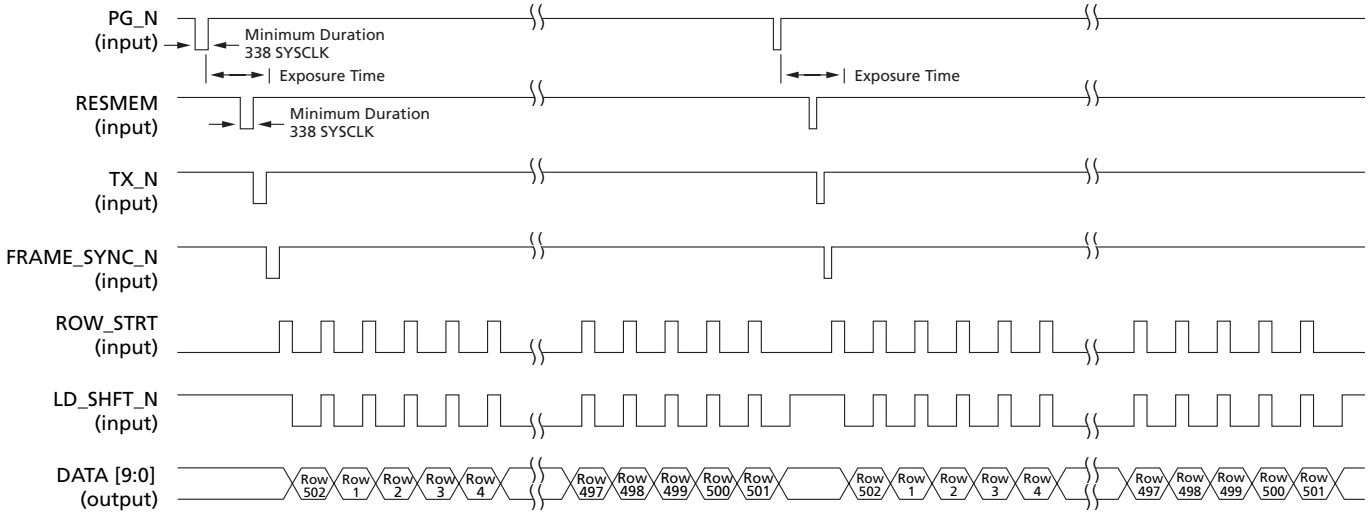


Figure 16: Sequential Slave Mode Frame Synchronization Waveforms Example



To increase intrascene dynamic range of the sensor in slave mode, the user can implement dual sampling. This is possible by applying an additional TX pulse during the integration period. By doing this, one combines two photo signals after different exposures. Figure 17 shows an example of the timing. N1 is the number of rows in the first exposure. N2 is the number of rows in the second exposure. N1 = 502 for the full frame exposure time. The intrascene dynamic range capability of the sensor is extended by the factor N1/N2. For N1 = 500 and N2 = 2, the dynamic range enhancement is approximately 48 dB. Figure 18 shows output signal vs. photocurrent. The knee point is dependent on the VRSTLOW bias, which determines the charge capacity of the photodiode. The saturation level of photodiode must be less than the saturation level of the ADC. Setting VRSTLOW to 1.2V is enough for the default gain settings. The slope of the curve after the knee point or compression level is determined by the N1/N2 ratio.

Figure 17: Extended High Dynamic Range Timing in Slave Mode

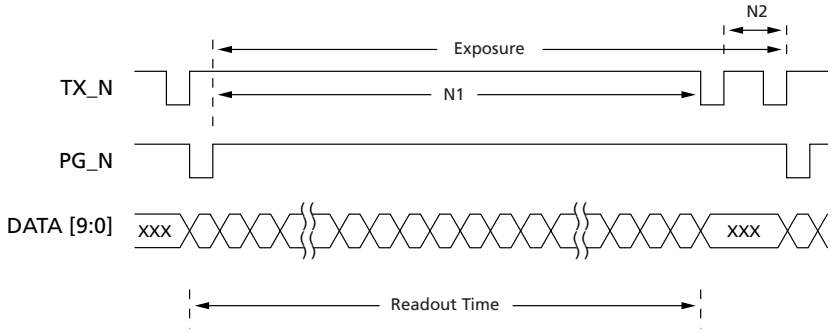
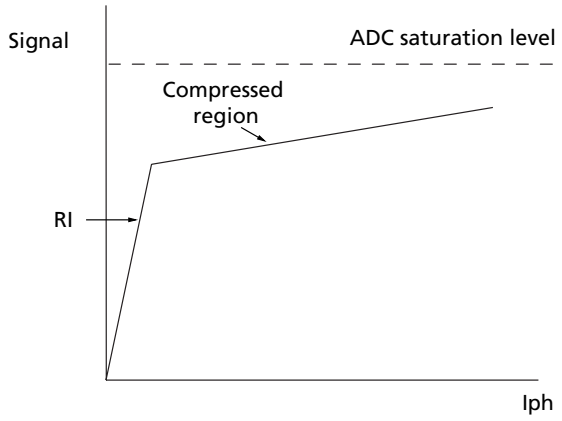


Figure 18: Output Signal vs. Photocurrent



Serial Bus Description

Registers are written to and read from the MT9V403 through the two-wire serial interface bus. The MT9V403 is a two-wire serial interface slave with device ID "1011100x" and is controlled by the two-wire serial interface clock (SCLK), which is driven by the two-wire serial interface master. Data is transferred into and out through the two-wire serial interface data (SDATA) line. The SDATA line is pulled up to 3.3V off-chip by a 1.5KΩ resistor. Either the slave or master device can pull the SDATA line down—the two-wire serial interface protocol determines which device is allowed to pull the SDATA line down at any given time. it is recommended that the MT9V403 have its own dedicated serial bus.

Protocol

The two-wire serial host interface bus defines several different transmission codes, as follows:

- a start bit
- the slave device eight-bit address
- a(n) (no) acknowledge bit
- an eight-bit message
- a stop bit

Sequence

A typical read or write sequence begins by the master sending a start bit. After the start bit, the master sends the slave device's eight-bit address. The last bit of the address determines if the request will be a read or a write, where a “0” indicates a write (i.e., address B8h) and a “1” indicates a read (i.e., address B9h). The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a write, the master then transfers the eight-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data eight bits at a time, with the slave sending an acknowledge bit after each eightbits. The MT9V403 uses a 16-bit data for its internal registers, thus requiring two eight-bit transfers to write to one register. To write/read this 16-bit data, first perform a write/read the eight MSBs, then perform another write/read for eight LSBs. After 16 bits are transferred, the register address should be incremented, so that the next 16 bits are written to the next register address. The master stops writing by sending a start or stop bit.

A typical read sequence is executed as follows. First the master sends the write-mode slave address and eight-bit register address, just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data eight bits at a time. The master sends an acknowledge bit after each eight-bit transfer. The register address should be incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

Bus Idle State

The bus is idle when both the data and clock lines are HIGH. Control of the bus is initiated with a start bit, and the bus is released with a stop bit. Only the master can generate the start and stop bits.

Start Bit

The start bit is defined as a HIGH-to-LOW transition of the data line while the clock line is HIGH.

Stop Bit

The stop bit is defined as a LOW-to-HIGH transition of the data line while the clock line is HIGH.

Slave Address

The eight-bit address of a two-wire serial interface device consists of seven bits of address and one bit of direction. A “0” in the LSB of the address indicates write mode, and a “1” indicates read mode.

Data Bit Transfer

One data bit is transferred during each clock pulse. The two-wire serial interface clock pulse is provided by the master. The data must be stable during the HIGH period of the two-wire serial interface clock—it can only change when the two-wire serial interface clock is LOW. Data is transferred eight bits at a time, followed by an acknowledge bit.

Acknowledge Bit

The master generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and the receiver indicates an acknowledge bit by pulling the data line LOW during the acknowledge clock pulse.

No-Acknowledge Bit

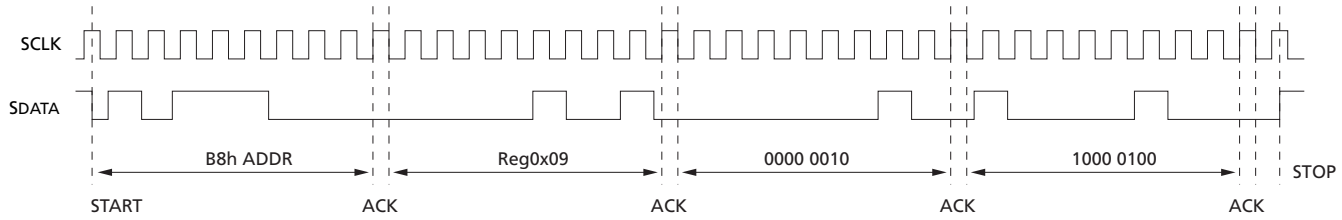
The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

Two-Wire Serial Interface Sample Write and Read Sequences

Example of a 16-Bit Write Sequence

A typical write sequence for writing 16 bits to a register is shown in Figure 19. A start bit given by the master, followed by the write address, starts the sequence. The image sensor will then give an acknowledge bit and expects the register address to come first, followed by the 16-bit data. After each eight bit, the image sensor will give an acknowledge bit. All 16 bits must be written before the register will be updated. After 16 bits are transferred, the register address should be incremented, so that the next 16 bits are written to the next register. The master stops writing by sending a start or stop bit.

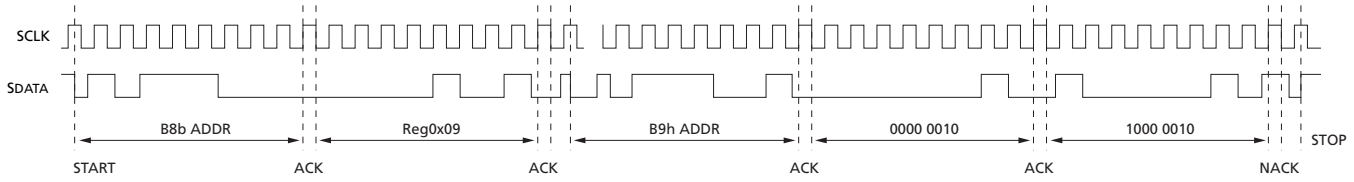
Figure 19: Timing Diagram Showing a Write to Register 9 with the Value 644



Example of a 16-Bit Read Sequence

A typical read sequence is shown in Figure 20. First the master has to write the register address, as in a write sequence. Then a start bit and the read address specifies that a read is about to happen from the register. The master then clocks out the register data eight bits at a time. The master sends an acknowledge bit after each eight-bit transfer. The register address should be incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

Figure 20: Timing Diagram Showing a Read from Register 9; Returned Value is 642



Registers

Table 5: Complete Register Description

Read/Write Control	Register Name	Function	Default Contents	Register Address
Read only	Reg0	Chip Version.	0000001100000001	00000000
W/R	Reg1	Row start address.	*******000000001	00000001
W/R	Reg2	Column start address.	******0000001001	00000010
W/R	Reg3	Stop row address.	*******111100000	00000011
W/R	Reg4	Stop column address.	******1010001000	00000100
W/R	Reg5	Number of blank columns (horizontal blanking).	********10101001	00000101
W/R	Reg6	Number of blank rows (vertical blanking).	********00100011	00000110
W/R	Reg7	Control mode. Bit 0 = 1 simultaneous mode. Bit 0 = 0 sequential mode. Bit 1 = 1 snapshot mode. Bit 2 = 1 master mode. Bits 3–7 not used; set to 0. Possible combinations are"00000101," "00000100," "00000010," "00000000". The last combination means slave mode.	********00000101	00000111
W/R	Reg8	Number of frame times in integration time.	********00000000	00001000
W/R	Reg9	Number of rows times in integration time. Maximum = 502. Minimum = 2.	*******111110110	00001001
W/R	Reg10	Interlaced mode control. Bit 0 = 1 interlaced mode 1. Readout of both fields even and odd. Bit 1 = 1 interlaced mode 1 = 2. Readout of only one field – even or odd. Depends on start row. Bits 2–7 not used; set to 0. Note: Interlaced mode 1 does not work with snapshot mode.	********00000000	00001010
W/R	Reg12	Calibration control. Bit 0 = 1 calibration at the beginning of every frame.	********00000000	00001100
W/R	Reg13	Dark offset enable and pixel memory reset pulse duration control. Bit 1 = 1 dark offset of ADC input signal using VOFF is enabled. Bits 2–7 not used; set to 0.	********00000000	00001101

Table 5: Complete Register Description (continued)

Read/Write Control	Register Name	Function	Default Contents	Register Address
W/R	Reg14	Clear signal control. Bit 0 = 1 reset row and column counters in digital block. Sensor is in idle mode. The two-wire serial interface works and it is still possible to WRITE/READ in registers. Changes of registers content follows without delay. Normally, change of register content occurs only at the beginning of next frame in cases where the two-wire serial interface data is not busy.	********00000000	00001110
Write only	Reg15	ADC calibration data input register.	*********0000000	00001111
W/R	Reg16	VLN_AMP bias control. Bit 7 = 1 disable internal bias. Bit 0 = 1 high bias. Bit 1 = 1 low bias. Bits 3–6, 8–15 not used, set to 0.	0000000000000000	00010000
W/R	Reg17	VLN2 bias control. Bit 7 = 1 disable internal bias. Bit 0 = 1 high bias. Bit 1 = 1 low bias. Bits 3–15 not used, set to 0.	0000000000000000	00010001
W/R	Reg18	VLN_OUT bias control. Bit 7 = 1disable internal bias. Bit 0 = 1 high bias. Bit 1 = 1 low bias. Bits 3–6, 8–15 not used, set to 0.	0000000000000000	00010010
W/R	Reg19	VLN1 bias control. Bit 7 = disable internal bias. Bit 0 = 1 high bias. Bit 1 = 1 low bias. Bits 3–6, 8–15 not used, set to 0.	0000000000000000	00010011
W/R	Reg20	VLP bias control. Bit 7 = 1 disable internal control. Bit 0 = 1 high bias. Bit 1 = 1 low bias. Bits 3–6, 8–15 not used, set to 0.	0000000000000000	00010100
W/R	Reg21	V_{REF} bias control. Bit 0-3 = bias value. Bit 7 = 1 disable internal bias. Bits 4–6, 8–15 not used, set to 0.	0000000000001010	00010101
W/R	Reg22	$V_{REF}2$ bias control. Bit 0-3 bias value. Bit 7= 1 disable internal bias. Bits 4–6, 8–15 not used, set to 0.	0000000000001010	00010110

Table 5: Complete Register Description (continued)

Read/Write Control	Register Name	Function	Default Contents	Register Address
W/R	Reg23	VOFF bias control. Bit 0-3 bias value. Bit 6 = 1 sign of offset is negative. Bit 7 = 1 disable internal bias. Bits 4–5, 8–15 not used, set to 0.	0000000000000000	00010111
W/R	Reg29	VLN2 bias booster. Bit 3 = 1 high bias.	0000000000000000	00011101
W/R	Reg43	Blue gain settings. Default gain is 2. Gain settings range is from 1 (00000001) to 18 (00010010).	********00000010	00101011
W/R	Reg44	Green 1 gain settings. Default gain is 2. Gain settings range is from 1 (00000001) to 18 (00010010).	********00000010	00101100
W/R	Reg45	Green 2 gain settings. Default gain is 2. Gain settings range is from 1 (00000001) to 18 (00010010).	********00000010	00101101
W/R	Reg46	Red gain settings. Default gain is 2. Gain settings range is from 1 (00000001) to 18 (00010010).	********00000010	00101110
W/R	Reg53	Global gain control. Bit 0 = 1 gain is multiplied by factor of 0.5	*********0000000	00110101
W/R	Reg59	VREF1 bias control. Bits 0-3 bias value. Bit 7 = 1 disable internal bias. Bits 4–6, 8–15 not used, set to 0.	0000000000001100	0011101
Read only	Reg143	ADC calibration data output register.	*********0000000	10001111

Register Start-up Sequence

Upon powering up the MT9V403, the sensor should be reset by bringing the LRST_N pin LOW. This will initialize all of the registers to their default values. Upon the release of reset, the sensor will perform ADC calibration. The default mode is simultaneous master mode with the horizontal blanking register set to 169 and the vertical blanking register set to 35. The default frame size is 648 x 480 pixels, excluding dark pixels. The first frame starts just three SYSCLK cycles after the end of calibration and the integration process takes place during this frame but valid data for the first pixel row is not output until the second frame.

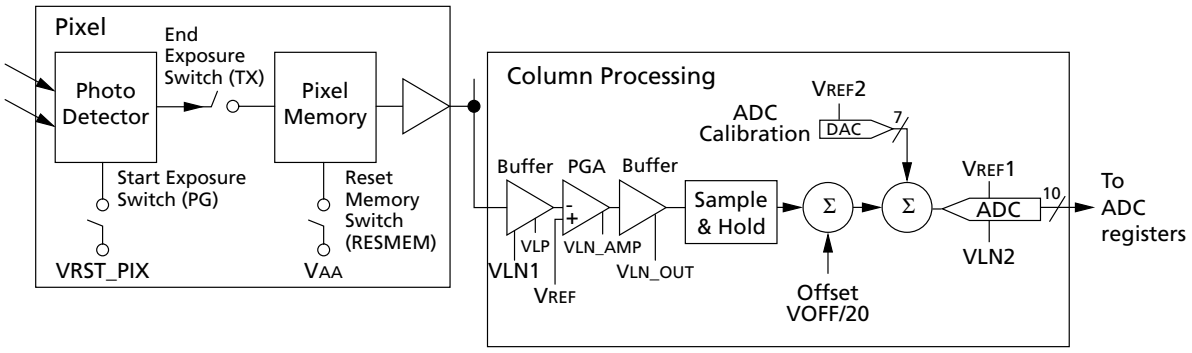
All two-wire serial interface parameters can be written to registers at any time but they do not take effect until the subsequent frame. Writing to two-wire serial interface registers has no effect on the output timing (i.e., it does not slow down or stop output); the exception to this rule is when the sensor is commanded to perform ADC calibration.

Feature Description

Signal Path

An example of the signal path is shown below in Figure 21.

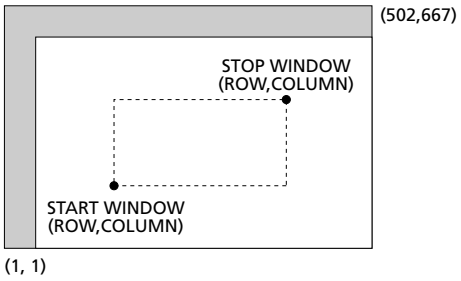
Figure 21: Signal Path



Window Location and Size

There is also an option to scan just a window of interest by using the two-wire serial interface to specify the coordinates of the upper right most pixel and the lower left most pixel to define the desired windowing area as shown in Figure 22. The user can increase the frame rate by decreasing the number of rows in a window. Decreasing the number of columns has no effect on frame rate. For example, for the full 667 column by 502 row resolution the MT9V403 operates at 196 fps, but if the vertical resolution is decreased by half (i.e., 251 rows) the frame rate increases proportionally so the frame rate is doubled to 392 fps.

Figure 22: Windowing Example



When windowing is utilized, the user should be aware of how the sensor timing is impacted. A key point to note is that the row time is always 671 clock cycles, independent of how many columns are actually read out of the sensor. Figure 23 provides a master mode row timing example for windowing from column 100 to column 200. This shows how changing the number of columns in a window will not change the timing nor the frame rate. Figure 24 provides a master mode frame timing example for windowing from row 300 to row 400. This shows how changing the number of rows in a window will increase the frame rate.

Figure 23: Row Timing for Master Mode and Snapshot Mode with Windowing

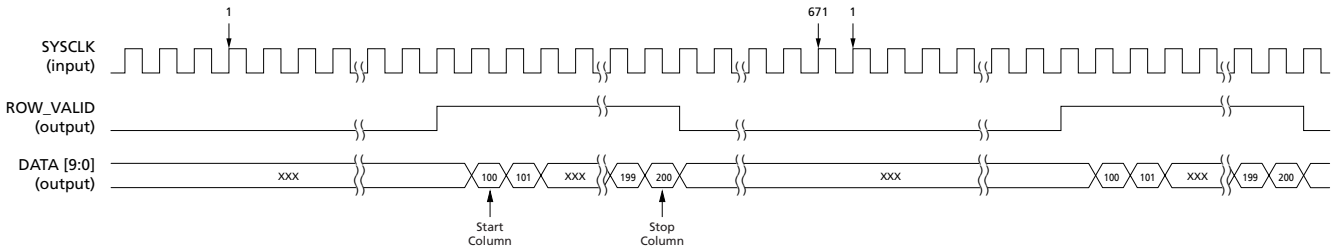
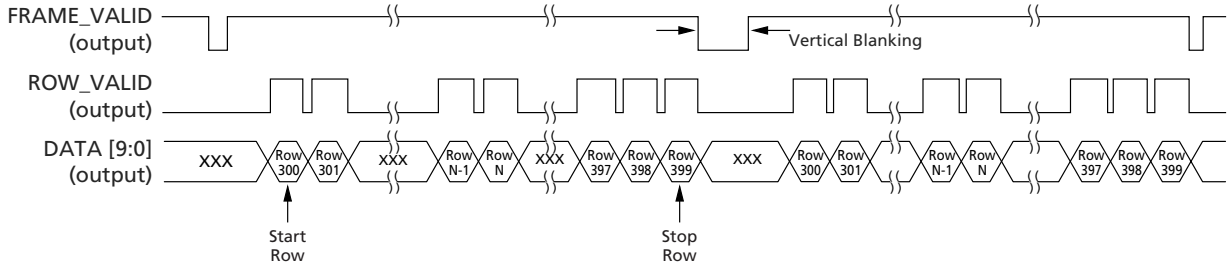


Figure 24: Frame Timing for Master Mode and Snapshot Mode with Windowing



In slave mode the user has more control of the sensor but the same basic rule applies; the row time is still always 671 clock cycles. Figure 25 provides a slave mode row timing example for windowing from column 100 to column 200. The row processing is initiated by raising ROW_STRT and requires 671 clock cycles to complete. The user can readout the desired window of columns by lowering LD_SHFT_N and the specified columns will appear on the output with a 3.5 SYSCLK + contents (reg2) -1 delay. The user must still wait the required 671 clock cycles for the row processing to complete before initiating the processing of the next row with ROW_STRT. Figure 26 provides a slave mode frame timing example for windowing from row 300 to row 400 which—similar to the master mode— shows how changing the number of rows in a window will increase the frame rate.

Figure 25: Row Timing for Slave Mode with Windowing

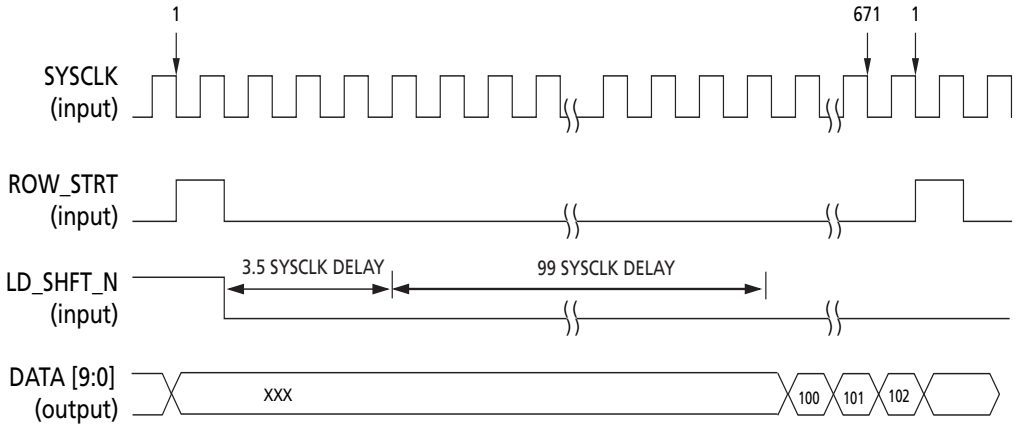
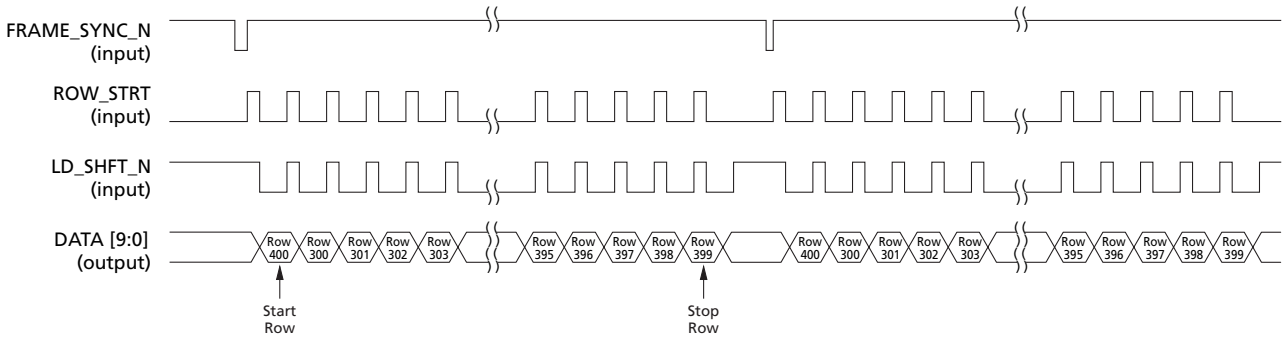


Figure 26: Frame Timing for Slave Mode with Windowing



Electronic Shutter Exposure Control

For the master and snapshot mode the electronic shutter's exposure duration (integration time) is programmed via the two-wire serial interface. The MT9V403 shutter can be operated to generate continuous video output (simultaneous master mode or sequential master mode) or capture single images (snapshot mode).

The minimum integration time in master or snapshot mode is 2 row times. With a 66 MHz SYSCLK the minimum integration time is 20µs (10µs row time ±2 rows). The maximum integration time is either is 256 frame times (1.3 sec @ 200 fps) or the inverse of the frame rate.

When in simultaneous master mode, the maximum integration time is limited by the inverse of the frame rate because one cannot integrate longer than a frame time. With a 66 MHz clock and full resolution (502 rows) the maximum integration time is 5ms (= 1/200 fps). In sequential master mode or snapshot mode the maximum integration time is limited to 256 frame times. Table 6 shows some examples of how the maximum integration time changes with resolution and clock speed.

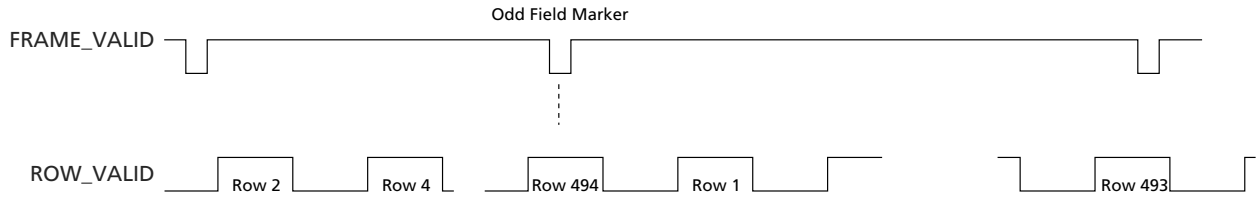
Table 6: Maximum Integration Time vs. Resolution and Clock Speed
Sequential Mode or Snapshot Mode

Resolution (# of rows)	Clock Speed (sysclk)	Frame Time {= N x 671 x 1/FSYSCLK}	Maximum Integration Time
502 (full resolution)	66 MHz	5.1ms	1.3 sec
251	66 MHz	2.6ms	0.7 sec
125	66 MHz	1.3ms	0.3 sec
63	66 MHz	0.6ms	0.2 sec
502 (full resolution)	24 MHz	14ms	3.6 sec
251	24 MHz	7ms	1.8 sec
125	24 MHz	5.1ms	0.9 sec
63	24 MHz	1.8ms	0.4 sec
502 (full resolution)	10 MHz	33ms	8 sec

Readout Scanning

The MT9V403 can operate in either progressive scan or interlaced scan modes. Progressive scan is the default mode. In the interlace scan mode there are two readout options. The frame synchronization waveforms for interlaced scanning are shown in Figure 27, which shows alternating readout of the even-numbered and odd-numbered rows in consecutive frames. There is also an option that allows sequential readout of only the odd or even rows of a frame (effectively a X2 vertical subsampling of the image).

Figure 27: Frame Synchronization Waveforms for Interlaced Scanning



Gain Settings

There are four independent gain controls which are programmed via the two-wire serial interface. The four gains correspond to four cells of the Bayer pattern color filter array: red, green1, blue, and green2. The gain step size can be set to 1 or 0.5. When the step size is 1 the gain can programmed in 18 steps from X1 to X18. When the step size is 0.5, the gain can be programmed 18 steps from X1 to X9. Global gain control is achieved by changing the four gains equally and simultaneously.

To obtain the desired analog signal chain gain, set the following registers as shown in Table .

Analog Biases

VLN1, VLP, VOFF, VREF, VREF1, VLN2 VREF2, VLN_AMP, and VLN_OUT are generated on-chip and can be adjusted via a two-wire serial interface. Also, the user may disable internal bias via a two-wire serial interface and apply external voltages to the sensor. VREF1DRV is generated on-chip but its internal bias cannot be disabled. VRST_PIX and VRSTLOW are not generated internally and external voltages must be applied.

Considerations when Setting Analog Voltages

The starting point for setting the analog voltages should be the values suggested in the typical values columns of the Tables 8 and 9. Additionally, Figure 21 on page 24, the "Signal Path Diagram," indicates how the analog voltages affect the image. Other considerations follow:

VRSTLOW: Functions as a pixel anti-blooming control. For high illumination conditions (typically used in conjunction with a short integration time) black/white spots may appear. To eliminate these artifacts, this voltage should be set to ~0.4V. Once set, this value should not have to be changed for different imaging conditions.

VLN2: Internal default value should be used as the starting point. VLN2 controls the current in the ADC comparators and there is a safe range where this voltage has no effect; settings below this range will cause the comparators to fail. For high-speed operation, VLN2 may need to be increased to remove random white spots. VLN2 may be further increased with register 17 by setting bit 0 to "1." If this does not completely solve the problem, set bit 7 in register 18 to disable VLN_OUT. VLN2 can also be further increased by setting bit 3 high in register 29 or by providing an external VLN2 bias.

VRST_PIX: Should be set to 2.5V.

VREF2: Internal default value is recommended.

VLN1: Internal default value is recommended.

VOFF: Internal default value is recommended.

VREF1: Internal default value is recommended.

VLP: Internal default value is recommended.

VLN_OUT: Internal default value is recommended.

VLN_AMP: Internal default value is recommended.

VREF: Internal default value is recommended.

ADC Calibration

The MT9V403 contains a special self-calibrating circuitry that enables it to reduce its own column-wise fixed-pattern noise. This calibration process consists of connecting a calibration signal to each of the 167 ADC inputs and estimating and storing these 167 offsets (as 7 bits) to subtract from subsequent samples. Self-calibration automatically occurs after global logic reset (LRST_N) or the two-wire serial interface (register 12), and programs new offset values for each ADC into calibration memory. These values may be different from those calculated in the previous calibration if there has been a change in environment (e.g., temperature). The accuracy of calibration is approximately $1mV_{rms}$.

Table 7: Pixel Gain Matrix

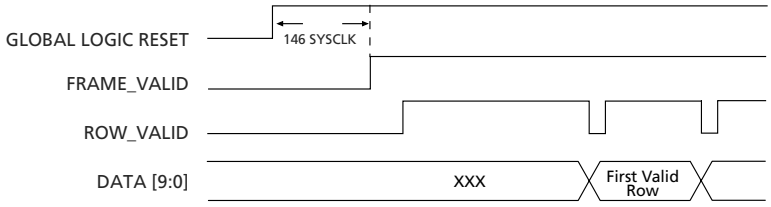
Registers 43-46	Register 53	Total Gain
0000 0001	0	1.0
0000 0010	0	2.0
0000 0011	0	3.0
0000 0100	0	4.0
0000 0101	0	5.0
0000 0110	0	6.0
0000 0111	0	7.
0000 1000	0	8.0
0000 1001	0	9.0
0000 1010	0	10.0
0000 1011	0	11.0
0000 1100	0	12.0
0000 1101	0	13.0
0000 1110	0	14.0
0000 1111	0	15.0
0001 0000	0	16.0
0001 0001	0	17.0
0001 0010	0	18.0
0000 0001	1	0.5
0000 0010	1	1.0
0000 0011	1	1.5
0000 0100	1	2.0
0000 0101	1	2.5
0000 0110	1	3.0
0000 0111	1	3.5
0000 1000	1	4.0
0000 1001	1	4.5
0000 1010	1	5.0
0000 1011	1	5.5
0000 1100	1	6.0
0000 1101	1	6.5
0000 1110	1	7.0
0000 1111	1	7.5
0001 0000	1	8.0
0001 0001	1	8.5
0001 0010	1	9.0

ADC calibration takes 146 SYSCLK cycles. Nominally, calibration should be initiated through the application of LRST_N, in which case the calibration takes place upon release of the LRST_N. Some applications may require initiating calibration by asynchronously writing a one- to two-wire serial interface to register 12, in which case the calibration is delayed until the beginning of the next frame. Calibration will continue to occur every frame until a zero is written to register 12. A timing diagram for the two-wire serial interface initiated calibration is shown in Figure 28.

In master mode and snapshot mode, during two-wire serial interface initiated calibration, ROW_VALID goes HIGH for 146 SYSCLK immediately after FRAME_VALID goes HIGH to indicate that the calibration process is occurring. The output of the sensor is

interrupted during the calibration process to prevent output noise from corrupting the calibration. After the calibration process is complete, ROW_VALID goes LOW and the normal data readout process commences when it returns HIGH. For two-wire serial interface initiated calibration in slave mode, the first ROW_STRT pulse of the calibration frame initiates the 146 SYSCLK calibration process. It is suggested that the user hold LD_SHFT_N HIGH during this calibration process to minimize calibration noise. When the calibration is complete, LD_SHFT_N may be lowered to commence the normal frame readout process.

Figure 28: Two-Wire Serial Interface Initiated Calibration



The calibration coefficients can be read from the MT9V403 and written to it, making it possible to further reduce column-wise fixed pattern noise by externally calculating and writing the proper offset values to the MT9V403. For example, the user may choose to calculate the more precise offset values by averaging several frames and uploading the coefficients to the MT9V403. The user may also calculate coefficients for several temperature values and upload the appropriate values based on the environment.

A special write-only two-wire serial interface register (register 15) is dedicated to the calibration data input. Calibration data can be continuously written to this register with an eight-bit write. To write to the calibration register, the typical two-wire serial interface write sequence is adhered to, including address (register 15), followed by 167 eight-bit transfers (note that each coefficient utilizes the 7 LSBs of the eight-bit two-wire serial interface word). This writing process must be continuous (ADC 1 to ADC 167) and coefficients cannot be selectively written.

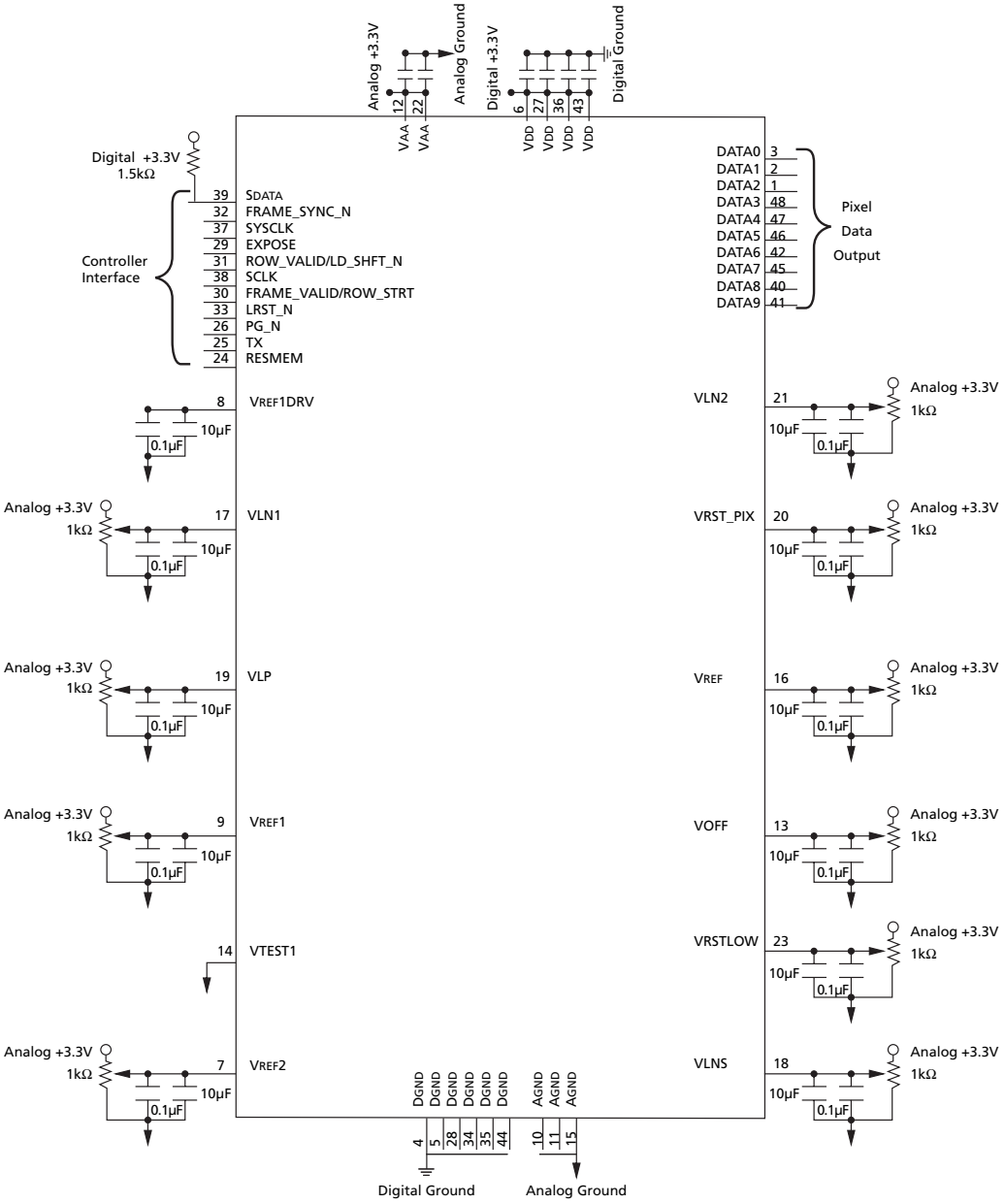
In a similar manner, a special read-only two-wire serial interface register (register 143) is dedicated to calibration data output. Calibration data can be continuously read from this register with an 8-bit read. To read from the calibration register, the typical two-wire serial interface write sequence is adhered to, including address (register 143), followed by 167 8-bit transfers (note that each coefficient utilizes the 7 LSBs of the eight-bits two-wire serial interface word). This reading process must be continuous (ADC 1 to ADC 167) and coefficients cannot be selectively read.

Note: The first calibration coefficient is always equal to zero.

Anti-Eclipse Circuit

The MT9V403 includes a pixel memory reset pulse duration control. This control enables a mode where the reset of the pixel is held for a longer period of time. This can be implemented by setting bit 0 to 7 in register 13. In some extremely bright lighting conditions, this extended reset may prevent the eclipse-like phenomena (black spots on a bright background) to which some CMOS sensors are prone.

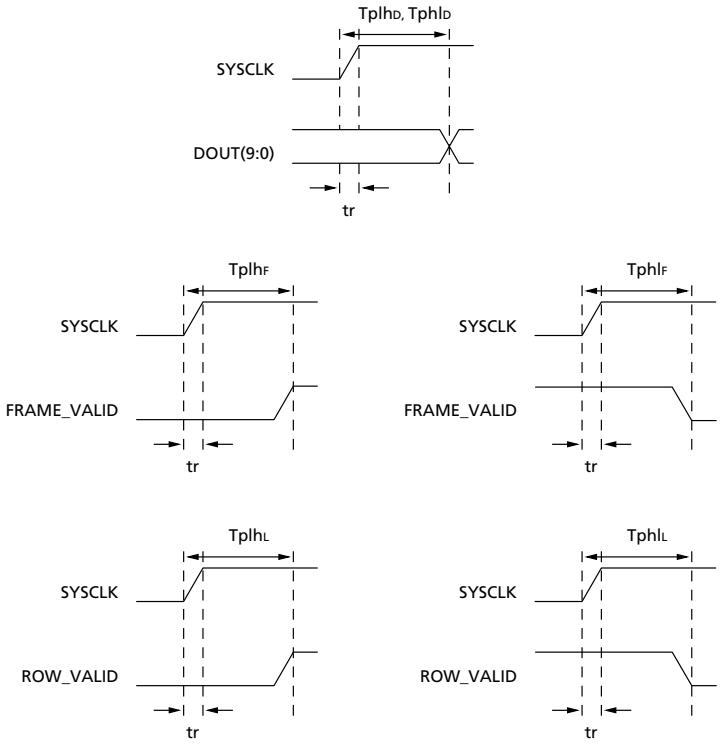
Figure 29: Board Connections



Notes: 1. VLN1, VLP, VOFF, VREF, VREF1, VLN2, and VREF2 are generated on-chip, but user may disable internal bias (via two-wire serial interface) and apply external voltages to sensor. VREF1DRV is generated on chip but its internal bias cannot be disabled. VRST_PIX and VRSTLOW are not generated internally and external voltages must be applied.

2. All bias pins should be decoupled with 0.1µF ceramic and 10µF electrolytic capacitors. (Please see board connections.) Capacitors should be placed as physically close as possible to the MT9V403 package.
3. Digital outputs can drive standard CMOS circuits with 30pF load, but less load capacitance results in less substrate noise on-chip. This is recommended to minimize load capacitance for better noise performance.

Figure 30: Propagation Delays for Data Output, Frame Valid, and Row Valid Signals



Electrical Specifications

Table 8: AC Electrical Characteristics
V_{PWR} = 3.3 ±0.3V; T_A = 25°C

Symbol	Definition	Condition	Min	Typ	Max	Unit
$^tPLH_D$	Data output propagation delay for LOW-to-HIGH transition	C_{LOAD} = 10pF		2		ns
$^tPHL_D$	Data output propagation delay for HIGH-to-LOW transition	C_{LOAD} = 10pF		2		ns
$^tPLH_L$	ROW_VALID propagation delay for LOW-to-HIGH transition	C_{LOAD} = 10pF		2		ns
$^tPHL_L$	ROW_VALID propagation delay for HIGH-to-LOW transition	C_{LOAD} = 10pF		2		ns
$^tPLH_F$	FRAME_VALID propagation delay for LOW-to-HIGH transition	C_{LOAD} = 10pF		2		ns
$^tPHL_F$	FRAME_VALID propagation delay for HIGH-to-LOW transition	C_{LOAD} = 10pF		2		ns

Table 9: DC Electrical Characteristics
V_{PWR} = 3.3 ±0.3V; T_A = 25°C

Symbol	Definition	Condition	Min	Typ[1]	Max	Unit
VLN_AMP		Internal/External	0.5	Internal (0.7)	1.5	V
VLN2		Internal/External	0.5	Internal (1.1)	1.5	V
VLN_OUT		Internal/External	0.5	Internal (0.8)	1.5	V
VLN1		Internal/External	0.5	Internal (0.7)	1.5	V
VLP		Internal/External	1.5	Internal (1.9)	2.5	V
V_{REF}		Internal/External	1	Internal (1.6)	2	V
V_{REF2}		Internal/External	0	Internal (1)	2	V
V_{REF1}		Internal/External	0	Internal (1)	2	V
VOFF		Internal/External	0	Internal (0)	3	V
VRST_PIX		External Only	1	2.5	3.3	V
VRSTLOW		External Only	0	0 – 0.4	1	V
VTEST		External Only	—	0	—	
$V_{REF1DRV}$		Internal Only	—	open	—	V
V_{IH}	Input High Voltage		2.5		V_{PWR} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IN}	Input Leakage Current	No Pull-up Resistor; V_{IN} - V_{PWR} or V_{GND}	-300		+300	uA
V_{OH}	Output High Voltage		V_{PWR} - 0.2			V
V_{OL}	Output Low Voltage		100		220	mV
I_{OH}	Output High Current				0.2	mA
I_{PWR}	Supply Current	CLKIN = 42 MHz; default setting		20		mA

Note: [1]Where indicated, internally generated biases are typically utilized. The parenthetical number indicates typical value if external voltage is applied.
This device contains circuitry to protect the inputs against damage from high static voltages or electric fields, but the user is advised to take precautions to avoid the application of any voltage higher than the maximum rated.

Two-Wire Serial Bus Timing

The two-wire serial bus operation requires a certain minimum number of master clock cycles between transitions. These are specified below in master clock cycles.

Figure 31: Serial Host Interface Start Condition Timing

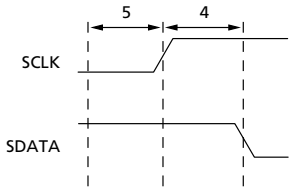
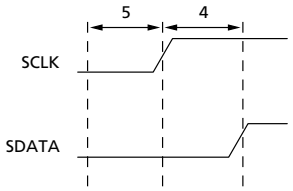
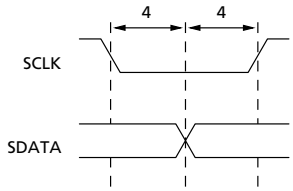


Figure 32: Serial Host Interface Stop Condition Timing



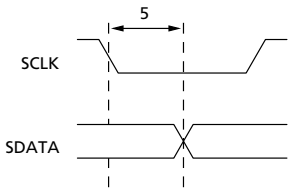
Note: All timing are in units of master clock cycle.

Figure 33: Serial Host Interface Data Timing for Write



Note: SDATA is driven by an off-chip transmitter.

Figure 34: Serial Host Interface Data Timing for Read



Note: SDATA is pulled LOW by the sensor, or allowed to be pulled HIGH by a pull-up resistor off-chip.

Figure 35: Acknowledge Signal Timing After an 8-Bit Write from Sensor

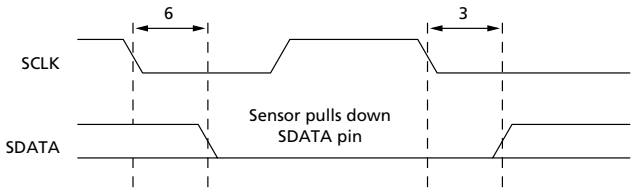
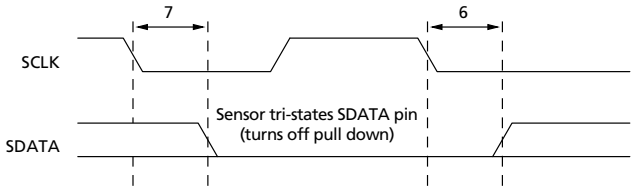


Figure 36: Acknowledge Signal Timing After an 8-Bit Read to Sensor



Note: After a read, the master receiver must pull down SDATA to acknowledge receipt of data bits. When read sequence is complete, the master must generate a no acknowledge by leaving SDATA to float HIGH. On the following cycle, a start or stop bit may be used.

Table 10: Image Sensor Characteristics
T_A = 25°C

Symbol	Parameter	Typ	Unit
^{R}I	Responsivity (ADC $V_{REF}1$ = 1V)	1,800	LSB/lux-sec.
DSNU	Dark signal non-uniformity	0.5	%rms
V_{DRK}	Output referred dark signal	100	mV/sec
Dyn_I	Internal dynamic range	60	dB
PRNU	Photo response non-uniformity	1	%rms
N_{SAT}	Pixel saturation level	110,000	electrons
NE	Input referred noise: Overlapped conversion and digital readout (200 fps)	98	electrons
K_{DRK}	Dark current temperature coefficient	100	%/8°C

Table 11: Pixel Array

Symbol	Parameter	Typ	Unit
Resolution	Number of pixels in active image	659 x 494	pixels
Pixel Size	X-Y dimensions	9.9	µm
Pixel Pitch	Center-to-center pixel spacing	9.9	µm
Pixel Fill Factor	Area of drawn active area	50	%
Shutter Efficiency	Equals: 1-(leakage into in pixel memory)	98.5	%

Figure 37: Quantum Efficiency—Monochrome

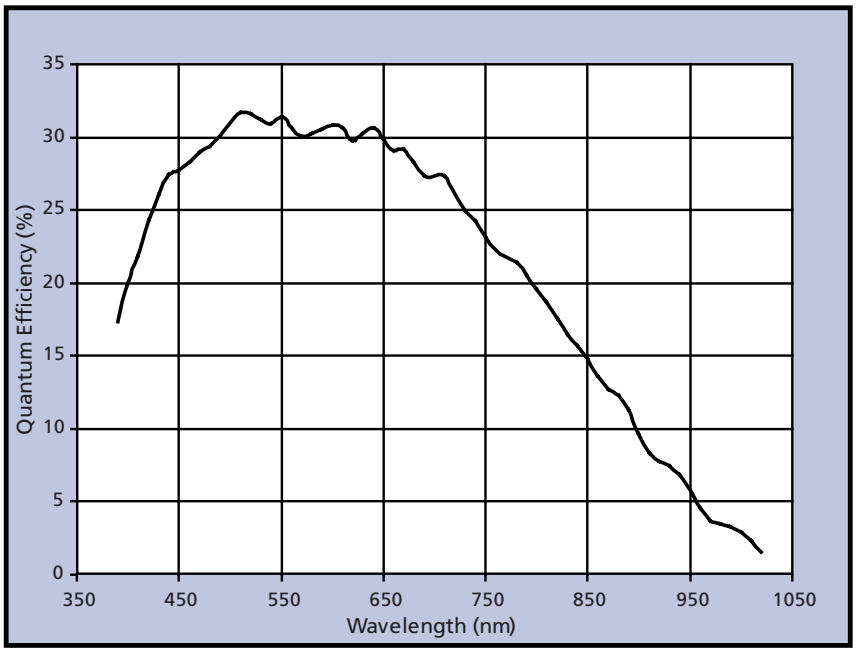


Figure 38: Quantum Efficiency—Color

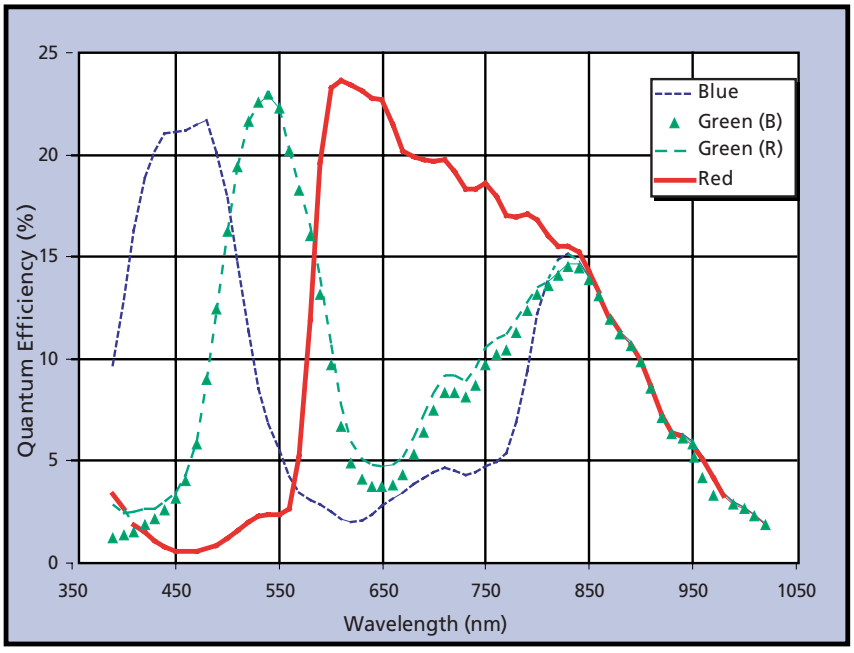
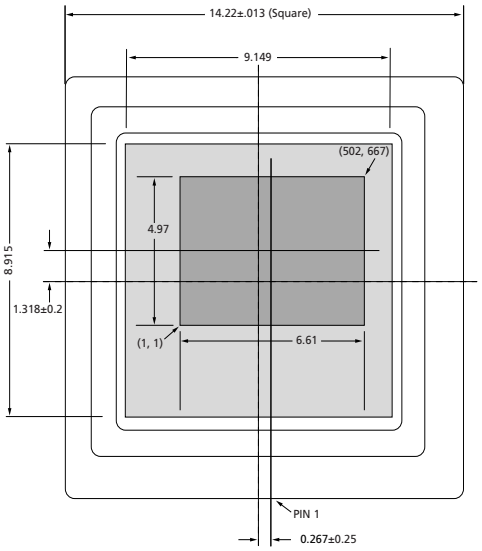
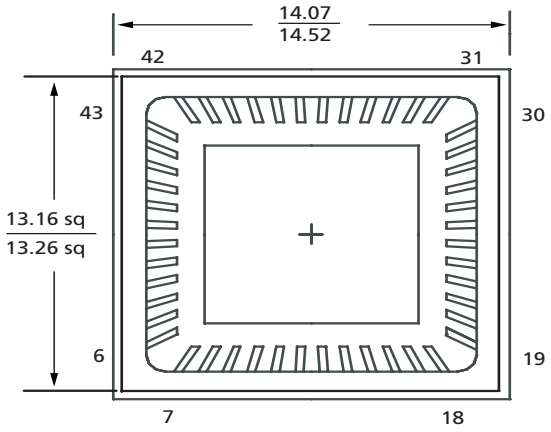


Figure 39: Pixel Array Offset Drawing



Note: 1. All dimensions are in millimeters.
2. Tolerance on die placement is ±0.25mm.
3. Rotation < ±2°.
4. Tilt ±2 mils.

Figure 40: Package Drawing – Top View



Notes: 1. Dimensions in mm.
2. $\frac{\text{MAX}}{\text{MIN}}$

Figure 41: Package View – Bottom View

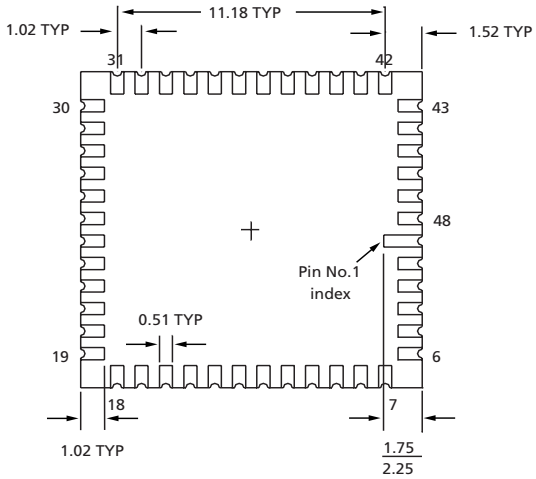
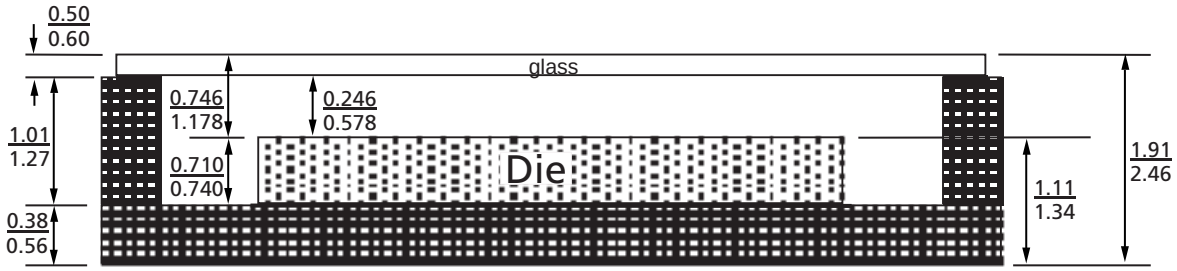


Figure 42: Package Drawing - Side View



Notes: 1. Dimensions in millimeters.
2. Borosilicate: glass with refractive index: 1.52nm at 546nm.
3. $\frac{\text{MAX}}{\text{MIN}}$

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Revision History

Rev C, 7/05

- Added Table of Contents, List of Figures, and List of Tables
- Added Table 1, Key Performance Parameters, on page 1
- Update Table 2, Pin Description, on page 6
- Update "Simultaneous Master Mode" on page 11
- Update Figure 13, Simultaneous Slave Mode Row Timing Diagram Example (Default Settings), on page 15
- Update Figure 15, Sequential Slave Mode Row Timing Diagram Example, on page 16
- Update "Serial Bus Description" on page 18
- Update Table 5, Complete Register Description, on page 21, Registers 10, 12 and 13
- Update "Window Location and Size" on page 24
- Update Figure 25, Row Timing for Slave Mode with Windowing, on page 25
- Update "Considerations when Setting Analog Voltages" on page 28
- Update "ADC Calibration" on page 28
- Update Table 8, AC Electrical Characteristics, on page 33
- Update Table 9, DC Electrical Characteristics, on page 33

Rev B, Preliminary, 1/04

- Removed Preliminary Status
- Updated Figure 13
- Updated I_{IN} Input Leakage current specifications in the DC Characteristics Table
- Added high-static note to DC Characteristics Table

Rev A, Preliminary, 8/03

- Original Release