

Polyphase Metering SoCs

FEATURES

- Accuracy < 0.1% Over 2000:1 Dynamic Range for Phase Current
- Meets or Exceeds ANSI C12.20 and IEC 62053 Standards
- Support for Multiple Sensors Such as Current Transformers, Rogowski Coils, or Shunts
- Power Measurement for up to Three Phases Plus Neutral
- Dedicated Pulse Output Pins for Active and Reactive Energy for Calibration
- Four-Quadrant Measurement per Phase or Cumulative
- Exact Phase Angle Measurements
- Digital Phase Correction for Current Transformers
- Temperature Compensated Energy Measurements
- 40-Hz to 70-Hz Line Frequency Range Using Single Calibration
- Flexible Power Supply Options With Automatic Switching
- Display Operates at Very Low Power During AC Mains Failure: 3 μ A in LPM3
- LCD Driver With Contrast Control for up to 320 Segments
- Password-Protected Real-Time Clock With Crystal Offset Calibration and Temperature Compensation
- Integrated Security Modules to Support Anti-Tamper
- Multiple Communication Interfaces for Smart Meter Implementations
- High-Performance 25-MHz CPU With 32-Bit Multiplier
- Wide Input Supply Voltage Range: 3.6 V Down to 1.8 V
- Ultra-Low-Power Consumption During Energy Measurement
 - 2.9 mW at 10-MHz Operation (3 V)
- Multiple Low-Power Modes
 - Standby Mode (LPM3): 2.1 μ A at 3 V, Wake Up in Less Than 5 μ s
 - RTC Mode (LPM3.5): 0.34 μ A at 3 V
 - Shutdown Mode (LPM4.5): 0.18 μ A at 3 V
- Up to 512KB of Single-Cycle Flash
- Up to 32KB of RAM With Single-Cycle Access
- Up to Seven Independent 24-Bit Sigma-Delta ADCs With Differential Inputs and Variable Gain
- System 10-Bit 200-kps ADC
 - Six Channels Plus Supply and Temperature Sensor Measurement
- Six Enhanced Communications Ports
 - Configurable Among Four UART, Six SPI, and Two I²C Interfaces
- Four 16-Bit Timers With Nine Total Capture/Compare Registers
- 128-Pin LQFP (PEU) Package With 90 I/O Pins
- 100-Pin LQFP (PZ) Package With 62 I/O Pins
- Industrial Temperature Range of –40°C to 85°C
- 3-Phase Electronic Watt-Hour Meter Development Tools
 - [EVM430-F6779](#) With [SLAA577](#) App Note
 - [MSP430™ Energy Library](#)
- For Complete Module Descriptions, See the *MSP430x5xx and MSP430x6xx Family User's Guide (SLAU208)*

APPLICATIONS

- 3-Phase Electronic Watt-Hour Meters
- Utility Metering
- Energy Monitoring



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DESCRIPTION

The Texas Instruments MSP430F677x1 family of polyphase metering SoCs are powerful highly integrated solutions for revenue meters that offer accuracy and low system cost with few external components. The F677x1 family of devices uses the low-power MSP430 CPU with a 32-bit multiplier to perform all energy calculations, metering applications such as tariff rate management, and communications with AMR and AMI modules.

The F677x1 devices feature TI's 24-bit sigma-delta converter technology, which provides better than 0.1% accuracy. Family members include up to 512KB of flash, 32KB of RAM, and an LCD controller with support for up to 320 segments.

The ultra-low-power nature of the F677x1 devices means that the system power supply can be minimized to reduce overall cost. Lowest standby power means that backup energy storage can be minimized and critical data retained longer in case of a mains power failure.

The F677x1 family of devices executes the TI energy measurement software library, which calculates all relevant energy and power results. The energy measurement software library is available with the F677x1 devices at no cost. Industry standard development tools and hardware platforms are available to speed development of meters that meet all of the ANSI and IEC standards globally.

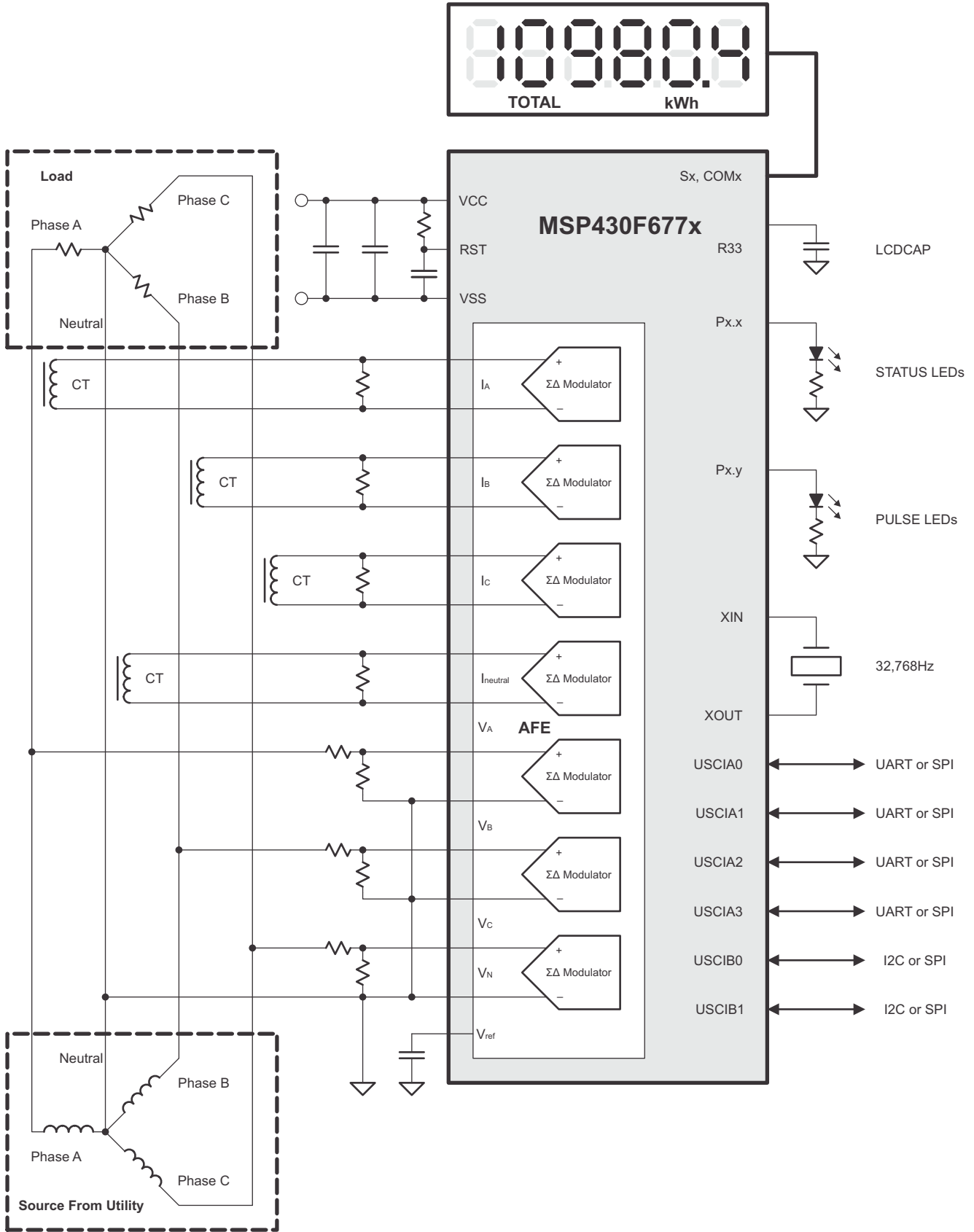


Figure 1. 3-Phase 4-Wire Star Connection Using MSP430F677x1

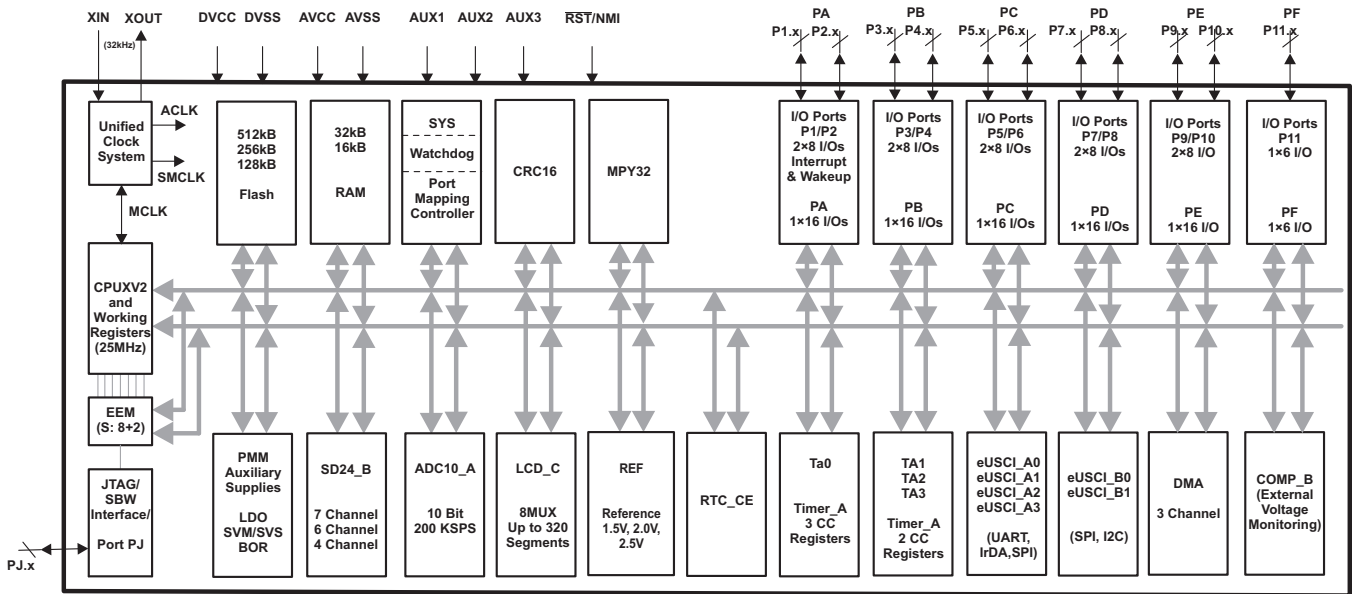
Family members available are summarized in [Table 1](#).

Table 1. Family Members⁽¹⁾⁽²⁾

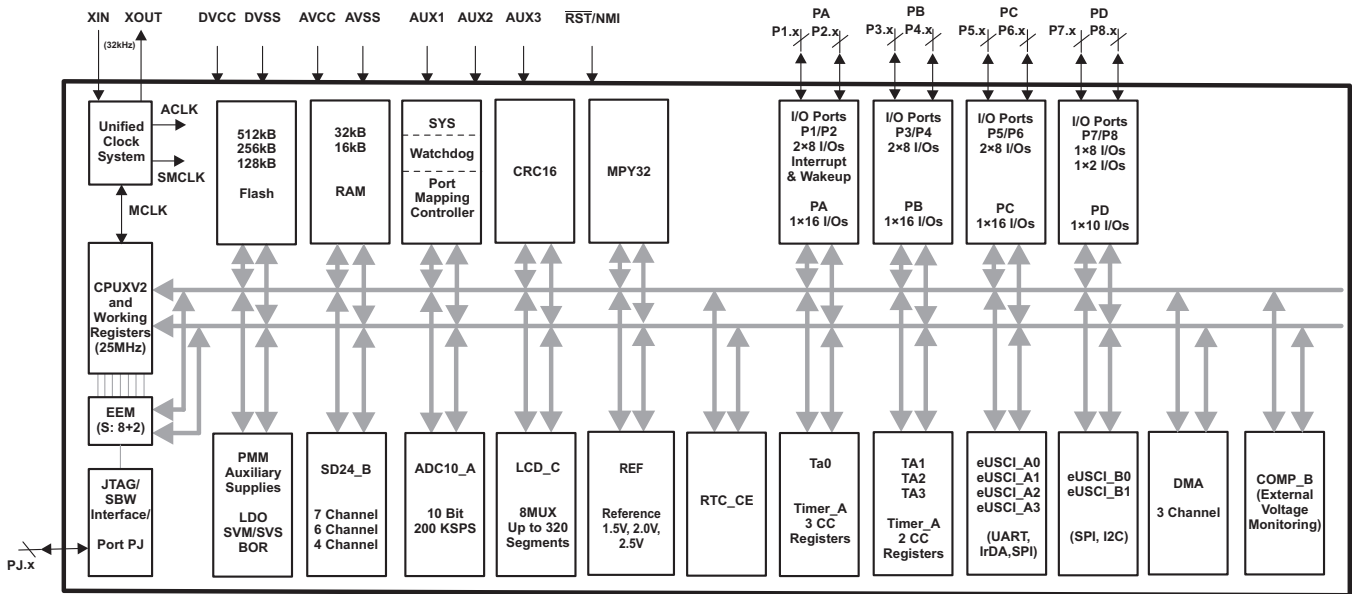
| Device | Flash (KB) | SRAM (KB) | SD24_B Converters | ADC10_A Channels | Timer_A ⁽³⁾ | eUSCI | | I/O | Package Type |
|-----------------|------------|-----------|-------------------|------------------|------------------------|----------------------------|----------------------------------|-----|--------------|
| | | | | | | Channel A: UART, IrDA, SPI | Channel B: SPI, I ² C | | |
| MSP430F67791PEU | 512 | 32 | 7 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 90 | 128 PEU |
| MSP430F67781PEU | 512 | 16 | 7 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 90 | 128 PEU |
| MSP430F67771PEU | 256 | 32 | 7 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 90 | 128 PEU |
| MSP430F67761PEU | 256 | 16 | 7 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 90 | 128 PEU |
| MSP430F67751PEU | 128 | 16 | 7 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 90 | 128 PEU |
| MSP430F67691PEU | 512 | 32 | 6 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 90 | 128 PEU |
| MSP430F67681PEU | 512 | 16 | 6 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 90 | 128 PEU |
| MSP430F67671PEU | 256 | 32 | 6 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 90 | 128 PEU |
| MSP430F67661PEU | 256 | 16 | 6 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 90 | 128 PEU |
| MSP430F67651PEU | 128 | 16 | 6 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 90 | 128 PEU |
| MSP430F67491PEU | 512 | 32 | 4 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 90 | 128 PEU |
| MSP430F67481PEU | 512 | 16 | 4 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 90 | 128 PEU |
| MSP430F67471PEU | 256 | 32 | 4 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 90 | 128 PEU |
| MSP430F67461PEU | 256 | 16 | 4 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 90 | 128 PEU |
| MSP430F67451PEU | 128 | 16 | 4 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 90 | 128 PEU |
| MSP430F67791PZ | 512 | 32 | 7 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 62 | 100 PZ |
| MSP430F67781PZ | 512 | 16 | 7 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 62 | 100 PZ |
| MSP430F67771PZ | 256 | 32 | 7 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 62 | 100 PZ |
| MSP430F67761PZ | 256 | 16 | 7 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 62 | 100 PZ |
| MSP430F67751PZ | 128 | 16 | 7 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 62 | 100 PZ |
| MSP430F67691PZ | 512 | 32 | 6 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 62 | 100 PZ |
| MSP430F67681PZ | 512 | 16 | 6 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 62 | 100 PZ |
| MSP430F67671PZ | 256 | 32 | 6 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 62 | 100 PZ |
| MSP430F67661PZ | 256 | 16 | 6 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 62 | 100 PZ |
| MSP430F67651PZ | 128 | 16 | 6 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 62 | 100 PZ |
| MSP430F67491PZ | 512 | 32 | 4 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 62 | 100 PZ |
| MSP430F67481PZ | 512 | 16 | 4 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 62 | 100 PZ |
| MSP430F67471PZ | 256 | 32 | 4 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 62 | 100 PZ |
| MSP430F67461PZ | 256 | 16 | 4 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 62 | 100 PZ |
| MSP430F67451PZ | 128 | 16 | 4 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 62 | 100 PZ |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
- (3) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.

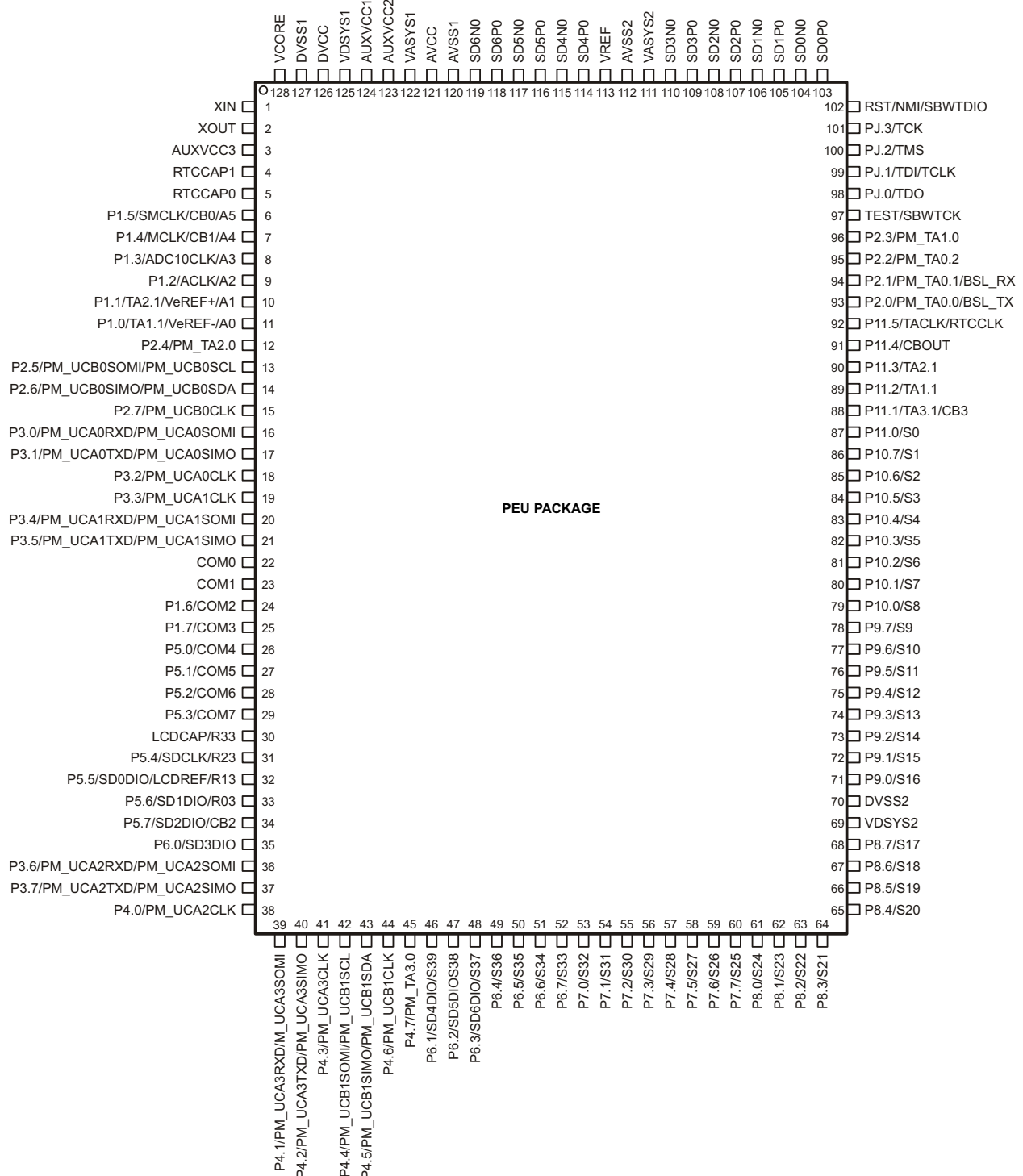
Functional Block Diagram – MSP430F677x1IPEU, MSP430F676x1IPEU, and MSP430F674x1IPEU



Functional Block Diagram – MSP430F677x1IPZ, MSP430F676x1IPZ, and MSP430F674x1IPZ



Pin Designation, MSP430F677x1IPEU

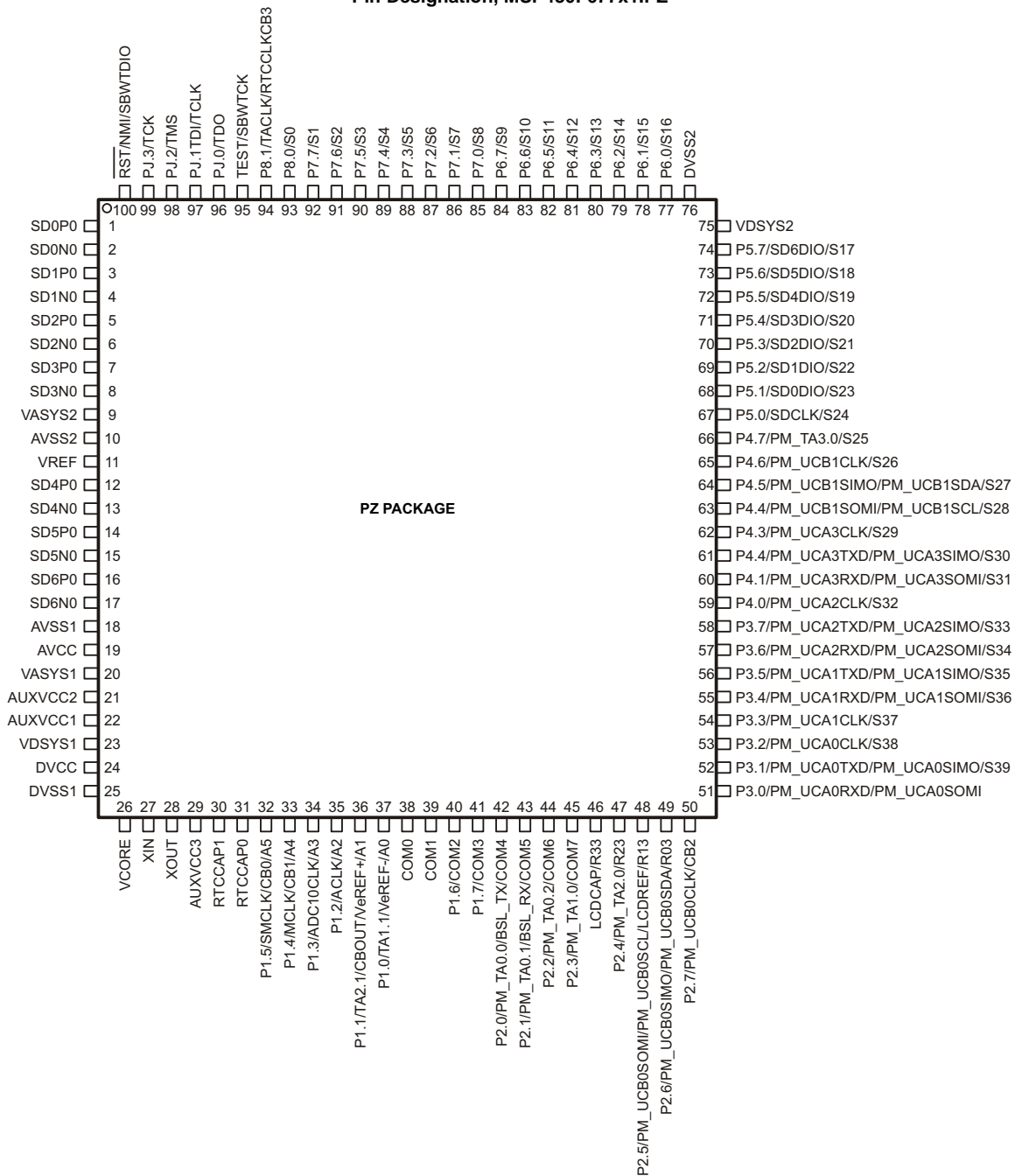


- A. The secondary digital functions on Ports P2, P3 and P4 are fully mappable. The pin designation shows only the default mapping. See [Table 15](#) for details.
- B. The pair of pins VDSYS1 and VDSYS2, VASYS1 and VASYS2 must be connected externally on board for proper device operation.
- C. **CAUTION:** The LDCAP/R33 pin must be connected to DVSS if it is not used.

Table 2. Pinout Differences for MSP430F677x1IPEU, MSP430F676x1IPEU, and MSP430F674x1IPEU

| PIN NUMBER | PIN NAME | | |
|---------------|------------------|------------------|------------------|
| | MSP430F677x1IPEU | MSP430F676x1IPEU | MSP430F674x1IPEU |
| 46 | P6.1/SD4DIO/S39 | P6.1/SD4DIO/S39 | P6.1/S39 |
| 47 | P6.2/SD5DIO/S38 | P6.2/SD5DIO/S38 | P6.2/S38 |
| 48 | P6.3/SD6DIO/S37 | P6.3/S37 | P6.3/S37 |
| 113 | VREF | VREF | VREF |
| 114 | SD4P0 | SD4P0 | NC |
| 115 | SD4N0 | SD4N0 | NC |
| 116 | SD5P0 | SD5P0 | NC |
| 117 | SD5N0 | SD5N0 | NC |
| 118 | SD6P0 | NC | NC |
| 119 | SD6N0 | NC | NC |

Pin Designation, MSP430F677x1IPZ



- D. The secondary digital functions on Ports P2, P3 and P4 are fully mappable. The pin designation shows only the default mapping. See [Table 15](#) for details.
- E. The pair of pins VDSYS1 and VDSYS2, VASYS1 and VASYS2 must be connected externally on board for proper device operation.
- F. **CAUTION:** The LDCAP/R33 pin must be connected to DVSS if it is not used.

Table 3. Pinout Differences for MSP430F677x1IPZ, MSP430F676x1IPZ, and MSP430F674x1IPZ

| PIN NUMBER | PIN NAME | | |
|---------------|-----------------|-----------------|-----------------|
| | MSP430F677x1IPZ | MSP430F676x1IPZ | MSP430F674x1IPZ |
| 11 | VREF | VREF | VREF |
| 12 | SD4P0 | SD4P0 | NC |
| 13 | SD4N0 | SD4N0 | NC |
| 14 | SD5P0 | SD5P0 | NC |
| 15 | SD5N0 | SD5NO | NC |
| 16 | SD6P0 | NC | NC |
| 17 | SD6N0 | NC | NC |
| 72 | P5.5/SD4DIO/S19 | P5.5/SD4DIO/S19 | P5.5/S19 |
| 73 | P5.6/SD5DIO/S18 | P5.6/SD5DIO/S18 | P5.6/S18 |
| 74 | P5.7/SD6DIO/S17 | P5.7/S17 | P5.7/S17 |

Table 4. Terminal Functions – PEU Package

| TERMINAL | | I/O ⁽¹⁾ | DESCRIPTION |
|---------------------------------|------------|--------------------|---|
| NAME | NO. PEU | | |
| XIN | 1 | I/O | Input terminal for crystal oscillator |
| XOUT | 2 | I/O | Output terminal for crystal oscillator |
| AUXVCC3 | 3 | | Auxiliary power supply AUXVCC3 for back up subsystem |
| RTCCAP1 | 4 | I | External time capture pin 1 for RTC_C |
| RTCCAP0 | 5 | I | External time capture pin 0 for RTC_C |
| P1.5/SMCLK/CB0/A5 | 6 | I/O | General-purpose digital I/O with port interrupt SMCLK clock output Comparator_B input CB0 Analog input A5 - 10-bit ADC |
| P1.4/MCLK/CB1/A4 | 7 | I/O | General-purpose digital I/O with port interrupt MCLK clock output Comparator_B input CB1 Analog input A4 - 10-bit ADC |
| P1.3/ADC10CLK/A3 | 8 | I/O | General-purpose digital I/O with port interrupt ADC10_A clock output Analog input A3 - 10-bit ADC |
| P1.2/ACLK/A2 | 9 | I/O | General-purpose digital I/O with port interrupt ACLK clock output Analog input A2 - 10-bit ADC |
| P1.1/TA2.1/VeREF+/A1 | 10 | I/O | General-purpose digital I/O with port interrupt Timer TA2 CCR1 capture: CCI1A input, compare: Out1 output Positive terminal for the ADC's reference voltage for an external applied reference voltage Analog input A1 - 10-bit ADC |
| P1.0/TA1.1/VeREF-/A0 | 11 | I/O | General-purpose digital I/O with port interrupt Timer TA1 CCR1 capture: CCI1A input, compare: Out1 output Negative terminal for the ADC's reference voltage for an external applied reference voltage Analog input A0 - 10-bit ADC |
| P2.4/PM_TA2.0 | 12 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: Timer TA2 capture CCR0: CCI0A input, compare: Out0 output |
| P2.5/PM_UCB0SOMI/ PM_UCB0SCL | 13 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: eUSCI_B0 SPI slave out master in Default mapping: eUSCI_B0 I2C clock |
| P2.6/PM_UCB0SIMO/ PM_UCB0SDA | 14 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: eUSCI_B0 SPI slave in master out Default mapping: eUSCI_B0 I2C data |
| P2.7/PM_UCB0CLK | 15 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: eUSCI_B0 clock input/output |
| P3.0/PM_UCA0RXD/ PM_UCA0SOMI | 16 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: eUSCI_A0 UART receive data Default mapping: eUSCI_A0 SPI slave out master in |
| P3.1/PM_UCA0TXD/ PM_UCA0SIMO | 17 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: eUSCI_A0 UART transmit data Default mapping: eUSCI_A0 SPI slave in master out |

(1) I = input, O = output

Table 4. Terminal Functions – PEU Package (continued)

| TERMINAL | | I/O ⁽¹⁾ | DESCRIPTION |
|---------------------------------|------------|--------------------|--|
| NAME | NO. PEU | | |
| P3.2/PM_UCA0CLK | 18 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: eUSCI_A0 clock input/output |
| P3.3/PM_UCA1CLK | 19 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: eUSCI_A1 clock input/output |
| P3.4/PM_UCA1RXD/ PM_UCA1SOMI | 20 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: eUSCI_A1 UART receive data Default mapping: eUSCI_A1 SPI slave out master in |
| P3.5/PM_UCA1TXD/ PM_UCA1SIMO | 21 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: eUSCI_A1 UART transmit data Default mapping: eUSCI_A1 SPI slave in master out |
| COM0 | 22 | O | LCD common output COM0 for LCD backplane |
| COM1 | 23 | O | LCD common output COM1 for LCD backplane |
| P1.6/COM2 | 24 | I/O | General-purpose digital I/O with port interrupt LCD common output COM2 for LCD backplane |
| P1.7/COM3 | 25 | I/O | General-purpose digital I/O with port interrupt LCD common output COM3 for LCD backplane |
| P5.0/COM4 | 26 | I/O | General-purpose digital I/O LCD common output COM4 for LCD backplane |
| P5.1/COM5 | 27 | I/O | General-purpose digital I/O LCD common output COM5 for LCD backplane |
| P5.2/COM6 | 28 | I/O | General-purpose digital I/O LCD common output COM6 for LCD backplane |
| P5.3/COM7 | 29 | I/O | General-purpose digital I/O LCD common output COM7 for LCD backplane |
| LDCAP/R33 | 30 | I/O | LCD capacitor connection Input/output port of most positive analog LCD voltage (V1) CAUTION: This pin must be connected to DVSS if not used. |
| P5.4/SDCLK/R23 | 31 | I/O | General-purpose digital I/O SD24_B bit stream clock input/output Input/Output port of second most positive analog LCD voltage (V2) |
| P5.5/SD0DIO/ LCDREF/R13 | 32 | I/O | General-purpose digital I/O SD24_B converter 0 bit stream data input/output External reference voltage input for regulated LCD voltage Input/Output port of third most positive analog LCD voltage (V3 or V4) |
| P5.6/SD1DIO/R03 | 33 | I/O | General-purpose digital I/O SD24_B converter 1 bit stream data input/output Input/output port of lowest analog LCD voltage (V5) |
| P5.7/SD2DIO/CB2 | 34 | I/O | General-purpose digital I/O SD24_B converter 2 bit stream data input/output Comparator_B input CB2 |
| P6.0/SD3DIO | 35 | I/O | General-purpose digital I/O SD24_B converter 3 bit stream data input/output |

Table 4. Terminal Functions – PEU Package (continued)

| TERMINAL | | I/O ⁽¹⁾ | DESCRIPTION |
|---------------------------------|------------|--------------------|---|
| NAME | NO. PEU | | |
| P3.6/PM_UCA2RXD/ PM_UCA2SOMI | 36 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: eUSCI_A2 UART receive data Default mapping: eUSCI_A2 SPI slave out master in |
| P3.7/PM_UCA2TXD/ PM_UCA2SIMO | 37 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: eUSCI_A2 UART transmit data Default mapping: eUSCI_A2 SPI slave in master out |
| P4.0/PM_UCA2CLK | 38 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: eUSCI_A2 clock input/output |
| P4.1/PM_UCA3RXD/ PM_UCA3SOMI | 39 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: eUSCI_A3 UART receive data Default mapping: eUSCI_A3 SPI slave out master in |
| P4.2/PM_UCA3TXD/ PM_UCA3SIMO | 40 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: eUSCI_A3 UART transmit data Default mapping: eUSCI_A3 SPI slave in master out |
| P4.3/PM_UCA3CLK | 41 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: eUSCI_A3 clock input/output |
| P4.4/PM_UCB1SOMI/ PM_UCB1SCL | 42 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: eUSCI_B1 SPI slave out, master in Default mapping: eUSCI_B1 I2C clock |
| P4.5/PM_UCB1SIMO/ PM_UCB1SDA | 43 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: eUSCI_B1 SPI slave in, master out Default mapping: eUSCI_B1 I2C data |
| P4.6/PM_UCB1CLK | 44 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: eUSCI_B1 clock input/output |
| P4.7/PM_TA3.0 | 45 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: Timer TA3 capture CCR0: CCI0A input, compare: Out0 output |
| P6.1/SD4DIO/S39 | 46 | I/O | General-purpose digital I/O SD24_B converter 4 bit stream data input/output (not available in F674x devices) LCD segment output S39 |
| P6.2/SD5DIO/S38 | 47 | I/O | General-purpose digital I/O SD24_B converter 5 bit stream data input/output (not available in F674x devices) LCD segment output S38 |
| P6.3/SD6DIO/S37 | 48 | I/O | General-purpose digital I/O SD24_B converter 6 bit stream data input/output (not available in F674x, F676x devices) LCD segment output S37 |
| P6.4/S36 | 49 | I/O | General-purpose digital I/O LCD segment output S36 |
| P6.5/S35 | 50 | I/O | General-purpose digital I/O LCD segment output S35 |
| P6.6/S34 | 51 | I/O | General-purpose digital I/O LCD segment output S34 |
| P6.7/S33 | 52 | I/O | General-purpose digital I/O LCD segment output S33 |

Table 4. Terminal Functions – PEU Package (continued)

| TERMINAL | | I/O ⁽¹⁾ | DESCRIPTION |
|-----------------------|------------|--------------------|---|
| NAME | NO. PEU | | |
| P7.0/S32 | 53 | I/O | General-purpose digital I/O LCD segment output S32 |
| P7.1/S31 | 54 | I/O | General-purpose digital I/O LCD segment output S31 |
| P7.2/S30 | 55 | I/O | General-purpose digital I/O LCD segment output S30 |
| P7.3/S29 | 56 | I/O | General-purpose digital I/O LCD segment output S29 |
| P7.4/S28 | 57 | I/O | General-purpose digital I/O LCD segment output S28 |
| P7.5/S27 | 58 | I/O | General-purpose digital I/O LCD segment output S27 |
| P7.6/S26 | 59 | I/O | General-purpose digital I/O LCD segment output S26 |
| P7.7/S25 | 60 | I/O | General-purpose digital I/O LCD segment output S25 |
| P8.0/S24 | 61 | I/O | General-purpose digital I/O LCD segment output S24 |
| P8.1/S23 | 62 | I/O | General-purpose digital I/O LCD segment output S23 |
| P8.2/S22 | 63 | I/O | General-purpose digital I/O LCD segment output S22 |
| P8.3/S21 | 64 | I/O | General-purpose digital I/O LCD segment output S21 |
| P8.4/S20 | 65 | I/O | General-purpose digital I/O LCD segment output S20 |
| P8.5/S19 | 66 | I/O | General-purpose digital I/O LCD segment output S19 |
| P8.6/S18 | 67 | I/O | General-purpose digital I/O LCD segment output S18 |
| P8.7/S17 | 68 | I/O | General-purpose digital I/O LCD segment output S17 |
| VDSYS2 ⁽²⁾ | 69 | | Digital power supply for I/Os |
| DVSS2 | 70 | | Digital ground supply |
| P9.0/S16 | 71 | I/O | General-purpose digital I/O LCD segment output S16 |
| P9.1/S15 | 72 | I/O | General-purpose digital I/O LCD segment output S15 |
| P9.2/S14 | 73 | I/O | General-purpose digital I/O LCD segment output S14 |

(2) The pins VDSYS1 and VDSYS2 must be connected externally on board for proper device operation.

Table 4. Terminal Functions – PEU Package (continued)

| TERMINAL | | I/O ⁽¹⁾ | DESCRIPTION |
|----------------------|------------|--------------------|--|
| NAME | NO. PEU | | |
| P9.3/S13 | 74 | I/O | General-purpose digital I/O LCD segment output S13 |
| P9.4/S12 | 75 | I/O | General-purpose digital I/O LCD segment output S12 |
| P9.5/S11 | 76 | I/O | General-purpose digital I/O LCD segment output S11 |
| P9.6/S10 | 77 | I/O | General-purpose digital I/O LCD segment output S10 |
| P9.7/S9 | 78 | I/O | General-purpose digital I/O LCD segment output S9 |
| P10.0/S8 | 79 | I/O | General-purpose digital I/O LCD segment output S8 |
| P10.1/S7 | 80 | I/O | General-purpose digital I/O LCD segment output S7 |
| P10.2/S6 | 81 | I/O | General-purpose digital I/O LCD segment output S6 |
| P10.3/S5 | 82 | I/O | General-purpose digital I/O LCD segment output S5 |
| P10.4/S4 | 83 | I/O | General-purpose digital I/O LCD segment output S4 |
| P10.5/S3 | 84 | I/O | General-purpose digital I/O LCD segment output S3 |
| P10.6/S2 | 85 | I/O | General-purpose digital I/O LCD segment output S2 |
| P10.7/S1 | 86 | I/O | General-purpose digital I/O LCD segment output S1 |
| P11.0/S0 | 87 | I/O | General-purpose digital I/O LCD segment output S0 |
| P11.1/TA3.1/CB3 | 88 | I/O | General-purpose digital I/O Timer TA3 capture CCR1: CCI1A input, compare: Out1 output Comparator_B input CB3 |
| P11.2/TA1.1 | 89 | I/O | General-purpose digital I/O Timer TA1 capture CCR1: CCI1A input, compare: Out1 output |
| P11.3/TA2.1 | 90 | I/O | General-purpose digital I/O Timer TA2 capture CCR1: CCI1A input, compare: Out1 output |
| P11.4/CBOUT | 91 | I/O | General-purpose digital I/O Comparator_B Output |
| P11.5/TACLK/RTCCLK | 92 | I/O | General-purpose digital I/O Timer clock input TACLK for TA0, TA1, TA2, TA3 RTCCLK clock output |
| P2.0/PM_TA0.0/BSL_TX | 93 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: Timer TA0 capture CCR0: CCI0A input, compare: Out0 output Bootstrap loader: Data transmit |

Table 4. Terminal Functions – PEU Package (continued)

| TERMINAL | | I/O ⁽¹⁾ | DESCRIPTION |
|---|------------|--------------------|---|
| NAME | NO. PEU | | |
| P2.1/PM_TA0.1/BSL_RX | 94 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: Timer TA0 capture CCR1: CCI1A input, compare: Out1 output Bootstrap loader: Data receive |
| P2.2/PM_TA0.2 | 95 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: Timer TA0 capture CCR2: CCI2A input, compare: Out2 output |
| P2.3/PM_TA1.0 | 96 | I/O | General-purpose digital I/O port interrupt and with mappable secondary function Default mapping: Timer TA1 capture CCR0: CCI0A input, compare: Out0 output |
| TEST/SBWTK | 97 | I | Test mode pin – select digital I/O on JTAG pins Spy-Bi-Wire input clock |
| PJ.0/TDO | 98 | I/O | General-purpose digital I/O Test data output |
| PJ.1/TDI/TCLK | 99 | I/O | General-purpose digital I/O Test data input or Test clock input |
| PJ.2/TMS | 100 | I/O | General-purpose digital I/O Test mode select |
| PJ.3/TCK | 101 | I/O | General-purpose digital I/O Test clock |
| $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ | 102 | I/O | Reset input active low ⁽³⁾ Non-maskable interrupt input Spy-By-Wire data input/output |
| SD0P0 | 103 | I | SD24_B positive analog input for converter 0 ⁽⁴⁾ |
| SD0N0 | 104 | I | SD24_B negative analog input for converter 0 ⁽⁴⁾ |
| SD1P0 | 105 | I | SD24_B positive analog input for converter 1 ⁽⁴⁾ |
| SD1N0 | 106 | I | SD24_B negative analog input for converter 1 ⁽⁴⁾ |
| SD2P0 | 107 | I | SD24_B positive analog input for converter 2 ⁽⁴⁾ |
| SD2N0 | 108 | I | SD24_B negative analog input for converter 2 ⁽⁴⁾ |
| SD3P0 | 109 | I | SD24_B positive analog input for converter 3 ⁽⁴⁾ |
| SD3N0 | 110 | I | SD24_B negative analog input for converter 3 ⁽³⁾ |
| VASYS2 | 111 | | Analog power supply selected between AVCC, AUXVCC1, AUXVCC2. Connect recommended capacitor value of C _{VSYS} |
| AVSS2 | 112 | | Analog ground supply |
| VREF | 113 | I | SD24_B external reference voltage |
| SD4P0 | 114 | I | SD24_B positive analog input for converter 4 ⁽⁴⁾ (not available on F674x1 devices) |
| SD4N0 | 115 | I | SD24_B negative analog input for converter 4 ⁽⁴⁾ (not available on F674x1 devices) |
| SD5P0 | 116 | I | SD24_B positive analog input for converter 5 ⁽⁴⁾ (not available on F674x1 devices) |
| SD5N0 | 117 | I | SD24_B negative analog input for converter 5 ⁽⁴⁾ (not available on F674x1 devices) |
| SD6P0 | 118 | I | SD24_B positive analog input for converter 6 ⁽⁴⁾ (not available on F676x1, F674x1 devices) |
| SD6N0 | 119 | I | SD24_B negative analog input for converter 6 ⁽⁴⁾ (not available on F676x1, F674x1 devices) |
| AVSS1 | 120 | | Analog ground supply |

(3) When this pin is configured as reset, the internal pullup resistor is enabled by default.

(4) It is recommended to short unused analog input pairs and connect them to analog ground.

Table 4. Terminal Functions – PEU Package (continued)

| TERMINAL | | I/O ⁽¹⁾ | DESCRIPTION |
|-----------------------|------------|--------------------|--|
| NAME | NO. PEU | | |
| AVCC | 121 | | Analog power supply |
| VASYS1 | 122 | | Analog power supply selected between AVCC, AUXVCC1, AUXVCC2. Connect recommended capacitor value of $C_{V_{SYS}}$ |
| AUXVCC2 | 123 | | Auxiliary power supply AUXVCC2 |
| AUXVCC1 | 124 | | Auxiliary power supply AUXVCC1 |
| VDSYS1 ⁽⁵⁾ | 125 | | Digital power supply selected between DVCC, AUXVCC1, AUXVCC2. Connect recommended capacitor value of $C_{V_{SYS}}$. |
| DVCC | 126 | | Digital power supply |
| DVSS1 | 127 | | Digital ground supply |
| VCORE ⁽⁶⁾ | 128 | | Regulated core power supply (internal use only, no external current loading) |

(5) The pins VDSYS1 and VDSYS2 must be connected externally on board for proper device operation.

(6) VCORE is for internal use only. No external current loading is possible. VCORE should only be connected to the recommended capacitor value, C_{VCORE} .

Table 5. Terminal Functions – PZ Package

| TERMINAL | | I/O ⁽¹⁾ | DESCRIPTION |
|-----------------------|-----------|--------------------|---|
| NAME | NO. PZ | | |
| SD0P0 | 1 | I | SD24_B positive analog input for converter 0 ⁽²⁾ |
| SD0N0 | 2 | I | SD24_B negative analog input for converter 0 ⁽²⁾ |
| SD1P0 | 3 | I | SD24_B positive analog input for converter 1 ⁽²⁾ |
| SD1N0 | 4 | I | SD24_B negative analog input for converter 1 ⁽²⁾ |
| SD2P0 | 5 | I | SD24_B positive analog input for converter 2 ⁽²⁾ |
| SD2N0 | 6 | I | SD24_B negative analog input for converter 2 ⁽²⁾ |
| SD3P0 | 7 | I | SD24_B positive analog input for converter 3 ⁽²⁾ |
| SD3N0 | 8 | I | SD24_B negative analog input for converter 3 ⁽²⁾ |
| VASYS2 | 9 | | Analog power supply selected between AVCC, AUXVCC1, AUXVCC2. Connect recommended capacitor value of C _{VSYS} . |
| AVSS2 | 10 | | Analog ground supply |
| VREF | 11 | I | SD24_B external reference voltage |
| SD4P0 | 12 | I | SD24_B positive analog input for converter 4 ⁽²⁾ (not available on F674x devices) |
| SD4N0 | 13 | I | SD24_B negative analog input for converter 4 ⁽²⁾ (not available on F674x1 devices) |
| SD5P0 | 14 | I | SD24_B positive analog input for converter 5 ⁽²⁾ (not available on F674x1 devices) |
| SD5N0 | 15 | I | SD24_B negative analog input for converter 5 ⁽²⁾ (not available on F674x1 devices) |
| SD6P0 | 16 | I | SD24_B positive analog input for converter 6 ⁽²⁾ (not available on F676x1, F674x1 devices) |
| SD6N0 | 17 | I | SD24_B negative analog input for converter 6 ⁽²⁾ (not available on F676x1, F674x1 devices) |
| AVSS1 | 18 | | Analog ground supply |
| AVCC | 19 | | Analog power supply |
| VASYS1 | 20 | | Analog power supply selected between AVCC, AUXVCC1, AUXVCC2. Connect recommended capacitor value of C _{VSYS} |
| AUXVCC2 | 21 | | Auxiliary power supply AUXVCC2 |
| AUXVCC1 | 22 | | Auxiliary power supply AUXVCC1 |
| VDSYS1 ⁽³⁾ | 23 | | Digital power supply selected between DVCC, AUXVCC1, AUXVCC2. Connect recommended capacitor value of C _{VSYS} . |
| DVCC | 24 | | Digital power supply |
| DVSS1 | 25 | | Digital ground supply |
| VCORE ⁽⁴⁾ | 26 | | Regulated core power supply (internal use only, no external current loading) |
| XIN | 27 | I/O | Input terminal for crystal oscillator |
| XOUT | 28 | I/O | Output terminal for crystal oscillator |
| AUXVCC3 | 29 | | Auxiliary power supply AUXVCC3 for back up subsystem |
| RTCCAP1 | 30 | I | External time capture pin 1 for RTC_C |
| RTCCAP0 | 31 | I | External time capture pin 0 for RTC_C |
| P1.5/SMCLK/CB0/A5 | 32 | I/O | General-purpose digital I/O with port interrupt SMCLK clock output Comparator_B input CB0 Analog input A5 - 10-bit ADC |
| P1.4/MCLK/CB1/A4 | 33 | I/O | General-purpose digital I/O with port interrupt MCLK clock output Comparator_B input CB1 Analog input A4 - 10-bit ADC |

(1) I = input, O = output

(2) It is recommended to short unused analog input pairs and connect them to analog ground.

(3) The pins VDSYS1 and VDSYS2 must be connected externally on board for proper device operation.

(4) VCORE is for internal use only. No external current loading is possible. VCORE should only be connected to the recommended capacitor value, C_{VCORE}.

Table 5. Terminal Functions – PZ Package (continued)

| TERMINAL | | I/O ⁽¹⁾ | DESCRIPTION |
|--------------------------------|-----------|--------------------|--|
| NAME | NO. PZ | | |
| P1.3/ADC10CLK/A3 | 34 | I/O | General-purpose digital I/O with port interrupt ADC10_A clock output Analog input A3 - 10-bit ADC |
| P1.2/ACLK/A2 | 35 | I/O | General-purpose digital I/O with port interrupt ACLK clock output Analog input A2 - 10-bit ADC |
| P1.1/TA2.1/CBOUT/ VeREF+/A1 | 36 | I/O | General-purpose digital I/O with port interrupt Timer TA2 CCR1 capture: CCI1A input, compare: Out1 output Comparator_B Output Positive terminal for the ADC reference voltage for an external applied reference voltage Analog input A1 - 10-bit ADC |
| P1.0/TA1.1/VeREF-/A0 | 37 | I/O | General-purpose digital I/O with port interrupt Timer TA1 CCR1 capture: CCI1A input, compare: Out1 output Negative terminal for the ADC's reference voltage for an external applied reference voltage Analog input A0 - 10-bit ADC |
| COM0 | 38 | I/O | LCD common output COM0 for LCD backplane |
| COM1 | 39 | I/O | LCD common output COM1 for LCD backplane |
| P1.6/COM2 | 40 | I/O | General-purpose digital I/O with port interrupt LCD common output COM2 for LCD backplane |
| P1.7/COM3 | 41 | I/O | General-purpose digital I/O with port interrupt LCD common output COM3 for LCD backplane |
| P2.0/PM_TA0.0/ BSL_TX/COM4 | 42 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default Mapping: Timer TA0 CCR0 capture: CCI0A input, compare: Out0 output Bootstrap loader: Data transmit LCD common output COM4 for LCD backplane |
| P2.1/PM_TA0.1/ BSL_RX/COM5 | 43 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default Mapping: Timer TA0 CCR1 capture: CCI1A input, compare: Out1 output Bootstrap loader: Data receive LCD common output COM5 for LCD backplane |
| P2.2/PM_TA0.2/COM6 | 44 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default Mapping: Timer TA0 CCR0 capture: CCI2A input, compare: Out2 output LCD common output COM6 for LCD backplane |
| P2.3/PM_TA1.0/COM7 | 45 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default Mapping: Timer TA1 CCR0 capture: CCI0A input, compare: Out0 output LCD common output COM7 for LCD backplane |
| LDCAP/R33 | 46 | I/O | LCD capacitor connection Input/output port of most positive analog LCD voltage (V1) CAUTION: This pin must be connected to DVSS if not used. |
| P2.4/PM_TA2.0/R23 | 47 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default Mapping: Timer TA2 CCR0 capture: CCI0A input, compare: Out0 output Input/Output port of second most positive analog LCD voltage (V2) |

Table 5. Terminal Functions – PZ Package (continued)

| TERMINAL | | I/O ⁽¹⁾ | DESCRIPTION |
|--|-----------|--------------------|--|
| NAME | NO. PZ | | |
| P2.5/PM_UCB0SOMI/ PM_UCB0SCL/LCDREF/ R13 | 48 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: eUSCI_B0 SPI slave out, master in Default mapping: eUSCI_B0 I2C clock External reference voltage input for regulated LCD voltage Input/Output port of third most positive analog LCD voltage (V3 or V4) |
| P2.6/PM_UCB0SIMO/ PM_UCB0SDA/R03 | 49 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: eUSCI_B0 SPI slave in, master out Default mapping: eUSCI_B0 I2C data Input/output port of lowest analog LCD voltage (V5) |
| P2.7/PM_UCB0CLK/CB2 | 50 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: eUSCI_B0 clock input/output Comparator_B input CB2 |
| P3.0/PM_UCA0RXD/ PM_UCA0SOMI | 51 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: eUSCI_A0 UART receive data Default mapping: eUSCI_A0 SPI slave out, master in |
| P3.1/PM_UCA0TXD/ PM_UCA0SIMO/S39 | 52 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: eUSCI_A0 UART transmit data Default mapping: eUSCI_A0 SPI slave in, master out LCD segment output S39 |
| P3.2/PM_UCA0CLK/S38 | 53 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: eUSCI_A0 clock input/output LCD segment output S38 |
| P3.3/PM_UCA1CLK/S37 | 54 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: eUSCI_A1 clock input/output LCD segment output S37 |
| P3.4/PM_UCA1RXD/ PM_UCA1SOMI/S36 | 55 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: eUSCI_A1 UART receive data Default mapping: eUSCI_A1 SPI slave out, master in LCD segment output S36 |
| P3.5/PM_UCA1TXD/ PM_UCA1SIMO/S35 | 56 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: eUSCI_A1 UART transmit data Default mapping: eUSCI_A1 SPI slave in, master out LCD segment output S35 |
| P3.6/PM_UCA2RXD/ PM_UCA2SOMI/S34 | 57 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: eUSCI_A2 UART receive data Default mapping: eUSCI_A2 SPI slave out, master in LCD segment output S34 |
| P3.7/PM_UCA2TXD/ PM_UCA2SIMO/S33 | 58 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: eUSCI_A2 UART transmit data Default mapping: eUSCI_A2 SPI slave in, master out LCD segment output S33 |
| P4.0/PM_UCA2CLK/S32 | 59 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: eUSCI_A2 clock input/output LCD segment output S32 |

Table 5. Terminal Functions – PZ Package (continued)

| TERMINAL | | I/O ⁽¹⁾ | DESCRIPTION |
|-------------------------------------|-----------|--------------------|--|
| NAME | NO. PZ | | |
| P4.1/PM_UCA3RXD/ PM_UCA3SOMI/S31 | 60 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: eUSCI_A3 UART receive data Default mapping: eUSCI_A3 SPI slave out, master in LCD segment output S31 |
| P4.2/PM_UCA3TXD/ PM_UCA3SIMO/S30 | 61 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: eUSCI_A3 UART transmit data Default mapping: eUSCI_A3 SPI slave in, master out LCD segment output S30 |
| P4.3/PM_UCA3CLK/S29 | 62 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: eUSCI_A3 clock input/output LCD segment output S29 |
| P4.4/PM_UCB1SOMI/ PM_UCB1SCL/S28 | 63 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: eUSCI_B1 SPI slave out, master in Default mapping: eUSCI_B1 I2C clock LCD segment output S28 |
| P4.5/PM_UCB1SIMO/ PM_UCB1SDA/S27 | 64 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: eUSCI_B1 SPI slave in, master out Default mapping: eUSCI_B1 I2C data LCD segment output S27 |
| P4.6/PM_UCB1CLK/S26 | 65 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: eUSCI_B1 clock input/output LCD segment output S26 |
| P4.7/PM_TA3.0/S25 | 66 | I/O | General-purpose digital I/O with mappable secondary function Default Mapping: Timer TA3 CCR0 capture: CCI0A input, compare: Out0 output LCD segment output S25 |
| P5.0/SDCLK/S24 | 67 | I/O | General-purpose digital I/O SD24_B bit stream clock input/output LCD segment output S24 |
| P5.1/PM_SD0DIO/S23 | 68 | I/O | General-purpose digital I/O Default mapping: SD24_B converter 0 bit stream data input/output LCD segment output S23 |
| P5.2/PM_SD1DIO/S22 | 69 | I/O | General-purpose digital I/O Default mapping: SD24_B converter 1 bit stream data input/output LCD segment output S22 |
| P5.3/PM_SD2DIO/S21 | 70 | I/O | General-purpose digital I/O Default mapping: SD24_B converter 2 bit stream data input/output LCD segment output S21 |
| P5.4/PM_SD3DIO/S20 | 71 | I/O | General-purpose digital I/O Default mapping: SD24_B converter 3 bit stream data input/output LCD segment output S20 |
| P5.5/PM_SD4DIO/S19 | 72 | I/O | General-purpose digital I/O Default mapping: SD24_B converter 4 bit stream data input/output (not available on F674x1 devices) LCD segment output S19 |

Table 5. Terminal Functions – PZ Package (continued)

| TERMINAL | | I/O ⁽¹⁾ | DESCRIPTION |
|-----------------------|-----------|--------------------|---|
| NAME | NO. PZ | | |
| P5.6/PM_SD5DIO/S18 | 73 | I/O | General-purpose digital I/O Default mapping: SD24_B converter 5 bit stream data input/output (not available on F674x1 devices) LCD segment output S18 |
| P5.7/PM_SD6DIO/S17 | 74 | I/O | General-purpose digital I/O Default mapping: SD24_B converter 4 bit stream data input/output (not available on F676x1, F674x1 devices) LCD segment output S17 |
| VDSYS2 ⁽⁵⁾ | 75 | | Digital power supply for I/Os |
| DVSS2 | 76 | | Digital ground supply |
| P6.0/S16 | 77 | I/O | General-purpose digital I/O LCD segment output S16 |
| P6.1/S15 | 78 | I/O | General-purpose digital I/O LCD segment output S15 |
| P6.2/S14 | 79 | I/O | General-purpose digital I/O LCD segment output S14 |
| P6.3/S13 | 80 | I/O | General-purpose digital I/O LCD segment output S13 |
| P6.4/S12 | 81 | I/O | General-purpose digital I/O LCD segment output S12 |
| P6.5/S11 | 82 | I/O | General-purpose digital I/O LCD segment output S11 |
| P6.6/S10 | 83 | I/O | General-purpose digital I/O LCD segment output S10 |
| P6.7/S9 | 84 | I/O | General-purpose digital I/O LCD segment output S9 |
| P7.0/S8 | 85 | I/O | General-purpose digital I/O LCD segment output S8 |
| P7.1/S7 | 86 | I/O | General-purpose digital I/O LCD segment output S7 |
| P7.2/S6 | 87 | I/O | General-purpose digital I/O LCD segment output S6 |
| P7.3/S5 | 88 | I/O | General-purpose digital I/O LCD segment output S5 |
| P7.4/S4 | 89 | I/O | General-purpose digital I/O LCD segment output S4 |
| P7.5/S3 | 90 | I/O | General-purpose digital I/O LCD segment output S3 |
| P7.6/S2 | 91 | I/O | General-purpose digital I/O LCD segment output S2 |
| P7.7/S1 | 92 | I/O | General-purpose digital I/O LCD segment output S1 |

(5) The pins VDSYS1 and VDSYS2 must be connected externally on board for proper device operation.

Table 5. Terminal Functions – PZ Package (continued)

| TERMINAL | | I/O ⁽¹⁾ | DESCRIPTION |
|---|-----------|--------------------|--|
| NAME | NO. PZ | | |
| P8.0/S0 | 93 | I/O | General-purpose digital I/O LCD segment output S0 |
| P8.1/TACLK/RTCCLK/CB3 | 94 | I/O | General-purpose digital I/O Timer clock input TACLK for TA0, TA1, TA2, TA3 RTCCLK clock output Comparator_B input CB3 |
| TEST/SBWTCK | 95 | I | Test mode pin – select digital I/O on JTAG pins Spy-By-Wire input clock |
| PJ.0/TDO | 96 | I/O | General-purpose digital I/O Test data output |
| PJ.1/TDI/TCLK | 97 | I/O | General-purpose digital I/O Test data input or Test clock input |
| PJ.2/TMS | 98 | I/O | General-purpose digital I/O Test mode select |
| PJ.3/TCK | 99 | I/O | General-purpose digital I/O Test clock |
| $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ | 100 | I/O | Reset input active low ⁽⁶⁾ Non-maskable interrupt input Spy-By-Wire data input/output |

(6) When this pin is configured as reset, the internal pullup resistor is enabled by default.

Development Tools Support

All MSP430™ microcontrollers are supported by a wide variety of software and hardware development tools. Tools are available from TI and various third parties. See them all at www.ti.com/msp430tools.

Hardware Features

See the *Code Composer Studio for MSP430 User's Guide (SLAU157)* for details on the available features.

| MSP430 Architecture | 4-Wire JTAG | 2-Wire JTAG | Break-points (N) | Range Break-points | Clock Control | State Sequencer | Trace Buffer | LPMx.5 Debugging Support |
|---------------------|-------------|-------------|------------------|--------------------|---------------|-----------------|--------------|--------------------------|
| MSP430Xv2 | Yes | Yes | 3 | Yes | Yes | No | No | Yes |

Recommended Hardware Options

Target Socket Boards

The target socket boards allow easy programming and debugging of the device using JTAG. They also feature header pin outs for prototyping. Target socket boards are orderable individually or as a kit with the JTAG programmer and debugger included. The following table shows the compatible target boards and the supported packages.

| Package | Target Board and Programmer Bundle | Target Board Only |
|--------------------|------------------------------------|---------------------------------|
| 128-pin LQFP (PEU) | MSP-FET430U128 | MSP-TS430PEU128 |

Experimenter Boards

Experimenter Boards and Evaluation kits are available for some MSP430 devices. These kits feature additional hardware components and connectivity for full system evaluation and prototyping. See www.ti.com/msp430tools for details.

Debugging and Programming Tools

Hardware programming and debugging tools are available from TI and from its third party suppliers. See the full list of available tools at www.ti.com/msp430tools.

Production Programmers

The production programmers expedite loading firmware to devices by programming several devices simultaneously.

| Part Number | PC Port | Features | Provider |
|--------------------------|----------------|---|-------------------|
| MSP-GANG | Serial and USB | Program up to eight devices at a time. Works with PC or standalone. | Texas Instruments |

Recommended Software Options

Integrated Development Environments

Software development tools are available from TI or from third parties. Open source solutions are also available. This device is supported by Code Composer Studio™ IDE (CCS).

MSP430Ware

[MSP430Ware](#) is a collection of code examples, data sheets, and other design resources for all MSP430 devices delivered in a convenient package. In addition to providing a complete collection of existing MSP430 design resources, MSP430Ware also includes a high-level API called MSP430 Driver Library. This library makes it easy to program MSP430 hardware. MSP430Ware is available as a component of CCS or as a standalone package.

SYS/BIOS

SYS/BIOS is an advanced real-time operating system for the MSP430 microcontrollers. It features preemptive deterministic multi-tasking, hardware abstraction, memory management, and real-time analysis. SYS/BIOS is available free of charge and is provided with full source code.

Command-Line Programmer

MSP430 Flasher is an open-source, shell-based interface for programming MSP430 microcontrollers through a FET programmer or eZ430 using JTAG or Spy-Bi-Wire (SBW) communication. MSP430 Flasher can be used to download binary files (.txt or .hex) files directly to the MSP430 Flash without the need for an IDE.

Device and Development Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP430™ MCU devices and support tools. Each MSP430™ MCU commercial family member has one of three prefixes: MSP, PMS, or XMS (for example, MSP430F5259). Texas Instruments recommends two of three possible prefix designators for its support tools: MSP and MSPX. These prefixes represent evolutionary stages of product development from engineering prototypes (with XMS for devices and MSPX for tools) through fully qualified production devices and tools (with MSP for devices and MSP for tools).

Device development evolutionary flow:

XMS – Experimental device that is not necessarily representative of the final device's electrical specifications

PMS – Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification

MSP – Fully qualified production device

Support tool development evolutionary flow:

MSPX – Development-support product that has not yet completed Texas Instruments internal qualification testing.

MSP – Fully-qualified development-support product

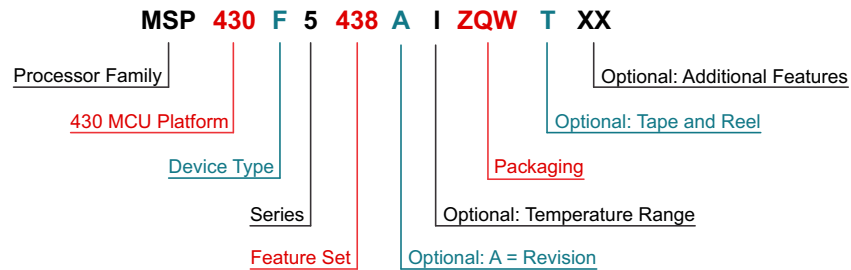
XMS and PMS devices and MSPX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices and MSP development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS and PMS) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, PZP) and temperature range (for example, T). [Figure 2](#) provides a legend for reading the complete device name for any family member.

Part Number Decoder


| | | |
|--------------------------------------|--|--|
| Processor Family | CC = Embedded RF Radio MSP = Mixed Signal Processor XMS = Experimental Silicon PMS = Prototype Device | |
| 430 MCU Platform | TI's Low Power Microcontroller Platform | |
| Device Type | Memory Type C = ROM F = Flash FR = FRAM G = Flash or FRAM (Value Line) L = No Nonvolatile Memory | Specialized Application AFE = Analog Front End BT = Preprogrammed with Bluetooth BQ = Contactless Power CG = ROM Medical FE = Flash Energy Meter FG = Flash Medical FW = Flash Electronic Flow Meter |
| Series | 1 Series = Up to 8 MHz 2 Series = Up to 16 MHz 3 Series = Legacy 4 Series = Up to 16 MHz w/ LCD | 5 Series = Up to 25 MHz 6 Series = Up to 25 MHz w/ LCD 0 = Low Voltage Series |
| Feature Set | Various Levels of Integration Within a Series | |
| Optional: A = Revision | N/A | |
| Optional: Temperature Range | S = 0°C to 50°C C = 0°C to 70°C I = -40°C to 85°C T = -40°C to 105°C | |
| Packaging | www.ti.com/packaging | |
| Optional: Tape and Reel | T = Small Reel (7 inch) R = Large Reel (11 inch) No Markings = Tube or Tray | |
| Optional: Additional Features | -EP = Enhanced Product (-40°C to 105°C) -HT = Extreme Temperature Parts (-55°C to 150°C) -Q1 = Automotive Q100 Qualified | |

Figure 2. Device Nomenclature

Short-Form Description

CPU ([Link to User's Guide](#))

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

Instruction Set

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data. [Table 6](#) shows examples of the three types of instruction formats; [Table 7](#) shows the address modes.

| | |
|--------------------------|-----------|
| Program Counter | PC/R0 |
| Stack Pointer | SP/R1 |
| Status Register | SR/CG1/R2 |
| Constant Generator | CG2/R3 |
| General-Purpose Register | R4 |
| General-Purpose Register | R5 |
| General-Purpose Register | R6 |
| General-Purpose Register | R7 |
| General-Purpose Register | R8 |
| General-Purpose Register | R9 |
| General-Purpose Register | R10 |
| General-Purpose Register | R11 |
| General-Purpose Register | R12 |
| General-Purpose Register | R13 |
| General-Purpose Register | R14 |
| General-Purpose Register | R15 |

Table 6. Instruction Word Formats

| INSTRUCTION WORD FORMAT | EXAMPLE | OPERATION |
|-----------------------------------|-----------|-----------------------|
| Dual operands, source-destination | ADD R4,R5 | R4 + R5 → R5 |
| Single operands, destination only | CALL R8 | PC → (TOS), R8 → PC |
| Relative jump, un/conditional | JNE | Jump-on-equal bit = 0 |

Table 7. Address Mode Descriptions

| ADDRESS MODE | S ⁽¹⁾ | D ⁽¹⁾ | SYNTAX | EXAMPLE | OPERATION |
|------------------------|------------------|------------------|--------------------|------------------|-------------------------------|
| Register | + | + | MOV Rs,Rd | MOV R10,R11 | R10 → R11 |
| Indexed | + | + | MOV X(Rn),Y(Rm) | MOV 2(R5),6(R6) | M(2+R5) → M(6+R6) |
| Symbolic (PC relative) | + | + | MOV EDE,TONI | | M(EDE) → M(TONI) |
| Absolute | + | + | MOV & MEM, & TCDAT | | M(MEM) → M(TCDAT) |
| Indirect | + | | MOV @Rn,Y(Rm) | MOV @R10,Tab(R6) | M(R10) → M(Tab+R6) |
| Indirect autoincrement | + | | MOV @Rn+,Rm | MOV @R10+,R11 | M(R10) → R11 R10 + 2 → R10 |
| Immediate | + | | MOV #X,TONI | MOV #45,TONI | #45 → M(TONI) |

(1) S = source, D = destination

Operating Modes

The MSP430 has one active mode and six software selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following seven operating modes can be configured by software:

- Active mode (AM)
 - All clocks are active
- Low-power mode 0 (LPM0)
 - CPU is disabled
 - ACLK and SMCLK remain active, MCLK is disabled
 - FLL loop control remains active
- Low-power mode 1 (LPM1)
 - CPU is disabled
 - FLL loop control is disabled
 - ACLK and SMCLK remain active, MCLK is disabled
- Low-power mode 2 (LPM2)
 - CPU is disabled
 - MCLK and FLL loop control and DCOCLK are disabled
 - DCO's dc-generator remains enabled
 - ACLK remains active
- Low-power mode 3 (LPM3)
 - CPU is disabled
 - MCLK, FLL loop control, and DCOCLK are disabled
 - DCO's dc-generator is disabled
 - ACLK remains active
- Low-power mode 4 (LPM4)
 - CPU is disabled
 - ACLK is disabled
 - MCLK, FLL loop control, and DCOCLK are disabled
 - DCO's dc-generator is disabled
 - Crystal oscillator is stopped
 - Complete data retention
- Low-power mode 3.5 (LPM3.5)
 - Internal regulator disabled
 - No RAM retention, Backup RAM retained
 - I/O pad state retention
 - RTC clocked by low-frequency oscillator
 - Wakeup from $\overline{\text{RST}}$ /NMI, RTC_C events, Ports P1 and P2
- Low-power mode 4.5 (LPM4.5)
 - Internal regulator disabled
 - No RAM retention, Backup RAM retained
 - RTC is disabled
 - I/O pad state retention
 - Wakeup from $\overline{\text{RST}}$ /NMI, Ports P1 and P2

Interrupt Vector Addresses

The interrupt vectors and the power-up start address are located in the address range 0FFFFh to 0FF80h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

Table 8. Interrupt Sources, Flags, and Vectors

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|--|---|------------------|--------------|-------------|
| System Reset Power-Up External Reset Watchdog Timeout, Key Violation Flash Memory Key Violation | WDTIFG, KEYV (SYSRSTIV) ^{(1) (2)} | Reset | 0FFFEh | 63, highest |
| System NMI PMM Vacant Memory Access JTAG Mailbox | SVMLIFG, SVMHIFG, DLYLIFG, DLYHIFG, VLRLIFG, VLRHIFG, VMAIFG, JMBNIFG, JMBOUTIFG (SYSSNIV) ^{(1) (3)} | (Non)maskable | 0FFFCCh | 62 |
| User NMI NMI Oscillator Fault Flash Memory Access Violation Supply Switched | NMIIFG, OFIFG, ACCVIFG, AUXSWGIFG (SYSUNIV) ^{(1) (3)} | (Non)maskable | 0FFFAh | 61 |
| Watchdog Timer_A Interval Timer Mode | WDTIFG | Maskable | 0FFF8h | 60 |
| eUSCI_A0 Receive or Transmit | UCA0RXIFG, UCA0TXIFG (UCA0IV) ^{(1) (4)} | Maskable | 0FFF6h | 59 |
| eUSCI_B0 Receive or Transmit | UCB0RXIFG, UCB0TXIFG (UCB0IV) ^{(1) (4)} | Maskable | 0FFF4h | 58 |
| ADC10_A | ADC10IFG0, ADC10INIFG, ADC10LOIFG, ADC10HIIFG, ADC10TOVIFG, ADC10OVIFG (ADC10IV) ^{(1) (4)} | Maskable | 0FFF2h | 57 |
| SD24_B | SD24_B Interrupt Flags (SD24IV) ^{(1) (4)} | Maskable | 0FFF0h | 56 |
| Timer TA0 | TA0CCR0 CCIFG0 ⁽⁴⁾ | Maskable | 0FFEEh | 55 |
| Timer TA0 | TA0CCR1 CCIFG1, TA0CCR2 CCIFG2, TA0IFG (TA0IV) ^{(1) (4)} | Maskable | 0FFECCh | 54 |
| eUSCI_A1 Receive or Transmit | UCA1RXIFG, UCA1TXIFG (UCA1IV) ^{(1) (4)} | Maskable | 0FFEAh | 53 |
| eUSCI_A2 Receive or Transmit | UCA2RXIFG, UCA2TXIFG (UCA2IV) ^{(1) (4)} | Maskable | 0FFE8h | 52 |
| Auxiliary Supplies | AUXSWGIFG, AUXIFG0, AUXIFG1, AUXIFG2 (AUXIV) ^{(1) (4)} | Maskable | 0FFE6h | 51 |
| DMA | DMA0IFG, DMA1IFG, DMA2IFG (DMAIV) ^{(1) (4)} | Maskable | 0FFE4h | 50 |
| Timer TA1 | TA1CCR0 CCIFG0 ⁽⁴⁾ | Maskable | 0FFE2h | 49 |
| Timer TA1 | TA1CCR1 CCIFG1, TA1IFG (TA1IV) ^{(1) (4)} | Maskable | 0FFE0h | 48 |
| eUSCI_A3 Receive or Transmit | UCA3RXIFG, UCA3TXIFG (UCA3IV) ^{(1) (4)} | Maskable | 0FFDEh | 47 |
| eUSCI_B1 Receive or Transmit | UCB1RXIFG, UCB1TXIFG (UCB1IV) ^{(1) (4)} | Maskable | 0FFDCh | 46 |
| I/O Port P1 | P1IFG.0 to P1IFG.7 (P1IV) ^{(1) (4)} | Maskable | 0FFDAh | 45 |
| Timer TA2 | TA2CCR0 CCIFG0 ⁽⁴⁾ | Maskable | 0FFD8h | 44 |
| Timer TA2 | TA2CCR1 CCIFG1, TA2IFG (TA2IV) ^{(1) (4)} | Maskable | 0FFD6h | 43 |
| I/O Port P2 | P2IFG.0 to P2IFG.7 (P2IV) ^{(1) (4)} | Maskable | 0FFD4h | 42 |
| Timer TA3 | TA3CCR0 CCIFG0 ⁽⁴⁾ | Maskable | 0FFD2h | 41 |
| Timer TA3 | TA3CCR1 CCIFG1, TA3IFG (TA3IV) ^{(1) (4)} | Maskable | 0FFD0h | 40 |
| LCD_C | LCD_C Interrupt Flags (LCDCIV) ^{(1) (4)} | Maskable | 0FFCEh | 39 |
| RTC_C | RTCOFIFG, RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG (RTCIV) ^{(1) (4)} | Maskable | 0FFCCh | 38 |

(1) Multiple source flags

(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space or vacant memory space.

(3) (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.

(4) Interrupt flags are located in the module.

Table 8. Interrupt Sources, Flags, and Vectors (continued)

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|------------------|--|------------------|--------------|-----------|
| Comparator_B | Comparator_B Interrupt Flags (CBIV) ⁽¹⁾ | Maskable | 0FFCAh | 37 |
| Reserved | Reserved ⁽⁵⁾ | | 0FFC6h | 35 |
| | | | ⋮ | ⋮ |
| | | | 0FF80h | 0, lowest |

(5) Reserved interrupt vectors at addresses are not used in this device and can be used for regular program code if necessary. To maintain compatibility with other devices, it is recommended to reserve these locations.

Special Function Registers (SFRs)

The MSP430 SFRs are located in the lowest address space and can be accessed via word or byte formats.

| | | |
|---------------|------------------|---|
| Legend | rw: | Bit can be read and written. |
| | rw-0,1: | Bit can be read and written. It is reset or set by PUC. |
| | rw-(0,1): | Bit can be read and written. It is reset or set by POR. |
| | rw-[0,1]: | Bit can be read and written. It is reset or set by BOR. |
| | – | SFR bit is not present in device. |

Table 9. Interrupt Enable 1

| | | | | | | | |
|-----------------|----------------|---------------|--------------|--------------|----|------------------|--------------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| – | – | – | – | – | – | AUXSWNMIE | – |
| | | | | | | rw-0 | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| JMBOUTIE | JMBINIE | ACCVIE | NMIIE | VMAIE | – | OFIE | WDTIE |
| rw-0 | rw-0 | rw-0 | rw-0 | rw-0 | | rw-0 | rw-0 |

| | |
|------------------|--|
| WDTIE | Watchdog timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured as a general-purpose timer. |
| OFIE | Oscillator fault interrupt enable |
| VMAIE | Vacant memory access interrupt enable |
| NMIIE | Nonmaskable interrupt enable |
| ACCVIE | Flash access violation interrupt enable |
| JMBINIE | JTAG mailbox input interrupt enable |
| JMBOUTIE | JTAG mailbox output interrupt enable |
| AUXSWNMIE | Supply switched non-maskable interrupt enable |

Table 10. Interrupt Flag 1

| | | | | | | | |
|------------------|-----------------|----|---------------|---------------|----|--------------|---------------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| – | – | – | – | – | – | – | – |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| JMBOUTIFG | JMBINIFG | – | NMIIFG | VMAIFG | – | OFIFG | WDTIFG |
| rw-[0] | rw-[0] | | rw-0 | rw-0 | | rw-0 | rw-0 |

| | |
|------------------|---|
| WDTIFG | Set on watchdog timer overflow (in watchdog mode) or security key violation Reset on V _{CC} power-on or a reset condition at the $\overline{\text{RST}}$ /NMI pin in reset mode |
| OFIFG | Flag set on oscillator fault |
| VMAIFG | Set on vacant memory access |
| NMIIFG | Set via $\overline{\text{RST}}$ /NMI pin |
| JMBINIFG | Set on JTAG mailbox input message |
| JMBOUTIFG | Set on JTAG mailbox output register ready for next message |

Memory Organization

Table 11. Memory Organization

| | | MSP430F67791 MSP430F67691 MSP430F67491 | MSP430F67781 MSP430F67681 MSP430F67481 | MSP430F67771 MSP430F67671 MSP430F67471 |
|---------------------------------------|------------|---|---|---|
| Main Memory (flash) | Total Size | 512kB | 512kB | 256kB |
| Main: Interrupt vector | | 00FFFFh to 00FF80h | 00FFFFh to 00FF80h | 00FFFFh to 00FF80h |
| Main: code memory | Bank 3 | 128kB 08BFFFh to 06C000h | 128kB 08BFFFh to 06C000h | not available |
| | Bank 2 | 128kB 06BFFFh to 04C000h | 128kB 06BFFFh to 04C000h | not available |
| | Bank 1 | 128kB 04BFFFh to 02C000h | 128kB 04BFFFh to 02C000h | 128kB 04BFFFh to 02C000h |
| | Bank 0 | 128kB 02BFFFh to 00C000h | 128kB 02BFFFh to 00C000h | 128kB 02BFFFh to 00C000h |
| RAM | Total Size | 32kB | 16kB | 32kB |
| | Sector 7 | 4kB 009BFFFh to 008C00h | not available | 4kB 009BFFFh to 008C00h |
| | Sector 6 | 4kB 008BFFFh to 007C00h | not available | 4kB 008BFFFh to 007C00h |
| | Sector 5 | 4kB 007BFFFh to 006C00h | not available | 4kB 007BFFFh to 006C00h |
| | Sector 4 | 4kB 006BFFFh to 005C00h | not available | 4kB 006BFFFh to 005C00h |
| | Sector 3 | 4kB 005BFFFh to 004C00h | 4kB 005BFFFh to 004C00h | 4kB 005BFFFh to 004C00h |
| | Sector 2 | 4kB 004BFFFh to 003C00h | 4kB 004BFFFh to 003C00h | 4kB 004BFFFh to 003C00h |
| | Sector 1 | 4kB 003BFFFh to 002C00h | 4kB 003BFFFh to 002C00h | 4kB 003BFFFh to 002C00h |
| | Sector 0 | 4kB 002BFFFh to 001C00h | 4kB 002BFFFh to 001C00h | 4kB 002BFFFh to 001C00h |
| Device Descriptor | | 128 B 001AFFh to 001A80h | 128 B 001AFFh to 001A80h | 128 B 001AFFh to 001A80h |
| | | 128 B 001A7Fh to 001A00h | 128 B 001A7Fh to 001A00h | 128 B 001A7Fh to 001A00h |
| Information memory (flash) | Info A | 128 B 0019FFh to 001980h | 128 B 0019FFh to 001980h | 128 B 0019FFh to 001980h |
| | Info B | 128 B 00197Fh to 001900h | 128 B 00197Fh to 001900h | 128 B 00197Fh to 001900h |
| | Info C | 128 B 0018FFh to 001880h | 128 B 0018FFh to 001880h | 128 B 0018FFh to 001880h |
| | Info D | 128 B 00187Fh to 001800h | 128 B 00187Fh to 001800h | 128 B 00187Fh to 001800h |
| Bootstrap loader (BSL) memory (flash) | BSL 3 | 512 B 0017FFh to 001600h | 512 B 0017FFh to 001600h | 512 B 0017FFh to 001600h |
| | BSL 2 | 512 B 0015FFh to 001400h | 512 B 0015FFh to 001400h | 512 B 0015FFh to 001400h |
| | BSL 1 | 512 B 0013FFh to 001200h | 512 B 0013FFh to 001200h | 512 B 0013FFh to 001200h |
| | BSL 0 | 512 B 0011FFh to 001000h | 512 B 0011FFh to 001000h | 512 B 0011FFh to 001000h |
| Peripherals | | 4 KB 000FFFh to 0h | 4 KB 000FFFh to 0h | 4 KB 000FFFh to 0h |

| | | MSP430F67761 MSP430F67661 MSP430F67461 | MSP430F67751 MSP430F67651 MSP430F67451 |
|---|------------|---|---|
| Main Memory (flash) | Total Size | 256kB | 128kB |
| Main: code memory Main: Interrupt vector | | 00FFFFh to 00FF80h | 00FFFFh to 00FF80h |
| | Bank 3 | not available | not available |
| | Bank 2 | not available | not available |
| | Bank 1 | 128kB 04BFFFh to 02C000h | not available |
| | Bank 0 | 128kB 02BFFFh to 00C000h | 128kB 02BFFFh to 00C000h |
| RAM | Total Size | 16kB | 16kB |
| | Sector 7 | not available | not available |
| | Sector 6 | not available | not available |
| | Sector 5 | not available | not available |
| | Sector 4 | not available | not available |
| | Sector 3 | 4kB 005BFFFh to 004C00h | 4kB 005BFFFh to 004C00h |
| | Sector 2 | 4kB 004BFFFh to 003C00h | 4kB 004BFFFh to 003C00h |
| | Sector 1 | 4kB 003BFFFh to 002C00h | 4kB 003BFFFh to 002C00h |
| | Sector 0 | 4kB 002BFFFh to 001C00h | 4kB 002BFFFh to 001C00h |
| Device Descriptor | | 128 B 001AFFh to 001A80h | 128 B 001AFFh to 001A80h |
| | | 128 B 001A7Fh to 001A00h | 128 B 001A7Fh to 001A00h |
| Information memory (flash) | Info A | 128 B 0019FFh to 001980h | 128 B 0019FFh to 001980h |
| | Info B | 128 B 00197Fh to 001900h | 128 B 00197Fh to 001900h |
| | Info C | 128 B 0018FFh to 001880h | 128 B 0018FFh to 001880h |
| | Info D | 128 B 00187Fh to 001800h | 128 B 00187Fh to 001800h |
| Bootstrap loader (BSL) memory (flash) | BSL 3 | 512 B 0017FFh to 001600h | 512 B 0017FFh to 001600h |
| | BSL 2 | 512 B 0015FFh to 001400h | 512 B 0015FFh to 001400h |
| | BSL 1 | 512 B 0013FFh to 001200h | 512 B 0013FFh to 001200h |
| | BSL 0 | 512 B 0011FFh to 001000h | 512 B 0011FFh to 001000h |
| Peripherals | | 4 KB 000FFFh to 0h | 4 KB 000FFFh to 0h |

Bootstrap Loader (BSL)

The BSL enables users to program the flash memory or RAM using various serial interfaces. Access to the device memory via the BSL is protected by a user-defined password. BSL entry requires a specific entry sequence on the RST/NMI/SBWDIO and TEST/SBWTCK pins. For a complete description of the features of the BSL and its implementation, see the *MSP430 Programming Via the Bootstrap Loader User's Guide* (SLAU319).

Table 12. UART BSL Pin Requirements and Functions

| DEVICE SIGNAL | BSL FUNCTION |
|------------------------------------|-----------------------|
| $\overline{\text{RST/NMI/SBWDIO}}$ | Entry sequence signal |
| TEST/SBWTCK | Entry sequence signal |
| P2.0 | Data transmit |
| P2.1 | Data receive |
| VCC | Power supply |
| VSS | Ground supply |

JTAG Operation

JTAG Standard Interface

The MSP430 family supports the standard JTAG interface which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the $\overline{\text{RST/NMI/SBWDIO}}$ is required to interface with MSP430 development tools and device programmers. The JTAG pin requirements are shown in Table 13. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide* (SLAU278). For a complete description of the features of the JTAG interface and its implementation, see *MSP430 Programming Via the JTAG Interface* (SLAU320).

Table 13. JTAG Pin Requirements and Functions

| DEVICE SIGNAL | DIRECTION | FUNCTION |
|------------------------------------|-----------|-----------------------------|
| PJ.3/TCK | IN | JTAG clock input |
| PJ.2/TMS | IN | JTAG state control |
| PJ.1/TDI/TCLK | IN | JTAG data input, TCLK input |
| PJ.0/TDO | OUT | JTAG data output |
| TEST/SBWTCK | IN | Enable JTAG pins |
| $\overline{\text{RST/NMI/SBWDIO}}$ | IN | External reset |
| VCC | | Power supply |
| VSS | | Ground supply |

Spy-Bi-Wire Interface

In addition to the standard JTAG interface, the MSP430 family supports the two wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. The Spy-Bi-Wire interface pin requirements are shown in Table 14. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide* (SLAU278). For a complete description of the features of the JTAG interface and its implementation, see *MSP430 Programming Via the JTAG Interface* (SLAU320).

Table 14. Spy-Bi-Wire Pin Requirements and Functions

| DEVICE SIGNAL | DIRECTION | FUNCTION |
|------------------------------------|-----------|-------------------------------|
| TEST/SBWTCK | IN | Spy-Bi-Wire clock input |
| $\overline{\text{RST/NMI/SBWDIO}}$ | IN, OUT | Spy-Bi-Wire data input/output |
| VCC | | Power supply |
| VSS | | Ground supply |

Flash Memory ([Link to User's Guide](#))

The flash memory can be programmed via the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. The CPU can perform single-byte, single-word, and long-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n. Segments A to D are also called *information memory*.
- Segment A can be locked separately.

RAM Memory ([Link to User's Guide](#))

The RAM memory is made up of n sectors. Each sector can be completely powered down to save leakage; however, all data is lost. Features of the RAM memory include:

- RAM memory has n sectors of 4K bytes each.
- Each sector 0 to n can be complete disabled, however data retention is lost.
- Each sector 0 to n automatically enters low power retention mode when possible.

Backup RAM Memory ([Link to User's Guide](#))

The Backup RAM provides a limited number of bytes of RAM that are retained during LPM3.5. This Backup RAM is part of the Backup subsystem that operates on dedicated power supply AUXVCC3. There are 8 bytes of Backup RAM available in this device. It can be wordwise accessed via the registers BAKMEM0, BAKMEM1, BAKMEM2, and BAKMEM3. The Backup RAM registers cannot be accessed by CPU when the high-side SVS is disabled by the user application.

Peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x5xx and MSP430x6xx Family User's Guide (SLAU208)*.

Oscillator and System Clock ([Link to User's Guide](#))

The Unified Clock System (UCS) module includes support for a 32768-Hz watch crystal oscillator, an internal very-low-power low-frequency oscillator (VLO), an internal trimmed low-frequency oscillator (REFO), and an integrated internal digitally controlled oscillator (DCO). The UCS module is designed to meet the requirements of both low system cost and low power consumption. The UCS module features digital frequency locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the selected FLL reference frequency. The internal DCO provides a fast turn-on clock source and stabilizes in less than 5 μ s. The UCS module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal, the internal low-frequency oscillator (VLO), or the trimmed low-frequency oscillator (REFO).
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced by same sources made available to ACLK.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources made available to ACLK.
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, ACLK/8, ACLK/16, ACLK/32.

Power Management Module (PMM) ([Link to User's Guide](#))

The PMM includes an integrated voltage regulator that supplies the core voltage to the device and contains programmable output levels to provide for power optimization. The PMM also includes supply voltage supervisor (SVS) and supply voltage monitoring (SVM) circuitry, as well as brownout protection. The brownout circuit is implemented to provide the proper internal reset signal to the device during power-on and power-off. The SVS/SVM circuitry detects if the supply voltage drops below a user-selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (the device is not automatically reset). SVS and SVM circuitry is available on the primary supply and core supply.

Auxiliary Supply System ([Link to User's Guide](#))

The auxiliary supply system provides the option to operate the device from auxiliary supplies when the primary supply fails. There are two auxiliary supplies (AUXVCC1 and AUXVCC2) supported in MSP430F67xx. This module supports automatic and manual switching from primary supply to auxiliary supplies while maintaining full functionality. It allows threshold-based monitoring of primary and auxiliary supplies. The device can be started from primary supply or AUXVCC1, whichever is higher. Auxiliary supply system enables internal monitoring of voltage levels on primary and auxiliary supplies using ADC10_A. This module also implements a simple charger for backup capacitors.

Backup Subsystem ([Link to User's Guide](#))

The Backup subsystem operates on a dedicated power supply AUXVCC3. This subsystem includes low-frequency oscillator, Real-Time Clock module, and Backup RAM. The functionality of Backup subsystem is retained during LPM3.5. The Backup subsystem module registers cannot be accessed by CPU when the high side SVS is disabled by user.

Digital I/O ([Link to User's Guide](#))

There are up to eleven 8-bit I/O ports implemented. For 128-pin options, Ports P1 to P10 are complete, and Port P11 is 6 bits wide. For 100-pin options, Ports P1 to P7 are complete, Port P8 is 2 bits wide, and ports P9, P10, and P11 are completely removed. Port PJ contains four individual I/O pins, common to all devices. All I/O bits are individually programmable.

- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on all ports.
- Programmable drive strength on all ports.
- Edge-selectable interrupt and LPM3.5, LPM4.5 wakeup input capability available for all bits of ports P1 and P2.
- Read-write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise (P1 Through P11) or word-wise in pairs (PA Through PF).

Port Mapping Controller ([Link to User's Guide](#))

The port mapping controller allows flexible and reconfigurable mapping of digital functions to Ports P2, P3, and P4.

Table 15. Port Mapping Mnemonics and Functions

| VALUE | PxMAPy MNEMONIC | INPUT PIN FUNCTION | OUTPUT PIN FUNCTION |
|-------|-----------------|--|---------------------|
| 0 | PM_NONE | None | DVSS |
| 1 | PM_UCA0RXD | eUSCI_A0 UART RXD (direction controlled by eUSCI – Input) | |
| | PM_UCA0SOMI | eUSCI_A0 SPI slave out master in (direction controlled by eUSCI) | |
| 2 | PM_UCA0TXD | eUSCI_A0 UART TXD (direction controlled by eUSCI – Output) | |
| | PM_UCA0SIMO | eUSCI_A0 SPI slave in master out (direction controlled by eUSCI) | |
| 3 | PM_UCA0CLK | eUSCI_A0 clock input/output (direction controlled by eUSCI) | |
| 4 | PM_UCA0STE | eUSCI_A0 SPI slave transmit enable (direction controlled by eUSCI) | |
| 5 | PM_UCA1RXD | eUSCI_A1 UART RXD (direction controlled by eUSCI – Input) | |
| | PM_UCA1SOMI | eUSCI_A1 SPI slave out master in (direction controlled by eUSCI) | |
| 6 | PM_UCA1TXD | eUSCI_A1 UART TXD (direction controlled by eUSCI – Output) | |
| | PM_UCA1SIMO | eUSCI_A1 SPI slave in master out (direction controlled by eUSCI) | |
| 7 | PM_UCA1CLK | eUSCI_A1 clock input/output (direction controlled by eUSCI) | |
| 8 | PM_UCA1STE | eUSCI_A1 SPI slave transmit enable (direction controlled by eUSCI) | |
| 9 | PM_UCA2RXD | eUSCI_A2 UART RXD (direction controlled by eUSCI – Input) | |
| | PM_UCA2SOMI | eUSCI_A2 SPI slave out master in (direction controlled by eUSCI) | |
| 10 | PM_UCA2TXD | eUSCI_A2 UART TXD (direction controlled by eUSCI – Output) | |
| | PM_UCA2SIMO | eUSCI_A2 SPI slave in master out (direction controlled by eUSCI) | |
| 11 | PM_UCA2CLK | eUSCI_A2 clock input/output (direction controlled by eUSCI) | |

Table 15. Port Mapping Mnemonics and Functions (continued)

| VALUE | PxMAPy MNEMONIC | INPUT PIN FUNCTION | OUTPUT PIN FUNCTION |
|-------------------------|-----------------|--|------------------------------|
| 12 | PM_UCA2STE | eUSCI_A2 SPI slave transmit enable (direction controlled by eUSCI) | |
| 13 | PM_UCA3RXD | eUSCI_A3 UART RXD (direction controlled by eUSCI – Input) | |
| | PM_UCA3SOMI | eUSCI_A3 SPI slave out master in (direction controlled by eUSCI) | |
| 14 | PM_UCA3TXD | eUSCI_A3 UART TXD (direction controlled by eUSCI – Output) | |
| | PM_UCA3SIMO | eUSCI_A3 SPI slave in master out (direction controlled by eUSCI) | |
| 15 | PM_UCA3CLK | eUSCI_A3 clock input/output (direction controlled by eUSCI) | |
| 16 | PM_UCA3STE | eUSCI_A3 SPI slave transmit enable (direction controlled by eUSCI) | |
| 17 | PM_UCB0SIMO | eUSCI_B0 SPI slave in master out (direction controlled by eUSCI) | |
| | PM_UCB0SDA | eUSCI_B0 I2C data (open drain and direction controlled by eUSCI) | |
| 18 | PM_UCB0SOMI | eUSCI_B0 SPI slave out master in (direction controlled by eUSCI) | |
| | PM_UCB0SCL | eUSCI_B0 I2C clock (open drain and direction controlled by eUSCI) | |
| 19 | PM_UCB0CLK | eUSCI_B0 clock input/output (direction controlled by eUSCI) | |
| 20 | PM_UCB0STE | eUSCI_B0 SPI slave transmit enable (direction controlled by eUSCI) | |
| 21 | PM_UCB1SIMO | eUSCI_B1 SPI slave in master out (direction controlled by eUSCI) | |
| | PM_UCB1SDA | eUSCI_B1 I2C data (open drain and direction controlled by eUSCI) | |
| 22 | PM_UCB1SOMI | eUSCI_B1 SPI slave out master in (direction controlled by eUSCI) | |
| | PM_UCB1SCL | eUSCI_B1 I2C clock (open drain and direction controlled by eUSCI) | |
| 23 | PM_UCB1CLK | eUSCI_B1 clock input/output (direction controlled by eUSCI) | |
| 24 | PM_UCB1STE | eUSCI_B1 SPI slave transmit enable (direction controlled by eUSCI) | |
| 25 | PM_TA0.0 | TA0 CCR0 capture input CCI0A | TA0 CCR0 compare output Out0 |
| 26 | PM_TA0.1 | TA0 CCR1 capture input CCI1A | TA0 CCR1 compare output Out1 |
| 27 | PM_TA0.2 | TA0 CCR2 capture input CCI2A | TA0 CCR2 compare output Out2 |
| 28 | PM_TA1.0 | TA1 CCR0 capture input CCI0A | TA1 CCR0 compare output Out0 |
| 29 | PM_TA2.0 | TA2 CCR0 capture input CCI0A | TA2 CCR0 compare output Out0 |
| 30 | PM_TA3.0 | TA3 CCR0 capture input CCI0A | TA3 CCR0 compare output Out0 |
| 31(0FFh) ⁽¹⁾ | PM_ANALOG | Disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. | |

(1) The value of the PM_ANALOG mnemonic is set to 0FFh. The port mapping registers are only 5 bits wide and the upper bits are ignored, which results in a read value of 31.

Table 16. Default Port Mapping

| PIN NAME | | PxMAPy MNEMONIC | INPUT PIN FUNCTION | OUTPUT PIN FUNCTION |
|----------------------------------|-------------------------------------|----------------------------|--|------------------------------|
| PEU | PZ | | | |
| P2.0/PM_TA0.0 | P2.0/PM_TA0.0/COM4 | PM_TA0.0 | TA0 CCR0 capture input CCI0A | TA0 CCR0 compare output Out0 |
| P2.1/PM_TA0.1 | P2.1/PM_TA0.1/COM5 | PM_TA0.1 | TA0 CCR1 capture input CCI1A | TA0 CCR1 compare output Out1 |
| P2.2/PM_TA0.2 | P2.2/PM_TA0.2/COM6 | PM_TA0.2 | TA0 CCR2 capture input CCI2A | TA0 CCR2 compare output Out2 |
| P2.3/PM_TA1.0 | P2.3/PM_TA1.0/COM7 | PM_TA1.0 | TA1 CCR0 capture input CCI0A | TA1 CCR0 compare output Out0 |
| P2.4/PM_TA2.0 | P1.1/PM_TA2.0/R23 | PM_TA2.0 | TA2 CCR0 capture input CCI0A | TA2 CCR0 compare output Out0 |
| P2.5/PM_UCB0SOMI/ PM_UCB0SCL | P2.0/PM_UCB0SOMI/ PM_UCB0SCL/R13 | PM_UCB0SOMI/ PM_UCB0SCL | eUSCI_B0 SPI slave out master in (direction controlled by eUSCI), eUSCI_B0 I2C clock (open drain and direction controlled by eUSCI) | |
| P2.6/PM_UCB0SIMO/ PM_UCB0SDA | P2.6/PM_UCB0SIMO/ PM_UCB0SDA/R03 | PM_UCB0SIMO/ PM_UCB0SDA | eUSCI_B0 SPI slave in master out (direction controlled by eUSCI), eUSCI_B0 I2C data (open drain and direction controlled by eUSCI) | |
| P2.7/PM_UCB0CLK | P2.7/PM_UCB0CLK/CB2 | PM_UCB0CLK | eUSCI_B0 clock input/output (direction controlled by eUSCI) | |
| P3.0/PM_UCA0RXD/ PM_UCA0SOMI | P3.0/PM_UCA0RXD/ PM_UCA0SOMI | PM_UCA0RXD/ PM_UCA0SOMI | eUSCI_A0 UART RXD (direction controlled by eUSCI – input), eUSCI_A0 SPI slave out master in (direction controlled by eUSCI) | |
| P3.1/PM_UCA0TXD/ PM_UCA0SIMO | P3.1/PM_UCA0TXD/ PM_UCA0SIMO/S39 | PM_UCA0TXD/ PM_UCA0SIMO | eUSCI_A0 UART TXD (direction controlled by eUSCI – output), eUSCI_A0 SPI slave in master out (direction controlled by eUSCI) | |
| P3.2/PM_UCA0CLK | P3.2/PM_UCA0CLK/S38 | PM_UCA0CLK | eUSCI_A0 clock input/output (direction controlled by eUSCI) | |
| P3.3/PM_UCA1CLK | P3.3/PM_UCA1CLK/S37 | PM_UCA1CLK | eUSCI_A1 clock input/output (direction controlled by eUSCI) | |
| P3.4/PM_UCA1RXD/ PM_UCA1SOMI/ | P3.4/PM_UCA1RXD/ PM_UCA1SOMI/S36 | PM_UCA1RXD/ PM_UCA1SOMI | eUSCI_A1 UART RXD (direction controlled by eUSCI – input), eUSCI_A1 SPI slave out master in (direction controlled by eUSCI) | |

Table 16. Default Port Mapping (continued)

| PIN NAME | | PxMAPy MNEMONIC | INPUT PIN FUNCTION | OUTPUT PIN FUNCTION |
|----------------------------------|-------------------------------------|----------------------------|--|------------------------------|
| PEU | PZ | | | |
| P3.5/PM_UCA1TXD/ PM_UCA1SIMO | P3.5/PM_UCA1TXD/ PM_UCA1SIMO/S35 | PM_UCA1TXD/ PM_UCA1SIMO | eUSCI_A1 UART TXD (direction controlled by eUSCI – output), eUSCI_A1 SPI slave in master out (direction controlled by eUSCI) | |
| P3.6/PM_UCA2RXD/ PM_UCA2SOMI/ | P3.6/PM_UCA2RXD/ PM_UCA2SOMI/S34 | PM_UCA2RXD/ PM_UCA2SOMI | eUSCI_A2 UART RXD (direction controlled by eUSCI – input), eUSCI_A2 SPI slave out master in (direction controlled by eUSCI) | |
| P3.7/PM_UCA2TXD/ PM_UCA2SIMO | P3.7/PM_UCA2TXD/ PM_UCA2SIMO/S33 | PM_UCA2TXD/ PM_UCA2SIMO | eUSCI_A2 UART TXD (direction controlled by eUSCI – output), eUSCI_A2 SPI slave in master out (direction controlled by eUSCI) | |
| P4.0/PM_UCA2CLK | P4.0/PM_UCA2CLK/S32 | PM_UCA2CLK | eUSCI_A2 clock input/output (direction controlled by eUSCI) | |
| P4.1/PM_UCA3RXD/ PM_UCA3SOMI/ | P4.1/PM_UCA3RXD/ PM_UCA3SOMI/S31 | PM_UCA3RXD/ PM_UCA3SOMI | eUSCI_A3 UART RXD (direction controlled by eUSCI – input), eUSCI_A3 SPI slave out master in (direction controlled by eUSCI) | |
| P4.2/PM_UCA3TXD/ PM_UCA3SIMO | P4.2/PM_UCA3TXD/ PM_UCA3SIMO/S30 | PM_UCA3TXD/ PM_UCA3SIMO | eUSCI_A3 UART TXD (direction controlled by eUSCI – output), eUSCI_A3 SPI slave in master out (direction controlled by eUSCI) | |
| P4.3/PM_UCA3CLK | P4.3/PM_UCA3CLK/S29 | PM_UCA3CLK | eUSCI_A3 clock input/output (direction controlled by eUSCI) | |
| P4.4/PM_UCB1SOMI/ PM_UCB1SCL | P4.4/PM_UCB1SOMI/ PM_UCB1SCL/S28 | PM_UCB1SOMI/ PM_UCB1SCL | eUSCI_B1 SPI slave out master in (direction controlled by eUSCI), eUSCI_B1 I2C clock (open drain and direction controlled by eUSCI) | |
| P4.5/PM_UCB1SIMO/ PM_UCB1SDA | P4.5/PM_UCB1SIMO/ PM_UCB1SDA/S27 | PM_UCB1SIMO/ PM_UCB1SDA | eUSCI_B1 SPI slave in master out (direction controlled by eUSCI), eUSCI_B1 I2C data (open drain and direction controlled by eUSCI) | |
| P4.6/PM_UCB1CLK | P4.6/PM_UCB1CLK/S26 | PM_UCB1CLK | eUSCI_B1 clock input/output (direction controlled by eUSCI) | |
| P4.7/PM_TA3.0 | P4.7/PM_TA3.0/S25 | PM_TA3.0 | TA3 CCR0 capture input CCI0A | TA3 CCR0 compare output Out0 |

System Module (SYS) ([Link to User's Guide](#))

The SYS module handles many of the system functions within the device. These include power on reset and power up clear handling, NMI source selection and management, reset interrupt vector generators, bootstrap loader entry mechanisms, and configuration management (device descriptors). It also includes a data exchange mechanism using JTAG called a JTAG mailbox that can be used in the application.

Table 17. System Module Interrupt Vector Registers

| INTERRUPT VECTOR REGISTER | ADDRESS | INTERRUPT EVENT | VALUE | PRIORITY |
|--------------------------------|------------|--------------------------------|-------|----------|
| SYSRSTIV , System Reset | 019Eh | No interrupt pending | 00h | |
| | | Brownout (BOR) | 02h | Highest |
| | | RST/NMI (POR) | 04h | |
| | | DoBOR (BOR) | 06h | |
| | | Wakeup from LPMx.5 | 08h | |
| | | Security violation (BOR) | 0Ah | |
| | | SVSL (POR) | 0Ch | |
| | | SVSH (POR) | 0Eh | |
| | | SVML_OVP (POR) | 10h | |
| | | SVMH_OVP (POR) | 12h | |
| | | DoPOR (POR) | 14h | |
| | | WDT timeout (PUC) | 16h | |
| | | WDT key violation (PUC) | 18h | |
| | | KEYV flash key violation (PUC) | 1Ah | |
| | | Reserved | 1Ch | |
| | | Peripheral area fetch (PUC) | 1Eh | |
| | | PMM key violation (PUC) | 20h | |
| Reserved | 22h to 3Eh | Lowest | | |
| SYSSNIV , System NMI | 019Ch | No interrupt pending | 00h | |
| | | SVMLIFG | 02h | Highest |
| | | SVMHIFG | 04h | |
| | | DLYLIFG | 06h | |
| | | DLYHIFG | 08h | |

Table 17. System Module Interrupt Vector Registers (continued)

| INTERRUPT VECTOR REGISTER | ADDRESS | INTERRUPT EVENT | VALUE | PRIORITY |
|---------------------------|---------|----------------------|------------|----------|
| | | VMAIFG | 0Ah | |
| | | JMBINIFG | 0Ch | |
| | | JMBOUTIFG | 0Eh | |
| | | VLRIFG | 10h | |
| | | VLRHIFG | 12h | |
| | | Reserved | 14h to 1Eh | Lowest |
| SYSUNIV, User NMI | 019Ah | No interrupt pending | 00h | |
| | | NMIFG | 02h | Highest |
| | | OFIFG | 04h | |
| | | ACCVIFG | 06h | |
| | | AUXSWGIFG | 08h | |
| | | Reserved | 0Ah to 1Eh | Lowest |

Watchdog Timer (WDT_A) ([Link to User's Guide](#))

The primary function of the watchdog timer is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the timer can be configured as an interval timer and can generate interrupts at selected time intervals.

DMA Controller ([Link to User's Guide](#))

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC10_A conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral.

Table 18. DMA Trigger Assignments⁽¹⁾

| TRIGGER | CHANNEL | | |
|---------|---------------|---------------|---------------|
| | 0 | 1 | 2 |
| 0 | DMAREQ | DMAREQ | DMAREQ |
| 1 | TA0CCR0 CCIFG | TA0CCR0 CCIFG | TA0CCR0 CCIFG |
| 2 | TA0CCR2 CCIFG | TA0CCR2 CCIFG | TA0CCR2 CCIFG |
| 3 | TA1CCR0 CCIFG | TA1CCR0 CCIFG | TA1CCR0 CCIFG |
| 4 | Reserved | Reserved | Reserved |
| 5 | TA2CCR0 CCIFG | TA2CCR0 CCIFG | TA2CCR0 CCIFG |
| 6 | Reserved | Reserved | Reserved |
| 7 | TA3CCR0 CCIFG | TA3CCR0 CCIFG | TA3CCR0 CCIFG |
| 8 | Reserved | Reserved | Reserved |
| 9 | Reserved | Reserved | Reserved |
| 10 | Reserved | Reserved | Reserved |
| 11 | Reserved | Reserved | Reserved |
| 12 | Reserved | Reserved | Reserved |
| 13 | SD24IFG | SD24IFG | SD24IFG |
| 14 | Reserved | Reserved | Reserved |
| 15 | Reserved | Reserved | Reserved |
| 16 | UCA0RXIFG | UCA0RXIFG | UCA0RXIFG |
| 17 | UCA0TXIFG | UCA0TXIFG | UCA0TXIFG |

(1) Reserved DMA triggers may be used by other devices in the family. Reserved DMA triggers do not cause any DMA trigger event when selected.

Table 18. DMA Trigger Assignments⁽¹⁾ (continued)

| TRIGGER | CHANNEL | | |
|---------|------------|------------|------------|
| | 0 | 1 | 2 |
| 18 | UCA1RXIFG | UCA1RXIFG | UCA1RXIFG |
| 19 | UCA1TXIFG | UCA1TXIFG | UCA1TXIFG |
| 20 | UCA2RXIFG | UCA2RXIFG | UCA2RXIFG |
| 21 | UCA2TXIFG | UCA2TXIFG | UCA2TXIFG |
| 22 | UCB0RXIFG0 | UCB0RXIFG0 | UCB0RXIFG0 |
| 23 | UCB0TXIFG0 | UCB0TXIFG0 | UCB0TXIFG0 |
| 24 | ADC10IFG0 | ADC10IFG0 | ADC10IFG0 |
| 25 | UCA3RXIFG | UCA3RXIFG | UCA3RXIFG |
| 26 | UCA3TXIFG | UCA3TXIFG | UCA3TXIFG |
| 27 | UCB1RXIFG0 | UCB1RXIFG0 | UCB1RXIFG0 |
| 28 | UCB1TXIFG0 | UCB1TXIFG0 | UCB1TXIFG0 |
| 29 | MPY ready | MPY ready | MPY ready |
| 30 | DMA2IFG | DMA0IFG | DMA1IFG |
| 31 | Reserved | Reserved | Reserved |

CRC16 (Link to User's Guide)

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 module signature is based on the CRC-CCITT standard.

Hardware Multiplier (Link to User's Guide)

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-bit, 24-bit, 16-bit, and 8-bit operands. The module is capable of supporting signed and unsigned multiplication as well as signed and unsigned multiply and accumulate operations.

Enhanced Universal Serial Communication Interface (eUSCI) (Links to User's Guide: [UART Mode](#), [SPI Mode](#), [I2C Mode](#))

The eUSCI module is used for serial data communication. The eUSCI module supports synchronous communication protocols such as SPI (3 or 4 pin) and I²C, and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection, and IrDA.

The eUSCI_An module provides support for SPI (3 or 4 pin), UART, enhanced UART, and IrDA.

The eUSCI_Bn module provides support for SPI (3 or 4 pin) and I2C.

Four eUSCI_A and two eUSCI_B module are implemented in MSP430F677x devices.

ADC10_A (Link to User's Guide)

The ADC10_A module supports fast, 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator and a conversion results buffer. A window comparator with a lower and upper limit allows CPU independent result monitoring with three window comparator interrupt flags.

SD24_B (Link to User's Guide)

The SD24_B module integrates up to seven independent 24-bit sigma-delta A/D converters. Each converter is designed with a fully differential analog input pair and programmable gain amplifier input stage. Also the converters are based on second-order over-sampling sigma-delta modulators and digital decimation filters. The decimation filters are comb type filters with selectable oversampling ratios of up to 1024.

TA0 (Link to User's Guide)

TA0 is a 16-bit timer/counter (Timer_A type) with three capture/compare registers. TA0 can support multiple capture/compares, PWM outputs, and interval timing. TA0 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 19. TA0 Signal Connections

| DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL |
|---------------------|-------------------|--------------|----------------------|----------------------|
| PM_TACLK | TACLK | Timer | NA | NA |
| ACLK (internal) | ACLK | | | |
| SMCLK (internal) | SMCLK | | | |
| PM_TACLK | INCLK | CCR0 | TA0 | PM_TA0.0 |
| PM_TA0.0 | CCI0A | | | |
| CBOUT (Internal) | CCI0B | | | |
| DVSS | GND | | | |
| DVCC | VCC | CCR1 | TA1 | PM_TA0.1 |
| PM_TA0.1 | CCI1A | | | |
| ACLK (internal) | CCI1B | | | |
| DVSS | GND | | | |
| DVCC | VCC | CCR2 | TA2 | PM_TA0.2 |
| PM_TA0.2 | CCI2A | | | |
| DVSS | CCI2B | | | |
| DVSS | GND | | | |
| DVCC | VCC | | | |

TA1 (Link to User's Guide)

TA1 is a 16-bit timer/counter (Timer_A type) with two capture/compare registers. TA1 can support multiple capture/compares, PWM outputs, and interval timing. TA1 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 20. TA1 Signal Connections

| DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL |
|---------------------|-------------------|--------------|----------------------|----------------------|
| | | | | PZ |
| PM_TACLK | TACLK | Timer | NA | NA |
| ACLK (internal) | ACLK | | | |
| SMCLK (internal) | SMCLK | | | |
| PM_TACLK | INCLK | CCR0 | TA0 | PM_TA1.0 |
| PM_TA1.0 | CCI0A | | | |
| CBOUT (Internal) | CCI0B | | | |
| DVSS | GND | | | |
| DVCC | VCC | CCR1 | TA1 | PM_TA1.1 |
| PM_TA1.1 | CCI1A | | | |
| ACLK (internal) | CCI1B | | | |
| DVSS | GND | | | |
| DVCC | VCC | | | |

TA2 (Link to User's Guide)

TA2 is a 16-bit timer/counter (Timer_A type) with two capture/compare registers. TA2 can support multiple capture/compares, PWM outputs, and interval timing. TA2 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 21. TA2 Signal Connections

| DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL |
|---------------------|-------------------|--------------|----------------------|----------------------|
| PM_TACLK | TACLK | Timer | NA | NA |
| ACLK (internal) | ACLK | | | |
| SMCLK (internal) | SMCLK | | | |
| PM_TACLK | INCLK | CCR0 | TA0 | PM_TA2.0 |
| PM_TA2.0 | CCI0A | | | |
| CBOUT (Internal) | CCI0B | | | |
| DVSS | GND | | | |
| DVCC | VCC | | | |
| PM_TA2.1 | CCI1A | CCR1 | TA1 | PM_TA2.1 |
| ACLK (internal) | CCI1B | | | |
| DVSS | GND | | | |
| DVCC | VCC | | | |

TA3 (Link to User's Guide)

TA3 is a 16-bit timer/counter (Timer_A type) with two capture/compare registers. TA3 can support multiple capture/compares, PWM outputs, and interval timing. TA3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 22. TA3 Signal Connections

| DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL |
|---------------------|-------------------|--------------|----------------------|----------------------|
| PM_TACLK | TACLK | Timer | NA | |
| ACLK (internal) | ACLK | | | |
| SMCLK (internal) | SMCLK | | | |
| PM_TACLK | INCLK | CCR0 | TA0 | PM_TA3.0 |
| PM_TA3.0 | CCI0A | | | |
| CBOUT (Internal) | CCI0B | | | |
| DVSS | GND | | | |
| DVCC | VCC | | | |
| PM_TA3.1 | CCI1A | CCR1 | TA1 | PM_TA3.1 |
| ACLK (internal) | CCI1B | | | |
| DVSS | GND | | | |
| DVCC | VCC | | | |

SD24_B Triggers

Table 23 shows the input trigger connections to SD24_B converters from Timer_A modules and output trigger pulse connection from SD24_B to ADC10_A.

Table 23. SD24_B Input/Output Trigger Connections

| DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL |
|---------------------|--------------------------------------|--------------|----------------------|--|
| TA0.1 (internal) | SD24_B SD24CHx.SD24SCSx = 001b | SD24_B | Trigger Pulse | ADC10_A (internal) ADC10SHSx = 011b |
| TA2.1 (internal) | SD24_B SD24CHx.SD24SCSx = 010b | | | |
| TA3.1 (internal) | SD24_B SD24CHx.SD24SCSx = 011b | | | |

ADC10_A Triggers

Table 24 shows input trigger connections to ADC10_A from Timer_A modules and SD24_B.

Table 24. ADC10_A Input Trigger Connections

| DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK |
|------------------------------------|-----------------------------|--------------|
| TA0.1 (internal) | ADC10_A ADC10SHSx = 001b | ADC10_A |
| TA3.0 (internal) | ADC10_A ADC10SHSx = 010b | |
| SD24_B trigger pulse (internal) | ADC10_A ADC10SHSx = 011b | |

Real-Time Clock (RTC_C) ([Link to User's Guide](#))

The RTC_C module can be configured for real-time clock (RTC) and calendar mode providing seconds, hours, day of week, day of month, month, and year. The RTC_C control and configuration registers are password protected to ensure clock integrity against run away code. Calendar mode integrates an internal calendar that compensates for months with less than 31 days and includes leap year correction. The RTC_C also supports flexible alarm functions, offset calibration, temperature compensation and time capture on two external events. The RTC_C on this device operates on dedicated AUXVCC3 supply and supports operation in LPM3.5.

REF Voltage Reference ([Link to User's Guide](#))

The reference module (REF) is responsible for generation of all critical reference voltages that can be used by the various analog peripherals in the device. These include the ADC10_A, LCD_C, and SD24_B modules.

LCD_C ([Link to User's Guide](#))

The LCD_C driver generates the segment and common signals required to drive a liquid crystal display (LCD). The LCD_C controller has dedicated data memories to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2-mux, 3-mux, 4-mux, up to 8-mux LCDs are supported. The module can provide a LCD voltage independent of the supply voltage with its integrated charge pump. It is possible to control the level of the LCD voltage and thus contrast by software. The module also provides an automatic blinking capability for individual segments in static, 2-mux, 3-mux, and 4-mux modes.

Comparator_B ([Link to User's Guide](#))

The primary function of the Comparator_B module is to support precision slope analog-to-digital conversions, battery voltage supervision, and monitoring of external analog signals.

Embedded Emulation Module (EEM) ([Link to User's Guide](#))

The Embedded Emulation Module (EEM) supports real-time in-system debugging. The L version of the EEM implemented on all devices has the following features:

- Eight hardware triggers or breakpoints on memory access
- Two hardware triggers or breakpoints on CPU register write access
- Up to ten hardware triggers can be combined to form complex triggers or breakpoints
- Two cycle counters
- Sequencer
- State storage
- Clock control on module level

Peripheral File Map
Table 25. Peripherals

| MODULE NAME | BASE ADDRESS | OFFSET ADDRESS RANGE |
|--|--------------|----------------------|
| Special Functions (see Table 26) | 0100h | 000h-01Fh |
| PMM (see Table 27) | 0120h | 000h-01Fh |
| Flash Control (see Table 28) | 0140h | 000h-00Fh |
| CRC16 (see Table 29) | 0150h | 000h-007h |
| RAM Control (see Table 30) | 0158h | 000h-001h |
| Watchdog (see Table 31) | 015Ch | 000h-001h |
| UCS (see Table 32) | 0160h | 000h-01Fh |
| SYS (see Table 33) | 0180h | 000h-01Fh |
| Shared Reference (see Table 34) | 01B0h | 000h-001h |
| Port Mapping Control (see Table 35) | 01C0h | 000h-007h |
| Port Mapping Port P2 (see Table 36) | 01D0h | 000h-007h |
| Port Mapping Port P3 (see Table 37) | 01D8h | 000h-007h |
| Port Mapping Port P4 (see Table 38) | 01E0h | 000h-007h |
| Port P1, P2 (see Table 39) | 0200h | 000h-01Fh |
| Port P3, P4 (see Table 40) | 0220h | 000h-00Bh |
| Port P5, P6 (see Table 41) | 0240h | 000h-00Bh |
| Port P7, P8 (see Table 42) | 0260h | 000h-00Bh |
| Port P9, P10 (see Table 43) (Ports P9 and P10 not available in PZ package) | 0280h | 000h-00Bh |
| Port P11 (see Table 44) (Port P11 not available in PZ package) | 02A0h | 000h-00Bh |
| Port PJ (see Table 45) | 0320h | 000h-01Fh |
| Timer TA0 (see Table 46) | 0340h | 000h-03Fh |
| Timer TA1 (see Table 47) | 0380h | 000h-03Fh |
| Timer TA2 (see Table 48) | 0400h | 000h-03Fh |
| Timer TA3 (see Table 49) | 0440h | 000h-03Fh |
| Backup Memory (see Table 50) | 0480h | 000h-00Fh |
| 32-Bit Hardware Multiplier (see Table 52) | 04C0h | 000h-02Fh |
| DMA General Control (see Table 53) | 0500h | 000h-00Fh |
| DMA Channel 0 (see Table 54) | 0500h | 010h-01Fh |
| DMA Channel 1 (see Table 55) | 0500h | 020h-02Fh |
| DMA Channel 2 (see Table 56) | 0500h | 030h-03Fh |
| RTC_C (see Table 51) | 0C80h | 000h-03Fh |
| eUSCI_A0 (see Table 57) | 05C0h | 000h-01Fh |
| eUSCI_A1 (see Table 58) | 05E0h | 000h-01Fh |
| eUSCI_A2 (see Table 59) | 0600h | 000h-01Fh |
| eUSCI_A3 (see Table 60) | 0620h | 000h-01Fh |
| eUSCI_B0 (see Table 61) | 0640h | 000h-02Fh |
| eUSCI_B1 (see Table 62) | 0680h | 000h-02Fh |
| ADC10_A (see Table 63) | 0740h | 000h-01Fh |
| SD24_B(see Table 64) | 0800h | 000h-06Fh |
| Comparator_B (see Table 65) | 08C0h | 000h-00Fh |
| Auxiliary Supply (see Table 66) | 09E0h | 000h-01Fh |
| LCD_C (see Table 67) | 0A00h | 000h-05Fh |

Table 26. Special Function Registers (Base Address: 0100h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-----------------------|----------|--------|
| SFR interrupt enable | SFRIE1 | 00h |
| SFR interrupt flag | SFRIFG1 | 02h |
| SFR reset pin control | SFRRPCR | 04h |

Table 27. PMM Registers (Base Address: 0120h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------------------|----------|--------|
| PMM Control 0 | PMMCTL0 | 00h |
| PMM control 1 | PMMCTL1 | 02h |
| SVS high side control | SVSMHCTL | 04h |
| SVS low side control | SVSMLCTL | 06h |
| PMM interrupt flags | PMMIFG | 0Ch |
| PMM interrupt enable | PMMIE | 0Eh |
| PMM Power Mode 5 control register 0 | PM5CTL0 | 10h |

Table 28. Flash Control Registers (Base Address: 0140h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| Flash control 1 | FCTL1 | 00h |
| Flash control 3 | FCTL3 | 04h |
| Flash control 4 | FCTL4 | 06h |

Table 29. CRC16 Registers (Base Address: 0150h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|-----------|--------|
| CRC data input | CRC16DI | 00h |
| CRC result | CRCINIRES | 04h |

Table 30. RAM Control Registers (Base Address: 0158h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| RAM control 0 | RCCTL0 | 00h |

Table 31. Watchdog Registers (Base Address: 015Ch)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|------------------------|----------|--------|
| Watchdog timer control | WDTCTL | 00h |

Table 32. UCS Registers (Base Address: 0160h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| UCS control 0 | UCSCTL0 | 00h |
| UCS control 1 | UCSCTL1 | 02h |
| UCS control 2 | UCSCTL2 | 04h |
| UCS control 3 | UCSCTL3 | 06h |
| UCS control 4 | UCSCTL4 | 08h |
| UCS control 5 | UCSCTL5 | 0Ah |
| UCS control 6 | UCSCTL6 | 0Ch |
| UCS control 7 | UCSCTL7 | 0Eh |
| UCS control 8 | UCSCTL8 | 10h |

Table 33. SYS Registers (Base Address: 0180h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------------------|-----------|--------|
| System control | SYSCCTL | 00h |
| Bootstrap loader configuration area | SYSBSLC | 02h |
| JTAG mailbox control | SYSJMBC | 06h |
| JTAG mailbox input 0 | SYSJMBIO | 08h |
| JTAG mailbox input 1 | SYSJMBI1 | 0Ah |
| JTAG mailbox output 0 | SYSJMBO0 | 0Ch |
| JTAG mailbox output 1 | SYSJMBO1 | 0Eh |
| Bus Error vector generator | SYSBERRIV | 18h |
| User NMI vector generator | SYSUNIV | 1Ah |
| System NMI vector generator | SYSSNIV | 1Ch |
| Reset vector generator | SYSRSTIV | 1Eh |

Table 34. Shared Reference Registers (Base Address: 01B0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------|----------|--------|
| Shared reference control | REFCTL | 00h |

Table 35. Port Mapping Controller (Base Address: 01C0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------------|----------|--------|
| Port mapping password register | PMAPPWD | 00h |
| Port mapping control register | PMAPCTL | 02h |

Table 36. Port Mapping for Port P2 (Base Address: 01D0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------|----------|--------|
| Port P2.0 mapping register | P2MAP0 | 00h |
| Port P2.1 mapping register | P2MAP1 | 01h |
| Port P2.2 mapping register | P2MAP2 | 02h |
| Port P2.3 mapping register | P2MAP3 | 03h |
| Port P2.4 mapping register | P2MAP4 | 04h |
| Port P2.5 mapping register | P2MAP5 | 05h |
| Port P2.6 mapping register | P2MAP6 | 06h |
| Port P2.7 mapping register | P2MAP7 | 07h |

Table 37. Port Mapping for Port P3 (Base Address: 01D8h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------|----------|--------|
| Port P3.0 mapping register | P3MAP0 | 00h |
| Port P3.1 mapping register | P3MAP1 | 01h |
| Port P3.2 mapping register | P3MAP2 | 02h |
| Port P3.3 mapping register | P3MAP3 | 03h |
| Port P3.4 mapping register | P3MAP4 | 04h |
| Port P3.5 mapping register | P3MAP5 | 05h |
| Port P3.6 mapping register | P3MAP6 | 06h |
| Port P3.7 mapping register | P3MAP7 | 07h |

Table 38. Port Mapping for Port P4 (Base Address: 01E0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------|----------|--------|
| Port P4.0 mapping register | P4MAP0 | 00h |
| Port P4.1 mapping register | P4MAP1 | 01h |
| Port P4.2 mapping register | P4MAP2 | 02h |
| Port P4.3 mapping register | P4MAP3 | 03h |
| Port P4.4 mapping register | P4MAP4 | 04h |
| Port P4.5 mapping register | P4MAP5 | 05h |
| Port P4.6 mapping register | P4MAP6 | 06h |
| Port P4.7 mapping register | P4MAP7 | 07h |

Table 39. Port P1, P2 Registers (Base Address: 0200h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|------------------------------------|----------|--------|
| Port P1 input | P1IN | 00h |
| Port P1 output | P1OUT | 02h |
| Port P1 direction | P1DIR | 04h |
| Port P1 pullup/pulldown enable | P1REN | 06h |
| Port P1 drive strength | P1DS | 08h |
| Port P1 selection 0 | P1SEL0 | 0Ah |
| Port P1 selection 1 | P1SEL1 | 0Ch |
| Port P1 interrupt vector word | P1IV | 0Eh |
| Port P1 interrupt edge select | P1IES | 18h |
| Port P1 interrupt enable | P1IE | 1Ah |
| Port P1 interrupt flag | P1IFG | 1Ch |
| Port P2 input | P2IN | 01h |
| Port P2 output | P2OUT | 03h |
| Port P2 direction | P2DIR | 05h |
| Port P2 pullup/pulldown enable | P2REN | 07h |
| Port P2 drive strength | P2DS | 09h |
| Port P2 selection 0 | P2SEL0 | 0Bh |
| Port P2 selection 1 ⁽¹⁾ | P2SEL1 | 0Dh |
| Port P2 interrupt vector word | P2IV | 1Eh |
| Port P2 interrupt edge select | P2IES | 19h |
| Port P2 interrupt enable | P2IE | 1Bh |
| Port P2 interrupt flag | P2IFG | 1Dh |

(1) P2SEL1 is an empty control register to be consistent with P1SEL1 in 16-bit access.

Table 40. Port P3, P4 Registers (Base Address: 0220h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------------|----------|--------|
| Port P3 input | P3IN | 00h |
| Port P3 output | P3OUT | 02h |
| Port P3 direction | P3DIR | 04h |
| Port P3 pullup/pulldown enable | P3REN | 06h |
| Port P3 drive strength | P3DS | 08h |
| Port P3 selection 0 | P3SEL0 | 0Ah |
| Port P4 input | P4IN | 01h |
| Port P4 output | P4OUT | 03h |
| Port P4 direction | P4DIR | 05h |
| Port P4 pullup/pulldown enable | P4REN | 07h |
| Port P4 drive strength | P4DS | 09h |
| Port P4 selection 0 | P4SEL0 | 0Bh |

Table 41. Port P5, P6 Registers (Base Address: 0240h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|------------------------------------|----------|--------|
| Port P5 input | P5IN | 00h |
| Port P5 output | P5OUT | 02h |
| Port P5 direction | P5DIR | 04h |
| Port P5 pullup/pulldown enable | P5REN | 06h |
| Port P5 drive strength | P5DS | 08h |
| Port P5 selection 0 | P5SEL0 | 0Ah |
| Port P5 selection 1 | P5SEL1 | 0Ch |
| Port P6 input | P6IN | 01h |
| Port P6 output | P6OUT | 03h |
| Port P6 direction | P6DIR | 05h |
| Port P6 pullup/pulldown enable | P6REN | 07h |
| Port P6 drive strength | P6DS | 09h |
| Port P6 selection 0 | P6SEL0 | 0Bh |
| Port P6 selection 1 ⁽¹⁾ | P6SEL1 | 0Dh |

(1) P6SEL1 is an empty control register to be consistent with P5SEL1 in 16-bit access.

Table 42. Port P7, P8 Registers (Base Address: 0260h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------------|----------|--------|
| Port P7 input | P7IN | 00h |
| Port P7 output | P7OUT | 02h |
| Port P7 direction | P7DIR | 04h |
| Port P7 pullup/pulldown enable | P7REN | 06h |
| Port P7 drive strength | P7DS | 08h |
| Port P7 selection 0 | P7SEL0 | 0Ah |
| Port P8 input | P8IN | 01h |
| Port P8 output | P8OUT | 03h |
| Port P8 direction | P8DIR | 05h |
| Port P8 pullup/pulldown enable | P8REN | 07h |
| Port P8 drive strength | P8DS | 09h |
| Port P8 selection 0 | P8SEL0 | 0Bh |

Table 43. Port P9, P10 Registers (Base Address: 0280h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---------------------------------|----------|--------|
| Port P9 input | P9IN | 00h |
| Port P9 output | P9OUT | 02h |
| Port P9 direction | P9DIR | 04h |
| Port P9 pullup/pulldown enable | P9REN | 06h |
| Port P9 drive strength | P9DS | 08h |
| Port P9 selection 0 | P9SEL0 | 0Ah |
| Port P10 input | P10IN | 01h |
| Port P10 output | P10OUT | 03h |
| Port P10 direction | P10DIR | 05h |
| Port P10 pullup/pulldown enable | P10REN | 07h |
| Port P10 drive strength | P10DS | 09h |
| Port P10 selection 0 | P10SEL0 | 0Bh |

Table 44. Port 11 Registers (Base Address: 02A0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---------------------------------|----------|--------|
| Port P11 input | P11IN | 00h |
| Port P11 output | P11OUT | 02h |
| Port P11 direction | P11DIR | 04h |
| Port P11 pullup/pulldown enable | P11REN | 06h |
| Port P11 drive strength | P11DS | 08h |
| Port P11 selection 0 | P11SEL0 | 0Ah |

Table 45. Port J Registers (Base Address: 0320h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------------|----------|--------|
| Port PJ input | PJIN | 00h |
| Port PJ output | PJOUT | 02h |
| Port PJ direction | PJDIR | 04h |
| Port PJ pullup/pulldown enable | PJREN | 06h |
| Port PJ drive strength | PJDS | 08h |
| Port PJ selection | PJSEL | 0Ah |

Table 46. TA0 Registers (Base Address: 0340h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------|----------|--------|
| TA0 control | TA0CTL | 00h |
| Capture/compare control 0 | TA0CCTL0 | 02h |
| Capture/compare control 1 | TA0CCTL1 | 04h |
| Capture/compare control 2 | TA0CCTL2 | 06h |
| TA0 counter register | TA0R | 10h |
| Capture/compare register 0 | TA0CCR0 | 12h |
| Capture/compare register 1 | TA0CCR1 | 14h |
| Capture/compare register 2 | TA0CCR2 | 16h |
| TA0 expansion register 0 | TA0EX0 | 20h |
| TA0 interrupt vector | TA0IV | 2Eh |

Table 47. TA1 Registers (Base Address: 0380h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------|----------|--------|
| TA1 control | TA1CTL | 00h |
| Capture/compare control 0 | TA1CCTL0 | 02h |
| Capture/compare control 1 | TA1CCTL1 | 04h |
| TA1 counter register | TA1R | 10h |
| Capture/compare register 0 | TA1CCR0 | 12h |
| Capture/compare register 1 | TA1CCR1 | 14h |
| TA1 expansion register 0 | TA1EX0 | 20h |
| TA1 interrupt vector | TA1IV | 2Eh |

Table 48. TA2 Registers (Base Address: 0400h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------|----------|--------|
| TA2 control | TA2CTL | 00h |
| Capture/compare control 0 | TA2CCTL0 | 02h |
| Capture/compare control 1 | TA2CCTL1 | 04h |
| TA2 counter register | TA2R | 10h |
| Capture/compare register 0 | TA2CCR0 | 12h |
| Capture/compare register 1 | TA2CCR1 | 14h |
| TA2 expansion register 0 | TA2EX0 | 20h |
| TA2 interrupt vector | TA2IV | 2Eh |

Table 49. TA3 Registers (Base Address: 0440h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------|----------|--------|
| TA3 control | TA3CTL | 00h |
| Capture/compare control 0 | TA3CCTL0 | 02h |
| Capture/compare control 1 | TA3CCTL1 | 04h |
| TA3 counter register | TA3R | 10h |
| Capture/compare register 0 | TA3CCR0 | 12h |
| Capture/compare register 1 | TA3CCR1 | 14h |
| TA3 expansion register 0 | TA3EX0 | 20h |
| TA3 interrupt vector | TA3IV | 2Eh |

Table 50. Backup Memory Registers (Base Address: 0480h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| Backup Memory 0 | BAKMEM0 | 00h |
| Backup Memory 1 | BAKMEM1 | 02h |
| Backup Memory 2 | BAKMEM2 | 04h |
| Backup Memory 3 | BAKMEM3 | 06h |

Table 51. RTC_C Registers (Base Address: 0C80h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|-------------|--------|
| RTC control 0 | RTCCTL0 | 00h |
| RTC password | RTCPWD | 01h |
| RTC control 1 | RTCCTL1 | 02h |
| RTC control 3 | RTCCTL3 | 03h |
| RTC offset calibration | RTCOCAL | 04h |
| RTC temperature compensation | RTCTCMP | 06h |
| RTC prescaler 0 control | RTCPS0CTL | 08h |
| RTC prescaler 1 control | RTCPS1CTL | 0Ah |
| RTC prescaler 0 | RTCPS0 | 0Ch |
| RTC prescaler 1 | RTCPS1 | 0Dh |
| RTC interrupt vector word | RTCIV | 0Eh |
| RTC seconds | RTCSEC | 10h |
| RTC minutes | RTCMIN | 11h |
| RTC hours | RTCHOUR | 12h |
| RTC day of week | RTCDOW | 13h |
| RTC days | RTCDAY | 14h |
| RTC month | RTCMON | 15h |
| RTC year | RTCYEAR | 16h |
| RTC alarm minutes | RTCAMIN | 18h |
| RTC alarm hours | RTCAHOUR | 19h |
| RTC alarm day of week | RTCADOW | 1Ah |
| RTC alarm days | RTCADAY | 1Bh |
| Binary-to-BCD conversion register | BIN2BCD | 1Ch |
| BCD-to-Binary conversion register | BCD2BIN | 1Eh |
| Real-Time Clock Time Capture Control Register | RTCTCCTL | 20h |
| Tamper Detect Pin 0 Control Register | RTCCAP0CTL | 21h |
| Tamper Detect Pin 1 Control Register | RTCCAP1CTL | 22h |
| RTC seconds Backup Register 0 | RTCSECBAK0 | 30h |
| RTC minutes Backup Register 0 | RTCMINBAK0 | 31h |
| RTC hours Backup Register 0 | RTCHOURBAK0 | 32h |
| RTC days Backup Register 0 | RTCDAYBAK0 | 33h |
| RTC month Backup Register 0 | RTCMONBAK0 | 34h |
| RTC year Backup Register 0 | RTCYEARBAK0 | 36h |
| RTC seconds Backup Register 1 | RTCSECBAK1 | 38h |
| RTC minutes Backup Register 1 | RTCMINBAK1 | 39h |
| RTC hours Backup Register 1 | RTCHOURBAK1 | 3Ah |
| RTC days Backup Register 1 | RTCDAYBAK1 | 3Bh |
| RTC month Backup Register 1 | RTCMONBAK1 | 3Ch |
| RTC year Backup Register 1 | RTCYEARBAK1 | 3Eh |

Table 52. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|-----------|--------|
| 16-bit operand 1 – multiply | MPY | 00h |
| 16-bit operand 1 – signed multiply | MPYS | 02h |
| 16-bit operand 1 – multiply accumulate | MAC | 04h |
| 16-bit operand 1 – signed multiply accumulate | MACS | 06h |
| 16-bit operand 2 | OP2 | 08h |
| 16 × 16 result low word | RESLO | 0Ah |
| 16 × 16 result high word | RESHI | 0Ch |
| 16 × 16 sum extension register | SUMEXT | 0Eh |
| 32-bit operand 1 – multiply low word | MPY32L | 10h |
| 32-bit operand 1 – multiply high word | MPY32H | 12h |
| 32-bit operand 1 – signed multiply low word | MPYS32L | 14h |
| 32-bit operand 1 – signed multiply high word | MPYS32H | 16h |
| 32-bit operand 1 – multiply accumulate low word | MAC32L | 18h |
| 32-bit operand 1 – multiply accumulate high word | MAC32H | 1Ah |
| 32-bit operand 1 – signed multiply accumulate low word | MACS32L | 1Ch |
| 32-bit operand 1 – signed multiply accumulate high word | MACS32H | 1Eh |
| 32-bit operand 2 – low word | OP2L | 20h |
| 32-bit operand 2 – high word | OP2H | 22h |
| 32 × 32 result 0 – least significant word | RES0 | 24h |
| 32 × 32 result 1 | RES1 | 26h |
| 32 × 32 result 2 | RES2 | 28h |
| 32 × 32 result 3 – most significant word | RES3 | 2Ah |
| MPY32 control register 0 | MPY32CTL0 | 2Ch |

Table 53. DMA General Control Registers (Base Address: 0500h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| DMA module control 0 | DMACTL0 | 00h |
| DMA module control 1 | DMACTL1 | 02h |
| DMA module control 2 | DMACTL2 | 04h |
| DMA module control 3 | DMACTL3 | 06h |
| DMA module control 4 | DMACTL4 | 08h |
| DMA interrupt vector | DMAIV | 0Eh |

Table 54. DMA Channel 0 Registers (Base Address: 0500h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--|----------|--------|
| DMA channel 0 control | DMA0CTL | 10h |
| DMA channel 0 source address low | DMA0SAL | 12h |
| DMA channel 0 source address high | DMA0SAH | 14h |
| DMA channel 0 destination address low | DMA0DAL | 16h |
| DMA channel 0 destination address high | DMA0DAH | 18h |
| DMA channel 0 transfer size | DMA0SZ | 1Ah |

Table 55. DMA Channel 1 Registers (Base Address: 0500h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--|----------|--------|
| DMA channel 1 control | DMA1CTL | 20h |
| DMA channel 1 source address low | DMA1SAL | 22h |
| DMA channel 1 source address high | DMA1SAH | 24h |
| DMA channel 1 destination address low | DMA1DAL | 26h |
| DMA channel 1 destination address high | DMA1DAH | 28h |
| DMA channel 1 transfer size | DMA1SZ | 2Ah |

Table 56. DMA Channel 2 Registers (Base Address: 0500h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--|----------|--------|
| DMA channel 2 control | DMA2CTL | 30h |
| DMA channel 2 source address low | DMA2SAL | 32h |
| DMA channel 2 source address high | DMA2SAH | 34h |
| DMA channel 2 destination address low | DMA2DAL | 36h |
| DMA channel 2 destination address high | DMA2DAH | 38h |
| DMA channel 2 transfer size | DMA2SZ | 3Ah |

Table 57. eUSCI_A0 Registers (Base Address: 05C0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|------------------------------|------------|--------|
| USCI_A control word 0 | UCA0CTLW0 | 00h |
| USCI_A control word 1 | UCA0CTLW1 | 02h |
| USCI_A baud rate 0 | UCA0BR0 | 06h |
| USCI_A baud rate 1 | UCA0BR1 | 07h |
| USCI_A modulation control | UCA0MCTLW | 08h |
| USCI_A status | UCA0STAT | 0Ah |
| USCI_A receive buffer | UCA0RXBUF | 0Ch |
| USCI_A transmit buffer | UCA0TXBUF | 0Eh |
| USCI_A LIN control | UCA0ABCTL | 10h |
| USCI_A IrDA transmit control | UCA0IRTCTL | 12h |
| USCI_A IrDA receive control | UCA0IRRCTL | 13h |
| USCI_A interrupt enable | UCA0IE | 1Ah |
| USCI_A interrupt flags | UCA0IFG | 1Ch |
| USCI_A interrupt vector word | UCA0IV | 1Eh |

Table 58. eUSCI_A1 Registers (Base Address:05E0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|------------------------------|------------|--------|
| USCI_A control word 0 | UCA1CTLW0 | 00h |
| USCI_A control word 1 | UCA1CTLW1 | 02h |
| USCI_A baud rate 0 | UCA1BR0 | 06h |
| USCI_A baud rate 1 | UCA1BR1 | 07h |
| USCI_A modulation control | UCA1MCTLW | 08h |
| USCI_A status | UCA1STAT | 0Ah |
| USCI_A receive buffer | UCA1RXBUF | 0Ch |
| USCI_A transmit buffer | UCA1TXBUF | 0Eh |
| USCI_A LIN control | UCA1ABCTL | 10h |
| USCI_A IrDA transmit control | UCA1IRTCTL | 12h |
| USCI_A IrDA receive control | UCA1IRRCTL | 13h |
| USCI_A interrupt enable | UCA1IE | 1Ah |
| USCI_A interrupt flags | UCA1IFG | 1Ch |
| USCI_A interrupt vector word | UCA1IV | 1Eh |

Table 59. eUSCI_A2 Registers (Base Address:0600h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|------------------------------|------------|--------|
| USCI_A control word 0 | UCA2CTLW0 | 00h |
| USCI_A control word 1 | UCA2CTLW1 | 02h |
| USCI_A baud rate 0 | UCA2BR0 | 06h |
| USCI_A baud rate 1 | UCA2BR1 | 07h |
| USCI_A modulation control | UCA2MCTLW | 08h |
| USCI_A status | UCA2STAT | 0Ah |
| USCI_A receive buffer | UCA2RXBUF | 0Ch |
| USCI_A transmit buffer | UCA2TXBUF | 0Eh |
| USCI_A LIN control | UCA2ABCTL | 10h |
| USCI_A IrDA transmit control | UCA2IRTCTL | 12h |
| USCI_A IrDA receive control | UCA2IRRCTL | 13h |
| USCI_A interrupt enable | UCA2IE | 1Ah |
| USCI_A interrupt flags | UCA2IFG | 1Ch |
| USCI_A interrupt vector word | UCA2IV | 1Eh |

Table 60. eUSCI_A3 Registers (Base Address: 0620h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|------------------------------|------------|--------|
| USCI_A control word 0 | UCA2CTLW0 | 00h |
| USCI_A control word 1 | UCA2CTLW1 | 02h |
| USCI_A baud rate 0 | UCA2BR0 | 06h |
| USCI_A baud rate 1 | UCA2BR1 | 07h |
| USCI_A modulation control | UCA2MCTLW | 08h |
| USCI_A status | UCA2STAT | 0Ah |
| USCI_A receive buffer | UCA2RXBUF | 0Ch |
| USCI_A transmit buffer | UCA2TXBUF | 0Eh |
| USCI_A LIN control | UCA2ABCTL | 10h |
| USCI_A IrDA transmit control | UCA2IRTCTL | 12h |
| USCI_A IrDA receive control | UCA2IRRCTL | 13h |
| USCI_A interrupt enable | UCA2IE | 1Ah |
| USCI_A interrupt flags | UCA2IFG | 1Ch |
| USCI_A interrupt vector word | UCA2IV | 1Eh |

Table 61. eUSCI_B0 Registers (Base Address: 0640h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------------|-------------|--------|
| USCI_B control word 0 | UCB0CTLW0 | 00h |
| USCI_B control word 1 | UCB0CTLW1 | 02h |
| USCI_B bit rate 0 | UCB0BR0 | 06h |
| USCI_B bit rate 1 | UCB0BR1 | 07h |
| USCI_B status word | UCB0STATW | 08h |
| USCI_B byte counter threshold | UCB0TBCNT | 0Ah |
| USCI_B receive buffer | UCB0RXBUF | 0Ch |
| USCI_B transmit buffer | UCB0TXBUF | 0Eh |
| USCI_B I2C own address 0 | UCB0I2COA0 | 14h |
| USCI_B I2C own address 1 | UCB0I2COA1 | 16h |
| USCI_B I2C own address 2 | UCB0I2COA2 | 18h |
| USCI_B I2C own address 3 | UCB0I2COA3 | 1Ah |
| USCI_B received address | UCB0ADDRX | 1Ch |
| USCI_B address mask | UCB0ADDMASK | 1Eh |
| USCI I2C slave address | UCB0I2CSA | 20h |
| USCI interrupt enable | UCB0IE | 2Ah |
| USCI interrupt flags | UCB0IFG | 2Ch |
| USCI interrupt vector word | UCB0IV | 2Eh |

Table 62. eUSCI_B1 Registers (Base Address: 0680h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------------|-------------|--------|
| USCI_B control word 0 | UCB0CTLW0 | 00h |
| USCI_B control word 1 | UCB0CTLW1 | 02h |
| USCI_B bit rate 0 | UCB0BR0 | 06h |
| USCI_B bit rate 1 | UCB0BR1 | 07h |
| USCI_B status word | UCB0STATW | 08h |
| USCI_B byte counter threshold | UCB0TBCNT | 0Ah |
| USCI_B receive buffer | UCB0RXBUF | 0Ch |
| USCI_B transmit buffer | UCB0TXBUF | 0Eh |
| USCI_B I2C own address 0 | UCB0I2COA0 | 14h |
| USCI_B I2C own address 1 | UCB0I2COA1 | 16h |
| USCI_B I2C own address 2 | UCB0I2COA2 | 18h |
| USCI_B I2C own address 3 | UCB0I2COA3 | 1Ah |
| USCI_B received address | UCB0ADDRX | 1Ch |
| USCI_B address mask | UCB0ADDMASK | 1Eh |
| USCI I2C slave address | UCB0I2CSA | 20h |
| USCI interrupt enable | UCB0IE | 2Ah |
| USCI interrupt flags | UCB0IFG | 2Ch |
| USCI interrupt vector word | UCB0IV | 2Eh |

Table 63. ADC10_A Registers (Base Address: 0740h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--|------------|--------|
| ADC10_A Control register 0 | ADC10CTL0 | 00h |
| ADC10_A Control register 1 | ADC10CTL1 | 02h |
| ADC10_A Control register 2 | ADC10CTL2 | 04h |
| ADC10_A Window Comparator Low Threshold | ADC10LO | 06h |
| ADC10_A Window Comparator High Threshold | ADC10HI | 08h |
| ADC10_A Memory Control Register 0 | ADC10MCTL0 | 0Ah |
| ADC10_A Conversion Memory Register | ADC10MCTL0 | 12h |
| ADC10_A Interrupt Enable | ADC10IE | 1Ah |
| ADC10_A Interrupt Flags | ADC10IGH | 1Ch |
| ADC10_A Interrupt Vector Word | ADC10IV | 1Eh |

Table 64. SD24_B Registers (Base Address: 0800h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|-------------|--------|
| SD24_B Control 0 register | SD24BCTL0 | 00h |
| SD24_B Control 1 register | SD24BCTL1 | 02h |
| SD24_B Trigger Control register | SD24BTRGCTL | 04h |
| SD24_B Trigger OSR Control register | SD24BTRGOSR | 06h |
| SD24_B Trigger Preload register | SD24BTRGPRE | 08h |
| SD24_B interrupt flag register | SD24BIFG | 0Ah |
| SD24_B interrupt enable register | SD24BIE | 0Ch |
| SD24_B Interrupt Vector register | SD24BIV | 0Eh |
| SD24_B converter 0 Control register | SD24BCCTL0 | 10h |
| SD24_B converter 0 Input Control register | SD24BINCTL0 | 12h |
| SD24_B converter 0 OSR Control register | SD24BOSR0 | 14h |
| SD24_B converter 0 Preload register | SD24BPRE0 | 16h |
| SD24_B converter 1 Control register | SD24BCCTL1 | 18h |
| SD24_B Converter 1 Input Control register | SD24BINCTL1 | 1Ah |
| SD24_B Converter 1 OSR Control register | SD24BOSR1 | 1Ch |
| SD24_B Converter 1 Preload register | SD24BPRE1 | 1Eh |
| SD24_B Converter 2 Control register | SD24BCCTL2 | 20h |
| SD24_B Converter 2 Input Control register | SD24BINCTL2 | 22h |
| SD24_B Converter 2 OSR Control register | SD24BOSR2 | 24h |
| SD24_B Converter 2 Preload register | SD24BPRE2 | 26h |
| SD24_B converter 3 Control register | SD24BCCTL3 | 28h |
| SD24_B converter 3 Input Control register | SD24BINCTL3 | 2Ah |
| SD24_B converter 3 OSR Control register | SD24BOSR3 | 2Ch |
| SD24_B converter 3 Preload register | SD24BPRE3 | 2Eh |
| SD24_B converter 4 Control register | SD24BCCTL4 | 30h |
| SD24_B Converter 4 Input Control register | SD24BINCTL4 | 32h |
| SD24_B Converter 4 OSR Control register | SD24BOSR4 | 34h |
| SD24_B Converter 4 Preload register | SD24BPRE4 | 36h |
| SD24_B Converter 5 Control register | SD24BCCTL5 | 38h |
| SD24_B Converter 5 Input Control register | SD24BINCTL5 | 3Ah |
| SD24_B Converter 5 OSR Control register | SD24BOSR5 | 3Ch |
| SD24_B Converter 5 Preload register | SD24BPRE5 | 3Eh |
| SD24_B Converter 6 Control register | SD24BCCTL6 | 40h |
| SD24_B Converter 6 Input Control register | SD24BINCTL6 | 42h |
| SD24_B Converter 6 OSR Control register | SD24BOSR6 | 44h |
| SD24_B Converter 6 Preload register | SD24BPRE6 | 46h |
| SD24_B Converter 0 Conversion Memory Low Word register | SD24BMEML0 | 50h |
| SD24_B Converter 0 Conversion Memory High Word register | SD24BMEMH0 | 52h |
| SD24_B Converter 1 Conversion Memory Low Word register | SD24BMEML1 | 54h |
| SD24_B Converter 1 Conversion Memory High Word register | SD24BMEMH1 | 56h |
| SD24_B Converter 2 Conversion Memory Low Word register | SD24BMEML2 | 58h |
| SD24_B Converter 2 Conversion Memory High Word register | SD24BMEMH2 | 5Ah |
| SD24_B Converter 3 Conversion Memory Low Word register | SD24BMEML3 | 5Ch |
| SD24_B Converter 3 Conversion Memory High Word register | SD24BMEMH3 | 5Eh |
| SD24_B Converter 4 Conversion Memory Low Word register | SD24BMEML4 | 60h |
| SD24_B Converter 4 Conversion Memory High Word register | SD24BMEMH4 | 62h |
| SD24_B Converter 5 Conversion Memory Low Word register | SD24BMEML5 | 64h |

Table 64. SD24_B Registers (Base Address: 0800h) (continued)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|------------|--------|
| SD24_B Converter 5 Conversion Memory High Word register | SD24BMEMH5 | 66h |
| SD24_B Converter 6 Conversion Memory Low Word register | SD24BMEML6 | 68h |
| SD24_B Converter 6 Conversion Memory High Word register | SD24BMEMH6 | 6Ah |

Table 65. Comparator_B Register (Base Address: 08C0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|------------------------------|----------|--------|
| Comp_B control register 0 | CBCTL0 | 00h |
| Comp_B control register 1 | CBCTL1 | 02h |
| Comp_B control register 2 | CBCTL2 | 04h |
| Comp_B control register 3 | CBCTL3 | 06h |
| Comp_B interrupt register | CBINT | 0Ch |
| Comp_B interrupt vector word | CBIV | 0Eh |

Table 66. Auxiliary Supply Registers (Base Address: 09E0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------------------|-----------|--------|
| Auxiliary Supply Control 0 register | AUXCTL0 | 00h |
| Auxiliary Supply Control 1 register | AUXCTL1 | 02h |
| Auxiliary Supply Control 2 register | AUXCTL2 | 04h |
| AUX2 Charger Control | AUX2CHCTL | 12h |
| AUX3 Charger Control | AUX3CHCTL | 14h |
| AUX ADC Control | AUXADCCTL | 16h |
| AUX Interrupt Flag | AUXIFG | 1Ah |
| AUX Interrupt Enable | AUXIE | 1Ch |
| AUX Interrupt Vector Word | AUXIV | 1Eh |

Table 67. LCD_C Registers (Base Address: 0A00h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|------------------------------------|------------|--------|
| LCD_C control register 0 | LCDCCTL0 | 000h |
| LCD_C control register 1 | LCDCCTL1 | 002h |
| LCD_C blinking control register | LCDCBLKCTL | 004h |
| LCD_C memory control register | LCDCMEMCTL | 006h |
| LCD_C voltage control register | LCDCVCTL | 008h |
| LCD_C port control 0 | LCDCPCTL0 | 00Ah |
| LCD_C port control 1 | LCDCPCTL1 | 00Ch |
| LCD_C port control 2 | LCDCPCTL2 | 00Eh |
| LCD_C charge pump control register | LCDCCPCTL | 012h |
| LCD_C interrupt vector | LCDCIV | 01Eh |
| Static and 2 to 4 mux modes | | |
| LCD_C memory 1 | LCDM1 | 020h |
| LCD_C memory 2 | LCDM2 | 021h |
| ⋮ | ⋮ | ⋮ |
| LCD_C memory 20 | LCDM20 | 033h |
| LCD_C blinking memory 1 | LCDBM1 | 040h |
| LCD_C blinking memory 2 | LCDBM2 | 041h |
| ⋮ | ⋮ | ⋮ |
| LCD_C blinking memory 20 | LCDBM20 | 053h |
| 5 to 8 mux modes | | |
| LCD_C memory 1 | LCDM1 | 020h |
| LCD_C memory 2 | LCDM2 | 021h |
| ⋮ | ⋮ | ⋮ |
| LCD_C memory 40 | LCDM40 | 047h |

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | |
|---|-----------------------------------|
| Voltage applied at DVCC to DVSS | –0.3 V to 4.1 V |
| Voltage applied to any pin (excluding VCORE) ⁽²⁾ | –0.3 V to V _{CC} + 0.3 V |
| Diode current at any device pin | ±2 mA |
| Storage temperature range, T _{stg} ⁽³⁾ | –55°C to 105°C |
| Maximum junction temperature, T _J | 95°C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages referenced to V_{SS}. V_{CORE} is for internal device use only. No external DC loading or voltage should be applied.
- (3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

Recommended Operating Conditions

Typical values are specified at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

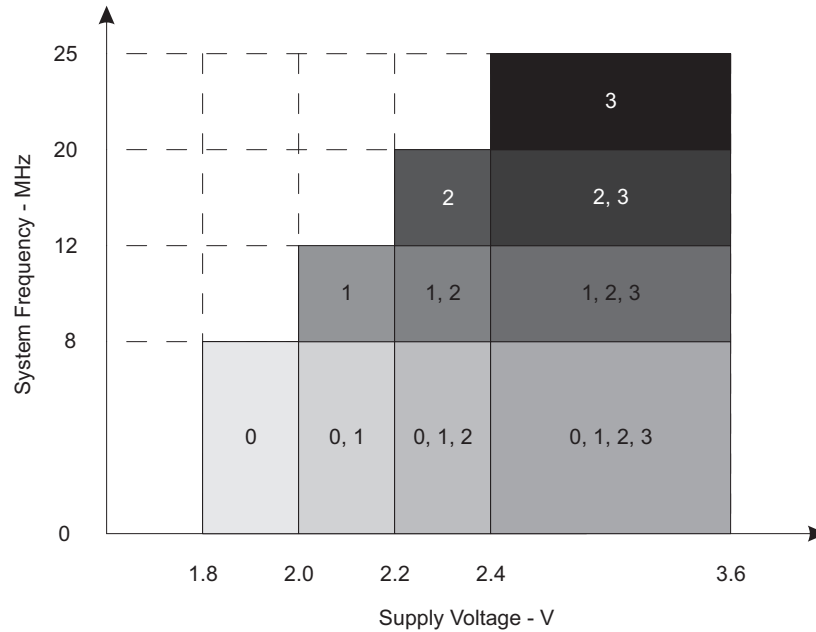
| | | MIN | NOM | MAX | UNIT |
|---|--|--|-----|---------------------------|------|
| V _{CC} | Supply voltage during program execution and flash programming. V _{AVCC} = V _{DVCC} = V _{CC} ⁽¹⁾⁽²⁾ | PMMCOREVx = 0 | 1.8 | 3.6 | V |
| | | PMMCOREVx = 0, 1 | 2.0 | 3.6 | V |
| | | PMMCOREVx = 0, 1, 2 | 2.2 | 3.6 | V |
| | | PMMCOREVx = 0, 1, 2, 3 | 2.4 | 3.6 | V |
| V _{SS} | Supply voltage V _{AVSS} = V _{DVSS} = V _{SS} | | 0 | | V |
| T _A | Operating free-air temperature | I version | –40 | 85 | °C |
| T _J | Operating junction temperature | I version | –40 | 85 | °C |
| C _{VCORE} | Recommended capacitor at VCORE | | 470 | | nF |
| C _{DVCC} / C _{VCORE} | Capacitor ratio of DVCC to VCORE | | 10 | | |
| f _{SYSTEM} | Processor frequency (maximum MCLK frequency) ^{(3) (4)} (see Figure 3) | PMMCOREVx = 0, 1.8 V ≤ V _{CC} ≤ 3.6 V (default condition) | 0 | 8.0 | MHz |
| | | PMMCOREVx = 1, 2 V ≤ V _{CC} ≤ 3.6 V | 0 | 12.0 | |
| | | PMMCOREVx = 2, 2.2 V ≤ V _{CC} ≤ 3.6 V | 0 | 20.0 | |
| | | PMMCOREVx = 3, 2.4 V ≤ V _{CC} ≤ 3.6 V | 0 | 25.0 | |
| I _{LOAD, DVCCD} | Maximum load current that can be drawn from DVCC for core and IO (I _{LOAD} = I _{CORE} + I _{IO}) | | | 20 | mA |
| I _{LOAD, AUX1D} | Maximum load current that can be drawn from AUXVCC1 for core and IO (I _{LOAD} = I _{CORE} + I _{IO}) | | | 20 | mA |
| I _{LOAD, AUX2D} | Maximum load current that can be drawn from AUXVCC2 for core and IO (I _{LOAD} = I _{CORE} + I _{IO}) | | | 20 | mA |
| I _{LOAD, AVCCA} | Maximum load current that can be drawn from AVCC for analog modules (I _{LOAD} = I _{Modules}) | | | 10 | mA |
| I _{LOAD, AUX1A} | Maximum load current that can be drawn from AUXVCC1 for analog modules (I _{LOAD} = I _{Modules}) | | | 5 | mA |
| I _{LOAD, AUX2A} | Maximum load current that can be drawn from AUXVCC2 for analog modules (I _{LOAD} = I _{Modules}) | | | 5 | mA |
| P _{INT} | Internal power dissipation | | | V _{CC} × I(DVCC) | W |

- (1) It is recommended to power AVCC and DVCC from the same source. A maximum difference of 0.3 V between V(AVCC) and V(DVCC) can be tolerated during power up and operation.
- (2) The minimum supply voltage is defined by the supervisor SVS levels when it is enabled. See the [PMM, SVS High Side](#) threshold parameters for the exact values and further details.
- (3) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse duration of the specified maximum frequency.
- (4) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.

Recommended Operating Conditions (continued)

Typical values are specified at $V_{CC} = 3.3\text{ V}$ and $T_A = 25^\circ\text{C}$ (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|-----------|---|-----|-----|--|------|
| P_{IO} | I/O power dissipation of the I/O pins powered by DVCC | | | $(V_{CC} - V_{IOH}) \times I_{IOH} + V_{IOL} \times I_{IOL}$ | W |
| P_{MAX} | Maximum allowed power dissipation, $P_{MAX} > P_{IO} + P_{INT}$ | | | $(T_J - T_A)/\theta_{JA}$ | W |



The numbers within the fields denote the supported PMMCOREVx settings.

Figure 3. Maximum System Frequency

Electrical Characteristics

Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)⁽¹⁾⁽²⁾⁽³⁾

| PARAMETER | EXECUTION MEMORY | V_{CC} | PMMCOREV _x | FREQUENCY ($f_{DCO} = f_{MCLK} = f_{SMCLK}$) | | | | | | | | | | UNIT |
|-----------------------|------------------|----------|-----------------------|--|------|-------|------|--------|------|--------|-----|--------|-------|------|
| | | | | 1 MHz | | 8 MHz | | 12 MHz | | 20 MHz | | 25 MHz | | |
| | | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{AM, Flash}^{(4)}$ | Flash | 3 V | 0 | 0.32 | 0.50 | 2.08 | 2.84 | | | | | | | mA |
| | | | 1 | 0.35 | | 2.35 | | 3.50 | 4.76 | | | | | |
| | | | 2 | 0.39 | | 2.68 | | 3.99 | | 6.61 | 8.3 | | | |
| | | | 3 | 0.41 | | 2.83 | | 4.22 | | 6.98 | | 8.67 | 11.75 | |
| $I_{AM, RAM}^{(5)}$ | RAM | 3 V | 0 | 0.19 | | 1.04 | | | | | | | mA | |
| | | | 1 | 0.21 | | 1.20 | | 1.77 | | | | | | |
| | | | 2 | 0.23 | | 1.38 | | 2.04 | | 3.35 | | | | |
| | | | 3 | 0.24 | | 1.47 | | 2.18 | | 3.58 | | 4.44 | | |

- (1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.
- (2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
- (3) Characterized with program executing typical data processing.
 $f_{ACLK} = 32786\text{ Hz}$, $f_{DCO} = f_{MCLK} = f_{SMCLK}$ at specified frequency.
 $XTS = CPUOFF = SCG0 = SCG1 = OSCOFF = SMCLKOFF = 0$.
- (4) Active mode supply current when program executes in flash at a nominal supply voltage of 3.0V.
- (5) Active mode supply current when program executes in RAM at a nominal supply voltage of 3.0V.

Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current

 over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾⁽²⁾

| PARAMETER | V_{CC} | PMMCOREVx | Temperature (T_A) | | | | | | UNIT |
|---|----------|-----------|-----------------------|-----|------|-----|----------|---------|------|
| | | | -40°C | | 25°C | | 85°C | | |
| | | | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM0,1MHz}$ Low-power mode 0 ^{(3) (4)} | 2.2 V | 0 | 70 | | 75 | | 86 | μA | |
| | 3 V | 3 | 81 | | 87 | 105 | 100 130 | | |
| I_{LPM2} Low-power mode 2 ^{(5) (4)} | 2.2 V | 0 | 5.9 | | 6.5 | | 12.5 | μA | |
| | 3 V | 3 | 6.7 | | 7.3 | 18 | 13.8 30 | | |
| $I_{LPM3,XT1LF}$ Low-power mode 3, crystal mode ^{(6) (4)} | 2.2 V | 0 | 1.50 | | 2.0 | | 7.8 | μA | |
| | | 1 | 1.65 | | 2.2 | | 8.3 | | |
| | | 2 | 1.80 | | 2.4 | | 8.6 | | |
| | | 3 | 1.84 | | 2.4 | | 8.6 | | |
| $I_{LPM3,XT1LF}$ Low-power mode 3, crystal mode ^{(6) (4)} | 3 V | 0 | 2.0 | | 2.5 | | 8.5 | μA | |
| | | 1 | 2.1 | | 2.7 | | 9.0 | | |
| | | 2 | 2.3 | | 2.9 | | 9.3 | | |
| | | 3 | 2.3 | | 2.9 | | 9.3 25 | | |
| $I_{LPM3,VLO}$ Low-power mode 3, VLO mode ^{(7) (4)} | 3 V | 0 | 1.3 | | 1.7 | | 7.5 | μA | |
| | | 1 | 1.3 | | 1.8 | | 7.9 | | |
| | | 2 | 1.4 | | 1.9 | | 8.2 | | |
| | | 3 | 1.4 | | 1.9 | | 8.2 25.0 | | |
| I_{LPM4} Low-power mode 4 ^{(8) (4)} | 3 V | 0 | 1.2 | | 1.6 | | 7.4 | μA | |
| | | 1 | 1.2 | | 1.7 | | 7.8 | | |
| | | 2 | 1.3 | | 1.7 | | 7.9 | | |
| | | 3 | 1.3 | | 1.7 | | 8.0 23.0 | | |
| $I_{LPM3.5}$ Low-power mode 3.5, RTC active on AUXVCC3 ⁽⁹⁾ | 2.2V | | 0.7 | | 0.9 | | 1.4 | μA | |
| | 3.0V | | 1.0 | | 1.2 | 1.5 | 1.8 3.0 | | |
| $I_{LPM4.5}$ Low-power mode 4.5 ⁽¹⁰⁾ | 3.0V | | 0.6 | | 0.7 | 1.0 | 1.2 2.0 | μA | |

- (1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.
- (2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
- (3) Current for watchdog timer clocked by SMCLK included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVE_x = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0); f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 1 MHz
- (4) Current for brownout, high side supervisor (SVSH) normal mode included. Low side supervisor and monitors disabled (SVSL, SVM_L). High side monitor disabled (SVM_H). RAM retention enabled.
- (5) Current for watchdog timer and RTC clocked by ACLK included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVE_x = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 (LPM2); f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 0 MHz; DCO setting = 1 MHz operation, DCO bias generator enabled.
- (6) Current for watchdog timer and RTC clocked by low frequency clock included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVE_x = 0). CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3); f_{ACLK} = 32768 Hz, f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz
- (7) Current for watchdog timer and RTC clocked by low frequency clock included. ACLK = VLO. CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3); f_{ACLK} = f_{VLO} , f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz
- (8) CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 (LPM4); f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 MHz
- (9) f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 32768 Hz, PMMREGOFF = 1, RTC active on AUXVCC3 supply
- (10) f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 0 Hz, PMMREGOFF = 1

Low-Power Mode With LCD Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾⁽²⁾

| PARAMETER | V_{CC} | PMMCOREVx | Temperature (T_A) | | | | | | UNIT |
|---------------------------------|----------|-----------|-----------------------|-----|------|-----|-----------|---------|------|
| | | | -40°C | | 25°C | | 85°C | | |
| | | | TYP | MAX | TYP | MAX | TYP | MAX | |
| I_{LPM3} LCD, ext. bias | 3 V | 0 | 2.5 | | 3.1 | | 9.1 | μA | |
| | | 1 | 2.6 | | 3.3 | | 9.5 | | |
| | | 2 | 2.8 | | 3.5 | | 9.9 | | |
| | | 3 | 2.8 | | 3.5 | 6.0 | 10.0 25.0 | | |
| I_{LPM3} LCD, int. bias | 3 V | 0 | 2.9 | | 3.5 | | 9.7 | μA | |
| | | 1 | 3.1 | | 3.7 | | 10.1 | | |
| | | 2 | 3.2 | | 4.0 | | 10.5 | | |
| | | 3 | 3.3 | | 4.0 | 5.5 | 10.5 25.0 | | |
| I_{LPM3} LCD,CP | 2.2 V | 0 | 2.2 | | 2.8 | | 8.8 | μA | |
| | | 1 | 2.3 | | 3.0 | | 9.1 | | |
| | | 2 | 2.5 | | 3.2 | | 9.5 | | |
| | 3 V | 0 | 2.6 | | 3.2 | | 9.3 | μA | |
| | | 1 | 2.8 | | 3.4 | | 9.7 | | |
| | | 2 | 2.9 | | 3.6 | | 10.1 | | |
| | | 3 | 3.0 | | 3.7 | | 10.2 | | |

- All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.
- The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
- Current for watchdog timer and RTC clocked by ACLK included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVE_x = 0). CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3); f_{ACLK} = 32768 Hz, f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz
Current for brownout, high side supervisor (SVSH) normal mode included. Low side supervisor and monitors disabled (SVSL, SVM_L). High side monitor disabled (SVM_H). RAM retention enabled.
- LCDM_x = 11 (4-mux mode), LCDREXT = 1, LCDEXTBIAS = 1 (external biasing), LCD2B = 0 (1/3 bias), LCDCPEN = 0 (charge pump disabled), LCDSSEL = 0, LCDPRE_x = 101, LCDDIV_x = 00011 (f_{LCD} = 32768 Hz / 32 / 4 = 256 Hz)
Current through external resistors not included (voltage levels are supplied by test equipment).
Even segments S0,S2,... = 0, odd segments S1,S3,... = 1. No LCD panel load.
- LCDM_x = 11 (4-mux mode), LCDREXT = 0, LCDEXTBIAS = 0 (internal biasing), LCD2B = 0 (1/3 bias), LCDCPEN = 0 (charge pump disabled), LCDSSEL = 0, LCDPRE_x = 101, LCDDIV_x = 00011 (f_{LCD} = 32768 Hz / 32 / 4 = 256 Hz)
Even segments S0,S2,... = 0, odd segments S1,S3,... = 1. No LCD panel load.
- LCDM_x = 11 (4-mux mode), LCDREXT = 0, LCDEXTBIAS = 0 (internal biasing), LCD2B = 0 (1/3 bias), LCDCPEN = 1 (charge pump enabled), VLCD_x = 1000 (V_{LCD} = 3V, typ.), LCDSSEL = 0, LCDPRE_x = 101, LCDDIV_x = 00011 (f_{LCD} = 32768 Hz / 32 / 4 = 256 Hz)
Even segments S0,S2,... = 0, odd segments S1,S3,... = 1. No LCD panel load.

Schmitt-Trigger Inputs – General Purpose I/O

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------|---|--|-----------------|------|-----|------|------|
| V _{IT+} | Positive-going input threshold voltage | | 1.8 V | 0.80 | | 1.40 | V |
| | | | 3 V | 1.50 | | 2.10 | |
| V _{IT-} | Negative-going input threshold voltage | | 1.8 V | 0.45 | | 1.00 | V |
| | | | 3 V | 0.75 | | 1.65 | |
| V _{hys} | Input voltage hysteresis (V _{IT+} – V _{IT-}) | | 1.8 V | 0.3 | | 0.85 | V |
| | | | 3 V | 0.4 | | 1.0 | |
| R _{Pull} | Pullup or pulldown resistor ⁽¹⁾ | For pullup: V _{IN} = V _{SS} , For pulldown: V _{IN} = V _{CC} | | 20 | 35 | 50 | kΩ |
| C _I | Input capacitance | V _{IN} = V _{SS} or V _{CC} | | | 5 | | pF |

(1) Also applies to \overline{RST} pin when pullup or pulldown resistor is enabled.

Inputs – Ports P1 and P2⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|--------------------|--|-----------------|-----|-----|------|
| t _(int) | External interrupt timing ⁽²⁾ Port P1, P2: P1.x to P2.x, External trigger pulse duration to set interrupt flag | 2.2 V, 3 V | 20 | | ns |

(1) Some devices may contain additional ports with interrupts. See the block diagram and terminal function descriptions.

(2) An external signal sets the interrupt flag every time the minimum interrupt pulse duration t_(int) is met. It may be set by trigger signals shorter than t_(int).

Leakage Current – General Purpose I/O

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|------------------------|-----------------|-----------------|-----|-----|------|
| I _{lkg(Px.y)} | (1)(2) | 1.8 V, 3 V | -50 | +50 | nA |

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pins, unless otherwise noted.

(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.

Outputs – General Purpose I/O (Full Drive Strength)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|-----------------|---------------------------|--|-----------------|------|------|------|
| V _{OH} | High-level output voltage | I _(OHmax) = -3 mA ⁽¹⁾ | 1.8 V | 1.55 | 1.80 | V |
| | | I _(OHmax) = -10 mA ⁽¹⁾ | | 1.20 | 1.80 | |
| | | I _(OHmax) = -5 mA ⁽¹⁾ | 3 V | 2.75 | 3.00 | |
| | | I _(OHmax) = -15 mA ⁽¹⁾ | | 2.40 | 3.00 | |
| V _{OL} | Low-level output voltage | I _(OLmax) = 3 mA ⁽²⁾ | 1.8 V | 0.00 | 0.25 | V |
| | | I _(OLmax) = 10 mA ⁽³⁾ | | 0.00 | 0.60 | |
| | | I _(OLmax) = 5 mA ⁽²⁾ | 3 V | 0.00 | 0.25 | |
| | | I _(OLmax) = 15 mA ⁽³⁾ | | 0.00 | 0.60 | |

- (1) The maximum total current, I_(OHmax), for all outputs combined should not exceed ±20 mA to hold the maximum voltage drop specified. See [Recommended Operating Conditions](#) for more details.
- (2) The maximum total current, I_(OLmax), for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
- (3) The maximum total current, I_(OLmax), for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.

Outputs – General Purpose I/O (Reduced Drive Strength)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|-----------------|---------------------------|---|-----------------|------|------|------|
| V _{OH} | High-level output voltage | I _(OHmax) = -1 mA ⁽²⁾ | 1.8 V | 1.55 | 1.80 | V |
| | | I _(OHmax) = -3 mA ⁽²⁾ | | 1.20 | 1.80 | |
| | | I _(OHmax) = -2 mA ⁽²⁾ | 3 V | 2.75 | 3.00 | |
| | | I _(OHmax) = -6 mA ⁽²⁾ | | 2.40 | 3.00 | |
| V _{OL} | Low-level output voltage | I _(OLmax) = 1 mA ⁽³⁾ | 1.8 V | 0.00 | 0.25 | V |
| | | I _(OLmax) = 3 mA ⁽⁴⁾ | | 0.00 | 0.60 | |
| | | I _(OLmax) = 2 mA ⁽³⁾ | 3 V | 0.00 | 0.25 | |
| | | I _(OLmax) = 6 mA ⁽⁴⁾ | | 0.00 | 0.60 | |

- (1) Selecting reduced drive strength may reduce EMI.
- (2) The maximum total current, I_(OHmax), for all outputs combined should not exceed ±20 mA to hold the maximum voltage drop specified. See [Recommended Operating Conditions](#) for more details.
- (3) The maximum total current, I_(OLmax), for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.
- (4) The maximum total current, I_(OLmax), for all outputs combined, should not exceed ±100 mA to hold the maximum voltage drop specified.

Output Frequency – General Purpose I/O

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|-----------------------|-----------------------------------|---|-----|-----|------|
| f _{Px,y} | Port output frequency (with load) | ⁽¹⁾⁽²⁾ V _{CC} = 1.8 V, PMMCOREVx = 0 | | 16 | MHz |
| | | V _{CC} = 3 V, PMMCOREVx = 3 | | 25 | |
| f _{Port_CLK} | Clock output frequency | V _{CC} = 1.8 V, PMMCOREVx = 0 | | 16 | MHz |
| | | V _{CC} = 3 V, PMMCOREVx = 3 | | 25 | |

- (1) A resistive divider with 2 × R₁ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider. For full drive strength, R₁ = 550 Ω. For reduced drive strength, R₁ = 1.6 kΩ. C_L = 20 pF is connected to the output to V_{SS}.
- (2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

Typical Characteristics – Outputs, Reduced Drive Strength (PxDS.y = 0)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

**TYPICAL LOW-LEVEL OUTPUT CURRENT
vs
LOW-LEVEL OUTPUT VOLTAGE**

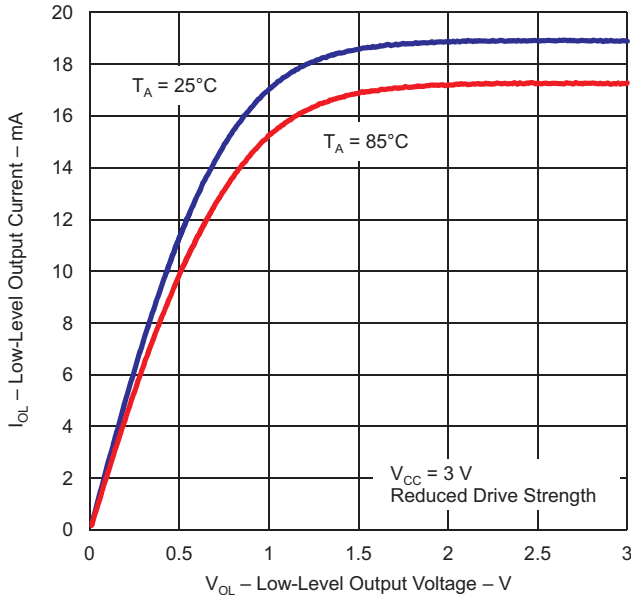


Figure 4.

**TYPICAL LOW-LEVEL OUTPUT CURRENT
vs
LOW-LEVEL OUTPUT VOLTAGE**

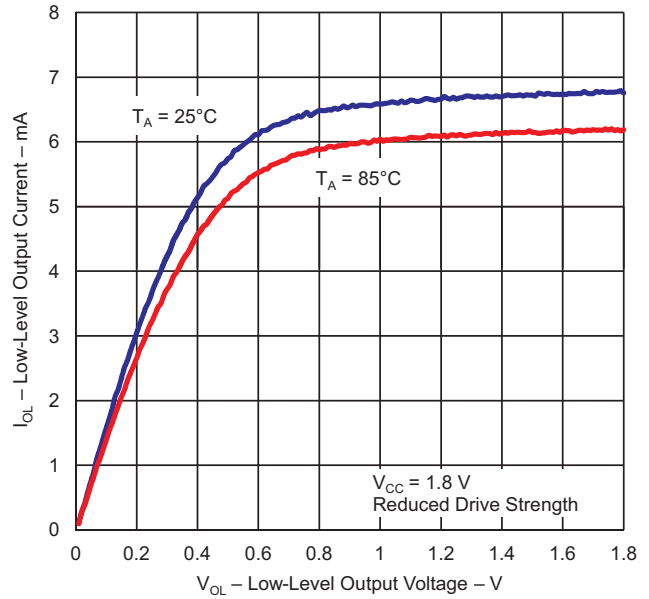


Figure 5.

**TYPICAL HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE**

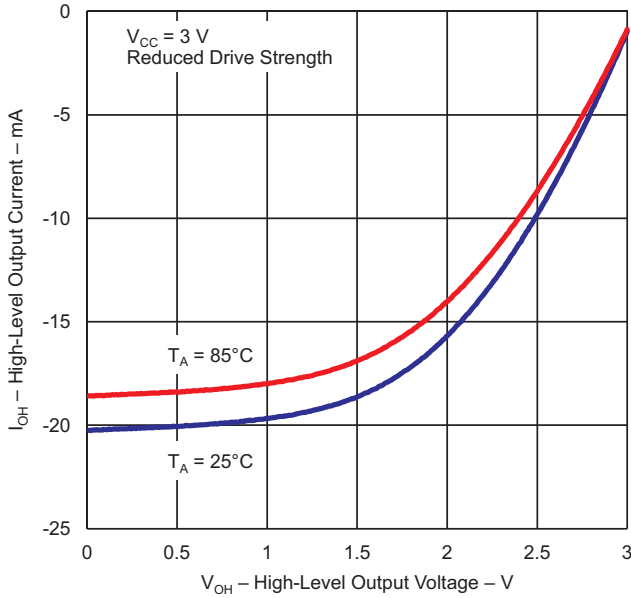


Figure 6.

**TYPICAL HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE**

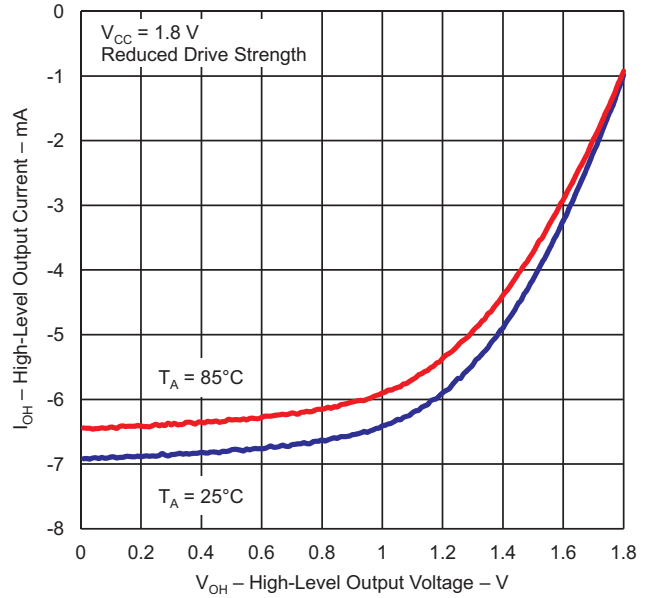


Figure 7.

Typical Characteristics – Outputs, Full Drive Strength (PxDS.y = 1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

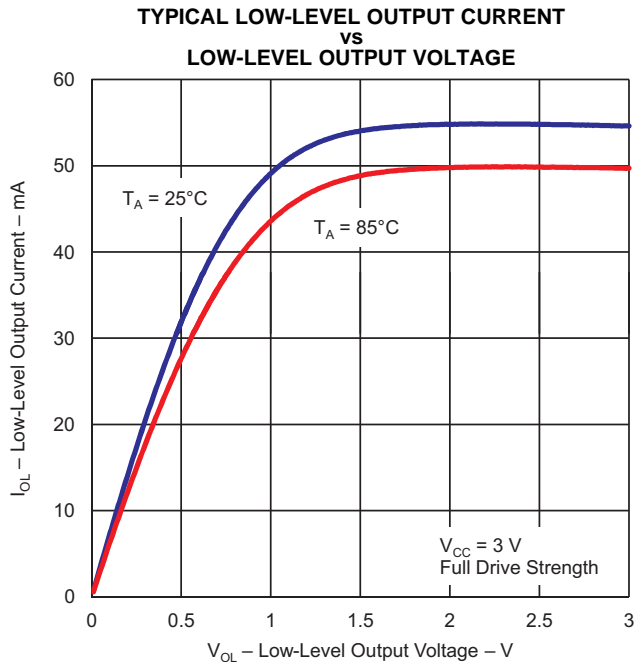


Figure 8.

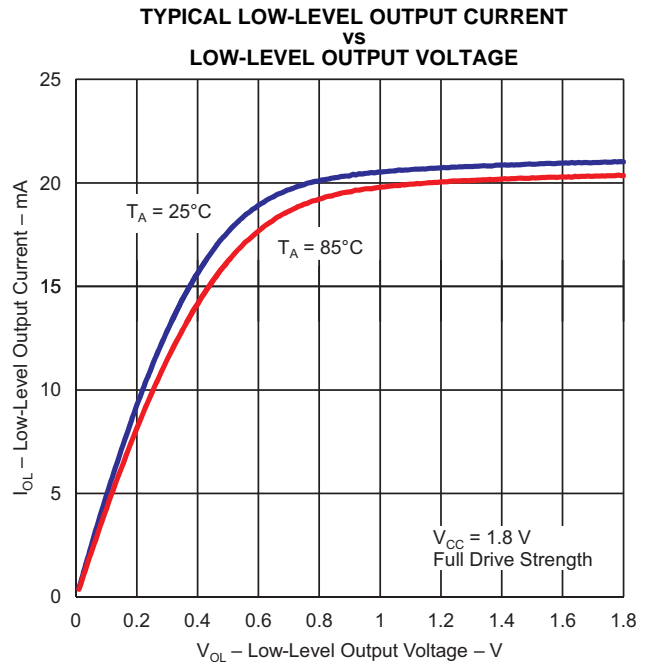


Figure 9.

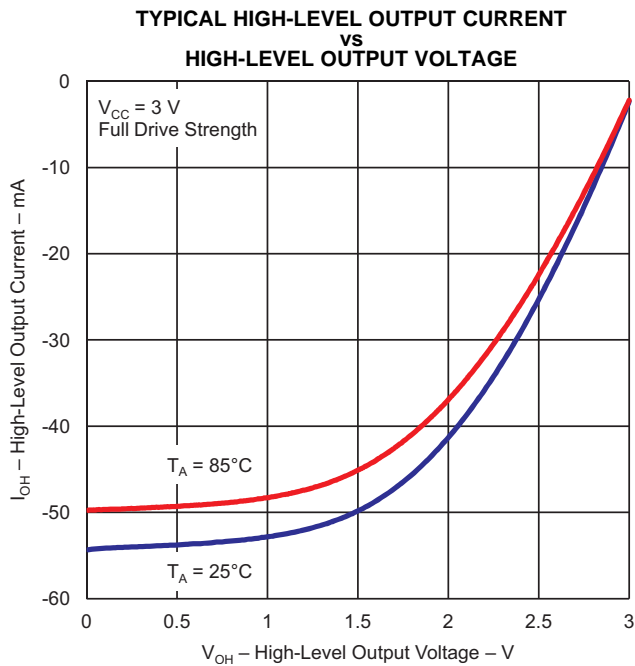


Figure 10.

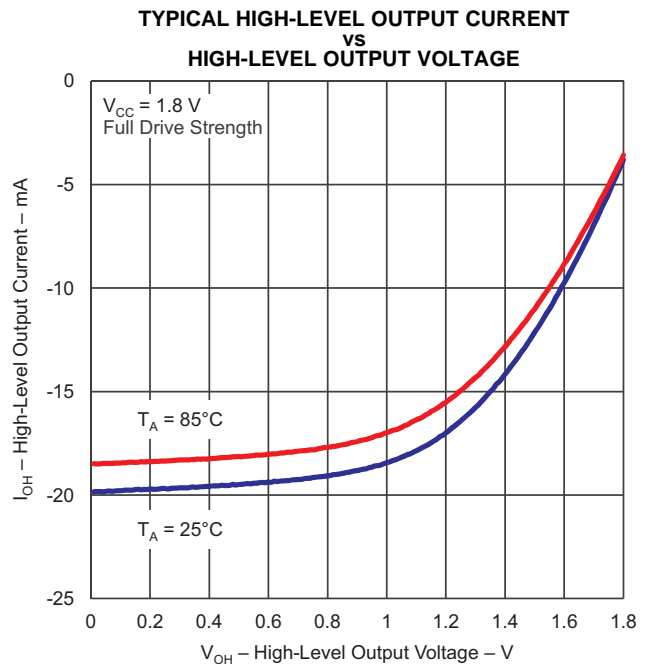


Figure 11.

Crystal Oscillator, XT1, Low-Frequency Mode⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|----------------------|--|-----------------|-----|---|-------|------------|
| $\Delta I_{DVCC,LF}$ | Differential XT1 oscillator crystal current consumption from lowest drive setting, LF mode | 3 V | | 0.075 | | μA |
| | $f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 1, T _A = 25°C | | | | | |
| | $f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 2, T _A = 25°C | | | | | |
| | $f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 3, T _A = 25°C | | | 0.290 | | |
| $f_{XT1,LF0}$ | XT1 oscillator crystal frequency, LF mode | | | 32768 | | Hz |
| $f_{XT1,LF,SW}$ | XT1 oscillator logic-level square-wave input frequency, LF mode | | 10 | 32.768 | 50 | kHz |
| O _{A,LF} | Oscillation allowance for LF crystals ⁽⁴⁾ | | | 210 | | k Ω |
| | | | | $f_{XT1,LF} = 32768$ Hz, C _{L,eff} = 6 pF | | |
| C _{L,eff} | Integrated effective load capacitance, LF mode ⁽⁵⁾ | | | 2 | | pF |
| | | | | XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 0, $f_{XT1,LF} = 32768$ Hz, C _{L,eff} = 6 pF | | |
| | | | | XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 1, $f_{XT1,LF} = 32768$ Hz, C _{L,eff} = 12 pF | | |
| | | | | XTS = 0, XT1BYPASS = 1 ⁽²⁾ ⁽³⁾ | | |
| | | | | 5.5 | | |
| | | | | XTS = 0, XCAP _x = 1 | | |
| | | | | XTS = 0, XCAP _x = 2 | | |
| | | | | XTS = 0, XCAP _x = 3 | | |
| | | | | 12.0 | | |
| | Duty cycle, LF mode | | 30 | | 70 | % |
| $f_{Fault,LF}$ | Oscillator fault frequency, LF mode ⁽⁷⁾ | | 10 | | 10000 | Hz |
| $t_{START,LF}$ | Startup time, LF mode | 3 V | | 1000 | | ms |
| | | | | $f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 0, T _A = 25°C, C _{L,eff} = 6 pF | | |
| | $f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 3, T _A = 25°C, C _{L,eff} = 12 pF | | | 500 | | |

- (1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
 - (a) Keep the trace between the device and the crystal as short as possible.
 - (b) Design a good ground plane around the oscillator pins.
 - (c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
 - (d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
 - (e) Use assembly materials and techniques to avoid any parasitic load on the oscillator XIN and XOUT pins.
 - (f) If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.
- (2) When XT1BYPASS is set, XT1 circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet.
- (3) Maximum frequency of operation of the entire device cannot be exceeded.
- (4) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the XT1DRIVE_x settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
 - (a) For XT1DRIVE_x = 0, C_{L,eff} ≤ 6 pF.
 - (b) For XT1DRIVE_x = 1, 6 pF ≤ C_{L,eff} ≤ 9 pF.
 - (c) For XT1DRIVE_x = 2, 6 pF ≤ C_{L,eff} ≤ 10 pF.
 - (d) For XT1DRIVE_x = 3, C_{L,eff} ≥ 6 pF.
- (5) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Since the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
- (6) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
- (7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
- (8) Measured with logic-level input frequency but also applies to operation with crystals.

Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------------------------|------------------------------------|------------------|-----------------|-----|-----|-----|------|
| f _{VLO} | VLO frequency | Measured at ACLK | 1.8 V to 3.6 V | 6 | 9.6 | 15 | kHz |
| df _{VLO} /dT | VLO frequency temperature drift | Measured at ACLK | 1.8 V to 3.6 V | | 0.5 | | %/°C |
| df _{VLO} /dV _{CC} | VLO frequency supply voltage drift | Measured at ACLK | 1.8 V to 3.6 V | | 4 | | %/V |
| | Duty cycle | Measured at ACLK | 1.8 V to 3.6 V | 40 | 50 | 60 | % |

Internal Reference, Low-Frequency Oscillator (REFO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--------------------------------------|-------------------------------------|------------------------|-----------------|------|-------|------|------|
| I _{REFO} | REFO oscillator current consumption | T _A = 25°C | 1.8 V to 3.6 V | | 3 | | μA |
| f _{REFO} | REFO frequency calibrated | Measured at ACLK | 1.8 V to 3.6 V | | 32768 | | Hz |
| | REFO absolute tolerance calibrated | Full temperature range | 1.8 V to 3.6 V | -3.5 | | +3.5 | % |
| | | T _A = 25°C | 3 V | -1.5 | | +1.5 | % |
| df _{REFO} /dT | REFO frequency temperature drift | Measured at ACLK | 1.8 V to 3.6 V | | 0.01 | | %/°C |
| df _{REFO} /dV _{CC} | REFO frequency supply voltage drift | Measured at ACLK | 1.8 V to 3.6 V | | 1.0 | | %/V |
| | Duty cycle | Measured at ACLK | 1.8 V to 3.6 V | 40 | 50 | 60 | % |
| t _{START} | REFO startup time | 40%/60% duty cycle | 1.8 V to 3.6 V | | 25 | | μs |

DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|--|--|------|-----|------|-------|
| f _{DCO(0,0)} | DCO frequency (0, 0) ⁽¹⁾ | DCORSELx = 0, DCOx = 0, MODx = 0 | 0.07 | | 0.20 | MHz |
| f _{DCO(0,31)} | DCO frequency (0, 31) ⁽¹⁾ | DCORSELx = 0, DCOx = 31, MODx = 0 | 0.70 | | 1.70 | MHz |
| f _{DCO(1,0)} | DCO frequency (1, 0) ⁽¹⁾ | DCORSELx = 1, DCOx = 0, MODx = 0 | 0.15 | | 0.36 | MHz |
| f _{DCO(1,31)} | DCO frequency (1, 31) ⁽¹⁾ | DCORSELx = 1, DCOx = 31, MODx = 0 | 1.47 | | 3.45 | MHz |
| f _{DCO(2,0)} | DCO frequency (2, 0) ⁽¹⁾ | DCORSELx = 2, DCOx = 0, MODx = 0 | 0.32 | | 0.75 | MHz |
| f _{DCO(2,31)} | DCO frequency (2, 31) ⁽¹⁾ | DCORSELx = 2, DCOx = 31, MODx = 0 | 3.17 | | 7.38 | MHz |
| f _{DCO(3,0)} | DCO frequency (3, 0) ⁽¹⁾ | DCORSELx = 3, DCOx = 0, MODx = 0 | 0.64 | | 1.51 | MHz |
| f _{DCO(3,31)} | DCO frequency (3, 31) ⁽¹⁾ | DCORSELx = 3, DCOx = 31, MODx = 0 | 6.07 | | 14.0 | MHz |
| f _{DCO(4,0)} | DCO frequency (4, 0) ⁽¹⁾ | DCORSELx = 4, DCOx = 0, MODx = 0 | 1.3 | | 3.2 | MHz |
| f _{DCO(4,31)} | DCO frequency (4, 31) ⁽¹⁾ | DCORSELx = 4, DCOx = 31, MODx = 0 | 12.3 | | 28.2 | MHz |
| f _{DCO(5,0)} | DCO frequency (5, 0) ⁽¹⁾ | DCORSELx = 5, DCOx = 0, MODx = 0 | 2.5 | | 6.0 | MHz |
| f _{DCO(5,31)} | DCO frequency (5, 31) ⁽¹⁾ | DCORSELx = 5, DCOx = 31, MODx = 0 | 23.7 | | 54.1 | MHz |
| f _{DCO(6,0)} | DCO frequency (6, 0) ⁽¹⁾ | DCORSELx = 6, DCOx = 0, MODx = 0 | 4.6 | | 10.7 | MHz |
| f _{DCO(6,31)} | DCO frequency (6, 31) ⁽¹⁾ | DCORSELx = 6, DCOx = 31, MODx = 0 | 39.0 | | 88.0 | MHz |
| f _{DCO(7,0)} | DCO frequency (7, 0) ⁽¹⁾ | DCORSELx = 7, DCOx = 0, MODx = 0 | 8.5 | | 19.6 | MHz |
| f _{DCO(7,31)} | DCO frequency (7, 31) ⁽¹⁾ | DCORSELx = 7, DCOx = 31, MODx = 0 | 60 | | 135 | MHz |
| S _{DCORSEL} | Frequency step between range DCORSEL and DCORSEL + 1 | S _{RSEL} = f _{DCO(DCORSEL+1,DCO)} /f _{DCO(DCORSEL,DCO)} | 1.2 | | 2.3 | ratio |
| S _{DCO} | Frequency step between tap DCO and DCO + 1 | S _{DCO} = f _{DCO(DCORSEL,DCO+1)} /f _{DCO(DCORSEL,DCO)} | 1.02 | | 1.12 | ratio |
| | Duty cycle | Measured at SMCLK | 40 | 50 | 60 | % |
| df _{DCO} /dT | DCO frequency temperature drift | f _{DCO} = 1 MHz | | 0.1 | | %/°C |

(1) When selecting the proper DCO frequency range (DCORSELx), the target DCO frequency, f_{DCO}, should be set to reside within the range of f_{DCO(n,0),MAX} ≤ f_{DCO} ≤ f_{DCO(n,31),MIN}, where f_{DCO(n,0),MAX} represents the maximum frequency specified for the DCO frequency, range n, tap 0 (DCOx = 0) and f_{DCO(n,31),MIN} represents the minimum frequency specified for the DCO frequency, range n, tap 31 (DCOx = 31). This ensures that the target DCO frequency resides within the range selected. It should also be noted that if the actual f_{DCO} frequency for the selected range causes the FLL or the application to select tap 0 or 31, the DCO fault flag is set to report that the selected range is at its minimum or maximum tap setting.

DCO Frequency (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------|--|-----|-----|-----|------|
| df_{DCO}/dV_{CORE} | DCO frequency voltage drift $f_{DCO} = 1$ MHz | | 1.9 | | %/V |

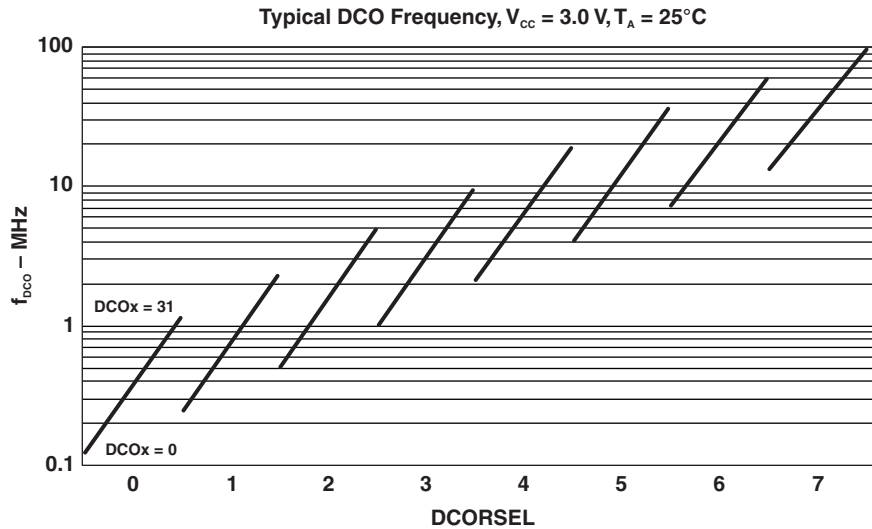


Figure 12. Typical DCO Frequency

PMM, Brown-Out Reset (BOR)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|---|------|------|------|---------|
| $V_{(DVCC_BOR_IT-)}$ | BOR _H on voltage, DV _{CC} falling level $ dV_{CC}/dt < 3$ V/s | | | 1.45 | V |
| $V_{(DVCC_BOR_IT+)}$ | BOR _H off voltage, DV _{CC} rising level $ dV_{CC}/dt < 3$ V/s | 0.80 | 1.20 | 1.50 | V |
| $V_{(DVCC_BOR_hys)}$ | BOR _H hysteresis | 50 | | 250 | mV |
| t_{RESET} | Pulse duration required at $\overline{RST}/\overline{NMI}$ pin to accept a reset | 2 | | | μ s |

PMM, Core Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|--|-----|------|-----|------|
| $V_{CORE3(AM)}$ | Core voltage, active mode, PMMCOREV = 3 2.4 V \leq DV _{CC} \leq 3.6 V | | 1.91 | | V |
| $V_{CORE2(AM)}$ | Core voltage, active mode, PMMCOREV = 2 2.2 V \leq DV _{CC} \leq 3.6 V | | 1.81 | | V |
| $V_{CORE1(AM)}$ | Core voltage, active mode, PMMCOREV = 1 2 V \leq DV _{CC} \leq 3.6 V | | 1.61 | | V |
| $V_{CORE0(AM)}$ | Core voltage, active mode, PMMCOREV = 0 1.8 V \leq DV _{CC} \leq 3.6 V | | 1.41 | | V |
| $V_{CORE3(LPM)}$ | Core voltage, low-current mode, PMMCOREV = 3 2.4 V \leq DV _{CC} \leq 3.6 V | | 1.94 | | V |
| $V_{CORE2(LPM)}$ | Core voltage, low-current mode, PMMCOREV = 2 2.2 V \leq DV _{CC} \leq 3.6 V | | 1.92 | | V |
| $V_{CORE1(LPM)}$ | Core voltage, low-current mode, PMMCOREV = 1 2 V \leq DV _{CC} \leq 3.6 V | | 1.73 | | V |
| $V_{CORE0(LPM)}$ | Core voltage, low-current mode, PMMCOREV = 0 1.8 V \leq DV _{CC} \leq 3.6 V | | 1.52 | | V |

PMM, SVS High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------|---------------------------------------|---|------|------|------|---------------|
| $I_{(SVSH)}$ | SVS current consumption | SVSHE = 0, $DV_{CC} = 3.6\text{ V}$ | 0 | | | nA |
| | | SVSHE = 1, $DV_{CC} = 3.6\text{ V}$, SVSHFP = 0 | 200 | | | nA |
| | | SVSHE = 1, $DV_{CC} = 3.6\text{ V}$, SVSHFP = 1 | 1.5 | | | μA |
| $V_{(SVSH_IT-)}$ | SVS _H on voltage level | SVSHE = 1, SVSHRVL = 0 | 1.60 | 1.65 | 1.75 | V |
| | | SVSHE = 1, SVSHRVL = 1 | 1.77 | 1.84 | 1.95 | |
| | | SVSHE = 1, SVSHRVL = 2 | 1.93 | 2.00 | 2.12 | |
| | | SVSHE = 1, SVSHRVL = 3 | 2.09 | 2.16 | 2.29 | |
| $V_{(SVSH_IT+)}$ | SVS _H off voltage level | SVSHE = 1, SVSMHRRL = 0 | 1.65 | 1.75 | 1.85 | V |
| | | SVSHE = 1, SVSMHRRL = 1 | 1.85 | 1.95 | 2.05 | |
| | | SVSHE = 1, SVSMHRRL = 2 | 2.05 | 2.15 | 2.25 | |
| | | SVSHE = 1, SVSMHRRL = 3 | 2.15 | 2.25 | 2.35 | |
| | | SVSHE = 1, SVSMHRRL = 4 | 2.30 | 2.40 | 2.55 | |
| | | SVSHE = 1, SVSMHRRL = 5 | 2.57 | 2.70 | 2.83 | |
| | | SVSHE = 1, SVSMHRRL = 6 | 2.90 | 3.05 | 3.20 | |
| | | SVSHE = 1, SVSMHRRL = 7 | 2.90 | 3.05 | 3.20 | |
| $t_{pd(SVSH)}$ | SVS _H propagation delay | SVSHE = 1, $dV_{DVCC}/dt = 10\text{ mV}/\mu\text{s}$, SVSHFP = 1 | 2.5 | | | μs |
| | | SVSHE = 1, $dV_{DVCC}/dt = 1\text{ mV}/\mu\text{s}$, SVSHFP = 0 | 20 | | | |
| $t_{(SVSH)}$ | SVS _H on or off delay time | SVSHE = 0 → 1, $dV_{DVCC}/dt = 10\text{ mV}/\mu\text{s}$, SVSHFP = 1 | 12.5 | | | μs |
| | | SVSHE = 0 → 1, $dV_{DVCC}/dt = 1\text{ mV}/\mu\text{s}$, SVSHFP = 0 | 100 | | | |
| dV_{DVCC}/dt | DVCC rise time | | 0 | | 1000 | V/s |

PMM, SVM High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------|---|--|------|------|------|------|
| $I_{(SVMH)}$ | SVM _H current consumption | SVMHE = 0, DV _{CC} = 3.6 V | | 0 | | nA |
| | | SVMHE = 1, DV _{CC} = 3.6 V, SVMHFP = 0 | | 200 | | nA |
| | | SVMHE = 1, DV _{CC} = 3.6 V, SVMHFP = 1 | | 1.5 | | μA |
| $V_{(SVMH)}$ | SVM _H on or off voltage level ⁽¹⁾ | SVMHE = 1, SVSMHRRRL = 0 | 1.63 | 1.73 | 1.83 | V |
| | | SVMHE = 1, SVSMHRRRL = 1 | 1.83 | 1.93 | 2.03 | |
| | | SVMHE = 1, SVSMHRRRL = 2 | 2.03 | 2.13 | 2.23 | |
| | | SVMHE = 1, SVSMHRRRL = 3 | 2.13 | 2.23 | 2.33 | |
| | | SVMHE = 1, SVSMHRRRL = 4 | 2.28 | 2.40 | 2.53 | |
| | | SVMHE = 1, SVSMHRRRL = 5 | 2.55 | 2.70 | 2.81 | |
| | | SVMHE = 1, SVSMHRRRL = 6 | 2.88 | 3.02 | 3.18 | |
| | | SVMHE = 1, SVSMHRRRL = 7 | 2.88 | 3.02 | 3.18 | |
| $t_{pd(SVMH)}$ | SVM _H propagation delay | SVMHE = 1, dV _{DVCC} /dt = 10 mV/μs, SVMHFP = 1 | | 2.5 | | μs |
| | | SVMHE = 1, dV _{DVCC} /dt = 1 mV/μs, SVMHFP = 0 | | 20 | | |
| $t_{(SVMH)}$ | SVM _H on or off delay time | SVMHE = 0 → 1, dV _{DVCC} /dt = 10 mV/μs, SVMHFP = 1 | | 12.5 | | μs |
| | | SVMHE = 0 → 1, dV _{DVCC} /dt = 1 mV/μs, SVMHFP = 0 | | 100 | | |

(1) The SVM_H settings available depend on the V_{CORE} (PMMCOREV_x) setting. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx and MSP430x6xx Family User's Guide (SLAU208)* on recommended settings and use.

PMM, SVS Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------|---------------------------------------|--|-----|------|-----|------|
| $I_{(SVSL)}$ | SVS _L current consumption | SVSLE = 0, PMMCOREV = 2 | | 0 | | nA |
| | | SVSLE = 1, PMMCOREV = 2, SVSLFP = 0 | | 200 | | nA |
| | | SVSLE = 1, PMMCOREV = 2, SVSLFP = 1 | | 1.5 | | μA |
| $t_{pd(SVSL)}$ | SVS _L propagation delay | SVSLE = 1, dV _{CORE} /dt = 10 mV/μs, SVSLFP = 1 | | 2.5 | | μs |
| | | SVSLE = 1, dV _{CORE} /dt = 1 mV/μs, SVSLFP = 0 | | 20 | | |
| $t_{(SVSL)}$ | SVS _L on or off delay time | SVSLE = 0 → 1, dV _{CORE} /dt = 10 mV/μs, SVSLFP = 1 | | 12.5 | | μs |
| | | SVSLE = 0 → 1, dV _{CORE} /dt = 1 mV/μs, SVSLFP = 0 | | 100 | | |

PMM, SVM Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|---------------------------------------|---|-----|------|-----|------|
| $I_{(SVM_L)}$ | SVM _L current consumption | SVMLE = 0, PMMCOREV = 2 | | 0 | | nA |
| | | SVMLE = 1, PMMCOREV = 2, SVM_LFP = 0 | | 200 | | nA |
| | | SVMLE = 1, PMMCOREV = 2, SVM_LFP = 1 | | 1.5 | | μA |
| $t_{pd(SVM_L)}$ | SVM _L propagation delay | SVMLE = 1, dV _{CORE} /dt = 10 mV/μs, SVM_LFP = 1 | | 2.5 | | μs |
| | | SVMLE = 1, dV _{CORE} /dt = 1 mV/μs, SVM_LFP = 0 | | 20 | | |
| $t_{(SVM_L)}$ | SVM _L on or off delay time | SVMLE = 0 → 1, dV _{CORE} /dt = 10 mV/μs, SVM_LFP = 1 | | 12.5 | | μs |
| | | SVMLE = 0 → 1, dV _{CORE} /dt = 1 mV/μs, SVM_LFP = 0 | | 100 | | |

Wake-Up From Low-Power Modes and Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------|---|---|-------------------------|-----|-----|------|
| $t_{WAKE-UP-FAST}$ | Wake-up time from LPM2, LPM3, or LPM4 to active mode ⁽¹⁾ | PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 1 | $f_{MCLK} \geq 4.0$ MHz | | 5 | μs |
| | | | $f_{MCLK} < 4.0$ MHz | | 10 | |
| $t_{WAKE-UP-SLOW}$ | Wake-up time from LPM2, LPM3 or LPM4 to active mode ⁽²⁾ | PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 0 | | 150 | 165 | μs |
| $t_{WAKE-UP-LPM4.5}$ | Wake-up time from LPM4.5 to active mode ⁽³⁾ | | | 2 | 3 | ms |
| $t_{WAKE-UP-RESET}$ | Wake-up time from \overline{RST} or BOR event to active mode ⁽³⁾ | | | 2 | 3 | ms |

- (1) This value represents the time from the wakeup event to the first active edge of MCLK. The wakeup time depends on the performance mode of the low side supervisor (SVS_L) and low side monitor (SVM_L). Fastest wakeup times are possible with SVS_L and SVM_L in full performance mode or disabled when operating in AM, LPM0, and LPM1. Various options are available for SVS_L and SVM_L while operating in LPM2, LPM3, and LPM4. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx and MSP430x6xx Family User's Guide (SLAU208)*.
- (2) This value represents the time from the wakeup event to the first active edge of MCLK. The wakeup time depends on the performance mode of the low side supervisor (SVS_L) and low side monitor (SVM_L). In this case, the SVS_L and SVM_L are in normal mode (low current) mode when operating in AM, LPM0, and LPM1. Various options are available for SVS_L and SVM_L while operating in LPM2, LPM3, and LPM4. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx and MSP430x6xx Family User's Guide (SLAU208)*.
- (3) This value represents the time from the wakeup event to the reset vector execution.

Auxiliary Supplies Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|-----------------------|--|---------------|------|-----|------|
| V_{CC} | Supply voltage range for all supplies at pins DVCC, AVCC, AUX1, AUX2, AUX3 | 1.8 | | 3.6 | V |
| V_{DSYS} | Digital system supply voltage range, $V_{DSYS} = V_{CC} - R_{ON} \times I_{LOAD}$ | PMMCOREVx = 0 | | 3.6 | V |
| | | PMMCOREVx = 1 | 2.0 | 3.6 | |
| | | PMMCOREVx = 2 | 2.2 | 3.6 | |
| | | PMMCOREVx = 3 | 2.4 | 3.6 | |
| V_{ASYS} | Analog system supply voltage range, $V_{ASYS} = V_{CC} - R_{ON} \times I_{LOAD}$ | See modules | | | V |
| T_A | Ambient temperature range | -40 | | 85 | °C |
| $T_{A,HTOL}$ | Ambient temperature during HTOL (module should be functional during HTOL) | | | 150 | °C |
| $C_{VCC}, C_{AUX1/2}$ | Recommended capacitor at pins DVCC, AVCC, AUX1, AUX2 | | 4.7 | | µF |
| C_{VSYs} | Recommended capacitor at pins VDSYS1, VDSYS2 and VASYS1, VASYS2 | | 4.7 | | µF |
| $C_{V CORE}$ | Recommended capacitance at pin V CORE | | 0.47 | | µF |
| C_{AUX3} | Recommended capacitor at pin AUX3 | | 0.47 | | µF |

Auxiliary Supplies - AUX3 (Backup Subsystem) Currents

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V_{CC} | T_A | MIN | TYP | MAX | UNIT |
|-------------------|--------------------------------|----------|-------|-----|-----|------|------|
| $I_{AUX3,RTCOn}$ | AUX3 current with RTC enabled | 3 V | 25°C | | | 0.86 | µA |
| | | | 85°C | | | 1.2 | |
| $I_{AUX3,RTCOff}$ | AUX3 current with RTC disabled | 3 V | 25°C | | | 120 | nA |
| | | | 85°C | | | 220 | |

Auxiliary Supplies - Auxiliary Supply Monitor

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------|--|-------------------------------------|-------------------------------------|-------------------------------------|------|
| $I_{CC,Monitor}$ | Average supply current for monitoring circuitry drawn from VDSYS LOCKAUX = 0, AUXMRx = 0 AUX0MD = 0, AUX1MD = 0, AUX2MD = 1, VDSYS = DVCC, VASYS = AVCC, Current measured at VDSYS | | | 1.10 | µA |
| $I_{Meas,Monitor}$ | Average current drawn from monitored supply during measurement cycle LOCKAUX = 0, AUXMRx = 0 AUX0MD = 0, AUX1MD = 0, AUX2MD = 1, VDSYS = DVCC, VASYS = AVCC, Current measured at AUXVCC1 | | | 0.13 | µA |
| $V_{Monitor}$ | General | V_{SVMH} (SVSMHRRLx = AUXLVLx) | V_{SVMH} (SVSMHRRLx = AUXLVLx) | V_{SVMH} (SVSMHRRLx = AUXLVLx) | V |
| | | X - 5% | | X + 5% | |
| | AUXLVLx = 0 | 1.65 | 1.75 | 1.85 | |
| | AUXLVLx = 1 | 1.85 | 1.95 | 2.05 | |
| | AUXLVLx = 2 | 2.05 | 2.15 | 2.25 | |
| | AUXLVLx = 3 | 2.15 | 2.25 | 2.35 | |
| | AUXLVLx = 4 | 2.30 | 2.40 | 2.55 | |
| | AUXLVLx = 5 | 2.57 | 2.70 | 2.83 | |
| AUXLVLx = 6 | 2.90 | 3.00 | 3.20 | | |
| AUXLVLx = 7 | 2.90 | 3.00 | 3.20 | | |

Auxiliary Supplies - Switch On-Resistance

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|--|---|-----------------|-----|-----|-----|------|
| R _{ON,DVCC} | On-resistance of switch between DVCC and VDSYS | I _{LOAD} = I _{CORE} + I _{IO} = 10 mA + 10 mA = 20 mA | | | | 5 | Ω |
| R _{ON,DAUX1} | On-resistance of switch between AUX1 and VDSYS | I _{LOAD} = I _{CORE} + I _{IO} = 10 mA + 10 mA = 20 mA | | | | 5 | Ω |
| R _{ON,DAUX2} | On-resistance of switch between AUX2 and VDSYS | I _{LOAD} = I _{CORE} + I _{IO} = 10 mA + 10 mA = 20 mA | | | | 5 | Ω |
| R _{ON,AVCC} | On-resistance of switch between AVCC and V _{ASYS} | I _{LOAD} = I _{Modules} = 10 mA | | | | 5 | Ω |
| R _{ON,AAUX1} | On-resistance of switch between AUX1 and V _{ASYS} | I _{LOAD} = I _{Modules} = 5 mA | | | | 20 | Ω |
| R _{ON,AAUX2} | On-resistance of switch between AUX2 and V _{ASYS} | I _{LOAD} = I _{Modules} = 5 mA | | | | 20 | Ω |

Auxiliary Supplies - Switching Time

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|----------------------|--|-----------------|-----------------|-----|-----|-----|------|
| t _{Switch} | Time from occurrence of trigger (SVM or software) to "new" supply connected to system supplies | | | | | 100 | ns |
| t _{Recover} | "Recovery time" after a switch over took place. During that time no further switching takes place. | | | 170 | | 480 | μs |

Auxiliary Supplies - Switch Leakage

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------|--|---|-----------------|-----|-----|-----|------|
| I _{SW,Lkg} | Current into DVCC, AVCC, AUX1, or AUX2 if not selected | Per supply (but not the highest supply) | | | 75 | 250 | nA |
| I _{Vmax} | Current drawn from highest supply | | | 500 | 700 | | nA |

Auxiliary Supplies - Auxiliary Supplies to ADC10_A

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|------------------------|---|------------------------------------|-----------------|------|-----|------|------|
| V ₃ | Supply voltage divider V ₃ = V _{Supply} /3 | | 1.8 V | 0.57 | 0.6 | 0.63 | V |
| | | | 3 V | 0.95 | 1.0 | 1.05 | |
| | | | 3.6 V | 1.14 | 1.2 | 1.26 | |
| R _{V3} | Load resistance | AUXADCR _x = 0 | | | | 15 | kΩ |
| | | AUXADCR _x = 1 | | | | 1.5 | kΩ |
| | | AUXADCR _x = 2 | | | | 0.6 | kΩ |
| t _{Sample,V3} | Sampling time required if V ₃ selected. | Error of conversion result ≤ 1 LSB | | 1000 | | | ns |
| | | | | 1000 | | | ns |
| | | | | 1000 | | | ns |

Auxiliary Supplies - Charge Limiting Resistor

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------|--------------------------|----------------------|-----------------|-----|-----|-----|------|
| R _{CHARGE} | Charge limiting resistor | CHC _x = 1 | 3 V | | | 5 | kΩ |
| | | CHC _x = 2 | 3 V | | | 10 | |
| | | CHC _x = 3 | 3 V | | | 20 | |

Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------|-------------------------------|--|-----------------|-----|-----|-----|------|
| f _{TA} | Timer_A input clock frequency | Internal: SMCLK or ACLK, External: TACLK, Duty cycle = 50% ± 10% | 1.8 V, 3 V | | | 25 | MHz |
| t _{TA,cap} | Timer_A capture timing | All capture inputs. Minimum pulse duration required for capture. | 1.8 V, 3 V | 20 | | | ns |

eUSCI (UART Mode) Recommended Operating Conditions

| PARAMETER | | CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------|---|---|-----------------|-----|---------------------|-----|------|
| f _{eUSCI} | eUSCI input clock frequency | Internal: SMCLK or ACLK, External: UCLK, Duty cycle = 50% ± 10% | | | f _{SYSTEM} | | MHz |
| f _{BITCLK} | BITCLK clock frequency (equals baud rate in Mbaud) | | | | | 5 | MHz |

eUSCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|----------------|---|-----------------|-----------------|-----|-----|-----|------|
| t _t | UART receive deglitch time ⁽¹⁾ | UCGLITx = 0 | 2 V, 3 V | 10 | 15 | 25 | ns |
| | | UCGLITx = 1 | | 30 | 50 | 85 | |
| | | UCGLITx = 2 | | 50 | 80 | 150 | |
| | | UCGLITx = 3 | | 70 | 120 | 200 | |

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To make sure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

eUSCI (SPI Master Mode) Recommended Operating Conditions

| PARAMETER | | CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--------------------|-----------------------------|--|-----------------|-----|---------------------|-----|------|
| f _{eUSCI} | eUSCI input clock frequency | Internal: SMCLK or ACLK, Duty cycle = 50% ± 10% | | | f _{SYSTEM} | | MHz |

eUSCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|---|--------------------------------|-----------------|-----|-----|-----|------|
| t _{STE,LEAD} | STE lead time, STE low to clock | UCSTEM = 0, UCMODEx = 01 or 10 | 2 V, 3 V | 150 | | | ns |
| | | UCSTEM = 1, UCMODEx = 01 or 10 | 2 V, 3 V | 150 | | | |
| t _{STE,LAG} | STE lag time, Last clock to STE high | UCSTEM = 0, UCMODEx = 01 or 10 | 2 V, 3 V | 200 | | | ns |
| | | UCSTEM = 1, UCMODEx = 01 or 10 | 2 V, 3 V | 200 | | | |
| t _{STE,ACC} | STE access time, STE low to SIMO data out | UCSTEM = 0, UCMODEx = 01 or 10 | 2 V | | | 50 | ns |
| | | | 3V | | | 30 | |
| | | UCSTEM = 1, UCMODEx = 01 or 10 | 2 V | | | 50 | |
| | | | 3 V | | | 30 | |
| t _{STE,DIS} | STE disable time, STE high to SIMO high impedance | UCSTEM = 0, UCMODEx = 01 or 10 | 2 V | | | 40 | ns |
| | | | 3V | | | 25 | |
| | | UCSTEM = 1, UCMODEx = 01 or 10 | 2 V | | | 40 | |
| | | | 3 V | | | 25 | |
| t _{SU,MI} | SOMI input data setup time | | 2 V | 50 | | | ns |
| | | | 3 V | 30 | | | |

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} = \max(t_{VALID,MO(eUSCI)} + t_{SU,SI(Slave)}, t_{SU,MI(eUSCI)} + t_{VALID,SO(Slave)})$.
For the slave's parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$ see the SPI parameters of the attached slave.

eUSCI (SPI Master Mode) (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--|--|-----------------|-----|-----|-----|------|
| t _{HD,MI} SOMI input data hold time | | 2 V | 0 | | | ns |
| | | 3 V | 0 | | | |
| t _{VALID,MO} SIMO output data valid time ⁽²⁾ | UCLK edge to SIMO valid, C _L = 20 pF | 2 V | | | 9 | ns |
| | | 3 V | | | 5 | |
| t _{HD,MO} SIMO output data hold time ⁽³⁾ | C _L = 20 pF | 2 V | 0 | | | ns |
| | | 3 V | 0 | | | |

- (2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in [Figure 13](#) and [Figure 14](#).
- (3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in [Figure 13](#) and [Figure 14](#).

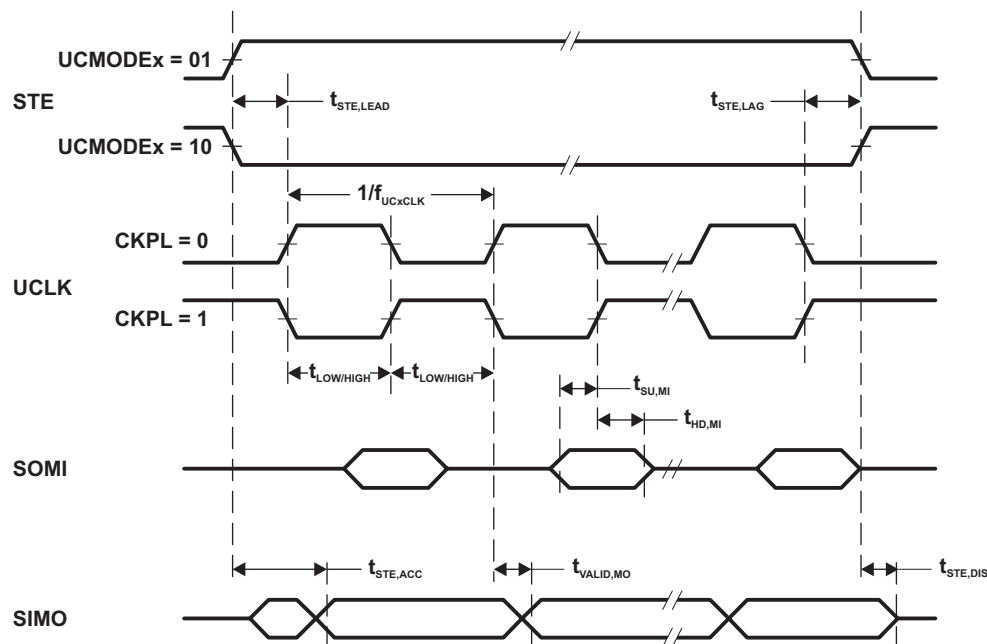


Figure 13. SPI Master Mode, CKPH = 0

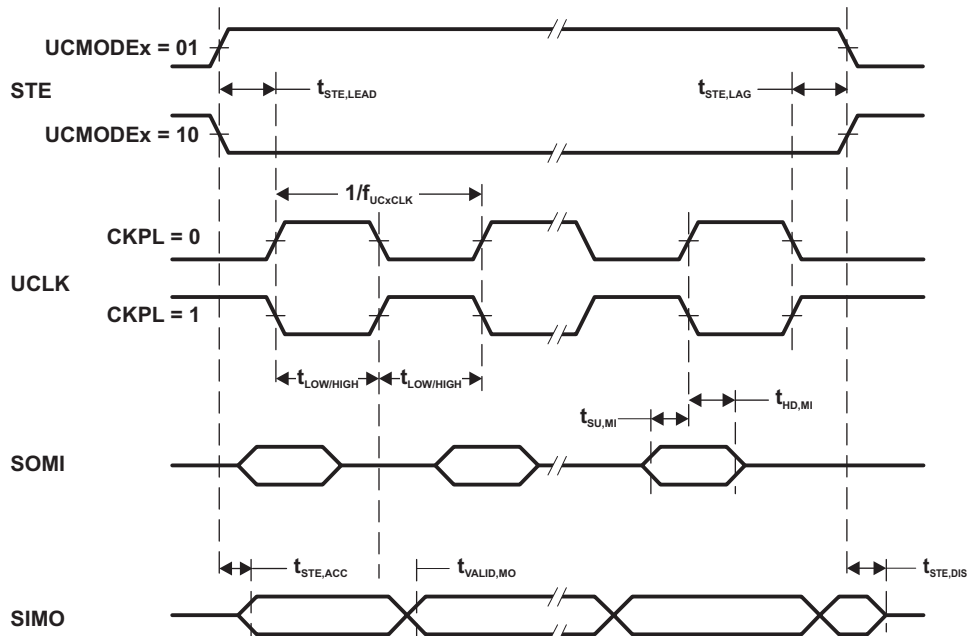


Figure 14. SPI Master Mode, CKPH = 1

eUSCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|---|--|-----------------|-----|-----|-----|------|
| t _{STE,LEAD} | STE lead time, STE low to clock | | 2 V | 4 | | | ns |
| | | | 3 V | 3 | | | |
| t _{STE,LAG} | STE lag time, Last clock to STE high | | 2 V | 0 | | | ns |
| | | | 3 V | 0 | | | |
| t _{STE,ACC} | STE access time, STE low to SOMI data out | | 2 V | | | 46 | ns |
| | | | 3 V | | | 24 | |
| t _{STE,DIS} | STE disable time, STE high to SOMI high impedance | | 2 V | | | 38 | ns |
| | | | 3 V | | | 25 | |
| t _{SU,SI} | SIMO input data setup time | | 2 V | 2 | | | ns |
| | | | 3 V | 1 | | | |
| t _{HD,SI} | SIMO input data hold time | | 2 V | 2 | | | ns |
| | | | 3 V | 2 | | | |
| t _{VALID,SO} | SOMI output data valid time ⁽²⁾ | UCLK edge to SOMI valid, C _L = 20 pF | 2 V | | | 55 | ns |
| | | | 3 V | | | 32 | |
| t _{HD,SO} | SOMI output data hold time ⁽³⁾ | C _L = 20 pF | 2 V | 24 | | | ns |
| | | | 3 V | 16 | | | |

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(eUSCI)}, t_{SU,MI(Master)} + t_{VALID,SO(eUSCI)})$.

For the master's parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$ refer to the SPI parameters of the attached slave.

(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in Figure 15 and Figure 16.

(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in Figure 15 and Figure 16.

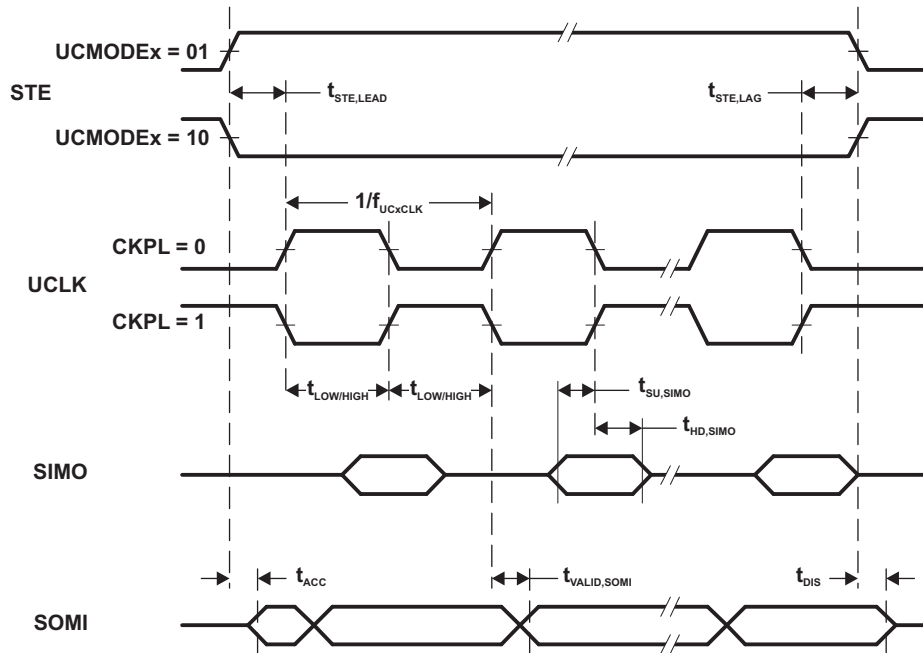


Figure 15. SPI Slave Mode, CKPH = 0

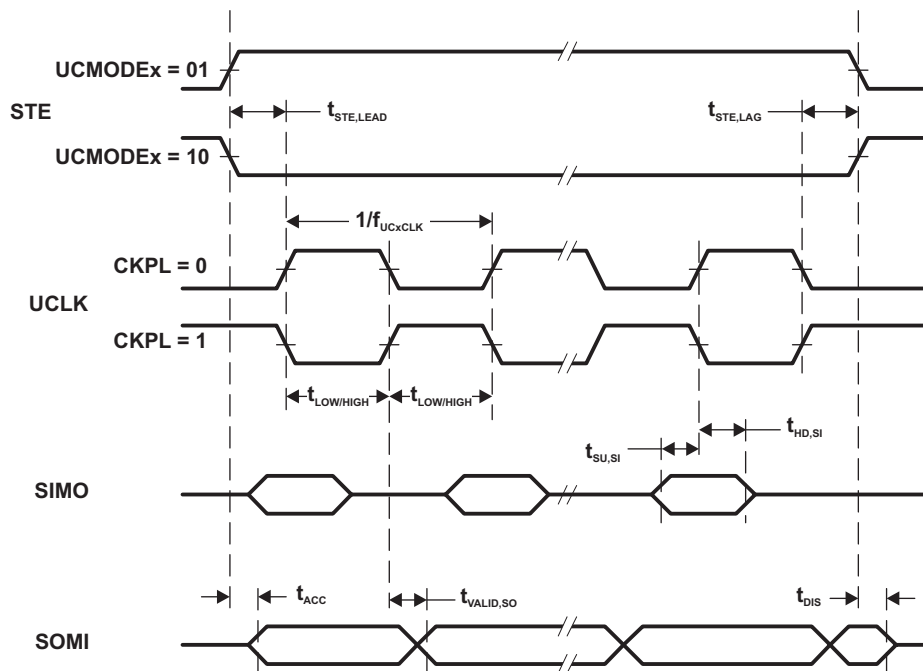
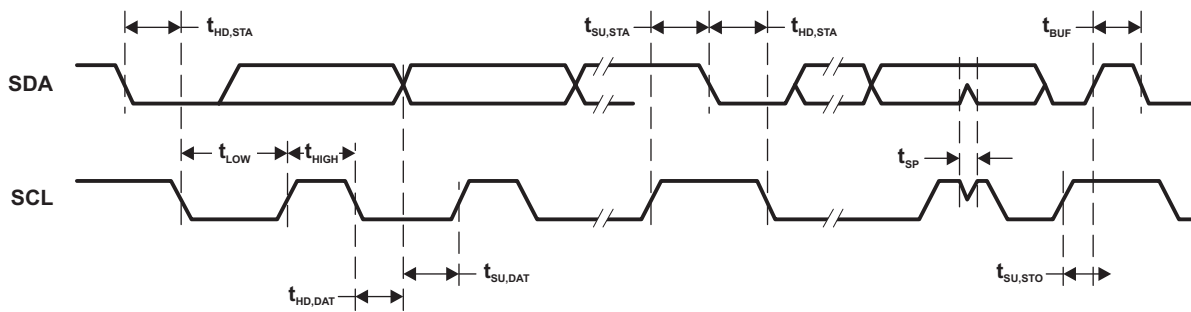


Figure 16. SPI Slave Mode, CKPH = 1

eUSCI (I2C Mode)

 over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 17](#))

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT | |
|----------------------|--|--|-------------|---------------------|-----|------|----|
| f _{eUSCI} | eUSCI input clock frequency Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10% | | | f _{SYSTEM} | | MHz | |
| f _{SCL} | SCL clock frequency | 2 V, 3 V | 0 | | 400 | kHz | |
| t _{HD,STA} | Hold time (repeated) START | f _{SCL} = 100 kHz 2 V, 3 V | 5.1 | | | μs | |
| | | f _{SCL} > 100 kHz | 1.5 | | | | |
| t _{SU,STA} | Setup time for a repeated START | f _{SCL} = 100 kHz 2 V, 3 V | 5.1 | | | μs | |
| | | f _{SCL} > 100 kHz | 1.4 | | | | |
| t _{HD,DAT} | Data hold time | 2 V, 3 V | 0.4 | | | μs | |
| t _{SU,DAT} | Data setup time | f _{SCL} = 100 kHz 2 V, 3 V | 5.0 | | | μs | |
| | | f _{SCL} > 100 kHz | 1.3 | | | | |
| t _{SU,STO} | Setup time for STOP | f _{SCL} = 100 kHz 2 V, 3 V | 5.2 | | | μs | |
| | | f _{SCL} > 100 kHz | 1.7 | | | | |
| t _{SP} | Pulse duration of spikes suppressed by input filter | 2 V, 3 V | UCGLITx = 0 | | 75 | 220 | ns |
| | | | UCGLITx = 1 | | 35 | 120 | ns |
| | | | UCGLITx = 2 | | 30 | 60 | ns |
| | | | UCGLITx = 3 | | 20 | 35 | ns |
| t _{TIMEOUT} | Clock low timeout | 2 V, 3 V | UCCLTOx = 1 | | 30 | | ms |
| | | | UCCLTOx = 2 | | 33 | | ms |
| | | | UCCLTOx = 3 | | 37 | | ms |


Figure 17. I2C Mode Timing

Schmitt-Trigger Inputs – RTC Tamper Detect Pin

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | AUXVCC3 | MIN | TYP | MAX | UNIT |
|-------------------|---|--|------|-----|------|------|
| V _{IT+} | Positive-going input threshold voltage | 1.8 V | 0.80 | | 1.40 | V |
| | | 3 V | 1.50 | | 2.10 | |
| V _{IT-} | Negative-going input threshold voltage | 1.8 V | 0.45 | | 1.00 | V |
| | | 3 V | 0.75 | | 1.65 | |
| V _{hys} | Input voltage hysteresis (V _{IT+} – V _{IT-}) | 1.8 V | 0.3 | | 0.85 | V |
| | | 3 V | 0.4 | | 1.0 | |
| R _{Pull} | Pullup or pulldown resistor | For pullup: V _{IN} = V _{SS} For pulldown: V _{IN} = AUXVCC3 | 20 | 35 | 50 | kΩ |
| C _I | Input capacitance | V _{IN} = V _{SS} or AUXVCC3 | | 5 | | pF |

Inputs – RTC Tamper Detect Pin⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | AUXVCC3 | MIN | MAX | UNIT |
|-------------|--|--|------------|-----|-----|------|
| $t_{(int)}$ | External interrupt timing ⁽²⁾ | Port P1, P2: P1.x to P2.x, External trigger pulse duration to set interrupt flag | 2.2 V, 3 V | 20 | | ns |

- (1) Some devices may contain additional ports with interrupts. See the block diagram and terminal function descriptions.
 (2) An external signal sets the interrupt flag every time the minimum interrupt pulse duration $t_{(int)}$ is met. It may be set by trigger signals shorter than $t_{(int)}$.

Leakage Current – RTC Tamper Detect Pin

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | AUXVCC3 | MIN | MAX | UNIT |
|-----------------|--------------------------------|-----------------|---------------------------------|-----|-----|------|
| $I_{lkg(Px.y)}$ | High-impedance leakage current | | ⁽¹⁾⁽²⁾ 1.8 V, 3 V | -50 | +50 | nA |

- (1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pins, unless otherwise noted.
 (2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.

Outputs – RTC Tamper Detect Pin

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | AUXVCC3 | MIN | MAX | UNIT |
|-----------|---------------------------|----------------------------------|---------|------|------|------|
| V_{OH} | High-level output voltage | $I_{(OHmax)} = -100 \mu A^{(1)}$ | 1.8 V | 1.50 | 1.80 | V |
| | | $I_{(OHmax)} = -200 \mu A^{(1)}$ | | 1.20 | 1.80 | |
| | | $I_{(OHmax)} = -100 \mu A^{(1)}$ | 3 V | 2.70 | 3.00 | |
| | | $I_{(OHmax)} = -200 \mu A^{(1)}$ | | 2.40 | 3.00 | |
| V_{OL} | Low-level output voltage | $I_{(OLmax)} = 100 \mu A^{(1)}$ | 1.8 V | 0.00 | 0.25 | V |
| | | $I_{(OLmax)} = 200 \mu A^{(1)}$ | | 0.00 | 0.60 | |
| | | $I_{(OLmax)} = 100 \mu A^{(1)}$ | 3 V | 0.00 | 0.25 | |
| | | $I_{(OLmax)} = 200 \mu A^{(1)}$ | | 0.00 | 0.60 | |

- (1) The maximum total current, $I_{(OHmax)}$, for all outputs combined should not exceed ± 20 mA to hold the maximum voltage drop specified. See [Recommended Operating Conditions](#) for more details.

LCD_C Recommended Operating Conditions

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT | |
|----------------------------|--|---|-----|-----------|---|------------------|
| $V_{CC,LCD_C,CP\ en,3.6}$ | Supply voltage range, charge pump enabled, $V_{LCD} \leq 3.6\text{ V}$ | LCDCPEN = 1, $0000 < VLCDx \leq 1111$ (charge pump enabled, $V_{LCD} \leq 3.6\text{ V}$) | | 2.2 | 3.6 | V |
| $V_{CC,LCD_C,CP\ en,3.3}$ | Supply voltage range, charge pump enabled, $V_{LCD} \leq 3.3\text{ V}$ | LCDCPEN = 1, $0000 < VLCDx \leq 1100$ (charge pump enabled, $V_{LCD} \leq 3.3\text{ V}$) | | 2.0 | 3.6 | V |
| $V_{CC,LCD_C,int.\ bias}$ | Supply voltage range, internal biasing, charge pump disabled | LCDCPEN = 0, VLCDEXT = 0 | | 2.4 | 3.6 | V |
| $V_{CC,LCD_C,ext.\ bias}$ | Supply voltage range, external biasing, charge pump disabled | LCDCPEN = 0, VLCDEXT = 0 | | 2.4 | 3.6 | V |
| $V_{CC,LCD_C,VLCDEXT}$ | Supply voltage range, external LCD voltage, internal or external biasing, charge pump disabled | LCDCPEN = 0, VLCDEXT = 1 | | 2.0 | 3.6 | V |
| $V_{LCDCAP/R33}$ | External LCD voltage at LCDCAP/R33, internal or external biasing, charge pump disabled | LCDCPEN = 0, VLCDEXT = 1 | | 2.4 | 3.6 | V |
| C_{LCDCAP} | Capacitor on LCDCAP when charge pump enabled | LCDCPEN = 1, $VLCDx > 0000$ (charge pump enabled) | | 4.7 | 4.7 | 10 μF |
| f_{Frame} | LCD frame frequency range | $f_{LCD} = 2 \times \text{mux} \times f_{FRAME}$ with mux = 1 (static), 2, 3, 4. | | 0 | 100 | Hz |
| $f_{ACLK,in}$ | ACLK input frequency range | | | 30 | 32 | 40 kHz |
| C_{Panel} | Panel capacitance | 100-Hz frame frequency | | | 10000 | pF |
| V_{R33} | Analog input voltage at R33 | LCDCPEN = 0, VLCDEXT = 1 | | 2.4 | $V_{CC}+0.2$ | V |
| $V_{R23,1/3bias}$ | Analog input voltage at R23 | LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 0 | | V_{R13} | $\frac{V_{R03} + 2/3*(V_{R33} - V_{R03})}{V_{R33}}$ | V |
| $V_{R13,1/3bias}$ | Analog input voltage at R13 with 1/3 biasing | LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 0 | | V_{R03} | $\frac{V_{R03} + 1/3*(V_{R33} - V_{R03})}{V_{R23}}$ | V |
| $V_{R13,1/2bias}$ | Analog input voltage at R13 with 1/2 biasing | LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 1 | | V_{R03} | $\frac{V_{R03} + 1/2*(V_{R33} - V_{R03})}{V_{R33}}$ | V |
| V_{R03} | Analog input voltage at R03 | R0EXT = 1 | | V_{SS} | | V |
| $V_{LCD}-V_{R03}$ | Voltage difference between V_{LCD} and R03 | LCDCPEN = 0, R0EXT = 1 | | 2.4 | $V_{CC}+0.2$ | V |
| $V_{LCDREF/R13}$ | External LCD reference voltage applied at LCDREF/R13 | VLCDFREFx = 01 | | 0.8 | 1.2 | 1.5 V |

LCD_C Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------------|--|--|-----------------|------|-----------------|-----|------|
| V _{LCD} | LCD voltage | VLCDx = 0000, VLCDEXT = 0 | 2.4 V to 3.6 V | | V _{CC} | | V |
| | | LCDCPEN = 1, VLCDx = 0001 | 2 V to 3.6 V | | 2.60 | | V |
| | | LCDCPEN = 1, VLCDx = 0010 | 2 V to 3.6 V | | 2.66 | | V |
| | | LCDCPEN = 1, VLCDx = 0011 | 2 V to 3.6 V | | 2.72 | | V |
| | | LCDCPEN = 1, VLCDx = 0100 | 2 V to 3.6 V | | 2.78 | | V |
| | | LCDCPEN = 1, VLCDx = 0101 | 2 V to 3.6 V | | 2.84 | | V |
| | | LCDCPEN = 1, VLCDx = 0110 | 2 V to 3.6 V | | 2.90 | | V |
| | | LCDCPEN = 1, VLCDx = 0111 | 2 V to 3.6 V | | 2.96 | | V |
| | | LCDCPEN = 1, VLCDx = 1000 | 2 V to 3.6 V | | 3.02 | | V |
| | | LCDCPEN = 1, VLCDx = 1001 | 2 V to 3.6 V | | 3.08 | | V |
| | | LCDCPEN = 1, VLCDx = 1010 | 2 V to 3.6 V | | 3.14 | | V |
| | | LCDCPEN = 1, VLCDx = 1011 | 2 V to 3.6 V | | 3.20 | | V |
| | | LCDCPEN = 1, VLCDx = 1100 | 2 V to 3.6 V | | 3.26 | | V |
| | | LCDCPEN = 1, VLCDx = 1101 | 2.2 V to 3.6 V | | 3.32 | | V |
| | | LCDCPEN = 1, VLCDx = 1110 | 2.2 V to 3.6 V | | 3.38 | | V |
| LCDCPEN = 1, VLCDx = 1111 | 2.2 V to 3.6 V | | 3.50 | 3.72 | V | | |
| I _{CC,Peak,CP} | Peak supply currents due to charge pump activities | LCDCPEN = 1, VLCDx = 1111 | 2.2 V | | 200 | | μA |
| t _{LCD,CP,on} | Time to charge C _{LCD} when discharged | C _{LCD} = 4.7 μF, LCDCPEN = 0→1, VLCDx = 1111 | 2.2 V | | 100 | 500 | ms |
| I _{CP,Load} | Maximum charge pump load current | LCDCPEN = 1, VLCDx = 1111 | 2.2 V | 50 | | | μA |
| R _{LCD,Seg} | LCD driver output impedance, segment lines | LCDCPEN = 1, VLCDx = 1000, I _{LOAD} = ±10 μA | 2.2 V | | | 10 | kΩ |
| R _{LCD,COM} | LCD driver output impedance, common lines | LCDCPEN = 1, VLCDx = 1000, I _{LOAD} = ±10 μA | 2.2 V | | | 10 | kΩ |

SD24_B Power Supply and Recommended Operating Conditions

| | | | MIN | TYP | MAX | UNIT |
|-----------------|---|---|------------------------|------|-----------------|------|
| V_{CC} | Analog supply voltage | $AV_{CC} = DV_{CC}, AV_{SS} = DV_{SS} = 0\text{ V}$ | 2.4 | | 3.6 | V |
| T_A | Ambient temperature | | -40 | | 85 | °C |
| f_{SD} | Modulator clock frequency | | 0.03 | | 2.3 | MHz |
| V_I | Absolute input voltage range | | $AV_{SS} - 1\text{ V}$ | | AV_{CC} | V |
| V_{IC} | Common-mode input voltage range | | $AV_{SS} - 1\text{ V}$ | | AV_{CC} | V |
| $V_{ID,FS}$ | Differential full scale input voltage | Bipolar Mode, $V_{ID} = V_{I,A+} - V_{I,A-}$ | $V_{REF}/GAIN$ | | $+V_{REF}/GAIN$ | mV |
| | | Unipolar Mode, $V_{ID} = V_{I,A+} - V_{I,A-}$ | 0 | | $+V_{REF}/GAIN$ | |
| V_{ID} | Differential input voltage for specified performance ⁽¹⁾ | REFON = 1 | SD24GAINx = 1 | ±900 | ±930 | mV |
| | | | SD24GAINx = 2 | ±450 | ±460 | |
| | | | SD24GAINx = 4 | ±225 | ±230 | |
| | | | SD24GAINx = 8 | ±112 | ±120 | |
| | | | SD24GAINx = 16 | ±56 | ±60 | |
| | | | SD24GAINx = 32 | ±28 | ±30 | |
| | | | SD24GAINx = 64 | ±14 | ±14 | |
| SD24GAINx = 128 | ±7 | ±7.25 | | | | |
| C_{REF} | VREF load capacitance ⁽²⁾ | SD24REFS = 1 | | 100 | | nF |

(1) The full-scale range (FSR) is defined by $V_{FS+} = +V_{REF}/GAIN$ and $V_{FS-} = -V_{REF}/GAIN$: $FSR = V_{FS+} - V_{FS-} = 2 \cdot V_{REF}/GAIN$. If V_{REF} is sourced externally, the analog input range should not exceed 80% of V_{FS+} or V_{FS-} ; that is, $V_{ID} = 0.8 V_{FS-}$ to $0.8 V_{FS+}$. If V_{REF} is sourced internally, the given V_{ID} ranges apply. MIN values are calculated based on a V_{REF} of 1.125V. TYP values are calculated based on a V_{REF} of 1.16 V.

(2) There is no capacitance required on VREF. However, a capacitance of 100nF is recommended to reduce any reference voltage noise.

SD24_B Analog Input ⁽¹⁾

| PARAMETER | TEST CONDITIONS | | V_{CC} | MIN | TYP | MAX | UNIT |
|--|---------------------------|----------------|----------|-----|-----|-----|------|
| C_i Input capacitance | SD24GAINx = 1 | | | | 5.0 | | pF |
| | SD24GAINx = 2 | | | | 5.0 | | |
| | SD24GAINx = 4 | | | | 5.0 | | |
| | SD24GAINx = 8 | | | | 5.0 | | |
| | SD24GAINx = 16 | | | | 5.0 | | |
| | SD24GAINx = 32, 64, 128 | | | | 5.0 | | |
| Z_i Input impedance (pin A+ or A- to AV_{SS}) | $f_{SD24} = 1\text{ MHz}$ | SD24GAINx = 1 | 3 V | | 200 | | kΩ |
| | | SD24GAINx = 8 | 3 V | | 200 | | |
| | | SD24GAINx = 32 | 3 V | | 200 | | |
| Z_{ID} Differential input impedance (pin A+ to pin A-) | $f_{SD24} = 1\text{ MHz}$ | SD24GAINx = 1 | 3 V | 300 | 400 | | kΩ |
| | | SD24GAINx = 8 | 3 V | | 400 | | |
| | | SD24GAINx = 32 | 3 V | 300 | 400 | | |

(1) All parameters pertain to each SD24_B converter.

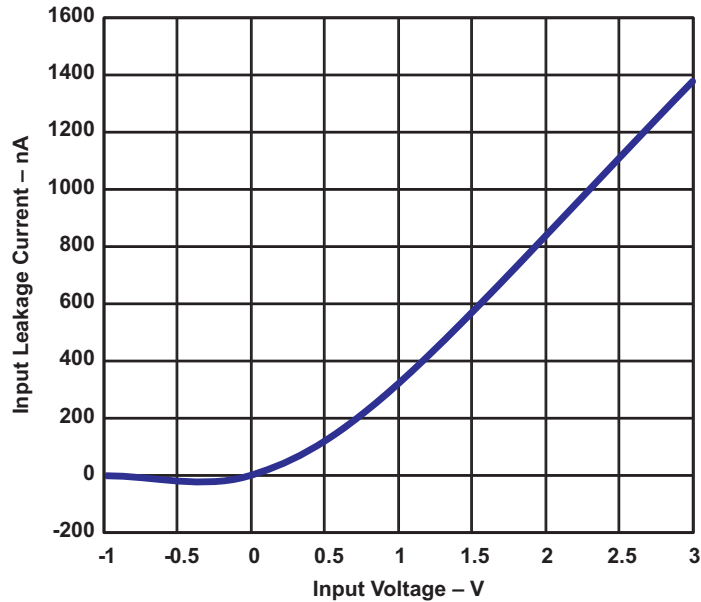


Figure 18. Input Leakage Current vs Input Voltage (Modulator OFF)

SD24_B Supply Currents

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT | |
|---|--|-----------------|-----|-----|-----|------|----|
| I _{SD,256} Analog plus digital supply current per converter (reference not included) | f _{SD24} = 1 MHz, SD24OSR = 256 | SD24GAIN: 1 | 3 V | | 490 | 600 | μA |
| | | SD24GAIN: 2 | 3 V | | 490 | 600 | |
| | | SD24GAIN: 4 | 3 V | | 490 | 600 | |
| | | SD24GAIN: 8 | 3 V | | 559 | 700 | |
| | | SD24GAIN: 16 | 3 V | | 559 | 700 | |
| | | SD24GAIN: 32 | 3 V | | 627 | 800 | |
| | | SD24GAIN: 64 | 3 V | | 627 | 800 | |
| I _{SD,512} Analog plus digital supply current per converter (reference not included) | f _{SD24} = 2 MHz, SD24OSR = 512 | SD24GAIN: 1 | 3 V | | 600 | 700 | μA |
| | | SD24GAIN: 8 | 3 V | | 677 | 800 | |
| | | SD24GAIN: 32 | 3 V | | 740 | 900 | |

SD24_B Performance

f_{SD24} = 1 MHz, SD24OSRx = 256, SD24REFON = 1

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--|-----------------|-----------------|-------|-----|-------|----------|
| INL Integral nonlinearity, end-point fit | SD24GAIN: 1 | 3 V | -0.01 | | +0.01 | % of FSR |
| | SD24GAIN: 8 | 3 V | -0.01 | | +0.01 | |
| | SD24GAIN: 32 | 3 V | -0.01 | | +0.01 | |
| G _{nom} Nominal gain | SD24GAIN: 1 | 3 V | | 1 | | |
| | SD24GAIN: 2 | 3 V | | 2 | | |
| | SD24GAIN: 4 | 3 V | | 4 | | |
| | SD24GAIN: 8 | 3 V | | 8 | | |
| | SD24GAIN: 16 | 3 V | | 16 | | |
| | SD24GAIN: 32 | 3 V | | 32 | | |
| | SD24GAIN: 64 | 3 V | | 64 | | |
| SD24GAIN: 128 | 3 V | | 128 | | | |

SD24_B Performance (continued)
 $f_{SD24} = 1 \text{ MHz}$, $SD24OSRx = 256$, $SD24REFON = 1$

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|-------------------------------|--|---|-----|------|------|------|------------------|
| E_G | Gain error ⁽¹⁾ | SD24GAIN: 1, with external reference (1.2 V) | 3 V | -1 | | +1 | % |
| | | SD24GAIN: 8, with external reference (1.2 V) | 3 V | -2 | | +2 | |
| | | SD24GAIN: 32, with external reference (1.2 V) | 3 V | -2 | | +2 | |
| $\Delta E_G/\Delta T$ | Gain error temperature coefficient ⁽²⁾ , internal reference | SD24GAIN: 1, 8, or 32 (with internal reference) | 3 V | | | 80 | ppm/°C |
| $\Delta E_G/\Delta T$ | Gain error temperature coefficient ⁽²⁾ , external reference | SD24GAIN: 1 (with external reference) | 3 V | | | 15 | ppm/°C |
| | | SD24GAIN: 8 (with external reference) | 3 V | | | 15 | |
| | | SD24GAIN: 32 (with external reference) | 3 V | | | 15 | |
| $\Delta E_G/\Delta V_{CC}$ | Gain error vs V_{CC} ⁽³⁾ | SD24GAIN: 1 | 3 V | | 0.1 | | %/V |
| | | SD24GAIN: 8 | 3 V | | 0.1 | | |
| | | SD24GAIN: 32 | 3 V | | 0.4 | | |
| $E_{OS}[V]$ | Offset error ⁽⁴⁾ | SD24GAIN: 1 (with $V_{diff} = 0V$) | 3 V | | | 2.3 | mV |
| | | SD24GAIN: 8 | 3 V | | | 1 | |
| | | SD24GAIN: 32 | 3 V | | | 0.5 | |
| $E_{OS}[FS]$ | Offset error ⁽⁴⁾ | SD24GAIN: 1 (with $V_{diff} = 0V$) | 3 V | -0.2 | | +0.2 | % FS |
| | | SD24GAIN: 8 | 3 V | -0.7 | | +0.7 | % FS |
| | | SD24GAIN: 32 | 3 V | -1.4 | | +1.4 | % FS |
| $\Delta E_{OS}/\Delta T$ | Offset error temperature coefficient ⁽⁵⁾ | SD24GAIN: 1 | 3 V | | 2 | | $\mu V/^\circ C$ |
| | | SD24GAIN: 8 | 3 V | | 0.25 | | |
| | | SD24GAIN: 32 | 3 V | | 0.1 | | |
| $\Delta E_{OS}/\Delta V_{CC}$ | Offset error vs V_{CC} ⁽⁶⁾ | SD24GAIN: 1 | 3 V | | 500 | | $\mu V/V$ |
| | | SD24GAIN: 8 | 3 V | | 125 | | |
| | | SD24GAIN: 32 | 3 V | | 50 | | |
| CMRR,DC | Common mode rejection at DC ⁽⁷⁾ | SD24GAIN: 1 | 3 V | | -120 | | dB |
| | | SD24GAIN: 8 | 3 V | | -110 | | |
| | | SD24GAIN: 32 | 3 V | | -100 | | |

- The gain error E_G specifies the deviation of the actual gain G_{act} from the nominal gain G_{nom} : $E_G = (G_{act} - G_{nom})/G_{nom}$. It covers process, temperature and supply voltage variations.
- The gain error temperature coefficient $\Delta E_G/\Delta T$ specifies the variation of the gain error E_G over temperature ($E_G(T) = (G_{act}(T) - G_{nom})/G_{nom}$) using the box method (that is, minimum and maximum values):
 $\Delta E_G/\Delta T = (\text{MAX}(E_G(T)) - \text{MIN}(E_G(T))) / (\text{MAX}(T) - \text{MIN}(T)) = (\text{MAX}(G_{act}(T)) - \text{MIN}(G_{act}(T))) / G_{nom} / (\text{MAX}(T) - \text{MIN}(T))$
 with T ranging from -40°C to +85°C.
- The gain error vs V_{CC} coefficient $\Delta E_G/\Delta V_{CC}$ specifies the variation of the gain error E_G over supply voltage ($E_G(V_{CC}) = (G_{act}(V_{CC}) - G_{nom})/G_{nom}$) using the box method (that is, minimum and maximum values):
 $\Delta E_G/\Delta V_{CC} = (\text{MAX}(E_G(V_{CC})) - \text{MIN}(E_G(V_{CC}))) / (\text{MAX}(V_{CC}) - \text{MIN}(V_{CC})) = (\text{MAX}(G_{act}(V_{CC})) - \text{MIN}(G_{act}(V_{CC}))) / G_{nom} / (\text{MAX}(V_{CC}) - \text{MIN}(V_{CC}))$
 with V_{CC} ranging from 2.4V to 3.6V.
- The offset error E_{OS} is measured with shorted inputs in 2s complement mode with +100% FS = V_{REF}/G and -100% FS = $-V_{REF}/G$. Conversion between E_{OS} [FS] and E_{OS} [V] is as follows: E_{OS} [FS] = E_{OS} [V] × G/V_{REF} ; E_{OS} [V] = E_{OS} [FS] × V_{REF}/G .
- The offset error temperature coefficient $\Delta E_{OS}/\Delta T$ specifies the variation of the offset error E_{OS} over temperature using the box method (that is, minimum and maximum values):
 $\Delta E_{OS}/\Delta T = (\text{MAX}(E_{OS}(T)) - \text{MIN}(E_{OS}(T))) / (\text{MAX}(T) - \text{MIN}(T))$
 with T ranging from -40°C to +85°C.
- The offset error vs V_{CC} $\Delta E_{OS}/\Delta V_{CC}$ specifies the variation of the offset error E_{OS} over supply voltage using the box method (that is, minimum and maximum values):
 $\Delta E_{OS}/\Delta V_{CC} = (\text{MAX}(E_{OS}(V_{CC})) - \text{MIN}(E_{OS}(V_{CC}))) / (\text{MAX}(V_{CC}) - \text{MIN}(V_{CC}))$
 with V_{CC} ranging from 2.4V to 3.6V.
- The DC CMRR specifies the change in the measured differential input voltage value when the common mode voltage varies:
 $\text{DC CMRR} = -20\log(\Delta_{MAX}/FSR)$ with Δ_{MAX} being the difference between the minimum value and the maximum value measured when sweeping the common mode voltage.
 The DC CMRR is measured with both inputs connected to the common mode voltage (that is, no differential input signal is applied), and the common mode voltage is swept from -1V to V_{CC} .

SD24_B Performance (continued)

 $f_{SD24} = 1 \text{ MHz}$, $SD24OSRx = 256$, $SD24REFON = 1$

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|-------------|--|---|-----|-----|------|-----|------|
| CMRR,50Hz | Common mode rejection at 50 Hz ⁽⁸⁾ | SD24GAIN: 1, $f_{CM} = 50 \text{ Hz}$, $V_{CM} = 930 \text{ mV}$ | 3 V | | -120 | | dB |
| | | SD24GAIN: 8, $f_{CM} = 50 \text{ Hz}$, $V_{CM} = 120 \text{ mV}$ | 3 V | | -110 | | |
| | | SD24GAIN: 32, $f_{CM} = 50 \text{ Hz}$, $V_{CM} = 30 \text{ mV}$ | 3 V | | -100 | | |
| AC PSRR,ext | AC power supply rejection ratio, external reference ⁽⁹⁾ | SD24GAIN: 1, $V_{CC} = 3 \text{ V} + 50 \text{ mV} \times \sin(2\pi \times f_{VCC} \times t)$, $f_{VCC} = 50 \text{ Hz}$ | | | -61 | | dB |
| | | SD24GAIN: 8, $V_{CC} = 3 \text{ V} + 50 \text{ mV} \times \sin(2\pi \times f_{VCC} \times t)$, $f_{VCC} = 50 \text{ Hz}$ | | | -75 | | |
| | | SD24GAIN: 32, $V_{CC} = 3 \text{ V} + 50 \text{ mV} \times \sin(2\pi \times f_{VCC} \times t)$, $f_{VCC} = 50 \text{ Hz}$ | | | -79 | | |
| AC PSRR,int | AC power supply rejection ratio, internal reference ⁽⁹⁾ | SD24GAIN: 1, $V_{CC} = 3 \text{ V} + 50 \text{ mV} \times \sin(2\pi \times f_{VCC} \times t)$, $f_{VCC} = 50 \text{ Hz}$ | | | -61 | | dB |
| | | SD24GAIN: 8, $V_{CC} = 3 \text{ V} + 50 \text{ mV} \times \sin(2\pi \times f_{VCC} \times t)$, $f_{VCC} = 50 \text{ Hz}$ | | | -75 | | |
| | | SD24GAIN: 32, $V_{CC} = 3 \text{ V} + 50 \text{ mV} \times \sin(2\pi \times f_{VCC} \times t)$, $f_{VCC} = 50 \text{ Hz}$ | | | -79 | | |
| XT | Crosstalk between converters ⁽¹⁰⁾ | Crosstalk source: SD24GAIN: 1, Sine-wave with maximum possible V_{pp} , $f_{IN} = 50 \text{ Hz}$, 100 Hz, Converter under test: SD24GAIN: 1 | 3 V | | -120 | | dB |
| | | Crosstalk source: SD24GAIN: 1, Sine-wave with maximum possible V_{pp} , $f_{IN} = 50 \text{ Hz}$, 100 Hz, Converter under test: SD24GAIN: 8 | 3 V | | -115 | | |
| | | Crosstalk source: SD24GAIN: 1, Sine-wave with maximum possible V_{pp} , $f_{IN} = 50 \text{ Hz}$, 100 Hz, Converter under test: SD24GAIN: 32 | 3 V | | -110 | | |

(8) The AC CMRR is the difference between a hypothetical signal with the amplitude and frequency of the applied common mode ripple applied to the inputs of the ADC and the actual common mode signal spur visible in the FFT spectrum:
 $AC \text{ CMRR} = \text{Error Spur [dBFS]} - 20\log(V_{CM}/1.2V/G) \text{ [dBFS]}$ with a common mode signal of $V_{CM} \times \sin(2\pi \times f_{CM} \times t)$ applied to the analog inputs.

The AC CMRR is measured with the both inputs connected to the common mode signal; that is, no differential input signal is applied. With the specified typical values the error spur is within the noise floor (as specified by the SINAD values).

(9) The AC PSRR is the difference between a hypothetical signal with the amplitude and frequency of the applied supply voltage ripple applied to the inputs of the ADC and the actual supply ripple spur visible in the FFT spectrum:
 $AC \text{ PSRR} = \text{Error Spur [dBFS]} - 20\log(50\text{mV}/1.2V/G) \text{ [dBFS]}$ with a signal of $50\text{mV} \times \sin(2\pi \times f_{VCC} \times t)$ added to V_{CC} .

The AC PSRR is measured with the inputs grounded; that is, no analog input signal is applied.

With the specified typical values the error spur is within the noise floor (as specified by the SINAD values).

SD24GAIN: 1 → Hypothetical signal: $20\log(50\text{mV}/1.2V/1) = -27.6 \text{ dBFS}$

SD24GAIN: 8 → Hypothetical signal: $20\log(50\text{mV}/1.2V/8) = -9.5 \text{ dBFS}$

SD24GAIN: 32 → Hypothetical signal: $20\log(50\text{mV}/1.2V/32) = 2.5 \text{ dBFS}$

(10) The crosstalk XT is specified as the tone level of the signal applied to the crosstalk source seen in the spectrum of the converter under test. It is measured with the inputs of the converter under test being grounded.

SD24_B, AC Performance

 $f_{SD24} = 1 \text{ MHz}$, $SD24OSRx = 256$, $SD24REFON = 1$

| PARAMETER | | TEST CONDITIONS | V_{CC} | MIN | TYP | MAX | UNIT |
|-----------|------------------------------------|-----------------|------------------------------|-----|-----|-----|------|
| SINAD | Signal-to-noise + distortion ratio | SD24GAIN: 1 | $f_{IN} = 50\text{Hz}^{(1)}$ | 3 V | 84 | 86 | dB |
| | | SD24GAIN: 2 | | | 85 | | |
| | | SD24GAIN: 4 | | | 84 | | |
| | | SD24GAIN: 8 | | | 81 | 83 | |
| | | SD24GAIN: 16 | | | 80 | | |
| | | SD24GAIN: 32 | | | 71 | 73 | |
| | | SD24GAIN: 64 | | | 67 | | |
| | | SD24GAIN: 128 | | | 61 | | |
| THD | Total harmonic distortion | SD24GAIN: 1 | $f_{IN} = 50\text{Hz}^{(1)}$ | 3 V | 95 | dB | |
| | | SD24GAIN: 8 | | | 90 | | |
| | | SD24GAIN: 32 | | | 86 | | |

- (1) The following voltages were applied to the SD24_B inputs: $V_{I,A+}(t) = 0 \text{ V} + V_{PP}/2 \times \sin(2\pi \times f_{IN} \times t)$ and $V_{I,A-}(t) = 0 \text{ V} - V_{PP}/2 \times \sin(2\pi \times f_{IN} \times t)$ resulting in a differential voltage of $V_{ID} = V_{I,A+}(t) - V_{I,A-}(t) = V_{PP} \times \sin(2\pi \times f_{IN} \times t)$ with V_{PP} being selected as the maximum value allowed for a given range (according to SD24_B recommended operating conditions).

SD24_B, AC Performance

 $f_{SD24} = 2 \text{ MHz}$, $SD24OSRx = 512$, $SD24REFON = 1$

| PARAMETER | | TEST CONDITIONS | V_{CC} | MIN | TYP | MAX | UNIT |
|-----------|------------------------------------|-----------------|------------------------------|-----|-----|-----|------|
| SINAD | Signal-to-noise + distortion ratio | SD24GAIN: 1 | $f_{IN} = 50\text{Hz}^{(1)}$ | 3 V | 87 | dB | |
| | | SD24GAIN: 2 | | | 85 | | |
| | | SD24GAIN: 4 | | | 84 | | |
| | | SD24GAIN: 8 | | | 83 | | |
| | | SD24GAIN: 16 | | | 81 | | |
| | | SD24GAIN: 32 | | | 76 | | |
| | | SD24GAIN: 64 | | | 71 | | |
| | | SD24GAIN: 128 | | | 65 | | |

- (1) The following voltages were applied to the SD24_B inputs: $V_{I,A+}(t) = 0 \text{ V} + V_{PP}/2 \times \sin(2\pi \times f_{IN} \times t)$ and $V_{I,A-}(t) = 0 \text{ V} - V_{PP}/2 \times \sin(2\pi \times f_{IN} \times t)$ resulting in a differential voltage of $V_{ID} = V_{I,A+}(t) - V_{I,A-}(t) = V_{PP} \times \sin(2\pi \times f_{IN} \times t)$ with V_{PP} being selected as the maximum value allowed for a given range (according to SD24_B recommended operating conditions).

SD24_B, AC Performance

 $f_{SD24} = 32 \text{ kHz}$, $SD24OSRx = 512$, $SD24REFON = 1$

| PARAMETER | | TEST CONDITIONS | V_{CC} | MIN | TYP | MAX | UNIT |
|-----------|------------------------------------|-----------------|------------------------------|-----|-----|-----|------|
| SINAD | Signal-to-noise + distortion ratio | SD24GAIN: 1 | $f_{IN} = 50\text{Hz}^{(1)}$ | 3 V | 89 | dB | |
| | | SD24GAIN: 2 | | | 85 | | |
| | | SD24GAIN: 4 | | | 84 | | |
| | | SD24GAIN: 8 | | | 82 | | |
| | | SD24GAIN: 16 | | | 80 | | |
| | | SD24GAIN: 32 | | | 76 | | |
| | | SD24GAIN: 64 | | | 67 | | |
| | | SD24GAIN: 128 | | | 61 | | |

- (1) The following voltages were applied to the SD24_B inputs: $V_{I,A+}(t) = 0 \text{ V} + V_{PP}/2 \times \sin(2\pi \times f_{IN} \times t)$ and $V_{I,A-}(t) = 0 \text{ V} - V_{PP}/2 \times \sin(2\pi \times f_{IN} \times t)$ resulting in a differential voltage of $V_{ID} = V_{I,A+}(t) - V_{I,A-}(t) = V_{PP} \times \sin(2\pi \times f_{IN} \times t)$ with V_{PP} being selected as the maximum value allowed for a given range (according to SD24_B recommended operating conditions).

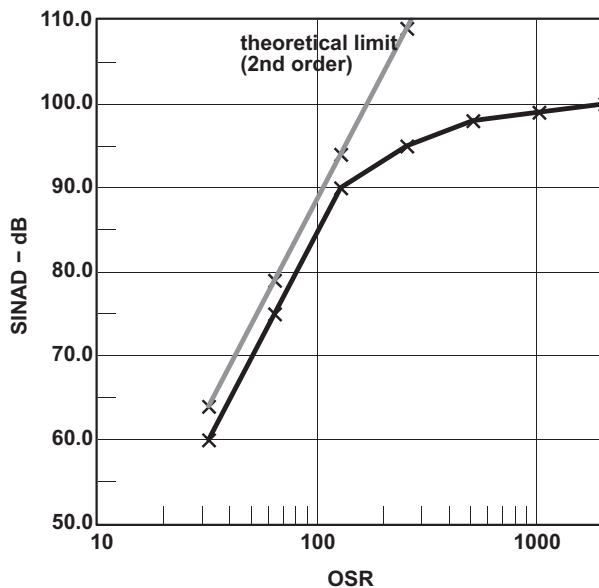


Figure 19. SINAD vs OSR
($f_{SD24} = 1\text{MHz}$, $SD24REFON = 1$, $SD24GAIN: 1$)

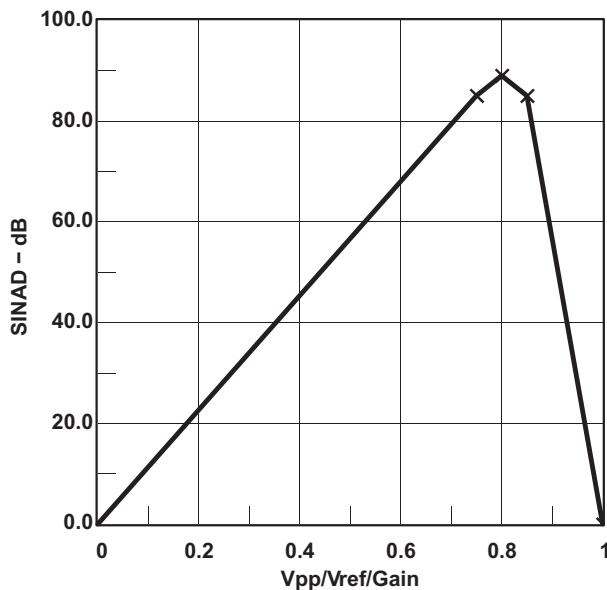


Figure 20. SINAD vs V_{PP}

SD24_B External Reference Input

ensure correct input voltage range according to V_{REF}

| PARAMETER | TEST CONDITIONS | V_{CC} | MIN | TYP | MAX | UNIT |
|----------------------------|-----------------|----------|-----|------|-----|------|
| $V_{REF(I)}$ Input voltage | $SD24REFS = 0$ | 3 V | 1.0 | 1.20 | 1.5 | V |
| $I_{REF(I)}$ Input current | $SD24REFS = 0$ | 3 V | | | 50 | nA |

10-Bit ADC Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---|---|---|-----------------|-----|-----|------------------|------|
| AV _{CC} | Analog supply voltage | AV _{CC} and DV _{CC} are connected together, AV _{SS} and DV _{SS} are connected together, V _(AVSS) = V _(DVSS) = 0 V | | 1.8 | | 3.6 | V |
| V _(Ax) | Analog input voltage range ⁽¹⁾ | All ADC10_A pins | | 0 | | AV _{CC} | V |
| I _{ADC10_A} | Operating supply current into AV _{CC} terminal, REF module and reference buffer off | f _{ADC10CLK} = 5 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 00 | 2.2 V | | 68 | 100 | μA |
| | | | 3 V | | 78 | 110 | |
| | Operating supply current into AV _{CC} terminal, REF module on, reference buffer on | f _{ADC10CLK} = 5 MHz, ADC10ON = 1, REFON = 1, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 01 | 3 V | | 124 | 180 | μA |
| | | f _{ADC10CLK} = 5 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 10, VREF = 2.5 V | 3 V | | 105 | 160 | μA |
| Operating supply current into AV _{CC} terminal, REF module off, reference buffer off | f _{ADC10CLK} = 5 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 11, VREF = 2.5 V | 3 V | | 72 | 110 | μA | |
| C _I | Input capacitance | Only one terminal Ax can be selected at one time from the pad to the ADC10_A capacitor array including wiring and pad. | 2.2 V | | 3.5 | | pF |
| R _I | Input MUX ON resistance | AV _{CC} > 2.0V, 0 V ≤ V _{Ax} ≤ AV _{CC} | | | | 36 | kΩ |
| | | 1.8V < AV _{CC} < 2.0V, 0 V ≤ V _{Ax} ≤ AV _{CC} | | | | 96 | |

- (1) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results. The external reference voltage requires decoupling capacitors. Two decoupling capacitors, 10 μF and 100 nF, should be connected to VREF to decouple the dynamic current required for an external reference source if it is used for the ADC10_A. Also see the *MSP430x6xx Family User's Guide (SLAU208)*.

10-Bit ADC Timing Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|--|---|-----------------|------|--------------------|-----|------|
| f _{ADC10CLK} | | For specified performance of ADC10_A linearity parameters | 2.2 V, 3 V | 0.45 | 5 | 5.5 | MHz |
| f _{ADC10OSC} | Internal ADC10_A oscillator ⁽¹⁾ | ADC10DIV = 0, f _{ADC10CLK} = f _{ADC10OSC} | 2.2 V, 3 V | 4.4 | 4.9 | 5.6 | MHz |
| t _{CONVERT} | Conversion time | REFON = 0, Internal oscillator, 12 ADC10CLK cycles, 10-bit mode, f _{ADC10OSC} = 4 MHz to 5 MHz | 2.2 V, 3 V | 2.4 | | 3.0 | μs |
| | | External f _{ADC10CLK} from ACLK, MCLK or SMCLK, ADC10SSEL ≠ 0 | | | See ⁽²⁾ | | |
| t _{ADC10ON} | Turn on settling time of the ADC | See ⁽³⁾ | | | | 100 | ns |
| t _{Sample} | Sampling time | R _S = 1000 Ω, R _I = 96 kΩ, C _I = 3.5 pF ⁽⁴⁾ | 1.8 V | 3 | | | μs |
| | | R _S = 1000 Ω, R _I = 36 kΩ, C _I = 3.5 pF ⁽⁴⁾ | 3 V | 1 | | | μs |

- (1) The ADC10OSC is sourced directly from MODOSC inside the UCS.
 (2) $12 \times \text{ADC10DIV} \times 1/f_{\text{ADC10CLK}}$
 (3) The condition is that the error in a conversion started after t_{ADC10ON} is less than ±0.5 LSB. The reference and input signal are already settled.
 (4) Approximately eight Tau (τ) are needed to get an error of less than ±0.5 LSB

10-Bit ADC Linearity Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|----------------|------------------------------|---|-----------------|------|-----|------|------|
| E _I | Integral linearity error | $1.4\text{ V} \leq (V_{eREF+} - V_{REF-}/N_{eREF-})_{min} \leq 1.6\text{ V}$ | 2.2 V, 3 V | -1.0 | | +1.0 | LSB |
| | | $1.6\text{ V} < (V_{eREF+} - V_{REF-}/N_{eREF-})_{min} \leq V_{AVCC}$ | | -1.0 | | +1.0 | |
| E _D | Differential linearity error | $(V_{eREF+} - V_{REF-}/N_{eREF-})_{min} \leq (V_{eREF+} - V_{REF-}/N_{eREF-})$, C _{VREF+} = 20 pF | 2.2 V, 3 V | -1.0 | | +1.0 | LSB |
| E _O | Offset error | $(V_{eREF+} - V_{REF-}/N_{eREF-})_{min} \leq (V_{eREF+} - V_{REF-}/N_{eREF-})$, Internal impedance of source R _S < 100 Ω, C _{VREF+} = 20 pF | 2.2 V, 3 V | -1.0 | | +1.0 | LSB |
| E _G | Gain error | $(V_{eREF+} - V_{REF-}/N_{eREF-})_{min} \leq (V_{eREF+} - V_{REF-}/N_{eREF-})$, C _{VREF+} = 20 pF | 2.2 V, 3 V | -1.0 | | +1.0 | LSB |
| E _T | Total unadjusted error | $(V_{eREF+} - V_{REF-}/N_{eREF-})_{min} \leq (V_{eREF+} - V_{REF-}/N_{eREF-})$, C _{VREF+} = 20 pF | 2.2 V, 3 V | -2.0 | | +2.0 | LSB |

10-Bit ADC External Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--|---|--|-----------------|-------------------|-----|-----------------|------|
| V _{eREF+} | Positive external reference voltage input | $V_{eREF+} > V_{REF-}/N_{eREF-}$ ⁽²⁾ | | 1.4 | | V _{CC} | V |
| V _{eREF-} | Negative external reference voltage input | $V_{eREF+} > V_{REF-}/N_{eREF-}$ ⁽³⁾ | | 0 | | 1.2 | V |
| (V _{eREF+} - V _{eREF-}) | Differential external reference voltage input | $V_{eREF+} > V_{REF-}/N_{eREF-}$ ⁽⁴⁾ | | 1.4 | | V _{CC} | V |
| I _{VeREF+} I _{VeREF-} | Static input current | $1.4\text{ V} \leq V_{eREF+} \leq V_{AVCC}$, V _{eREF-} = 0 V, f _{ADC10CLK} = 5 MHz, ADC10SHTX = 0x0001, Conversion rate 200 ksp/s | 2.2 V, 3 V | -26 | | +26 | μA |
| | | $1.4\text{ V} \leq V_{eREF+} \leq V_{AVCC}$, V _{eREF-} = 0 V, f _{ADC10CLK} = 5 MHz, ADC10SHTX = 0x1000, Conversion rate 20 ksp/s | 2.2 V, 3 V | -1 | | +1 | μA |
| C _{VREF+} | Capacitance at VREF+ terminal | | | ⁽⁵⁾ 10 | | | μF |

- (1) The external reference is used during ADC conversion to charge and discharge the capacitance array. The input capacitance, C_I, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 10-bit accuracy.
- (2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
- (3) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
- (4) The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.
- (5) Two decoupling capacitors, 10 μF and 100 nF, should be connected to VREF to decouple the dynamic current required for an external reference source if it is used for the ADC10_A. Also see the *MSP430x5xx and MSP430x6xx Family User's Guide (SLAU208)*.

REF Built-In Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT | |
|-----------------------------|---|--|------------|-------|--------|--------|----|
| V _{REF+} | Positive built-in reference voltage | REFVSEL = {2} for 2.5 V, REFON = 1 | 3 V | 2.47 | 2.51 | 2.55 | V |
| | | REFVSEL = {1} for 2 V, REFON = 1 | 3 V | 1.96 | 1.99 | 2.02 | |
| | | REFVSEL = {0} for 1.5 V, REFON = 1 | 2.2 V, 3 V | 1.48 | 1.5 | 1.52 | |
| AV _{CC(min)} | AVCC minimum voltage, Positive built-in reference active | REFVSEL = {0} for 1.5 V | | 2.2 | | V | |
| | | REFVSEL = {1} for 2 V | | 2.2 | | | |
| | | REFVSEL = {2} for 2.5 V | | 2.7 | | | |
| I _{REF+} | Operating supply current into AVCC terminal ⁽¹⁾ | f _{ADC10CLK} = 5.0 MHz, REFON = 1, REFBURST = 0, REFVSEL = {2} for 2.5 V | 3 V | | 18 | 24 | μA |
| | | f _{ADC10CLK} = 5.0 MHz, REFON = 1, REFBURST = 0, REFVSEL = {1} for 2 V | 3 V | | 16.1 | 21 | μA |
| | | f _{ADC10CLK} = 5.0 MHz, REFON = 1, REFBURST = 0, REFVSEL = {0} for 1.5 V | 3 V | | 14.4 | 21 | μA |
| TC _{REF+} | Temperature coefficient of built-in reference ⁽²⁾ | I _{VREF+} = 0 A, REFVSEL = (0, 1, 2), REFON = 1 | | < 18 | 50 | ppm/°C | |
| I _{SENSOR} | Operating supply current into AVCC terminal ⁽³⁾ | REFON = 0, INCH = 0Ah, ADC10ON = N/A, T _A = 30°C | 2.2 V | | 17 | 22 | μA |
| | | | 3 V | | 17 | 22 | |
| V _{SENSOR} | See ⁽⁴⁾ | ADC10ON = 1, INCH = 0Ah, T _A = 30°C | 2.2 V | | 770 | mV | |
| | | | 3 V | | 770 | | |
| V _{MID} | AV _{CC} divider at channel 11 | ADC10ON = 1, INCH = 0Bh, V _{MID} is approximately 0.5 × V _{AVCC} | 2.2 V | 1.06 | 1.1 | 1.14 | V |
| | | | 3 V | 1.46 | 1.5 | 1.54 | |
| t _{SENSOR(sample)} | Sample time required if channel 10 is selected ⁽⁵⁾ | ADC10ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB | | 30 | | μs | |
| t _{VMID(sample)} | Sample time required if channel 11 is selected ⁽⁶⁾ | ADC10ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB | | 1 | | μs | |
| PSRR _{DC} | Power supply rejection ratio (dc) | AV _{CC} = AV _{CC(min)} - AV _{CC(max)} , T _A = 25°C, REFVSEL = (0, 1, 2), REFON = 1 | | 120 | | μV/V | |
| PSRR _{AC} | Power supply rejection ratio (ac) | AV _{CC} = AV _{CC(min)} - AV _{CC(max)} , T _A = 25°C, f = 1 kHz, ΔV _{pp} = 100 mV, REFVSEL = (0, 1, 2), REFON = 1 | | 6.4 | | mV/V | |
| t _{SETTLE} | Settling time of reference voltage ⁽⁷⁾ | AV _{CC} = AV _{CC(min)} - AV _{CC(max)} , REFVSEL = (0, 1, 2), REFON = 0 → 1 | | 75 | | μs | |
| V _{SD24REF} | SD24_B internal reference voltage | SD24REFS = 1 | 3 V | 1.151 | 1.1623 | 1.174 | V |
| t _{ON} | SD24_B internal reference turn-on time | SD24REFS = 0→1, C _{REF} = 100 nF | 3 V | | 200 | | μs |

- (1) The internal reference current is supplied via terminal AVCC. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an A/D conversion.
- (2) Calculated using the box method: (MAX(-40 to 85°C) - MIN(-40 to 85°C)) / MIN(-40 to 85°C)/(85°C - (-40°C)).
- (3) The sensor current I_{SENSOR} is consumed if (ADC10ON = 1 and REFON = 1) or (ADC10ON = 1 and INCH = 0Ah and sample signal is high). When REFON = 1, I_{SENSOR} is already included in I_{REF+}.
- (4) The temperature sensor offset can be as much as ±20°C. A single-point calibration is recommended in order to minimize the offset error of the built-in temperature sensor.
- (5) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time t_{SENSOR(on)}.
- (6) The on-time t_{VMID(on)} is included in the sampling time t_{VMID(sample)}; no additional on time is needed.
- (7) The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB.

Comparator_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT | |
|------------------------|---|---|------------|--------------------------------|------------------------------|--------------------------------|----|
| V _{CC} | Supply voltage | | 1.8 | | 3.6 | V | |
| I _{AVCC_COMP} | Comparator operating supply current into AVCC, Excludes reference resistor ladder | CBPWRMD = 00, CBON = 1, CBRSx = 00 | 1.8 V | | 40 | μA | |
| | | | 2.2 V | 22 | 50 | | |
| | | | 3 V | 32 | 65 | | |
| | | 2.2 V, 3 V | 10 | 30 | | | |
| | | CBPWRMD = 10, CBON = 1, CBRSx = 00 | 2.2 V, 3 V | 0.2 | 0.85 | | |
| I _{AVCC_REF} | Quiescent current of resistor ladder into AVCC, Includes REF module current | CBREFACC = 1, CBREFLx = 01, CBRSx = 10, REFON = 0, CBON = 0 | 2.2 V, 3 V | 10 | 22 | μA | |
| | | | 2.2 V, 3 V | 33 | 40 | μA | |
| V _{IC} | Common mode input range | | 0 | | V _{CC} -1 | V | |
| V _{OFFSET} | Input offset voltage | CBPWRMD = 00 | | -20 | +20 | mV | |
| | | CBPWRMD = 01, 10 | | -20 | +20 | mV | |
| C _{IN} | Input capacitance | | | 5 | | pF | |
| R _{SIN} | Series input resistance | ON - switch closed | | 3 | 4 | kΩ | |
| | | OFF - switch opened | | 50 | | MΩ | |
| t _{PD} | Propagation delay, response time | CBPWRMD = 00, CBF = 0 | | | 450 | ns | |
| | | CBPWRMD = 01, CBF = 0 | | | 600 | ns | |
| | | CBPWRMD = 10, CBF = 0 | | | 50 | μs | |
| t _{PD,filter} | Propagation delay with filter active | CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLy = 00 | | 0.30 | 0.6 | 1.5 | μs |
| | | CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLy = 01 | | 0.5 | 1.0 | 1.8 | μs |
| | | CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLy = 10 | | 0.8 | 1.8 | 3.4 | μs |
| | | CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLy = 11 | | 1.5 | 3.4 | 6.5 | μs |
| t _{EN_CMP} | Comparator enable time | CBON = 0 to CBON = 1, CBPWRMD = 00, 01 | | 1 | 2 | μs | |
| | | CBON = 0 to CBON = 1, CBPWRMD = 10 | | | 50 | μs | |
| t _{EN_REF} | Resistor reference enable time | CBON = 0 to CBON = 1 | | 1.0 | 1.5 | μs | |
| TC _{REF} | Temperature coefficient reference | | | | 50 | ppm/°C | |
| V _{CB_REF} | Reference voltage for a given tap | V _{IN} = reference into resistor ladder, n = 0 to 31 | | V _{IN} × (n+1.5) / 32 | V _{IN} × (n+1) / 32 | V _{IN} × (n+0.5) / 32 | V |

Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|-----|-----|-----|------|
| DV _{CC(PGM/ERASE)} | Program and erase supply voltage | 1.8 | | 3.6 | V |
| I _{PGM} | Average supply current from DV _{CC} during program | | 3 | 5 | mA |
| I _{ERASE} | Average supply current from DV _{CC} during erase | | 6 | 15 | mA |
| I _{MERASE} , I _{BANK} | Average supply current from DV _{CC} during mass erase or bank erase | | 6 | 15 | mA |

Flash Memory (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------|---|--------------------------|--------|--------|-----|---------------|
| t_{CPT} | Cumulative program time | See ⁽¹⁾ | | | 16 | ms |
| | Program and erase endurance | | 10^4 | 10^5 | | cycles |
| $t_{Retention}$ | Data retention duration | $T_J = 25^\circ\text{C}$ | 100 | | | years |
| t_{Word} | Word or byte program time | See ⁽²⁾ | 64 | | 85 | μs |
| $t_{Block, 0}$ | Block program time for first byte or word | See ⁽²⁾ | 49 | | 65 | μs |
| $t_{Block, 1-(N-1)}$ | Block program time for each additional byte or word, except for last byte or word | See ⁽²⁾ | 37 | | 49 | μs |
| $t_{Block, N}$ | Block program time for last byte or word | See ⁽²⁾ | 55 | | 73 | μs |
| t_{Erase} | Erase time for segment erase, mass erase, and bank erase when available | See ⁽²⁾ | 23 | | 32 | ms |
| $f_{MCLK,MGR}$ | MCLK frequency in marginal read mode (FCTL4.MGR0 = 1 or FCTL4.MGR1 = 1) | | 0 | | 1 | MHz |

- (1) The cumulative program time must not be exceeded when writing to a 128-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
- (2) These values are hardwired into the flash controller's state machine.

JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------|--|-----------------|-------|-----|-----|---------------|
| f_{SBW} | Spy-Bi-Wire input frequency | 2.2 V, 3 V | 0 | | 20 | MHz |
| $t_{SBW,Low}$ | Spy-Bi-Wire low clock pulse length | 2.2 V, 3 V | 0.025 | | 15 | μs |
| $t_{SBW,En}$ | Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) ⁽¹⁾ | 2.2 V/3 V | | | 1 | μs |
| $t_{SBW,Rst}$ | Spy-Bi-Wire return to normal operation time | | 15 | | 100 | μs |
| f_{TCK} | TCK input frequency for 4-wire JTAG ⁽²⁾ | 2.2 V | 0 | | 5 | MHz |
| | | 3 V | 0 | | 10 | MHz |
| $R_{internal}$ | Internal pulldown resistance on TEST | 2.2 V, 3 V | 45 | 60 | 80 | k Ω |

- (1) Tools accessing the Spy-Bi-Wire interface need to wait for the minimum $t_{SBW,En}$ time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.
- (2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

INPUT/OUTPUT SCHEMATICS

Port P1, P1.0 Through P1.3 Input/Output With Schmitt Trigger (MSP430F677xIPEU Only)

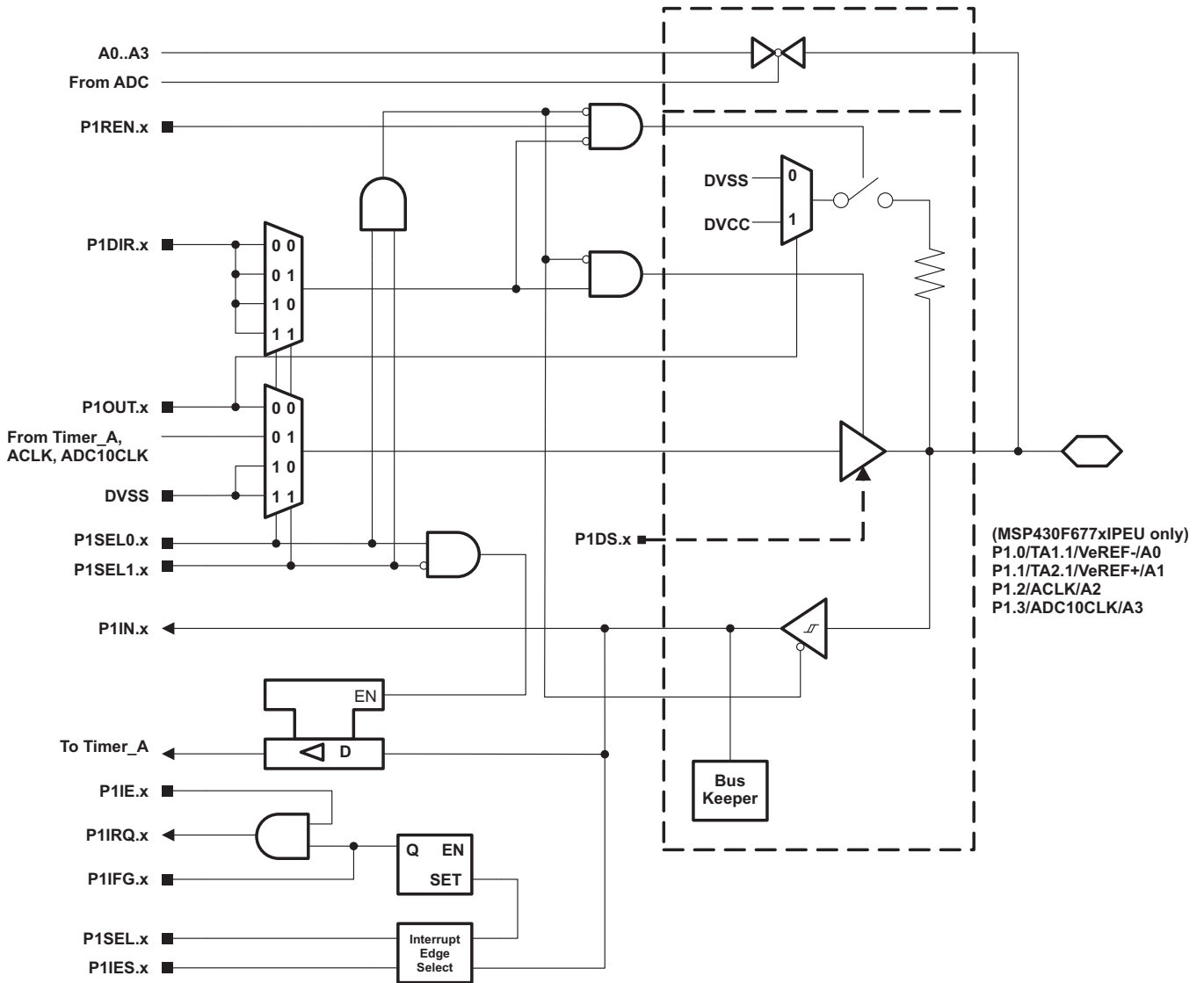


Table 68. Port P1 (P1.0 Through P1.3) Pin Functions (MSP430F677x1PEU Only)

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|----------------------|---|------------|--|----------|----------|
| | | | P1DIR.x | P1SEL1.x | P1SEL0.x |
| P1.0/TA1.1/VeREF-/A0 | 0 | P1.0 (I/O) | I:0; O:1 | 0 | 0 |
| | | TA1.CCI1A | 0 | 0 | 1 |
| | | TA1.1 | 1 | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | VeREF-/A0 | X | 1 | 1 |
| P1.1/TA2.1/VeREF+/A1 | 1 | P1.1 (I/O) | I:0; O:1 | 0 | 0 |
| | | TA2.CCI1A | 0 | 0 | 1 |
| | | TA2.1 | 1 | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | VeREF+/A1 | X | 1 | 1 |
| P1.2/ACLK/A2 | 2 | P1.2 (I/O) | I:0; O:1 | 0 | 0 |
| | | ACLK | 1 | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | A2 | X | 1 | 1 |
| P1.3/ADC10CLK/A3 | 3 | P1.3 (I/O) | I:0; O:1 | 0 | 0 |
| | | ADC10CLK | 1 | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | A3 | X | 1 | 1 |

(1) X = don't care

Port P1, P1.0 Through P1.3 Input/Output With Schmitt Trigger (MSP430F677xIPZ Only)

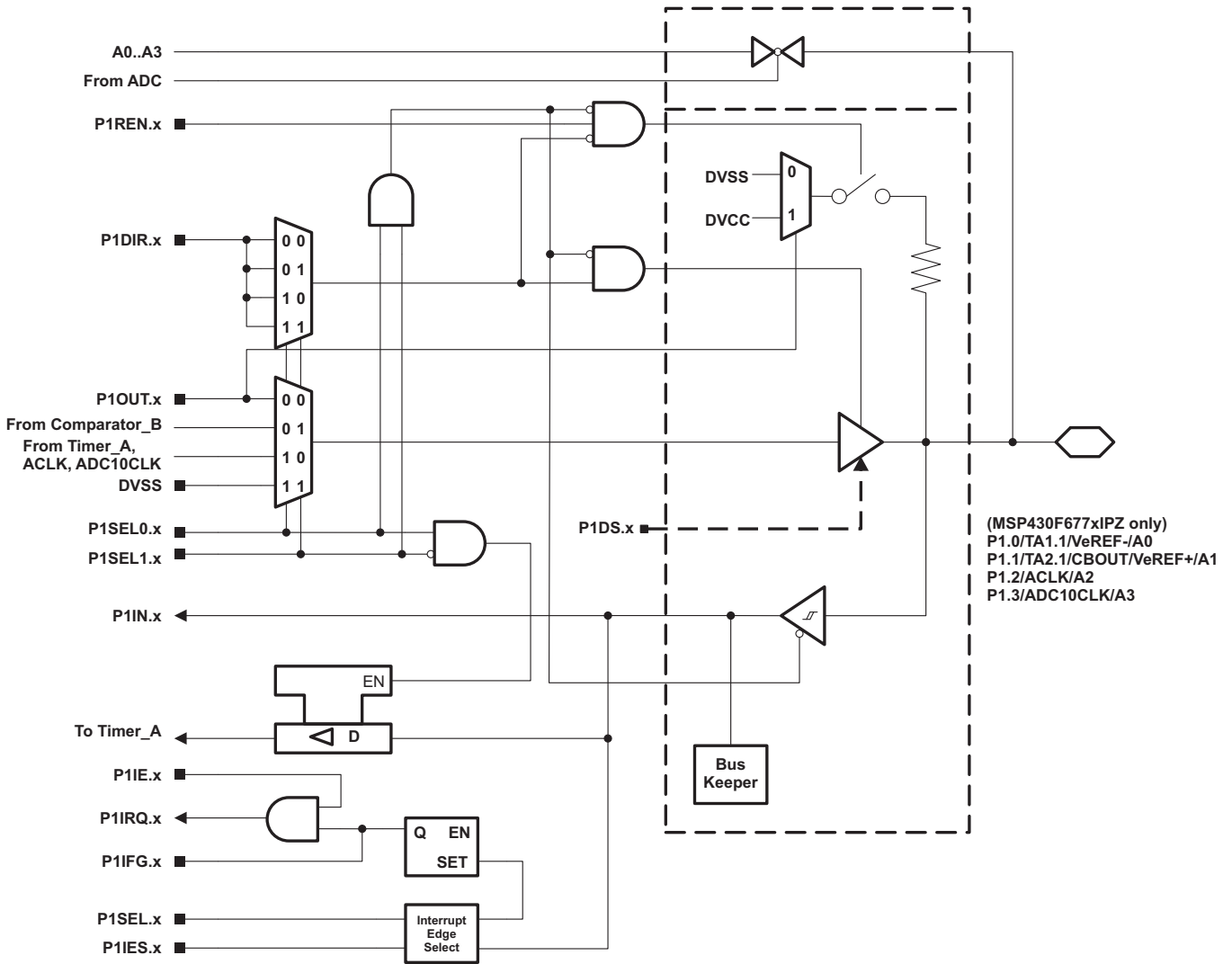


Table 69. Port P1 (P1.0, P1.1, P1.2, and P1.3) Pin Functions (MSP430F677xIPZ Only)

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|----------------------------|---|------------|--|----------|----------|
| | | | P1DIR.x | P1SEL1.x | P1SEL0.x |
| P1.0/TA1.1/VeREF-/A0 | 0 | P1.0 (I/O) | I:0; O:1 | 0 | 0 |
| | | TA1.CCI1A | 0 | 0 | 1 |
| | | TA1.1 | 1 | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | VeREF-/A0 | X | 1 | 1 |
| P1.1/TA2.1/CBOUT/VeREF+/A1 | 1 | P1.1 (I/O) | I:0; O:1 | 0 | 0 |
| | | TA2.CCI1A | 0 | 0 | 1 |
| | | TA2.1 | 1 | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | CBOUT | 1 | 1 | 0 |
| | | VeREF+/A1 | X | 1 | 1 |
| P1.2/ACLK/A2 | 2 | P1.2 (I/O) | I:0; O:1 | 0 | 0 |
| | | ACLK | 1 | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | A2 | X | 1 | 1 |
| P1.3/ADC10CLK/A3 | 3 | P1.3 (I/O) | I:0; O:1 | 0 | 0 |
| | | ADC10CLK | 1 | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | A3 | X | 1 | 1 |

(1) X = don't care

Port P1, P1.4 and P1.5 Input/Output With Schmitt Trigger (MSP430F677xIPEU and MSP430F677xIPZ)

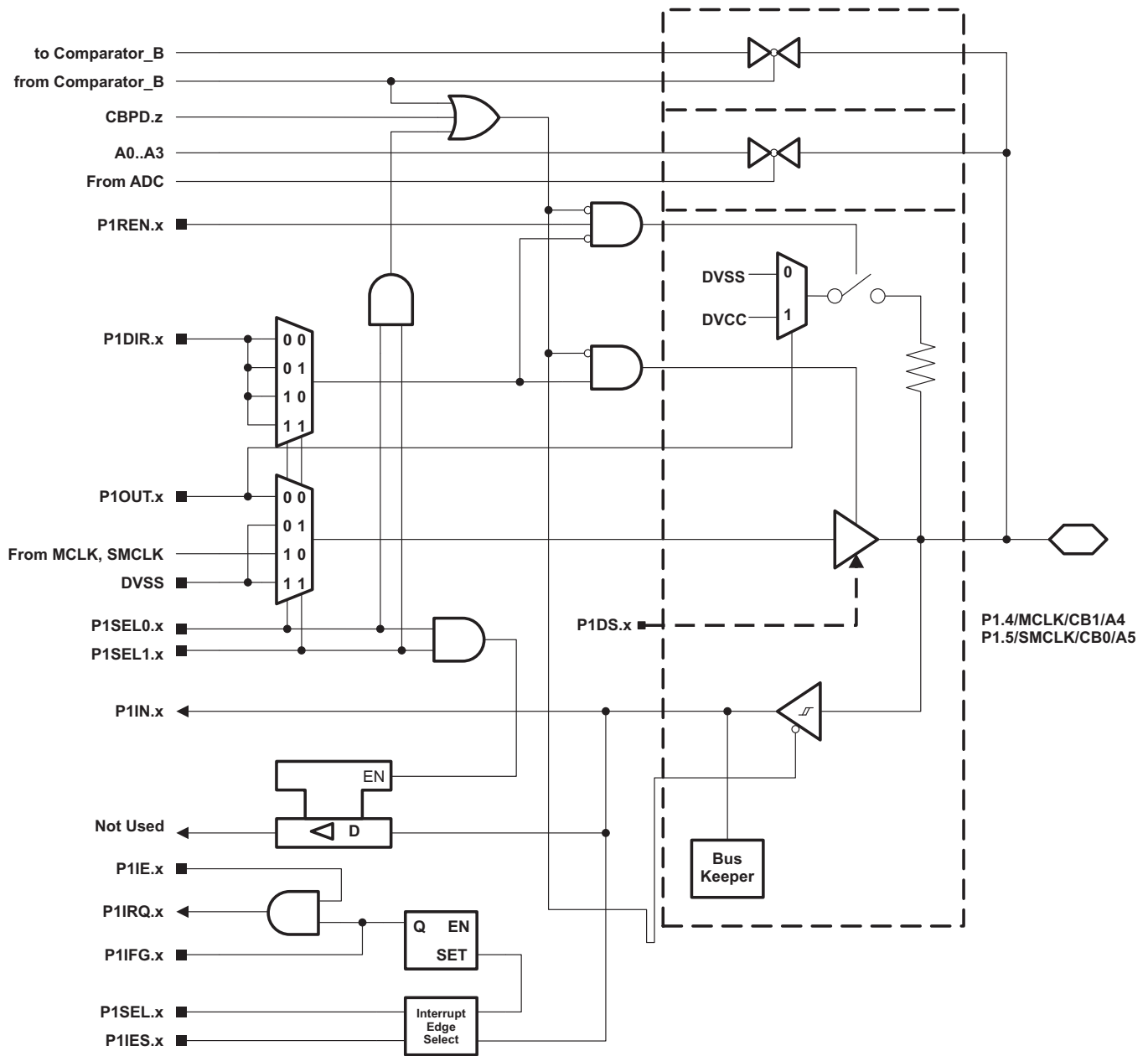


Table 70. Port P1 (P1.4 and P1.5) Pin Functions (MSP430F677xIPEU and MSP430F677xIPZ)

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | | |
|-------------------|---|------------|--|----------|----------|-----------|
| | | | P1DIR.x | P1SEL1.x | P1SEL0.x | CPBD.z |
| P1.4/MCLK/CB1/A4 | 4 | P1.4 (I/O) | I:0; O:1 | 0 | 0 | 0 |
| | | MCLK | 1 | 0 | 1 | 0 |
| | | N/A | 0 | 1 | 0 | 0 |
| | | DVSS | 1 | 1 | 0 | 0 |
| | | A4 | X | 1 | 1 | 0 |
| | | CB1 | X | X | X | 1 (z = 1) |
| P1.5/SMCLK/CB0/A5 | 5 | P1.5 (I/O) | I:0; O:1 | 0 | 0 | 0 |
| | | SMCLK | 1 | 0 | 1 | 0 |
| | | N/A | 0 | 1 | 0 | 0 |
| | | DVSS | 1 | 1 | 0 | 0 |
| | | A5 | X | 1 | 1 | 0 |
| | | CB0 | X | X | X | 1 (z = 0) |

(1) X = don't care

Port P1, P1.6 and P1.7 Input/Output With Schmitt Trigger (MSP430F677xIPEU and MSP430F677xIPZ)

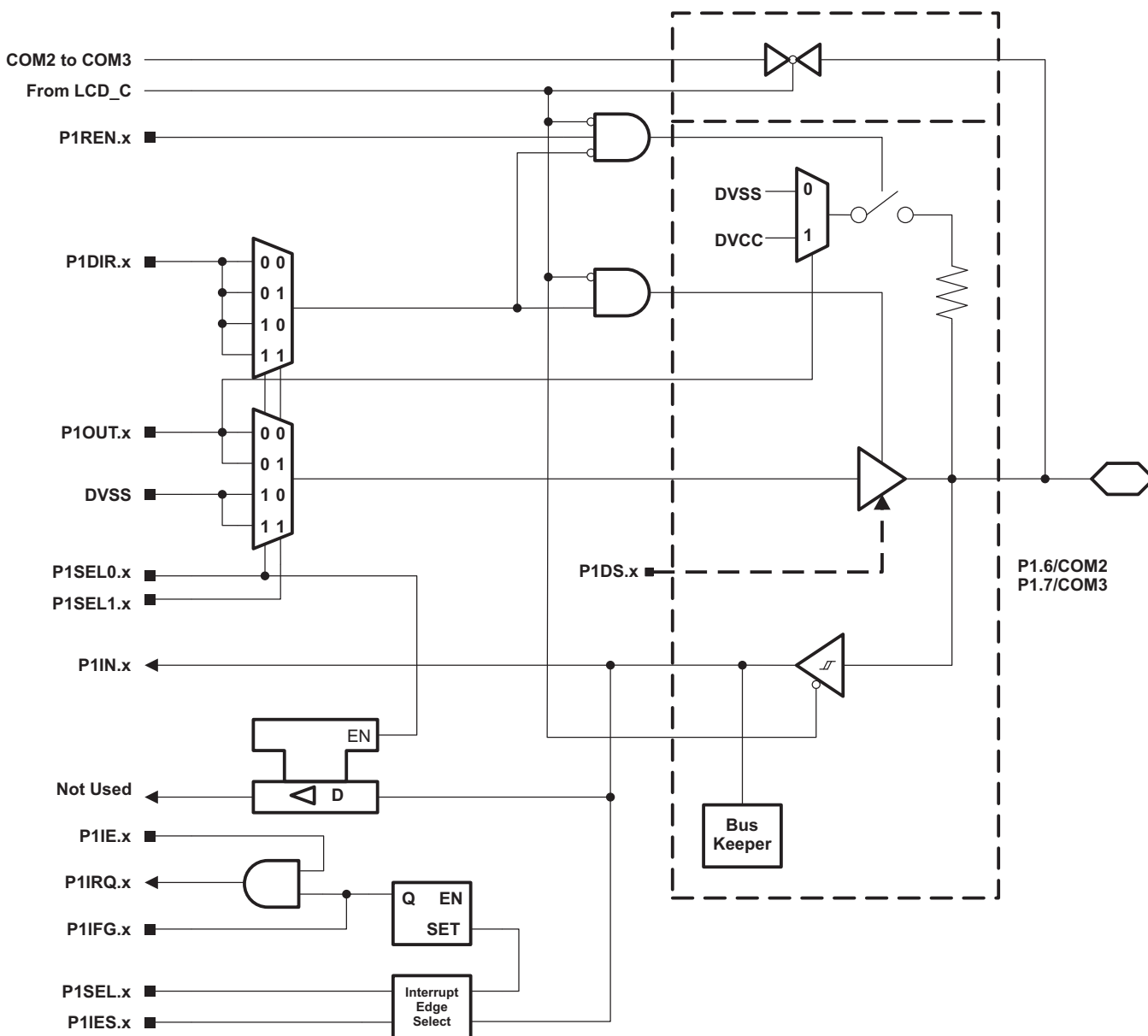


Table 71. Port P1 (P1.6 and P1.7) Pin Functions (MSP430F677xIPEU and MSP430F677xIPZ)

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | | |
|-----------------|---|------------|--|----------|----------|------------|
| | | | P1DIR.x | P1SEL1.x | P1SEL0.x | COM Enable |
| P1.6/COM2 | 6 | P1.6 (I/O) | I:0; O:1 | X | 0 | 0 |
| | | N/A | 0 | X | 1 | 0 |
| | | DVSS | 1 | X | 1 | 0 |
| | | COM2 | X | X | X | 1 |
| P1.7/COM3 | 7 | P1.7 (I/O) | I:0; O:1 | X | 0 | 0 |
| | | N/A | 0 | X | 1 | 0 |
| | | DVSS | 1 | X | 1 | 0 |
| | | COM3 | X | X | X | 1 |

(1) X = don't care

Port P2, P2.0 Through P2.7, Input/Output With Schmitt Trigger (MSP430F677x1PEU Only)

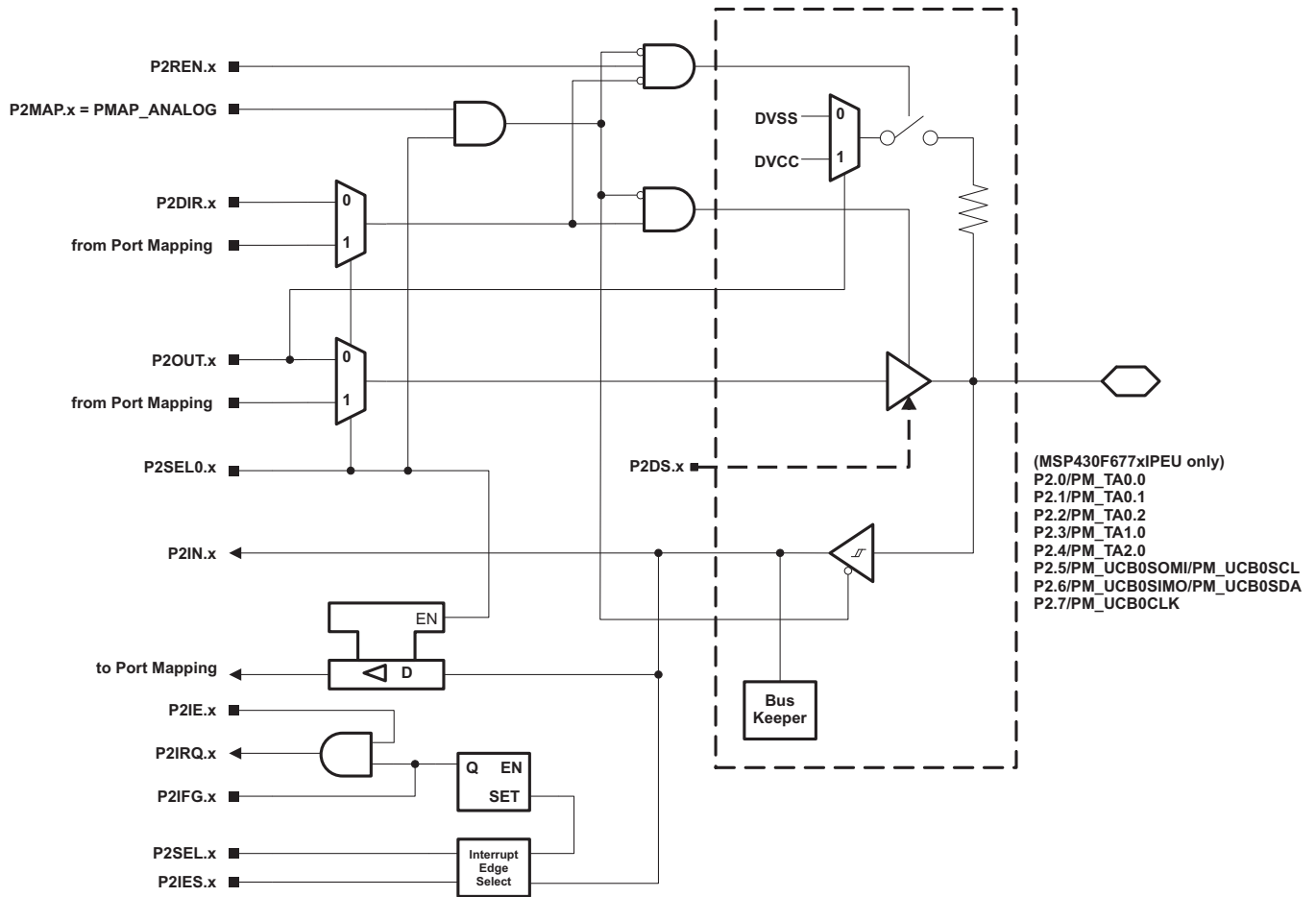


Table 72. Port P2 (P2.0 Through P2.7) Pin Functions (MSP430F677x1PEU Only)

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|---------------------------------|---|--|--|----------|---------|
| | | | P2DIR.x | P2SEL0.x | P2MAP.x |
| P2.0/PM_TA0.0 | 0 | P2.0 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped Secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P2.1/PM_TA0.1 | 1 | P2.1 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped Secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P2.2/PM_TA0.2 | 2 | P2.2 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped Secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P2.3/PM_TA1.0 | 3 | P2.3 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped Secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P2.4/PM_TA2.0 | 4 | P2.4 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped Secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P2.5/PM_UCB0SOMI/ PM_UCB0SCL | 5 | P2.5 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped Secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P2.6/PM_UCB0SIMO/ PM_UCB0SDA | 6 | P2.6 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped Secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P2.7/PM_UCB0CLK | 7 | P2.7 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped Secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |

(1) X = don't care

Port P2, P2.0 Through P2.3, Input/Output With Schmitt Trigger (MSP430F677xIPZ Only)

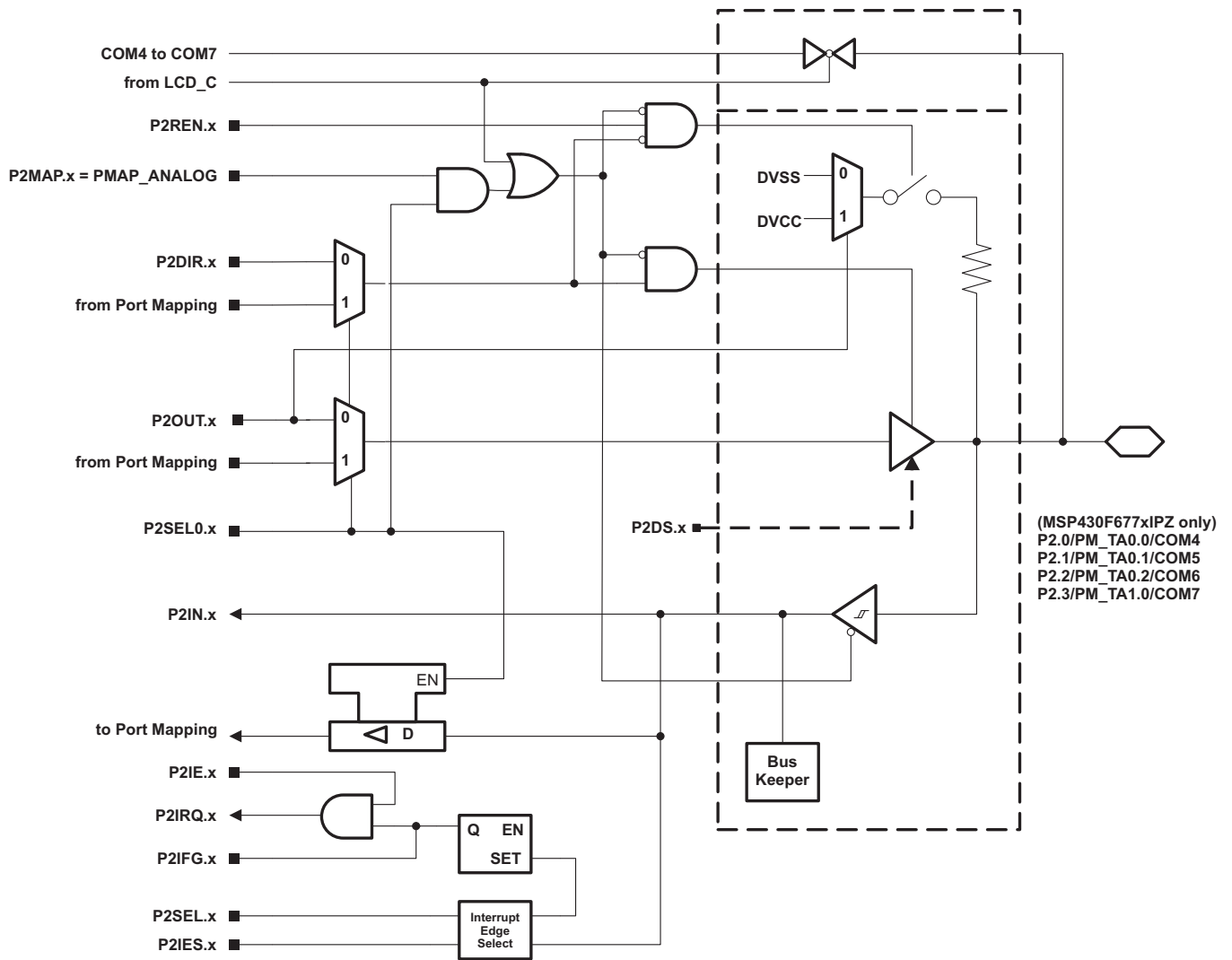


Table 73. Port P2 (P2.0 Through P2.3) Pin Functions (MSP430F677xIPZ Only)

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | | |
|------------------------|---|--|--|----------|---------|------------|
| | | | P2DIR.x | P2SEL0.x | P2MAP.x | COM Enable |
| P2.0/PM_TA0.0/ COM4 | 0 | P2.0 (I/O) | I:0; O:1 | 0 | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 30 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | COM4 | X | X | X | 1 |
| P2.1/PM_TA0.1/ COM5 | 1 | P2.1 (I/O) | I:0; O:1 | 0 | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 30 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | COM5 | X | X | X | 1 |
| P2.2/PM_TA0.2/ COM6 | 2 | P2.2 (I/O) | I:0; O:1 | 0 | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 30 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | COM6 | X | X | X | 1 |
| P2.3/PM_TA1.0/ COM7 | 3 | P2.3 (I/O) | I:0; O:1 | 0 | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 30 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | COM7 | X | X | X | 1 |

(1) X = don't care

Port P2, P2.4 Through P2.6, Input/Output With Schmitt Trigger (MSP430F677xIPZ Only)

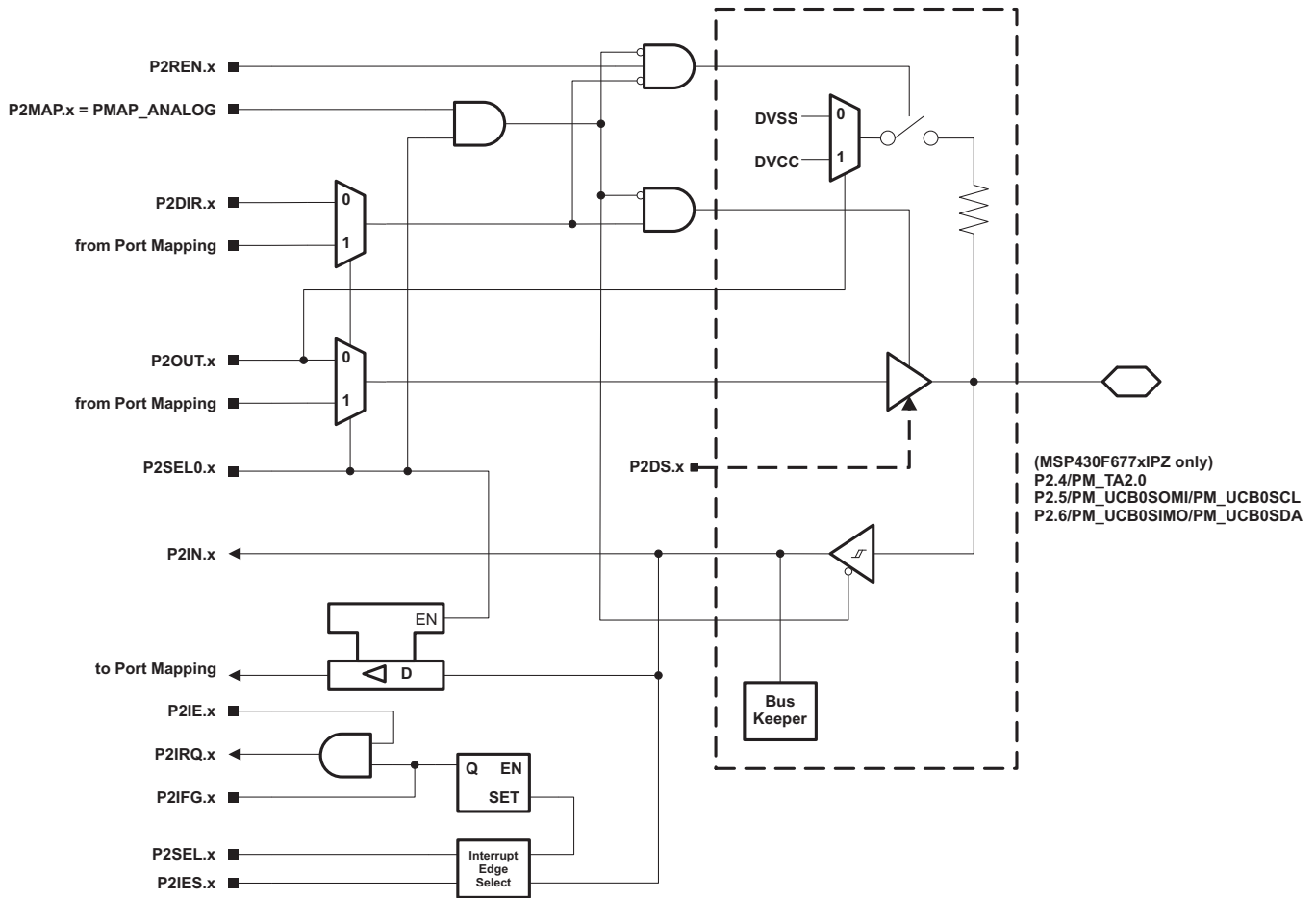


Table 74. Port P2 (P2.4 and P2.6) Pin Functions (MSP430F677xIPZ Only)

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|---------------------------------|---|-----------------------------------|--|----------|---------|
| | | | P2DIR.x | P2SEL0.x | P2MAP.x |
| P2.4/PM_TA2.0/R23 | 4 | P2.4 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped secondary digital function | X | 1 | ≤ 30 |
| | | R23 | X | 1 | = 31 |
| P2.5/PM_UCB0SOMI/PM_UCB0SCL/R13 | 5 | P2.5 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped secondary digital function | X | 1 | ≤ 30 |
| | | R13 | X | 1 | = 31 |
| P2.6/PM_UCB0SIMO/PM_UCB0SDA/R03 | 6 | P2.6 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped secondary digital function | X | 1 | ≤ 30 |
| | | R03 | X | 1 | = 31 |

(1) X = don't care

Port P2, P2.7, Input/Output With Schmitt Trigger (MSP430F677xIPZ Only)

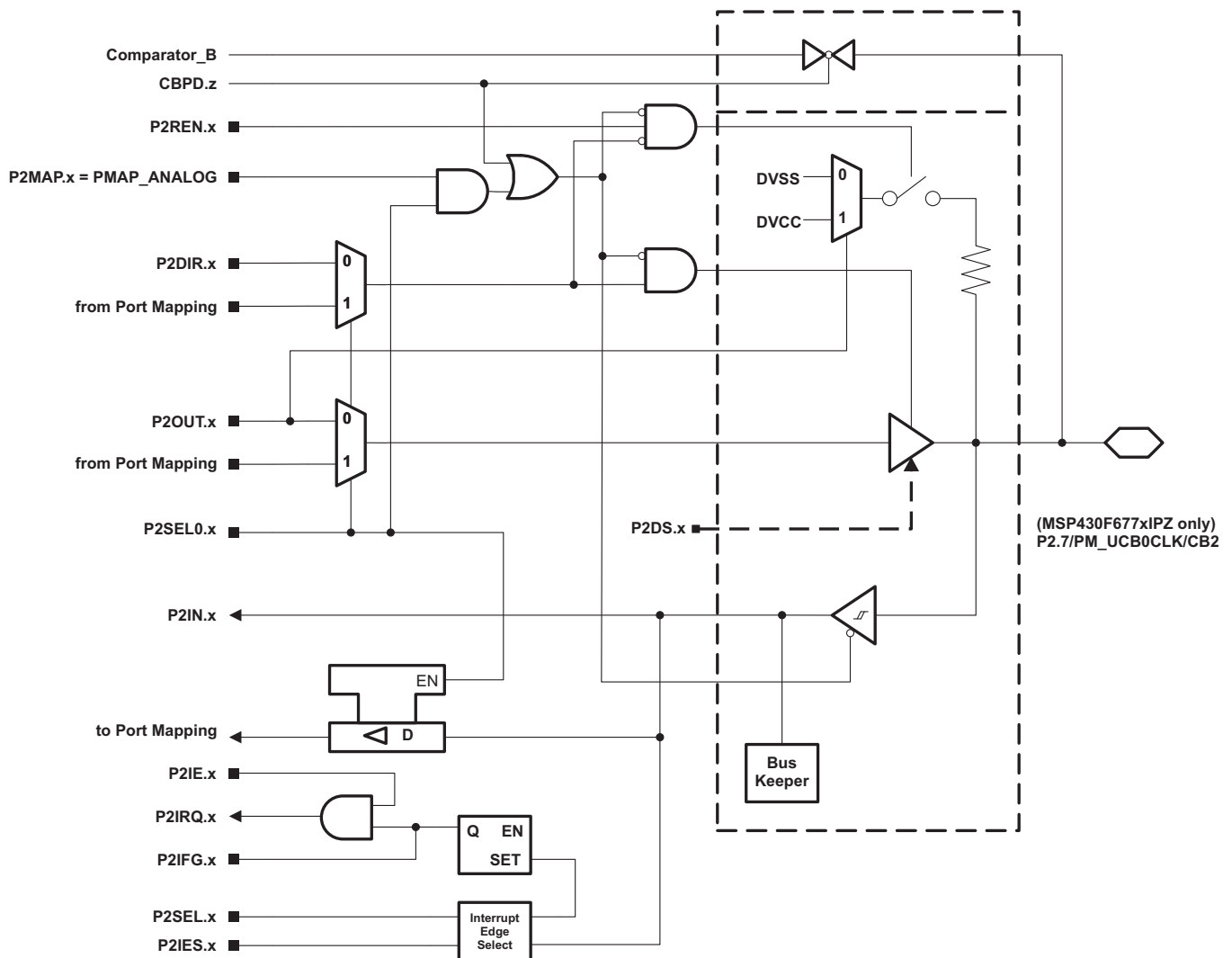


Table 75. Port P2 (P2.7) Pin Functions (MSP430F677xIPZ Only)

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | | |
|-------------------------|---|--|--|----------|---------|-----------|
| | | | P2DIR.x | P2SEL0.x | P2MAP.x | CBPD.z |
| P2.7/PM_UCB0CLK/ CB2 | 7 | P2.7 (I/O) | I:0; O:1 | 0 | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 30 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | CB2 | X | X | X | 1 (z = 2) |

(1) X = don't care

Port P3, P3.0 Through P3.7, Input/Output With Schmitt Trigger (MSP430F677xIPEU Only)

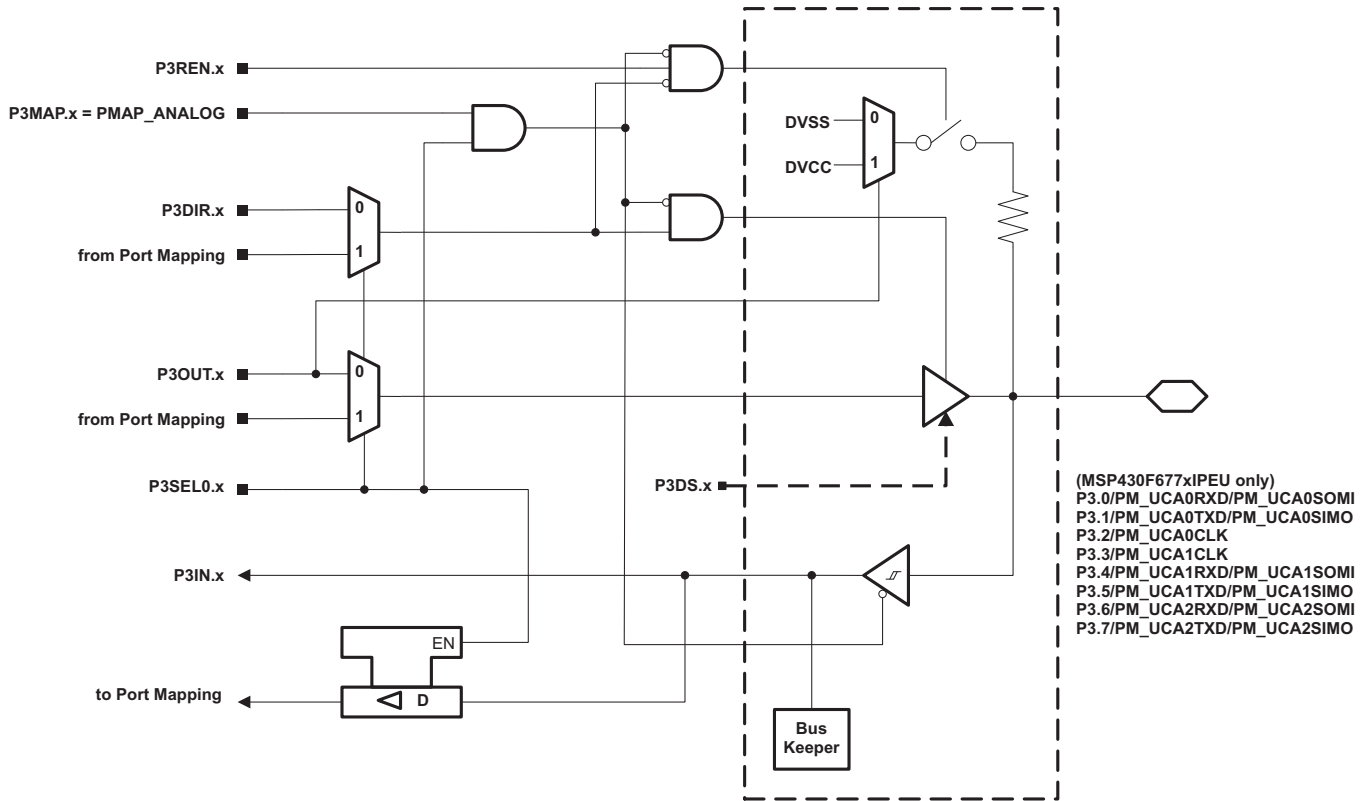


Table 76. Ports P3 (P3.0 Through P3.7) Pin Functions (MSP430F677xIPEU Only)

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|---------------------------------|---|--|--|----------|---------|
| | | | P3DIR.x | P3SEL0.x | P3MAP.x |
| P3.0/PM_UCA0RXD/ PM_UCA0SOMI | 0 | P3.0 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped Secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P3.1/PM_UCA0TXD/ PM_UCA0SIMO | 1 | P3.1 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped Secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P3.2/PM_UCA0CLK | 2 | P3.2 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped Secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P3.3/PM_UCA1CLK | 3 | P3.3 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped Secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P3.4/PM_UCA1RXD/ PM_UCA1SOMI | 4 | P3.4 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped Secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P3.5/PM_UCA1TXD/ PM_UCA1SIMO | 5 | P3.5 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped Secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P3.6/PM_UCA2RXD/ PM_UCA2SOMI | 6 | P3.6 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped Secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P3.7/PM_UCA2TXD/ PM_UCA2SIMO | 7 | P3.7 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped Secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |

(1) X = don't care

Port P3, P3.0, Input/Output With Schmitt Trigger (MSP430F677xIPZ Only)

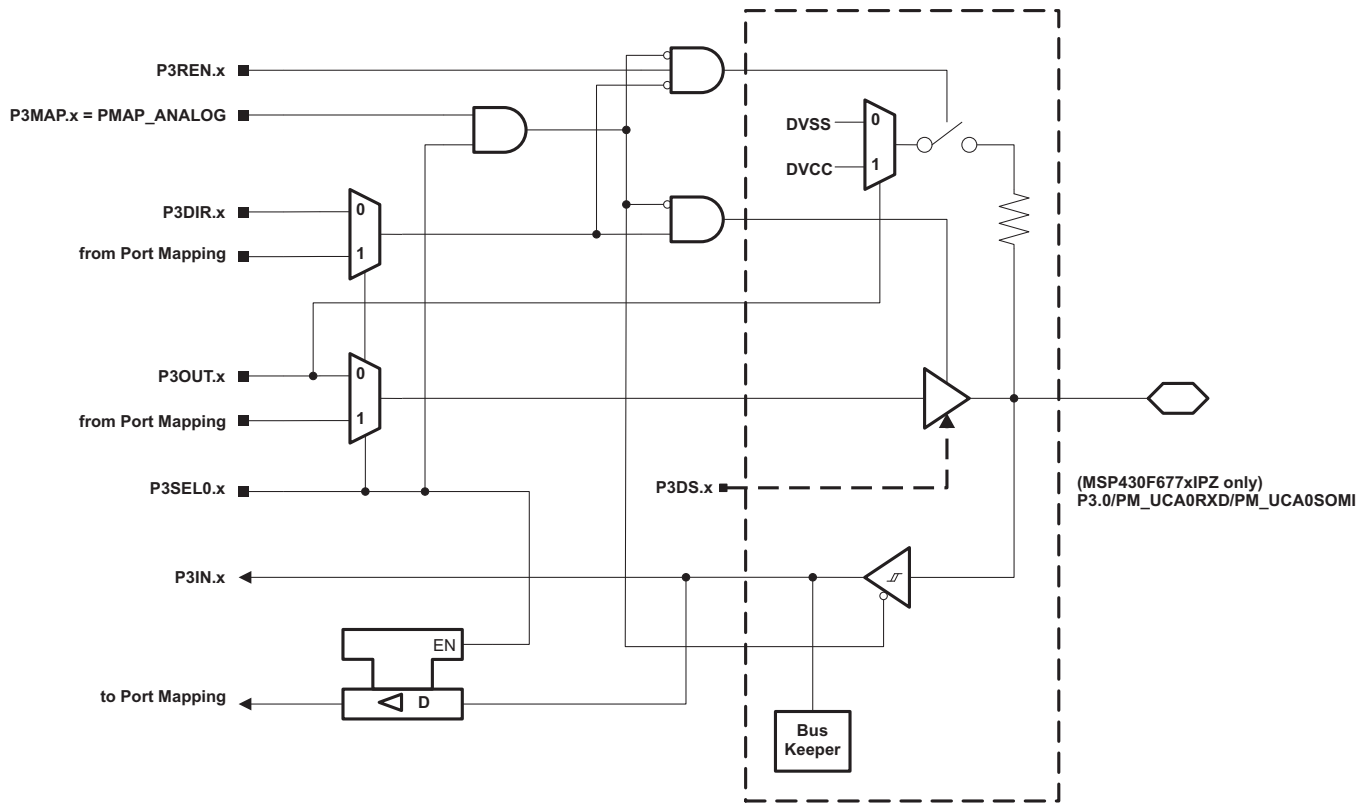


Table 77. Ports P3 (P3.0) Pin Functions (MSP430F677xIPZ Only)

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|---------------------------------|---|--|--|----------|---------|
| | | | P3DIR.x | P3SEL0.x | P3MAP.x |
| P3.0/PM_UCA0RXD/ PM_UCA0SOMI | 0 | P3.0 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped Secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |

(1) X = don't care

Port P3, P3.1 Through P3.7, Input/Output With Schmitt Trigger (MSP430F677xIPZ Only)

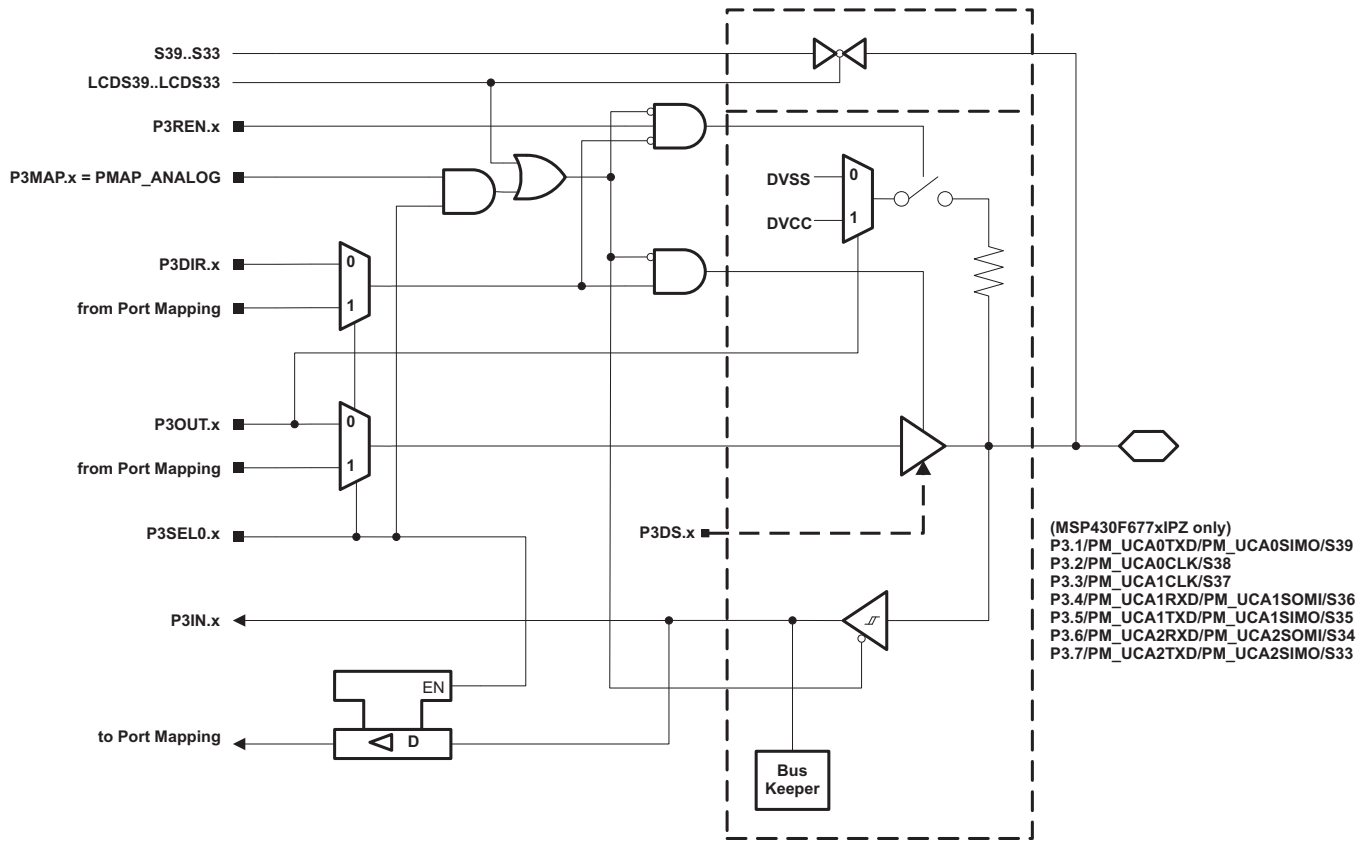


Table 78. Ports P3 (P3.1 Through P3.7) Pin Functions (MSP430F677xIPZ Only)

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | | |
|---|---|--|--|----------|---------|-----------|
| | | | P3DIR.x | P3SEL0.x | P3MAP.x | LCD39..33 |
| P3.1/PM_UCA0TXD/ PM_UCA0SIMO/S39 | 1 | P3.1 (I/O) | I:0; O:1 | 0 | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 30 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S39 | X | X | X | 1 |
| P3.2/PM_UCA0CLK/ S38 | 2 | P3.2 (I/O) | I:0; O:1 | 0 | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 30 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S38 | X | X | X | 1 |
| P3.3/PM_UCA1CLK/ S37 | 3 | P3.3 (I/O) | I:0; O:1 | 0 | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 30 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S37 | X | X | X | 1 |
| P3.4/PM_UCA1RXD / PM_UCA1SOMI/S36 | 4 | P3.4 (I/O) | I:0; O:1 | 0 | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 30 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S36 | X | X | X | 1 |
| P3.5/PM_UCA1TXD/ PM_UCA1SIMO/S35 | 5 | P3.5 (I/O) | I:0; O:1 | 0 | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 30 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S35 | X | X | X | 1 |
| P3.6/PM_UCA2RXD / PM_UCA2SOMI/S34 | 6 | P3.6 (I/O) | I:0; O:1 | 0 | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 30 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S34 | X | X | X | 1 |
| P3.7/PM_UCA2TXD/ PM_UCA2SIMO/S33 | 7 | P3.7 (I/O) | I:0; O:1 | 0 | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 30 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S33 | X | X | X | 1 |

(1) X = don't care

Port P4, P4.0 Through P4.7, Input/Output With Schmitt Trigger (MSP430F677x1PEU Only)

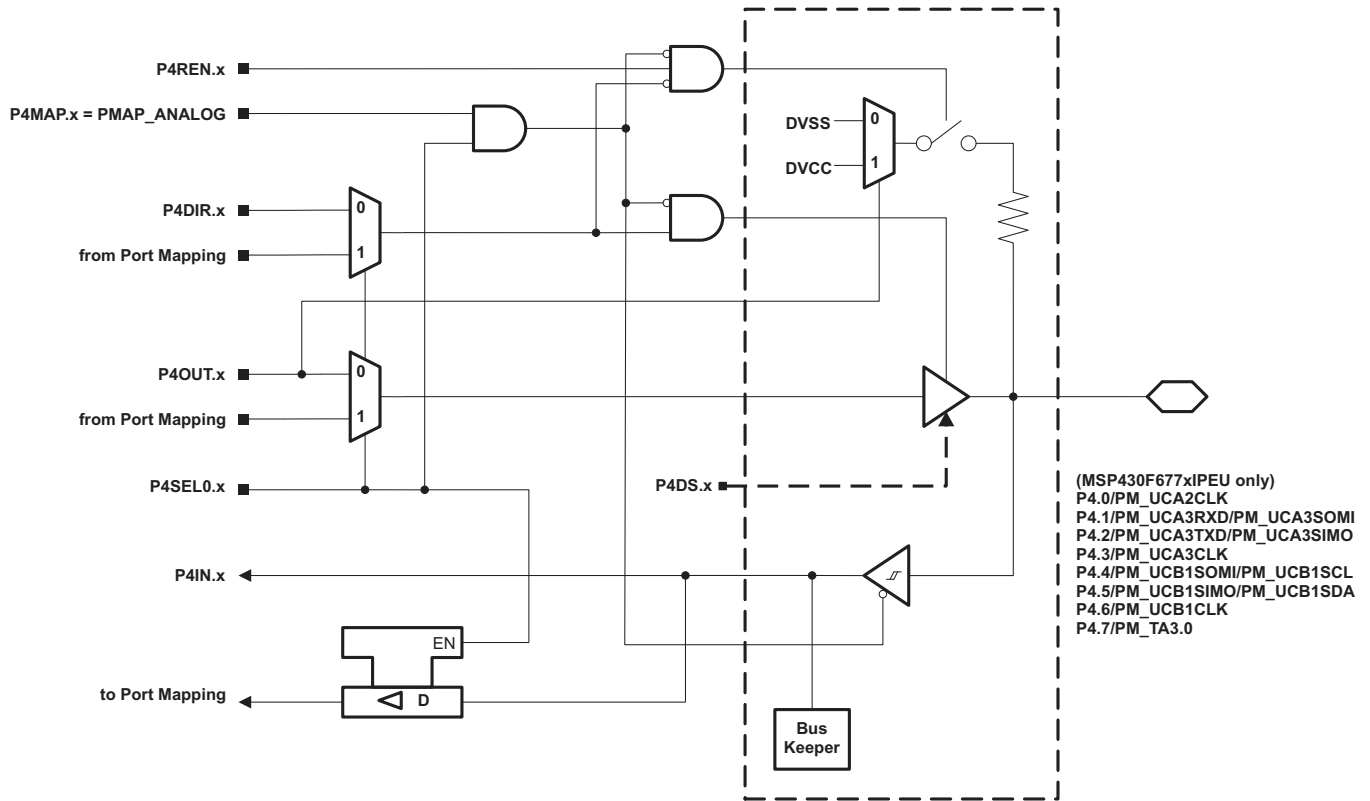


Table 79. Port P4 (P4.0 Through P4.7) Pin Functions (MSP430F677x1PEU Only)

| PIN NAME (P4.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|---------------------------------|---|--|--|----------|---------|
| | | | P4DIR.x | P4SEL0.x | P4MAP.x |
| P4.0/PM_UCA2CLK | 0 | P4.0 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped Secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P4.1/PM_UCA3RXD/ PM_UCA3SOMI | 1 | P4.1 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped Secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P4.2/PM_UCA3TXD/ PM_UCA3SIMO | 2 | P4.2 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped Secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P4.3/PM_UCA3CLK | 3 | P4.3 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped Secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P4.4/PM_UCB1SOMI/ PM_UCB1SCL | 4 | P4.4 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped Secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P4.5/PM_UCB1SIMO/ PM_UCB1SDA | 5 | P4.5 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped Secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P4.6/PM_UCB1CLK | 6 | P4.6 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped Secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P4.7/PM_TA3.0 | 7 | P4.7 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped Secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |

(1) X = don't care

Port P4, P4.0 Through P4.7, Input/Output With Schmitt Trigger (MSP430F677xIPZ Only)

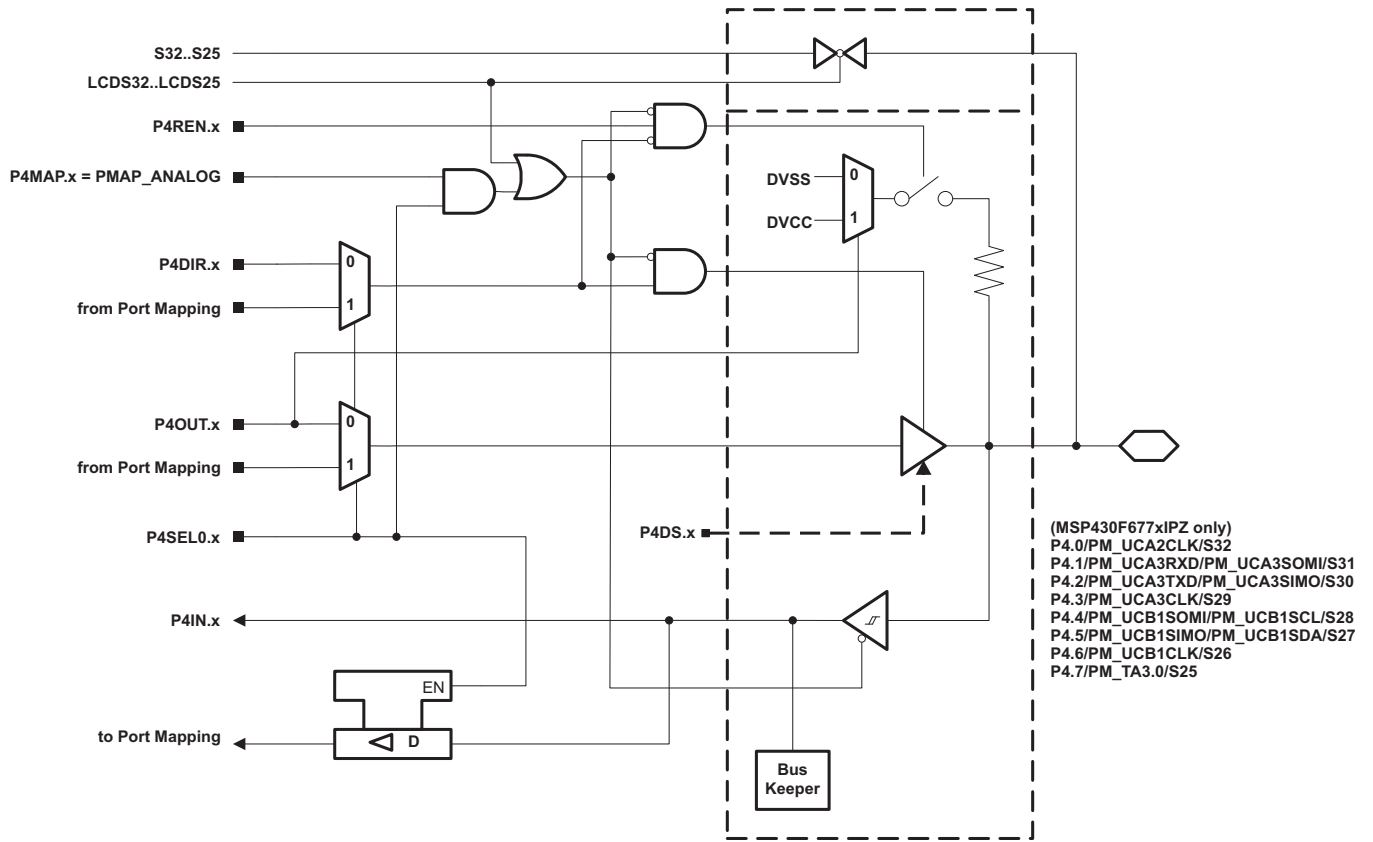


Table 80. Port P4 (P4.0 Through P4.7) Pin Functions (MSP430F677xIPZ Only)

| PIN NAME (P4.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | | |
|---|---|--|--|----------|---------|-----------|
| | | | P4DIR.x | P4SEL0.x | P4MAP.x | LCD32..25 |
| P4.0/PM_UCA2CLK/ S32 | 0 | P4.0 (I/O) | I:0; O:1 | 0 | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 30 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S32 | X | X | X | 1 |
| P4.1/PM_UCA3RXD / PM_UCA3SOMI/S31 | 1 | P4.1 (I/O) | I:0; O:1 | 0 | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 30 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S31 | X | X | X | 1 |
| P4.2/PM_UCA3TXD/ PM_UCA3SIMO/S30 | 2 | P4.2 (I/O) | I:0; O:1 | 0 | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 30 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S30 | X | X | X | 1 |
| P4.3/PM_UCA3CLK/ S29 | 3 | P4.3 (I/O) | I:0; O:1 | 0 | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 30 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S29 | X | X | X | 1 |
| P4.4/ PM_UCB1SOMI/ PM_UCB1SCL/S28 | 4 | P4.4 (I/O) | I:0; O:1 | 0 | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 30 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S28 | X | X | X | 1 |
| P4.5/ PM_UCB1SIMO/ PM_UCB1SDA/S27 | 5 | P4.5 (I/O) | I:0; O:1 | 0 | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 30 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S27 | X | X | X | 1 |
| P4.6/PM_UCB1CLK/ S26 | 6 | P4.6 (I/O) | I:0; O:1 | 0 | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 30 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S26 | X | X | X | 1 |
| P4.7/PM_TA3.0/S25 | 7 | P4.7 (I/O) | I:0; O:1 | 0 | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 30 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S25 | X | X | X | 1 |

(1) X = don't care

Port P5, P5.0 Through P5.3, Input/Output With Schmitt Trigger (MSP430F677xIPEU Only)

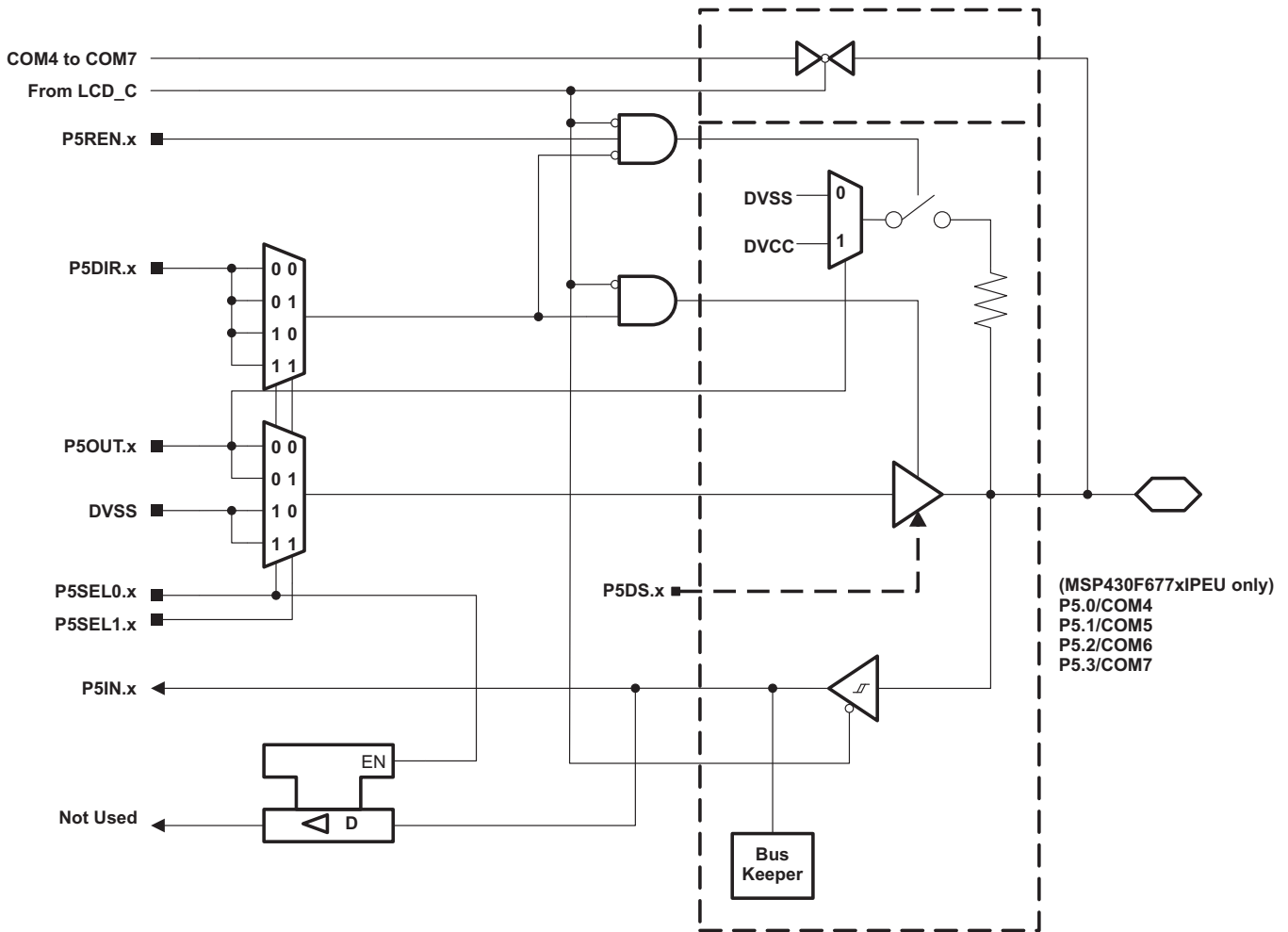


Table 81. Port P5 (P5.0 Through P5.3) Pin Functions (MSP430F677x1PEU Only)

| PIN NAME (P5.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | | |
|-----------------|---|------------|--|----------|----------|------------|
| | | | P5DIR.x | P5SEL1.x | P5SEL0.x | COM Enable |
| P5.0/COM4 | 0 | P5.0 (I/O) | I:0; O:1 | X | 0 | 0 |
| | | N/A | 0 | X | 1 | 0 |
| | | DVSS | 1 | X | 1 | 0 |
| | | COM4 | X | X | X | 1 |
| P5.1/COM5 | 1 | P5.1 (I/O) | I:0; O:1 | X | 0 | 0 |
| | | N/A | 0 | X | 1 | 0 |
| | | DVSS | 1 | X | 1 | 0 |
| | | COM5 | X | X | X | 1 |
| P5.2/COM6 | 2 | P5.2 (I/O) | I:0; O:1 | X | 0 | 0 |
| | | N/A | 0 | X | 1 | 0 |
| | | DVSS | 1 | X | 1 | 0 |
| | | COM6 | X | X | X | 1 |
| P5.3/COM7 | 3 | P5.3 (I/O) | I:0; O:1 | X | 0 | 0 |
| | | N/A | 0 | X | 1 | 0 |
| | | DVSS | 1 | X | 1 | 0 |
| | | COM7 | X | X | X | 1 |

(1) X = don't care

Port P5, P5.4 Through P5.6, Input/Output With Schmitt Trigger (MSP430F677xIPEU Only)

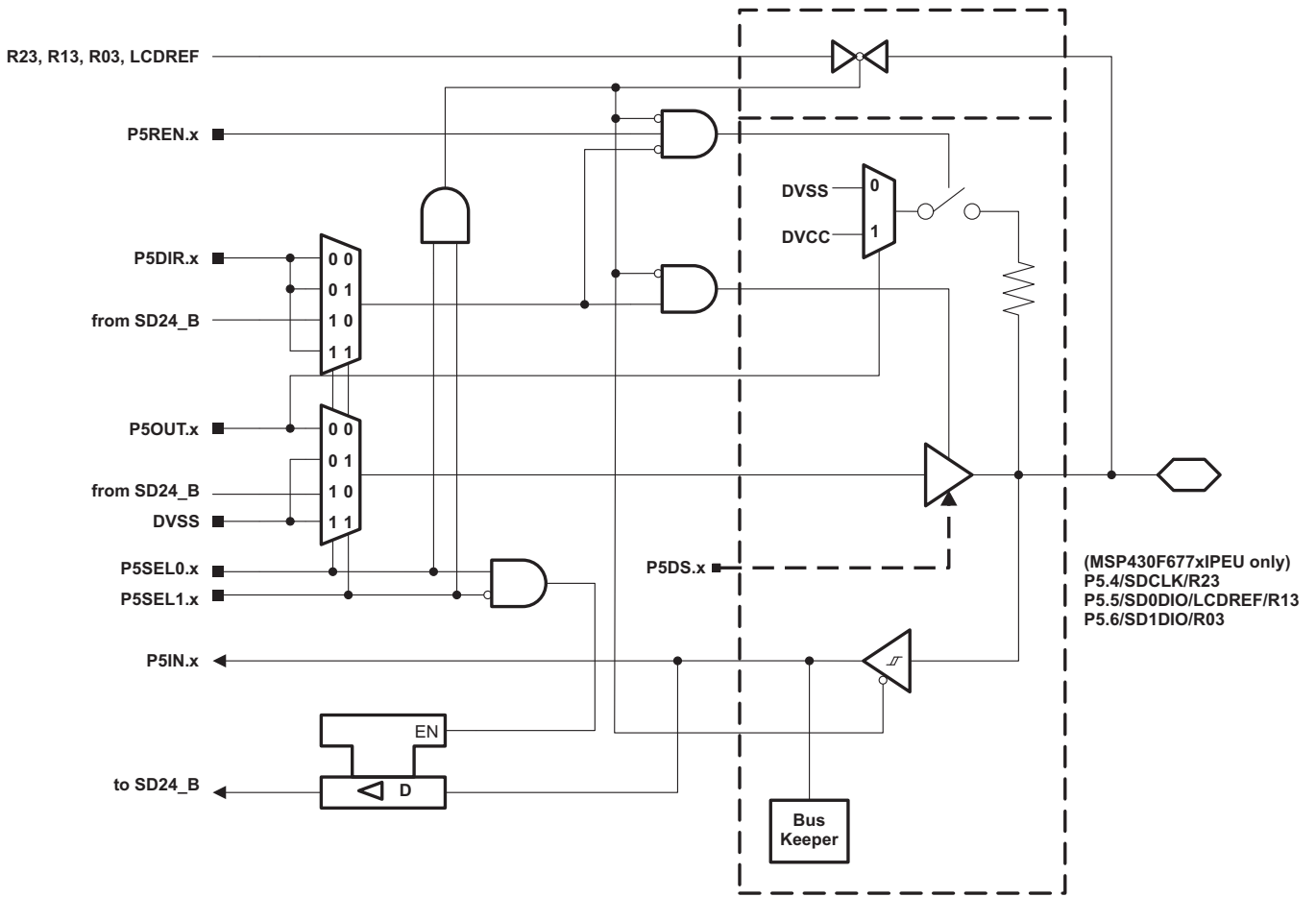


Table 82. Port P5 (P5.4 Through P5.6) Pin Functions (MSP430F677x1PEU Only)

| PIN NAME (P5.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|------------------------|---|----------------------------|--|----------|----------|
| | | | P5DIR.x | P5SEL1.x | P5SEL0.x |
| P5.4/SDCLK/R23 | 4 | P5.4 (I/O) | I:0; O:1 | 0 | 0 |
| | | Secondary digital function | X | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | R23 | X | 1 | 1 |
| P5.5/SD0DIO/LCDREF/R13 | 5 | P5.5 (I/O) | I:0; O:1 | 0 | 0 |
| | | Secondary digital function | X | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | LCDREF/R13 | X | 1 | 1 |
| PT.6/SD1DIO/R03 | 6 | P5.6 (I/O) | I:0; O:1 | 0 | 0 |
| | | Secondary digital function | X | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | R03 | X | 1 | 1 |

(1) X = don't care

Port P5, P5.7, Input/Output With Schmitt Trigger (MSP430F677xIPEU Only)

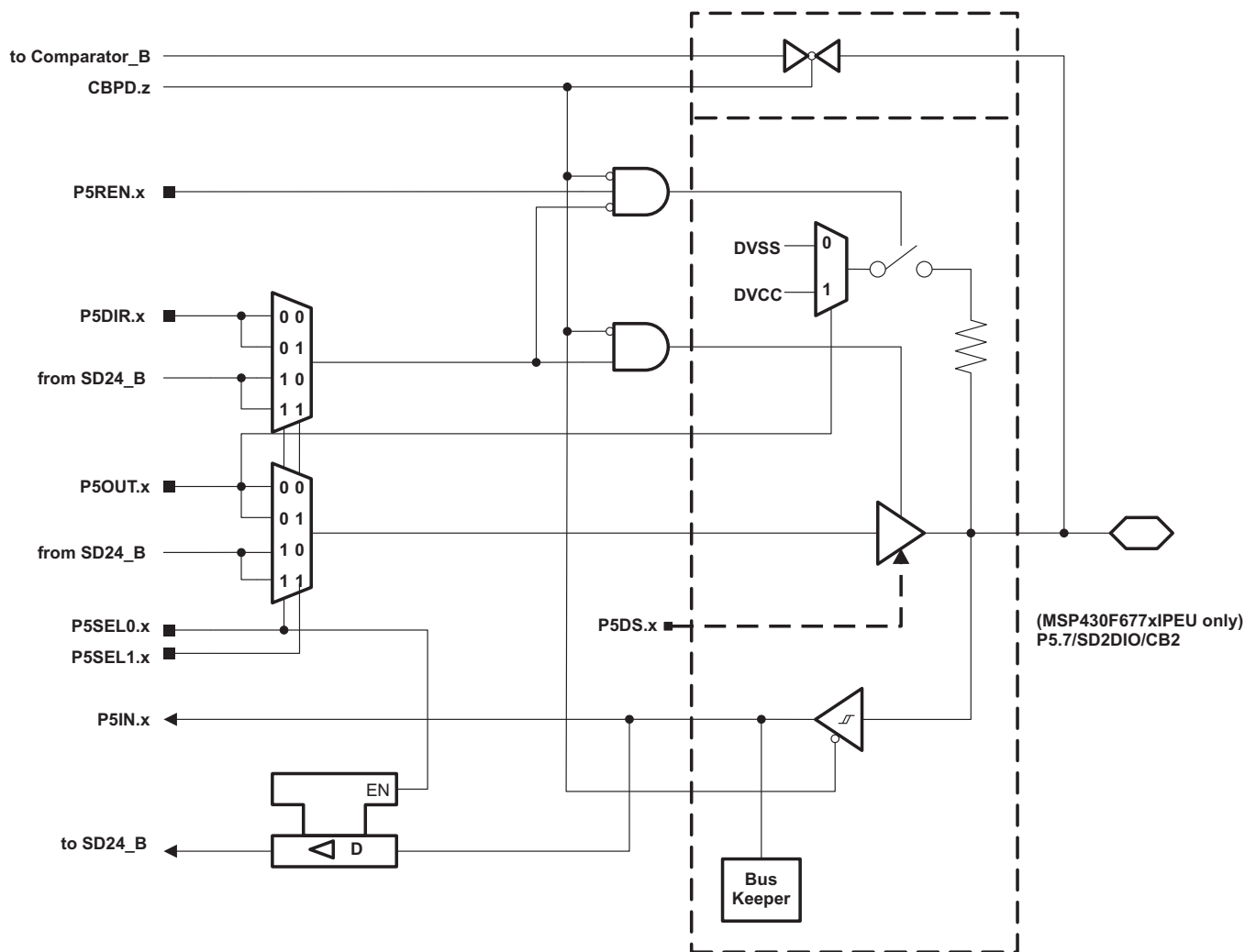


Table 83. Port P5 (P5.7) Pin Function (MSP430F677xIPEU Only)

| PIN NAME (P5.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | | |
|-----------------|---|----------------------------|--|----------|----------|-----------|
| | | | P5DIR.x | P5SEL1.x | P5SEL0.x | CBPD.z |
| P5.7/SD2DIO/CB2 | 7 | P5.7 (I/O) | I:0; O:1 | X | 0 | 0 |
| | 7 | Secondary digital function | X | X | 1 | 0 |
| | 7 | CB2 | X | X | X | 1 (z = 2) |

(1) X = don't care

Port P5, P5.0 Through P5.7, Input/Output With Schmitt Trigger (MSP430F677x1PZ Only)

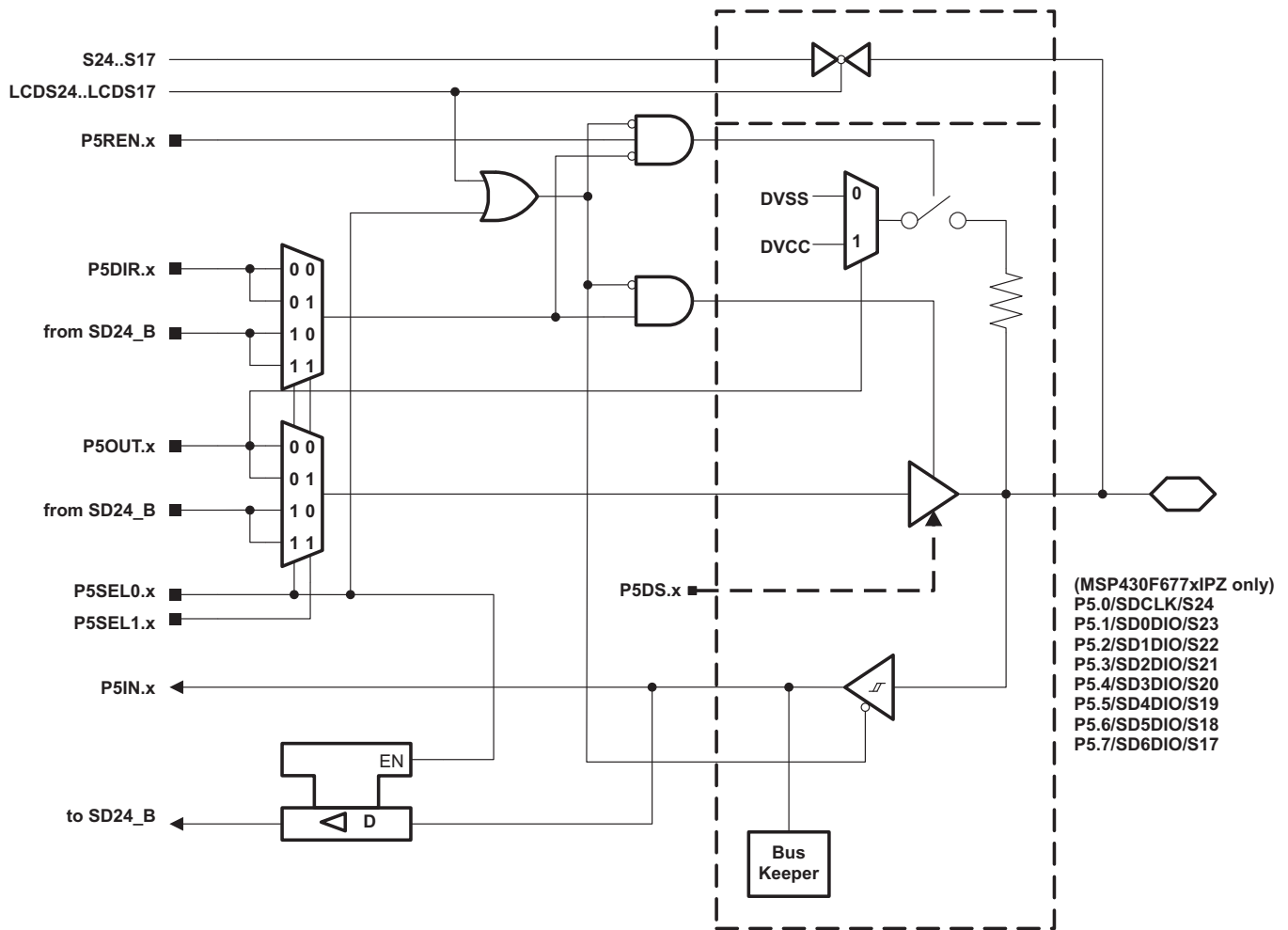


Table 84. Port P5 (P5.0 Through P5.7) Pin Function (MSP430F677xIPZ Only)

| PIN NAME (P5.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | | |
|-----------------|---|----------------------------|--|----------|----------|-----------|
| | | | P5DIR.x | P5SEL1.x | P5SEL0.x | LCD24..17 |
| P5.0/SDCLK/S24 | 0 | P5.0 (I/O) | I:0; O:1 | X | 0 | 0 |
| | | Secondary digital function | X | X | 1 | 0 |
| | | S24 | X | X | X | 1 |
| P5.1/SD0DIO/S23 | 1 | P5.1 (I/O) | I:0; O:1 | X | 0 | 0 |
| | | Secondary digital function | X | X | 1 | 0 |
| | | S23 | X | X | X | 1 |
| P5.2/SD1DIO/S22 | 2 | P5.2 (I/O) | I:0; O:1 | X | 0 | 0 |
| | | Secondary digital function | X | X | 1 | 0 |
| | | S22 | X | X | X | 1 |
| P5.3/SD2DIO/S21 | 3 | P5.3 (I/O) | I:0; O:1 | X | 0 | 0 |
| | | Secondary digital function | X | X | 1 | 0 |
| | | S21 | X | X | X | 1 |
| P5.4/SD3DIO/S20 | 4 | P5.4 (I/O) | I:0; O:1 | X | 0 | 0 |
| | | Secondary digital function | X | X | 1 | 0 |
| | | S20 | X | X | X | 1 |
| P5.5/SD4DIO/S19 | 5 | P5.5 (I/O) | I:0; O:1 | X | 0 | 0 |
| | | Secondary digital function | X | X | 1 | 0 |
| | | S19 | X | X | X | 1 |
| P5.6/SD5DIO/S18 | 6 | P5.6 (I/O) | I:0; O:1 | X | 0 | 0 |
| | | Secondary digital function | X | X | 1 | 0 |
| | | S18 | X | X | X | 1 |
| P5.7/SD6DIO/S17 | 7 | P5.7 (I/O) | I:0; O:1 | X | 0 | 0 |
| | | Secondary digital function | X | X | 1 | 0 |
| | | S17 | X | X | X | 1 |

(1) X = don't care

Port P6, P6.0, Input/Output With Schmitt Trigger (MSP430F677xIPEU Only)

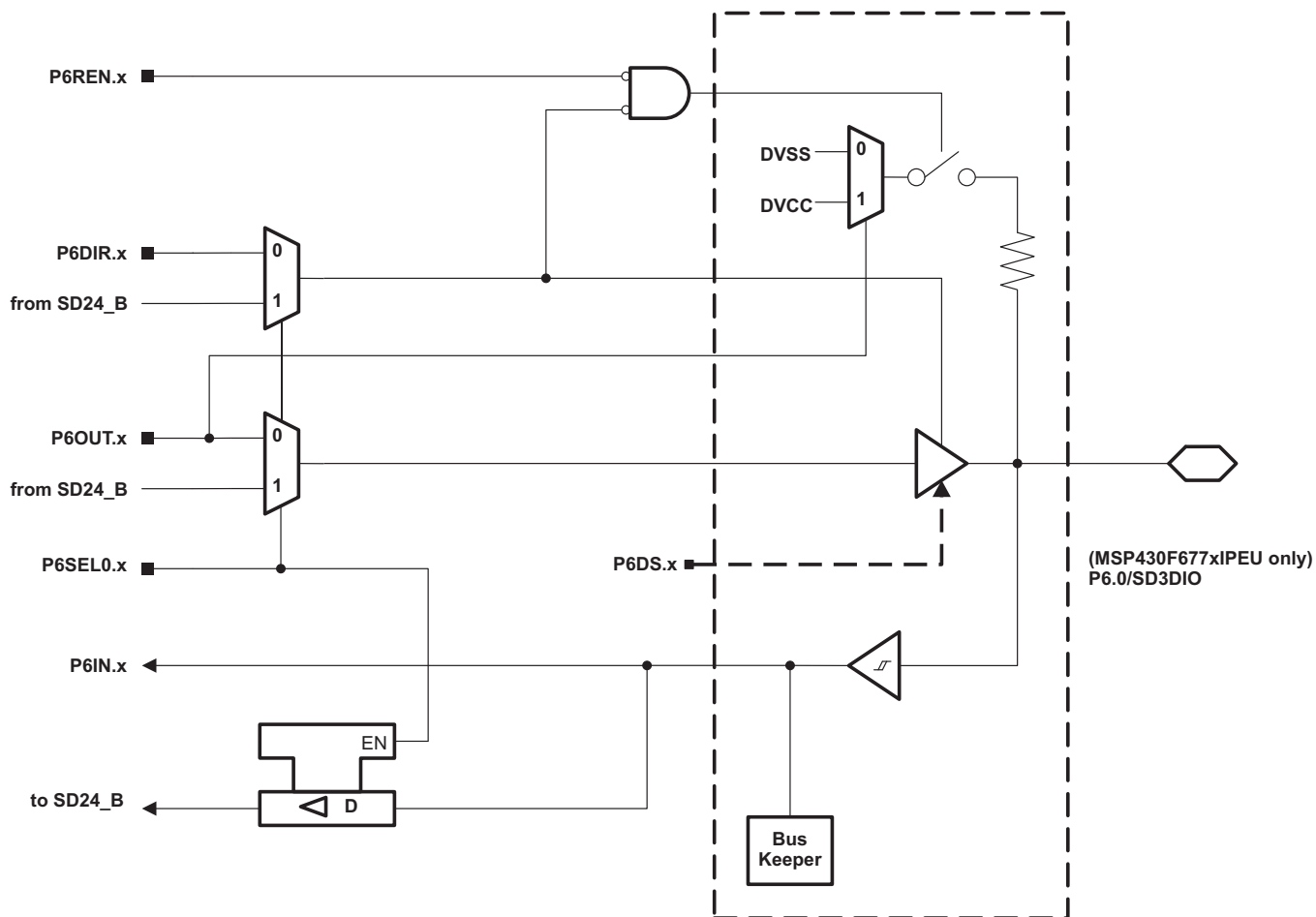


Table 85. Port P6 (P6.0) Pin Functions (MSP430F677xIPEU Only)

| PIN NAME (P6.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | |
|-----------------|---|----------------------------|--|----------|
| | | | P6DIR.x | P6SEL0.x |
| P6.0/SD3DIO | 0 | P6.0 (I/O) | I:0; O:1 | 0 |
| | | Secondary digital function | X | 1 |

(1) X = don't care

Port P6, P6.1 Through P6.3, Input/Output With Schmitt Trigger (MSP430F677xIPEU Only)

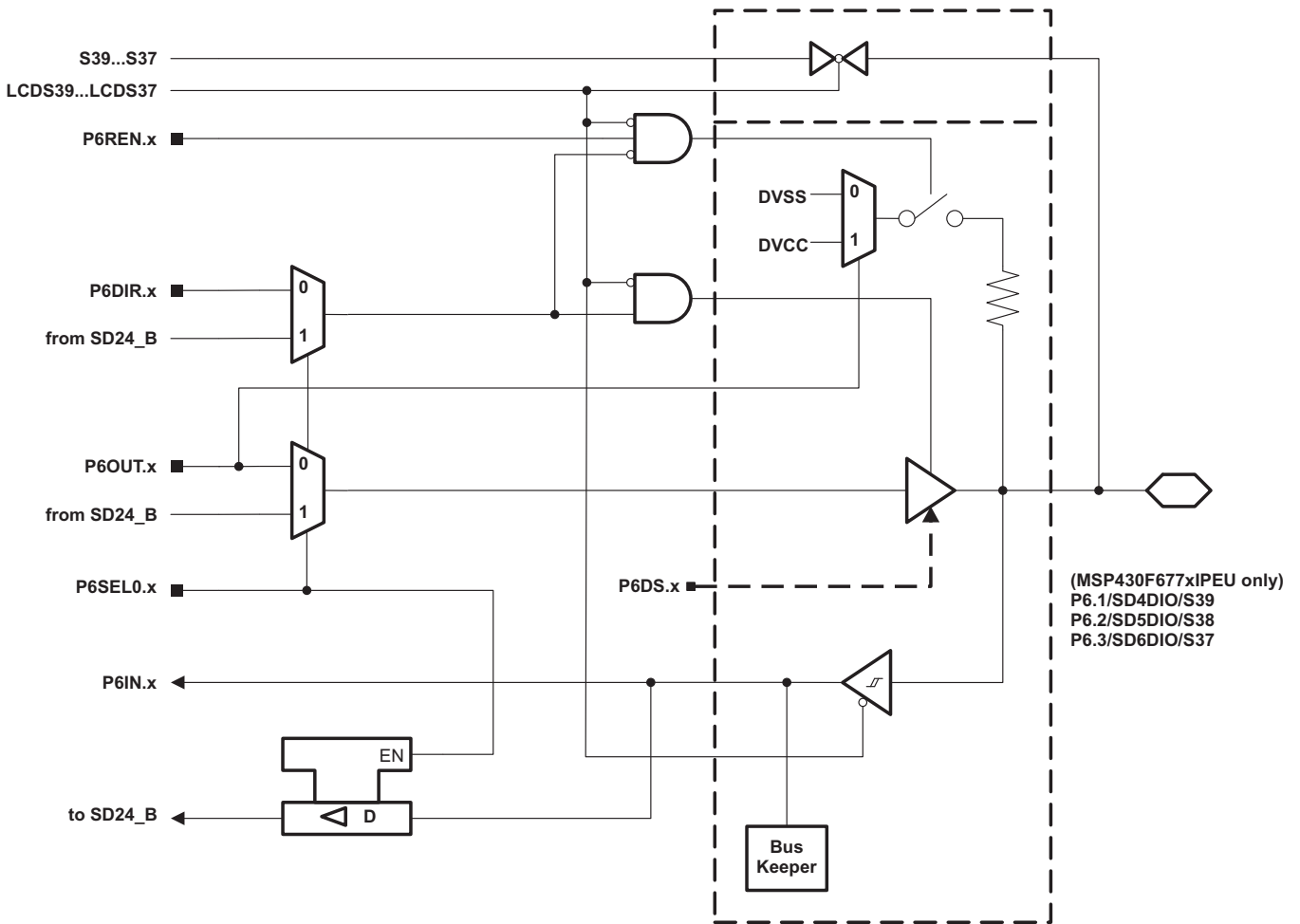


Table 86. Port P6 (P6.1 Through P6.3) Pin Functions (MSP430F677x1PEU Only)

| PIN NAME (P6.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|-----------------|---|----------------------------|--|----------|-----------|
| | | | P6DIR.x | P6SEL0.x | LCD39..37 |
| P6.1/SD4DIO/S39 | 1 | P6.1 (I/O) | I:0; O:1 | 0 | 0 |
| | | Secondary digital function | X | 1 | 0 |
| | | S39 | X | X | 1 |
| P6.2/SD5DIO/S38 | 2 | P6.2 (I/O) | I:0; O:1 | 0 | 0 |
| | | Secondary digital function | X | 1 | 0 |
| | | S38 | X | X | 1 |
| P6.3/SD6DIO/S37 | 3 | P6.3 (I/O) | I:0; O:1 | 0 | 0 |
| | | Secondary digital function | X | 1 | 0 |
| | | S37 | X | X | 1 |

(1) X = don't care

Port P6, P6.4 Through P6.7, Input/Output With Schmitt Trigger (MSP430F677xIPEU Only)

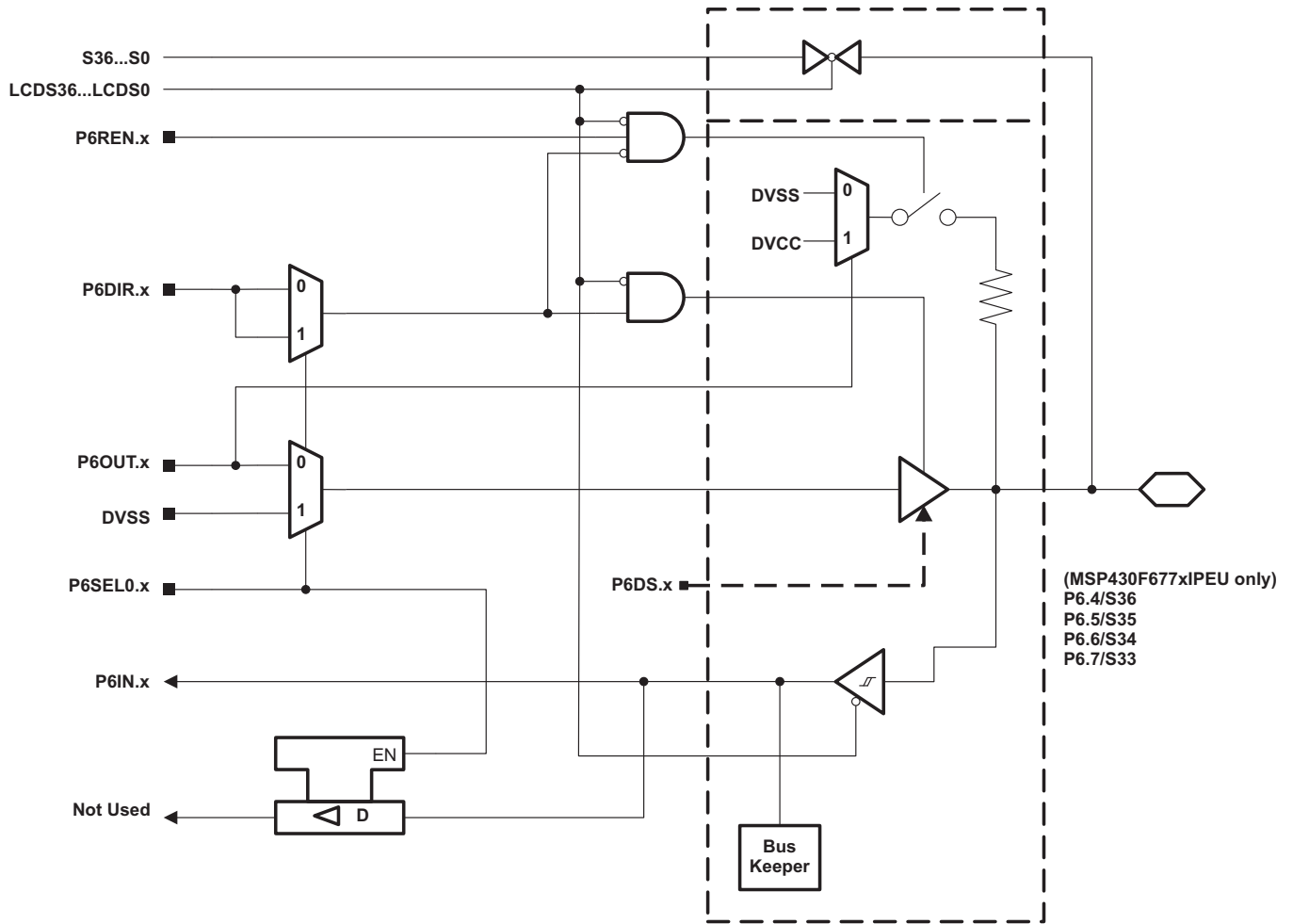


Table 87. Port P6 (P6.4 Through P6.7) Pin Functions (MSP430F67xxIPEU Only)

| PIN NAME (P6.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|-----------------|---|------------|--|----------|-----------|
| | | | P6DIR.x | P6SEL0.x | LCD36..33 |
| P6.4/S36 | 4 | P6.4 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S36 | X | X | 1 |
| P6.5/S35 | 5 | P6.5 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S35 | X | X | 1 |
| P6.6/S34 | 6 | P6.6(I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S34 | X | X | 1 |
| P6.7/S33 | 7 | P6.7 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S33 | X | X | 1 |

(1) X = don't care

Port P6, P6.0 Through P6.7, Input/Output With Schmitt Trigger (MSP430F677xIPZ Only)

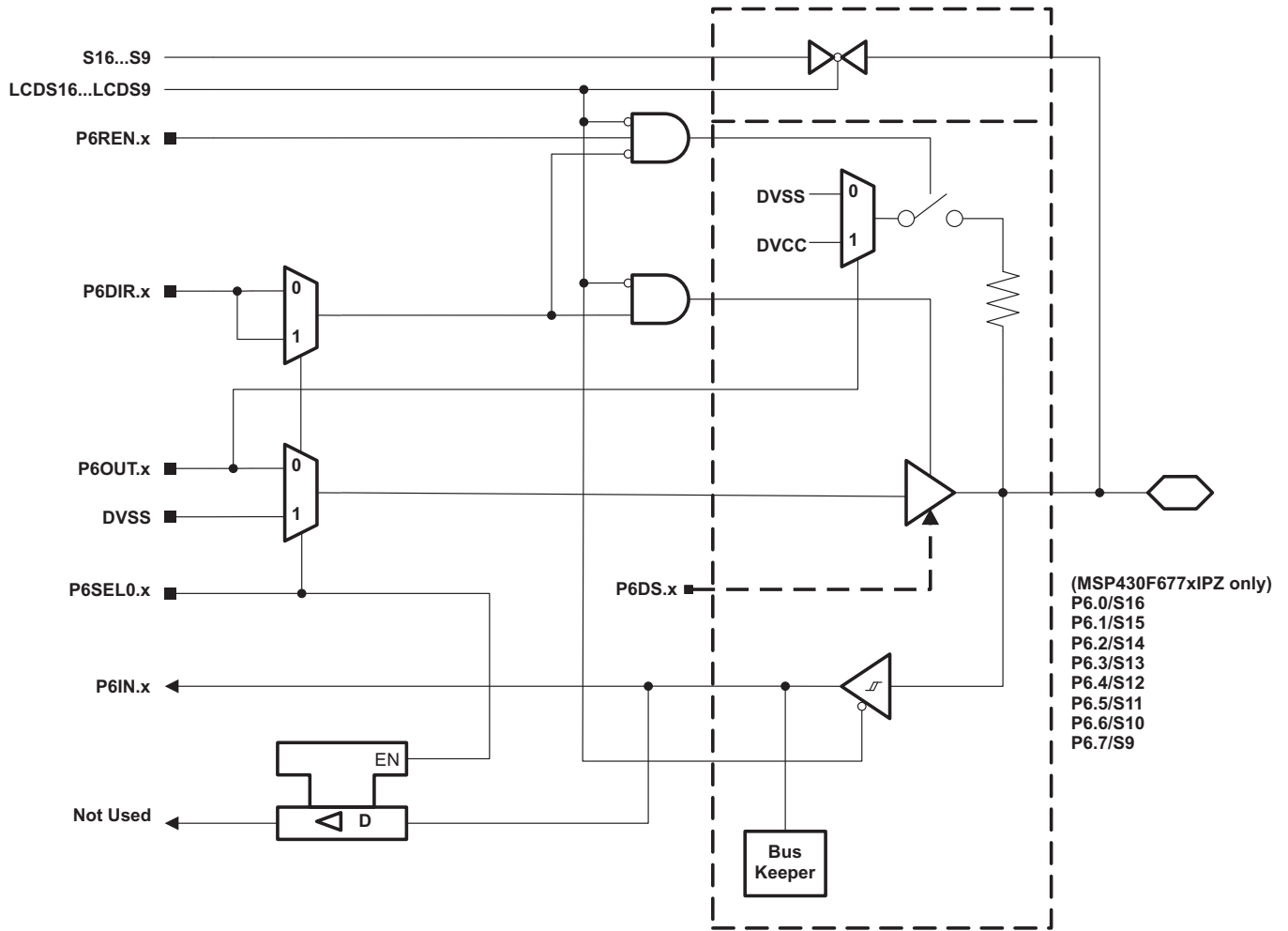


Table 88. Port P6 (P6.0 Through P6.7) Pin Functions (MSP430F67xxIPZ Only)

| PIN NAME (P6.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|-----------------|---|------------|--|----------|----------|
| | | | P6DIR.x | P6SEL0.x | LCD16..9 |
| P6.0/S16 | 0 | P6.0 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S16 | X | X | 1 |
| P6.1/S15 | 1 | P6.1 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S15 | X | X | 1 |
| P6.2/S14 | 2 | P6.2 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S14 | X | X | 1 |
| P6.3/S13 | 3 | P6.3 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S13 | X | X | 1 |
| P6.4/S12 | 4 | P6.4 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S12 | X | X | 1 |
| P6.5/S11 | 5 | P6.5 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S11 | X | X | 1 |
| P6.6/S10 | 6 | P6.6 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S10 | X | X | 1 |
| P6.7/S9 | 7 | P6.7 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S9 | X | X | 1 |

(1) X = don't care

Port P7, P7.0 Through P7.7, Input/Output With Schmitt Trigger (MSP430F67xxIPEU Only)

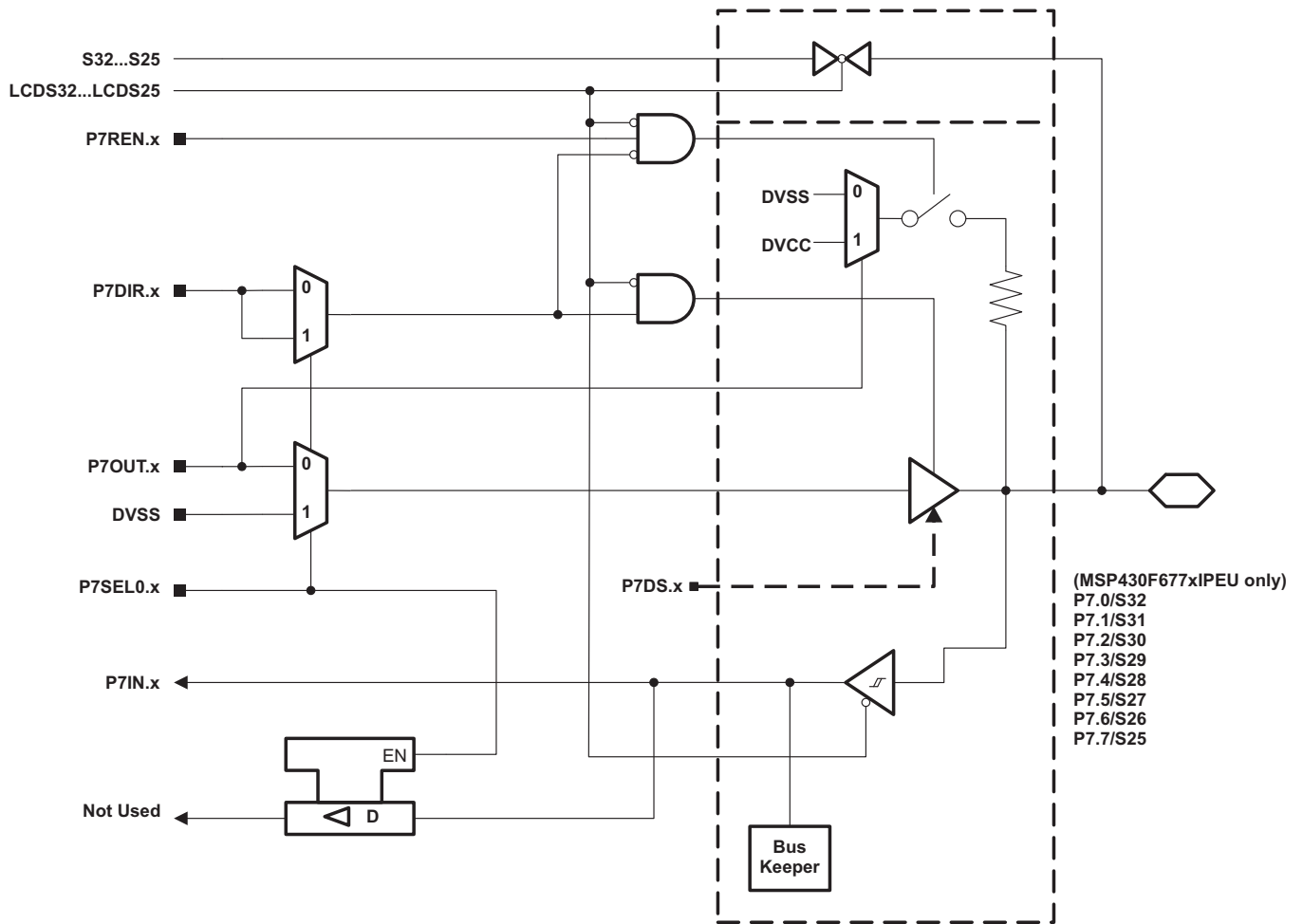


Table 89. Port P7 (P7.0 Through P7.7) Pin Functions (MSP430F67xxIPEU Only)

| PIN NAME (P7.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|-----------------|---|------------|--|----------|-----------|
| | | | P7DIR.x | P7SEL0.x | LCD32..25 |
| P7.0/S32 | 0 | P7.0 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S32 | X | X | 1 |
| P7.1/S31 | 1 | P7.1 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S31 | X | X | 1 |
| P7.2/S30 | 2 | P7.2 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S30 | X | X | 1 |
| P7.3/S29 | 3 | P7.3 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S29 | X | X | 1 |
| P7.4/S28 | 4 | P7.4 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S28 | X | X | 1 |
| P7.5/S27 | 5 | P7.5 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S27 | X | X | 1 |
| P7.6/S26 | 6 | P7.6 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S26 | X | X | 1 |
| P7.7/S25 | 7 | P7.7 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S25 | X | X | 1 |

(1) X = don't care

Port P7, P7.0 Through P7.7, Input/Output With Schmitt Trigger (MSP430F67xxIPZ Only)

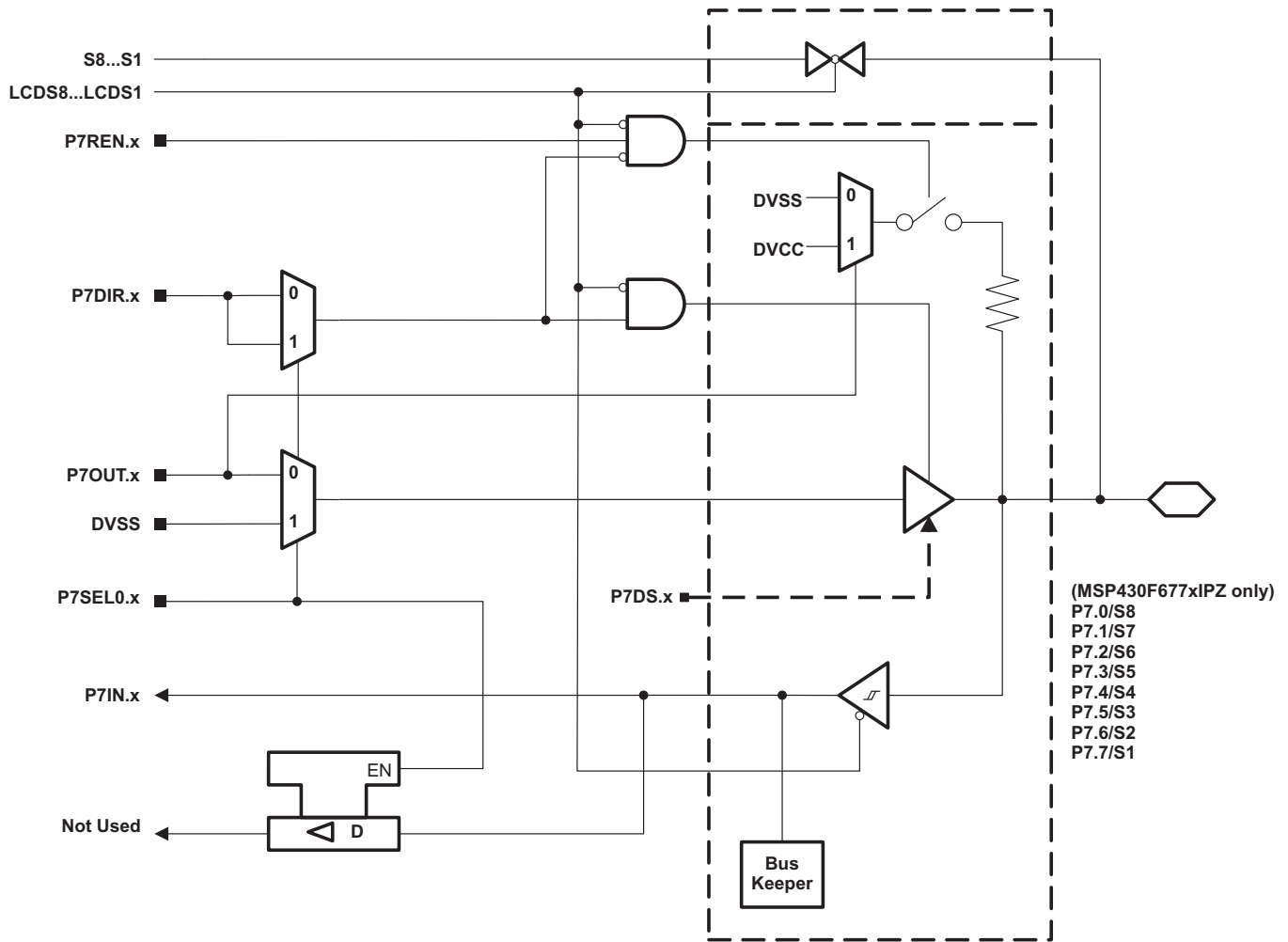


Table 90. Port P7 (P7.0 Through P7.7) Pin Functions (MSP430F67xxIPZ Only)

| PIN NAME (P7.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|-----------------|---|------------|--|----------|---------|
| | | | P7DIR.x | P7SEL0.x | LCD8..1 |
| P7.0/S8 | 0 | P7.0 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S8 | X | X | 1 |
| P7.1/S7 | 1 | P7.1 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S7 | X | X | 1 |
| P7.2/S6 | 2 | P7.2 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S6 | X | X | 1 |
| P7.3/S5 | 3 | P7.3 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S5 | X | X | 1 |
| P7.4/S4 | 4 | P7.4 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S4 | X | X | 1 |
| P7.5/S3 | 5 | P7.5 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S3 | X | X | 1 |
| P7.6/S2 | 6 | P7.6 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S2 | X | X | 1 |
| P7.7/S1 | 7 | P7.7 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S1 | X | X | 1 |

(1) X = don't care

Port P8, P8.0 Through P8.7, Input/Output With Schmitt Trigger (MSP430F677xIPEU Only)

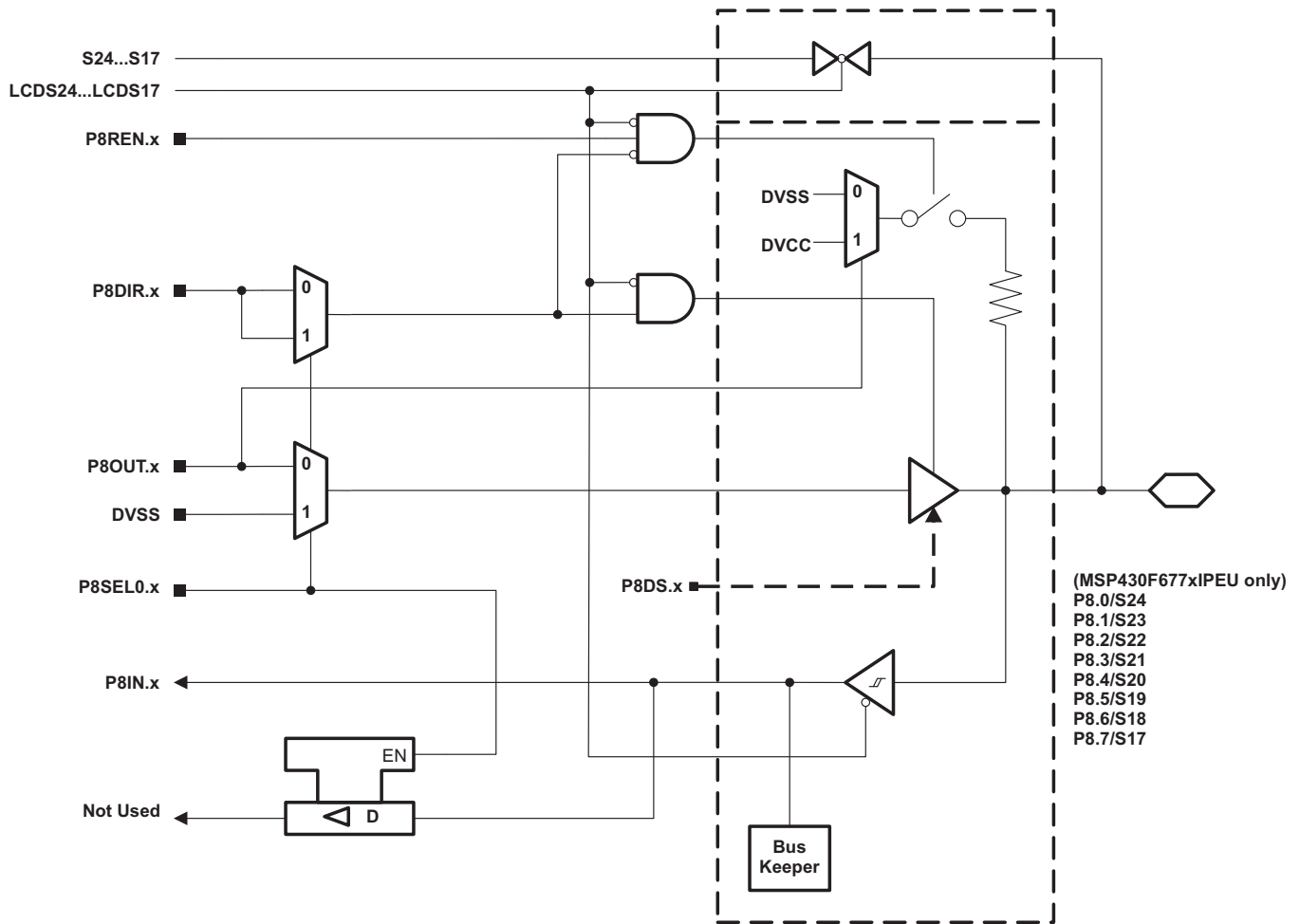


Table 91. Port P8 (P8.0 Through P8.7) Pin Functions (MSP430F677x1PEU Only)

| PIN NAME (P8.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|-----------------|---|------------|--|----------|-----------|
| | | | P8DIR.x | P8SEL0.x | LCD24..17 |
| P8.0/S24 | 0 | P8.0 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S24 | X | X | 1 |
| P8.1/S23 | 1 | P8.1 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S23 | X | X | 1 |
| P8.2/S22 | 2 | P8.2 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S22 | X | X | 1 |
| P8.3/S21 | 3 | P8.3 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S21 | X | X | 1 |
| P8.4/S20 | 4 | P8.4 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S20 | X | X | 1 |
| P8.5/S19 | 5 | P8.5 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S19 | X | X | 1 |
| P8.6/S18 | 6 | P8.6 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S18 | X | X | 1 |
| P8.7/S17 | 7 | P8.7 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S17 | X | X | 1 |

(1) X = don't care

Port P8, P8.0, Input/Output With Schmitt Trigger (MSP430F677xIPZ Only)

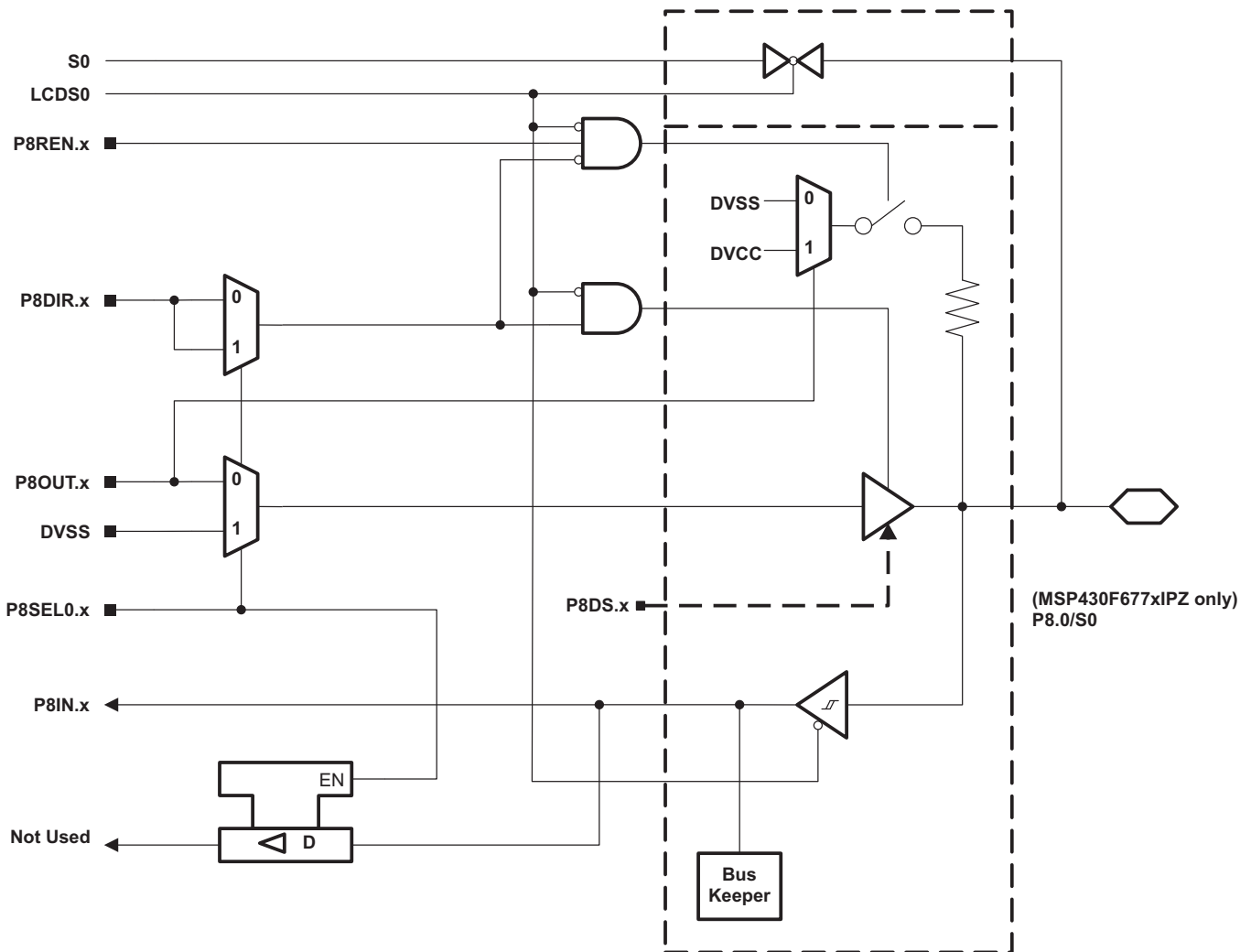


Table 92. Port P8 (P8.0) Pin Functions (MSP430F677xIPZ Only)

| PIN NAME (P8.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|-----------------|---|------------|--|----------|------|
| | | | P8DIR.x | P8SEL0.x | LCD0 |
| P8.0/S0 | 0 | P8.0 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S0 | X | X | 1 |

(1) X = don't care

Port P8, P8.1, Input/Output With Schmitt Trigger (MSP430F677xIPZ Only)

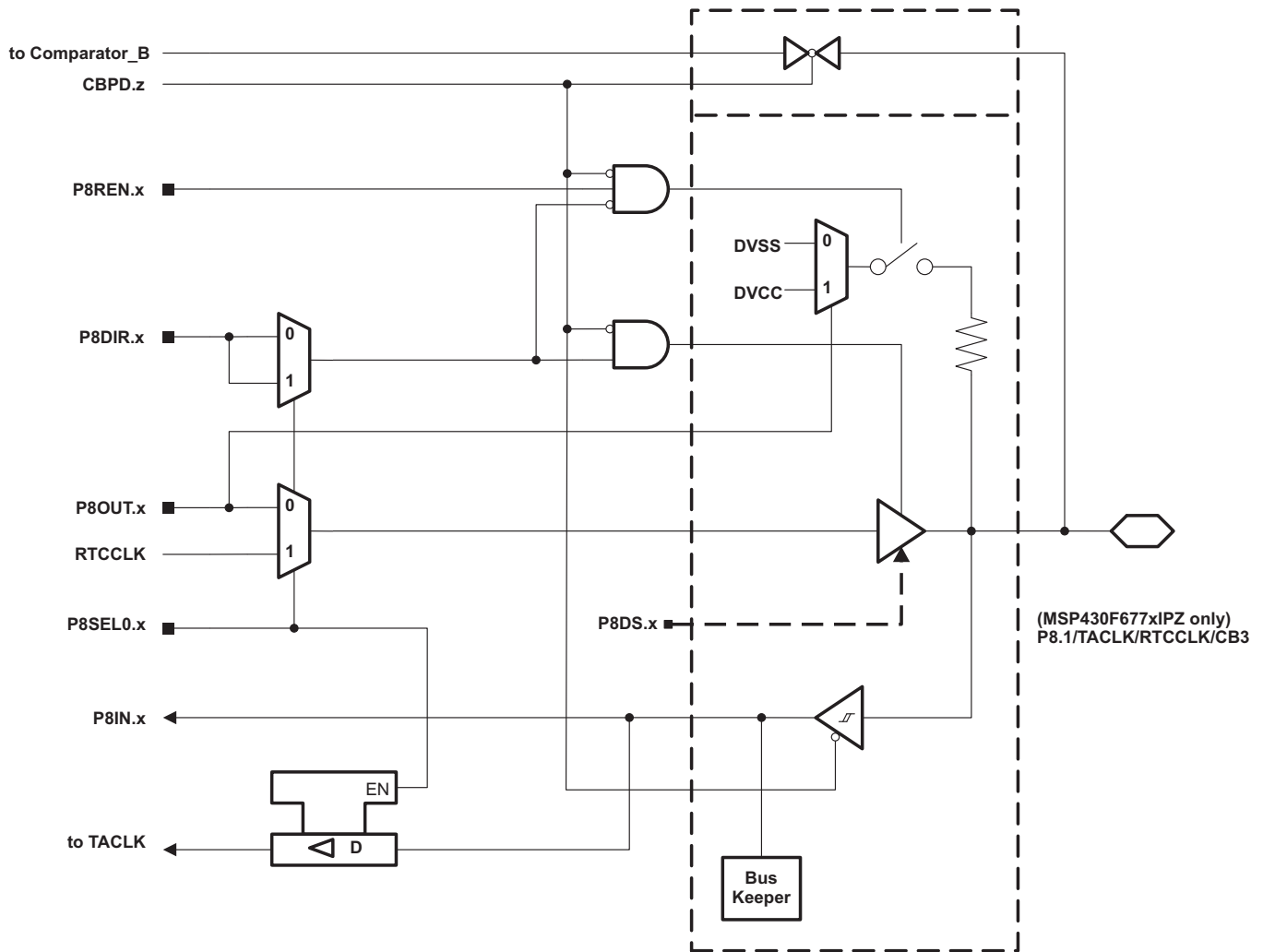


Table 93. Port P8 (P8.1) Pin Functions (MSP430F677xIPZ Only)

| PIN NAME (P8.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|---------------------------|---|------------|--|----------|-----------|
| | | | P8DIR.x | P8SEL0.x | CBPD.z |
| P8.1/TACLK/RTCCLK/ CB3 | 1 | P8.1 (I/O) | I:0; O:1 | 0 | 0 |
| | | TACLK | 0 | 1 | 0 |
| | | RTCCLK | 1 | 1 | 0 |
| | | CB3 | X | X | 1 (z = 3) |

(1) X = don't care

Port P9, P9.0 Through P9.7, Input/Output With Schmitt Trigger (MSP430F677xIPEU Only)

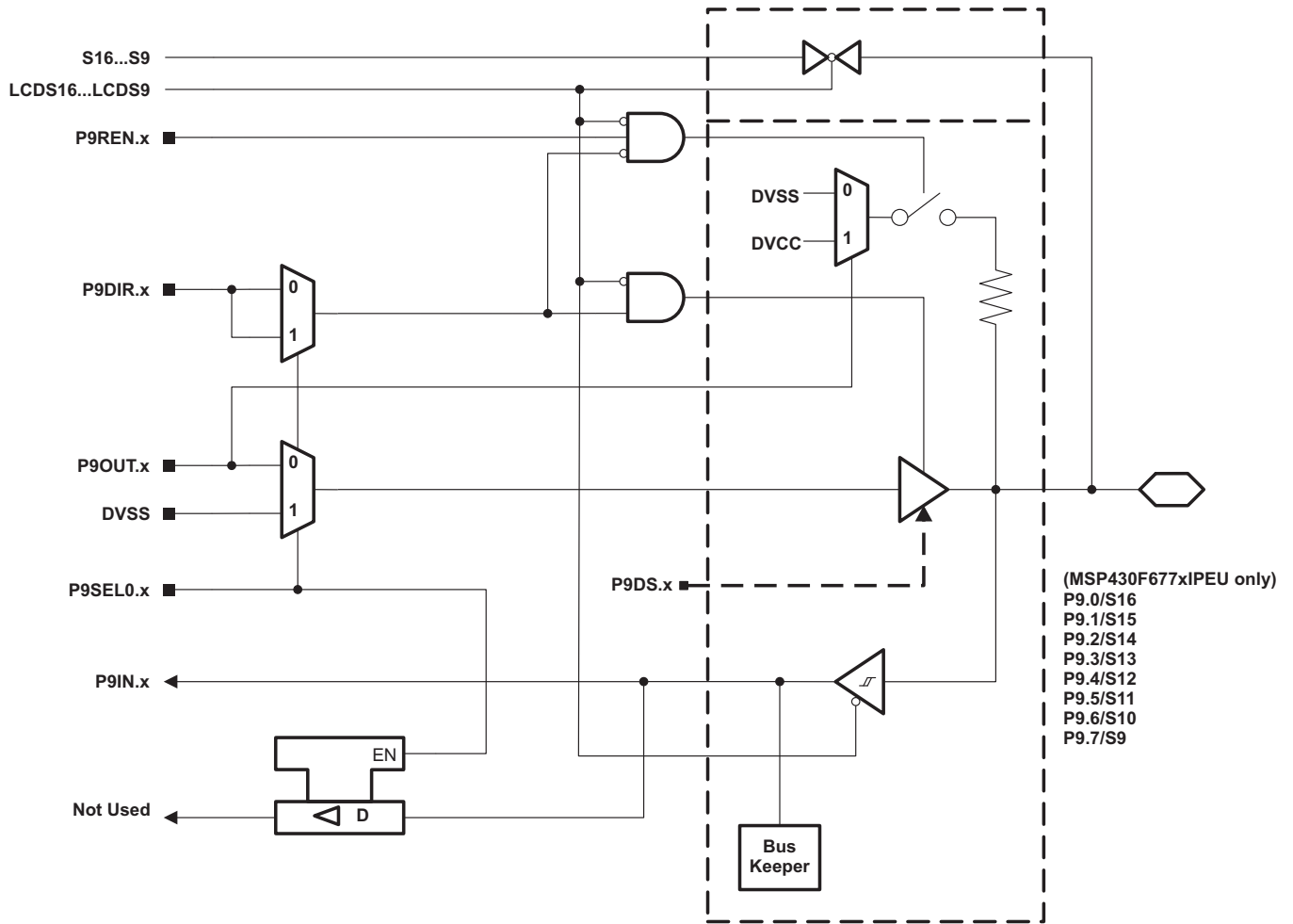


Table 94. Port P9 (P9.0 to P9.7) Pin Functions (MSP430F677xIPEU Only)

| PIN NAME (P9.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|-----------------|---|------------|--|----------|----------|
| | | | P9DIR.x | P9SEL0.x | LCD16..9 |
| P9.0/S16 | 0 | P9.0 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S16 | X | X | 1 |
| P9.1/S15 | 1 | P9.1 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S15 | X | X | 1 |
| P9.2/S14 | 2 | P9.2 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S14 | X | X | 1 |
| P9.3/S13 | 3 | P9.3 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S13 | X | X | 1 |
| P9.4/S12 | 4 | P9.4 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S12 | X | X | 1 |
| P9.5/S11 | 5 | P9.5 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S11 | X | X | 1 |
| P9.6/S10 | 6 | P9.6 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S10 | X | X | 1 |
| P9.7/S9 | 7 | P9.7 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S9 | X | X | 1 |

(1) X = don't care

Port P10, P10.0 Through P10.7, Input/Output With Schmitt Trigger (MSP430F677xIPEU Only)

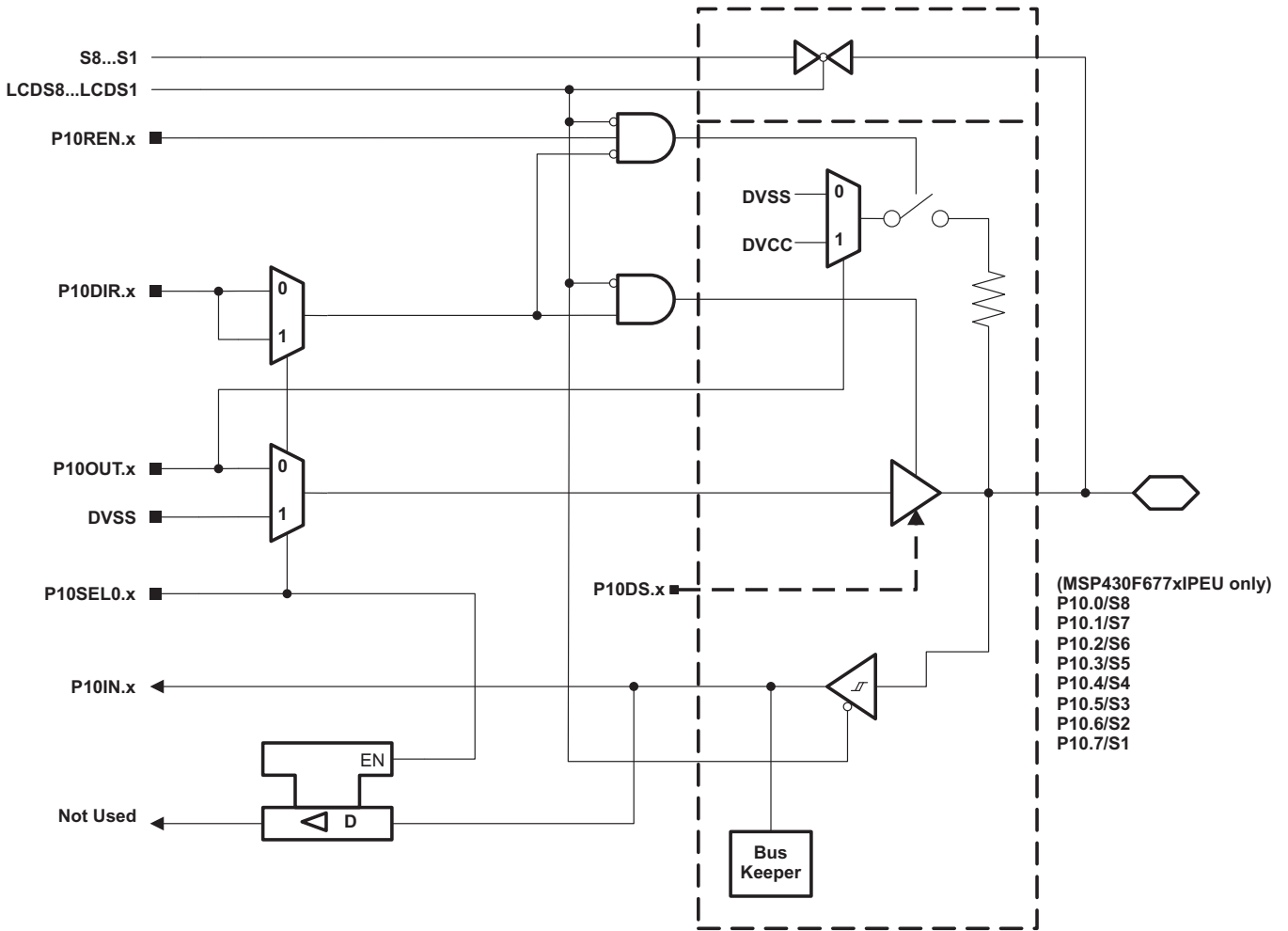


Table 95. Port P10 (P10.0 Through P10.7) Pin Functions (MSP430F677xIPEU Only)

| PIN NAME (P10.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|------------------|---|-------------|--|-----------|---------|
| | | | P10DIR.x | P10SEL0.x | LCD8..1 |
| P10.0/S8 | 0 | P10.0 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S8 | X | X | 1 |
| P10.1/S7 | 1 | P10.1 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S7 | X | X | 1 |
| P10.2/S6 | 2 | P10.2 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S6 | X | X | 1 |
| P10.3/S5 | 3 | P10.3 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S5 | X | X | 1 |
| P10.4/S4 | 4 | P10.4 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S4 | X | X | 1 |
| P10.5/S3 | 5 | P10.5 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S3 | X | X | 1 |
| P10.6/S2 | 6 | P10.6 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S2 | X | X | 1 |
| P10.7/S1 | 7 | P10.7 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S1 | X | X | 1 |

(1) X = don't care

Port P11, P11.0, Input/Output With Schmitt Trigger (MSP430F677xIPEU Only)

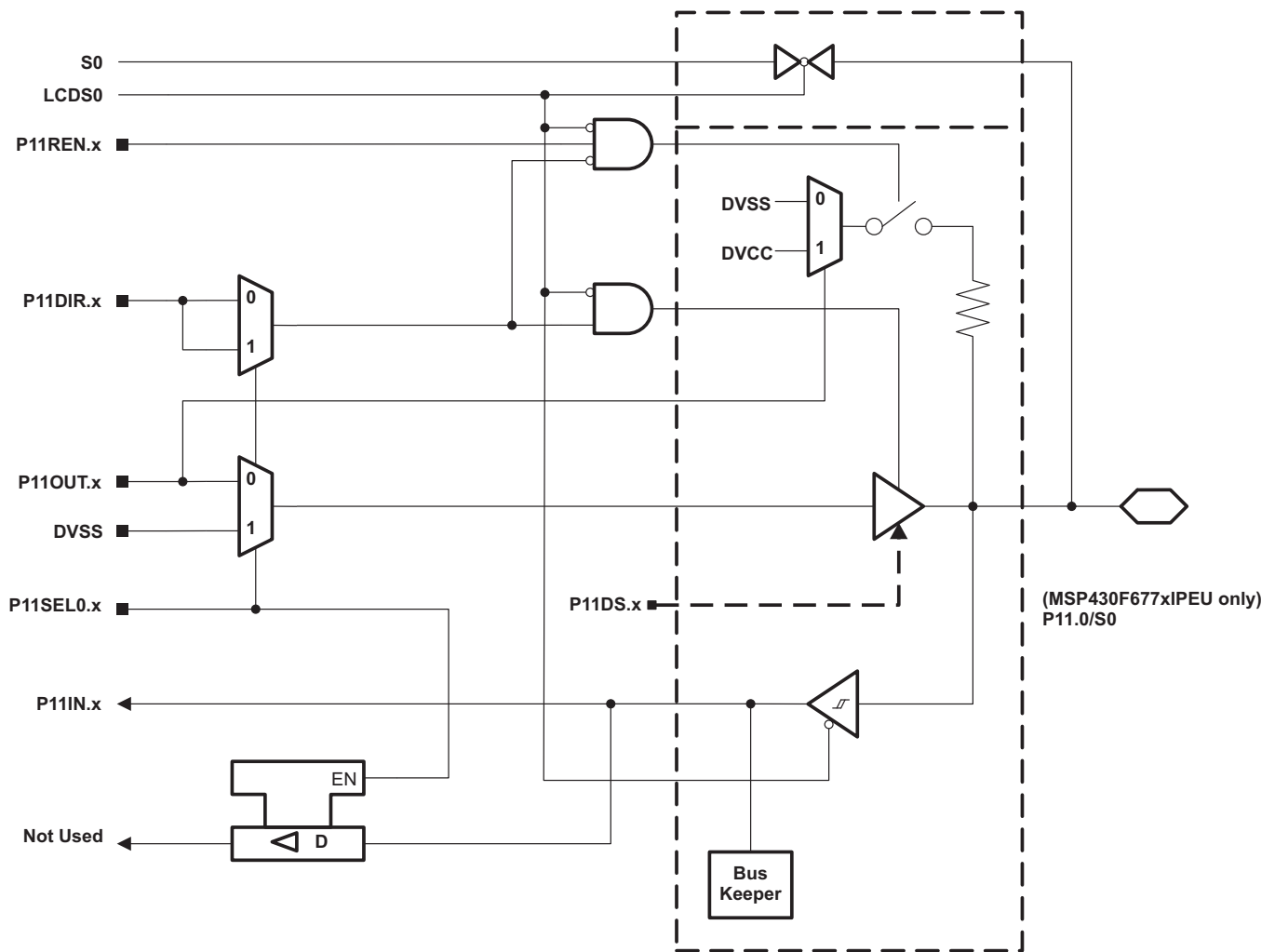


Table 96. Port P11 (P11.0) Pin Functions (MSP430F677xIPEU Only)

| PIN NAME (P11.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|------------------|---|-------------|--|-----------|------|
| | | | P11DIR.x | P11SEL0.x | LCD0 |
| P11.0/S0 | 0 | P11.0 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S0 | X | X | 1 |

(1) X = don't care

Port P11, P11.1, Input/Output With Schmitt Trigger (MSP430F677xIPEU Only)

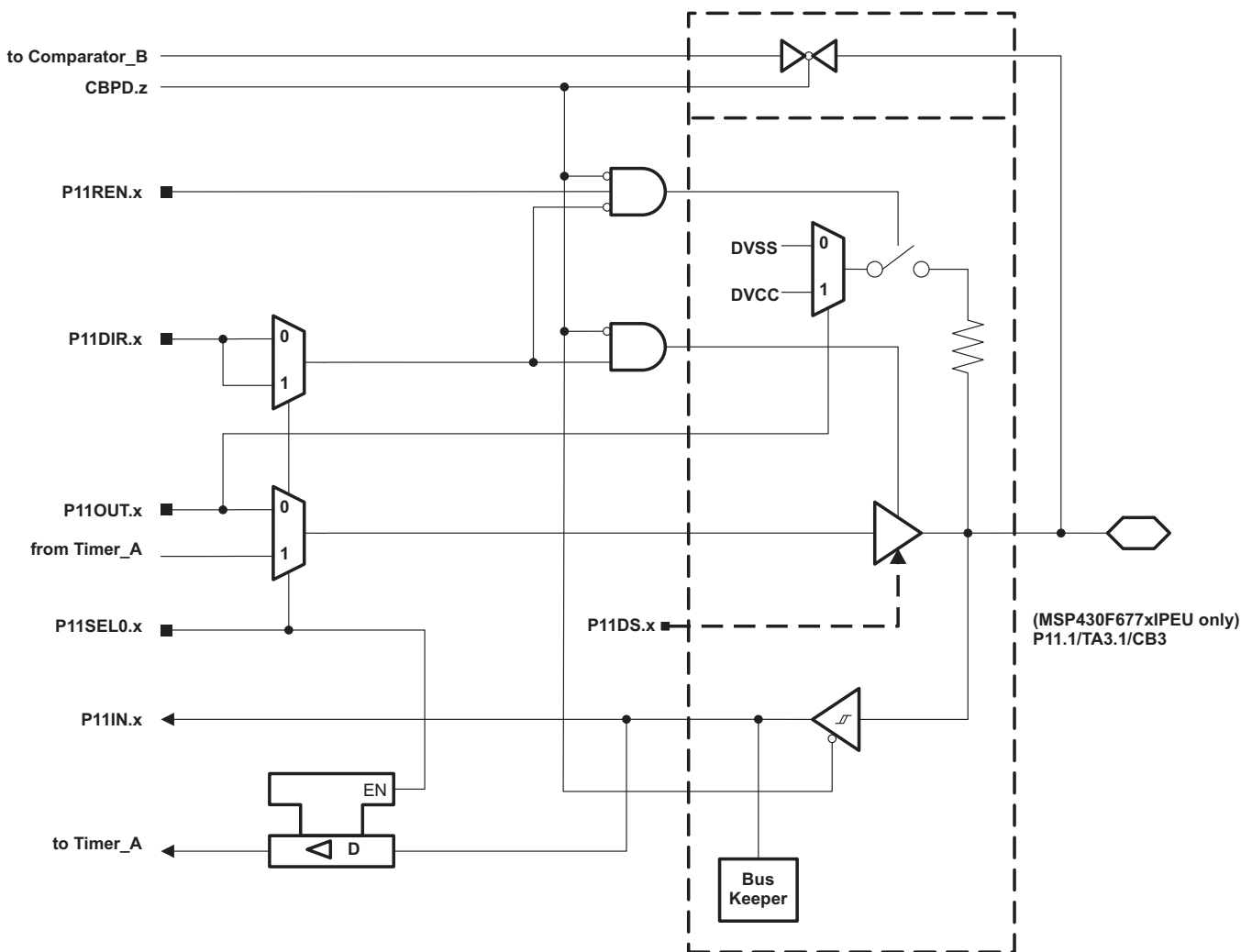


Table 97. Port P11 (P11.1) Pin Functions (MSP430F677xIPEU Only)

| PIN NAME (P11.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|------------------|---|-------------|--|-----------|--------|
| | | | P11DIR.x | P11SEL0.x | CBPD.z |
| P11.1/TA3.1/CB3 | 1 | P11.1 (I/O) | I:0; O:1 | 0 | 0 |
| | | TA3.CC1A | 0 | 1 | 0 |
| | | TA3.1 | 1 | 1 | 0 |
| | | CB3 | X | X | 1 |

(1) X = don't care

Port P11, P11.2 and P11.3, Input/Output With Schmitt Trigger (MSP430F677xIPEU Only)

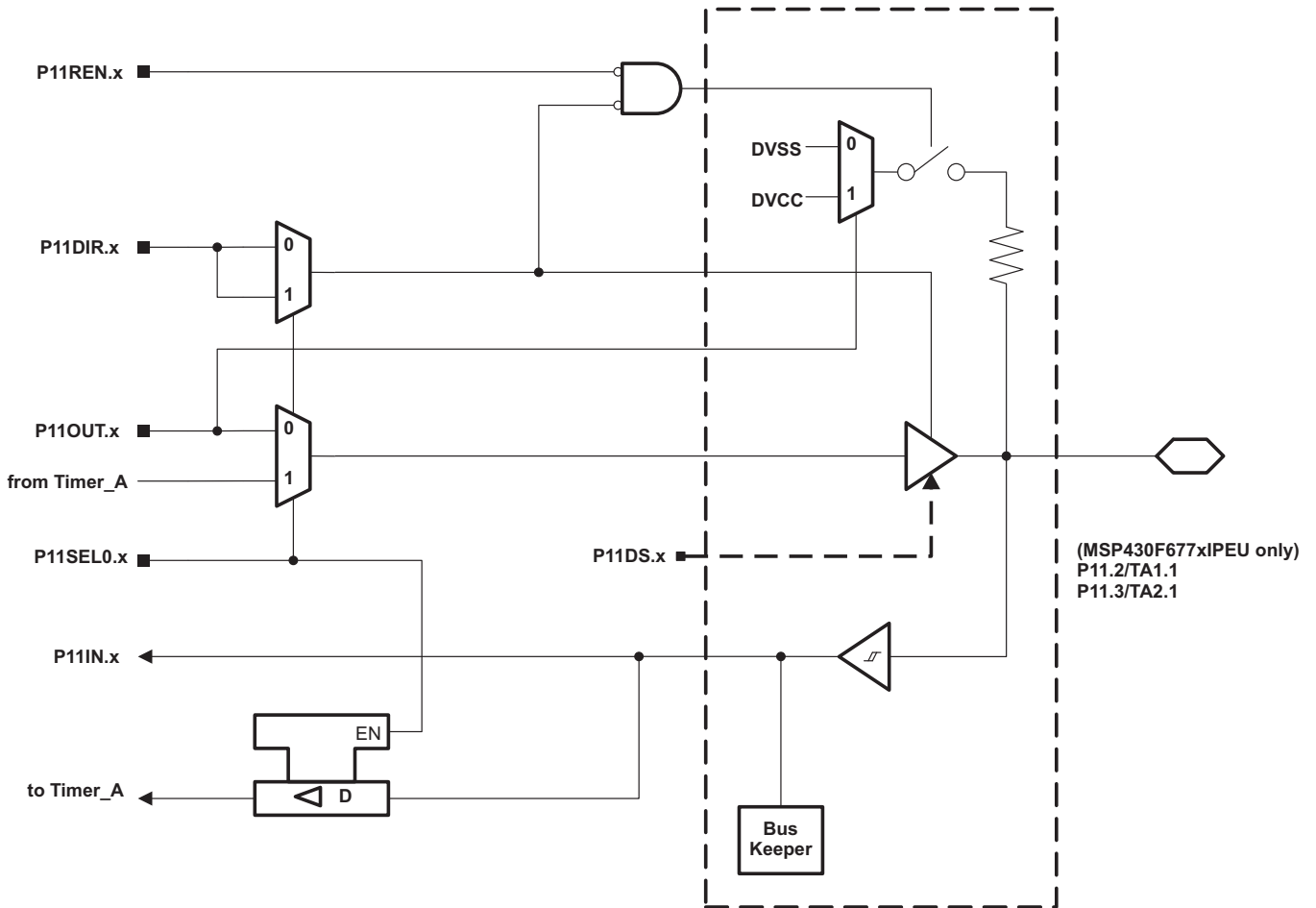


Table 98. Port P11 (P11.2 and P11.3) Pin Functions (MSP430F677xIPEU Only)

| PIN NAME (P11.x) | x | FUNCTION | CONTROL BITS OR SIGNALS | |
|------------------|---|-------------|-------------------------|-----------|
| | | | P11DIR.x | P11SEL0.x |
| P11.2/TA1.1 | 2 | P11.2 (I/O) | I:0; O:1 | 0 |
| | | TA1.CCI1A | 0 | 1 |
| | | TA1.1 | 1 | 1 |
| P11.3/TA2.1 | 3 | P11.3 (I/O) | I:0; O:1 | 0 |
| | | TA2.CCI1A | 0 | 1 |
| | | TA2.1 | 1 | 1 |

Port P11, P11.4 and P11.5, Input/Output With Schmitt Trigger (MSP430F677xIPEU Only)

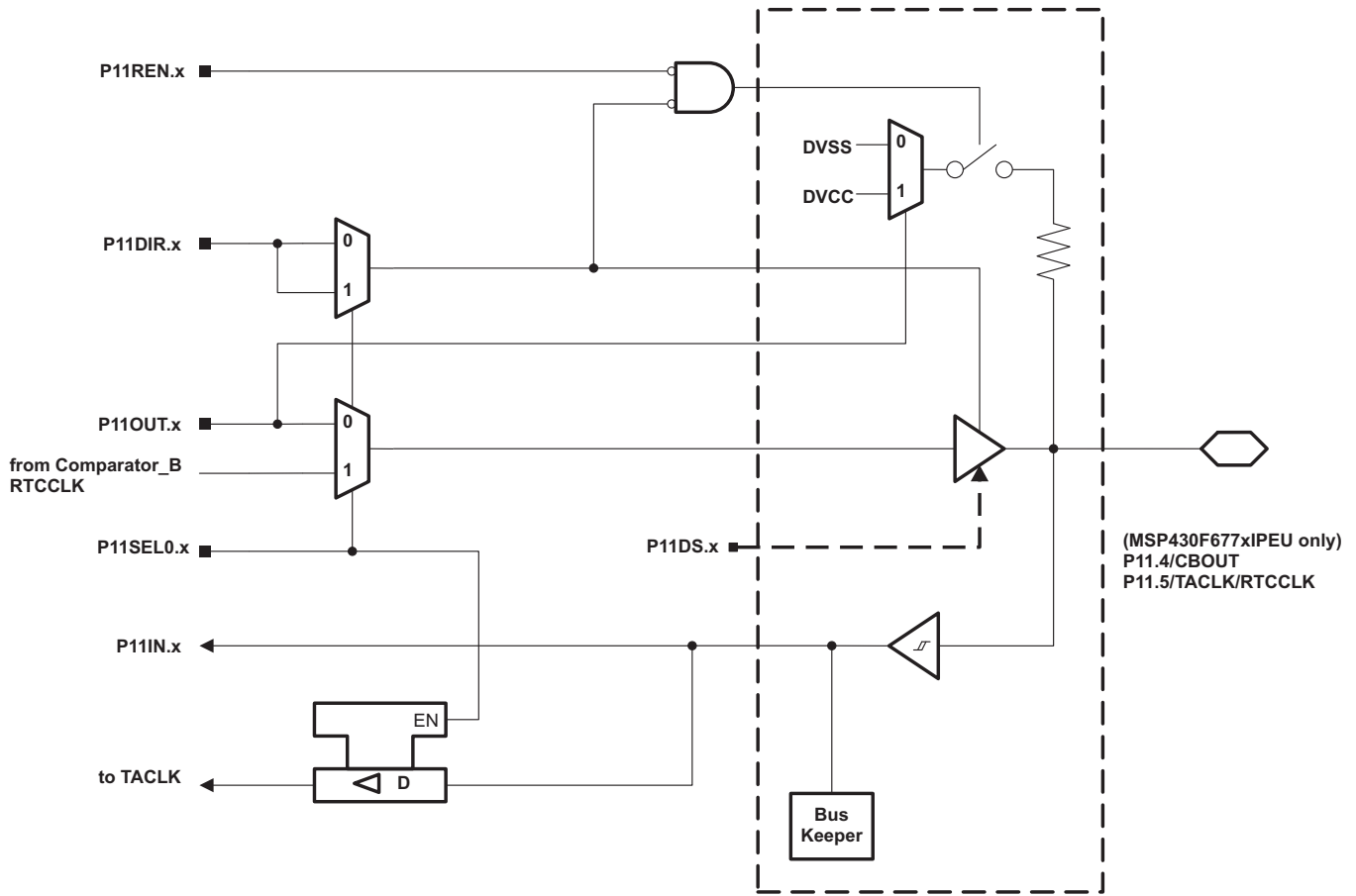
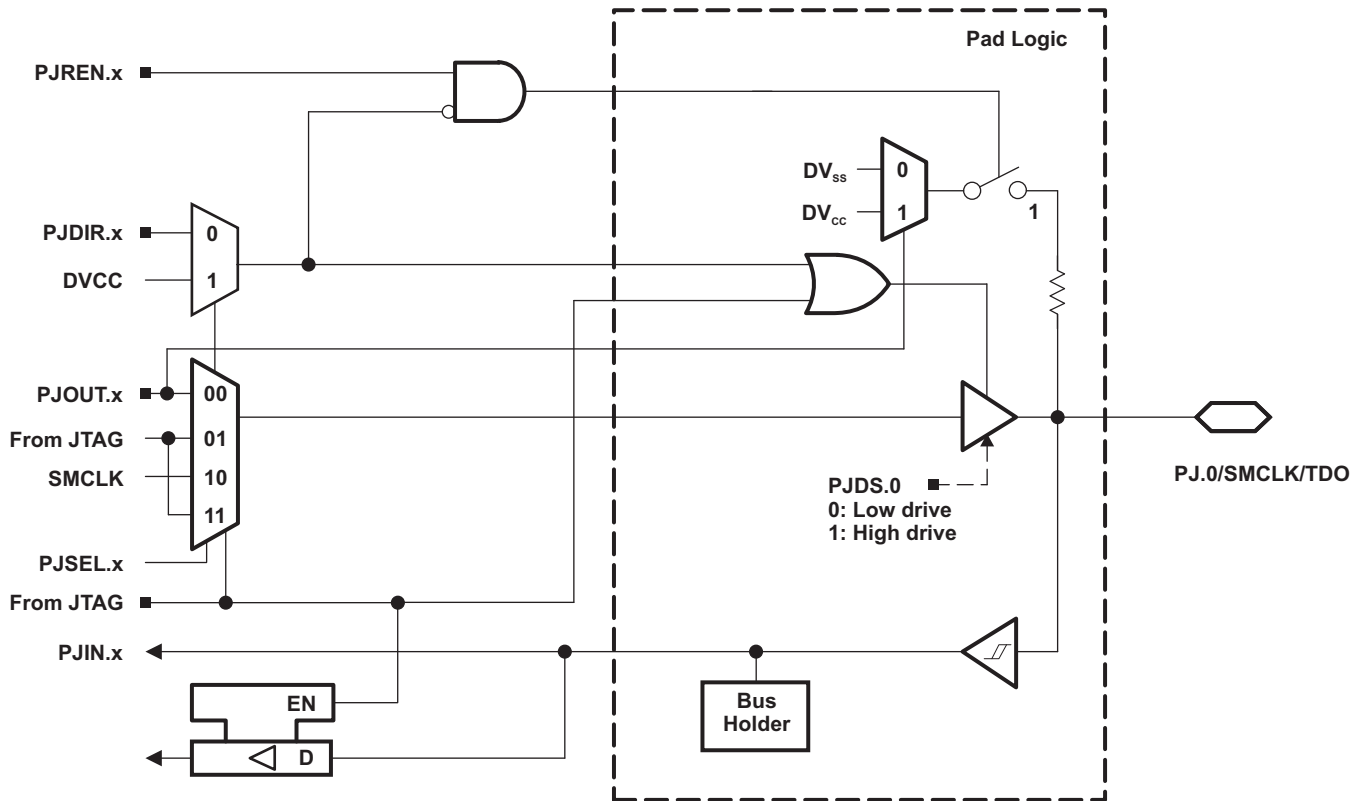


Table 99. Port P11 (P11.4 and P11.5) Pin Functions (MSP430F677xIPEU Only)

| PIN NAME (P11.x) | x | FUNCTION | CONTROL BITS OR SIGNALS | |
|--------------------|---|-------------|-------------------------|-----------|
| | | | P11DIR.x | P11SEL0.x |
| P11.4/CBOUT | 4 | P11.4 (I/O) | I:0; O:1 | 0 |
| | | N/A | 0 | 1 |
| | | CBOUT | 1 | 1 |
| P11.5/TACLK/RTCCLK | 5 | P11.5 (I/O) | I:0; O:1 | 0 |
| | | TACLK | 0 | 1 |
| | | RTCCLK | 1 | 1 |

Port J, J.0, JTAG pin TDO, Input/Output With Schmitt Trigger or Output



Port J, J.1 to J.3, JTAG Pins TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger or Output

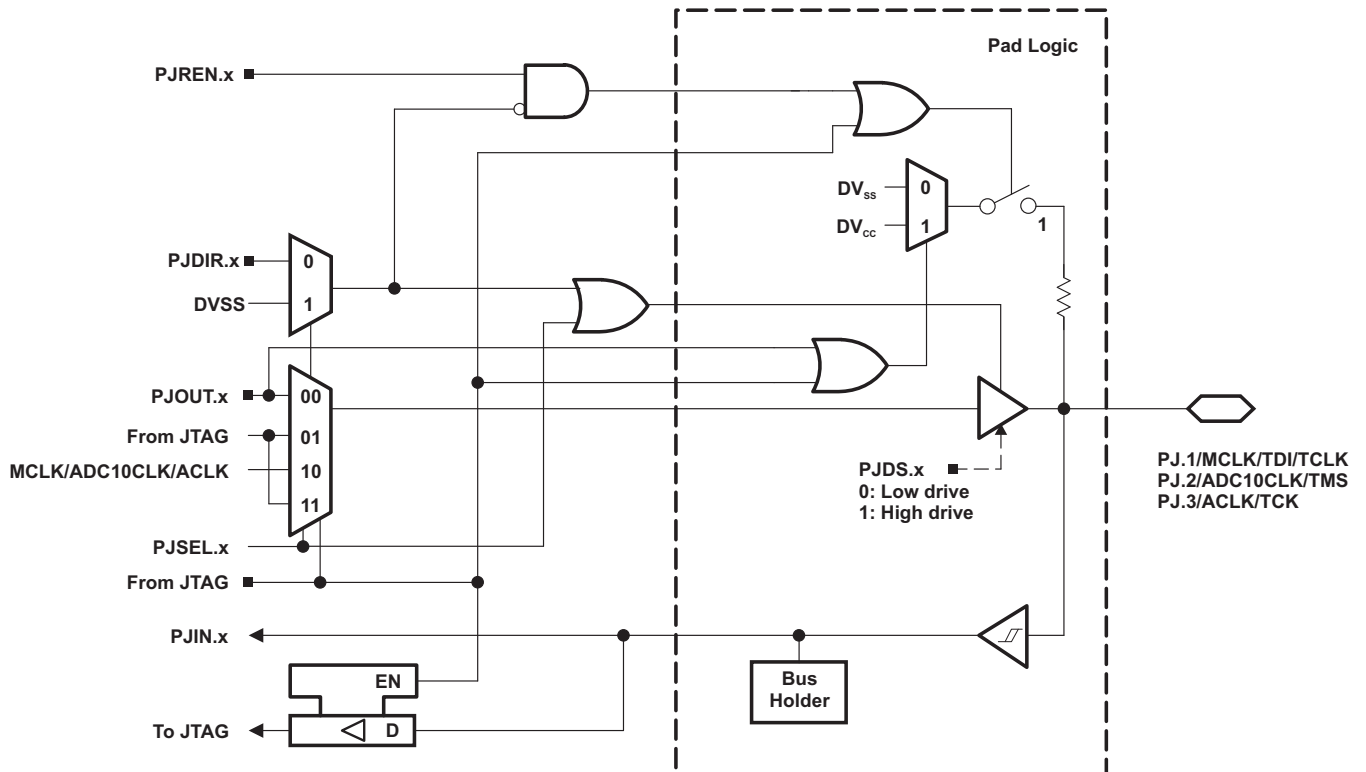


Table 100. Port PJ (PJ.0 to PJ.3) Pin Functions

| PIN NAME (PJ.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|--------------------|---|-----------------------------|--|---------|-----------|
| | | | PJDIR.x | PJSEL.x | JTAG MODE |
| PJ.0/SMCLK/TDO | 0 | PJ.0 (I/O) ⁽²⁾ | I: 0; O: 1 | 0 | 0 |
| | | SMCLK | 1 | 1 | 0 |
| | | TDO ⁽³⁾ | x | x | 1 |
| PJ.1/MCLK/TDI/TCLK | 1 | PJ.1 (I/O) ⁽²⁾ | I: 0; O: 1 | 0 | 0 |
| | | MCLK | 1 | 1 | 0 |
| | | TDI/TCLK ^{(3) (4)} | x | x | 1 |
| PJ.2/ADC10CLK/TMS | 2 | PJ.2 (I/O) ⁽²⁾ | I: 0; O: 1 | 0 | 0 |
| | | ADC10CLK | 1 | 1 | 0 |
| | | TMS ^{(3) (4)} | x | x | 1 |
| PJ.3/ACLK/TCK | 3 | PJ.3 (I/O) ⁽²⁾ | I: 0; O: 1 | 0 | 0 |
| | | ACLK | 1 | 1 | 0 |
| | | TCK ^{(3) (4)} | x | x | 1 |

(1) X = don't care

(2) Default condition

(3) The pin direction is controlled by the JTAG module.

(4) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are don't care.

Device Descriptors (TLV)

list the complete contents of the device descriptor tag-length-value (TLV) structure for each device type.

Table 101. F677x1 Device Descriptor Table

| | Description | Address | Size in bytes | F67791IPEU F67791IPZ | F67781IPEU F67781IPZ | F67771IPEU F67771IPZ | F67761IPEU F67761IPZ | F67751IPEU F67751IPZ |
|-------------------|------------------------|---------|---------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| | | | | Value | Value | Value | Value | Value |
| Info Block | Info Length | 1A00h | 1 | 06h | 06h | 06h | 06h | 06h |
| | CRC Length | 1A01h | 1 | 06h | 06h | 06h | 06h | 06h |
| | CRC Value | 1A02h | 2 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| | Device ID | 1A04h | 2 | 81A5h | 81A4h | 81A3h | 81A2h | 81A1h |
| | Hardware Revision | 1A06h | 1 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| | Firmware Revision | 1A07h | 1 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| Die Record | Die Record Tag | 1A08h | 1 | 08h | 08h | 08h | 08h | 08h |
| | Die Record Length | 1A09h | 1 | 0Ah | 0Ah | 0Ah | 0Ah | 0Ah |
| | Lot ID | 1A0Ah | 4 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| | X Position | 1A0Eh | 2 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| | Y Position | 1A10h | 2 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| | Test Record CP | 1A12h | 1 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| | Test Record FT | 1A13h | 1 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| ADC10 Calibration | ADC Calibration Tag | 1A14h | 1 | 13h | 13h | 13h | 13h | 13h |
| | ADC Calibration Length | 1A15h | 1 | 10h | 10h | 10h | 10h | 10h |
| | ADC Gain Factor | 1A16h | 2 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| | ADC Offset | 1A18h | 2 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| | ADC 15T30 | 1A1Ah | 2 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| | ADC 15T85 | 1A1Ch | 2 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| | ADC 20T30 | 1A1Eh | 2 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| | ADC 20T85 | 1A20h | 2 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| | ADC 25T30 | 1A22h | 2 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| ADC 25T85 | 1A24h | 2 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit | |

Table 102. F676x1 Device Descriptor Table

| | Description | Address | Size in bytes | F676911PEU F676911PZ | F676811PEU F676811PZ | F676711PEU F676711PZ | F676611PEU F676611PZ | F676511PEU F676511PZ |
|-------------------|------------------------|---------|---------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| | | | | Value | Value | Value | Value | Value |
| Info Block | Info Length | 1A00h | 1 | 06h | 06h | 06h | 06h | 06h |
| | CRC Length | 1A01h | 1 | 06h | 06h | 06h | 06h | 06h |
| | CRC Value | 1A02h | 2 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| | Device ID | 1A04h | 2 | 81A0h | 819Fh | 819Eh | 819Dh | 819Ch |
| | Hardware Revision | 1A06h | 1 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| | Firmware Revision | 1A07h | 1 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| Die Record | Die Record Tag | 1A08h | 1 | 08h | 08h | 08h | 08h | 08h |
| | Die Record Length | 1A09h | 1 | 0Ah | 0Ah | 0Ah | 0Ah | 0Ah |
| | Lot ID | 1A0Ah | 4 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| | X Position | 1A0Eh | 2 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| | Y Position | 1A10h | 2 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| | Test Record CP | 1A12h | 1 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| | Test Record FT | 1A13h | 1 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| ADC10 Calibration | ADC Calibration Tag | 1A14h | 1 | 13h | 13h | 13h | 13h | 13h |
| | ADC Calibration Length | 1A15h | 1 | 10h | 10h | 10h | 10h | 10h |
| | ADC Gain Factor | 1A16h | 2 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| | ADC Offset | 1A18h | 2 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| | ADC 15T30 | 1A1Ah | 2 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| | ADC 15T85 | 1A1Ch | 2 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| | ADC 20T30 | 1A1Eh | 2 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| | ADC 20T85 | 1A20h | 2 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| | ADC 25T30 | 1A22h | 2 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| ADC 25T85 | 1A24h | 2 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit | |

Table 103. F674x1 Device Descriptor Table

| | Description | Address | Size in bytes | F674911PEU F674911PZ | F674811PEU F674811PZ | F674711PEU F674711PZ | F674611PEU F674611PZ | F674511PEU F674511PZ |
|------------|-------------------|---------|---------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| | | | | Value | Value | Value | Value | Value |
| Info Block | Info Length | 1A00h | 1 | 06h | 06h | 06h | 06h | 06h |
| | CRC Length | 1A01h | 1 | 06h | 06h | 06h | 06h | 06h |
| | CRC Value | 1A02h | 2 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| | Device ID | 1A04h | 2 | 819Bh | 819Ah | 8199h | 8198h | 8197h |
| | Hardware Revision | 1A06h | 1 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| | Firmware Revision | 1A07h | 1 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| Die Record | Die Record Tag | 1A08h | 1 | 08h | 08h | 08h | 08h | 08h |
| | Die Record Length | 1A09h | 1 | 0Ah | 0Ah | 0Ah | 0Ah | 0Ah |
| | Lot ID | 1A0Ah | 4 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| | X Position | 1A0Eh | 2 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| | Y Position | 1A10h | 2 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| | Test Record CP | 1A12h | 1 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| | Test Record FT | 1A13h | 1 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |

Table 103. F674x1 Device Descriptor Table (continued)

| | | | | | | | | |
|----------------------|------------------------------|-------|---|----------|----------|----------|----------|----------|
| ADC10 Calibration | ADC Calibration Tag | 1A14h | 1 | 13h | 13h | 13h | 13h | 13h |
| | ADC Calibration Length | 1A15h | 1 | 10h | 10h | 10h | 10h | 10h |
| | ADC Gain Factor | 1A16h | 2 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| | ADC Offset | 1A18h | 2 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| | ADC 15T30 | 1A1Ah | 2 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| | ADC 15T85 | 1A1Ch | 2 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| | ADC 20T30 | 1A1Eh | 2 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| | ADC 20T85 | 1A20h | 2 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| | ADC 25T30 | 1A22h | 2 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |
| | ADC 25T85 | 1A24h | 2 | Per Unit | Per Unit | Per Unit | Per Unit | Per Unit |

REVISION HISTORY

| REVISION | DESCRIPTION |
|----------|---|
| SLAS815 | Production Data release |
| SLAS815A | <p>Made editorial changes to Features.</p> <p>Recommended Operating Conditions, Added TYP test conditions.</p> <p>Active Mode Supply Current Into V_{CC} Excluding External Current, Updated current values.</p> <p>Auxiliary Supplies - AUX3 (Backup Subsystem) Currents, Changed I_{AUX3,RTCOFF} at 85°C.</p> <p>DCO Frequency, Added note (1).</p> <p>Flash Memory, Updated Flash program and erase currents.</p> |
| SLAS815B | <p>Table 5, Corrected pin number for P2.6/PM_UCB0SIMO/PM_UCB0SDA/R03.</p> <p>10-Bit ADC External Reference, Note (1), changed "12-bit accuracy" to "10-bit accuracy".</p> |
| SLAS815C | <p>Features, Removed mention of encryption (does not apply to these devices).</p> <p>Added Applications.</p> <p>Removed Ordering Information table (see PACKAGE OPTION ADDENDUM at end of data sheet).</p> <p>Table 4 and Table 5, Added note to $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ pin.</p> <p>Added Development Tools Support and Device and Development Tool Nomenclature.</p> <p>Schmitt-Trigger Inputs – General Purpose I/O, Added note to R_{PULL}.</p> <p>Comparator_B, Corrected test conditions for I_{AVCC_REF}.</p> |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| MSP430F67451IPEU | ACTIVE | LQFP | PEU | 128 | 72 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67451 | Samples |
| MSP430F67451IPEUR | ACTIVE | LQFP | PEU | 128 | 750 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67451 | Samples |
| MSP430F67451IPZ | ACTIVE | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67451 | Samples |
| MSP430F67451IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67451 | Samples |
| MSP430F67461IPEU | ACTIVE | LQFP | PEU | 128 | 72 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67461 | Samples |
| MSP430F67461IPEUR | ACTIVE | LQFP | PEU | 128 | 750 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67461 | Samples |
| MSP430F67461IPZ | ACTIVE | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67461 | Samples |
| MSP430F67461IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67461 | Samples |
| MSP430F67471IPEU | ACTIVE | LQFP | PEU | 128 | 72 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67471 | Samples |
| MSP430F67471IPEUR | ACTIVE | LQFP | PEU | 128 | 750 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67471 | Samples |
| MSP430F67471IPZ | ACTIVE | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67471 | Samples |
| MSP430F67471IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67471 | Samples |
| MSP430F67481IPEU | ACTIVE | LQFP | PEU | 128 | 72 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67481 | Samples |
| MSP430F67481IPEUR | ACTIVE | LQFP | PEU | 128 | 750 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67481 | Samples |
| MSP430F67481IPZ | ACTIVE | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67481 | Samples |
| MSP430F67481IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67481 | Samples |
| MSP430F67491IPEU | ACTIVE | LQFP | PEU | 128 | 72 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67491 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| MSP430F67491IPEUR | ACTIVE | LQFP | PEU | 128 | 750 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67491 | Samples |
| MSP430F67491IPZ | ACTIVE | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67491 | Samples |
| MSP430F67491IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67491 | Samples |
| MSP430F67651IPEU | ACTIVE | LQFP | PEU | 128 | 72 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67651 | Samples |
| MSP430F67651IPEUR | ACTIVE | LQFP | PEU | 128 | 750 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67651 | Samples |
| MSP430F67651IPZ | ACTIVE | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67651 | Samples |
| MSP430F67651IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67651 | Samples |
| MSP430F67661IPEU | ACTIVE | LQFP | PEU | 128 | 72 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67661 | Samples |
| MSP430F67661IPEUR | ACTIVE | LQFP | PEU | 128 | 750 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67661 | Samples |
| MSP430F67661IPZ | ACTIVE | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67661 | Samples |
| MSP430F67661IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67661 | Samples |
| MSP430F67671IPEU | ACTIVE | LQFP | PEU | 128 | 72 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67671 | Samples |
| MSP430F67671IPEUR | ACTIVE | LQFP | PEU | 128 | 750 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67671 | Samples |
| MSP430F67671IPZ | ACTIVE | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67671 | Samples |
| MSP430F67671IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67671 | Samples |
| MSP430F67681IPEU | ACTIVE | LQFP | PEU | 128 | 72 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67681 | Samples |
| MSP430F67681IPEUR | ACTIVE | LQFP | PEU | 128 | 750 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67681 | Samples |
| MSP430F67681IPZ | ACTIVE | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67681 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| MSP430F67681IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67681 | Samples |
| MSP430F67691IPEU | ACTIVE | LQFP | PEU | 128 | 72 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67691 | Samples |
| MSP430F67691IPEUR | ACTIVE | LQFP | PEU | 128 | 750 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67691 | Samples |
| MSP430F67691IPZ | ACTIVE | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67691 | Samples |
| MSP430F67691IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67691 | Samples |
| MSP430F67751IPEU | ACTIVE | LQFP | PEU | 128 | 72 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67751 | Samples |
| MSP430F67751IPEUR | ACTIVE | LQFP | PEU | 128 | 750 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67751 | Samples |
| MSP430F67751IPZ | ACTIVE | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67751 | Samples |
| MSP430F67751IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67751 | Samples |
| MSP430F67761IPEU | ACTIVE | LQFP | PEU | 128 | 72 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67761 | Samples |
| MSP430F67761IPEUR | ACTIVE | LQFP | PEU | 128 | 750 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67761 | Samples |
| MSP430F67761IPZ | ACTIVE | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67761 | Samples |
| MSP430F67761IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67761 | Samples |
| MSP430F67771IPEU | ACTIVE | LQFP | PEU | 128 | 72 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67771 | Samples |
| MSP430F67771IPEUR | ACTIVE | LQFP | PEU | 128 | 750 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67771 | Samples |
| MSP430F67771IPZ | ACTIVE | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67771 | Samples |
| MSP430F67771IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67771 | Samples |
| MSP430F67781IPEU | ACTIVE | LQFP | PEU | 128 | 72 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67781 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| MSP430F67781IPEUR | ACTIVE | LQFP | PEU | 128 | 750 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67781 | Samples |
| MSP430F67781IPZ | ACTIVE | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67781 | Samples |
| MSP430F67781IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67781 | Samples |
| MSP430F67791IPEU | ACTIVE | LQFP | PEU | 128 | 72 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67791 | Samples |
| MSP430F67791IPEUR | ACTIVE | LQFP | PEU | 128 | 750 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67791 | Samples |
| MSP430F67791IPZ | ACTIVE | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67791 | Samples |
| MSP430F67791IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | | F67791 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

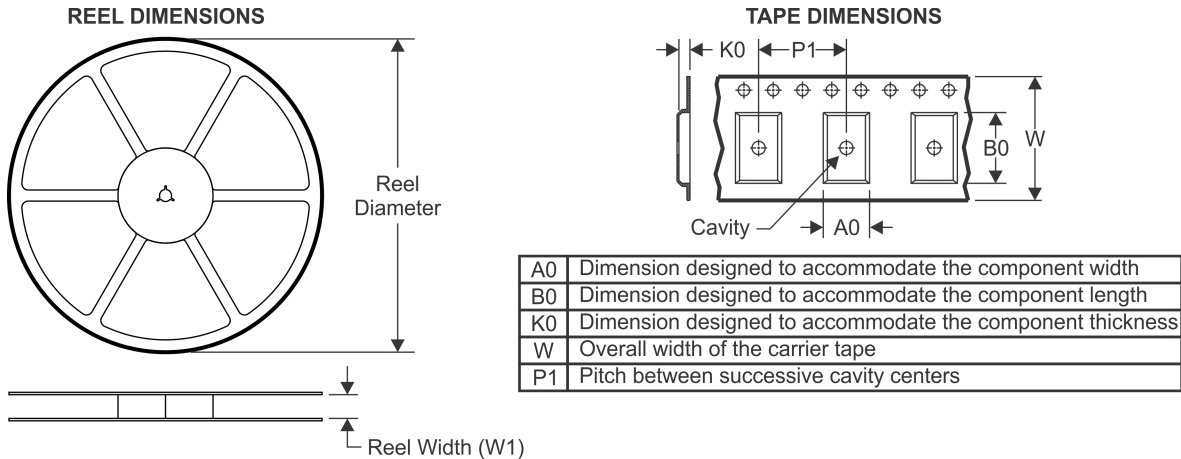
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

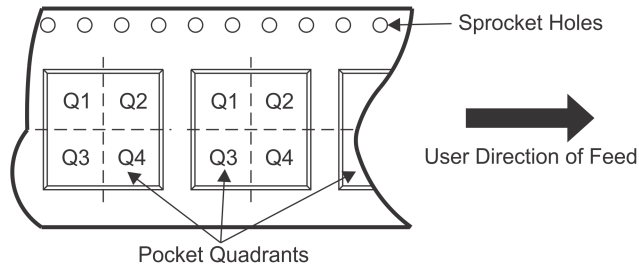
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TAPE AND REEL INFORMATION



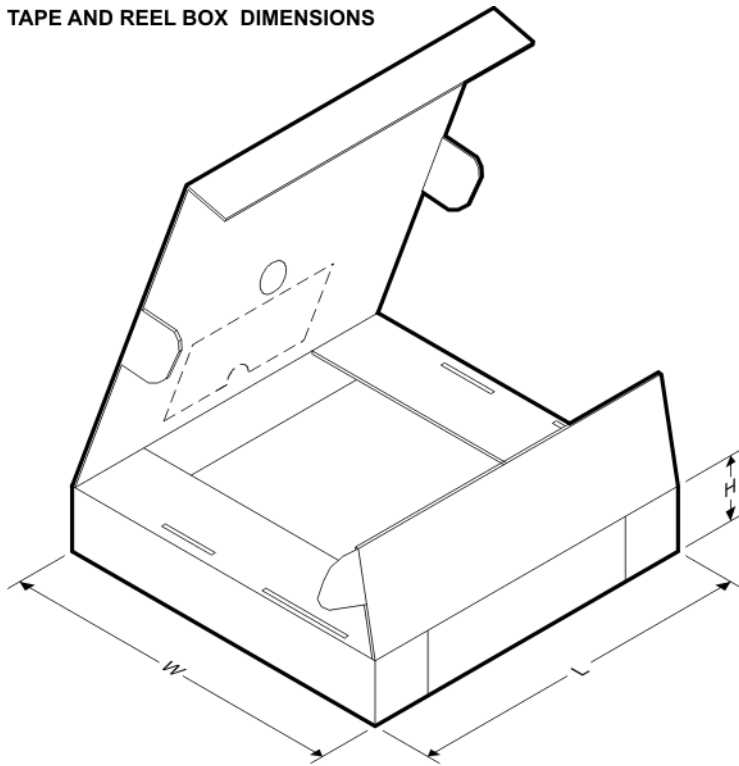
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MSP430F67451IPEUR | LQFP | PEU | 128 | 750 | 330.0 | 44.4 | 17.0 | 23.0 | 2.25 | 24.0 | 44.0 | Q1 |
| MSP430F67451IPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F67461IPEUR | LQFP | PEU | 128 | 750 | 330.0 | 44.4 | 17.0 | 23.0 | 2.25 | 24.0 | 44.0 | Q1 |
| MSP430F67461IPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F67471IPEUR | LQFP | PEU | 128 | 750 | 330.0 | 44.4 | 17.0 | 23.0 | 2.25 | 24.0 | 44.0 | Q1 |
| MSP430F67471IPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F67481IPEUR | LQFP | PEU | 128 | 750 | 330.0 | 44.4 | 17.0 | 23.0 | 2.25 | 24.0 | 44.0 | Q1 |
| MSP430F67481IPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F67491IPEUR | LQFP | PEU | 128 | 750 | 330.0 | 44.4 | 17.0 | 23.0 | 2.25 | 24.0 | 44.0 | Q1 |
| MSP430F67491IPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F67651IPEUR | LQFP | PEU | 128 | 750 | 330.0 | 44.4 | 17.0 | 23.0 | 2.25 | 24.0 | 44.0 | Q1 |
| MSP430F67651IPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F67661IPEUR | LQFP | PEU | 128 | 750 | 330.0 | 44.4 | 17.0 | 23.0 | 2.25 | 24.0 | 44.0 | Q1 |
| MSP430F67661IPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F67671IPEUR | LQFP | PEU | 128 | 750 | 330.0 | 44.4 | 17.0 | 23.0 | 2.25 | 24.0 | 44.0 | Q1 |
| MSP430F67671IPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F67681IPEUR | LQFP | PEU | 128 | 750 | 330.0 | 44.4 | 17.0 | 23.0 | 2.25 | 24.0 | 44.0 | Q1 |
| MSP430F67681IPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MSP430F67691IPEUR | LQFP | PEU | 128 | 750 | 330.0 | 44.4 | 17.0 | 23.0 | 2.25 | 24.0 | 44.0 | Q1 |
| MSP430F67691IPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F67751IPEUR | LQFP | PEU | 128 | 750 | 330.0 | 44.4 | 17.0 | 23.0 | 2.25 | 24.0 | 44.0 | Q1 |
| MSP430F67751IPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F67761IPEUR | LQFP | PEU | 128 | 750 | 330.0 | 44.4 | 17.0 | 23.0 | 2.25 | 24.0 | 44.0 | Q1 |
| MSP430F67761IPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F67771IPEUR | LQFP | PEU | 128 | 750 | 330.0 | 44.4 | 17.0 | 23.0 | 2.25 | 24.0 | 44.0 | Q1 |
| MSP430F67771IPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F67781IPEUR | LQFP | PEU | 128 | 750 | 330.0 | 44.4 | 17.0 | 23.0 | 2.25 | 24.0 | 44.0 | Q1 |
| MSP430F67781IPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F67791IPEUR | LQFP | PEU | 128 | 750 | 330.0 | 44.4 | 17.0 | 23.0 | 2.25 | 24.0 | 44.0 | Q1 |
| MSP430F67791IPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


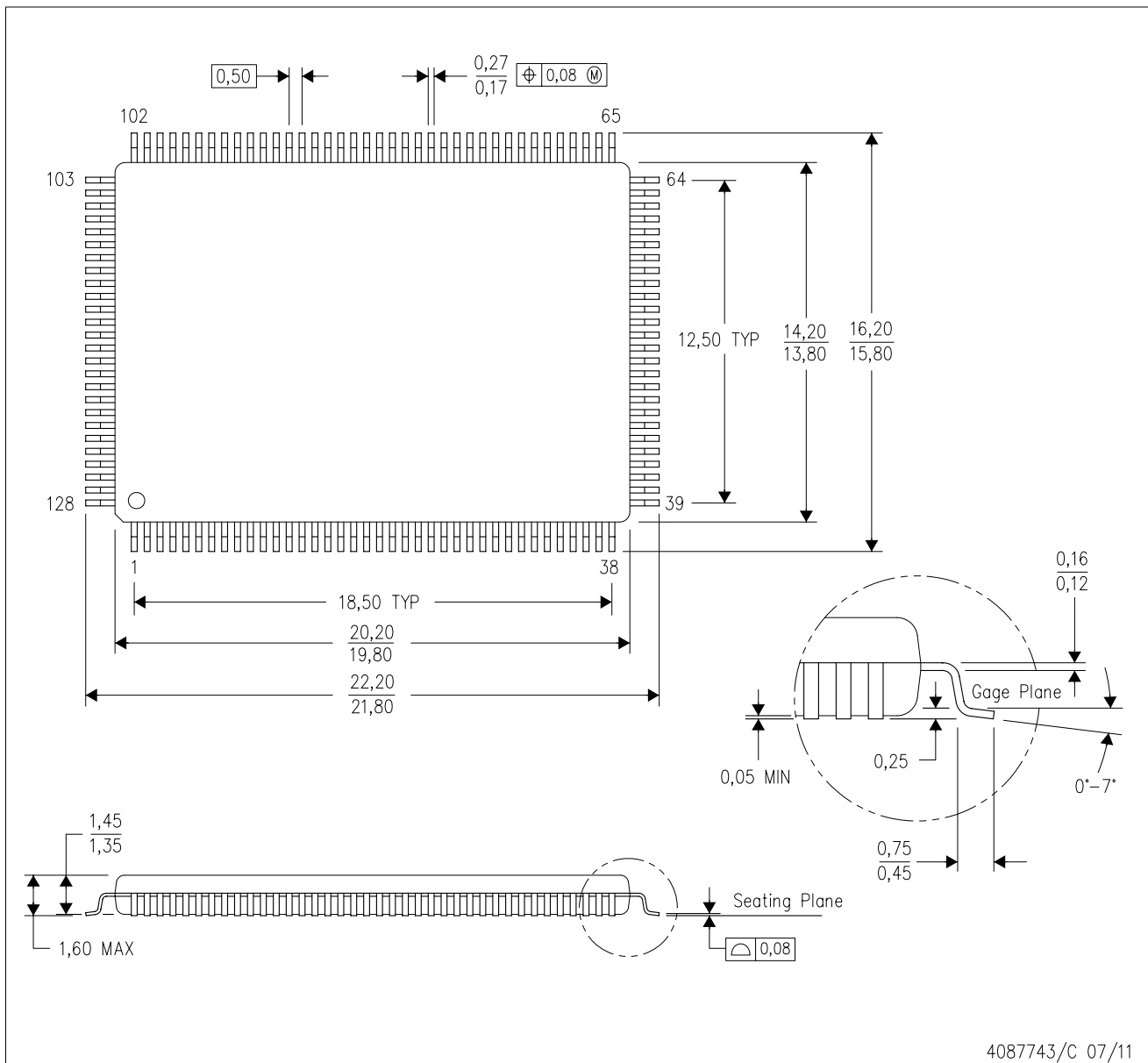
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| MSP430F67451IPEUR | LQFP | PEU | 128 | 750 | 367.0 | 367.0 | 67.0 |
| MSP430F67451IPZR | LQFP | PZ | 100 | 1000 | 367.0 | 367.0 | 45.0 |
| MSP430F67461IPEUR | LQFP | PEU | 128 | 750 | 367.0 | 367.0 | 67.0 |
| MSP430F67461IPZR | LQFP | PZ | 100 | 1000 | 367.0 | 367.0 | 45.0 |
| MSP430F67471IPEUR | LQFP | PEU | 128 | 750 | 367.0 | 367.0 | 67.0 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| MSP430F67471IPZR | LQFP | PZ | 100 | 1000 | 367.0 | 367.0 | 45.0 |
| MSP430F67481IPEUR | LQFP | PEU | 128 | 750 | 367.0 | 367.0 | 67.0 |
| MSP430F67481IPZR | LQFP | PZ | 100 | 1000 | 367.0 | 367.0 | 45.0 |
| MSP430F67491IPEUR | LQFP | PEU | 128 | 750 | 367.0 | 367.0 | 67.0 |
| MSP430F67491IPZR | LQFP | PZ | 100 | 1000 | 367.0 | 367.0 | 45.0 |
| MSP430F67651IPEUR | LQFP | PEU | 128 | 750 | 367.0 | 367.0 | 67.0 |
| MSP430F67651IPZR | LQFP | PZ | 100 | 1000 | 367.0 | 367.0 | 45.0 |
| MSP430F67661IPEUR | LQFP | PEU | 128 | 750 | 367.0 | 367.0 | 67.0 |
| MSP430F67661IPZR | LQFP | PZ | 100 | 1000 | 367.0 | 367.0 | 45.0 |
| MSP430F67671IPEUR | LQFP | PEU | 128 | 750 | 367.0 | 367.0 | 67.0 |
| MSP430F67671IPZR | LQFP | PZ | 100 | 1000 | 367.0 | 367.0 | 45.0 |
| MSP430F67681IPEUR | LQFP | PEU | 128 | 750 | 367.0 | 367.0 | 67.0 |
| MSP430F67681IPZR | LQFP | PZ | 100 | 1000 | 367.0 | 367.0 | 45.0 |
| MSP430F67691IPEUR | LQFP | PEU | 128 | 750 | 367.0 | 367.0 | 67.0 |
| MSP430F67691IPZR | LQFP | PZ | 100 | 1000 | 367.0 | 367.0 | 45.0 |
| MSP430F67751IPEUR | LQFP | PEU | 128 | 750 | 367.0 | 367.0 | 67.0 |
| MSP430F67751IPZR | LQFP | PZ | 100 | 1000 | 367.0 | 367.0 | 45.0 |
| MSP430F67761IPEUR | LQFP | PEU | 128 | 750 | 367.0 | 367.0 | 67.0 |
| MSP430F67761IPZR | LQFP | PZ | 100 | 1000 | 367.0 | 367.0 | 45.0 |
| MSP430F67771IPEUR | LQFP | PEU | 128 | 750 | 367.0 | 367.0 | 67.0 |
| MSP430F67771IPZR | LQFP | PZ | 100 | 1000 | 367.0 | 367.0 | 45.0 |
| MSP430F67781IPEUR | LQFP | PEU | 128 | 750 | 367.0 | 367.0 | 67.0 |
| MSP430F67781IPZR | LQFP | PZ | 100 | 1000 | 367.0 | 367.0 | 45.0 |
| MSP430F67791IPEUR | LQFP | PEU | 128 | 750 | 367.0 | 367.0 | 67.0 |
| MSP430F67791IPZR | LQFP | PZ | 100 | 1000 | 367.0 | 367.0 | 45.0 |

PEU (R-PQFP-G128)

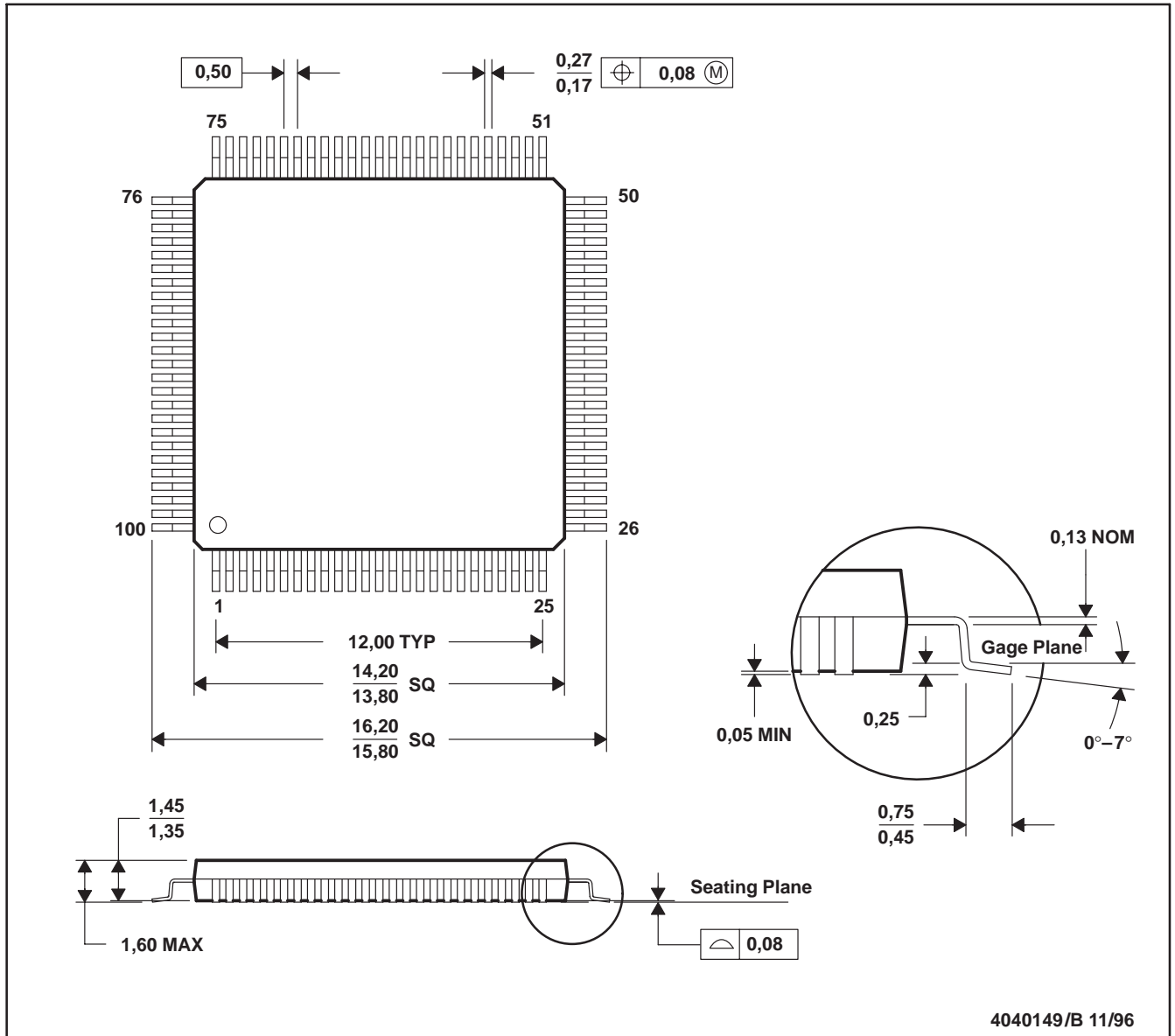
PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-026

PZ (S-PQFP-G100)

PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-026

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