SBAS323G − JUNE 2004 − REVISED OCTOBER 2007

Precision Analog-to-Digital Converter (ADC) and Digital-to-Analog Converters (DACs) with 8051 Microcontroller and Flash Memory

FEATURES

ANALOG FEATURES

- 24 Bits No Missing Codes
- 22 Bits Effective Resolution at 10Hz
  - Low Noise: 75nV
- PGA From 1 to 128
- Precision On-Chip Voltage Reference
  - Accuracy: 0.2%
  - Drift: 5ppm/°C
- 8 Differential/Single-Ended Channels
- On-Chip Offset/Gain Calibration
- Offset Drift: 0.1ppm/°C
- Gain Drift: 0.5ppm/°C
- On-Chip Temperature Sensor
- Selectable Buffer Input
- Burnout Detect
- 16-Bit Monotonic Voltage DACS:
  - Quad Voltage DACs (MSC1211, MSC1212)
  - Dual Voltage DACs (MSC1213, MSC1214)

DIGITAL FEATURES

Microcontroller Core

- 8051-Compatible
- High-Speed Core
  - 4 Clocks per Instruction Cycle
- DC to 40MHz at +85°C
- Single Instruction 100ns
- Dual Data Pointer

Memory

- Up To 32kB Flash Memory
- Flash Memory Partitioning
- Endurance 1M Erase/Write Cycles, 100-Year Data Retention
- In-System Serially Programmable
- External Program/Data Memory (64kB)
- 1,280 Bytes Data SRAM
- Flash Memory Security
- 2kB Boot ROM
- Programmable Wait State Control

Peripheral Features

- 34 I/O Pins
- Additional 32-Bit Accumulator
- Three 16-Bit Timer/Counters
- System Timers
- Programmable Watchdog Timer
- Full-Duplex Dual USARTs
- Master/Slave SPI™ with DMA
- Multi-master I²C™ (MSC1211 and MSC1213)
- 16-Bit PWM
- Power Management Control
- Internal Clock Divider
- Idle Mode Current < 200μA
- Stop Mode Current < 100nA
- Programmable Brownout Reset
- Programmable Low-Voltage Detect
- 24 Interrupt Sources
- Two Hardware Breakpoints

GENERAL FEATURES

- Pin-Compatible with MSC1210
- Package: TQFP-64
- Low Power: 4mW
- Industrial Temperature Range: −40°C to +125°C
- Power Supply: 2.7V to 5.25V

APPLICATIONS

- Industrial Process Control
- Instrumentation
- Liquid/Gas Chromatography
- Blood Analysis
- Smart Transmitters
- Portable Instruments
- Weigh Scales
- Pressure Transducers
- Intelligent Sensors
- Portable Applications
- DAS Systems

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PACKAGE/ORDERING INFORMATION(1)

PRODUCT	FLASH MEMORY	16-BIT DACS	I^2C	PACKAGE MARKING
MSC1211Y2	4k	4	Y	MSC1211Y2
MSC1211Y3	8k	4	Y	MSC1211Y3
MSC1211Y4	16k	4	Y	MSC1211Y4
MSC1211Y5	32k	4	Y	MSC1211Y5
MSC1212Y2	4k	4	N	MSC1212Y2
MSC1212Y3	8k	4	N	MSC1212Y3
MSC1212Y4	16k	4	N	MSC1212Y4
MSC1212Y5	32k	4	N	MSC1212Y4
MSC1213Y2	4k	2	Y	MSC1213Y2
MSC1213Y3	8k	2	Y	MSC1213Y3
MSC1213Y4	16k	2	Y	MSC1213Y4
MSC1213Y5	32k	2	Y	MSC1213Y5
MSC1214Y2	4k	2	N	MSC1214Y2
MSC1214Y3	8k	2	N	MSC1214Y3
MSC1214Y4	16k	2	N	MSC1214Y4
MSC1214Y5	32k	2	N	MSC1214Y5

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this datasheet, or refer to our web site at www.ti.com.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

			MSC1211/12/13/14	UNITS
Analog Inputs				
Input current	Momentary		100	mA
	Continuous		10	mA
Input voltage			AGND − 0.3 to AV_{DD} + 0.3	V
Power Supply				
DV_{DD} to DGND			−0.3 to +6	V
AV_{DD} to AGND			−0.3 to +6	V
AGND to DGND			−0.3 to +0.3	V
V_{REF} to AGND			−0.3 to AV_{DD} + 0.3	V
Digital input voltage to DGND			−0.3 to DV_{DD} + 0.3	V
Digital output voltage to DGND			−0.3 to DV_{DD} + 0.3	V
Maximum junction temperature (T_J Max)			+150	°C
Operating temperature range			−40 to +125	°C
Storage temperature range			−65 to +150	°C
Thermal resistance	Junction to ambient (θ_{JA})	High K (2s 2p)	48.9	°C/W
		Low K (1s)	72.9	°C/W
	Junction to case (θ_{JC})		12.2	°C/W
Package power dissipation			(T_J Max − $T_{AMBIENT}$)/θ_{JA}	W
Output current, all pins			200	mA
Output pin short-circuit			10	s
Digital Outputs				
Output current	Continuous		100	mA
I/O source/sink current			100	mA
Power pin maximum			300	mA

(1) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

MSC121xYX FAMILY FEATURES

FEATURES(1)	MSC121xY2(2)	MSC121xY3(2)	MSC121xY4(2)	MSC121xY5(2)
Flash Program Memory (Bytes)	Up to 4k	Up to 8k	Up to 16k	Up to 32k
Flash Data Memory (Bytes)	Up to 4k	Up to 8k	Up to 16k	Up to 32k
Internal Scratchpad SRAM (Bytes)	256	256	256	256
Internal MOVX RAM (Bytes)	1024	1024	1024	1024
Externally Accessible Memory (Bytes)	64k Program, 64k Data	64k Program, 64k Data	64k Program, 64k Data	64k Program, 64k Data

(1) All peripheral features are the same on all devices; the flash memory size is the only difference.
(2) The last digit of the part number (*N*) represents the onboard flash size = (2^N)kBytes.

ELECTRICAL CHARACTERISTICS: AV_{DD} = 5V

All specifications from T_{MIN} to T_{MAX}, DV_{DD} = +2.7V to 5.25V, AV_{DD} = +5V, f_{MOD} = 15.625kHz, PGA = 1, filter = Sinc^3, Buffer ON, f_{DATA} = 10Hz, Bipolar, f_{CLK} = 8MHz, and V_{REF} ≡ (REF IN+) − (REF IN−) = +2.5V, unless otherwise noted. For V_{DAC}, V_{REF} = AV_{DD}, R_{LOAD} = 10kΩ, and C_{LOAD} = 200pF, unless otherwise noted.

PARAMETER		CONDITIONS	MSC1211/12/13/14 MIN	TYP	MAX	UNITS
Analog Inputs (AIN0−AIN7, AINCOM)						
Analog Input Range		Buffer OFF	AGND − 0.1		AV_{DD} + 0.1	V
		Buffer ON	AGND + 50mV		AV_{DD} − 1.5	V
Full-Scale Input Voltage Range		(AIN+) − (AIN−)			$\pm V_{REF}$/PGA	V
Differential Input Impedance		Buffer OFF		7/PGA(1)		MΩ
Input Current		Buffer ON		0.5		nA
Bandwidth	Fast Settling Filter	−3dB		0.469 • f_{DATA}		
	Sinc^2 Filter	−3dB		0.318 • f_{DATA}		
	Sinc^3 Filter	−3dB		0.262 • f_{DATA}		
Programmable Gain Amplifier		User-Selectable Gain Range	1		128	
Input Capacitance		Buffer ON		9		pF
Input Leakage Current		Multiplexer Channel OFF, T = +25°C		0.5		pA
Burnout Current Sources		Buffer ON		±2		µA
ADC Offset DAC						
Offset DAC Range		Bipolar Mode		$\pm V_{REF}$/(2 • PGA)		V
Offset DAC Monotonicity			8			Bits
Offset DAC Gain Error				±1.5		% of Range
Offset DAC Gain Error Drift				1		ppm/°C
System Performance						
Resolution			24			Bits
ENOB		See Typical Characteristics		22		Bits
Output Noise			See Typical Characteristics			
No Missing Codes		Sinc^3 Filter, Decimation > 360	24			Bits
Integral Nonlinearity		End Point Fit, Bipolar Mode		0.0003	±0.0015	%FSR
Offset Error		After Calibration		±3.5		ppm of FS
Offset Drift(2)		Before Calibration		0.1		ppm of FS/°C
Gain Error(3)		After Calibration		−0.002		%
Gain Error Drift(2)		Before Calibration		0.5		ppm/°C
System Gain Calibration Range			80		120	% of FS
System Offset Calibration Range			−50		50	% of FS
Common-Mode Rejection		At DC		115		dB
		f_{CM} = 60Hz, f_{DATA} = 10Hz		130		dB
		f_{CM} = 50HZ, f_{DATA} = 50Hz		120		dB
		f_{CM} = 60Hz, f_{DATA} = 60Hz		120		dB
Normal-Mode Rejection		f_{SIG} = 50Hz, f_{DATA} = 50Hz		100		dB
		f_{SIG} = 60Hz, f_{DATA} = 60Hz		100		dB
Power-Supply Rejection		At DC, dB = −20log(ΔVOUT/ΔV_{DD})(4)		92		dB

(1) The input impedance for PGA = 128 is the same as that for PGA = 64 (that is, 7MΩ/64).
(2) Calibration can minimize these errors.
(3) The self gain calibration cannot have a REF IN+ of more than AV_{DD} −1.5V with Buffer ON. To calibrate gain, turn Buffer OFF.
(4) ΔV_{OUT} is change in digital result.
(5) 9pF switched capacitor at f_{SAMP} clock frequency (see Figure 14).
(6) Linearity calculated using a reduced code range of 512 to 65024; output unloaded.
(7) Ensured by design and characterization; not production tested.
(8) Analog Brownout Detect OFF (HCR1.3 = 1), Analog LVD OFF (LVDCON.7 = 1).

ELECTRICAL CHARACTERISTICS: AV_{DD} = 5V (continued)

All specifications from T_{MIN} to T_{MAX}, DV_{DD} = +2.7V to 5.25V, AV_{DD} = +5V, f_{MOD} = 15.625kHz, PGA = 1, filter = Sinc3, Buffer ON, f_{DATA} = 10Hz, Bipolar, f_{CLK} = 8MHz, and V_{REF} ≡ (REF IN+) − (REF IN−) = +2.5V, unless otherwise noted. For V_{DAC}, V_{REF} = AV_{DD}, R_{LOAD} = 10kΩ, and C_{LOAD} = 200pF, unless otherwise noted.

PARAMETER	CONDITIONS	MSC1211/12/13/14			UNITS
		MIN	TYP	MAX	
Voltage Reference Inputs					
Reference Input Range	REF IN+, REF IN−	AGND		AV_{DD}(3)	V
V_{REF}	V_{REF} ≡ (REF IN+) − (REF IN−)	0.1	2.5	AV_{DD}	V
V_{REF} Common-Mode Rejection	At DC		110		dB
Input Current(5)	V_{REF} = 2.5V, ADC Only		1		µA
DAC Reference Input Resistance	For Each DAC, PGA = 1		20		kΩ
On-Chip Voltage Reference					
Output Voltage	VREFH = 1 at +25°C, REFCLK = 250kHz	2.495	2.5	2.505	V
	VREFH = 0 at +25°C, REFCLK = 250kHz		1.25		V
Power-Supply Rejection Ratio			65		dB
Short-Circuit Current Source			2.6		mA
Short-Circuit Current Sink			50		µA
Short-Circuit Duration	Sink or Source		Indefinite		
Drift			5		ppm/°C
Output Impedance	Sourcing 100µA		3		Ω
Startup Time from Power ON	C_{REFOUT} = 0.1µF		8		ms
Temperature Sensor Voltage	Buffer ON, T = +25°C		115		mV
Temperature Sensor Coefficient	Buffer ON		375		µV/°C
Voltage DAC Static Performance(6)					
Resolution		16			Bits
Relative Accuracy			±0.05	±0.146	%FSR
Differential Nonlinearity	Ensured Monotonic by Design			±1	LSB
Zero Code Error	All 0s Loaded to DAC Register		+13	+35	mV
Full-Scale Error	All 1s Loaded to DAC Register	−1.25	0		% of FSR
Gain Error		−1.25	0	+1.25	% of FSR
Zero Code Error Drift			±20		µV/°C
Gain Temperature Coefficient			±5		ppm of FSR/°C
Voltage DAC Output Characteristics(7)					
Output Voltage Range	REF IN+ = AV_{DD}	AGND		AV_{DD}	V
Output Voltage Settling Time	To ±0.003% FSR, 0200h to FD00h		8		µs
Slew Rate			1		V/µs
DC Output Impedance			7		Ω
Short-Circuit Current	All 1s Loaded to DAC Register		20		mA
IDAC Output Characteristics					
Full-Scale Output Current	Maximum V_{REF} = 2.5V		25		mA
Maximum Short-Circuit Current Duration			Indefinite		
Compliance Voltage			AV_{DD} − 1.5		V
Relative Accuracy			0.185		% of FSR
Zero Code Error	All 0s Loaded to DAC Register		0.5		µA
Full-Scale Error	All 1s Loaded to DAC Register		−0.4		% of FSR
Gain Error			−0.6		% of FSR

(1) The input impedance for PGA = 128 is the same as that for PGA = 64 (that is, 7MΩ/64).
(2) Calibration can minimize these errors.
(3) The self gain calibration cannot have a REF IN+ of more than AV_{DD} −1.5V with Buffer ON. To calibrate gain, turn Buffer OFF.
(4) ΔV_{OUT} is change in digital result.
(5) 9pF switched capacitor at f_{SAMP} clock frequency (see Figure 14).
(6) Linearity calculated using a reduced code range of 512 to 65024; output unloaded.
(7) Ensured by design and characterization; not production tested.
(8) Analog Brownout Detect OFF (HCR1.3 = 1), Analog LVD OFF (LVDCON.7 = 1).

ELECTRICAL CHARACTERISTICS: AV_{DD} = 5V (continued)

All specifications from T_{MIN} to T_{MAX}, DV_{DD} = +2.7V to 5.25V, AV_{DD} = +5V, f_{MOD} = 15.625kHz, PGA = 1, filter = Sinc3, Buffer ON, f_{DATA} = 10Hz, Bipolar, f_{CLK} = 8MHz, and $V_{REF} \equiv$ (REF IN+) − (REF IN−) = +2.5V, unless otherwise noted. For V_{DAC}, $V_{REF} = AV_{DD}$, R_{LOAD} = 10kΩ, and C_{LOAD} = 200pF, unless otherwise noted.

PARAMETER		CONDITIONS	MSC1211/12/13/14 MIN	TYP	MAX	UNITS
Analog Power-Supply Requirements						
Analog Power-Supply Voltage		AV_{DD}	4.75	5	5.25	V
Analog Power-Supply Current	Analog Off Current(8)	Analog OFF, PDCON = 48h		< 1		nA
	ADC Current (I_{ADC})	PGA = 1, Buffer OFF		200		µA
		PGA = 128, Buffer OFF		500		µA
		PGA = 1, Buffer ON		240		µA
		PGA = 128, Buffer ON		850		µA
	VDAC Current (I_{VDAC})	Excluding Load Current, External Reference		250		µA
	V_{REF} Supply Current (I_{VREF})	ADC ON, V_{DAC} OFF		250		µA

(1) The input impedance for PGA = 128 is the same as that for PGA = 64 (that is, 7MΩ/64).
(2) Calibration can minimize these errors.
(3) The self gain calibration cannot have a REF IN+ of more than AV_{DD} −1.5V with Buffer ON. To calibrate gain, turn Buffer OFF.
(4) ΔV_{OUT} is change in digital result.
(5) 9pF switched capacitor at f_{SAMP} clock frequency (see Figure 14).
(6) Linearity calculated using a reduced code range of 512 to 65024; output unloaded.
(7) Ensured by design and characterization; not production tested.
(8) Analog Brownout Detect OFF (HCR1.3 = 1), Analog LVD OFF (LVDCON.7 = 1).

ELECTRICAL CHARACTERISTICS: AV_{DD} = 3V

All specifications from T_{MIN} to T_{MAX}, DV_{DD} = +2.7V to 5.25V, AV_{DD} = +3V, f_{MOD} = 15.625kHz, PGA = 1, filter = Sinc3, Buffer ON, f_{DATA} = 10Hz, Bipolar, f_{CLK} = 8MHz, and $V_{REF} \equiv$ (REF IN+) − (REF IN−) = +1.25V, unless otherwise noted. For V_{DAC}, $V_{REF} = AV_{DD}$, R_{LOAD} = 10kΩ, and C_{LOAD} = 200pF, unless otherwise noted.

PARAMETER		CONDITIONS	MSC1211/12/13/14 MIN	TYP	MAX	UNITS
Analog Inputs (AIN0−AIN7, AINCOM)						
Analog Input Range		Buffer OFF	AGND − 0.1		AV_{DD} + 0.1	V
		Buffer ON	AGND + 50mV		AV_{DD} − 1.5	V
Full-Scale Input Voltage Range		(AIN+) − (AIN−)			$\pm V_{REF}$/PGA	V
Differential Input Impedance		Buffer OFF		7/PGA(1)		MΩ
Input Current		Buffer ON		0.5		nA
Bandwidth	Fast Settling Filter	−3dB		0.469 • f_{DATA}		
	Sinc2 Filter	−3dB		0.318 • f_{DATA}		
	Sinc3 Filter	−3dB		0.262 • f_{DATA}		
Programmable Gain Amplifier		User-Selectable Gain Range	1		128	
Input Capacitance		Buffer ON		9		pF
Input Leakage Current		Multiplexer Channel OFF, T = +25°C		0.5		pA
Burnout Current Sources		Sensor Input Open Circuit		±2		µA

(1) The input impedance for PGA = 128 is the same as that for PGA = 64 (that is, 7MΩ/64).
(2) Calibration can minimize these errors.
(3) The gain calibration cannot have a REF IN+ of more than AV_{DD} −1.5V with Buffer ON. To calibrate gain, turn Buffer OFF.
(4) ΔV_{OUT} is change in digital result.
(5) 9pF switched capacitor at f_{SAMP} clock frequency (see Figure 14).
(6) Linearity calculated using a reduced code range of 512 to 65024; output unloaded.
(7) Ensured by design and characterization; not production tested.
(8) Analog Brownout Detect OFF (HCR1.3 = 1), Analog LVD OFF (LVDCON.7 = 1).

ELECTRICAL CHARACTERISTICS: AV_{DD} = 3V (continued)

All specifications from T_{MIN} to T_{MAX}, DV_{DD} = +2.7V to 5.25V, AV_{DD} = +3V, f_{MOD} = 15.625kHz, PGA = 1, filter = Sinc3, Buffer ON, f_{DATA} = 10Hz, Bipolar, f_{CLK} = 8MHz, and $V_{REF} \equiv$ (REF IN+) − (REF IN−) = +1.25V, unless otherwise noted. For V_{DAC}, V_{REF} = AV_{DD}, R_{LOAD} = 10kΩ, and C_{LOAD} = 200pF, unless otherwise noted.

PARAMETER	CONDITIONS	MSC1211/12/13/14			UNITS
		MIN	TYP	MAX	
ADC Offset DAC					
Offset DAC Range	Bipolar Mode		$\pm V_{REF}/(2 \bullet PGA)$		V
Offset DAC Monotonicity		8			Bits
Offset DAC Gain Error			±1.5		% of Range
Offset DAC Gain Error Drift			1		ppm/°C
System Performance					
Resolution		24			Bits
ENOB			22		Bits
Output Noise		See Typical Characteristics			
No Missing Codes	Sinc3 Filter	24			Bits
Integral Nonlinearity	End Point Fit, Bipolar Mode		0.0003	±0.0015	%FSR
Offset Error	After Calibration		±3.5		ppm of FS
Offset Drift(2)	Before Calibration		0.1		ppm of FS/°C
Gain Error(3)	After Calibration		−0.002		%
Gain Error Drift(2)	Before Calibration		1.0		ppm/°C
System Gain Calibration Range		80		120	% of FS
System Offset Calibration Range		−50		50	% of FS
Common-Mode Rejection	At DC		115		dB
	f_{CM} = 60Hz, f_{DATA} = 10Hz		130		dB
	f_{CM} = 50Hz, f_{DATA} = 50Hz		120		dB
	f_{CM} = 60Hz, f_{DATA} = 60Hz		120		dB
Normal Mode Rejection	f_{SIG} = 50Hz, f_{DATA} = 50Hz		100		dB
	f_{SIG} = 60Hz, f_{DATA} = 60Hz		100		dB
Power-Supply Rejection	At DC, dB = $-20\log(\Delta VOUT/\Delta V_{DD})$(4)		92		dB
Voltage Reference Inputs					
Reference Input Range	REF IN+, REF IN−	AGND		AV_{DD}(3)	V
V_{REF}	$V_{REF} \equiv$ (REF IN+) − (REF IN−)	0.1	1.25	AV_{DD}	V
V_{REF} Common-Mode Rejection	At DC		110		dB
Input Current(5)	V_{REF} = 1.25V, ADC Only		3		µA
DAC Reference Input Resistance	For Each DAC, PGA = 1		20		kΩ
On-Chip Voltage Reference					
Output Voltage	VREFH = 0 at +25°C, REFCLK = 250kHz	1.245	1.25	1.255	V
Power-Supply Rejection Ratio			65		dB
Short-Circuit Current Source			2.6		mA
Short-Circuit Current Sink			50		µA
Short-Circuit Duration	Sink or Source		Indefinite		
Drift			5		ppm/°C
Output Impedance	Sourcing 100µA		3		Ω
Startup Time from Power ON	C_{REFOUT} = 0.1µF		8		ms
Temperature Sensor Voltage	Buffer ON, T = +25°C		115		mV
Temperature Sensor Coefficient	Buffer ON		375		µV/°C

(1) The input impedance for PGA = 128 is the same as that for PGA = 64 (that is, 7MΩ/64).
(2) Calibration can minimize these errors.
(3) The gain calibration cannot have a REF IN+ of more than AV_{DD} −1.5V with Buffer ON. To calibrate gain, turn Buffer OFF.
(4) ΔV_{OUT} is change in digital result.
(5) 9pF switched capacitor at f_{SAMP} clock frequency (see Figure 14).
(6) Linearity calculated using a reduced code range of 512 to 65024; output unloaded.
(7) Ensured by design and characterization; not production tested.
(8) Analog Brownout Detect OFF (HCR1.3 = 1), Analog LVD OFF (LVDCON.7 = 1).

ELECTRICAL CHARACTERISTICS: AV_{DD} = 3V (continued)

All specifications from T_{MIN} to T_{MAX}, DV_{DD} = +2.7V to 5.25V, AV_{DD} = +3V, f_{MOD} = 15.625kHz, PGA = 1, filter = $Sinc^3$, Buffer ON, f_{DATA} = 10Hz, Bipolar, f_{CLK} = 8MHz, and V_{REF} ≡ (REF IN+) − (REF IN−) = +1.25V, unless otherwise noted. For V_{DAC}, V_{REF} = AV_{DD}, R_{LOAD} = 10kΩ, and C_{LOAD} = 200pF, unless otherwise noted.

PARAMETER		CONDITIONS	MSC1211/12/13/14 MIN	TYP	MAX	UNITS
Voltage DAC Static Performance(6)						
Resolution			16			Bits
Relative Accuracy				±0.05	±0.146	% of FSR
Differential Nonlinearity		Ensured Monotonic by Design			±1	LSB
Zero Code Error		All 0s Loaded to DAC Register		+13	+35	mV
Full-Scale Error		All 1s Loaded to DAC Register	−1.25	0		% of FSR
Gain Error			−1.25	0	±1.25	% of FSR
Zero Code Error Drift				±20		µV/°C
Gain Temperature Coefficient				±5		ppm of FSR/°C
Voltage DAC Output Characteristics(7)						
Output Voltage Range			AGND		AV_{DD}	V
Output Voltage Settling Time		To ±0.003% FSR, 0200h to FD00h		8		µs
Slew Rate				1		V/µs
DC Output Impedance				7		Ω
Short-Circuit Current		All 1s Loaded to DAC Register		16		mA
IDAC Output Characteristics						
Full-Scale Output Current		Maximum V_{REF} = 1.25V		25		mA
Maximum Short-Circuit Current Duration				Indefinite		
Compliance Voltage				AV_{DD} − 1.5		V
Relative Accuracy		Over Full Range		0.185		% of FSR
Zero Code Error				0.5		% of FSR
Full-Scale Error				−0.4		% of FSR
Gain Error				−0.6		% of FSR
Analog Power-Supply Requirements						
Analog Power-Supply Voltage		AV_{DD}	2.7	3.0	3.6	V
Analog Power-Supply Current	Analog Off Current(8)	Analog OFF, PDCON = 47h		< 1		nA
	ADC Current (I_{ADC})	PGA = 1, Buffer OFF		200		µA
		PGA = 128, Buffer OFF		500		µA
		PGA = 1, Buffer ON		240		µA
		PGA = 128, Buffer ON		850		µA
	VDAC Current (I_{VDAC})	Excluding Load Current, External Reference		250		µA
	V_{REF} Supply Current (I_{VDAC})	ADC ON, V_{DAC} OFF		250		µA

(1) The input impedance for PGA = 128 is the same as that for PGA = 64 (that is, 7MΩ/64).
(2) Calibration can minimize these errors.
(3) The gain calibration cannot have a REF IN+ of more than AV_{DD} −1.5V with Buffer ON. To calibrate gain, turn Buffer OFF.
(4) ΔV_{OUT} is change in digital result.
(5) 9pF switched capacitor at f_{SAMP} clock frequency (see Figure 14).
(6) Linearity calculated using a reduced code range of 512 to 65024; output unloaded.
(7) Ensured by design and characterization; not production tested.
(8) Analog Brownout Detect OFF (HCR1.3 = 1), Analog LVD OFF (LVDCON.7 = 1).

DIGITAL CHARACTERISTICS: DV_{DD} = 2.7V to 5.25V

All specifications from T_{MIN} to T_{MAX}, FMCON = 10h, all digital outputs high, PDCON = 00h (all peripherals ON) or PDCON = FFh (all peripherals OFF), $\overline{PSEN}$ and ALE enabled (all peripherals ON) or $\overline{PSEN}$ and ALE disabled (all peripherals OFF), unless otherwise specified.

PARAMETER		CONDITIONS	MSC1211/12/13/14 MIN	TYP	MAX	UNITS
Digital Power-Supply Requirements						
DV_{DD}			2.7	3	3.6	V
Digital Power-Supply Current		Normal Mode, f_{OSC} = 1MHz, peripherals OFF		0.9		mA
		Normal Mode, f_{OSC} = 1MHz, peripherals ON		1.1		mA
		Normal Mode, f_{OSC} = 8MHz, peripherals OFF		5.7		mA
		Normal Mode, f_{OSC} = 8MHz, peripherals ON		7.5		mA
		Crystal Operation Stop Mode(1)		100		nA
DV_{DD}			4.75	5	5.25	V
Digital Power-Supply Current		Normal Mode, f_{OSC} = 1MHz, peripherals OFF		1.7		mA
		Normal Mode, f_{OSC} = 1MHz, peripherals ON		2.4		mA
		Normal Mode, f_{OSC} = 8MHz, peripherals OFF		11		mA
		Normal Mode, f_{OSC} = 8MHz, peripherals ON		14.8		mA
		Crystal Operation Stop Mode(1)		100		nA
DIGITAL INPUT/OUTPUT (CMOS)						
Logic Level	V_{IH} (except XIN pin)		0.6 • DV_{DD}		DV_{DD}	V
	V_{IL} (except XIN pin)		DGND		0.2 • DV_{DD}	V
I/O Pin Hysteresis				700		mV
Ports 0−3, Input Leakage Current, Input Mode		V_{IH} = DV_{DD} or V_{IH} = 0V		< 1		pA
Pins $\overline{EA}$, RST Input Leakage Current				< 1		pA
V_{OL}, ALE, $\overline{PSEN}$, Ports 0−3, All Output Modes		I_{OL} = −1mA	DGND		0.4	V
		I_{OL} = −30mA (5V), −20mA (3V)		1.5		V
V_{OH}, ALE, $\overline{PSEN}$, Ports 0−3, Strong Drive Output		I_{OH} = 1mA	DV_{DD} − 0.4	DV_{DD} − 0.1	DV_{DD}	V
		I_{OH} = 30mA (5V), 20mA (5V)		DV_{DD} − 1.5		V
Ports 0−3, Pull-Up Resistors				9		kΩ
Pins ALE, $\overline{PSEN}$, Pull-Up Resistors During Reset		Flash Programming Mode Only		9		kΩ
OSCILLATOR/CLOCK INPUT/OUTPUT						
External Oscillator/Clock	V_{IH} (except XIN pin)	XOUT must be unconnected	0.6 • DV_{DD}		DV_{DD}	V
	V_{IL} (except XIN pin)	XOUT must be unconnected	DGND		0.2 • DV_{DD}	V

(1) Digital Brownout Detect disabled (HCR1.2 = 1), Low Voltage Detect disabled (LVDCON.3 = 1). Ports configured for CMOS output low.

FLASH MEMORY CHARACTERISTICS: DV_{DD} = 2.7V to 5.25V

PARAMETER	CONDITIONS	MSC1211/12/13/14 MIN	TYP	MAX	UNITS
Flash Memory Endurance		100,000	1,000,000		Cycles
Flash Memory Data Retention		100			Years
Mass and Page Erase Time	Set with FER in FTCON	10			ms
Flash Memory Write Time	Set with FWR in FTCON	30		40	µs
Flash Programming Current(1)	DV_{DD} = 3.0V			10	mA
	DV_{DD} = 5.0V			25	mA

(1) Peak current during Mass and Page Erase Time and Memory Write Time.

AC ELECTRICAL CHARACTERISTICS[1][2]: DV_{DD} = 2.7V to 5.25V

SYMBOL	FIGURE	PARAMETER	2.7V to 3.6V MIN	2.7V to 3.6V MAX	4.75V to 5.25V MIN	4.75V to 5.25V MAX	UNITS
System Clock							
f_{OSC}[3]	4	External Crystal Frequency (f_{OSC})	1	24	1	33	MHz
$1/t_{OSC}$[3]	4	External Clock Frequency (f_{OSC}) at +85°C	0	24	0	40	MHz
		External Clock Frequency (f_{OSC}) at +125°C	0	22	0	36	MHz
f_{OSC}[3]	4	External Ceramic Resonator Frequency (f_{OSC})	1	12	1	12	MHz
Program Memory							
t_{LHLL}	1	ALE Pulse Width	$1.5t_{CLK} - 5$		$1.5t_{CLK} - 5$		ns
t_{AVLL}	1	Address Valid to ALE Low	$0.5t_{CLK} - 10$		$0.5t_{CLK} - 7$		ns
t_{LLAX}	1	Address Hold After ALE Low	$0.5t_{CLK}$		$0.5t_{CLK}$		ns
t_{LLIV}	1	ALE Low to Valid Instruction In		$2.5t_{CLK} - 35$		$2.5t_{CLK} - 25$	ns
t_{LLPL}	1	ALE Low to $\overline{PSEN}$ Low	$0.5t_{CLK}$		$0.5t_{CLK}$		ns
t_{PLPH}	1	$\overline{PSEN}$ Pulse Width	$2t_{CLK} - 5$		$2t_{CLK} - 5$		ns
t_{PLIV}	1	$\overline{PSEN}$ Low to Valid Instruction In		$2t_{CLK} - 40$		$2t_{CLK} - 30$	ns
t_{PXIX}	1	Input Instruction Hold After $\overline{PSEN}$	5		−5		ns
t_{PXIZ}	1	Input Instruction Float After $\overline{PSEN}$		$t_{CLK} - 5$		t_{CLK}	ns
t_{AVIV}	1	Address to Valid Instruction In		$3t_{CLK} - 40$		$3t_{CLK} - 25$	ns
t_{PLAZ}	1	PSEN Low to Address Float		0		0	ns
Data Memory							
t_{RLRH}	2	$\overline{RD}$ Pulse Width (t_{MCS} = 0)[4]	$2t_{CLK} - 5$		$2t_{CLK} - 5$		ns
		$\overline{RD}$ Pulse Width (t_{MCS} > 0)[4]	$t_{MCS} - 5$		$t_{MCS} - 5$		ns
t_{WLWH}	3	$\overline{WR}$ Pulse Width (t_{MCS} = 0)[4]	$2t_{CLK} - 5$		$2t_{CLK} - 5$		ns
		$\overline{WR}$ Pulse Width (t_{MCS} > 0)[4]	$t_{MCS} - 5$		$t_{MCS} - 5$		ns
t_{RLDV}	2	$\overline{RD}$ Low to Valid Data In (t_{MCS} = 0)[4]		$2t_{CLK} - 40$		$2t_{CLK} - 30$	ns
		$\overline{RD}$ Low to Valid Data In (t_{MCS} > 0)[4]		$t_{MCS} - 40$		$t_{MCS} - 30$	ns
t_{RHDX}	2	Data Hold After Read	−5		−5		ns
t_{RHDZ}	2	Data Float After Read (t_{MCS} = 0)[4]		t_{CLK}		t_{CLK}	ns
		Data Float After Read (t_{MCS} > 0)[4]		$2t_{CLK}$		$2t_{CLK}$	ns
t_{LLDV}	2	ALE Low to Valid Data In (t_{MCS} = 0)[4]		$2.5t_{CLK} - 40$		$2.5t_{CLK} - 25$	ns
		ALE Low to Valid Data In (t_{MCS} > 0)[4]		$t_{CLK} + t_{MCS} - 40$		$t_{CLK} + t_{MCS} - 25$	ns
t_{AVDV}	2	Address to Valid Data In (t_{MCS} = 0)[4]		$3t_{CLK} - 40$		$3t_{CLK} - 25$	ns
		Address to Valid Data In (t_{MCS} > 0)[4]		$1.5t_{CLK} + t_{MCS} - 40$		$1.5t_{CLK} + t_{MCS} - 25$	ns
t_{LLWL}	2, 3	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low (t_{MCS} = 0)[4]	$0.5t_{CLK} - 5$	$0.5t_{CLK} + 5$	$0.5t_{CLK} - 5$	$0.5t_{CLK} + 5$	ns
		ALE Low to $\overline{RD}$ or $\overline{WR}$ Low (t_{MCS} > 0)[4]	$t_{CLK} - 5$	$t_{CLK} + 5$	$t_{CLK} - 5$	$t_{CLK} + 5$	ns
t_{AVWL}	2, 3	Address to $\overline{RD}$ or $\overline{WR}$ Low (t_{MCS} = 0)[4]	$t_{CLK} - 5$		$t_{CLK} - 5$		ns
		Address to $\overline{RD}$ or $\overline{WR}$ Low (t_{MCS} > 0)[4]	$2t_{CLK} - 5$		$2t_{CLK} - 5$		ns
t_{QVWX}	3	Data Valid to $\overline{WR}$ Transition	−8		−5		ns
t_{WHQX}	3	Data Hold After $\overline{WR}$	$t_{CLK} - 8$		$t_{CLK} - 5$		ns
t_{RLAZ}	2	$\overline{RD}$ Low to Address Float		$-0.5t_{CLK} - 5$		$-0.5t_{CLK} - 5$	ns
t_{WHLH}	2, 3	$\overline{RD}$ or $\overline{WR}$ High to ALE High (t_{MCS} = 0)[4]	−5	5	−5	5	ns
		$\overline{RD}$ or $\overline{WR}$ High to ALE High (t_{MCS} > 0)[4]	$t_{CLK} - 5$	$t_{CLK} + 5$	$t_{CLK} - 5$	$t_{CLK} + 5$	ns
External Clock							
t_{HIGH}	4	High Time[5]	15		10		ns
t_{LOW}	4	Low Time[5]	15		10		ns
t_R	4	Rise Time[5]		5		5	ns
t_F	4	Fall Time[5]		5		5	ns

(1) Parameters are valid over operating temperature range, unless otherwise specified.
(2) Load capacitance for Port 0, ALE, and $\overline{PSEN}$ = 100pF; load capacitance for all other outputs = 80pF.
(3) $t_{CLK} = 1/f_{OSC}$ = one oscillator clock period for clock divider = 1.
(4) t_{MCS} is a time period related to the Stretch MOVX selection. The following table shows the value of t_{MCS} for each stretch selection:
(5) These values are characterized, but not 100% production tested.

MD2	MD1	MD0	MOVX DURATION	t_{MCS}
0	0	0	2 Machine Cycles	0
0	0	1	3 Machine Cycles (default)	$4t_{CLK}$
0	1	0	4 Machine Cycles	$8t_{CLK}$
0	1	1	5 Machine Cycles	$12t_{CLK}$
1	0	0	6 Machine Cycles	$16t_{CLK}$
1	0	1	7 Machine Cycles	$20t_{CLK}$
1	1	0	8 Machine Cycles	$24t_{CLK}$
1	1	1	9 Machine Cycles	$28t_{CLK}$

EXPLANATION OF THE AC SYMBOLS

Each Timing Symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designators are:

A—Address
C—Clock
D—Input Data
H—Logic Level High
I—Instruction (program memory contents)
L—Logic Level Low, or ALE
P—$\overline{\text{PSEN}}$
Q—Output Data
R—$\overline{\text{RD}}$ Signal
t—Time
V—Valid
W—$\overline{\text{WR}}$ Signal
X—No Longer a Valid Logic Level
Z—Float

Examples:

(1) t_{AVLL} = Time for address valid to ALE Low.
(2) t_{LLPL} = Time for ALE Low to $\overline{\text{PSEN}}$ Low.

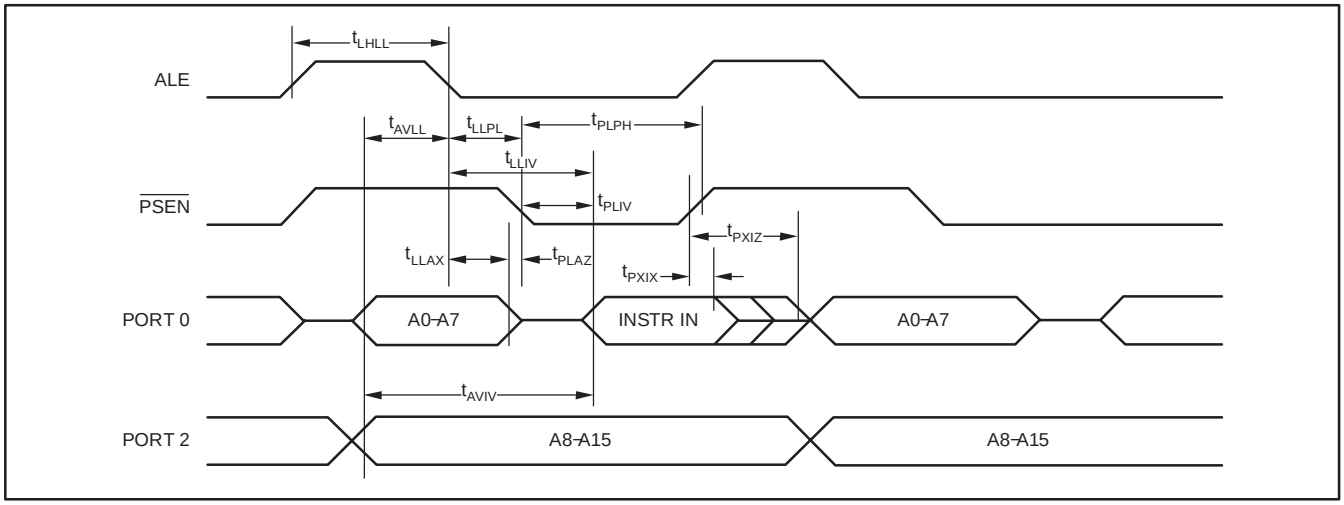


Figure 1. External Program Memory Read Cycle

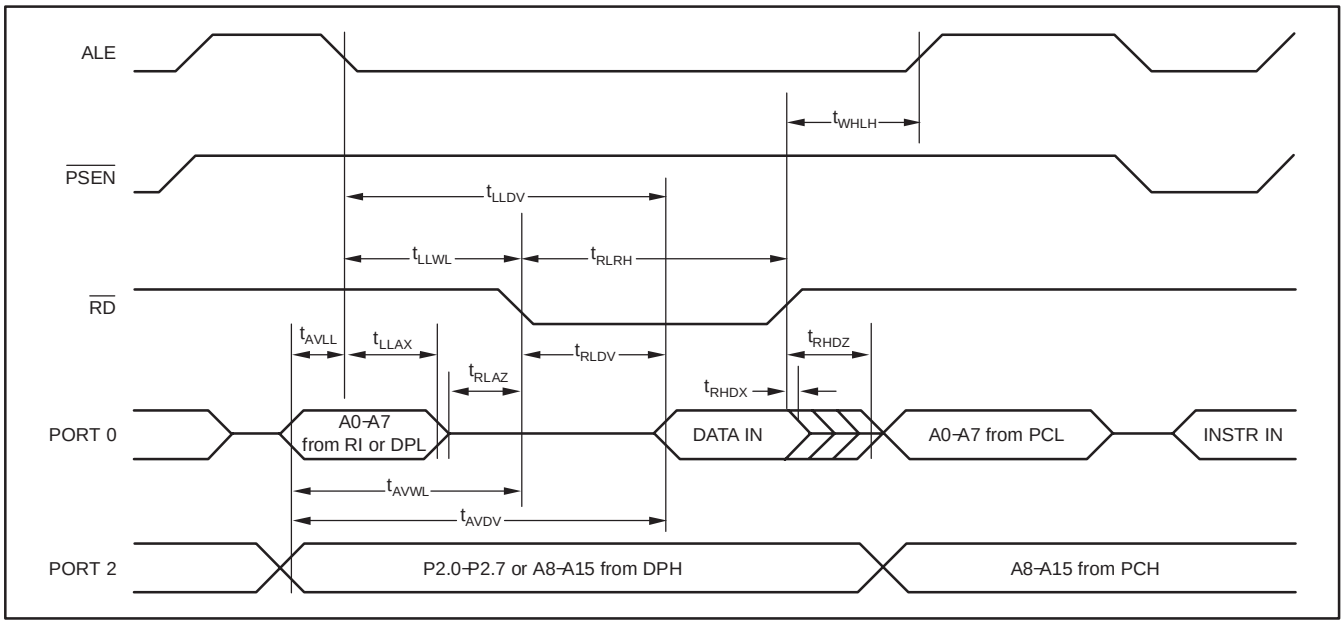


Figure 2. External Data Memory Read Cycle

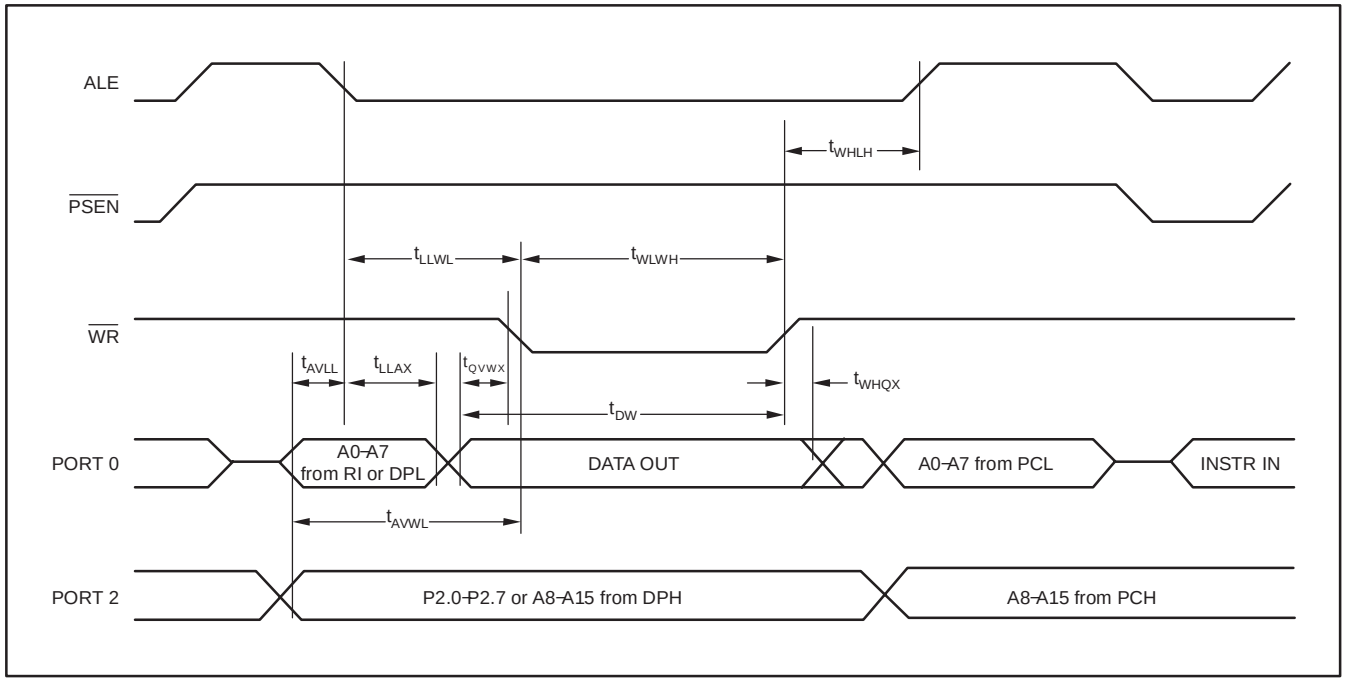


Figure 3. External Data Memory Write Cycle

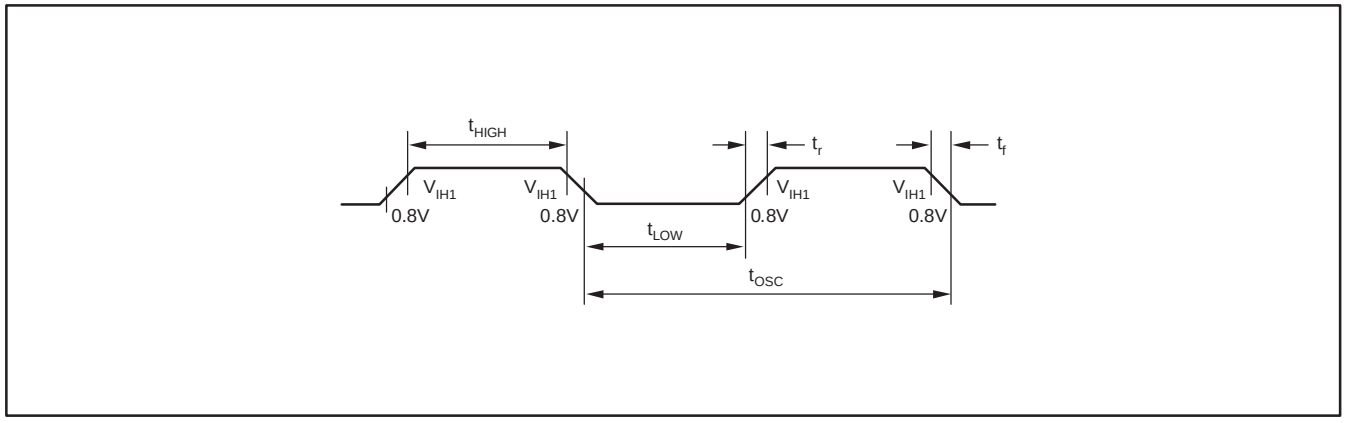


Figure 4. External Clock Drive CLK

RESET AND POWER-ON TIMING

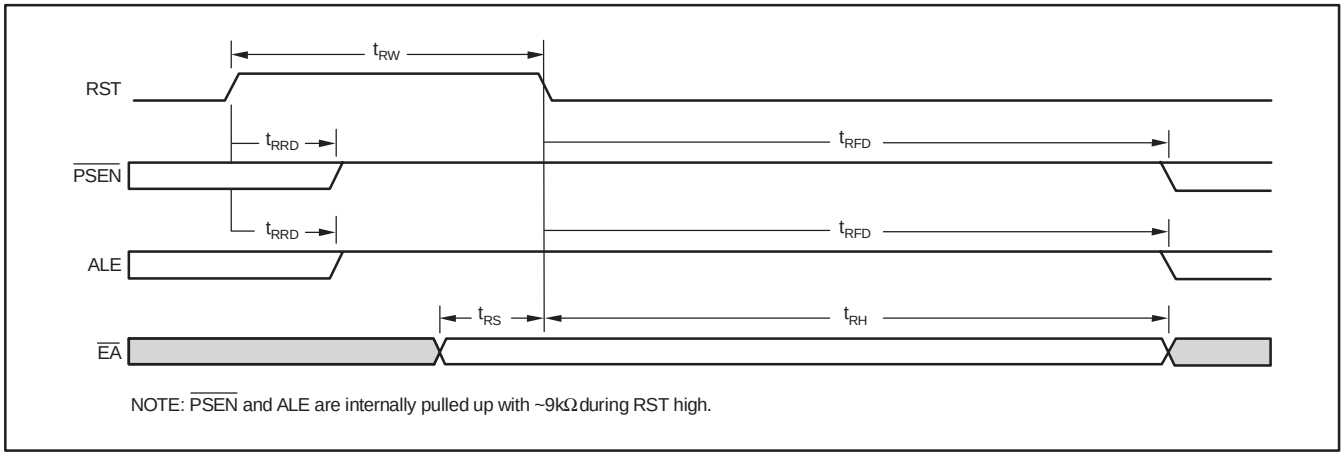


Figure 5. Reset Timing, User Application Mode

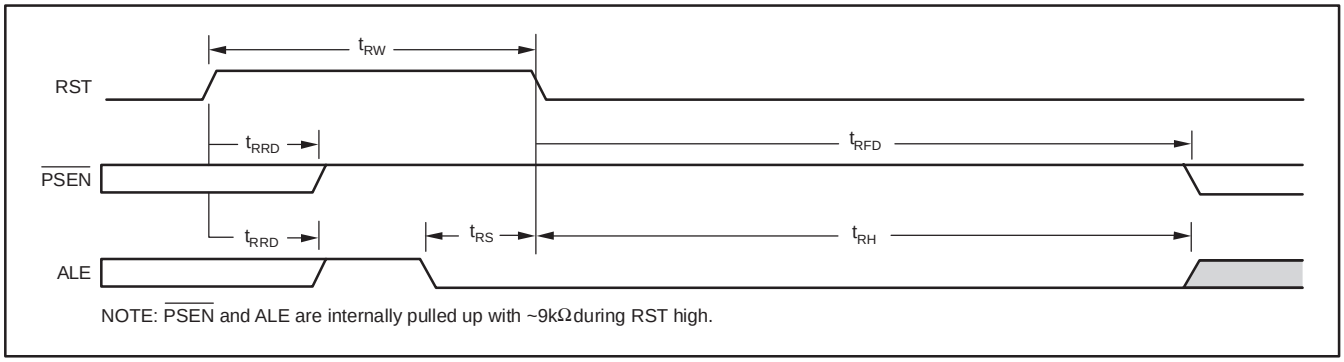


Figure 6. Parallel Flash Programming Power-On Timing ($\overline{EA}$ is ignored)

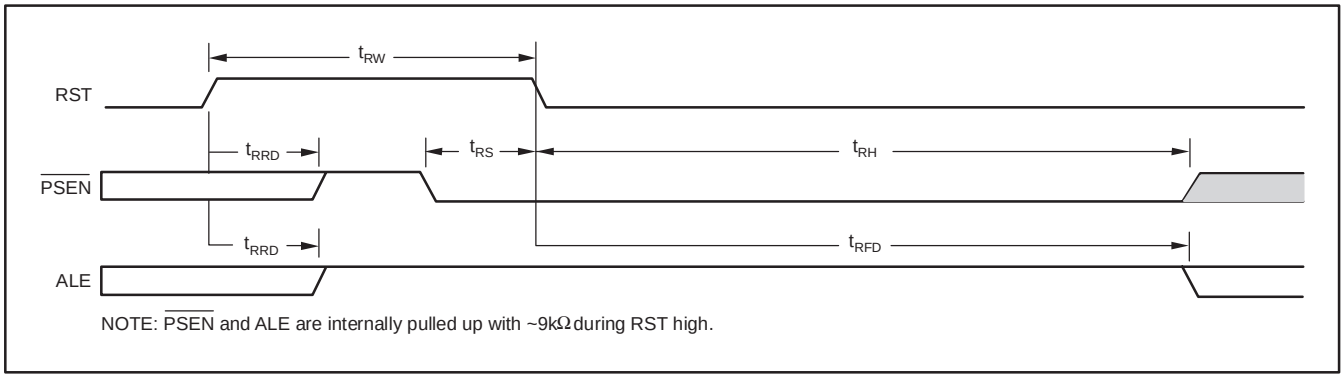
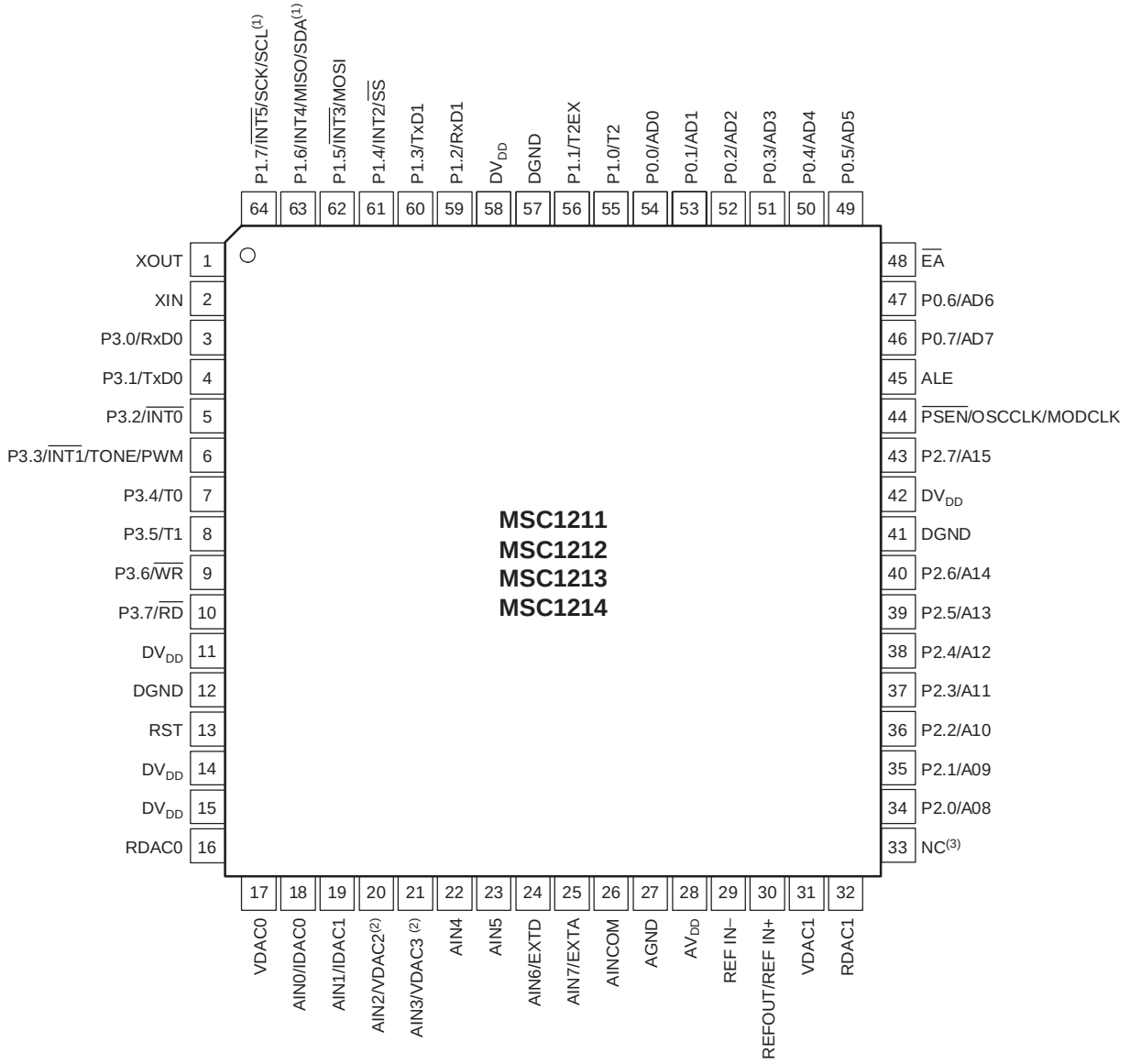


Figure 7. Serial Flash Programming Power-On Timing ($\overline{EA}$ is ignored)

Table 1. Serial/Parallel Flash Programming Timing

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{RW}	RST width	$2t_{OSC}$	—	—
t_{RRD}	RST rise to $\overline{PSEN}$ ALE internal pull high	—	5	µs
t_{RFD}	RST falling to $\overline{PSEN}$ and ALE start	—	$(2^{17} + 512)t_{OSC}$	—
t_{RS}	Input signal to RST falling setup time	t_{OSC}	—	—
t_{RH}	RST falling to input signal hold time	$(2^{17} + 512)t_{OSC}$	—	—



NOTES: (1) SCL and SDA are only available on the MSC1211 and MSC1213.
(2) VDAC2 and VDAC3 are only available on the MSC1211 and MSC1212.
(3) NC pin should be left unconnected.

PIN DESCRIPTIONS

PIN #	NAME	DESCRIPTION		
1	XOUT	The crystal oscillator pin XOUT supports parallel resonant AT-cut fundamental frequency crystals and ceramic resonators. XOUT serves as the output of the crystal amplifier.		
2	XIN	The crystal oscillator pin XIN supports parallel resonant AT-cut fundamental frequency crystals and ceramic resonators. XIN can also be an input if there is an external clock source instead of a crystal.		
3-10	P3.0-P3.7	Port 3 is a bidirectional I/O port. The alternate functions for Port 3 are listed below. Refer to P3DDR, SFR B3h−B4h.		
		Port	**Alternate Name(s)**	**Alternate Use**
		P3.0	RxD0	Serial port 0 input
		P3.1	TxD0	Serial port 1 input
		P3.2	$\overline{\text{INT0}}$	External interrupt 0
		P3.3	INT1/TONE/PWM	External interrupt 1/TONE/PWM output
		P3.4	T0	Timer 0 external input
		P3.5	T1	Timer 1 external input
		P3.6	$\overline{\text{WR}}$	External memory data write strobe
		P3.7	$\overline{\text{RD}}$	External memory data read strobe
11, 14, 15, 42, 58	DV_{DD}	Digital Power Supply		
12, 41, 57	DGND	Digital Ground		
13	RST	Holding the reset input high for two t_{OSC} periods will reset the device.		
16	RDAC0	IDAC0 Reference Resistor Pin		
17	VDAC0	VDAC0 Output		
27	AGND	Analog Ground		
18	AIN0/IDAC0	Analog Input Channel 0 / IDAC0 Output		
19	AIN1/IDAC1	Analog Input Channel 1 / IDAC1 Output		
20	AIN2/VDAC2	Analog Input Channel 2 / VDAC2 Output (MSC1211 and MSC1212 only)		
21	AIN3V/DAC3	Analog Input Channel 3 / VDAC3 Output (MSC1211 and MSC1212 only)		
22	AIN4	Analog Input Channel 4		
23	AIN5	Analog Input Channel 5		
24	AIN6/EXTD	Analog Input Channel 6 / LVD Comparator Input, Generates DLVD Interrupt		
25	AIN7/EXTA	Analog Input Channel 7 / LVD Comparator Input, Generates ALVD Interrupt		
26	AINCOM	Analog Common; can be used like any analog input except during Offset − Inputs shorted to this pin.		
28	AV_{DD}	Analog Power Supply		
29	REF IN−	Voltage Reference Negative Input (must be tied to AGND for internal V_{REF} use)		
30	REFOUT/REF IN+	Internal Voltage Reference Output / Voltage Reference Positive Input		
31	VDAC1	VDAC1 Output		
32	RDAC1	IDAC1 Reference Resistor Pin		
33	NC	No Connection; leave unconnected.		
34-40, 43	P2.0-P2.7	Port 2 is a bidirectional I/O port. The alternate functions for Port 2 are listed below. Refer to P2DDR, SFR B1h−B2h.		
		Port	**Alternate Name**	**Alternate Use**
		P2.0	A8	Address bit 8
		P2.1	A9	Address bit 9
		P2.2	A10	Address bit 10
		P2.3	A11	Address bit 11
		P2.4	A12	Address bit 12
		P2.5	A13	Address bit 13
		P2.6	A14	Address bit 14
		P2.7	A15	Address bit 15

(1) SDA and SCL are only available on the MSC1213.

PIN DESCRIPTIONS (continued)

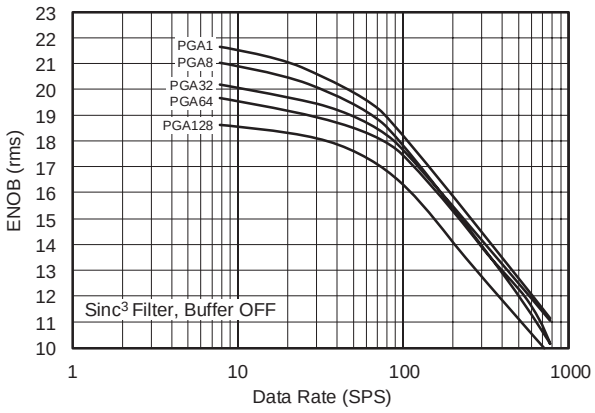
PIN #	NAME	DESCRIPTION		
44	$\overline{\text{PSEN}}$ OSCCLK MODCLK	Program Store Enable: Connected to optional external memory as a chip enable. $\overline{\text{PSEN}}$ will provide an active low pulse. In programming mode, $\overline{\text{PSEN}}$ is used as an input along with ALE to define serial or parallel programming mode. $\overline{\text{PSEN}}$ is held high for parallel programming and held low for serial programming. This pin can also be selected (when not using external memory) to output the Oscillator clock, Modulator clock, high, or low. Care should be taken so that loading on this pin should not inadvertently cause the device to enter programming mode.		
		ALE	**$\overline{\text{PSEN}}$**	**Program Mode Selection During Reset**
		NC	NC	Normal operation (User Application mode)
		0	NC	Parallel programming
		NC	0	Serial programming
		0	0	Reserved
45	ALE	Address Latch Enable: Used for latching the low byte of the address during an access to external memory. ALE is emitted at a constant rate of 1/4 the oscillator frequency, and can be used for external timing or clocking. One ALE pulse is skipped during each access to external data memory. In programming mode, ALE is used as an input along with $\overline{\text{PSEN}}$ to define serial or parallel programming mode. ALE is held high for serial programming and held low for parallel programming. This pin can also be selected (when not using external memory) to output high or low. Care should be taken so that loading on this pin should not inadvertently cause the device to enter programming mode.		
48	$\overline{\text{EA}}$	External Access Enable: $\overline{\text{EA}}$ must be externally held low to enable the device to fetch code from external program memory locations starting with 0000h. No internal pull-up on this pin.		
46, 47, 49-54	P0.0-P0.7	Port 0 is a bidirectional I/O port. The alternate functions for Port 0 are listed below.		
		Port	**Alternate Name**	**Alternate Use**
		P0.0	AD0	Address/Data bit 0
		P0.1	AD1	Address/Data bit 1
		P0.2	AD2	Address/Data bit 2
		P0.3	AD3	Address/Data bit 3
		P0.4	AD4	Address/Data bit 4
		P0.5	AD5	Address/Data bit 5
		P0.6	AD6	Address/Data bit 6
		P0.7	AD7	Address/Data bit 7
55, 56, 59-64	P1.0-P1.7	Port 1 is a bidirectional I/O port. The alternate functions for Port 1 are listed below. Refer to P1DDR, SFR AEh−AFh.		
		Port	**Alternate Name(s)**	**Alternate Use**
		P1.0	T2	T2 input
		P1.1	T2EX	T2 external input
		P1.2	RxD1	Serial port input
		P1.3	TxD1	Serial port output
		P1.4	INT2/$\overline{\text{SS}}$	External Interrupt / Slave Select
		P1.5	$\overline{\text{INT3}}$/MOSI	External Interrupt / Master Out-Slave In
		P1.6	INT4/MISO/SDA(1)	External Interrupt / Master In-Slave Out / SDA
		P1.7	$\overline{\text{INT5}}$/SCK/SCL(1)	External Interrupt / Serial Clock

(1) SDA and SCL are only available on the MSC1213.

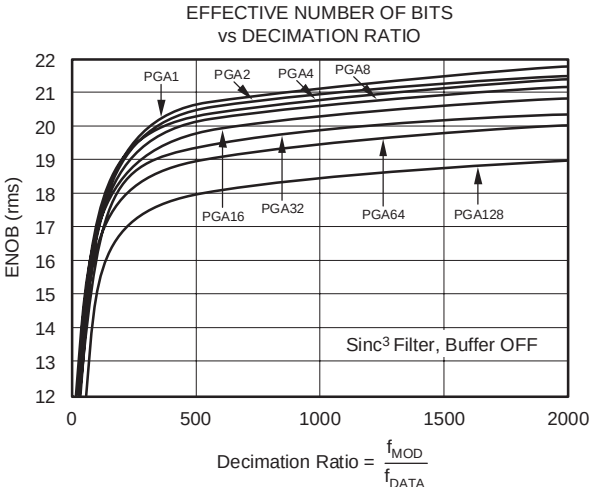
TYPICAL CHARACTERISTICS

AV_{DD} = +5V, DV_{DD} = +5V, f_{OSC} = 8MHz, PGA = 1, f_{MOD} = 15.625kHz, Bipolar, filter = Sinc3, Buffer ON, and $V_{REF} \equiv$ (REF IN+) − (REF IN−) = +2.5V, unless otherwise specified.

EFFECTIVE NUMBER OF BITS vs DATA RATE



EFFECTIVE NUMBER OF BITS vs DECIMATION RATIO



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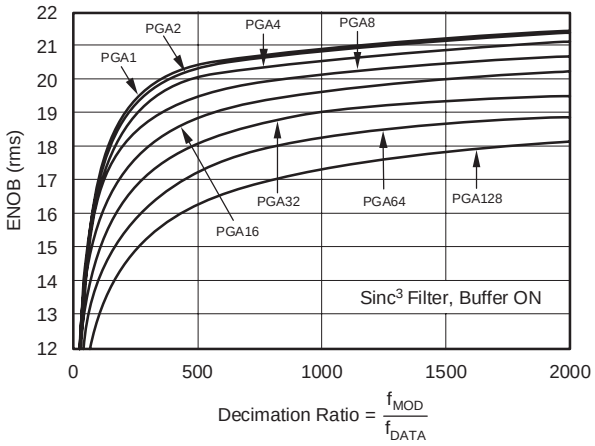
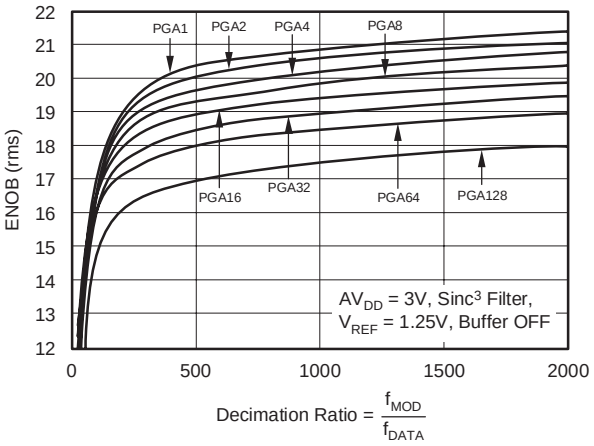
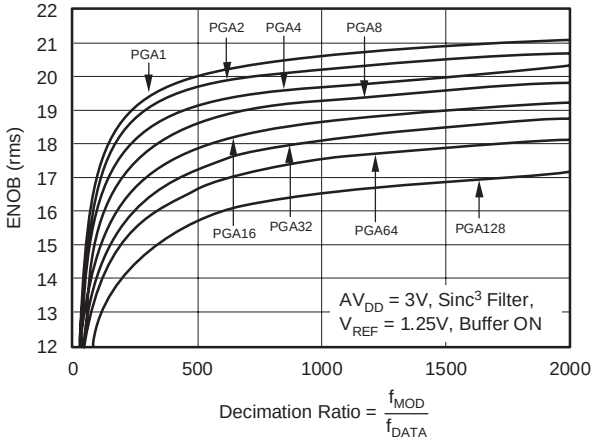


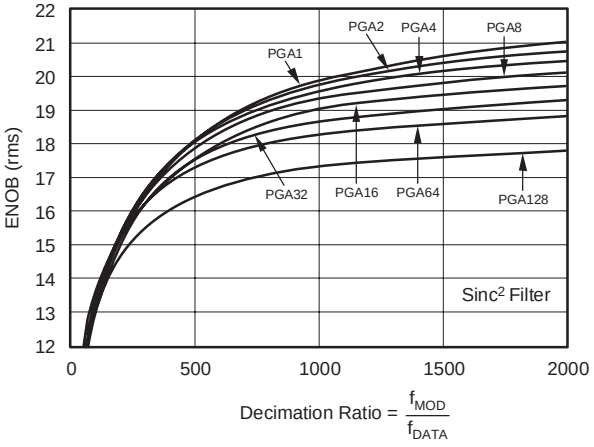
EFFECTIVE NUMBER OF BITS vs DECIMATION RATIO



EFFECTIVE NUMBER OF BITS vs DECIMATION RATIO



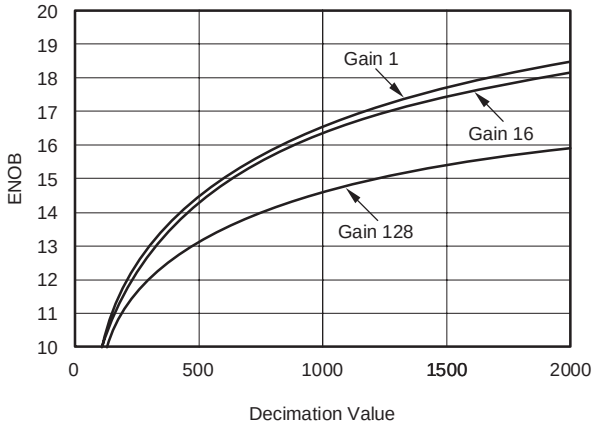
EFFECTIVE NUMBER OF BITS vs DECIMATION RATIO



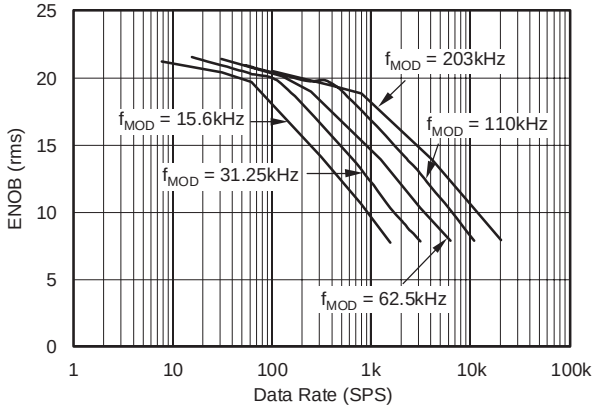
TYPICAL CHARACTERISTICS (Continued)

AV_{DD} = +5V, DV_{DD} = +5V, f_{OSC} = 8MHz, PGA = 1, f_{MOD} = 15.625kHz, Bipolar, filter = Sinc3, Buffer ON, and $V_{REF} \equiv$ (REF IN+) − (REF IN−) = +2.5V, unless otherwise specified.

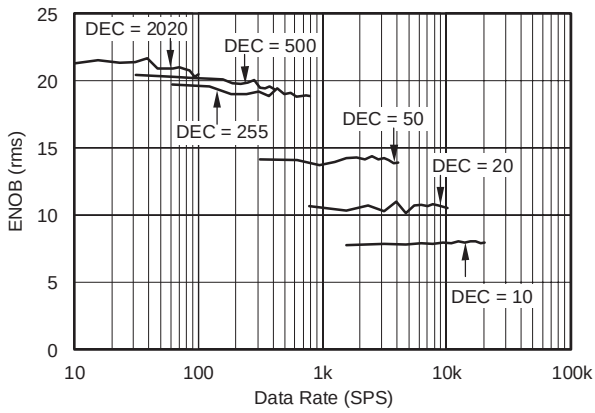
FAST SETTLING FILTER
EFFECTIVE NUMBER OF BITS vs DECIMATION RATIO



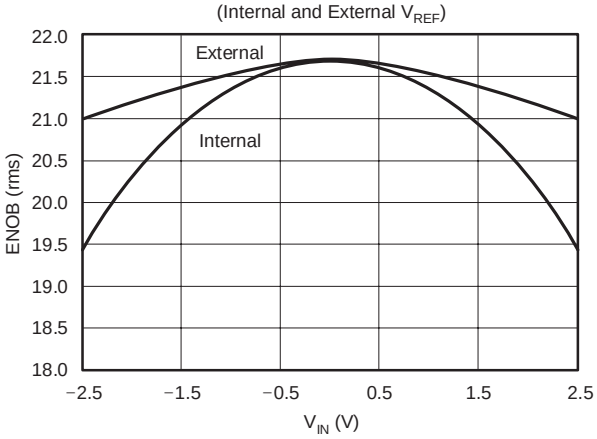
EFFECTIVE NUMBER OF BITS vs f_{MOD}
(set with ACLK)



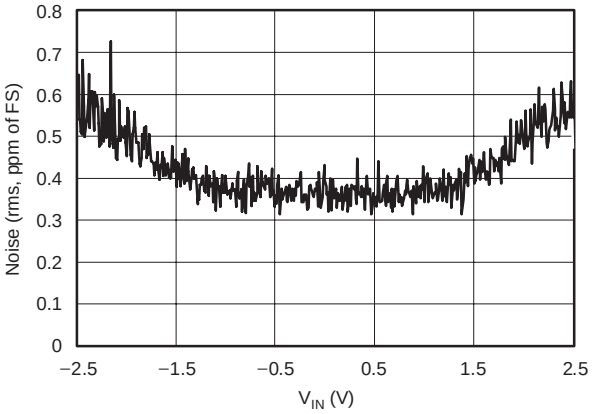
EFFECTIVE NUMBER OF BITS vs f_{MOD} (set with ACLK)
WITH FIXED DECIMATION, PGA = 1



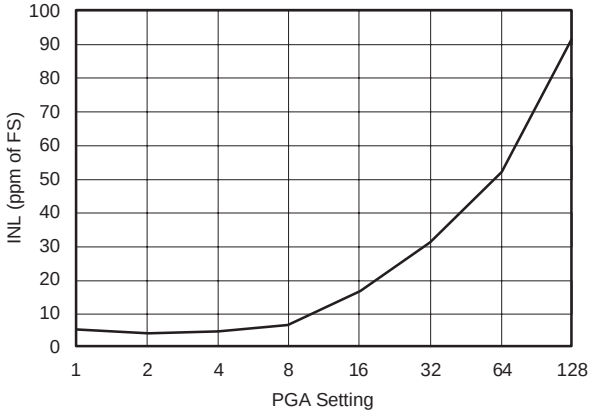
EFFECTIVE NUMBER OF BITS vs INPUT SIGNAL
(Internal and External V_{REF})



NOISE vs INPUT SIGNAL



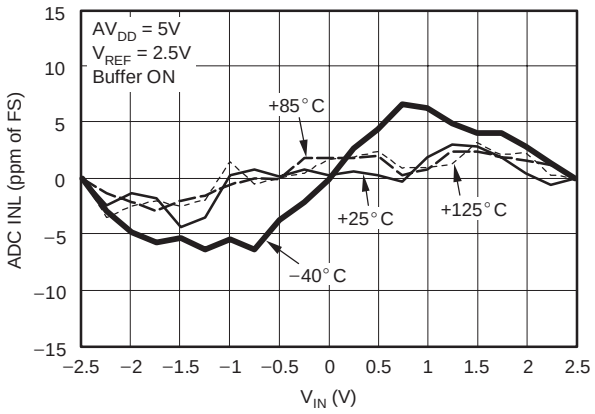
INL ERROR vs PGA



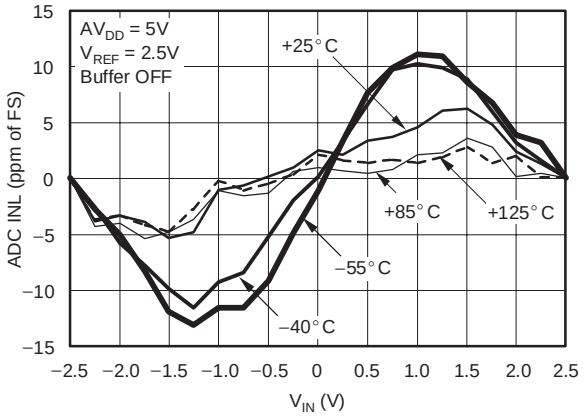
TYPICAL CHARACTERISTICS (Continued)

AV_{DD} = +5V, DV_{DD} = +5V, f_{OSC} = 8MHz, PGA = 1, f_{MOD} = 15.625kHz, Bipolar, filter = Sinc3, Buffer ON, and $V_{REF} \equiv$ (REF IN+) − (REF IN−) = +2.5V, unless otherwise specified.

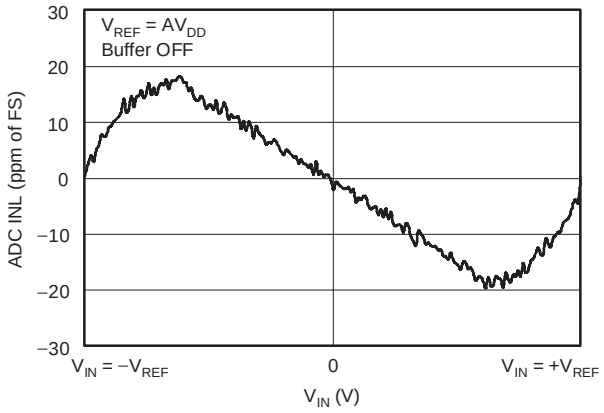
ADC INTEGRAL NONLINEARITY
vs INPUT SIGNAL



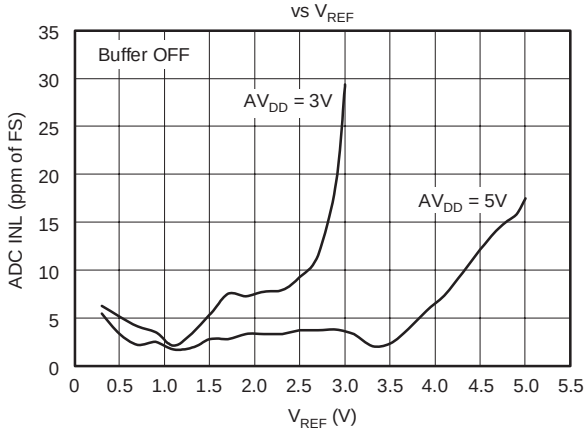
ADC INTEGRAL NONLINEARITY
vs INPUT SIGNAL



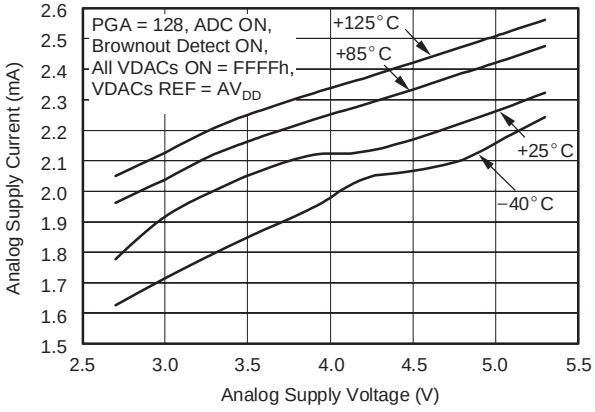
ADC INTEGRAL NONLINEARITY
vs INPUT SIGNAL



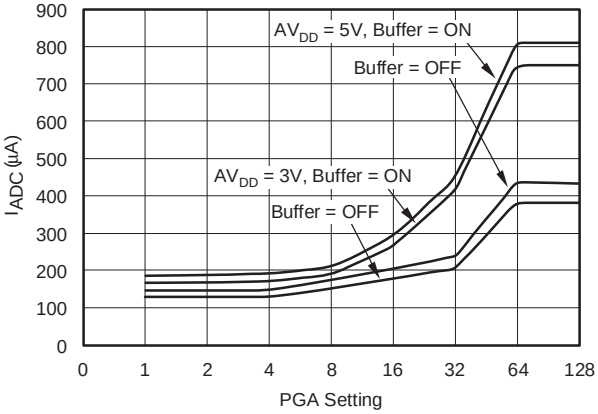
ADC INTEGRAL NONLINEARITY
vs V_{REF}



ANALOG SUPPLY CURRENT
vs ANALOG SUPPLY VOLTAGE



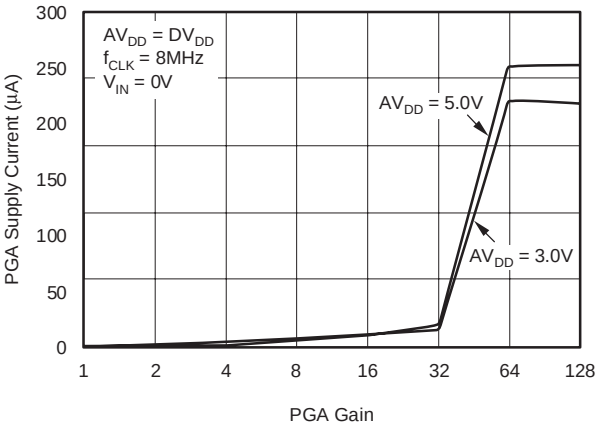
ADC CURRENT vs PGA



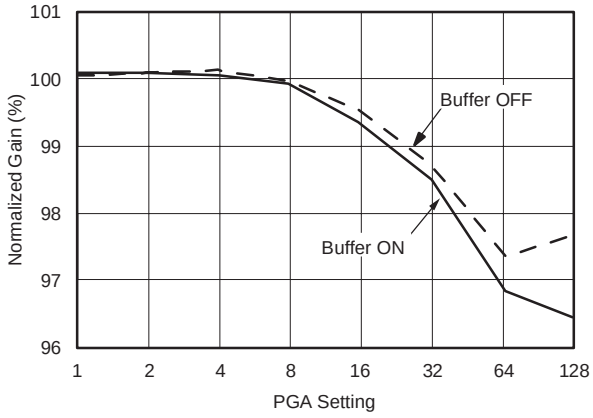
TYPICAL CHARACTERISTICS (Continued)

AV_{DD} = +5V, DV_{DD} = +5V, f_{OSC} = 8MHz, PGA = 1, f_{MOD} = 15.625kHz, Bipolar, filter = Sinc3, Buffer ON, and $V_{REF} \equiv$ (REF IN+) − (REF IN−) = +2.5V, unless otherwise specified.

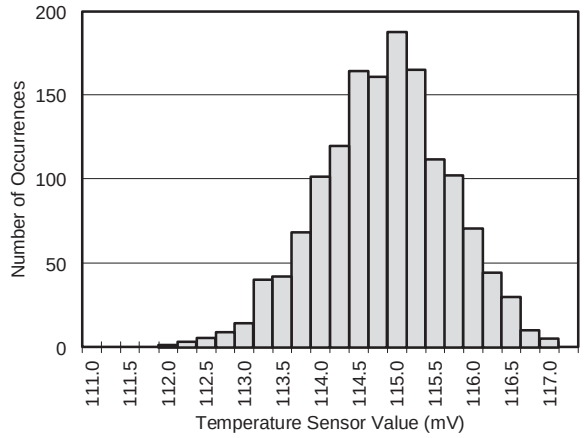
PGA SUPPLY CURRENT



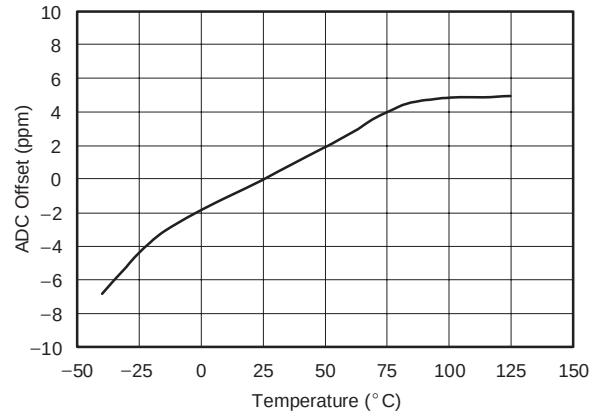
NORMALIZED GAIN vs PGA



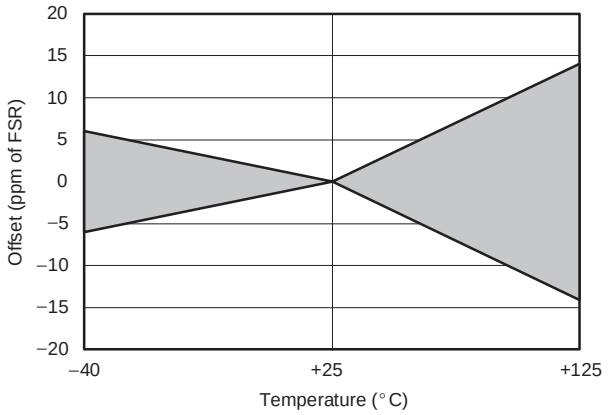
HISTOGRAM OF
TEMPERATURE SENSOR VALUES



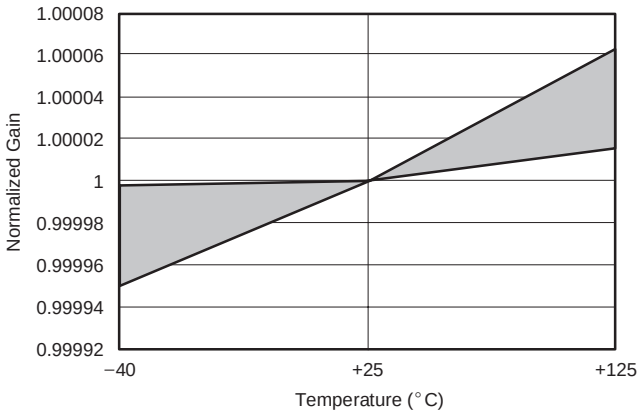
ADC OFFSET vs TEMPERATURE
(Offset Calibration at +25°C Only)



OFFSET DAC: OFFSET vs TEMPERATURE



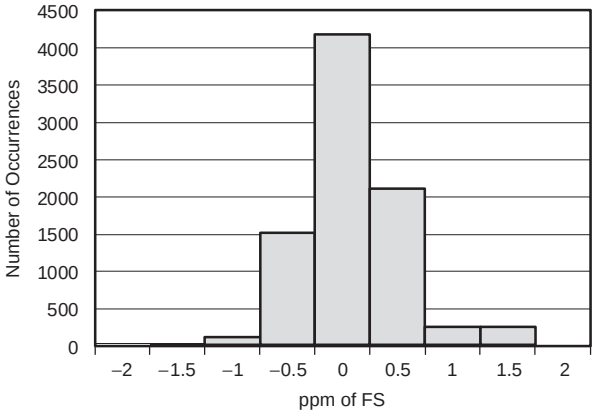
OFFSET DAC: GAIN vs TEMPERATURE



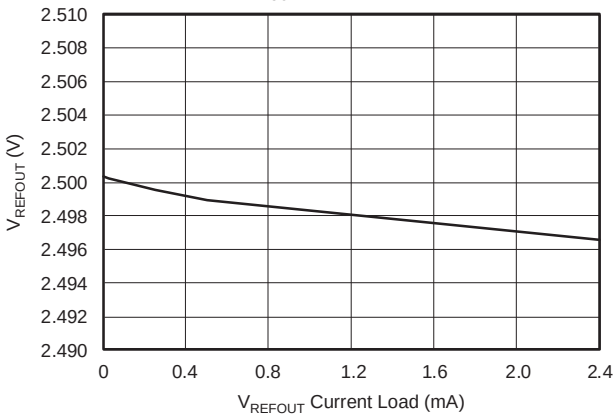
TYPICAL CHARACTERISTICS (Continued)

AV_{DD} = +5V, DV_{DD} = +5V, f_{OSC} = 8MHz, PGA = 1, f_{MOD} = 15.625kHz, Bipolar, filter = $Sinc^3$, Buffer ON, and $V_{REF} \equiv$ (REF IN+) − (REF IN−) = +2.5V, unless otherwise specified.

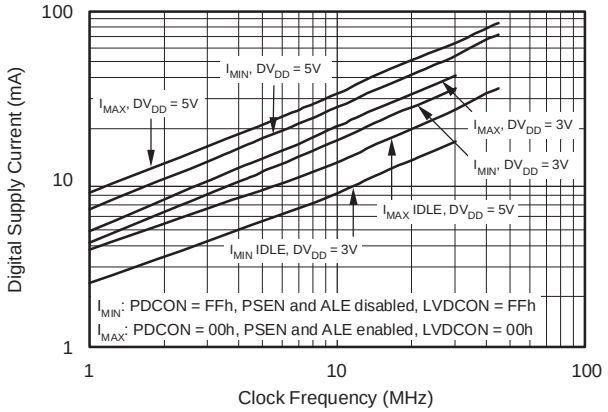
HISTOGRAM OF OUTPUT DATA



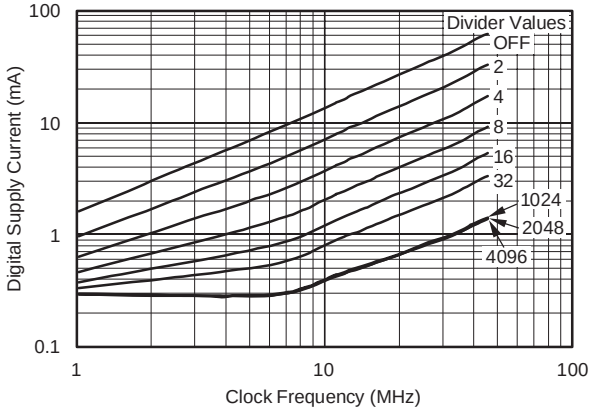
V_{REFOUT} vs LOAD CURRENT



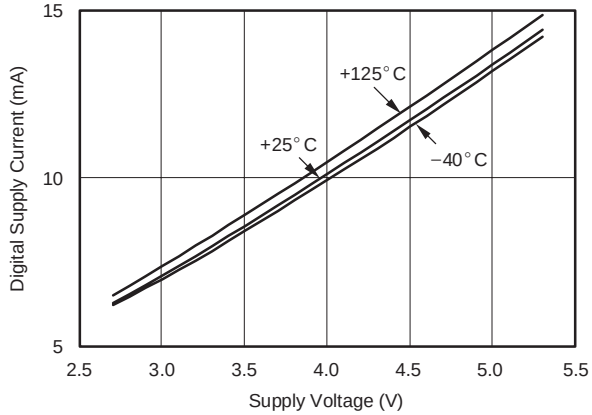
DIGITAL SUPPLY CURRENT vs FREQUENCY



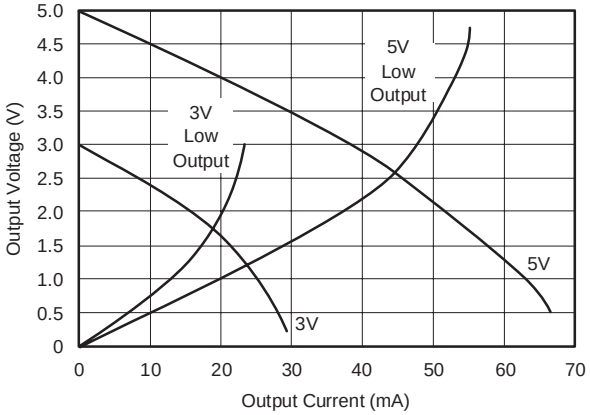
DIGITAL SUPPLY CURRENT vs CLOCK DIVIDER



DIGITAL SUPPLY CURRENT vs SUPPLY VOLTAGE



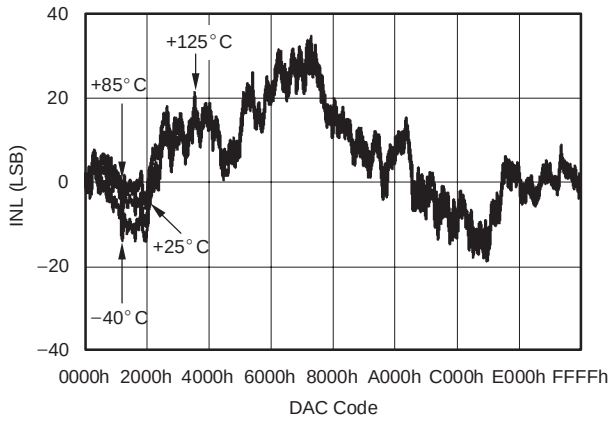
CMOS DIGITAL OUTPUT



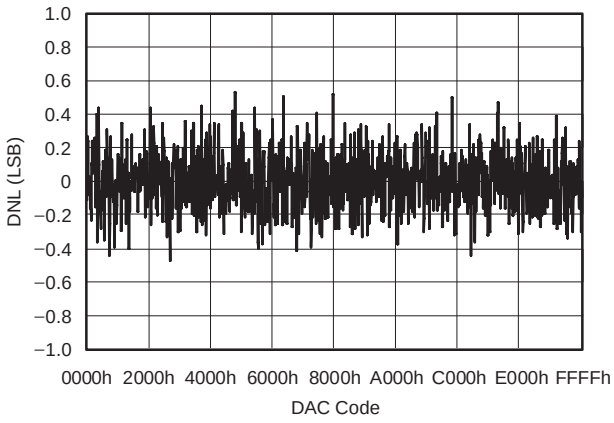
TYPICAL CHARACTERISTICS: VDACs

AV_{DD} = +5V, DV_{DD} = +5V, f_{OSC} = 8MHz, PGA = 1, f_{MOD} = 15.625kHz, Bipolar, filter = $Sinc^3$, Buffer ON, and $V_{REF} \equiv$ (REF IN+) − (REF IN−) = +2.5V, unless otherwise specified. For V_{DAC}: $V_{REF} = AV_{DD}$, R_{LOAD} = 10kΩ, and C_{LOAD} = 200pF unless otherwise noted.

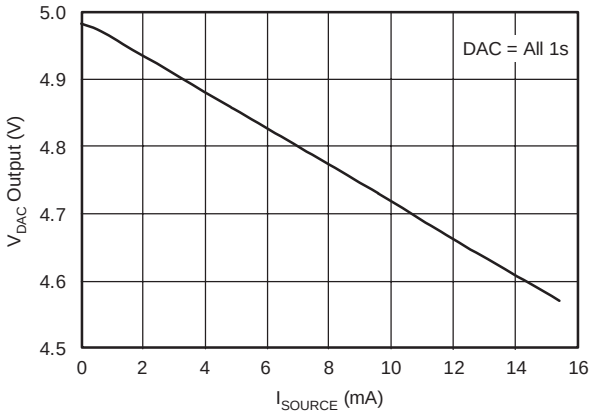
VDAC INTEGRAL NONLINEARITY vs CODE



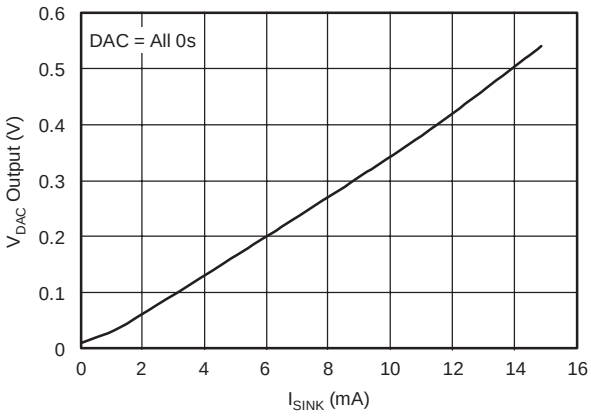
VDAC DIFFERENTIAL NONLINEARITY vs CODE



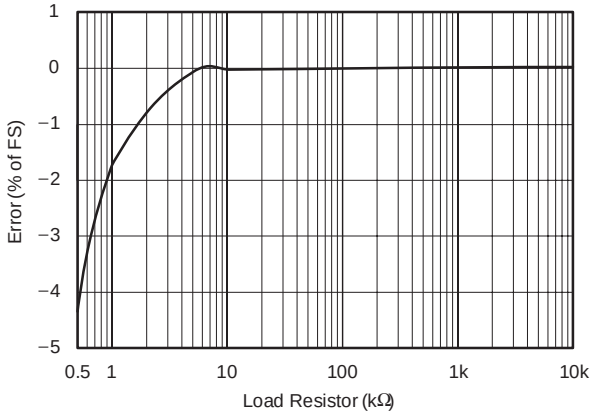
VDAC SOURCE CURRENT CAPABILITY



VDAC SINK CURRENT CAPABILITY



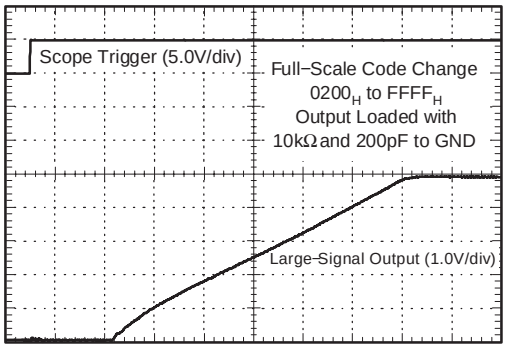
VDAC FULL−SCALE ERROR vs LOAD RESISTOR



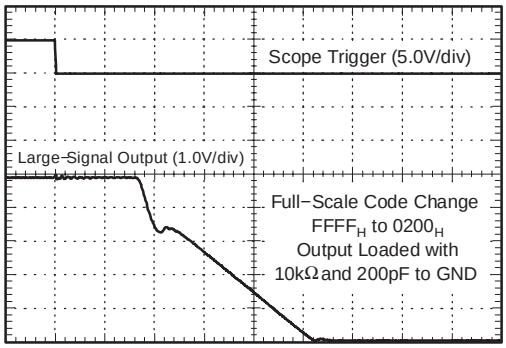
TYPICAL CHARACTERISTICS: VDACs (Continued)

AV_{DD} = +5V, DV_{DD} = +5V, f_{OSC} = 8MHz, PGA = 1, f_{MOD} = 15.625kHz, Bipolar, filter = $Sinc^3$, Buffer ON, and V_{REF} ≡ (REF IN+) − (REF IN−) = +2.5V, unless otherwise specified. For V_{DAC}: V_{REF} = AV_{DD}, R_{LOAD} = 10kΩ, and C_{LOAD} = 200pF unless otherwise noted.

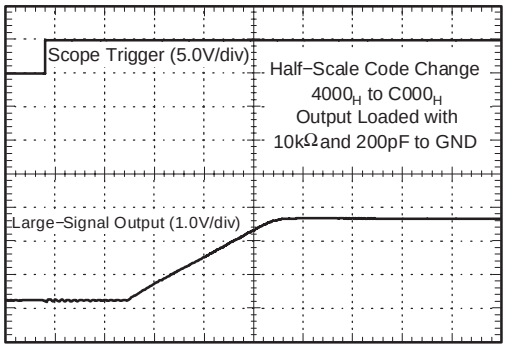
VDAC FULL−SCALE SETTLING TIME



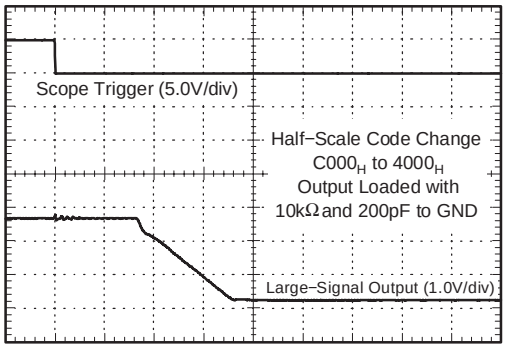
VDAC FULL−SCALE SETTLING TIME



VDAC HALF−SCALE SETTLING TIME



VDAC HALF−SCALE SETTLING TIME



DESCRIPTION

The MSC1211/12/13/14 are completely integrated families of mixed-signal devices incorporating a high-resolution delta-sigma (ΔΣ) ADC, 16-bit DACs, 8-channel multiplexer, burnout detect current sources, selectable buffered input, offset DAC, Programmable Gain Amplifier (PGA), temperature sensor, voltage reference, 8-bit microcontroller, Flash Program Memory, Flash Data Memory, and Data SRAM, as shown in Figure 8.

On-chip peripherals include an additional 32-bit accumulator, an SPI-compatible serial port with FIFO, dual USARTs, multiple digital input/output ports, a watchdog timer, low-voltage detect, on-chip power-on reset, 16-bit PWM, breakpoints, brownout reset, three timer/counters, and a system clock divider. The MSC1211 and MSC1213 also contain a hardware I^2C peripheral.

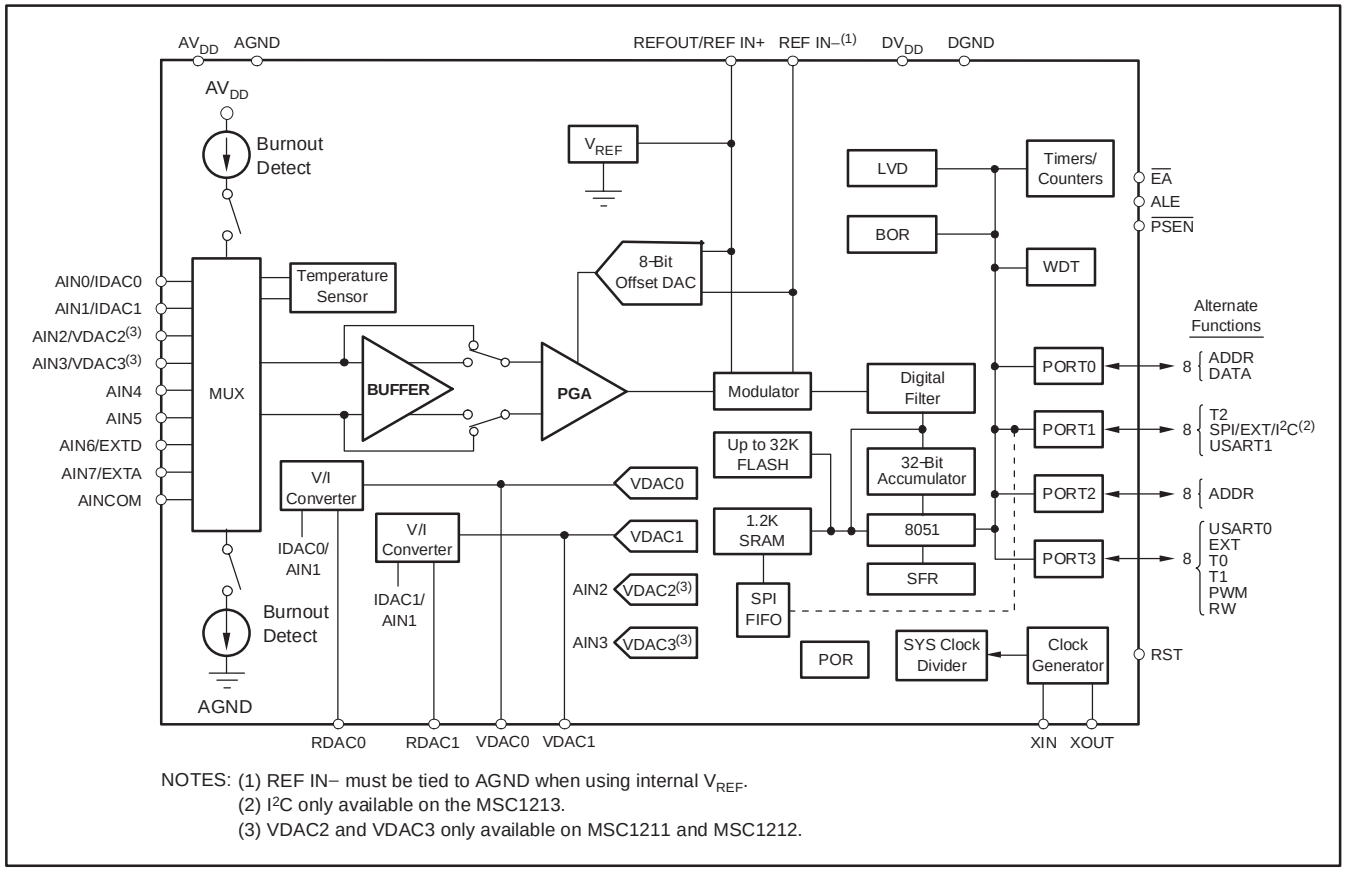
The devices accept low-level differential or single-ended signals directly from a transducer. The ADC provides 24 bits of resolution and 24 bits of no-missing-code performance using a $Sinc^3$ filter with a programmable sample rate. The ADC also has a selectable filter that allows for high-resolution, single-cycle conversion.

The microcontroller core is 8051 instruction set compatible. The microcontroller core is an optimized 8051 core that executes up to three times faster than the standard 8051 core, given the same clock source. This design makes it possible to run the devices at a lower external clock frequency and achieve the same performance at lower power than the standard 8051 core.

The MSC1211/12/13/14 allow users to uniquely configure the Flash and SRAM memory maps to meet the needs of their applications. The Flash is programmable down to 2.7V using both serial and parallel programming methods. The Flash endurance is 100k Erase/Write cycles. In addition, 1280 bytes of RAM are incorporated on-chip.

The parts have separate analog and digital supplies, which can be independently powered from 2.7V to +5.25V. At +3V operation, the power dissipation for each part is typically less than 4mW. The MSC1211/12/13/14 are all available in a TQFP-64 package.

The MSC1211/12/13/14 are designed for high-resolution measurement applications in smart transmitters, industrial process control, weigh scales, chromatography, and portable instrumentation.



NOTES: (1) REF IN− must be tied to AGND when using internal V_{REF}.
(2) I^2C only available on the MSC1213.
(3) VDAC2 and VDAC3 only available on MSC1211 and MSC1212.

Figure 8. Block Diagram

ENHANCED 8051 CORE

All instructions in the MSC1211/12/13/14 families perform exactly the same functions as they would in a standard 8051. The effects on bits, flags, and registers is the same; however, the timing is different. The MSC1211/12/13/14 families utilize an efficient 8051 core which results in an improved instruction execution speed of between 1.5 and 3 times faster than the original core for the same external clock speed (4 clock cycles per instruction versus 12 clock cycles per instruction, as shown in Figure 9). This efficiency translates into an effective throughput improvement of more than 2.5 times, using the same code and same external clock speed. Therefore, a device frequency of 40MHz for the MSC1211/12/13/14 actually performs at an equivalent execution speed of 100MHz compared to the standard 8051 core. This increased performance allows the the device to be run at slower external clock speeds, which reduces system noise and power consumption, but provides greater throughput. This performance difference can be seen in Figure 10. The timing of software loops will be faster with the MSC1211/12/13/14. However, the timer/counter operation of the MSC1211/12/13/14 may be maintained at 12 clocks per increment, or optionally run at 4 clocks per increment.

The MSC1211/12/13/14 also provide dual data pointers (DPTRs) to speed block Data Memory moves.

Additionally, both devices can stretch the number of memory cycles to access external Data Memory from between two and nine instruction cycles in order to accommodate different speeds of memory or devices, as shown in Table 2. The MSC1211/12/13/14 provide an external memory interface with a 16-bit address bus (P0 and P2). The 16-bit address bus makes it necessary to multiplex the low address byte through the P0 port. To enhance P0 and P2 for high-speed memory access, hardware configuration control is provided to configure the ports for external memory/peripheral interface or general-purpose I/O.

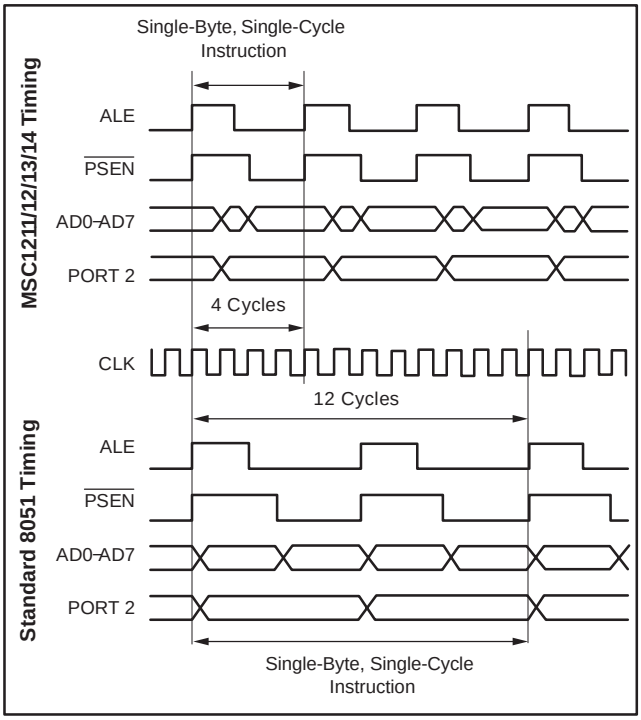


Figure 10. Comparison of MSC1211/12/13/14 Timing to Standard 8051 Timing

CKCON (8Eh) MD2:MD0	INSTRUCTION CYCLES (for MOVX)	$\overline{RD}$ or $\overline{WR}$ STROBE WIDTH (SYS CLKs)	$\overline{RD}$ or $\overline{WR}$ STROBE WIDTH (μs) AT 12MHz
000	2	2	0.167
001	3 (default)	4	0.333
010	4	8	0.667
011	5	12	1.000
100	6	16	1.333
101	7	20	1.667
110	8	24	2.000
111	9	28	2.333

Table 2. Memory Cycle Stretching (stretching of MOVX timing as defined by MD2, MD1, and MD0 bits in CKCON register at address 8Eh).

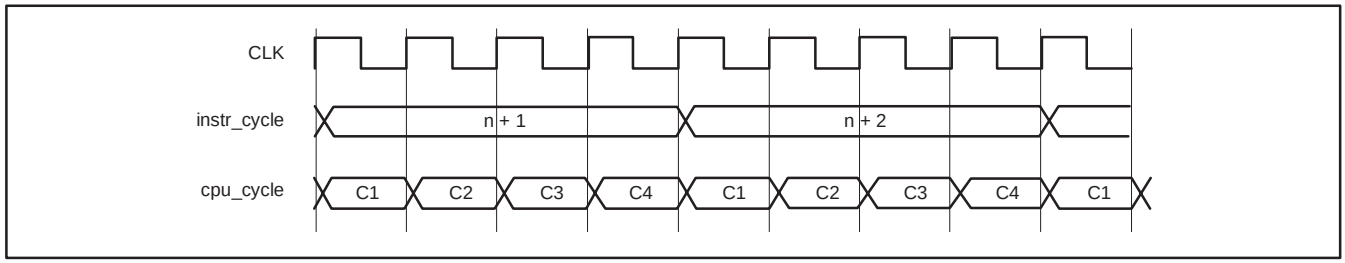


Figure 9. Instruction Timing Cycle

Furthermore, improvements were made to peripheral features that off-load processing from the core, and the user, to further improve efficiency. For instance, the SPI interface uses a FIFO, which allows the SPI interface to transmit and receive data with minimum overhead needed from the core. Also, a 32-bit accumulator was added to significantly reduce the processing overhead for multiple byte data from the ADC or other sources. This allows for 32-bit addition, subtraction and shifting to be accomplished in a few instruction cycles, compared to hundreds of instruction cycles executed through software implementation.

Family Device Compatibility

The hardware functionality and pin configuration across the MSC1211/12/13/14 families are fully compatible. To the user, the only differences between family members are the memory configuration, the number of DACs, and the availability of I^2C for the MSC1211 and MSC1213. This design makes migration between family members simple. This gives the user the ability to add or subtract software functions and to freely migrate between family members. Thus, the MSC1211/12/13/14 can become a standard device used across several application platforms.

Family Development Tools

The MSC1211/12/13/14 are fully compatible with the standard 8051 instruction set. This compatibility means that users can develop software for the MSC1211/12/13/14 with their existing 8051 development tools. Additionally, a complete, integrated development environment is provided with each demo board, and third-party developers also provide support.

Power-Down Modes

The MSC1211/12/13/14 can each power several of the on-chip peripherals and put the CPU into Idle mode. This is accomplished by shutting off the clocks to those sections, as shown in Figure 11.

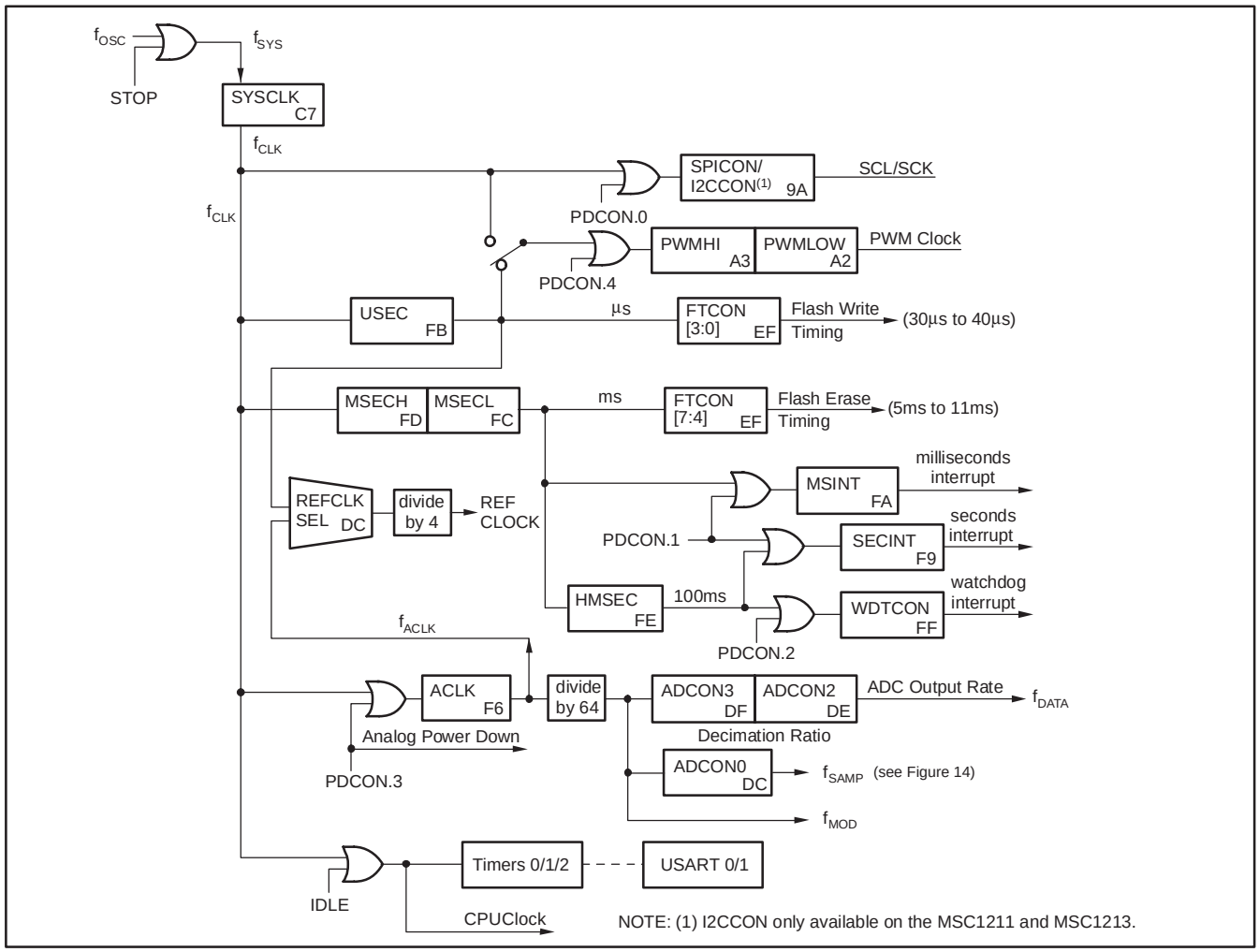


Figure 11. MSC1211/12/13/14 Timing Chain and Clock Control

OVERVIEW

The MSC1211/12/13/14 ADC structure is shown in Figure 12. The figure lists the components that make up the ADC, along with the corresponding special function register (SFR) associated with each component.

ADC INPUT MULTIPLEXER

The input multiplexer provides for any combination of differential inputs to be selected as the input channel, as shown in Figure 13. For example, if AIN0 is selected as the positive differential input channel, then any other channel can be selected as the negative differential input channel. With this method, it is possible to have up to eight fully differential input channels with common connections between them. It is also possible to switch the polarity of the differential input pair to negate any offset voltages. In addition, current sources are supplied that will source or sink current to detect open or short circuits on the pins.

TEMPERATURE SENSOR

On-chip diodes provide temperature sensing capability. When the configuration register for the input MUX is set to all 1s, the diodes are connected to the inputs of the ADC. All other channels are open.

BURNOUT DETECT

When the Burnout Detect (BOD) bit is set in the ADC control configuration register (ADCON0 DCh), two current sources are enabled. The current source on the positive input channel sources approximately 2μA of current. The current source on the negative input channel sinks approximately 2μA. The current sources allow for the detection of an open circuit (full-scale reading) or short circuit (small differential reading) on the selected input differential pair. The buffer should be on for sensor burnout detection.

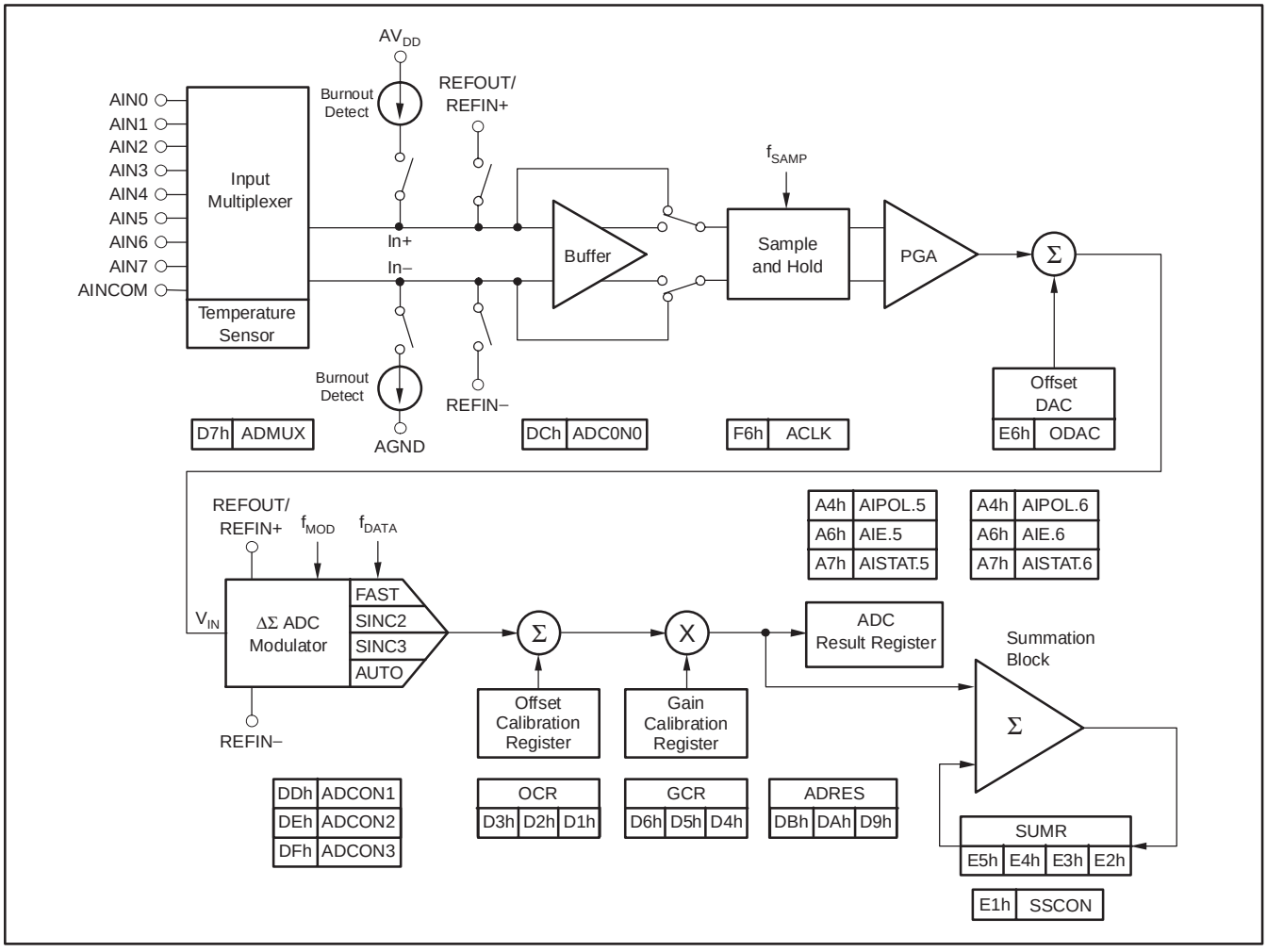


Figure 12. MSC1211/12/13/14 ADC Structure

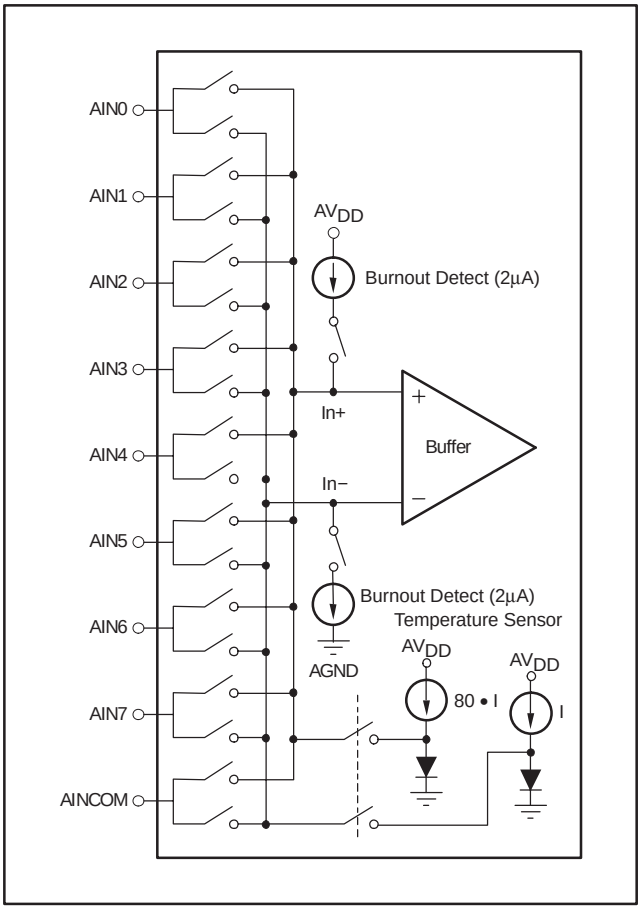


Figure 13. Input Multiplexer Configuration

ADC INPUT BUFFER

The analog input impedance is always high, regardless of PGA setting (when the buffer is enabled). With the buffer enabled, the input voltage range is reduced and the analog power-supply current is higher. If the limitation of input voltage range is acceptable, then the buffer is always preferred. The input impedance of the MSC1211/12/13/14 without the buffer is 7MΩ/PGA. The buffer is controlled by the state of the BUF bit in the ADC control register (ADCON0 DCh).

ADC ANALOG INPUT

When the buffer is not selected, the input impedance of the analog input changes with ACLK clock frequency (ACLK F6h) and gain (PGA). The relationship is:

$$\text{Impedance } (\Omega) = \frac{1}{f_{SAMP} \cdot C_S}$$

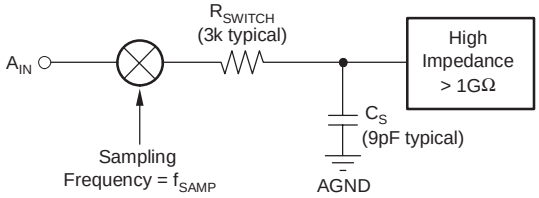
$$A_{IN} \text{ Impedance } (\Omega) = \left(\frac{1 \times 10^6}{\text{ACLK Frequency}}\right) \cdot \left(\frac{7M\Omega}{\text{PGA}}\right)$$

$$\text{where ACLK frequency } (f_{ACLK}) = \frac{f_{CLK}}{\text{ACLK} + 1}$$

$$\text{and modclk} = f_{MOD} = \frac{f_{ACLK}}{64}.$$

NOTE: The input impedance for PGA = 128 is the same as that for PGA = 64 (that is, $\frac{7M\Omega}{64}$).

Figure 14 shows the basic input structure of the MSC1211/12/13/14. The sampling frequency varies according to the PGA settings, as shown in the table in Figure 14.



PGA	CS
1	9pF
2	18pF
4 to 128	36pF

PGA	BIPOLAR MODE FULL-SCALE RANGE	UNIPOLAR MODE FULL-SCALE RANGE	fSAMP
1	±VREF	+VREF	fMOD
2	±VREF/2	+VREF/2	fMOD
4	±VREF/4	+VREF/4	fMOD
8	±VREF/8	+VREF/8	fMOD • 2
16	±VREF/16	+VREF/16	fMOD • 4
32	±VREF/32	+VREF/32	fMOD • 8
64	±VREF/64	+VREF/64	fMOD • 16
128	±VREF/128	+VREF/128	fMOD • 16

NOTE: fMOD = ACLK frequency/64

Figure 14. Analog Input Structure

ADC PGA

The PGA can be set to gains of 1, 2, 4, 8, 16, 32, 64, or 128. Using the PGA can actually improve the effective resolution of the ADC. For instance, with a PGA of 1 on a ±2.5V full-scale range (FSR), the ADC can resolve to 1.5µV. With a PGA of 128 on a ±19mV FSR, the ADC can resolve to 75nV, as shown in Table 3.

Table 3. Sampling Frequency versus PGA Setting

PGA SETTING	BIPOLAR MODE FULL-SCALE RANGE (V)	ENOB(1) AT 10HZ	RMS INPUT-REFERRED NOISE (nV)
1	±2.5V	21.7	1468
2	±1.25	21.5	843
4	±0.625	21.4	452
8	±0.313	21.2	259
16	±0.156	20.8	171
32	±0.0781	20.4	113
64	±0.039	20	74.5
128	±0.019	19	74.5

(1) ENOB = Log_2(FSR/RMS Noise) = $Log_2(2^{24})$ − $Log_2(\sigma_{CODES})$ = 24 − $Log_2(\sigma_{CODES})$

ADC OFFSET DAC

The analog input to the PGA can be offset (in bipolar mode) by up to half the full-scale input range of the PGA by using the ODAC register (SFR E6h). The ODAC (Offset DAC) register is an 8-bit value; the MSB is the sign and the seven LSBs provide the magnitude of the offset. Since the ODAC introduces an analog (instead of digital) offset to the PGA, using the ODAC does not reduce the range of the ADC.

ADC MODULATOR

The modulator is a single-loop, 2nd-order system. The modulator runs at a clock speed (f_{MOD}) that is derived from the CLK using the value in the Analog Clock (ACLK) register (SFR F6h). The data output rate is:

$$\text{Data Rate} = f_{DATA} = \frac{f_{MOD}}{\text{Decimation Ratio}}$$

$$\text{where } f_{MOD} = \frac{f_{CLK}}{(ACLK + 1) \cdot 64} = \frac{f_{ACLK}}{64}$$

and Decimation Ratio is set in [ADCON3:ADCON2].

ADC CALIBRATION

The offset and gain errors in the MSC1211/12/13/14, or the complete system, can be reduced with calibration. Calibration is controlled through the ADCON1 register (SFR DDh), bits CAL2:CAL0. Each calibration process takes seven t_{DATA} periods (data conversion time) to complete. Therefore, it takes 14 t_{DATA} periods to complete both an offset and gain calibration.

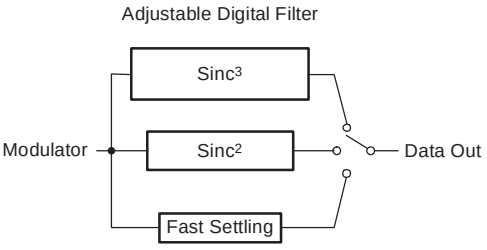
For system calibration, the appropriate signal must be applied to the inputs. The system offset calibration requires a zero input signal. It then computes an offset that will nullify offset in the system. The system gain calibration requires a positive full-scale input signal. It then computes a value to nullify gain errors in the system. Each of these calibrations will take seven t_{DATA} periods to complete.

Calibration should be performed after power on. It should also be done after a change in temperature, decimation ratio, buffer, Power Supply, voltage reference, or PGA. The Offset DAC wil affect offset calibration; therefore, the value of the Offset DAC should be zero until prior to performing a calibration.

At the completion of calibration, the ADC Interrupt bit goes high, which indicates the calibration is finished and valid data is available.

ADC DIGITAL FILTER

The Digital Filter can use either the Fast Settling, $Sinc^2$, or $Sinc^3$ filter, as shown in Figure 15. In addition, the Auto mode changes the Sinc filter after the input channel or PGA is changed. When switching to a new channel, it will use the Fast Settling filter for the next two conversions, the first of which should be discarded.



FILTER SETTLING TIME

FILTER	SETTLING TIME (Conversion Cycles)(1)
$Sinc^3$	3
$Sinc^2$	2
Fast	1

NOTE: (1) MUX change may add one cycle.

AUTO MODE FILTER SELECTION

CONVERSION CYCLE			
1	2	3	4
Fast	Fast	$Sinc^2$	$Sinc^3$

Figure 15. Filter Step Responses

It will then use the Sinc^2 followed by the Sinc^3 filter to improve noise performance. This combines the low-noise advantage of the Sinc^3 filter with the quick response of the Fast Settling Time filter. The frequency response of each filter is shown in Figure 16.

VOLTAGE REFERENCE

The MSC1211/12/13/14 can use either an internal or external voltage reference. The voltage reference selection is controlled via ADC Control Register 0 (ADCON0, SFR DCh). The default power-up configuration for the voltage reference is 2.5V internal.

The internal voltage reference can be selected as either 1.25V or 2.5V. The analog power supply (AV_{DD}) must be within the specified range for the selected internal voltage reference. The valid ranges are: V_{REF} = 2.5 internal (AV_{DD} = 3.3V to 5.25V) and V_{REF} = 1.25 internal (AV_{DD} = 2.7V to 5.25V). If the internal V_{REF} is selected, then AGND must be connected to REF IN−. The REFOUT/REF IN+ pin should also have a 0.1µF capacitor connected to AGND as close as possible to the pin. If the internal V_{REF} is not used, then V_{REF} should be disabled in ADCON0.

If the external voltage reference is selected, it can be used as either a single-ended input or differential input, for ratiometric measures. When using an external reference, it is important to note that the input current will increase for V_{REF} with higher PGA settings and with a higher modulator frequency. The external voltage reference can be used over the input range specified in the *Electrical Characteristics* section.

For applications requiring higher performance than that obtainable from the internal reference, use an external precision reference such as the REF50xx. The internal reference performance can be observed in the noise (and ENOB) versus input signal graphs in the *Typical Characteristics* section. All of the other ENOB plots are obtained with the inputs shorted together. By shorting the inputs, the inherent noise performance of only the ADC can be determined and displayed. When the inputs are not shorted, the extra noise comes from the reference. As can be seen in the ENOB vs Input Signal graph, the external reference adds about 0.7 bits of noise, whereas the internal reference adds about 2.3 bits of noise. This ENOB performance of 19.4 represents 21.16 bits of noise. With an LSB of 298nV, that translates to 6.3µV or a peak-to-peak noise of almost 42µV. The internal reference is initialized each time power is applied. That initialization can cause a shift in the output that is within the specified accuracy. An external reference provides the best noise, drift, and repeatability performance for high-precision applications.

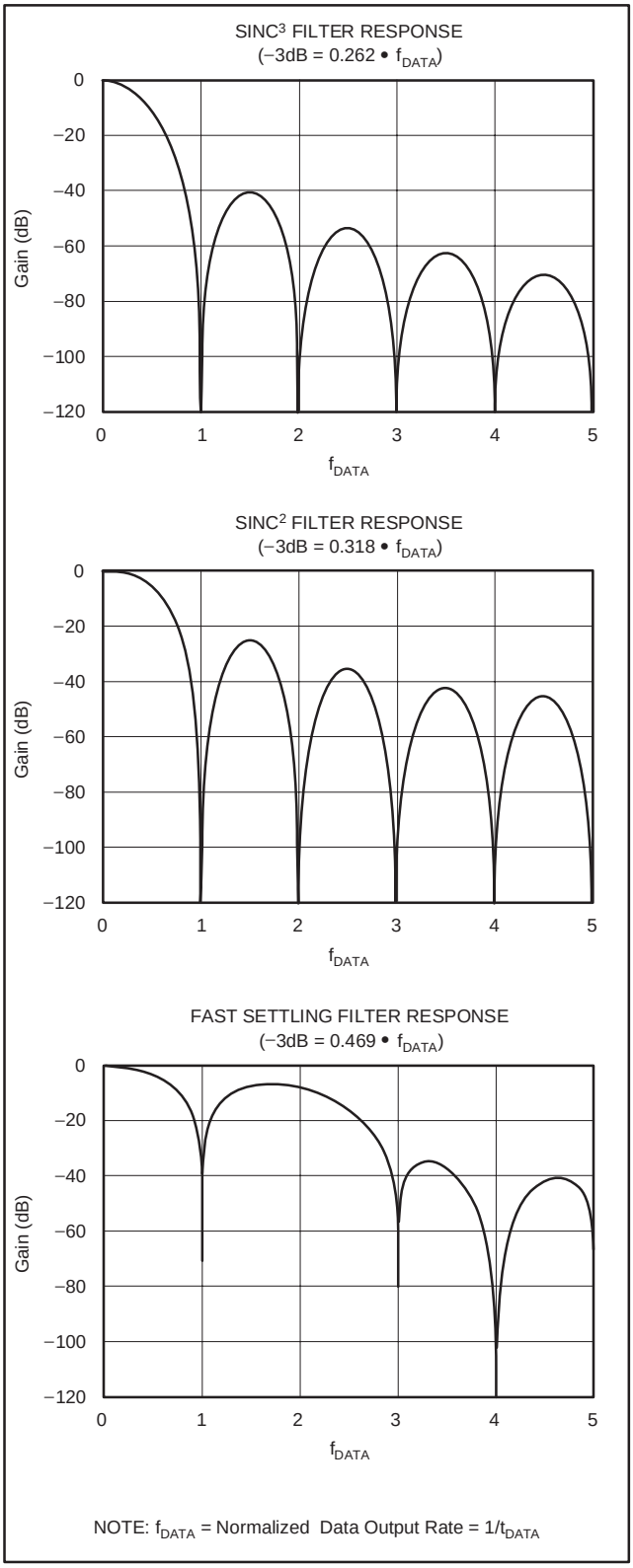


Figure 16. Filter Frequency Responses

VDAC

The architecture of the MSC1211/12/13/14 consists of a string DAC followed by an output buffer amplifier. Figure 17 shows a block diagram of the DAC architecture.

The input coding to the DAC is straight binary, so the ideal output voltage is given by:

$$VDAC = V_{REF} \cdot \left(\frac{D}{65536}\right)$$

where D = decimal equivalent of the binary code that is loaded to the DAC register; it can range from 0 to 65535.

DAC RESISTOR STRING

The DAC selects the voltage from a string of resistors from the reference to AGND. It is essentially a string of resistors, each of value R. The code loaded into the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier by closing one of the switches connecting the string to the amplifier. It is ensured monotonic because of the design architecture.

DAC OUTPUT AMPLIFIER

The output buffer amplifier is capable of generating rail-to-rail voltages on its output, which provides an output range of AGND to AV_{DD}. It is capable of driving a load of 2kΩ in parallel with 1000pF to GND. The source and sink capabilities of the output amplifier can be seen in the typical curves. The slew rate is 1V/µs with a full-scale settling time of 8µs.

DAC REFERENCE

Each DAC can be selected to use the REFOUT/REF IN+ pin voltage or the supply voltage AV_{DD} as the reference for the DAC.

DAC LOADING

The DAC can be selected to be turned off with a 1kΩ, 100kΩ, or open circuit on the DAC outputs.

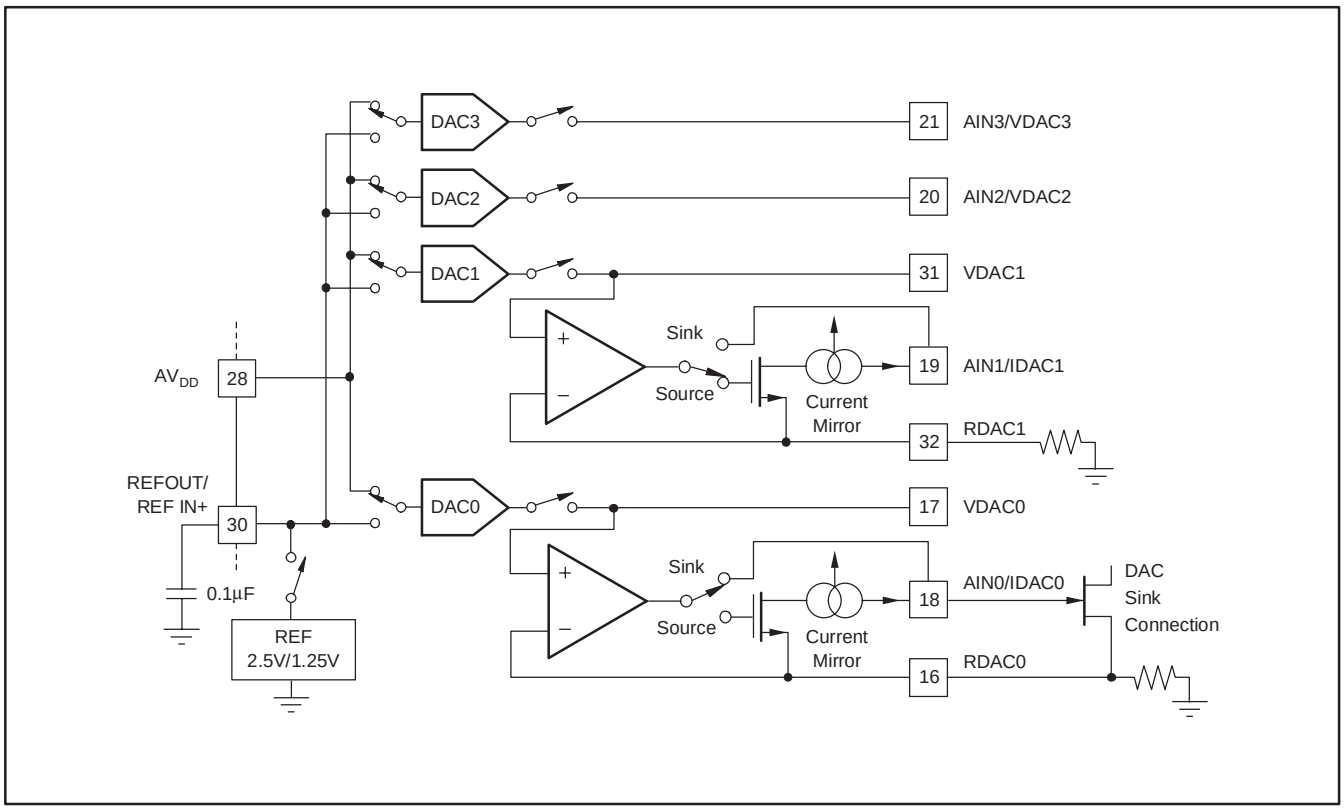


Figure 17. DAC Architecture

BIPOLAR OPERATION USING THE DAC

The DAC can be used for a bipolar output range, as shown in Figure 18; the circuit illustrates an output voltage range of $\pm V_{REF}$. Rail-to-rail operation at the amplifier output is achievable using an OPA703 as the output amplifier.

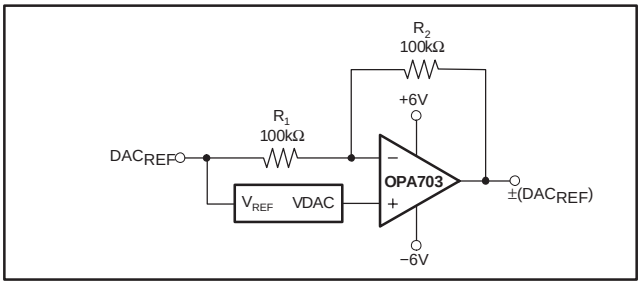


Figure 18. Bipolar Operation with the DAC

The output voltage for any input code can be calculated as follows:

$$V_O = \left[DAC_{REF} \cdot \left(\frac{D}{65536}\right) \cdot \left(\frac{R_1 + R_2}{R_1}\right) - DAC_{REF} \cdot \left(\frac{R_1}{R_2}\right) \right]$$

where *D* represents the input code in decimal (0 to 65535).

With DAC_{REF} = 5V, $R_1 = R_2$:

$$V_O = \left(\frac{10 \cdot D}{65536}\right) - 5V$$

This is an output voltage range of ±5V with 0000h corresponding to a –5V output and FFFFh corresponding to a +5V output. Similarly, using DAC_{REF} = 2.5V, a ±2.5V output voltage can be achieved.

IDAC

The IDAC can source current and sink current (through an external transistor). The compliance specification of the IDAC output defines the maximum output voltage to achieve the expected current.

$$IDAC_{OUT} = \begin{cases} \dfrac{4 \cdot V_{DAC}}{R_{DAC}} & \text{for Source mode} \\ \dfrac{V_{DAC}}{R_{DAC}} & \text{for Sink mode} \end{cases}$$

with $V_{DAC} < (AV_{DD} - 2V)$ for maximum code.

Refer to Figure 17 for the IDAC structure.

ANALOG/DIGITAL LOW-VOLTAGE DETECT

The MSC1211/12/13/14 contain an analog or digital low-voltage detect. When the analog or digital supply drops below the value programmed in LVDCON (SFR E7h), an interrupt is generated (one for each supply).

RESET

The device can be reset from the following sources:

- Power-on reset
- External reset
- Software reset
- Watchdog timer reset
- Brownout reset

An external reset is accomplished by taking the RST pin high for two t_{OSC} periods, followed by taking the RST pin low. A software reset is accomplished through the System Reset register (SRTST, 0F7h). A watchdog timer reset is enabled and controlled through Hardware Configuration Register 0 (HCR0) and the Watchdog Timer register (WDTCON, 0FFh). A brownout reset is enabled through Hardware Configuration Register 1 (HCR1). External reset, software reset, and watchdog timer reset complete after 2^{17} clock cycles. A brownout reset completes after 2^{15} clock cycles.

All sources of reset cause the digital pins to be pulled high from the initiation of the reset. For an external reset, taking the RST pin high stops device operation (crystal oscillation, internal oscillator, or PLL circuit operation) and causes all digital pins to be pulled high from that point. Taking the RST pin low initiates the reset procedure.

A recommended external reset circuit is shown in Figure 19. The serial 10kΩ resistor is recommended for any external reset circuit configuration.

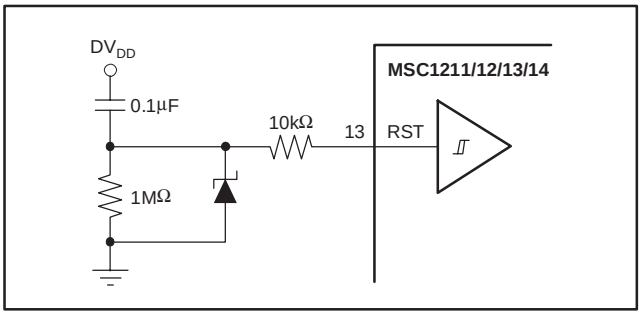


Figure 19. Typical Reset Circuit

POWER ON RESET

The on-chip Power On Reset (POR) circuitry releases the device from reset when $DV_{DD} \approx 2.0V$. The power supply ramp rate does not affect the POR. If the power supply falls below 1.0V for more than 200ms, then the POR will execute. If the power supply falls below 1.0V for less than 200ms, unexpected operation may occur. If these conditions are not met, the POR will not execute. For example, a negative spike on the DV_{DD} supply that does not remain below 1.0V for at least 200ms, will not initiate a POR.

If the Analog/Digital Brownout Reset circuit is on, the POR has no effect.

BROWNOUT RESET

The Brownout Reset (BOR) is enabled through HCR1. If the conditions for proper POR are not met, or the device encounters a brownout condition that does not generate a POR, the BOR can be used to ensure proper device operation. The BOR will hold the state of the device when the power supply drops below the threshold level programmed in HCR1, and then generate a reset when the supply rises above the threshold level. Note that, as the device is released from reset and program execution begins, the device current consumption may increase, which can result in a power supply voltage drop, which may initiate another brownout condition.

The BOR level should be chosen to match closely with the application. That is, with a high external clock frequency, the BOR level should match the minimum operating voltage range for the device or improper operation may still occur.

The BOR voltage is not calibrated until the end of the reset cycle; therefore, the actual BOR voltage will be approxiamtely 25% higher than the selected voltage. This can create a condition where the reset never ends (for example, when selecting a 4.5V BOR voltage for a 5V power supply).

IDLE MODE

Idle mode is entered by setting the IDLE bit in the Power Control register (PCON, 087h). In Idle mode, the CPU, Timer0, Timer1, and USARTs are stopped, but all other peripherals and digital pins remain active. The device can be returned to active mode via an active internal or external interrupt. This mode is typically used for reducing power consumption between ADC samples.

By configuring the device prior to entering Idle mode, further power reductions can be achieved (while in Idle mode). These reductions include powering down peripherals not in use in the PDCON register (0F1h) and reducing the system clock frequency by using the System Clock Divider register (SYSCLK, 0C7h).

STOP MODE

Stop mode is entered by setting the STOP bit in the Power Control register (PCON, 087h). In STOP mode, all internal clocks are halted. This mode has the lowest power consumption. The device can be returned to active mode only via an external or power-on reset (not brownout reset).

By configuring the device prior to entering Stop mode, further power reductions can be achieved (while in Stop mode). These power reductions include halting the external clock into the device, configuring all digital I/O pins as open drain with low output drive, disabling the ADC buffer, disabling the internal V_{REF}, disabling the DACs, and setting PDCON to 0FFh to power down all peripherals.

In Stop mode, all digital pins retain their values. If the BOR is enabled before entering Stop mode, the BOR circuit will continue to draw approximately 25μA of current from the power supply during Stop mode. To minimize power consumption, disable the BOR circuit before entering Stop mode.

POWER CONSUMPTION CONSIDERATIONS

The following suggestions will reduce current consumption in the MSC1211/12/13/14 devices:

1. Use the lowest supply voltage that will work in the application for both AV_{DD} and DV_{DD}.
2. Use the lowest clock frequency that will work in the application.
3. Use Idle mode and the system clock divider whenever possible. Note that the system clock divider also affects the ADC clock.
4. Avoid using 8051-compatible I/O mode on the I/O ports. The internal pull-up resistors will draw current when the outputs are low.
5. Use the delay line for Flash Memory control by setting the FRCM bit in the FMCON register (SFR EEh)
6. Power down peripherals when they are not needed. Refer to SFR PDCON, LVDCON, ADCON0, and DACCONx.

For more information about power cunsumption considerations, refer to application report SBAA139, *Minimizing Power Consumption on the MSC12xx*, available for download at www.ti.com.

MEMORY MAP

The MSC1211/12/13/14 contain on-chip SFR, Flash Memory, Scratchpad SRAM Memory, Boot ROM, and SRAM. The SFR registers are primarily used for control and status. The standard 8051 features and additional peripheral features of the MSC1211/12/13/14 are controlled through the SFR. Reading from an undefined SFR will return zero; writing to an undefined SFR is not recommended, and will have indeterminate effects.

Flash Memory is used for both Program Memory and Data Memory. The user has the ability to select the partition size of Program and Data Memory. The partition size is set through hardware configuration bits, which are programmed through either the parallel or serial programming methods. Both Program and Data Flash Memory are erasable and writable (programmable) in User Application mode (UAM). However, program execution can only occur from Program Memory. As an added precaution, a lock feature can be activated through the hardware configuration bits, which disables erase and writes to 4kB of Program Flash Memory or the entire Program Flash Memory in UAM.

The MSC1211/12/13/14 include 1kB of SRAM on-chip. SRAM starts at address 0 and is accessed through the MOVX instruction. This SRAM can also be located to start at 8400h and can be accessed as both Program and Data Memory.

FLASH MEMORY

The page size for Flash memory is 128 bytes. The respective page must be erased before it can be written to, regardless of whether it is mapped to Program or Data Memory space. The MSC1211/12/13/14 use a memory addressing scheme that separates Program Memory (FLASH/ROM) from Data Memory (FLASH/RAM). Each area is 64kB beginning at address 0000h and ending at FFFFh, as shown in Figure 20. The program and data segments can overlap since they are accessed in different ways. Program Memory is fetched by the microcontroller automatically. There is one instruction (MOVC) that is used to explicitly read the program area. This instruction is commonly used to read lookup tables. The Data Memory area is accessed explicitly using the MOVX instruction. This instruction provides multiple ways of specifying the target address. It is also used to access the 64kB of Data Memory. The address and data range of devices with on-chip Program and Data Memory overlap the 64kB memory space. When on-chip memory is enabled, accessing memory in the on-chip range will cause the device to access internal memory. Memory accesses beyond the internal range will be addressed externally via Ports 0 and 2.

The MSC1211/12/13/14 have two hardware configuration registers (HCR0 and HCR1) that are programmable only during Flash Memory Programming mode.

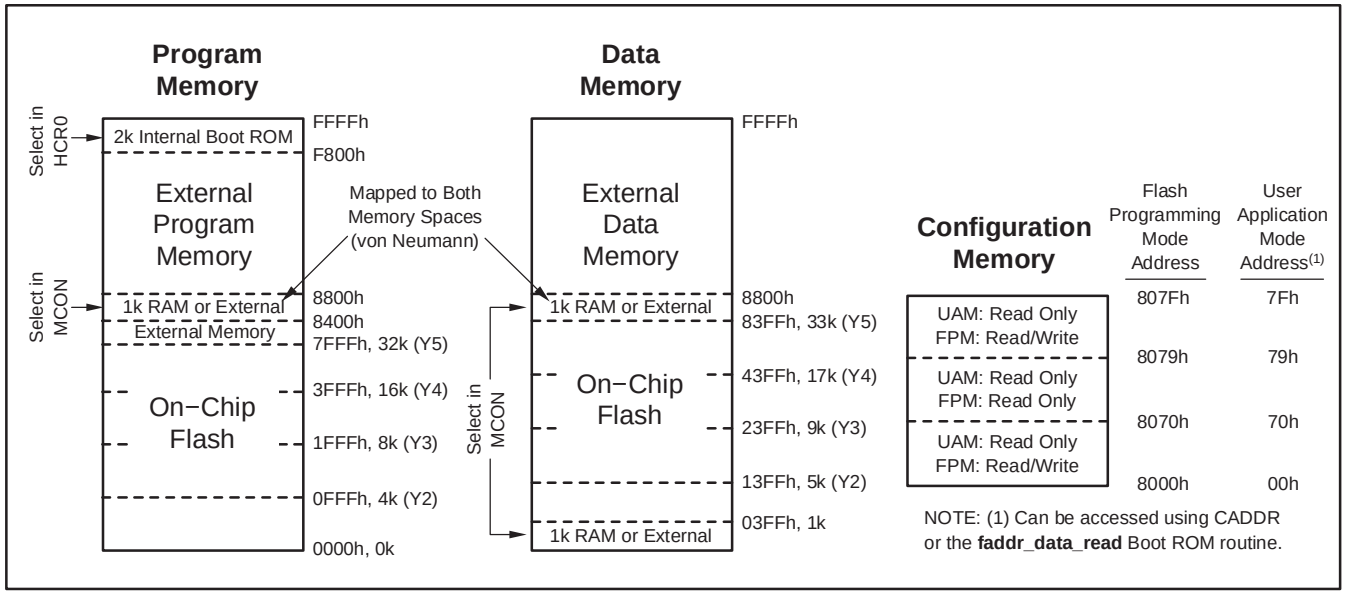


Figure 20. Memory Map

The MSC1211/12/13/14 allow the user to partition the Flash Memory between Program Memory and Data Memory. For instance, the MSC1213Y5 contains 32kB of Flash Memory on-chip. Through the hardware configuration registers, the user can define the partition between Program Memory (PM) and Data Memory (DM), as shown in Table 4 and Table 5. The MSC1211/12/13/14 families offer four memory configurations.

Table 4. MSC1211/12/13/14 Flash Partitioning

HCR0	MSC121xY2		MSC121xY3		MSC121xY4		MSC121xY5	
DFSEL	PM	DM	PM	DM	PM	DM	PM	DM
000	0kB	4kB	0kB	8kB	0kB	16kB	0kB	32kB
001	0kB	4kB	0kB	8kB	0kB	16kB	0kB	32kB
010	0kB	4kB	0kB	8kB	0kB	16kB	16kB	16kB
011	0kB	4kB	0kB	8kB	8kB	8kB	24kB	8kB
100	0kB	4kB	4kB	4kB	12kB	4kB	28kB	4kB
101	2kB	2kB	6kB	2kB	14kB	2kB	30kB	2kB
110	3kB	1kB	7kB	1kB	15kB	1kB	31kB	1kB
111 (default)	4kB	0kB	8kB	0kB	16kB	0kB	32kB	0kB

NOTE: When a 0kB Program Memory configuration is selected, program execution is external.

Table 5. MSC1211/12/13/14 Flash Memory Partitioning

HCR0	MSC121xY2		MSC121xY3		MSC121xY4		MSC121xY5	
DFSEL	PM	DM	PM	DM	PM	DM	PM	DM
000	0000	0400-13FF	0000	0400-23FF	0000	0400-43FF	0000	0400-83FF
001	0000	0400-13FF	0000	0400-23FF	0000	0400-43FF	0000	0400-83FF
010	0000	0400-13FF	0000	0400-23FF	0000	0400-43FF	0000-3FFF	0400-43FF
011	0000	0400-13FF	0000	0400-23FF	0000-1FFF	0400-23FF	0000-5FFF	0400-23FF
100	0000	0400-13FF	0000-0FFF	0400-13FF	0000-2FFF	0400-13FF	0000-6FFF	0400-13FF
101	0000-07FF	0400-0BFF	0000-17FF	0400-0BFF	0000-37FF	0400-0BFF	0000-77FF	0400-0BFF
110	0000-0BFF	0400-07FF	0000-1BFF	0400-07FF	0000-3BFF	0400-07FF	0000-7BFF	0400-07FF
111 (default)	0000-0FFF	− −	0000-1FFF	− −	0000-3FFF	− −	0000-7FFF	− −

NOTE: Program Memory accesses above the highest listed address will access external Program Memory.

It is important to note that the Flash Memory is readable and writable by the user through the MOVX instruction when configured as either Program or Data Memory (via the MXWS bit in the MWS SFR 8Fh). This flexibility means that the device can be partitioned for maximum Flash Program Memory size (no Flash Data Memory) and Flash Program Memory can be used as Flash Data Memory. However, this configuration may lead to undesirable behavior if the PC points to an area of Flash Program Memory that is being used for data storage. Therefore, it is recommended to use Flash partitioning when Flash Memory is used for data storage. Flash partitioning prohibits execution of code from Data Flash Memory. Additionally, the Program Memory erase/write can be disabled through hardware configuration bits (HCR0), while still providing access (read/write/erase) to Data Flash Memory.

The effect of memory mapping on Program and Data Memory is straightforward. The Program Memory is decreased in size from the top of internal Program Memory. Therefore, for example, if the MSC1213Y5 is partitioned with 31kB of Flash Program Memory and 1kB of Flash Data Memory, external Program Memory execution will begin at 7C00h (versus 8000h for 32kB). The Flash Data Memory is added on top of the SRAM memory. Thus, access to Data Memory (through MOVX) will access SRAM for addresses 0000h−03FFh and access Flash Memory for addresses 0400h−07FFh.

Data Memory

The MSC1211/12/13/14 can address 64kB of Data Memory. Scratchpad Memory provides 256 bytes in addition to the 64kB of Data Memory. The MOVX instruction is used to access the Data SRAM Memory. This includes 1024 bytes of on-chip Data SRAM Memory. The data bus values do not appear on Port 0 (during data bus timing) for internal memory access.

The MSC1211/12/13/14 also have on-chip Flash Data Memory which is readable and writable (depending on Memory Write Select register) during normal operation (full V_{DD} range). This memory is mapped into the external Data Memory space directly above the SRAM.

The MOVX instruction is used to write to Flash Memory. Flash Memory must be erased before it can be written. Flash Memory is erased in 128 byte pages.

CONFIGURATION MEMORY

The MSC121x Configuration Memory consists of 128 bytes. In UAM, all Configuration Memory is readable using the **faddr_data_read** Boot ROM routine, and the CADDR and CDATA registers. In UAM, however, none of the Configuration Memory is writable.

In serial or parallel programming mode, all Configuration Memory is readable. Most locations are also writable, except for addresses 8070h through 8079h, which are read-only.

The two hardware configuration registers reside in configuration memory at 807Eh (HCR1) and 807Fh (HCR0).

Figure 21 shows the configuration register mapping for programming mode and UAM. Note that reading/writing configuration memory in Flash Programming mode (FPM) requires 16-bit addressing; whereas, reading configuration memory in User Application mode (UAM) requires only 8-bit addressing.

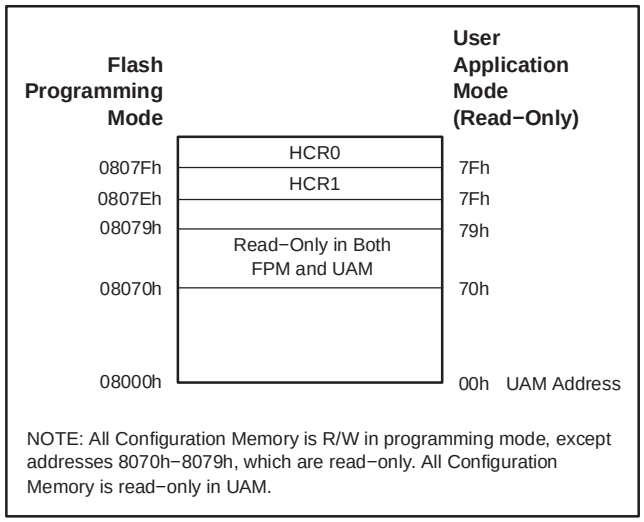


Figure 21. Configuration Memory Mapping for Programming Mode and UAM

REGISTER MAP

Figure 22 illustrates the Register Map. It is entirely separate from the Program and Data Memory areas discussed previously. A separate class of instructions is used to access the registers. There are 256 potential register locations. In practice, the MSC1211/12/13/14 have 256 bytes of Scratchpad RAM and up to 128 SFRs.

This is possible, since the upper 128 Scratchpad RAM locations can only be accessed indirectly. Thus, a direct reference to one of the upper 128 locations must be an SFR access. Direct RAM is reached at locations 0 to 7Fh (0 to 127).

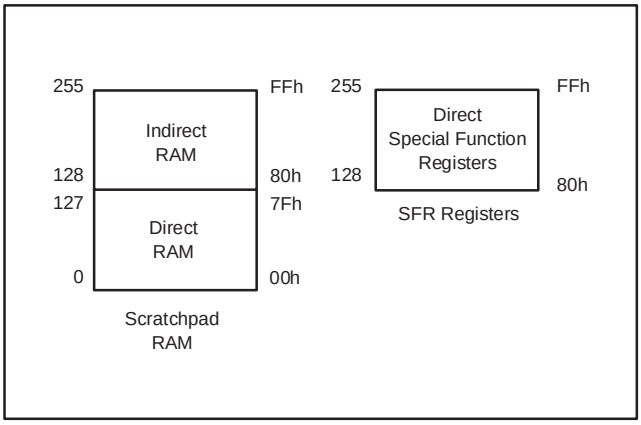


Figure 22. Register Map

SFRs are accessed directly between 80h and FFh (128 to 255). The RAM locations between 128 and 255 can be reached through an indirect reference to those locations. Scratchpad RAM is available for general-purpose data storage. It is commonly used in place of off-chip RAM when the total data contents are small. When off-chip RAM is needed, the Scratchpad area will still provide the fastest general-purpose access. Within the 256 bytes of RAM, there are several special-purpose areas.

Bit Addressable Locations

In addition to direct register access, some individual bits are also accessible. These are individually addressable bits in both the RAM and SFR area. In the Scratchpad RAM area, registers 20h to 2Fh are bit addressable. This provides 128 (16 • 8) individual bits available to software. A bit access is distinguished from a full-register access by the type of instruction. In the SFR area, any register location ending in a 0 or 8 is bit addressable. Figure 23 shows details of the on-chip RAM addressing including the locations of individual RAM bits.

Working Registers

As part of the lower 128 bytes of RAM, there are four banks of Working Registers, as shown in Figure 23. The Working Registers are general-purpose RAM locations that can be addressed in a special way. They are designated R0 through R7. Since there are four banks, the currently selected bank will be used by any instruction using R0—R7. This design allows software to change context by simply switching banks. Bank access is controlled via the Program Status Word register (PSW; 0D0h) in the SFR area described below. Registers R0 and R1 also allow their contents to be used for indirect addressing of the upper 128 bytes of RAM.

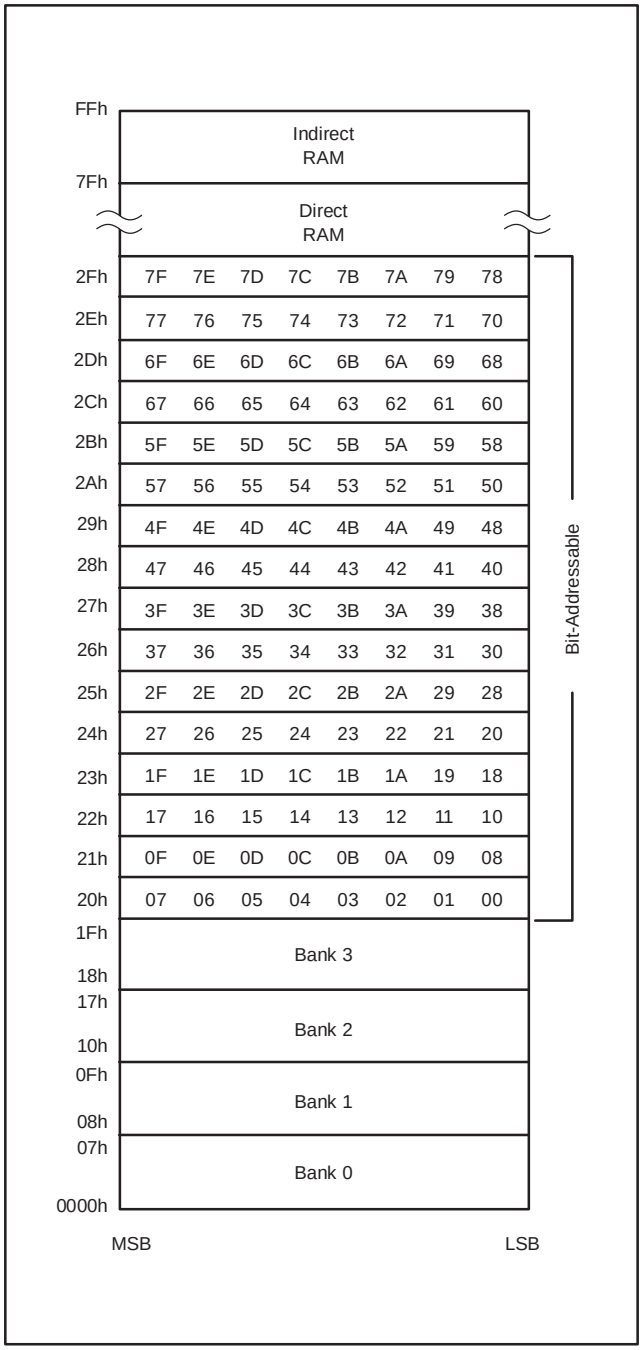


Figure 23. Scratchpad Register Addressing

Thus, an instruction can designate the value stored in R0 (for example) to address the upper RAM. The 16 bytes immediately above the these registers are bit addressable. So any of the 128 bits in this area can be directly accessed using bit addressable instructions.

Stack

Another use of the Scratchpad area is for the programmer's stack. This area is selected using the Stack Pointer (SP; 81h) SFR. Whenever a call or interrupt is invoked, the return address is placed on the Stack. It also is available to the programmer for variables, etc., since the Stack can be moved and there is no fixed location within the RAM designated as Stack. The Stack Pointer will default to 07h on reset. The user can then move it as needed. A convenient location would be the upper RAM area (> 7Fh) since this is only available indirectly. The SP will point to the last used value. Therefore, the next value placed on the Stack is put at SP + 1. Each PUSH or CALL will increment the SP by the appropriate value. Each POP or RET will decrement as well.

Program Memory

After reset, the CPU begins execution from Program Memory location 0000h. The selection of where Program Memory execution begins is made by tying the $\overline{EA}$ pin to DV_{DD} for internal access, or DGND for external access. When $\overline{EA}$ is tied to DV_{DD}, any PC fetches outside the internal Program Memory address occur from external memory. If $\overline{EA}$ is tied to DGND, then all PC fetches address external memory. Table 6 shows the standard internal Program Memory size for MSC1211/12/13/14 family members. If enabled the Boot ROM will appear from address F800h to FFFFh.

Table 6. MSC1211/12/13/14 Maximum Internal Program Memory Sizes

MODEL NUMBER	STANDARD INTERNAL PROGRAM MEMORY SIZE (BYTES)
MSC121xY5	32k
MSC121xY4	16k
MSC121xY3	8k
MSC121xY2	4k

ACCESSING EXTERNAL MEMORY

If external memory is used, P0 and P2 must be configured as address and data lines. If external memory is not used, P0 and P2 can be configured as general-purpose I/O lines through the hardware configuration register (HCR0, HCR1).

To enable access to external memory, bits 0 and 1 of the HCR1 register must be set to '0'. When these bits are enabled all memory accesses for both internal and external memory will appear on Ports 0 and 2. During the data portion of the cycle for internal memory, Port 0 will be zero for security purposes.

Accesses to external memory are of two types: to external Program Memory and to external Data Memory. Accesses to external Program Memory use signal $\overline{PSEN}$ (program store enable) as the read strobe. Accesses to external Data Memory use $\overline{RD}$ or $\overline{WR}$ (alternate functions of P3.7 and P3.6) to strobe the memory.

If desired, External Program Memory and external Data Memory may be combined by applying the $\overline{RD}$ and $\overline{PSEN}$ signals to the inputs of an AND gate and using the output of the gate as the read strobe to the external Program/Data Memory.

A program fetch from external Program Memory uses a 16-bit address. Accesses to external Data Memory can use either a 16-bit address (MOVX @DPTR) or an 8-bit address (MOVX @R_I).

If Port 2 is selected for external memory use (HCR1, bit 0), it cannot be used as general-purpose I/O. This bit (or Bit 1 of HCR1) also forces bits P3.6 and P3.7 to be used for $\overline{WR}$ and $\overline{RD}$ instead of I/O. Port 2, P3.6, and P3.7 should all be written to '1.'

If an 8-bit address is being used (MOVX @R_I), the contents of the MPAGE (92h) SFR remain at the Port 2 pins throughout the external memory cycle, which facilitates paging.

In any case, the low byte of the address is time-multiplexed with the data byte on Port 0. The ADDR/DATA signals use CMOS drivers in the Port 0, Port 2, $\overline{WR}$, and $\overline{RD}$ output buffers. Thus, in this application, the Port 0 pins are not open-drain outputs, and do not require external pull-ups for high-speed access. Signal ALE (Address Latch Enable) should be used to capture the address byte into an external latch. The address byte is valid at the negative transition of ALE. Then, in a write cycle, the data byte to be written appears on Port 0 just before $\overline{WR}$ is activated, and remains there until after $\overline{WR}$ is deactivated. In a read cycle, the incoming byte is accepted at Port 0 just before the read strobe is deactivated.

The functions of Port 0 and Port 2 are selected in HCR1. (Hardware configuration registers can only be changed during Flash Programming mode.) The default state is for Port 0 and Port 2 to be used as general-purpose I/O. If an external memory access is attempted when they are configured as general-purpose I/O, the values of Port 0 and Port 2 will not be affected.

External Program Memory is accessed under two conditions:

1. Whenever signal $\overline{EA}$ is low during reset, then all future code and data accesses are external; or
2. Whenever the Program Counter (PC) contains a number that is outside of the internal Program Memory address range, if the ports are enabled.

If Port 0 and Port 2 are selected for external memory, all 8 bits of Port 0 and Port 2, as well as P3.6 and P3.7, are dedicated to an output function and may not be used for general-purpose I/O. During external program fetches, Port 2 outputs the high byte of the PC.

Programming Flash Memory

There are four sections of Flash Memory for programming:

1. 128 configuration bytes.
2. Reset sector (4kB) (not to be confused with the 2kB Boot ROM).
3. Program Memory.
4. Data Memory.

Boot ROM

There is a 2kB Boot ROM that controls operation during serial or parallel programming. Additionally, the Boot ROM routines can be accessed during the user mode if it is enabled. When enabled, the Boot ROM routines will be located at memory addresses F800h−FFFFh during user mode. In program mode the Boot ROM is located in the first 2kB of Program Memory. For additional information, refer to Application Note SBAA085, available for download from the TI web site (www.ti.com).

The MSC1211/12/13/14 are shipped with Flash Memory erased (all 1s). Parallel programming methods typically involve a third-party programmer. Serial programming methods typically involve in-system programming. UAM allows Code Program and Data Memory programming. The actual code for Flash programming cannot execute from Flash. That code must execute from the Boot ROM or internal (von Neumann) RAM.

Flash Programming Mode

There are two programming modes: parallel and serial. The programming mode is selected by the state of the ALE and $\overline{\text{PSEN}}$ signals during reset (BOR, WDT, software, or POR). Serial programming mode is selected with $\overline{\text{PSEN}}$ = 0 and ALE = 1. Parallel programming mode is selected with $\overline{\text{PSEN}}$ = 1 and ALE = 0, as shown in Figure 24. If they are both high, the MSC1211/12/13/14 will operate in User Application mode. For both signals, low is a reserved mode and is not defined. Programming mode is exited with a reset and the normal mode selected.

Figure 25 shows the serial programming conection.

Serial programming mode works through USART0, and has special protocols. Table 7 describes these protocols, which are discussed at length in Application Note SBAA076 (available for download at www.ti.com). The serial programming mode works at a maximum baud rate determined by f_{OSC}.

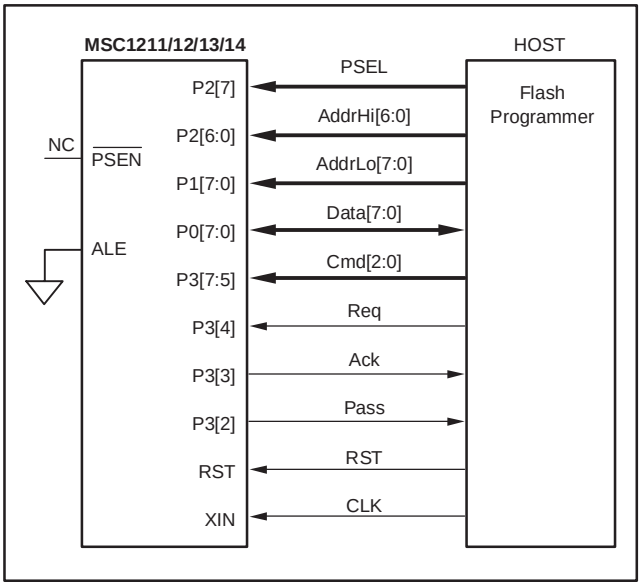


Figure 24. Parallel Programming Configuration

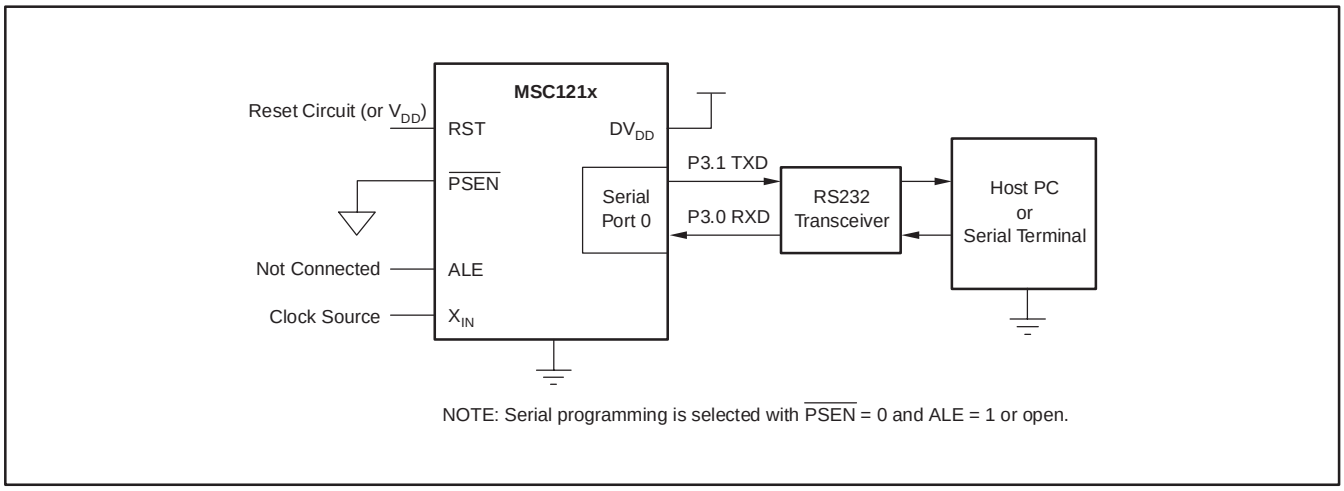


Figure 25. Serial Programming Connection

Table 7. MSC121x Boot ROM Routines

ADDRESS	ROUTINE	C DECLARATIONS	DESCRIPTION
FFD5	put_string	void put_string (char code *string);	Output string
FFD7	page_erase	char page_erase (int faddr, char fdata, char fdm);	Erase flash page
FFD9	write_flash	Assembly only; DPTR = address, R5 = data	Fast flash write
FFDB	write_flash_chk	char write_flash_chk (int faddr, char fdata, char fdm);	Write flash byte, verify
FFDD	write_flash_byte	char write_flash_byte (int faddr, char fdata, char fdm);	Write flash byte
FFDF	faddr_data_read	char faddr_data_read (char faddr);	Read HW config byte from addr
FFE1	data_x_c_read	char data_x_c_read (int faddr, char fdm);	Read xdata or code byte
FFE3	tx_byte	void tx_byte (char);	Send byte to USART0
FFE5	tx_hex	void tx_hex (char);	Send hex value to USART0
FFE7	putok	void putok (void);	Send “OK” to USART0
FFE9	rx_byte	char rx_byte (void);	Read byte from USART0
FFEB	rx_byte_echo	char rx_byte_echo (void);	Read and echo byte on USART0
FFED	rx_hex_echo	int rx_hex_echo (void);	Read and echo hex on USART0
FFEF	rx_hex_int_echo	int rx_hex_int_echo (void);	Read int as hex and echo: USART0
FFF1	rx_hex_rev_echo	int rx_hex_rev_echo (void);	Read int reversed as hex and echo: USART0
FFF3	autobaud	void autobaud (void);	Set baud with received CR
FFF5	putspace4	void putspace4 (void);	Output 4 spaces to USART0
FFF7	putspace3	void putspace3 (void);	Output 3 spaces to USART0
FFF9	putspace2	void putspace2 (void);	Output 2 spaces to USART0
FFFB	putspace1	void putspace1 (void);	Output 1 space to USART0
FFFB	putcr	void putcr (void);	Output CR, LF to USART0
F97D(1)	cmd_parse	void cmd_parser (void);	See SBAA076
FD3B(1)	monitor_isr	void monitor_isr ( ) interrupt 6	Push registers and call cmd_parser

(1) These addresses only relate to version 1.0 of the MSC1211/12/13/14 Boot ROM.

INTERRUPTS

The MSC1211/12/13/14 use a three-priority interrupt system. As shown in Table 8, each interrupt source has an independent priority bit, flag, interrupt vector, and enable (except that nine interrupts share the Auxiliary Interrupt (AI) at the highest priority). In addition, interrupts can be globally enabled or disabled. The interrupt structure is compatible with the original 8051 family. All of the standard interrupts are available.

Table 8. Interrupt Summary

INTERRUPT/EVENT	INTERRUPT ADDR	INTERRUPT NUM	PRIORITY	FLAG	ENABLE	PRIORITY CONTROL
DV_{DD} Low Voltage/HW Break-point	33h	6	High	EDLVB (AIE.0 or AIPOL.0)(1)(2) EBP (BPCON.7)(1)	EDLVB (AIE.0)(1) EBP (BPCON.0)(1)	N/A
AV_{DD} Low Voltage	33h	6	0	EALV (AIE.1 or AIPOL.1)(1)(2)	EALV (AIE.1)(1)	N/A
SPI Receive / I^2C(3)	33h	6	0	ESPIR/EI2C (AIE.2 or AIPOL.2)(1)(2)	ESPIR/EI2C (AIE.2)(1)	N/A
SPI Transmit	33h	6	0	ESPIT (AIE.3 or AIPOL.3)(1)(2)	ESPIT (AIE.3)(1)	N/A
Milliseconds Timer	33h	6	0	EMSEC (AIE.4 or AIPOL.4)(1)(2)	EMSEC (AIE.4)(1)	N/A
ADC	33h	6	0	EADC (AIE.5 or AIPOL.5)(1)(2)	EADC (AIE.5)(1)	N/A
Summation Register	33h	6	0	ESUM (AIE.6 or AIPOL.6)(1)(2)	ESUM (AIE.6)(1)	N/A
Seconds Timer	33h	6	0	ESEC (AIE.7 or AIPOL.7)(1)(2)	ESEC (AIE.7)(1)	N/A
External Interrupt 0	03h	0	1	IE0 (TCON.1)(4)	EX0 (IE.0)(6)	PX0 (IP.0)
Timer 0 Overflow	0Bh	1	2	TF0 (TCON.5)(5)	ET1 (IE.1)(6)	PT0 (IP.1)
External Interrupt 1	13h	2	3	IE1 (TCON.3)(4)	EX1 (IE.2)(6)	PX1 (IP.2)
Timer 1 Overflow	0Bh	3	4	TF1 (TCON.7)(5)	ET1 (IE.3)(6)	PT1 (IP.3)
Serial Port 0	23h	4	5	RI_0 (SCON0.0) TI_0 (SCON0.1)	ES0 (IE.4)(6)	PS0 (IP.4)
Timer 2 Overflow	2Bh	5	6	TF2 (T2CON.7)	ET2 (IE.5)(6)	PT2 (IP.5)
Serial Port 1	3Bh	7	7	RI_1 (SCON1.0) TI_1 (SCON1.1)	ES1 (IE.6)(6)	PS1 (IP.6)
External Interrupt 2	43h	8	8	IE2 (EXIF.4)(4)	EX2 (EIE.0)(6)	PX2 (EIP.0)
External Interrupt 3	4Bh	9	9	IE3 (EXIF.5)(4)	EX3 (EIE.1)(6)	PX3 (EIP.1)
External Interrupt 4	53h	10	10	IE4 (EXIF.6)(4)	EX4 (EIE.2)(6)	PX4 (EIP.2)
External Interrupt 5	5Bh	11	11	IE5 (EXIF.7)(4)	EX5 (EIE.3)(6)	PX5 (EIP.3)
Watchdog	63h	12	12 Low	WDTI (EICON.3)	EWDI (EIE.4)(6)	PWDI (EIP.4)

(1) These interrupts set the AI flag (EICON.4) and are enabled by EAI (EICON.5).
(2) For AIPOL.RDSEL = 1, reading AIPOL register gives current value of Auxiliary interrupts before masking. Reading AIE register gives value of AIE register contents.
For AIPOL.RDSEL = 0, Reading AIPOL register gives value of AIE register contents. Reading AIE register gives current value of Auxiliary interrupts before masking.
(3) I^2C is only available on the MSC1211 and MSC1213.
(4) If edge-triggered, cleared automatically by hardware on interrupt service routine vector. For EX0 or EX1, if level-triggered, the flag follows the state of the pin.
(5) Cleared automatically by hardware when interrupt vector occurs.
(6) Globally enabled by $\overline{EA}$ (IE.7).

Hardware Configuration Register 0 (HCR0)—Accessed Using SFR Registers CADDR and CDATA.

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CADDR 7Fh	EPMA	PML	RSL	EBR	EWDR	DFSEL2	DFSEL1	DFSEL0

NOTE: HCR0 is programmable only in Flash Programming mode, but can be read in User Application mode using the CADDR and CDATA SFRs or the **faddr_data_read** Boot ROM routine.

EPMA **Enable Programming Memory Access (Security Bit).**
bit 7
0: After reset in programming modes, Flash Memory can only be accessed in UAM until a mass erase is done.
1: Fully Accessible (default)

PML **Program Memory Lock (PML has priority over RSL).**
bit 6
0: Enable writing to Program Memory in UAM.
1: Disable writing to Program Memory in UAM (default).

RSL **Reset Sector Lock.** The reset sector can be used to provide another method of Flash Memory programming, which
bit 5 allows Program Memory updates without changing the jumpers for in-circuit code updates or program development. The code in this boot sector would then provide the monitor and programming routines with the ability to jump into the main Flash code when programming is finished.
0: Enable Reset Sector Writing
1: Enable Read-Only Mode for Reset Sector (4kB) (default)

EBR **Enable Boot ROM.** Boot ROM is 2kB of code located in ROM, not to be confused with the 4kB Boot Sector located
bit 4 in Flash Memory.
0: Disable Internal Boot ROM
1: Enable Internal Boot ROM (default)

EWDR **Enable Watchdog Reset.**
bit 3
0: Disable Watchdog Reset
1: Enable Watchdog Reset (default)

DFSEL1−0 **Data Flash Memory Size (see Table 4 and Table 5).**
bits 2−0
000: Reserved
001: 32kB, 16kB, 8kB, or 4kB Data Flash Memory
010: 16kB, 8kB, or 4kB Data Flash Memory
011: 8kB or 4kB Data Flash Memory
100: 4kB Data Flash Memory
101: 2kB Data Flash Memory
110: 1kB Data Flash Memory
111: No Data Flash Memory (default)

Hardware Configuration Register 1 (HCR1)

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CADDR 7Eh	DBLSEL1	DBLSEL0	ABLSEL1	ABLSEL0	DAB	DDB	EGP0	EGP23

NOTE: HCR1 is programmable only in Flash Programming mode, but can be read in User Application mode using the CADDR and CDATA SFRs or the **faddr_data_read** Boot ROM routine.

DBLSEL **Digital Supply Brownout Level Select**
bits 7−6 00: 4.5V
01: 4.2V
10: 2.7V
11: 2.5V (default)

ABLSEL **Analog Supply Brownout Level Select**
bits 5−4 00: 4.5V
01: 4.2V
10: 2.7V
11: 2.5V (default)

DAB **Disable Analog Power-Supply Brownout Reset**
bit 3 0: Enable Analog Brownout Reset
1: Disable Analog Brownout Reset (default)

DDB **Disable Digital Power-Supply Brownout Reset**
bit 2 0: Enable Digital Brownout Reset
1: Disable Digital Brownout Reset (default)

EGP0 **Enable General-Purpose I/O for Port 0**
bit 1 0: Port 0 is Used for External Memory, P3.6 and P3.7 Used for $\overline{WR}$ and $\overline{RD}$.
1: Port 0 is Used as General-Purpose I/O (default)

EGP23 **Enable General-Purpose I/O for Ports 2 and 3**
bit 0 0: Port 2 is Used for External Memory, P3.6 and P3.7. Used for $\overline{WR}$ and $\overline{RD}$.
1: Port 2 and Port3 are Used as General-Purpose I/O (default)

Configuration Memory Programming

Hardware Configuration Memory can be changed only in Serial Flash Programming mode or Parallel Programming mode.

Table 9. Special Function Registers

NOTE: (**Boldface** are in addition to standard 8051 registers, and unique to the MSC1211/12/13/14).

ADDRESS	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	RESET VALUE
80h	P0	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	FFh
81h	SP									07h
82h	DPL0									00h
83h	DPH0									00h
84h	**DPL1**									**00h**
85h	**DPH1**									**00h**
86h	**DPS**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**SEL**	**00h**
87h	**PCON**	**SMOD**	**0**	**1**	**1**	**GF1**	**GF0**	**STOP**	**IDLE**	**30h**
88h	TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00h
89h	TMOD	−−−−−−−−−−−−−−−Timer 1−−−−−−−−−−−−−−−				−−−−−−−−−−−−−−−Timer 0−−−−−−−−−−−−−−−				00h
		GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	
8Ah	TL0									00h
8Bh	TL1									00h
8Ch	TH0									00h
8Dh	TH1									00h
8Eh	**CKCON**	**0**	**0**	**T2M**	**T1M**	**T0M**	**MD2**	**MD1**	**MD0**	**01h**
8Fh	**MWS**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**MXWS**	**00h**
90h	P1	P1.7 $\overline{INT5}$/SCK/SCL	P1.6 $\overline{INT4}$/MISO/SDA	P1.5 $\overline{INT3}$/MOSI	P1.4 $\overline{INT2}$/$\overline{SS}$	P1.3 TXD1	P1.2 RXD1	P1.1 T2EX	P1.0 T2	FFh
91h	EXIF	IE5	IE4	IE3	IE2	1	0	0	0	08h
92h	**MPAGE**									**08h**
93h$_V$	**CADDR**									**00h**
94h	**CDATA**									**00h**
95h	**MCON**	**BPSEL**	**0**	**0**					**RAMMAP**	**00h**
96h										**00h**
97h										
98h	SCON0	SM0_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	00h
99h	SBUF0									00h
9Ah	**SPICON I2CCON(1)**	**SCK2 START**	**SCK1 STOP**	**SCK0 ACK**	**FIFO 0**	**ORDER FAST**	**MSTR MSTR**	**CPHA SCLA**	**CPOL FILEN**	**00h**
9Bh	**SPIDATA I2CDATA(1)**									**00h**
9Ch	**SPIRCON I2CGM(1)**	**RXCNT7 RXFLUSH GCMEN**	**RXCNT6**	**RXCNT5**	**RXCNT4**	**RXCNT3**	**RXCNT2 RXIRQ2**	**RXCNT1 RXIRQ1**	**RXCNT0 RXIRQ0**	**00h**
9Dh	**SPITCON I2CSTAT(1)**	**TXCNT7 TXFLUSH STAT7 SCKD7/SAE**	**TXCNT6 STAT5 SCKD6/SA6**	**TXCNT5 CLK_EN STAT5 SCKD5/SA5**	**TXCNT4 DRV_DLY STAT4 SCKD4/SA4**	**TXCNT3 DRV_EN STAT3 SCKD3/SA3**	**TXCNT2 TXIRQ2 0 SCKD2/SA2**	**TXCNT1 TXIRQ1 0 SCKD1/SA1**	**TXCNT0 TXIRQ0 0 SCKD0/SA0**	**00h**
9Eh	**SPISTART I2CSTART(1)**	**1**								**80h**
9Fh	**SPIEND**	**1**								**80h**
A0h	P2	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	FFh
A1h	**PWMCON**			**PPOL**	**PWMSEL**	**SPDSEL**	**TPCNTL2**	**TPCNTL1**	**TPCNTL0**	**00h**
A2h	**PWMLOW TONELOW**	**PWM7 TDIV7**	**PWM6 TDIV6**	**PWM5 TDIV5**	**PWM4 TDIV4**	**PWM3 TDIV3**	**PWM2 TDIV2**	**PWM1 TDIV1**	**PWM0 TDIV0**	**00h**
A3h	**PWMHI TONEHI**	**PWM15 TDIV15**	**PWM14 TDIV14**	**PWM13 TDIV13**	**PWM12 TDIV12**	**PWM11 TDIV11**	**PWM10 TDIV10**	**PWM9 TDIV9**	**PWM8 TDIV8**	**00h**
A4h	**AIPOL**	**ESEC**	**ESUM**	**EADC**	**EMSEC**	**ESPIT**	**ESPIR/EI2C**	**EALV**	**EDLVB RDSEL**	**00h**

(1) I^{2}C is only available on the MSC1211 and MSC1213.
(2) Applies to MSC1211 and MSC1213 only. See HWPC0 for MSC1212 and MSC1214.
(3) Applies to the MSC1211 and MSC1212. See HWPC1 for MSC1213 and MSC1214.

Table 9. Special Function Registers (continued)

NOTE: (**Boldface** are in addition to standard 8051 registers, and unique to the MSC1211/12/13/14).

ADDRESS	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	RESET VALUE
A5h	**PAI**	**0**	**0**	**0**	**0**	**PAI3**	**PAI2**	**PAI1**	**PAI0**	**00h**
A6h	**AIE**	**ESEC**	**ESUM**	**EADC**	**EMSEC**	**ESPIT**	**ESPIR/EI2C**	**EALV**	**EDLVB**	**00h**
A7h	**AISTAT**	**SEC**	**SUM**	**ADC**	**MSEC**	**SPIT**	**SPIR/I2CSI**	**ALVD**	**DLVD**	**00h**
A8h	IE	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0	00h
A9h	**BPCON**	**BP**	**0**	**0**	**0**	**0**	**0**	**PMSEL**	**EBP**	**00h**
AAh	**BPL**									
ABh	**BPH**									
ACh	**P0DDRL**	**P03H**	**P03L**	**P02H**	**P02L**	**P01H**	**P01L**	**P00H**	**P00L**	**00h**
ADh	**P0DDRH**	**P07H**	**P07L**	**P06H**	**P06L**	**P05H**	**P05L**	**P04H**	**P04L**	**00h**
AEh	**P1DDRL**	**P13H**	**P13L**	**P12H**	**P12L**	**P11H**	**P11L**	**P10H**	**P10L**	**00h**
AFh	**P1DDRH**	**P17H**	**P17L**	**P16H**	**P16L**	**P15H**	**P15L**	**P14H**	**P14L**	**00h**
B0h	P3	P3.7 RD	P3.6 WR	P3.5 T1	P3.4 T0	P3.3 INT1	P3.2 INT0	P3.1 TXD0	P3.0 RXD0	FFh
B1h	**P2DDRL**	**P23H**	**P23L**	**P22H**	**P22L**	**P21H**	**P21L**	**P20H**	**P20L**	**00h**
B2h	**P2DDRH**	**P27H**	**P27L**	**P26H**	**P26L**	**P25H**	**P25L**	**P24H**	**P24L**	**00h**
B3h	**P3DDRL**	**P33H**	**P33L**	**P32H**	**P32L**	**P31H**	**P31L**	**P30H**	**P30L**	**00h**
B4h	**P3DDRH**	**P37H**	**P33L**	**P32H**	**P32L**	**P31H**	**P31L**	**P30H**	**P30L**	**00h**
B5h	**DACL**									
B6h	**DACH**									
B7h	**DACSEL**	**DSEL7**	**DSEL6**	**DSEL5**	**DSEL4**	**DSEL3**	**DSEL2**	**DSEL1**	**DSEL0**	**00h**
B8h	IP	1	PS1	PT2	PS0	PT1	PX1	PT0	PX0	80h
B9h										
BAh										
BBh										
BCh										
BDh										
BEh										
BFh										
C0h	SCON1	SM0_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1	00h
C1h	SBUF1									00h
C2h										
C3h										
C4h										
C5h										
C6h	**EWU**						**EWUWDT**	**EWUEX1**	**EWUEX0**	**00h**
C7h	**SYSCLK**	**0**	**0**	**DIVMOD1**	**DIVMOD0**	**0**	**DIV2**	**DIV1**	**DIV0**	**00h**
C8h	T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$	00h
C9h										
CAh	RCAP2L									00h
CBh	RCAP2H									00h
CCh	TL2									00h
CDh	TH2									00h
CEh										
CFh										
D0h	PSW	CY	AC	F0	RS1	RS0	OV	F1	P	00h
D1h	**OCL**								**LSB**	**00h**

(1) I^2C is only available on the MSC1211 and MSC1213.
(2) Applies to MSC1211 and MSC1213 only. See HWPC0 for MSC1212 and MSC1214.
(3) Applies to the MSC1211 and MSC1212. See HWPC1 for MSC1213 and MSC1214.

Table 9. Special Function Registers (continued)

NOTE: (**Boldface** are in addition to standard 8051 registers, and unique to the MSC1211/12/13/14).

ADDRESS	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	RESET VALUE
D2h	**OCM**									**00h**
D3h	**OCH**	**MSB**								**00h**
D4h	**GCL**								**LSB**	**54h**
D5h	**GCM**									**ECh**
D6h	**GCH**	**MSB**								**5Fh**
D7h	**ADMUX**	**INP3**	**INP2**	**INP1**	**INP0**	**INN3**	**INN2**	**INN1**	**INN0**	**01h**
D8h	EICON	SMOD1	1	EAI	AI	WDTI	0	0	0	40h
D9h	**ADRESL**								**LSB**	**00h**
DAh	**ADRESM**									**00h**
DBh	**ADRESH**	**MSB**								**00h**
DCh	**ADCON0**	**REFCLK**	**BOD**	**EVREF**	**VREFH**	**EBUF**	**PGA2**	**PGA1**	**PGA0**	**30h**
DDh	**ADCON1**	**OF_UF**	**POL**	**SM1**	**SM0**	**—**	**CAL2**	**CAL1**	**CAL0**	**0000_0000b**
DEh	**ADCON2**	**DR7**	**DR6**	**DR5**	**DR4**	**DR3**	**DR2**	**DR1**	**DR0**	**1Bh**
DFh	**ADCON3**	**0**	**0**	**0**	**0**	**0**	**DR10**	**DR9**	**DR8**	**06h**
E0h	ACC									00h
E1h	**SSCON**	**SSCON1**	**SSCON0**	**SCNT2**	**SCNT1**	**SCNT0**	**SHF2**	**SHF1**	**SHF0**	**00h**
E2h	**SUMR0**									**00h**
E3h	**SUMR1**									**00h**
E4h	**SUMR2**									**00h**
E5h	**SUMR3**									**00h**
E6h	**ODAC**									**00h**
E7h	**LVDCON**	**ALVDIS**	**ALVD2**	**ALVD1**	**ALVD0**	**DLVDIS**	**DLVD2**	**DLVD1**	**DLVD0**	**00h**
E8h	EIE	1	1	1	EWDI	EX5	EX4	EX3	EX2	E0h
E9h	**HWPC0**	**0**	**0**	**0**	**0**	**0**	**1**	**MEMORY SIZE**		**0000_01xxb(2)**
EAh	**HWPC1**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**08h(3)**
EBh	**HWVER**									
ECh	**Reserved**									**00h**
EDh	**Reserved**									**00h**
EEh	**FMCON**	**0**	**PGERA**	**0**	**FRCM**	**0**	**BUSY**	**SPM**	**FPM**	**02h**
EFh	**FTCON**	**FER3**	**FER2**	**FER1**	**FER0**	**FWR3**	**FWR2**	**FWR1**	**FWR0**	**A5h**
F0h	B	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0	00h
F1h	**PDCON**	**0**	**PDDAC**	**PDI2C**	**PDPWM**	**PDADC**	**PDWDT**	**PDST**	**PDSPI**	**7Fh**
F2h	**PASEL**	**0**	**0**	**PSEN2**	**PSEN1**	**PSEN0**	**0**	**ALE1**	**ALE0**	**00h**
F3h										
F4h										
F5h										
F6h	**ACLK**	**0**	**FREQ6**	**FREQ5**	**FREQ4**	**FREQ3**	**FREQ2**	**FREQ1**	**FREQ0**	**03h**
F7h	**SRST**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**RSTREQ**	**00h**
F8h	EIP	1	1	1	PWDI	PX5	PX4	PX3	PX2	E0h
F9h	**SECINT**	**WRT**	**SECINT6**	**SECINT5**	**SECINT4**	**SECINT3**	**SECINT2**	**SECINT1**	**SECINT0**	**7Fh**
FAh	**MSINT**	**WRT**	**MSINT6**	**MSINT5**	**MSINT4**	**MSINT3**	**MSINT2**	**MSINT1**	**MSINT0**	**7Fh**
FBh	**USEC**	**0**	**0**	**FREQ5**	**FREQ4**	**FREQ3**	**FREQ2**	**FREQ1**	**FREQ0**	**03h**
FCh	**MSECL**									**9Fh**
FDh	**MSECH**									**0Fh**
FEh	**HMSEC**									**63h**
FFh	**WDTCON**	**EWDT**	**DWDT**	**RWDT**	**WDCNT4**	**WDCNT3**	**WDCNT2**	**WDCNT1**	**WDCNT0**	**00h**

(1) I^2C is only available on the MSC1211 and MSC1213.
(2) Applies to MSC1211 and MSC1213 only. See HWPC0 for MSC1212 and MSC1214.
(3) Applies to the MSC1211 and MSC1212. See HWPC1 for MSC1213 and MSC1214.

Table 10. Special Function Register Cross Reference

SFR	ADDRESS	FUNCTIONS	CPU	INTERRUPTS	PORTS	SERIAL COMM.	POWER AND CLOCKS	TIMER COUNTERS	PWM	FLASH MEMORY	ADC	DAC
P0	80h	Port 0			X							
SP	81h	Stack Pointer	X									
DPL0	82h	Data Pointer Low 0	X									
DPH0	83h	Data Pointer High 0	X									
DPL1	84h	Data Pointer Low 1	X									
DPH1	85h	Data Pointer High 1	X									
DPS	86h	Data Pointer Select	X									
PCON	87h	Power Control					X					
TCON	88h	Timer/Counter Control				X		X				
TMOD	89h	Timer Mode Control				X		X				
TL0	8Ah	Timer0 LSB						X				
TL1	8Bh	Timer1 LSB						X				
TH0	8Ch	Timer0 MSB						X				
TH1	8Dh	Timer1 MSB						X				
CKCON	8Eh	Clock Control				X	X	X				
MWS	8Fh	Memory Write Select								X		
P1	90h	Port 1			X							
EXIF	91h	External Interrupt Flag		X								
MPAGE	92h	Memory Page	X									
CADDR	93h	Configuration Address								X		
CDATA	94h	Configuration Data								X		
MCON	95h	Memory Control	X									
SCON0	98h	Serial Port 0 Control				X		X				
SBUF0	99h	Serial Data Buffer 0				X						
SPICON	9Ah	SPI Control				X						
I2CCON		I^2C Control				X						
SPIDATA	9Bh	SPI Data				X						
I2CDATA		I^2C Data				X						
SPIRCON	9Ch	SPI Receive Control				X						
I2CGM		I^2C Gen Call/Mult Master Enable				X						
SPITCON	9Dh	SPI Transmit Control				X						
I2CSTAT		I^2C Status				X						
SPISTART	9Eh	SPI Buffer Start Address				X						
I2CSTART		I^2C Start				X						
SPIEND	9Fh	SPI Buffer End Address				X						
P2	A0h	Port 2			X							
PWMCON	A1h	PWM Control					X		X			
PWMLOW	A2h	PWM Low Byte							X			
TONELOW		Tone Low Byte							X			
PWMHI	A3h	PWM HIgh Byte							X			
TONEHI		Tone Low Byte							X			
AIPOL	A4h	Auxiliary Interrupt Poll		X	X	X	X	X			X	
PAI	A5h	Pending Auxiliary Interrupt		X	X	X	X	X			X	
AIE	A6h	Auxiliary Interrupt Enable		X	X	X	X	X			X	
AISTAT	A7h	Auxiliary Interrupt Status		X	X	X	X	X			X	
IE	A8h	Interrupt Enable		X								

Table 10. Special Function Register Cross Reference (continued)

SFR	ADDRESS	FUNCTIONS	CPU	INTERRUPTS	PORTS	SERIAL COMM.	POWER AND CLOCKS	TIMER COUNTERS	PWM	FLASH MEMORY	ADC	DAC
BPCON	A9h	Breakpoint Control	X						X			
BPL	AAh	Breakpoint Low Address	X						X			
BPH	ABh	Breakpoint High Address	X						X			
P0DDRL	ACh	Port 0 Data Direction Low			X							
P0DDRH	ADh	Port 0 Data Direction High			X							
P1DDRL	AEh	Port 1 Data Direction Low			X							
P1DDRH	AFh	Port 1 Data Direction High			X							
P3	B0h	Port 3			X							
P2DDRL	B1h	Port 2 Data Direction Low			X							
P2DDRH	B2h	Port 2 Data Direction High			X							
P3DDRL	B3h	Port 3 Data Direction Low			X							
P3DDRH	B4h	Port 3 Data Direction High			X							
DACL	B5h	DAC Low Byte										X
DACH	B6h	DAC High Byte										X
DACSEL	B7h	DAC Select										X
DACCON	B7h	DAC Control										X
IP	B8h	Interrupt Priority		X								
SCON1	C0h	Serial Port 1 Control				X		X				
SBUF1	C1h	Serial Data Buffer 1				X						
EWU	C6h	Enable Wake Up		X			X					
SYSCLK	C7h	System Clock Divider				X	X	X	X	X	X	
T2CON	C8h	Timer 2 Control		X				X				
RCAP2L	CAh	Timer 2 Capture LSB		X				X				
RCAP2H	CBh	Timer 2 Capture MSB		X				X				
TL2	CCh	Timer 2 LSB						X				
TH2	CDh	Timer 2 MSB						X				
PSW	D0h	Program Status Word	X									
OCL	D1h	ADC Offset Calibration Low Byte									X	
OCM	D2h	ADC Offset Calibration Mid Byte									X	
OCH	D3h	ADC Offset Calibration High Byte									X	
GCL	D4h	ADC Gain Calibration Low Byte									X	
GCM	D5h	ADC Gain Calibration Mid Byte									X	
GCH	D6h	ADC Gain Calibration High Byte									X	
ADMUX	D7h	ADC Input Multiplexer									X	
EICON	D8h	Enable Interrupt Control		X		X	X				X	
ADRESL	D9h	ADC Results Low Byte									X	
ADRESM	DAh	ADC Results Middle Byte									X	
ADRESH	DBh	ADC Results High Byte									X	
ADCON0	DCh	ADC Control 0									X	
ADCON1	DDh	ADC Control 1									X	
ADCON2	DEh	ADC Control 2									X	
ADCON3	DFh	ADC Control 3									X	
ACC	E0h	Accumulator	X									
SSCON	E1h	Summation/Shifter Control	X								X	
SUMR0	E2h	Summation 0	X								X	
SUMR1	E3h	Summation 1	X								X	
SUMR2	E4h	Summation 2	X								X	
SUMR3	E5h	Summation 3	X								X	

Table 10. Special Function Register Cross Reference (continued)

SFR	ADDRESS	FUNCTIONS	CPU	INTERRUPTS	PORTS	SERIAL COMM.	POWER AND CLOCKS	TIMER COUNTERS	PWM	FLASH MEMORY	ADC	DAC
ODAC	E6h	Offset DAC									X	
LVDCON	E7h	Low Voltage Detect Control					X					
EIE	E8h	Extended Interrupt Enable		X								
HWPC0	E9h	Hardware Product Code 0	X									
HWPC1	EAh	Hardware Product Code 1	X									
HWVER	EBh	Hardware Version	X									
FMCON	EEh	Flash Memory Control								X		
FTCON	EFh	Flash Memory Timing Control								X		
B	F0h	Second Accumulator	X									
PDCON	F1h	Power Down Control				X	X	X			X	X
PASEL	F2h	$\overline{\text{PSEN}}$/ALE Select			X		X					
ACLK	F6h	Analog Clock					X				X	
SRST	F7h	System Reset	X				X					
EIP	F8h	Extended Interrupt Priority		X								
SECINT	F9h	Seconds Timer Interrupt		X			X					
MSINT	FAh	Milliseconds Timer Interrupt		X			X					
USEC	FBh	One Microsecond TImer					X		X	X		
MSECL	FCh	One Millisecond TImer Low Byte					X			X		
MSECH	FDh	One Millisecond Timer High Byte					X			X		
HMSEC	FEh	One Hundred Millisecond TImer					X					
WDTCON	FFh	Watchdog Timer	X				X					
HCR0	3Fh	Hardware Configuration Reg. 0								X		
HCR1	3Eh	Hardware Configuration Reg. 1					X					

Port 0 (P0)

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Reset Value
SFR 80h	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	FFh

P0.7−0 bits 7−0 **Port 0.** This port functions as a multiplexed address/data bus during external memory access, and as a general-purpose I/O port when external memory access is not needed. During external memory cycles, this port will contain the LSB of the address when ALE is high, and Data when ALE is low. When used as a general-purpose I/O, this port drive is selected by P0DDRL and P0DDRH (ACh, ADh). Whether Port 0 is used as general-purpose I/O or for external memory access is determined by the Flash Configuration Register (HCR1.1) (See SFR CADDR 93h).

Stack Pointer (SP)

	7	6	5	4	3	2	1	0	Reset Value
SFR 81h	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0	07h

SP.7−0 bits 7−0 **Stack Pointer.** The stack pointer identifies the location where the stack will begin. The stack pointer is incremented before every PUSH or CALL operation and decremented after each POP or RET/RETI. This register defaults to 07h after reset.

Data Pointer Low 0 (DPL0)

	7	6	5	4	3	2	1	0	Reset Value
SFR 82h	DPL0.7	DPL0.6	DPL0.5	DPL0.4	DPL0.3	DPL0.2	DPL0.1	DPL0.0	00h

DPL0.7−0 bits 7−0 Data Pointer Low 0. This register is the low byte of the standard 8051 16-bit data pointer. DPL0 and DPH0 are used to point to non-scratchpad data RAM. The current data pointer is selected by DPS (SFR 86h).

Data Pointer High 0 (DPH0)

	7	6	5	4	3	2	1	0	Reset Value
SFR 83h	DPH0.7	DPH0.6	DPH0.5	DPH0.4	DPH0.3	DPH0.2	DPH0.1	DPH0.0	00h

DPH0.7−0 bits 7−0 **Data Pointer High 0.** This register is the high byte of the standard 8051 16-bit data pointer. DPL0 and DPH0 are used to point to non-scratchpad data RAM. The current data pointer is selected by DPS (SFR 86h).

Data Pointer Low 1 (DPL1)

	7	6	5	4	3	2	1	0	Reset Value
SFR 84h	DPL1.7	DPL1.6	DPL1.5	DPL1.4	DPL1.3	DPL1.2	DPL1.1	DPL1.0	00h

DPL1.7−0 bits 7−0 Data Pointer Low 1. This register is the low byte of the auxiliary 16-bit data pointer. When the SEL bit (DPS.0) (SFR 86h) is set, DPL1 and DPH1 are used in place of DPL0 and DPH0 during DPTR operations.

Data Pointer High 1 (DPH1)

	7	6	5	4	3	2	1	0	Reset Value
SFR 85h	DPH1.7	DPH1.6	DPH1.5	DPH1.4	DPH1.3	DPH1.2	DPH1.1	DPH1.0	00h

DPH1.7−0 bits 7−0 **Data Pointer High.** This register is the high byte of the auxiliary 16-bit data pointer. When the SEL bit (DPS.0) (SFR 86h) is set, DPL1 and DPH1 are used in place of DPL0 and DPH0 during DPTR operations.

Data Pointer Select (DPS)

	7	6	5	4	3	2	1	0	Reset Value
SFR 86h	0	0	0	0	0	0	0	SEL	00h

SEL bit 0 — **Data Pointer Select.** This bit selects the active data pointer.
0: Instructions that use the DPTR will use DPL0 and DPH0.
1: Instructions that use the DPTR will use DPL1 and DPH1.

Power Control (PCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR 87h	SMOD	0	1	1	GF1	GF0	STOP	IDLE	30h

SMOD bit 7 — **Serial Port 0 Baud Rate Doubler Enable.** The serial baud rate doubling function for Serial Port 0.
0: Serial Port 0 baud rate will be a standard baud rate.
1: Serial Port 0 baud rate will be double that defined by baud rate generation equation.

GF1 bit 3 — **General-Purpose User Flag 1.** This is a general-purpose flag for software control.

GF0 bit 2 — **General-Purpose User Flag 0.** This is a general-purpose flag for software control.

STOP bit 1 — **Stop Mode Select.** Setting this bit halts the oscillator and blocks external clocks. This bit always reads as a 0. All digital pins and DACs keep their respective output values. Internal REF dies. Exit with RESET.

IDLE bit 0 — **Idle Mode Select.** Setting this bit freezes the CPU, Timer 0, 1, and 2, and the USARTs; other peripherals remain active. This bit will always be read as a 0. All digital pins and DACs keep their respective output values. Internal REF remains unchanged. Exit with AI (A6h) and EWU (C6h) interrupts.

Timer/Counter Control (TCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR 88h	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00h

TF1 bit 7 — **Timer 1 Overflow Flag.** This bit indicates when Timer 1 overflows its maximum count as defined by the current mode. This bit can be cleared by software and is automatically cleared when the CPU vectors to the Timer 1 interrupt service routine.

0: No Timer 1 overflow has been detected.

1: Timer 1 has overflowed its maximum count.

TR1 bit 6 — **Timer 1 Run Control.** This bit enables/disables the operation of Timer 1. Halting this timer preserves the current count in TH1, TL1.

0: Timer is halted.

1: Timer is enabled.

TF0 bit 5 — **Timer 0 Overflow Flag.** This bit indicates when Timer 0 overflows its maximum count as defined by the current mode. This bit can be cleared by software and is automatically cleared when the CPU vectors to the Timer 0 interrupt service routine.

0: No Timer 0 overflow has been detected.

1: Timer 0 has overflowed its maximum count.

TR0 bit 4 — **Timer 0 Run Control.** This bit enables/disables the operation of Timer 0. Halting this timer preserves the current count in TH0, TL0.

0: Timer is halted.

1: Timer is enabled.

IE1 bit 3 — **Interrupt 1 Edge Detect.** This bit is set when an edge/level of the type defined by IT1 is detected. If IT1 = 1, this bit will remain set until cleared in software or the start of the External Interrupt 1 service routine. If IT1 = 0, this bit will inversely reflect the state of the $\overline{\text{INT1}}$ pin.

IT1 bit 2 — **Interrupt 1 Type Select.** This bit selects whether the $\overline{\text{INT1}}$ pin will detect edge or level triggered interrupts.

0: $\overline{\text{INT1}}$ is level-triggered.

1: $\overline{\text{INT1}}$ is edge-triggered.

IE0 bit 1 — **Interrupt 0 Edge Detect.** This bit is set when an edge/level of the type defined by IT0 is detected. If IT0 = 1, this bit will remain set until cleared in software or the start of the External Interrupt 0 service routine. If IT0 = 0, this bit will inversely reflect the state of the $\overline{\text{INT0}}$ pin.

IT0 bit 0 — **Interrupt 0 Type Select.** This bit selects whether the $\overline{\text{INT0}}$ pin will detect edge or level triggered interrupts.

0: $\overline{\text{INT0}}$ is level-triggered.

1: $\overline{\text{INT0}}$ is edge-triggered.

Timer Mode Control (TMOD)

	7	6	5	4	3	2	1	0	Reset Value
SFR 89h	TIMER 1				TIMER 0				00h
	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	

GATE bit 7 — **Timer 1 Gate Control.** This bit enables/disables the ability of Timer 1 to increment.
0: Timer 1 will clock when TR1 = 1, regardless of the state of pin $\overline{INT1}$.
1: Timer 1 will clock only when TR1 = 1 and pin $\overline{INT1}$ = 1.

C/$\overline{T}$ bit 6 — **Timer 1 Counter/Timer Select.**
0: Timer is incremented by internal clocks.
1: Timer is incremented by pulses on T1 pin when TR1 (TCON.6, SFR 88h) is 1.

M1, M0 bits 5−4 — **Timer 1 Mode Select.** These bits select the operating mode of Timer 1.

M1	M0	MODE
0	0	Mode 0: 8-bit counter with 5-bit prescale.
0	1	Mode 1: 16 bits.
1	0	Mode 2: 8-bit counter with auto reload.
1	1	Mode 3: Timer 1 is halted, but holds its count.

GATE bit 3 — **Timer 0 Gate Control.** This bit enables/disables the ability of Timer 0 to increment.
0: Timer 0 will clock when TR0 = 1, regardless of the state of pin $\overline{INT0}$ (software control).
1: Timer 0 will clock only when TR0 = 1 and pin $\overline{INT0}$ = 1 (hardware control).

C/$\overline{T}$ bit 2 — **Timer 0 Counter/Timer Select.**
0: Timer is incremented by internal clocks.
1: Timer is incremented by pulses on pin T0 when TR0 (TCON.4, SFR 88h) is 1.

M1, M0 bits 1−0 — **Timer 0 Mode Select.** These bits select the operating mode of Timer 0.

M1	M0	MODE
0	0	Mode 0: 8-bit counter with 5-bit prescale.
0	1	Mode 1: 16 bits.
1	0	Mode 2: 8-bit counter with auto reload.
1	1	Mode 3: Two 8-bit counters.

Timer 0 LSB (TL0)

	7	6	5	4	3	2	1	0	Reset Value
SFR 8Ah	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0	00h

TL0.7−0 bits 7−0 — **Timer 0 LSB.** This register contains the least significant byte of Timer 0.

Timer 1 LSB (TL1)

	7	6	5	4	3	2	1	0	Reset Value
SFR 8Bh	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0	00h

TL1.7−0 bits 7−0 — **Timer 1 LSB.** This register contains the least significant byte of Timer 1.

Timer 0 MSB (TH0)

	7	6	5	4	3	2	1	0	Reset Value
SFR 8Ch	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0	00h

TH0.7−0 **Timer 0 MSB.** This register contains the most significant byte of Timer 0.
bits 7−0

Timer 1 MSB (TH1)

	7	6	5	4	3	2	1	0	Reset Value
SFR 8Dh	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0	00h

TH1.7−0 **Timer 1 MSB.** This register contains the most significant byte of Timer 1.
bits 7−0

Clock Control (CKCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR 8Eh	0	0	T2M	T1M	T0M	MD2	MD1	MD0	01h

T2M
bit 5 **Timer 2 Clock Select.** This bit controls the division of the system clock that drives Timer 2. This bit has no effect when the timer is in baud rate generator or clock output modes. Clearing this bit to 0 maintains 8051 compatibility. This bit has no effect on instruction cycle timing.

0: Timer 2 uses a divide by 12 of the crystal frequency.

1: Timer 2 uses a divide by 4 of the crystal frequency.

T1M
bit 4 **Timer 1 Clock Select.** This bit controls the division of the system clock that drives Timer 1. Clearing this bit to 0 maintains 8051 compatibility. This bit has no effect on instruction cycle timing.

0: Timer 1 uses a divide by 12 of the crystal frequency.

1: Timer 1 uses a divide by 4 of the crystal frequency.

T0M
bit 3 **Timer 0 Clock Select.** This bit controls the division of the system clock that drives Timer 0. Clearing this bit to 0 maintains 8051 compatibility. This bit has no effect on instruction cycle timing.

0: Timer 0 uses a divide by 12 of the crystal frequency.

1: Timer 0 uses a divide by 4 of the crystal frequency.

MD2, MD1, MD0
bits 2−0 **Stretch MOVX Select 2−0.** These bits select the time by which external MOVX cycles are to be stretched. This allows slower memory or peripherals to be accessed without using ports or manual software intervention. The width of the $\overline{RD}$ or $\overline{WR}$ strobe will be stretched by the specified interval, which will be transparent to the software except for the increased time to execute the MOVX instruction. All internal MOVX instructions on devices containing MOVX SRAM are performed at the 2 instruction cycle rate.

MD2	MD1	MD0	STRETCH VALUE	MOVX DURATION	$\overline{RD}$ or $\overline{WR}$ STROBE WIDTH (SYS CLKs)	$\overline{RD}$ or $\overline{WR}$ STROBE WIDTH (μs) at 12MHz
0	0	0	0	2 Instruction Cycles	2	0.167
0	0	1	1	3 Instruction Cycles (default)	4	0.333
0	1	0	2	4 Instruction Cycles	8	0.667
0	1	1	3	5 Instruction Cycles	12	1.000
1	0	0	4	6 Instruction Cycles	16	1.333
1	0	1	5	7 Instruction Cycles	20	1.667
1	1	0	6	8 Instruction Cycles	24	2.000
1	1	1	7	9 Instruction Cycles	28	2.333

Memory Write Select (MWS)

	7	6	5	4	3	2	1	0	Reset Value
SFR 8Fh	0	0	0	0	0	0	0	MXWS	00h

MXWS **MOVX Write Select.** This allows writing to the internal Flash Program Memory.
bit 0 0: MOVX operations will access Data Memory (default).
1: MOVX operations will access Program Memory. Write operations can be inhibited by the PML or RSL bits in HCR0.

Port 1 (P1)

	7	6	5	4	3	2	1	0	Reset Value
SFR 90h	P1.7 $\overline{\text{INT5}}$/SCK/SCL	P1.6 INT4/MISO/SDA	P1.5 $\overline{\text{INT3}}$/MOSI	P1.4 INT2/$\overline{\text{SS}}$	P1.3 TXD1	P1.2 RXD1	P1.1 T2EX	P1.0 T2	FFh

P1.7−0 **General-Purpose I/O Port 1.** This register functions as a general-purpose I/O port. In addition, all the pins have an
bits 7−0 alternative function listed below. Each of the functions is controlled by several other SFRs. The associated Port 1 latch bit must contain a logic ‘1’ before the pin can be used in its alternate function capacity. To use the alternate function, set the appropriate mode in P1DDRL (SFR AEh), P1DDRH (SFR AFh).

$\overline{\text{INT5}}$/SCK/SCL **External Interrupt 5.** A falling edge on this pin will cause an external interrupt 5 if enabled.
bit 7 **SPI Clock.** The master clock for SPI data transfers.
Serial Clock. The serial clock for I^2C data transfers (MSC1211 and MSC1213 only).

INT4/MISO/SDA **External Interrupt 4.** A rising edge on this pin will cause an external interrupt 4 if enabled.
bit 6 **Master In Slave Out.** For SPI data transfers, this pin receives data for the master and transmits data from the slave.
SDA. For I^2C data transfers, this pin is the data line (MSC1211 and MSC1213 only).

$\overline{\text{NT3}}$/MOSI **External Interrupt 3.** A falling edge on this pin will cause an external interrupt 3 if enabled.
bit 5 **Master Out Slave In.** For SPI data transfers, this pin transmits master data and receives slave data.

INT2/$\overline{\text{SS}}$ **External Interrupt 2.** A rising edge on this pin will cause an external interrupt 2 if enabled**.**
bit 4 **Slave Select.** During SPI operation, this pin provides the select signal for the slave device.

TXD1 **Serial Port 1 Transmit.** This pin transmits the serial Port 1 data in serial port modes 1, 2, 3, and emits the
bit 3 synchronizing clock in serial port mode 0.

RXD1 **Serial Port 1 Receive.** This pin receives the serial Port 1 data in serial port modes 1, 2, 3, and is a bidirectional data
bit 2 transfer pin in serial port mode 0.

T2EX **Timer 2 Capture/Reload Trigger.** A 1 to 0 transition on this pin will cause the value in the T2 registers to be
bit 1 transferred into the capture registers if enabled by EXEN2 (T2CON.3, SFR C8h). When in auto-reload mode, a 1 to 0 transition on this pin will reload the Timer 2 registers with the value in RCAP2L and RCAP2H if enabled by EXEN2 (T2CON.3, SFR C8h).

T2 **Timer 2 External Input.** A 1 to 0 transition on this pin will cause Timer 2 to increment or decrement depending on
bit 0 the timer configuration.

External Interrupt Flag (EXIF)

	7	6	5	4	3	2	1	0	Reset Value
SFR 91h	IE5	IE4	IE3	IE2	1	0	0	0	08h

IE5 bit 7 — **External Interrupt 5 Flag.** This bit will be set when a falling edge is detected on $\overline{\text{INT5}}$. This bit must be cleared manually by software. Setting this bit in software will cause an interrupt if enabled.

IE4 bit 6 — **External Interrupt 4 Flag.** This bit will be set when a rising edge is detected on INT4. This bit must be cleared manually by software. Setting this bit in software will cause an interrupt if enabled.

IE3 bit 5 — **External Interrupt 3 Flag.** This bit will be set when a falling edge is detected on $\overline{\text{INT3}}$. This bit must be cleared manually by software. Setting this bit in software will cause an interrupt if enabled.

IE2 bit 4 — **External Interrupt 2 Flag.** This bit will be set when a rising edge is detected on INT2. This bit must be cleared manually by software. Setting this bit in software will cause an interrupt if enabled.

Memory Page (MPAGE)

	7	6	5	4	3	2	1	0	Reset Value
SFR 92h									00h

MPAGE bits 7−0 — The 8051 uses Port 2 for the upper 8 bits of the external Data Memory access by `MOVX A@Ri` and `MOVX @Ri, A` instructions. The MSC1211/12/13/14 uses register MPAGE instead of Port 2. To access external Data Memory using the `MOVX A@Ri` and `MOVX @Ri, A` instructions, the user should preload the upper byte of the address into MPAGE (versus preloading into P2 for the standard 8051).

Configuration Address (CADDR) (write-only)

	7	6	5	4	3	2	1	0	Reset Value
SFR 93h									00h

CADDR bits 7−0 — **Configuration Address.** This register supplies the address for reading bytes in the 128 bytes of Flash Configuration Memory. It is recommended that **faddr_data_read** be used when accessing Configuration Memory.

CAUTION:If this register is written to while executing from Flash Memory, the CDATA register will be incorrect.

Configuration Data (CDATA)

	7	6	5	4	3	2	1	0	Reset Value
SFR 94h									00h

CDATA bits 7−0 — **Configuration Data.** This register will contain the data in the 128 bytes of Flash Configuration Memory that is located at the last written address in the CADDR register. This is a read-only register.

Memory Control (MCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR 95h	**BPSEL**	**0**	**0**	—	—	—	—	**RAMMAP**	00h

BPSEL bit 7 — **Breakpoint Address Selection**

Write: Select one of two Breakpoint registers: 0 or 1.
- 0: Select breakpoint register 0.
- 1: Select breakpoint register 1.

Read: Provides the Breakpoint register that created the last interrupt: 0 or 1.

RAMMAP bit 0 — **Memory Map 1kB extended SRAM.**

0: Address is: 0000h—03FFh (default) (Data Memory)

1: Address is 8400h—87FFh (Data and Program Memory)

Serial Port 0 Control (SCON0)

	7	6	5	4	3	2	1	0	Reset Value
SFR 98h	SM0_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	00h

SM0−2 bits 7−5 **Serial Port 0 Mode.** These bits control the mode of serial Port 0. Modes 1, 2, and 3 have 1 start and 1 stop bit in addition to the 8 or 9 data bits.

MODE	SM0	SM1	SM2	FUNCTION	LENGTH	PERIOD
0	0	0	0	Synchronous	8 bits	12 p_{CLK}(1)
0	0	0	1	Synchronous	8 bits	4 p_{CLK}(1)
1(2)	0	1	0	Asynchronous	10 bits	Timer 1 or 2 Baud Rate Equation
1(2)	0	1	1	Valid Stop Required(3)	10 bits	Timer 1 Baud Rate Equation
2	1	0	0	Asynchronous	11 bits	64 p_{CLK}(1) (SMOD = 0) 32 p_{CLK}(1) (SMOD = 1)
2	1	0	1	Asynchronous with Multiprocessor Communication(4)	11 bits	64 p_{CLK}(1) (SMOD = 0) 32 p_{CLK}(1) (SMOD = 1)
3(2)	1	1	0	Asynchronous	11 bits	Timer 1 or 2 Baud Rate Equation
3(2)	1	1	1	Asynchronous with Multiprocessor Communication(4)	11 bits	Timer 1 or 2 Baud Rate Equation

(1) p_{CLK} will be equal to t_{CLK}, except that p_{CLK} will stop for Idle mode.
(2) For modes 1 and 3, the selection of Timer 1 or 2 for baud rate is specified via the T2CON (C8h) register.
(3) RI_0 will only be activated when a valid STOP is received.
(4) RI_0 will not be activated if bit 9 = 0.

REN_0 bit 4 **Receive Enable.** This bit enables/disables the serial Port 0 received shift register.
0: Serial Port 0 reception disabled.
1: Serial Port 0 received enabled (modes 1, 2, and 3). Initiate synchronous reception (mode 0).

TB8_0 bit 3 **9th Transmission Bit State.** This bit defines the state of the 9th transmission bit in serial Port 0 modes 2 and 3.

RB8_0 bit 2 **9th Received Bit State.** This bit identifies the state of the 9th reception bit of received data in serial Port 0 modes 2 and 3. In serial port mode 1, when SM2_0 = 0, RB8_0 is the state of the stop bit. RB8_0 is not used in mode 0.

TI_0 bit 1 **Transmitter Interrupt Flag.** This bit indicates that data in the serial Port 0 buffer has been completely shifted out. In serial port mode 0, TI_0 is set at the end of the 8th data bit. In all other modes, this bit is set at the end of the last data bit. This bit must be manually cleared by software.

RI_0 bit 0 **Receiver Interrupt Flag.** This bit indicates that a byte of data has been received in the serial Port 0 buffer. In serial port mode 0, RI_0 is set at the end of the 8th bit. In serial port mode 1, RI_0 is set after the last sample of the incoming stop bit subject to the state of SM2_0. In modes 2 and 3, RI_0 is set after the last sample of RB8_0. This bit must be manually cleared by software.

Serial Data Buffer 0 (SBUF0)

	7	6	5	4	3	2	1	0	Reset Value
SFR 99h									00h

SBUF0 bits 7−0 **Serial Data Buffer 0.** Data for Serial Port 0 is read from or written to this location. The serial transmit and receive buffers are separate registers, but both are addressed at this location.

SPI Control (SPICON). Any change resets the SPI interface, counters, and pointers.

	7	6	5	4	3	2	1	0	Reset Value
SFR 9Ah	SCK2	SCK1	SCK0	FIFO	ORDER	MSTR	CPHA	CPOL	00h

SCK bits 7−5 **SCK Selection.** Selection of t_{CLK} divider for generation of SCK in Master mode.

SCK2	SCK1	SCK0	SCK PERIOD
0	0	0	$t_{CLK}/2$
0	0	1	$t_{CLK}/4$
0	1	0	$t_{CLK}/8$
0	1	1	$t_{CLK}/16$
1	0	0	$t_{CLK}/32$
1	0	1	$t_{CLK}/64$
1	1	0	$t_{CLK}/128$
1	1	1	$t_{CLK}/256$

FIFO bit 4 **Enable FIFO in On-Chip Indirect Memory.**
0: Both transmit and receive are double buffers
1: Circular FIFO used for transmit and receive bytes

ORDER bit 3 **Set Bit Order for Transmit and Receive.**
0: Most Significant Bits First
1: Least Significant Bits First

MSTR bit 2 **SPI Master Mode.**
0: Slave Mode
1: Master Mode

CPHA bit 1 **Serial Clock Phase Control.**
0: Valid data starting from half SCK period before the first edge of SCK
1: Valid data starting from the first edge of SCK

CPOL bit 0 **Serial Clock Polarity.**
0: SCK idle at logic low
1: SCK idle at logic high

I²C Control (I2CCON) (Available only on the MSC1211 and MSC1213)

	7	6	5	4	3	2	1	0	Reset Value
SFR 9Ah	START	STOP	ACK	0	FAST	MSTR	SCLS	FILEN	00h

START **Start Condition (Master mode).**
bit 7 Read: Current status of start condition or repeated start condition.
Write: When operating as a master, a start condition is transmitted when the START bit is set to 1. During a data transfer, if the START bit is set, a repeated start is transmitted after the current data transfer is complete. If no transfer is in progress when the START and STOP bits are set simultaneously, a START will be followed by a STOP.

STOP **Stop Condition (Master mode).**
bit 6 Read: Current status of stop condition.
Write: Setting STOP to logic 1 causes a stop condition to be transmitted. When a stop condition is received, hardware clears STOP to logic 0. If both START and STOP are set during a transfer, a stop condition is transmitted followed by a start condition.

ACK **Acknowledge.** Defines the ACK/NACK generation from the master/slave receiver during the acknowledge cycle.
bit 5 0: A NACK (high level on SDA) is returned during the acknowledge cycle.
1: An ACK (low level on SDA) is returned during the acknowledge cycle.
In slave transmit mode, 0 = Current byte is last byte, 1 = More to follow.

0 **Always set this value to zero.**
bit 4

FAST **Fast Mode Enable.**
bit 3 0: Standard Mode (100kHz)
1: Fast Mode (400kHz)

MSTR **SPI Master Mode.**
bit 2 0: Slave Mode
1: Master Mode

SCLS **Clock Stretch.**
bit 1 0: No effect
1: Release the clock line. For the slave mode, the clock is stretched for each data transfer. This bit releases the clock.

FILEN **Filter Enable. 50ns glitch filter.**
bit 0 0: Filter disabled
1: Filter enabled

SPI Data (SPIDATA) / I²C Data (I2CDATA)

	7	6	5	4	3	2	1	0	Reset Value
SFR 9Bh									00h

SPIDATA **SPI Data.** Data for SPI is read from or written to this location. The SPI transmit and receive buffers are
bits 7−0 separate registers, but both are addressed at this location. Read to clear the receive interrupt and write to clear the transmit interrupt.

I2CDATA **I2C Data . (MSC1211 and MSC1213 only.)** Data for I²C is read from or written to this location. The I²C transmit and receive buffers are separate registers, but both are addressed at this location. Writing to this register
bits 7−0 starts transmission. In Master mode, reading this register starts a Master read cycle.

SPI Receive Control (SPIRCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR 9Ch	RXCNT7 RXFLUSH	RXCNT6	RXCNT5	RXCNT4	RXCNT3	RXCNT2 RXIRQ2	RXCNT1 RXIRQ1	RXCNT0 RXIRQ0	00h

RXCNT **Receive Counter.** Read-only bits which read the number of bytes in the receive buffer (0 to 128).
bits 7−0

RXFLUSH **Flush Receive FIFO.** Write-only.
bit 7 0: No Action
1: SPI Receive Buffer Set to Empty

RXIRQ **Read IRQ Level.** Write-only.
bits 2−0

000	Generate IRQ when Receive Count = 1 or more.
001	Generate IRQ when Receive Count = 2 or more.
010	Generate IRQ when Receive Count = 4 or more.
011	Generate IRQ when Receive Count = 8 or more.
100	Generate IRQ when Receive Count = 16 or more.
101	Generate IRQ when Receive Count = 32 or more.
110	Generate IRQ when Receive Count = 64 or more.
111	Generate IRQ when Receive Count = 128 or more.

I^2C GM (I2CGM) (Available only on the MSC1211 and MSC1213)

	7	6	5	4	3	2	1	0	Reset Value
SFR 9Ch	GCMEN								00h

GCMEN **General Call/Multiple Master Enable.** Write-only.
bit 7 Slave mode: 0 = General call ignored, 1 = General call will be detected
Master mode: 0 = Single master, 1 = Multiple master mode

SPI Transmit Control (SPITCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR 9Dh	TXCNT7 TXFLUSH	TXCNT6	TXCNT5 CLK_EN	TXCNT4 DRV_DLY	TXCNT3 DRV_EN	TXCNT2 TXIRQ2	TXCNT1 TXIRQ1	TXCNT0 TXIRQ0	00h

TXCNT **Transmit Counter.** Read-only bits which read the number of bytes in the transmit buffer (0 to 128).
bits 7−0

TXFLUSH **Flush Transmit FIFO.** This bit is write-only. When set, the SPI transmit pointer is set equal to the FIFO Output pointer.
bit 7 This bit is 0 for a read operation.

CLK_EN **SCLK Driver Enable.**
bit 5 0: Disable SCLK Driver (Master Mode)
1: Enable SCLK Driver (Master Mode)

DRV_DLY **Drive Delay (refer to DRV_EN bit).**
bit 4 0: Drive Output Immediately
1: Drive Output After Current Byte Transfer

DRV_EN **Drive Enable.**
bit 3

DRV_DLY	DRV_EN	MOSI or MISO OUTPUT CONTROL
0	0	Tristate immediately.
0	1	Drive immediately.
1	0	Tristate after the current byte transfer.
1	1	Drive after the current byte transfer.

TXIRQ **Transmit IRQ Level. Write-only bits.**
bits 2−0

000	Generate IRQ when Transmit Count = 1 or less.
001	Generate IRQ when Transmit Count = 2 or less.
010	Generate IRQ when Transmit Count = 4 or less.
011	Generate IRQ when Transmit Count = 8 or less.
100	Generate IRQ when Transmit Count = 16 or less.
101	Generate IRQ when Transmit Count = 32 or less.
110	Generate IRQ when Transmit Count = 64 or less.
111	Generate IRQ when Transmit Count = 128 or less.

I²C Status (I2CSTAT) (Available only on the MSC1211 and MSC1213)

	7	6	5	4	3	2	1	0	Reset Value
SFR 9Dh	STAT7 SCKD7/SAE	STAT6 SCKD6/SA6	STAT5 SCKD5/SA5	STAT4 SCKD4/SA4	STAT3 SCKD3/SA3	0 SCKD2/SA2	0 SCKD1/SA1	0 SCKD0/SA0	00h

STAT7−3 **Status Code.** Read-only. Reading this register clears the status interrupt.
bit 7−3

STATUS CODE	STATUS OF THE HARDWARE	MODE
0x08	START condition transmitted.	Master
0x10	Repeated START condition transmitted.	Master
0x18	Slave address + W transmitted and ACK received.	Master
0x20	Slave address + W transmitted and NACK received.	Master
0x28	Data byte transmitted and ACK received.	Master
0x30	Data byte transmitted and NACK received.	Master
0x38	Arbitration lost.	Master
0x40	Slave address + R transmitted and ACK received.	Master
0x48	Slave address + R transmitted and NACK received.	Master
0x50	Data byte received and ACK transmitted.	Master
0x58	Data byte received and NACK transmitted.	Master
0x60	I2Cs slave address + W received and ACK transmitted.	Slave
0x70	General call received and ACK transmitted.	Slave
0x80	Previously addressed as slave, data byte received and ACK transmitted.	Slave
0x88	Previously addressed as slave, data byte received and NACK transmitted.	Slave
0x90	Previously addressed with GC, data byte received and ACK transmitted.	Slave
0x98	Previously addressed with GC, data byte received and NACK transmitted.	Slave
0xA0	A STOP or repeated START received when addressed as slave or GC.	Slave
0xA8	I2Cs slave address + R received and ACK transmitted.	Slave
0xB8	Previously addressed as slave, data byte transmitted and ACK received.	Slave
0xC0	Previously addressed as slave, data byte transmitted and NACK received.	Slave
0xC8	Previously addressed as slave, last data byte transmitted.	Slave

SCKD7−0 **Serial Clock Divisor.** Write-only, master mode.
bit 7−0 The frequency of the SCL line is set equal to Sysclk/[2 • (SCKD + 1)]. The minimum value for SCKD is 3.

SAE **Slave Address Enable.** Write-only, slave mode.
bit 7 In slave mode, if this is set, address recognition is enabled.

SA6−0 **Slave Address.** Write-only, slave mode.
bit 6−0 The address of this device is used in slave mode for address recognition.

I²C Start (I2CSTART) (Available only on the MSC1211 and MSC1213)

	7	6	5	4	3	2	1	0	Reset Value
SFR 9Eh									80h

I2CSTART bits 7−0 **I²C Start.** Write-only. When any value is written to this register, the I²C system is reset; that is, the counters and state machines will go back to the initial state. So, in multi-master mode when arbitration is lost, then the I²C should be reset so that the counters and finite state machines (FSMs) are brought back to the idle state.

SPI Buffer Start Address (SPISTART)

	7	6	5	4	3	2	1	0	Reset Value
SFR 9Eh	1								80h

SPISTART bits 6−0 **SPI FIFO Start Address.** Write-only. This specifies the start address of the SPI data buffer. This is a circular FIFO that is located in the 128 bytes of indirect RAM. The FIFO starts at this address and ends at the address specified in SPIEND. Must be less than SPIEND. Writing clears SPI transmit and receive counters.

SPITP bits 6−0 **SPI Transmit Pointer.** Read-only. This is the FIFO address for SPI transmissions. This is where the next byte will be written into the byte will be written into the SPI FIFO buffer. This pointer increments after each write to the SPI Data register unless that would make it equal to the SPI Receive pointer.

SPI Buffer End Address (SPIEND)

	7	6	5	4	3	2	1	0	Reset Value
SFR 9Fh	1								80h

SPIEND bits 6−0 **SPI FIFO End Address.** Write-only. This specifies the end address of the SPI data FIFO. This is a circular buffer that is located in the 128 bytes of indirect RAM. The buffer starts at SPISTART and ends at this address.

SPIRP bits 6−0 **SPI Receive Pointer.** Read-only. This is the FIFO address for SPI received bytes. This is the location of the next byte to be read from the SPI FIFO. This increments with each read from the SPI Data register until the RxCNT is zero.

Port 2 (P2)

	7	6	5	4	3	2	1	0	Reset Value
SFR A0h									FFh

P2 bits 7−0 **Port 2.** This port functions as an address bus during external memory access, and as a general-purpose I/O port. During external memory cycles, this port will contain the MSB of the address. Whether Port 2 is used as general-purpose I/O or for external memory access is determined by the Flash Configuration Register (HCR1.0).

PWM Control (PWMCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR A1h	—	—	PPOL	PWMSEL	SPDSEL	TPCNTL2	TPCNTL1	TPCNTL0	00h

PPOL **Period Polarity.** Specifies the starting level of the PWM pulse.
bit 5 0: ON Period. PWM Duty register programs the ON period.
1: OFF Period. PWM Duty register programs the OFF period.

PWMSEL **PWM Register Select.** Select which 16-bit register is accessed by PWMLOW/PWMHI.
bit 4 0: Period (must be 0 for TONE mode)
1: Duty

SPDSEL **Speed Select.**
bit 3 0: 1MHz (the USEC Clock)
1: SYSCLK

TPCNTL **Tone Generator/Pulse Width Modulation Control.**
bits 2−0

TPCNTL2	TPCNTL1	TPCNTL0	MODE
0	0	0	Disable (default)
0	0	1	PWM
0	1	1	TONE—Square
1	1	1	TONE—Staircase

Tone Low (TONELOW) /PWM Low (PWMLOW)

	7	6	5	4	3	2	1	0	Reset Value
SFR A2h	PWM7 TDIV7	PWM6 TDIV6	PWM5 TDIV5	PWM4 TDIV4	PWM3 TDIV3	PWM2 TDIV2	PWM1 TDIV1	PWM0 TDIV0	00h

PWMLOW **Pulse Width Modulator Low Bits.** These 8 bits are the least significant 8 bits of the PWM register.
bits 7−0

TDIV7−0 **Tone Divisor.** The low order bits that define the half-time period. For staircase mode the output is high impedance
bits 7−0 for the last 1/4 of this period.

Tone High (TONEHI)/PWM High (PWMHI)

	7	6	5	4	3	2	1	0	Reset Value
SFR A3h	PWM15 TDIV15	PWM14 TDIV14	PWM13 TDIV13	PWM12 TDIV12	PWM11 TDIV11	PWM10 TDIV10	PWM9 TDIV9	PWM8 TDIV8	00h

PWMHI **Pulse Width Modulator High Bits.** These 8 bits are the high order bits of the PWM register.
bits 7−0

TDIV15−8 **Tone Divisor.** The high order bits that define the half time period. For staircase mode the output is high impedance
bits 7−0 for the last 1/4 of this period.

Auxiliary Interrupt Poll (AIPOL)

		7	6	5	4	3	2	1	0	Reset Value
RD	SFR A4h	ESEC	ESUM	EADC	EMSEC	ESPIT	ESPIR/EI2C	EALV	EDLVB	00h
WR									RDSEL	00h

Auxiliary interrupts are enabled by EICON.4 (SFR D8h); other interrupts are enabled by the IE and EIE registers.

ESEC **Enable Seconds Timer Interrupt (lowest priority auxiliary interrupt).** Read-only.
bit 7 AIPOL.RDSEL = 1: Read: Current value of **Seconds Timer Interrupt** before masking.
AIPOL.RDSEL = 0: Read: Value of ESEC bit.

ESUM **Enable Summation Interrupt.** Read-only.
bit 6 AIPOL.RDSEL = 1: Read: Current value of **Summation Interrupt** before masking.
AIPOL.RDSEL = 0: Read: Value of ESUM bit.

EADC **Enable ADC Interrupt.** Read-only.
bit 5 AIPOL.RDSEL = 1: Read: Current value of **ADC Interrupt** before masking.
AIPOL.RDSEL = 0: Read: Value of EADC bit.

EMSEC **Enable Millisecond System Timer Interrupt.** Read-only.
bit 4 AIPOL.RDSEL = 1: Read: Current value of **Millisecond System Timer Interrupt** before masking.
AIPOL.RDSEL = 0: Read: Value of EMSEC bit.

ESPIT **Enable SPI Transmit Interrupt.** Read-only.
bit 3 AIPOL.RDSEL = 1: Read: Current value of **Enable SPI Transmit Interrupt** before masking.
AIPOL.RDSEL = 0: Read: Value of ESPIT bit.

ESPIR/EI2C **Enable SPI Receive Interrupt. Enable I2C Status Interrupt (I^2C available only on the MSC1213).** Read-only.
bit 2 AIPOL.RDSEL = 1: Read: Current value of **Enable SPI Receive Interrupt** or **I2C Status Interrupt** before masking.
AIPOL.RDSEL = 0: Read: Value of ESPIR/EI2C bit.

EALV **Enable Analog Low Voltage Interrupt.** Read-only.
bit 1 AIPOL.RDSEL = 1: Read: Current value of **Enable Analog Low Voltage Interrupt** before masking.
AIPOL.RDSEL = 0: Read: Value of EALV bit.

EDLVB **Enable Digital Low Voltage or Breakpoint Interrupt (highest priority auxiliary interrupt).** Read-only.
bit 0 AIPOL.RDSEL = 1: Read: Current value of **Enable Digital Low Voltage** or **Breakpoint Interrupt** before masking.
AIPOL.RDSEL = 0: Read: Value of EDLVB bit.

RDSEL **Read Select.** Write-only.
bit 0 AIPOL.RDSEL = 1: **Read state for AIE and AIPOL registers.** Reading AIPOL register gives current value of Auxiliary interrupts before masking. Reading AIE register gives value of AIE register contents.

AIPOL.RDSEL = 0: **Read state for AIE and AIPOL registers.** Reading AIPOL register gives value of AIE register contents. Reading AIE register gives current value of Auxiliary interrupts before masking.

Pending Auxiliary Interrupt (PAI)

	7	6	5	4	3	2	1	0	Reset Value
SFR A5h	0	0	0	0	PAI3	PAI2	PAI1	PAI0	00h

PAI3−0 bits 3−0 **Pending Auxiliary Interrupt.** The results of this register can be used as an index to vector to the appropriate interrupt routine. All of these interrupts vector through address 0033h.

PAI3	PAI2	PAI1	PAI0	AUXILIARY INTERRUPT STATUS
0	0	0	0	No Pending Auxiliary IRQ
0	0	0	1	Digital Low Voltage IRQ Pending
0	0	1	0	Analog Low Voltage IRQ Pending
0	0	1	1	SPI Receive IRQ Pending. I^2C Status Pending.
0	1	0	0	SPI Transmit IRQ Pending.
0	1	0	1	One Millisecond System Timer IRQ Pending.
0	1	1	0	Analog-to-Digital Conversion IRQ Pending.
0	1	1	1	Accumulator IRQ Pending.
1	0	0	0	One Second System Timer IRQ Pending.

Auxiliary Interrupt Enable (AIE)

	7	6	5	4	3	2	1	0	Reset Value
SFR A6h	ESEC	ESUM	EADC	EMSEC	ESPIT	ESPIR/EI2C	EALV	EDLVB	00h

Auxiliary interrupts are enabled by EICON.4 (SFR D8h); other interrupts are enabled by the IE and EIE registers.

ESEC **Enable Seconds Timer Interrupt (lowest priority auxiliary interrupt).**
bit 7 Write: Set mask bit for this interrupt; 0 = masked, 1 = enabled.
Read: When AIPOL.RDSEL = 0: Current value of **Seconds Timer Interrupt** before masking.
When AIPOL.RDSEL = 1: Value of **ESEC** bit.

ESUM **Enable Summation Interrupt.**
bit 6 Write: Set mask bit for this interrupt; 0 = masked, 1 = enabled.
Read: When AIPOL.RDSEL = 0: Current value of **Summation Interrupt** before masking.
When AIPOL.RDSEL = 1: Value of **ESUM** bit.

EADC **Enable ADC Interrupt.**
bit 5 Write: Set mask bit for this interrupt; 0 = masked, 1 = enabled.
Read: When AIPOL.RDSEL = 0: Current value of **ADC Interrupt** before masking.
When AIPOL.RDSEL = 1: Value of **EADC** bit.

EMSEC **Enable Millisecond System Timer Interrupt.**
bit 4 Write: Set mask bit for this interrupt; 0 = masked, 1 = enabled.
Read: When AIPOL.RDSEL = 0: Current value of **Millisecond System Timer Interrupt** before masking.
When AIPOL.RDSEL = 1: Value of **EMSEC** bit.

ESPIT **Enable SPI Transmit Interrupt.**
bit 3 Write: Set mask bit for this interrupt; 0 = masked, 1 = enabled.
Read: When AIPOL.RDSEL = 0: Current value of **SPI Transmit Interrupt** before masking.
When AIPOL.RDSEL = 1: Value of **ESPIT** bit.

ESPIR/EI2C **Enable SPI Receive Interrupt. Enable I^2C Status Interrupt. (I^2C available only on the MSC1213.)**
bit 2 Write: Set mask bit for this interrupt; 0 = masked, 1 = enabled.
Read: When AIPOL.RDSEL = 0: Current value of **SPI Receive Interrupt** or **I^2C Status Interrupt** before masking.
When AIPOL.RDSEL = 1: Value of **ESPIR/EI2C** bit.

EALV **Enable Analog Low Voltage Interrupt.**
bit 1 Write: Set mask bit for this interrupt; 0 = masked, 1 = enabled.
Read: When AIPOL.RDSEL = 0: Current value of **Analog Low Voltage Interrupt** before masking.
When AIPOL.RDSEL = 1: Value of **EALV** bit.

EDLVB **Enable Digital Low Voltage or Breakpoint Interrupt (highest priority auxiliary interrupt).**
bit 0 Write: Set mask bit for this interrupt; 0 = masked, 1 = enabled.
Read: When AIPOL.RDSEL = 0: Current value of **Digital Low Voltage** or **Breakpoint Interrupt** before masking.
When AIPOL.RDSEL = 1: Value of **EDLVB** bit.

Auxiliary Interrupt Status (AISTAT)

	7	6	5	4	3	2	1	0	Reset Value
SFR A7h	SEC	SUM	ADC	MSEC	SPIT	SPIR/I2CSI	ALVD	DLVD	00h

SEC **Second System Timer Interrupt Status Flag (lowest priority AI).**
bit 7 0: SEC interrupt inactive or masked.
1: SEC Interrupt active.

SUM **Summation Register Interrupt Status Flag.**
bit 6 0: SUM interrupt inactive or masked (if active, it is set inactive by reading the lowest byte of the Summation register).
1: SUM interrupt active.

ADC **ADC Interrupt Status Flag.**
bit 5 0: ADC interrupt inactive or masked (If active, it is set inactive by reading the lowest byte of the Data Output Register).
1: ADC interrupt active (If active no new data will be written to the Data Output Register).

MSEC **Millisecond System Timer Interrupt Status Flag.**
bit 4 0: MSEC interrupt inactive or masked.
1: MSEC interrupt active.

SPIT **SPI Transmit Interrupt Status Flag.**
bit 3 0: SPI transmit interrupt inactive or masked.
1: SPI transmit interrupt active.

SPIR/I2CSI **SPI Receive Interrupt Status Flag. I^2C Status Interrupt. (I^2C available only on the MSC1213.)**
bit 2 0: SPI receive or I2CSI interrupt inactive or masked.
1: SPI receive or I2CSI interrupt active.

ALVD **Analog Low Voltage Detect Interrupt Status Flag.**
bit 1 0: ALVD interrupt inactive or masked.
1: ALVD interrupt active.

DLVD **Digital Low Voltage Detect or Breakpoint Interrupt Status Flag (highest priority AI).**
bit 0 0: DLVD interrupt inactive or masked.
1: DLVD interrupt active.

Interrupt Enable (IE)

	7	6	5	4	3	2	1	0	Reset Value
SFR A8h	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0	00h

EA **Global Interrupt Enable.** This bit controls the global masking of all interrupts except those in AIE (SFR A6h).
bit 7 0: Disable interrupt sources. This bit overrides individual interrupt mask settings for this register.
1: Enable all individual interrupt masks. Individual interrupts in this register will occur if enabled.

ES1 **Enable Serial Port 1 Interrupt.** This bit controls the masking of the serial Port 1 interrupt.
bit 6 0: Disable all serial Port 1 interrupts.
1: Enable interrupt requests generated by the RI_1 (SCON1.0, SFR C0h) or TI_1 (SCON1.1, SFR C0h) flags.

ET2 **Enable Timer 2 Interrupt.** This bit controls the masking of the Timer 2 interrupt.
bit 5 0: Disable all Timer 2 interrupts.
1: Enable interrupt requests generated by the TF2 flag (T2CON.7, SFR C8h).

ES0 **Enable Serial port 0 interrupt.** This bit controls the masking of the serial Port 0 interrupt.
bit 4 0: Disable all serial Port 0 interrupts.
1: Enable interrupt requests generated by the RI_0 (SCON0.0, SFR 98h) or TI_0 (SCON0.1, SFR 98h) flags.

ET1 **Enable Timer 1 Interrupt.** This bit controls the masking of the Timer 1 interrupt.
bit 3 0: Disable Timer 1 interrupt.
1: Enable interrupt requests generated by the TF1 flag (TCON.7, SFR 88h).

EX1 **Enable External Interrupt 1.** This bit controls the masking of external interrupt 1.
bit 2 0: Disable external interrupt 1.
1: Enable interrupt requests generated by the $\overline{\text{INT1}}$ pin.

ET0 **Enable Timer 0 Interrupt.** This bit controls the masking of the Timer 0 interrupt.
bit 1 0: Disable all Timer 0 interrupts.
1: Enable interrupt requests generated by the TF0 flag (TCON.5, SFR 88h).

EX0 **Enable External Interrupt 0.** This bit controls the masking of external interrupt 0.
bit 0 0: Disable external interrupt 0.
1: Enable interrupt requests generated by the $\overline{\text{INT0}}$ pin.

Breakpoint Control (BPCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR A9h	BP	0	0	0	0	0	PMSEL	EBP	00h

Writing to this register sets the breakpoint condition specified by MCON, BPL, and BPH.

BP **Breakpoint Interrupt.** This bit indicates that a break condition has been recognized by a hardware breakpoint register(s).
bit 7 Read: Status of Breakpoint Interrupt. Will indicate a breakpoint match for any of the breakpoint registers.
Write: 0: No effect.
1: Clear Breakpoint 1 for breakpoint register selected by MCON (SFR 95h).

PMSEL **Program Memory Select.** Write this bit to select memory for address breakpoints of register selected in
bit 1 MCON (SFR 95h).
0: Break on address in Data Memory.
1: Break on address in Program Memory.

EBP **Enable Breakpoint.** This bit enables this breakpoint register. Address of breakpoint register selected by
bit 0 MCON (SFR 95h).
0: Breakpoint disabled.
1: Breakpoint enabled.

Breakpoint Low (BPL) Address for BP Register Selected in MCON (95h)

	7	6	5	4	3	2	1	0	Reset Value
SFR AAh	BPL.7	BPL.6	BPL.5	BPL.4	BPL.3	BPL.2	BPL.1	BPL.0	00h

BPL.7−0 **Breakpoint Low Address.** The low 8 bits of the 16-bit breakpoint address.
bits 7−0

Breakpoint High Address (BPH) Address for BP Register Selected in MCON (95h)

	7	6	5	4	3	2	1	0	Reset Value
SFR ABh	BPH.7	BPH.6	BPH.5	BPH.4	BPH.3	BPH.2	BPH.1	BPH.0	00h

BPH.7−0 **Breakpoint High Address.** The high 8 bits of the 16-bit breakpoint address**.**
bits 7−0

Port 0 Data Direction Low (P0DDRL)

	7	6	5	4	3	2	1	0	Reset Value
SFR ACh	P03H	P03L	P02H	P02L	P01H	P01L	P00H	P00L	00h

P0.3 **Port 0 Bit 3 Control.**

bits 7−6

P03H	P03L	
0	0	Standard 8051 (Pull-Up)
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P0.2 **Port 0 Bit 2 Control.**

bits 5−4

P02H	P02L	
0	0	Standard 8051 (Pull-Up)
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P0.1 **Port 0 Bit 1 Control.**

bits 3−2

P01H	P01L	
0	0	Standard 8051 (Pull-Up)
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P0.0 **Port 0 Bit 0 Control.**

bits 1−0

P00H	P00L	
0	0	Standard 8051 (Pull-Up)
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

NOTE: Port 0 also controlled by $\overline{EA}$ and Memory Access Control HCR1.EGP0.

Port 0 Data Direction High (P0DDRH)

	7	6	5	4	3	2	1	0	Reset Value
SFR ADh	P07H	P07L	P06H	P06L	P05H	P05L	P04H	P04L	00h

P0.7 **Port 0 Bit 7 Control.**

bits 7−6

P07H	P07L	
0	0	Standard 8051 (Pull-Up)
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P0.6 **Port 0 Bit 6 Control.**

bits 5−4

P06H	P06L	
0	0	Standard 8051 (Pull-Up)
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P0.5 **Port 0 Bit 5 Control.**

bits 3−2

P05H	P05L	
0	0	Standard 8051 (Pull-Up)
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P0.4 **Port 0 Bit 4 Control.**

bits 1−0

P04H	P04L	
0	0	Standard 8051 (Pull-Up)
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

NOTE: Port 0 also controlled by $\overline{EA}$ and Memory Access Control HCR1.EGP0.

Port 1 Data Direction Low (P1DDRL)

	7	6	5	4	3	2	1	0	Reset Value
SFR AEh	P13H	P13L	P12H	P12L	P11H	P11L	P10H	P10L	00h

P1.3 **Port 1 Bit 3 Control.**

bits 7−6

P13H	P13L	
0	0	Standard 8051 (Pull-Up)
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P1.2 **Port 1 Bit 2 Control.**

bits 5−4

P12H	P12L	
0	0	Standard 8051 (Pull-Up)
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P1.1 **Port 1 Bit 1 Control.**

bits 3−2

P11H	P11L	
0	0	Standard 8051 (Pull-Up)
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P1.0 **Port 1 Bit 0 Control.**

bits 1−0

P10H	P10L	
0	0	Standard 8051 (Pull-Up)
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

Port 1 Data Direction High (P1DDRH)

	7	6	5	4	3	2	1	0	Reset Value
SFR AFh	P17H	P17L	P16H	P16L	P15H	P15L	P14H	P14L	00h

P1.7 **Port 1 Bit 7 Control.**

bits 7−6

P17H	P17L	
0	0	Standard 8051 (Pull-Up)
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P1.6 **Port 1 Bit 6 Control.**

bits 5−4

P16H	P16L	
0	0	Standard 8051 (Pull-Up)
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P1.5 **Port 1 Bit 5 Control.**

bits 3−2

P15H	P15L	
0	0	Standard 8051 (Pull-Up)
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P1.4 **Port 1 Bit 4 Control.**

bits 1−0

P14H	P14L	
0	0	Standard 8051 (Pull-Up)
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

Port 3 (P3)

	7	6	5	4	3	2	1	0	Reset Value
SFR B0h	P3.7 $\overline{RD}$	P3.6 $\overline{WR}$	P3.5 T1	P3.4 T0	P3.3 $\overline{INT1}$	P3.2 $\overline{INT0}$	P3.1 TXD0	P3.0 RXD0	FFh

P3.7−0 bits 7−0 **General-Purpose I/O Port 3.** This register functions as a general-purpose I/O port. In addition, all the pins have an alternative function listed below. Each of the functions is controlled by several other SFRs. The associated Port 3 latch bit must contain a logic ‘1’ before the pin can be used in its alternate function capacity.

$\overline{RD}$ bit 7 **External Data Memory Read Strobe.** This pin provides an active low read strobe to an external memory device. If Port 0 or Port 2 is selected for external memory in the HCR1 register, this function will be enabled even if a ‘1’ is not written to this latch bit. When external memory is selected, the settings of P3DRRH are ignored.

$\overline{WR}$ bit 6 **External Data Memory Write Strobe.** This pin provides an active low write strobe to an external memory device. If Port 0 or Port 2 is selected for external memory in the HCR1 register, this function will be enabled even if a ‘1’ is not written to this latch bit. When external memory is selected, the settings of P3DRRH are ignored.

T1 bit 5 **Timer/Counter 1 External Input.** A 1 to 0 transition on this pin will increment Timer 1.

T0 bit 4 **Timer/Counter 0 External Input.** A 1 to 0 transition on this pin will increment Timer 0.

$\overline{INT1}$ bit 3 **External Interrupt 1.** A falling edge/low level on this pin will cause an external interrupt 1 if enabled.

$\overline{INT0}$ bit 2 **External Interrupt 0.** A falling edge/low level on this pin will cause an external interrupt 0 if enabled.

TXD0 bit 1 **Serial Port 0 Transmit.** This pin transmits the serial Port 0 data in serial port modes 1, 2, 3, and emits the synchronizing clock in serial port mode 0.

RXD0 bit 0 **Serial Port 0 Receive.** This pin receives the serial Port 0 data in serial port modes 1, 2, 3, and is a bidirectional data transfer pin in serial port mode 0.

Port 2 Data Direction Low (P2DDRL)

	7	6	5	4	3	2	1	0	Reset Value
SFR B1h	P23H	P23L	P22H	P22L	P21H	P21L	P20H	P20L	00h

P2.3 **Port 2 Bit 3 Control.**

bits 7−6

P23H	P23L	
0	0	Standard 8051 (Pull-Up)
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P2.2 **Port 2 Bit 2 Control.**

bits 5−4

P22H	P22L	
0	0	Standard 8051 (Pull-Up)
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P2.1 **Port 2 Bit 1 Control.**

bits 3−2

P21H	P21L	
0	0	Standard 8051 (Pull-Up)
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P2.0 **Port 2 Bit 0 Control.**

bits 1−0

P20H	P20L	
0	0	Standard 8051 (Pull-Up)
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

NOTE: Port 2 also controlled by $\overline{EA}$ and Memory Access Control HCR1.EGP23.

Port 2 Data Direction High (P2DDRH)

	7	6	5	4	3	2	1	0	Reset Value
SFR B2h	P27H	P27L	P26H	P26L	P25H	P25L	P24H	P24L	00h

P2.7 **Port 2 Bit 7 Control.**

bits 7−6

P27H	P27L	
0	0	Standard 8051 (Pull-Up)
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P2.6 **Port 2 Bit 6 Control.**

bits 5−4

P26H	P26L	
0	0	Standard 8051 (Pull-Up)
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P2.5 **Port 2 Bit 5 Control.**

bits 3−2

P25H	P25L	
0	0	Standard 8051 (Pull-Up)
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P2.4 **Port 2 Bit 4 Control.**

bits 1−0

P24H	P24L	
0	0	Standard 8051 (Pull-Up)
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

NOTE: Port 2 also controlled by $\overline{EA}$ and Memory Access Control HCR1.EGP23.

Port 3 Data Direction Low (P3DDRL)

	7	6	5	4	3	2	1	0	Reset Value
SFR B3h	P33H	P33L	P32H	P32L	P31H	P31L	P30H	P30L	00h

P3.3 **Port 3 Bit 3 Control.**

bits 7−6

P33H	P33L	
0	0	Standard 8051 (Pull-Up)
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P3.2 **Port 3 Bit 2 Control.**

bits 5−4

P32H	P32L	
0	0	Standard 8051 (Pull-Up)
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P3.1 **Port 3 Bit 1 Control.**

bits 3−2

P31H	P31L	
0	0	Standard 8051 (Pull-Up)
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P3.0 **Port 3 Bit 0 Control.**

bits 1−0

P30H	P30L	
0	0	Standard 8051 (Pull-Up)
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

Port 3 Data Direction High (P3DDRH)

	7	6	5	4	3	2	1	0	Reset Value
SFR B4h	P37H	P37L	P36H	P36L	P35H	P35L	P34H	P34L	00h

P3.7 Port 3 Bit 7 Control.

bits 7−6

P37H	P37L	
0	0	Standard 8051 (Pull-Up)
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

NOTE: Port 3.7 also controlled by $\overline{EA}$ and Memory Access Control HCR1.1.

P3.6 Port 3 Bit 6 Control.

bits 5−4

P36H	P36L	
0	0	Standard 8051 (Pull-Up)
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

NOTE: Port 3.6 also controlled by $\overline{EA}$ and Memory Access Control HCR1.1.

P3.5 Port 3 Bit 5 Control.

bits 3−2

P35H	P35L	
0	0	Standard 8051 (Pull-Up)
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P3.4 Port 3 Bit 4 Control.

bits 1−0

P34H	P34L	
0	0	Standard 8051 (Pull-Up)
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

DAC Low Byte (DACL)

	7	6	5	4	3	2	1	0	Reset Value
SFR B5h									00h

DACL7−0 **Least Significant Byte Register for DAC0−3, DAC Control (0 and 2), and DAC Load Control .**
bits 7−0

NOTE: DAC2 and DAC3 available only on the MSC1211 and MSC1212.

DAC High Byte (DACH)

	7	6	5	4	3	2	1	0	Reset Value
SFR B6h									00h

DACH7−0 **Most Significant Byte Register for DAC0−3 and DAC Control (1 and 3).**
bits 7−0

NOTE: DAC2 and DAC3 available only on the MSC1211 and MSC1212.

DAC Select (DACSEL)

	7	6	5	4	3	2	1	0	Reset Value
SFR B7h	DSEL7	DSEL6	DSEL5	DSEL4	DSEL3	DSEL2	DSEL1	DSEL0	00h

DSEL7−0 **DAC Select and DAC Control Select.** The DACSEL register selects which DAC output register or which DAC
bits 7−0 control register is accessed by the DACL and DACH registers.

DACSEL (B7h)	DACH (B6h)	DACL (B5h)	RESET VALUE
00h	DAC0 (high)	DAC0 (low)	0000h
01h	DAC1 (high)	DAC1 (low)	0000h
02h	DAC2(1) (high)	DAC2(1) (low)	0000h
03h	DAC3(1) (high)	DAC3(1) (low)	0000h
04h	DACCON1	DACCON0	6363h
05h	DACCON3(1)	DACCON2(1)	0303h
06h	—	LOADCON	−−00h
07h	—	—	—

(1) DAC2 and DAC3 available only on the MSC1211 and MSC1212.

DAC0 Control (DACCON0)

DACSEL = 04h	7	6	5	4	3	2	1	0	Reset Value
SFR B5h	COR0	EOD0	IDAC0DIS	IDAC0SINK	0	SELREF0	DOM0_1	DOM0_0	63h

COR0 **Current Over Range on DAC0**

bit 7 Write: 0 = Clear to release from high-impedance state back to normal mode unless an over-range condition exists.
1 = NOP

Read: 0 = No current over range for DAC0.
0 = NOP
1 = IDAC overcurrent for three consecutive ticks on ms clock USEC (EOD0 = 1) or Current Over Range raw signal (EOD0 = 0).

EOD0 **Enable Over-Current Detection**

bit 6 0 = Disable over-current detection.
1 = Enable over-current detection (default). After three consecutive ticks on MSEC clock of overcurrent, the DAC is disabled; however, the register values are preserved. Writing to COR0 releases the high-impedance state.

IDAC0DIS **IDAC0 Disable (for DOM0 = 00)**

bit 5 0 = IDAC on mode for DAC0.
1 = IDAC off mode for DAC0 (default).

IDAC0SINK **ENABLE CURRENT SINK**

bit 4 0 = DAC0 is sourcing current.
1 = DAC0 is sinking current using external device.

Not Used

bit 3

SELREF0 **Select the Reference Voltage for DAC0 Voltage Reference.**

bit 2 0 = DAC0 V_{REF} = AV_{DD} (default).
1 = DAC0 V_{REF} = voltage on REF IN+/REFOUT pin.

DOM0_1−0 **DAC Output Mode DAC0.**

bits 1−0

DOM0	OUTPUT MODE for DAC0
00	Normal VDAC output; IDAC controlled by IDAC0DIS bit.
01	Power-Down mode—VDAC output off 1kΩ to AGND, IDAC off.
10	Power-Down mode—VDAC output off 100kΩ to AGND, IDAC off.
11	Power-Down mode—VDAC output off high impedance, IDAC off (default).

DAC1 Control (DACCON1)

DACSEL = 04h	7	6	5	4	3	2	1	0	Reset Value
SFR B6h	COR1	EOD1	IDAC1DIS	IDAC1SINK	0	SELREF1	DOM1_1	DOM1_0	63h

COR1 **Current Over Range on DAC1**

bit 7 Write: 0 = Clear to release from high-impedance state back to normal mode unless an over-range condition exists.
1 = No effect.
Read: 0 = No current over range for DAC1.
0 = No effect.
1 = IDAC overcurrent for three consecutive ticks on ms clock USEC (EOD1 = 1) or Current Over Range raw signal (EOD0 = 0).

EOD1 **Enable Over-Current Detection**

bit 6 0 = Disable over-current detection.
1 = Enable over-current detection (default). After three consecutive ticks on MSEC clock of overcurrent, the DAC is disabled; however, the register values are preserved. Writing to COR1 releases the high-impedance state.

IDAC1DIS **IDAC1 Disable (for DOM1 = 00)**

bit 5 0 = IDAC on mode for DAC1.
1 = IDAC off mode for DAC1 (default).

IDAC1SINK **ENABLE CURRENT SINK**

bit 4 0 = DAC1 is sourcing current.
1 = DAC1 is sinking current using external device.

Not Used

bit 3

SELREF1 **Select the Reference Voltage for DAC1 Voltage Reference.**

bit 2 0 = DAC1 V_{REF} = AV_{DD} (default).
1 = DAC1 V_{REF} = voltage on V_{REF} IN pins.

DOM1_1−0 **DAC Output Mode DAC1.**

bits 1−0

DOM1	OUTPUT MODE for DAC1
00	Normal VDAC output; IDAC controlled by IDAC1DIS bit.
01	Power-Down mode—VDAC output off 1kΩ to AGND, IDAC off.
10	Power-Down mode—VDAC output off 100kΩ to AGND, IDAC off.
11	Power-Down mode—VDAC output off high impedance, IDAC off (default).

DAC2 Control (DACCON2) (Available only on the MSC1211 and MSC1212)

DACSEL = 05h	7	6	5	4	3	2	1	0	Reset Value
SFR B5h	0	0	0	0	0	SELREF2	DOM2_1	DOM2_0	03h

SELREF2 Select the Reference Voltage for DAC2 Voltage Reference.

bit 2 0 = DAC2 V_{REF} = AV_{DD} (default).
1 = DAC2 V_{REF} = internal V_{REF}.

DOM2_1−0 DAC Output Mode DAC2.

bits 1−0

DOM2	OUTPUT MODE for DAC2
00	Normal VDAC output.
01	Power-Down mode—VDAC output off 1kΩ to AGND, IDAC off.
10	Power-Down mode—VDAC output off 100kΩ to AGND, IDAC off.
11	Power-Down mode—VDAC output off high impedance, IDAC off (default).

DAC3 Control (DACCON3) (Available only on the MSC1211 and MSC1212)

DACSEL = 05h	7	6	5	4	3	2	1	0	Reset Value
SFR B6h	0	0	0	0	0	SELREF3	DOM3_1	DOM3_0	03h

SELREF3 Select the Reference Voltage for DAC3 Voltage Reference.

bit 2 0 = DAC3 V_{REF} = AV_{DD} (default).
1 = DAC3 V_{REF} = internal V_{REF}.

DOM3_1−0 DAC Output Mode DAC3.

bits 1−0

DOM2	OUTPUT MODE for DAC3
00	Normal VDAC output.
01	Power-Down mode—VDAC output off 1kΩ to AGND, IDAC off.
10	Power-Down mode—VDAC output off 100kΩ to AGND, IDAC off.
11	Power-Down mode—VDAC output off high impedance, IDAC off (default).

DAC Load Control (LOADCON)

DACSEL = 06h	7	6	5	4	3	2	1	0	Reset Value
SFR B5h	D3LOAD1	D3LOAD0	D2LOAD1	D2LOAD0	D1LOAD1	D1LOAD0	D0LOAD1	D0LOAD0	00h

D3LOAD1−0 (Available only on MSC1211 and MSC1212)

bit 7−6 The DAC load options are listed below:

DxLOAD	OUTPUT MODE for
00	Direct load: write to DACxL directly loads the DAC buffer and the DAC output (write to DACxH does not load DAC output).
01	Delay load: the values last written to DACxL/DACxH will be transferred to the DAC output on the next MSEC timer tick.
10	Delay load: the values last written to DACxL/DACxH will be transferred to the DAC output on the next HMSEC timer tick.
11	Sync load: the values contained in the DACxL/DACxH registers will be transferred to the DAC output immediately after 11b is written to this register.

D2LOAD1−0 (Available only on MSC1211 and MSC1212)

bit 5−4

D1LOAD1−0

bit 3−2

D0LOAD1−0

bit 1−0

Interrupt Priority (IP)

	7	6	5	4	3	2	1	0	Reset Value
SFR B8h	1	PS1	PT2	PS0	PT1	PX1	PT0	PX0	80h

PS1 **Serial Port 1 Interrupt.** This bit controls the priority of the serial Port 1 interrupt.
bit 6 0 = Serial Port 1 priority is determined by the natural priority order.
1 = Serial Port 1 is a high-priority interrupt.

PT2 **Timer 2 Interrupt.** This bit controls the priority of the Timer 2 interrupt.
bit 5 0 = Timer 2 priority is determined by the natural priority order.
1 = Timer 2 priority is a high-priority interrupt.

PS0 **Serial Port 0 Interrupt.** This bit controls the priority of the serial Port 0 interrupt.
bit 4 0 = Serial Port 0 priority is determined by the natural priority order.
1 = Serial Port 0 is a high-priority interrupt.

PT1 **Timer 1 Interrupt.** This bit controls the priority of the Timer 1 interrupt.
bit 3 0 = Timer 1 priority is determined by the natural priority order.
1 = Timer 1 priority is a high-priority interrupt.

PX1 **External Interrupt 1.** This bit controls the priority of external interrupt 1.
bit 2 0 = External interrupt 1 priority is determined by the natural priority order.
1 = External interrupt 1 is a high-priority interrupt.

PT0 **Timer 0 Interrupt.** This bit controls the priority of the Timer 0 interrupt.
bit 1 0 = Timer 0 priority is determined by the natural priority order.
1 = Timer 0 priority is a high-priority interrupt.

PX0 **External Interrupt 0.** This bit controls the priority of external interrupt 0.
bit 0 0 = External interrupt 0 priority is determined by the natural priority order.
1 = External interrupt 0 is a high-priority interrupt.

Serial Port 1 Control (SCON1)

	7	6	5	4	3	2	1	0	Reset Value
SFR C0h	SM0_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1	00h

SM0−2 bits 7−5 **Serial Port 1 Mode.** These bits control the mode of serial Port 1. Modes 1, 2, and 3 have 1 start and 1 stop bit in addition to the 8 or 9 data bits.

MODE	SM0	SM1	SM2	FUNCTION	LENGTH	PERIOD
0	0	0	0	Synchronous	8 bits	12 p_{CLK}(1)
0	0	0	1	Synchronous	8 bits	4 p_{CLK}(1)
1(2)	0	1	0	Asynchronous	10 bits	Timer 1 Baud Rate Equation
1(2)	0	1	1	Valid Stop Required(3)	10 bits	Timer 1 Baud Rate Equation
2	1	0	0	Asynchronous	11 bits	64 p_{CLK}(1) (SMOD = 0) 32 p_{CLK}(1) (SMOD = 1)
2	1	0	1	Asynchronous with Multiprocessor Communication(4)	11 bits	64 p_{CLK}(1) (SMOD = 0) 32 p_{CLK}(1) (SMOD = 1)
3(2)	1	1	0	Asynchronous	11 bits	Timer 1 Baud Rate Equation
3(2)	1	1	1	Asynchronous with Multiprocessor Communication(4)	11 bits	Timer 1 Baud Rate Equation

(1) p_{CLK} will be equal to t_{CLK}, except that p_{CLK} will stop for Idle mode.
(2) For modes 1 and 3, the selection of Timer 1 for baud rate is specified via the T2CON (C8h) register.
(3) RI_0 will only be activated when a valid STOP is received.
(4) RI_0 will not be activated if bit 9 = 0.

REN_1 bit 4 **Receive Enable.** This bit enables/disables the serial Port 1 received shift register.
0 = Serial Port 1 reception disabled.
1 = Serial Port 1 received enabled (modes 1, 2, and 3). Initiate synchronous reception (mode 0).

TB8_1 bit 3 **9th Transmission Bit State.** This bit defines the state of the 9th transmission bit in serial Port 1 modes 2 and 3.

RB8_1 bit 2 **9th Received Bit State.** This bit identifies the state of the 9th reception bit of received data in serial Port 1 modes 2 and 3. In serial port mode 1, when SM2_1 = 0, RB8_1 is the state of the stop bit. RB8_1 is not used in mode 0.

TI_1 bit 1 **Transmitter Interrupt Flag.** This bit indicates that data in the serial Port 1 buffer has been completely shifted out. In serial port mode 0, TI_1 is set at the end of the 8th data bit. In all other modes, this bit is set at the end of the last data bit. This bit must be cleared by software to transmit the next byte.

RI_1 bit 0 **Receiver Interrupt Flag.** This bit indicates that a byte of data has been received in the serial Port 1 buffer. In serial port mode 0, RI_1 is set at the end of the 8th bit. In serial port mode 1, RI_1 is set after the last sample of the incoming stop bit subject to the state of SM2_1. In modes 2 and 3, RI_1 is set after the last sample of RB8_1. This bit must be cleared by software to receive the next byte.

Serial Data Buffer 1 (SBUF1)

	7	6	5	4	3	2	1	0	Reset Value
SFR C1h									00h

SBUF1.7−0 bits 7−0 **Serial Data Buffer 1.** Data for serial Port 1 is read from or written to this location. The serial transmit and receive buffers are separate registers, but both are addressed at this location.

Enable Wake Up (EWU) Waking Up from Idle Mode

	7	6	5	4	3	2	1	0	Reset Value
SFR C6h	—	—	—	—	—	EWUWDT	EWUEX1	EWUEX0	00h

Auxiliary interrupts will wake up from Idle mode. They are enabled with EAI (EICON.5).

EWUWDT **Enable Wake Up Watchdog Timer.** Wake using watchdog timer interrupt.
bit 2 0 = Don't wake up on watchdog timer interrupt.
1 = Wake up on watchdog timer interrupt.

EWUEX1 **Enable Wake Up External 1.** Wake using external interrupt source 1.
bit 1 0 = Don't wake up on external interrupt source 1.
1 = Wake up on external interrupt source 1.

EWUEX0 **Enable Wake Up External 0.** Wake using external interrupt source 0.
bit 0 0 = Don't wake up on external interrupt source 0.
1 = Wake up on external interrupt source 0.

System Clock Divider (SYSCLK)

	7	6	5	4	3	2	1	0	Reset Value
SFR C7h	0	0	DIVMOD1	DIVMOD0	0	DIV2	DIV1	DIV0	00h

NOTE: Changing SYSCLK registers affects all internal clocks, including the ADC clock.

DIVMOD1−0 Clock Divide Mode
bits 5−4 Write:

DIVMOD	DIVIDE MODE
00	Normal mode (default, no divide).
01	Immediate mode: start divide immediately; return to Normal mode on Idle mode wakeup condition or by direct write to SFR.
10	Delay mode: same as Immediate mode, except that the mode changes with the millisecond interrupt (MSINT). If MSINT is enabled, the divide will start on the next MSINT and return to normal mode on the following MSINT. If MSINT is not enabled, the divide will start on the next MSINT condition (even if masked) but will not leave the divide mode until the MSINT counter overflows, which follows a wakeup condition. Can exit by directly writing to SFR.
11	Manual mode: start divide immediately; exit mode only by directly writing to SFR. Same as immediate mode, but cannot return to Normal mode on Idle mode wakeup condition; only by directly writing to SFR.

Read:

DIVMOD	DIVISION MODE STATUS
00	No divide
01	Divider is in Immediate mode
10	Divider is in Delay mode
11	Medium mode

DIV2−0 Divide Mode
bit 2−0

DIV	DIVISOR	f_{CLK} FREQUENCY
000	Divide by 2 (default)	$f_{CLK} = f_{SYS}/2$
001	Divide by 4	$f_{CLK} = f_{SYS}/4$
010	Divide by 8	$f_{CLK} = f_{SYS}/8$
011	Divide by 16	$f_{CLK} = f_{SYS}/16$
100	Divide by 32	$f_{CLK} = f_{SYS}/32$
101	Divide by 1024	$f_{CLK} = f_{SYS}/1024$
110	Divide by 2048	$f_{CLK} = f_{SYS}/2048$
111	Divide by 4096	$f_{CLK} = f_{SYS}/4096$

Timer 2 Control (T2CON)

	7	6	5	4	3	2	1	0	Reset Value
SFR C8h	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$	00h

TF2 bit 7 — **Timer 2 Overflow Flag.** This flag will be set when Timer 2 overflows from FFFFh. It must be cleared by software. TF2 will only be set if RCLK and TCLK are both cleared to '0'. Writing a '1' to TF2 forces a Timer 2 interrupt if enabled.

EXF2 bit 6 — **Timer 2 External Flag.** A negative transition on the T2EX pin (P1.1) will cause this flag to be set based on the EXEN2 (T2CON.3) bit. If set by a negative transition, this flag must be cleared to '0' by software. Setting this bit in software will force a timer interrupt if enabled.

RCLK bit 5 — **Receive Clock Flag.** This bit determines the serial Port 0 timebase when receiving data in serial modes 1 or 3.

0 = Timer 1 overflow is used to determine receiver baud rate for USART0.

1 = Timer 2 overflow is used to determine receiver baud rate for USART0.

Setting this bit will force Timer 2 into baud rate generation mode. The timer will operate from a divide by 2 of the external clock.

TCLK bit 4 — **Transmit Clock Flag.** This bit determines the serial Port 0 timebase when transmitting data in serial modes 1 or 3.

0 = Timer 1 overflow is used to determine transmitter baud rate for USART0.

1 = Timer 2 overflow is used to determine transmitter baud rate for USART0.

Setting this bit will force Timer 2 into baud rate generation mode. The timer will operate from a divide by 2 of the external clock.

EXEN2 bit 3 — **Timer 2 External Enable.** This bit enables the capture/reload function on the T2EX pin if Timer 2 is not generating baud rates for the serial port.

0 = Timer 2 will ignore all external events at T2EX.

1 = Timer 2 will capture or reload a value if a negative transition is detected on the T2EX pin.

TR2 bit 2 — **Timer 2 Run Control.** This bit enables/disables the operation of Timer 2. Halting this timer will preserve the current count in TH2, TL2.

0 = Timer 2 is halted.

1 = Timer 2 is enabled.

C/$\overline{T2}$ bit 1 — **Counter/Timer Select.** This bit determines whether Timer 2 will function as a timer or counter. Independent of this bit, Timer 2 runs at 2 clocks per tick when used in baud rate generator mode.

0 = Timer 2 functions as a timer. The speed of Timer 2 is determined by the T2M bit (CKCON.5).

1 = Timer 2 will count negative transitions on the T2 pin (P1.0).

CP/$\overline{RL2}$ bit 0 — **Capture/Reload Select.** This bit determines whether the capture or reload function will be used for Timer 2. If either RCLK or TCLK is set, this bit will not function and the timer will function in an auto-reload mode following each overflow.

0 = Auto-reloads will occur when Timer 2 overflows or a falling edge is detected on T2EX if EXEN2 = 1.

1 = Timer 2 captures will occur when a falling edge is detected on T2EX if EXEN2 = 1.

Timer 2 Capture LSB (RCAP2L)

	7	6	5	4	3	2	1	0	Reset Value
SFR CAh									00h

RCAP2L bits 7−0 — **Timer 2 Capture LSB.** This register is used to capture the TL2 value when Timer 2 is configured in capture mode. RCAP2L is also used as the LSB of a 16-bit reload value when Timer 2 is configured in auto-reload mode.

Timer 2 Capture MSB (RCAP2H)

	7	6	5	4	3	2	1	0	Reset Value
SFR CBh									00h

RCAP2H bits 7−0 **Timer 2 Capture MSB.** This register is used to capture the TH2 value when Timer 2 is configured in capture mode. RCAP2H is also used as the MSB of a 16-bit reload value when Timer 2 is configured in auto-reload mode.

Timer 2 LSB (TL2)

	7	6	5	4	3	2	1	0	Reset Value
SFR CCh									00h

TL2 bits 7−0 **Timer 2 LSB.** This register contains the least significant byte of Timer 2.

Timer 2 MSB (TH2)

	7	6	5	4	3	2	1	0	Reset Value
SFR CDh									00h

TH2 bits 7−0 **Timer 2 MSB.** This register contains the most significant byte of Timer 2.

Program Status Word (PSW)

	7	6	5	4	3	2	1	0	Reset Value
SFR D0h	CY	AC	F0	RS1	RS0	OV	F1	P	00h

CY bit 7 **Carry Flag.** This bit is set when the last arithmetic operation resulted in a carry (during addition) or a borrow (during subtraction). Otherwise, it is cleared to ‘0’ by all arithmetic operations.

AC bit 6 **Auxiliary Carry Flag.** This bit is set to ‘1’ if the last arithmetic operation resulted in a carry into (during addition), or a borrow (during subtraction) from the high order nibble. Otherwise, it is cleared to ‘0’ by all arithmetic operations.

F0 bit 5 **User Flag 0.** This is a bit-addressable, general-purpose flag for software control.

RS1, RS0 bits 4−3 **Register Bank Select 1−0.** These bits select which register bank is addressed during register accesses.

RS1	RS0	REGISTER BANK	ADDRESS
0	0	0	00h − 07h
0	1	1	08h − 0Fh
1	0	2	10h − 17h
1	1	3	18h − 1Fh

OV bit 2 **Overflow Flag.** This bit is set to ‘1’ if the last arithmetic operation resulted in a carry (addition), borrow (subtraction), or overflow (multiply or divide). Otherwise, it is cleared to ‘0’ by all arithmetic operations.

F1 bit 1 **User Flag 1.** This is a bit-addressable, general-purpose flag for software control.

P bit 0 **Parity Flag.** This bit is set to ‘1’ if the modulo-2 sum of the 8 bits of the accumulator is 1 (odd parity), and cleared to ‘0’ on even parity.

ADC Offset Calibration Low Byte (OCL)

	7	6	5	4	3	2	1	0	Reset Value
SFR D1h									00h

OCL **ADC Offset Calibration Low Byte.** This is the low byte of the 24-bit word that contains the ADC offset
bits 7−0 calibration. A value that is written to this location will set the ADC offset calibration value.

ADC Offset Calibration Middle Byte (OCM)

	7	6	5	4	3	2	1	0	Reset Value
SFR D2h									00h

OCM **ADC Offset Calibration Middle Byte.** This is the middle byte of the 24-bit word that contains the ADC offset
bits 7−0 calibration. A value that is written to this location will set the ADC offset calibration value.

ADC Offset Calibration High Byte (OCH)

	7	6	5	4	3	2	1	0	Reset Value
SFR D3h									00h

OCH **ADC Offset Calibration High Byte.** This is the high byte of the 24-bit word that contains the ADC offset
bits 7−0 calibration. A value that is written to this location will set the ADC offset calibration value.

ADC Gain Calibration Low Byte (GCL)

	7	6	5	4	3	2	1	0	Reset Value
SFR D4h									5Ah

GCL **ADC Gain Calibration Low Byte.** This is the low byte of the 24-bit word that contains the ADC gain
bits 7−0 calibration. A value that is written to this location will set the ADC gain calibration value.

ADC Gain Calibration Middle Byte (GCM)

	7	6	5	4	3	2	1	0	Reset Value
SFR D5h									ECh

GCM **ADC Gain Calibration Middle Byte.** This is the middle byte of the 24-bit word that contains the ADC gain
bits 7−0 calibration. A value that is written to this location will set the ADC gain calibration value.

ADC Gain Calibration High Byte (GCH)

	7	6	5	4	3	2	1	0	Reset Value
SFR D6h									5Fh

GCH **ADC Gain Calibration High Byte.** This is the high byte of the 24-bit word that contains the ADC gain
bits 7−0 calibration. A value that is written to this location will set the ADC gain calibration value.

ADC Input Multiplexer (ADMUX)

	7	6	5	4	3	2	1	0	Reset Value
SFR D7h	INP3	INP2	INP1	INP0	INN3	INN2	INN1	INN0	01h

INP3−0 bits 7−4 **Input Multiplexer Positive Input.** This selects the positive signal input.

INP3	INP2	INP1	INP0	POSITIVE INPUT
0	0	0	0	AIN0 (default)
0	0	0	1	AIN1
0	0	1	0	AIN2
0	0	1	1	AIN3
0	1	0	0	AIN4
0	1	0	1	AIN5
0	1	1	0	AIN6
0	1	1	1	AIN7
1	0	0	0	AINCOM
1	1	1	1	Temperature Sensor (requires ADMUX = FFh)

INN3−0 bits 3−0 **Input Multiplexer Negative Input.** This selects the negative signal input.

INN3	INN2	INN1	INN0	NEGATIVE INPUT
0	0	0	0	AIN0
0	0	0	1	AIN1 (default)
0	0	1	0	AIN2
0	0	1	1	AIN3
0	1	0	0	AIN4
0	1	0	1	AIN5
0	1	1	0	AIN6
0	1	1	1	AIN7
1	0	0	0	AINCOM
1	1	1	1	Temperature Sensor (requires ADMUX = FFh)

Enable Interrupt Control (EICON)

	7	6	5	4	3	2	1	0	Reset Value
SFR D8h	SMOD1	1	EAI	AI	WDTI	0	0	0	40h

SMOD1 **Serial Port 1 Mode.** When this bit is set the serial baud rate for Port 1 will be doubled.
bit 7 0 = Standard baud rate for Port 1 (default).
1 = Double baud rate for Port 1.

EAI **Enable Auxiliary Interrupt.** The Auxiliary Interrupt accesses nine different interrupts which are masked and
bit 5 identified by SFR registers PAI (SFR A5h), AIE (SFR A6h), and AISTAT (SFR A7h).
0 = Auxiliary Interrupt disabled (default).
1 = Auxiliary Interrupt enabled.

AI **Auxiliary Interrupt Flag.** AI must be cleared by software before exiting the interrupt service routine, after the source
bit 4 of the interrupt is cleared. Otherwise, the interrupt occurs again. Setting AI in software generates an Auxiliary Interrupt, if enabled.
0 = No Auxiliary Interrupt detected (default).
1 = Auxiliary Interrupt detected.

WDTI **Watchdog Timer Interrupt Flag.** WDTI must be cleared by software before exiting the interrupt service routine.
bit 3 Otherwise, the interrupt occurs again. Setting WDTI in software generates a watchdog time interrupt, if enabled. The Watchdog timer can generate an interrupt or reset. The interrupt is available only if the reset action is disabled in HCR0.
0 = No Watchdog Timer Interrupt Detected (default).
1 = Watchdog Timer Interrupt Detected.

ADC Results Low Byte (ADRESL)

	7	6	5	4	3	2	1	0	Reset Value
SFR D9h									00h

ADRESL **The ADC Results Low Byte.** This is the low byte of the 24-bit word that contains the ADC results.
bits 7−0 Reading from this register clears the ADC interrupt; however, AI in EICON (SFR D8) must also be cleared.

ADC Results Middle Byte (ADRESM)

	7	6	5	4	3	2	1	0	Reset Value
SFR DAh									00h

ADRESM **The ADC Results Middle Byte.** This is the middle byte of the 24-bit word that contains the A/D conversion results.
bits 7−0

ADC Results High Byte (ADRESH)

	7	6	5	4	3	2	1	0	Reset Value
SFR DBh									00h

ADRESH **The ADC Results High Byte.** This is the high byte of the 24-bit word that contains the A/D conversion results.
bits 7−0

ADC Control 0 (ADCON0)

	7	6	5	4	3	2	1	0	Reset Value
SFR DCh	REFCLK	BOD	EVREF	VREFH	EBUF	PGA2	PGA1	PGA0	30h

REFCLK bit 7 **Reference Clock.** The reference is specified with a 250kHz clock. The REFCLK should be selected by choosing the appropriate source so that it does not exceed 250kHz.

$$0 = \frac{t_{CLK}}{(ACLK + 1) * 4}$$

$$1 = \frac{USEC}{4}$$

BOD bit 6 **Burnout Detect.** When enabled this connects a positive current source to the positive channel and a negative current source to the negative channel. If the channel is open circuit then the ADC results will be full-scale. Used with Buffer ON.

0 = Burnout Current Sources Off (default).

1 = Burnout Current Sources On.

EVREF bit 5 **Enable Internal Voltage Reference.** If the internal voltage reference is not used, it should be turned off to save power and reduce noise.

0 = Internal Voltage Reference Off.

1 = Internal Voltage Reference On (default). REF IN− should be connected to AGND in this mode. REF IN+ should have a 0.1µF capacitor.

VREFH bit 4 **Voltage Reference High Select.** The internal voltage reference can be selected to be 2.5V or 1.25V.

0 = REFOUT/REF IN+ is 1.25V.

1 = REFOUT/REF IN+ is 2.5V (default).

EBUF bit 3 **Enable Buffer.** Enable the input buffer to provide higher input impedance but limits the input voltage range and dissipates more power.

0 = Buffer disabled (default).

1 = Buffer enabled.

PGA2−0 bits 2−0 **Programmable Gain Amplifier.** Sets the gain for the PGA from 1 to 128.

PGA2	PGA1	PGA0	GAIN
0	0	0	1 (default)
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

ADC Control 1 (ADCON1)

	7	6	5	4	3	2	1	0	Reset Value
SFR DDh	OF_UF	POL	SM1	SM0	—	CAL2	CAL1	CAL0	0000 0000b

OF_UF bit 7 — **Overflow/Underflow.** If this bit is set, the data in the summation register is invalid. Either an overflow or underflow occurred. The bit is cleared by writing a '0' to it.

POL bit 6 — **Polarity.** Polarity of the ADC result and Summation register.
0 = Bipolar.
1 = Unipolar. The LSB size is 1/2 the size of bipolar (twice the resolution).

POL	ANALOG INPUT	DIGITAL OUTPUT
0	+FSR	7FFFFFh
	ZERO	000000h
	−FSR	800000h
1	+FSR	FFFFFFh
	ZERO	000000h
	−FSR	000000h

SM1−0 bits 5−4 — **Settling Mode.** Selects the type of filter or auto-select which defines the digital filter settling characteristics.

SM1	SM0	SETTLING MODE
0	0	Auto
0	1	Fast Settling Filter
1	0	$Sinc^2$ Filter
1	1	$Sinc^3$ Filter

CAL2−0 bits 2−0 — **Calibration Mode Control Bits.**
Writing to these bits initiates the ADC calibration.

CAL2	CAL1	CAL0	CALIBRATION MODE
0	0	0	No Calibration (default)
0	0	1	Self-Calibration, Offset and Gain
0	1	0	Self-Calibration, Offset only
0	1	1	Self-Calibration, Gain only
1	0	0	System Calibration, Offset only
1	0	1	System Calibration, Gain only
1	1	0	Reserved
1	1	1	Reserved

NOTE: Read Value—000b.

ADC Control 2 (ADCON2)

	7	6	5	4	3	2	1	0	Reset Value
SFR DEh	DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0	1Bh

DR7−0 bits 7−0 — **Decimation Ratio LSB.**

ADC Control 3 (ADCON3)

	7	6	5	4	3	2	1	0	Reset Value
SFR DFh	—	—	—	—	—	DR10	DR9	DR8	06h

DR10−8 bits 2−0 — **Decimation Ratio Most Significant 3 Bits.** The ADC output data rate = (ACLK + 1)/64/Decimation Ratio.

Accumulator (A or ACC)

	7	6	5	4	3	2	1	0	Reset Value
SFR E0h	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0	00h

ACC.7−0 **Accumulator.** This register serves as the accumulator for arithmetic and logic operations.
bits 7−0

Summation/Shifter Control (SSCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR E1h	SSCON1	SSCON0	SCNT2	SCNT1	SCNT0	SHF2	SHF1	SHF0	00h

The Summation register is powered down when the ADC is powered down. If all zeroes are written to this register, the 32-bit SUMR3−0 registers will be cleared. The Summation registers will do sign-extend if Bipolar mode is selected in ADCON1.

SSCON1−0 Summation/Shift Count.
bits 7−6

SSCON1	SSCON0	SCNT2	SCNT1	SCNT0	SHF2	SHF1	SHF0	DESCRIPTION
0	0	0	0	0	0	0	0	Clear Summation Register
0	0	0	1	0	0	0	0	CPU Summation on Write to SUMR0 (sum count/shift ignored)
0	0	1	0	0	0	0	0	CPU Subtraction on Write to SUMR0 (sum count/shift ignored)
1	0	x	x	x	Note (1)	Note (1)	Note (1)	CPU Shift only
0	1	Note (1)	Note (1)	Note (1)	x	x	x	ADC Summation only
1	1	Note (1)	Note (1)	Note (1)	Note (1)	Note (1)	Note (1)	ADC Summation completes, then shift completes

(1) Refer to register bit definition.

SCNT2−0 **Summation Count.** When the summation is complete an interrupt will be generated unless masked. Reading the
bits 5−3 SUMR0 register clears the interrupt.

SCNT2	SCNT1	SCNT0	SUMMATION COUNT
0	0	0	2
0	0	1	4
0	1	0	8
0	1	1	16
1	0	0	32
1	0	1	64
1	1	0	128
1	1	1	256

SHF2−0 **Shift Count.**
bits 2−0

SHF2	SHF1	SHF0	SHIFT	DIVIDE
0	0	0	1	2
0	0	1	2	4
0	1	0	3	8
0	1	1	4	16
1	0	0	5	32
1	0	1	6	64
1	1	0	7	128
1	1	1	8	256

Summation 0 (SUMR0)

	7	6	5	4	3	2	1	0	Reset Value
SFR E2h									00h

SUMR0 **Summation 0.** This is the least significant byte of the 32-bit summation register, or bits 0 to 7.
bits 7−0 Write: values in SUMR3−0 are added to the summation register.
Read: clears the Summation Count Interrupt; however, AI in EICON (SFR D8) must also be cleared.

Summation 1 (SUMR1)

	7	6	5	4	3	2	1	0	Reset Value
SFR E3h									00h

SUMR1 **Summation 1.** This is the most significant byte of the lowest 16 bits of the summation register, or bits 8−15.
bits 7−0

Summation 2 (SUMR2)

	7	6	5	4	3	2	1	0	Reset Value
SFR E4h									00h

SUMR2 **Summation 2.** This is the most significant byte of the lowest 24 bits of the summation register, or bits 16−23.
bits 7−0

Summation 3 (SUMR3)

	7	6	5	4	3	2	1	0	Reset Value
SFR E5h									00h

SUMR3 **Summation 3.** This is the most significant byte of the 32-bit summation register, or bits 24−31.
bits 7−0

Offset DAC (ODAC)

	7	6	5	4	3	2	1	0	Reset Value
SFR E6h									00h

ODAC **Offset DAC.** This register will shift the input by up to half of the ADC full-scale input range. The Offset DAC
bits 7−0 value is summed into the ADC prior to conversion. Writing 00h or 80h to ODAC turns off the Offset DAC.. The offset DAC should be cleared prior to calibration, since the offset DAC analog output is applied directly to the ADC input.

bit 7 Offset DAC Sign bit.
0 = Positive
1 = Negative

bit 6−0 $$\text{Offset} = \frac{-V_{REF}}{2 \cdot PGA} \cdot \left(\frac{ODAC[6:0]}{127} \right) \cdot (-1)^{bit7}$$

NOTE: ODAC cannot be used to offset the analog inputs so that the buffer can be used for signals within 50mV of AGND.

Low Voltage Detect Control (LVDCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR E7h	ALVDIS	ALVD2	ALVD1	ALVD0	DLVDIS	DLVD2	DLVD1	DLVD0	00h

ALVDIS **Analog Low Voltage Detect Disable.**

bit 7 0 = Enable Detection of Low Analog Supply Voltage.

1 = Disable Detection of Low Analog Supply Voltage.

ALVD2−0 **Analog Voltage Detection Level.**

bits 6−4

ALVD2	ALVD1	ALVD0	VOLTAGE LEVEL
0	0	0	AV_{DD} 2.7V (default)
0	0	1	AV_{DD} 3.0V
0	1	0	AV_{DD} 3.3V
0	1	1	AV_{DD} 4.0V
1	0	0	AV_{DD} 4.2V
1	0	1	AV_{DD} 4.5V
1	1	0	AV_{DD} 4.7V
1	1	1	External Voltage AIN7 compared to 1.2V

DLVDIS **Digital Low Voltage Detect Disable.**

bit 3 0 = Enable Detection of Low Digital Supply Voltage.

1 = Disable Detection of Low Digital Supply Voltage.

DLVD2−0 **Digital Voltage Detection Level.**

bits 2−0

DLVD2	DLVD1	DLVD0	VOLTAGE LEVEL
0	0	0	DV_{DD} 2.7V (default)
0	0	1	DV_{DD} 3.0V
0	1	0	DV_{DD} 3.3V
0	1	1	DV_{DD} 4.0V
1	0	0	DV_{DD} 4.2V
1	0	1	DV_{DD} 4.5V
1	1	0	DV_{DD} 4.7V
1	1	1	External Voltage AIN6 compared to 1.2V

Extended Interrupt Enable (EIE)

	7	6	5	4	3	2	1	0	Reset Value
SFR E8h	1	1	1	EWDI	EX5	EX4	EX3	EX2	E0h

EWDI bit 4 **Enable Watchdog Interrupt.** This bit enables/disables the watchdog interrupt. The Watchdog timer is enabled by (SFR FFh) and PDCON (SFR F1h) registers.
0 = Disable the Watchdog Interrupt
1 = Enable Interrupt Request Generated by the Watchdog Timer

EX5 bit 3 **External Interrupt 5 Enable.** This bit enables/disables external interrupt 5.
0 = Disable External Interrupt 5
1 = Enable External Interrupt 5

EX4 bit 2 **External Interrupt 4 Enable.** This bit enables/disables external interrupt 4.
0 = Disable External Interrupt 4
1 = Enable External Interrupt 4

EX3 bit 1 **External Interrupt 3 Enable.** This bit enables/disables external interrupt 3.
0 = Disable External Interrupt 3
1 = Enable External Interrupt 3

EX2 bit 0 **External Interrupt 2 Enable.** This bit enables/disables external interrupt 2.
0 = Disable External Interrupt 2
1 = Enable External Interrupt 2

Hardware Product Code 0 (HWPC0)

	7	6	5	4	3	2	1	0	Reset Value
SFR E9h	0	0	0	0	0	1	MEMORY SIZE		0000_01xxb(1)

(1) Applies to MSC1211 and MSC1213 only. Reset value for MSC1212 and MSC1214 is 0000_00xxb.

HWPC0.7−0 bits 7−0 **Hardware Product Code LSB.** Read-only.

MEMORY SIZE		MODEL	FLASH MEMORY
0	0	MSC121xY2	4kB
0	0	MSC121xY3	8kB
1	0	MSC121xY4	16kB
1	1	MSC121xY5	32kB

Hardware Product Code 1 (HWPC1)

	7	6	5	4	3	2	1	0	Reset Value
SFR EAh	0	0	0	0	1	0	0	0	08h(1)

(1) Applies to MSC1211 and MSC1212 only. Reset value for MSC1213 and MSC1214 is 18h.

HWPC1.7−0 bits 7−0 **Hardware Product Code MSB.** Read-only.

Hardware Version (HDWVER)

	7	6	5	4	3	2	1	0	Reset Value
SFR EBh									

Flash Memory Control (FMCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR EEh	0	PGERA	0	FRCM	0	BUSY	SPM	FPM	02h

PGERA **Page Erase.** Available in both user and program modes.
bit 6 0 = Disable Page Erase Mode
1 = Enable Page Erase Mode (automatically set by **page_erase** Boot ROM routine).

FRCM **Frequency Control Mode.**
bit 4 0 = Bypass (default)
1 = Use Delay Line. Recommended for saving power.

BUSY **Write/Erase BUSY Signal.**
bit 2 0 = Idle or Available
1 = Busy

SPM **Serial/Parallel Programming Mode.** Read-only.
bit 1 0 = Indicates the device is in parallel programming mode.
1 = Indicates the device is in serial programming mode (if FPM also = 1).

FPM **Flash Programming Mode.** Read-only.
bit 0 0 = Indicates the device is operating in UAM.
1 = Indicates the device is operating in programming mode.

Flash Memory Timing Control (FTCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR EFh	FER3	FER2	FER1	FER0	FWR3	FWR2	FWR1	FWR0	A5h

Refer to *Flash Memory Characteristics*

FER3−0 **Set Erase.** Flash Erase Time = (1 + FER) • (MSEC + 1) • t_{CLK}. This can be broken into multiple shorter erase times.
bits 7−4 For more Information, see Application Report SBAA137, *Incremental Flash Memory Page Erase*, available for download from www.ti.com.
Industrial temperature range: 10ms
Commercial temperature range: 4ms

FWR3−0 **Set Write.** Set Flash Write Time = (1 + FWR) • (USEC + 1) • 5 • t_{CLK}. Total writing time will be longer. For more
bits 3−0 Information, see Application Report SBAA087, *In-Application Flash Programming*, available for download from www.ti.com.
Range: 30µs to 40µs.

B Register (B)

	7	6	5	4	3	2	1	0	Reset Value
SFR F0h	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0	00h

B.7−0 **B Register.** This register serves as a second accumulator for certain arithmetic operations.
bits 7−0

Power-Down Control (PDCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR F1h	0	PDDAC	PDI2C	PDPWM	PDADC	PDWDT	PDST	PDSPI	7Fh

Turning peripheral modules off puts the MSC1211/12/13/14 in the lowest power mode.

PDDAC **DAC Module Control.**
bit 6 0 = DACs On
1 = DACs Power Down

PDI2C **I2C Control (MSC1211 and MSC1213 only).**
bit 5 0 = I^2C On (the state is undefined if PDSPI is also = 0)
1 = I^2C Power Down

PDPWM **Pulse Width Module Control.**
bit 4 0 = PWM On
1 = PWM Power Down

PDADC **ADC Control.**
bit 3 0 = ADC On
1 = ADC, V_{REF}, and Summation registers are powered down.

PDWDT **Watchdog Timer Control.**
bit 2 0 = Watchdog Timer On
1 = Watchdog Timer Power Down

PDST **System Timer Control.**
bit 1 0 = System Timer On
1 = System Timer Power Down

PDSPI **SPI System Control.**
bit 0 0 = SPI System On (the state is undefined if PDI2C is also = 0)
1 = SPI System Power Down

$\overline{\text{PSEN}}$/ALE Select (PASEL)

	7	6	5	4	3	2	1	0	Reset Value
SFR F2h	0	0	PSEN2	PSEN1	PSEN0	0	ALE1	ALE0	00h

PSEN2−0 **$\overline{\text{PSEN}}$ Mode Select.**
bits 5−3

PSEN2	PSEN1	PSEN0	
0	0	X	$\overline{\text{PSEN}}$
0	1	X	CLK
1	0	X	ADC MODCLK
1	1	0	Low
1	1	1	High

ALE1−0 **ALE Mode Select.**
bits 1−0

ALE1	ALE0	
0	X	ALE
1	0	Low
1	1	High

NOTE: X = don't care.

Analog Clock (ACLK)

	7	6	5	4	3	2	1	0	Reset Value
SFR F6h	0	FREQ6	FREQ5	FREQ4	FREQ3	FREQ2	FREQ1	FREQ0	03h

FREQ6−0 **Clock Frequency Selection.** This value + 1 divides the system clock to create the ACLK frequency.

bit 6−0

$$\text{ACLK frequency} = \frac{f_{CLK}}{\text{FREQ} + 1}$$

$$f_{MOD} = \frac{f_{CLK}}{(\text{ACLK} + 1) * 64}$$

$$\text{Data Rate} = \frac{f_{MOD}}{\text{Decimation}}$$

System Reset (SRST)

	7	6	5	4	3	2	1	0	Reset Value
SFR F7h	0	0	0	0	0	0	0	RSTREQ	00h

RSTREQ **Reset Request.** Setting this bit to ‘1’ and then clearing to ‘0’ will generate a system reset.
bit 0

Extended Interrupt Priority (EIP)

	7	6	5	4	3	2	1	0	Reset Value
SFR F8h	1	1	1	PWDI	PX5	PX4	PX3	PX2	E0h

PWDI **Watchdog Interrupt Priority.** This bit controls the priority of the watchdog interrupt.
bit 4
0 = The watchdog interrupt is low priority.
1 = The watchdog interrupt is high priority.

PX5 **External Interrupt 5 Priority.** This bit controls the priority of external interrupt 5.
bit 3
0 = External interrupt 5 is low priority.
1 = External interrupt 5 is high priority.

PX4 **External Interrupt 4 Priority.** This bit controls the priority of external interrupt 4.
bit 2
0 = External interrupt 4 is low priority.
1 = External interrupt 4 is high priority.

PX3 **External Interrupt 3 Priority.** This bit controls the priority of external interrupt 3.
bit 1
0 = External interrupt 3 is low priority.
1 = External interrupt 3 is high priority.

PX2 **External Interrupt 2 Priority.** This bit controls the priority of external interrupt 2.
bit 0
0 = External interrupt 2 is low priority.
1 = External interrupt 2 is high priority.

Seconds Timer Interrupt (SECINT)

	7	6	5	4	3	2	1	0	Reset Value
SFR F9h	WRT	SECINT6	SECINT5	SECINT4	SECINT3	SECINT2	SECINT1	SECINT0	7Fh

This system clock is divided by the value of the 16-bit register MSECH:MSECL. Then, that 1ms timer tick is divided by the register HMSEC which provides the 100ms signal used by this seconds timer. Therefore, this seconds timer can generate an interrupt which occurs from 100ms to 12.8 seconds. Reading this register will clear the Seconds Interrupt; however, AI in EICON (SFR D8h) must also be cleared. This Interrupt can be monitored in the AIE or AIPOL registers.

WRT **Write Control.** Determines whether to write the value immediately or wait until the current count is finished.
bit 7 Read = 0.
0 = Delay Write Operation. The SEC value is loaded when the current count expires.
1 = Write Immediately. The counter is loaded once the CPU completes the write operation.

SECINT6−0 **Seconds Count.** Normal operation would use 100ms as the clock interval.
bits 6−0 Seconds Interrupt = (1 + SEC) • (HMSEC + 1) • (MSEC + 1) • t_{CLK}.

Milliseconds Timer Interrupt (MSINT)

	7	6	5	4	3	2	1	0	Reset Value
SFR FAh	WRT	MSINT6	MSINT5	MSINT4	MSINT3	MSINT2	MSINT1	MSINT0	7Fh

The clock used for this timer is the 1ms clock, which results from dividing the system clock by the values in registers MSECH:MSECL. Reading this register is necessary for clearing the interrupt; however, AI in EICON (SFR D8h) must also be cleared.

WRT **Write Control.** Determines whether to write the value immediately or wait until the current count is finished. Read = 0.
bit 7 0 = Delay Write Operation. The MSINT value is loaded when the current count expires.
1 = Write Immediately. The MSINT counter is loaded once the CPU completes the write operation.

MSINT6−0 **Milliseconds Count.** Normal operation would use 1ms as the clock interval.
bits 6−0 MS Interrupt Interval = (1 + MSINT) • (MSEC + 1) • t_{CLK}

One Microsecond Timer (USEC)

	7	6	5	4	3	2	1	0	Reset Value
SFR FBh	0	0	FREQ5	FREQ4	FREQ3	FREQ2	FREQ1	FREQ0	03h

FREQ5−0 **Clock Frequency − 1.** This value + 1 divides the system clock to create a 1µs Clock.
bits 5−0 USEC = CLK/(FREQ + 1). This clock is used to set Flash write time. See FTCON (SFR EFh).

One Millisecond Timer Low Byte (MSECL)

	7	6	5	4	3	2	1	0	Reset Value
SFR FCh	MSECL7	MSECL6	MSECL5	MSECL4	MSECL3	MSECL2	MSECL1	MSECL0	9Fh

MSECL7−0 **One Millisecond Timer Low Byte.** This value in combination with the next register is used to create a 1ms clock.
bits 7−0 1ms = (MSECH • 256 + MSECL + 1) • t_{CLK}. This clock is used to set Flash erase time. See FTCON (SFR EFh).

One Millisecond Timer High Byte (MSECH)

	7	6	5	4	3	2	1	0	Reset Value
SFR FDh	MSECH7	MSECH6	MSECH5	MSECH4	MSECH3	MSECH2	MSECH1	MSECH0	0Fh

MSECH7−0 **One Millisecond Timer High Byte.** This value in combination with the previous register is used to create a 1ms clock.
bits 7−0 1ms = (MSECH • 256 + MSECL + 1) • t_{CLK}.

One Hundred Millisecond Timer (HMSEC)

	7	6	5	4	3	2	1	0	Reset Value
SFR FEh	WRT	HMSEC6	HMSEC5	HMSEC4	HMSEC3	HMSEC2	HMSEC1	HMSEC0	63h

WRT **Write Control.** Determines whether to write the value immediately or wait until the current count is finished. Read = 0.
bit 7 0 = Delay Write Operation. The MSINT value is loaded when the current count expires.
1 = Write Immediately. The MSINT counter is loaded once the CPU completes the write operation.

HMSEC6−0 **One Hundred Millisecond.** This clock divides the 1ms clock to create a 100ms clock.
bits 6−0 100ms = (MSECH • 256 + MSECL + 1) • (HMSEC + 1) • t_{CLK}.

Watchdog Timer (WDTCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR FFh	EWDT	DWDT	RWDT	WDCNT4	WDCNT3	WDCNT2	WDCNT1	WDCNT0	00h

EWDT **Enable Watchdog (R/W).**
bit 7 Write 1/Write 0 sequence sets the Watchdog Enable Counting bit.

DWDT **Disable Watchdog (R/W).**
bit 6 Write 1/Write 0 sequence clears the Watchdog Enable Counting bit.

RWDT **Reset Watchdog (R/W).**
bit 5 Write 1/Write 0 sequence restarts the Watchdog Counter.

WDCNT4−0 **Watchdog Count (R/W).**
bits 4−0 Watchdog expires in (WDCNT + 1) • HMSEC to (WDCNT + 2) • HMSEC, if the sequence is not asserted. There is an uncertainty of 1 count.

Revision History

DATE	REV	PAGE	SECTION	DESCRIPTION
10/07	G	29	Voltage Reference	Added paragraph to end of section.
7/06	F	32	Brownout Reset	Added paragraph on BOR voltage calibration.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSC1211Y2PAGT	ACTIVE	TQFP	PAG	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	-40 to 125	MSC1211Y2	Samples
MSC1211Y3PAGT	ACTIVE	TQFP	PAG	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	-40 to 125	MSC1211Y3	Samples
MSC1211Y4PAGT	ACTIVE	TQFP	PAG	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	-40 to 125	MSC1211Y4	Samples
MSC1211Y4PAGTG4	ACTIVE	TQFP	PAG	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	-40 to 125	MSC1211Y4	Samples
MSC1211Y5PAGR	ACTIVE	TQFP	PAG	64	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	-40 to 125	MSC1211Y5	Samples
MSC1211Y5PAGT	ACTIVE	TQFP	PAG	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	-40 to 125	MSC1211Y5	Samples
MSC1212Y2PAGT	OBSOLETE	TQFP	PAG	64		TBD	Call TI	Call TI	-40 to 125	MSC1212Y2	
MSC1212Y2PAGTG4	OBSOLETE	TQFP	PAG	64		TBD	Call TI	Call TI	-40 to 125		
MSC1212Y3PAGT	ACTIVE	TQFP	PAG	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	-40 to 125	MSC1212Y3	Samples
MSC1212Y3PAGTG4	ACTIVE	TQFP	PAG	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	-40 to 125	MSC1212Y3	Samples
MSC1212Y4PAGT	ACTIVE	TQFP	PAG	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	-40 to 125	MSC1212Y4	Samples
MSC1212Y5PAGT	ACTIVE	TQFP	PAG	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	-40 to 125	MSC1212Y5	Samples
MSC1213Y2PAGT	ACTIVE	TQFP	PAG	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	-40 to 125	MSC1213Y2	Samples
MSC1213Y3PAGT	ACTIVE	TQFP	PAG	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	-40 to 125	MSC1213Y3	Samples
MSC1213Y4PAGT	ACTIVE	TQFP	PAG	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	-40 to 125	MSC1213Y4	Samples
MSC1213Y5PAGR	ACTIVE	TQFP	PAG	64	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	-40 to 125	MSC1213Y5	Samples
MSC1213Y5PAGT	ACTIVE	TQFP	PAG	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	-40 to 125	MSC1213Y5	Samples
MSC1213Y5PAGTG4	ACTIVE	TQFP	PAG	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	-40 to 125	MSC1213Y5	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSC1214Y3PAGT	ACTIVE	TQFP	PAG	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	-40 to 125	MSC1214Y3	Samples
MSC1214Y4PAGT	ACTIVE	TQFP	PAG	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	-40 to 125	MSC1214Y4	Samples
MSC1214Y5PAGR	ACTIVE	TQFP	PAG	64	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	-40 to 125	MSC1214Y5	Samples
MSC1214Y5PAGT	ACTIVE	TQFP	PAG	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	-40 to 125	MSC1214Y5	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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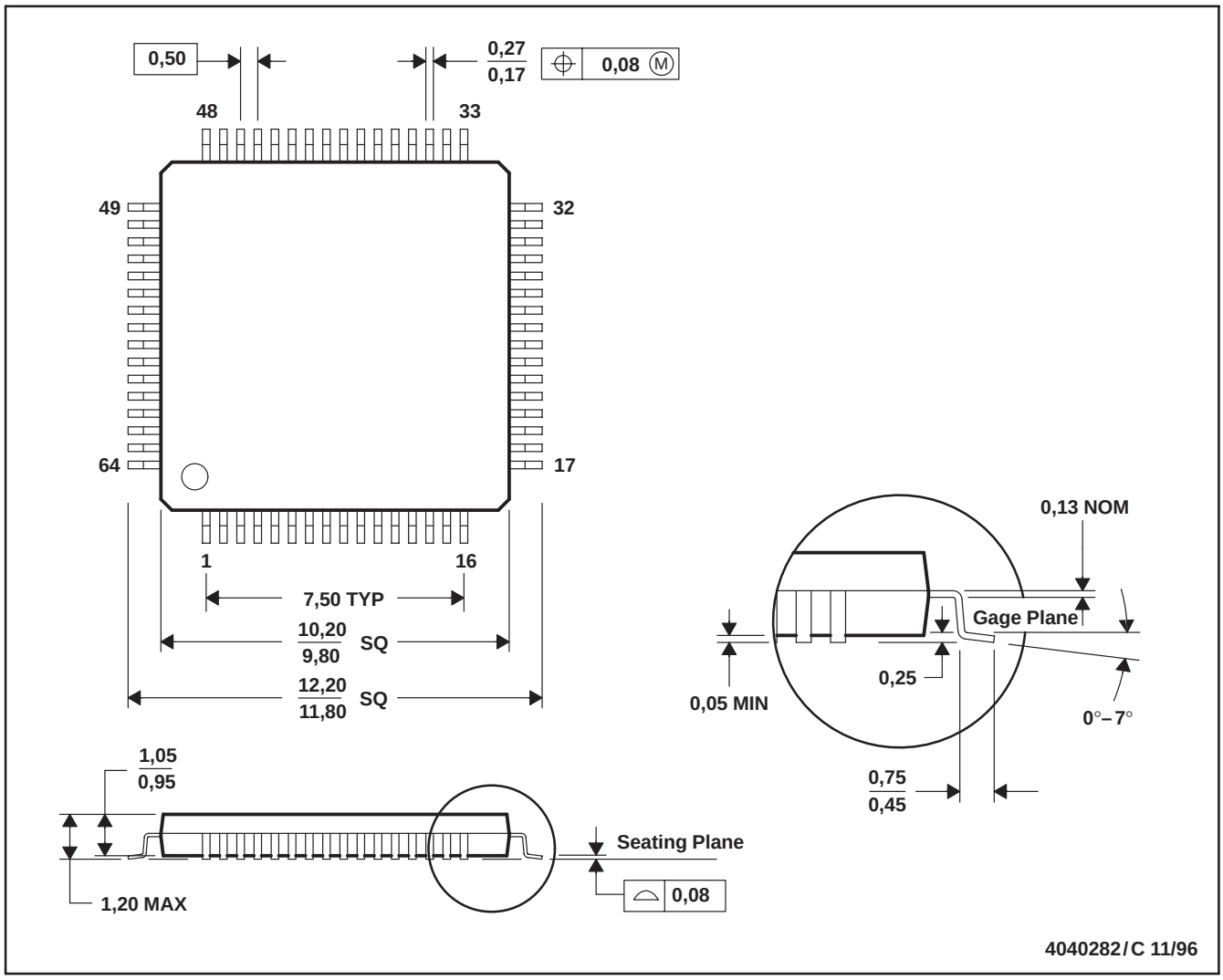
PAG (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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