MPQ8861

18V, 12A, High-Efficiency, Wide-Input, Synchronous, Step-Down Converter with Integrated Telemetry via I²C Interface for Automotive, AEC-Q100 Qualified

PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

DESCRIPTION

The MPQ8861 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with an I²C control interface. The MPQ8861 offers a fully integrated solution that achieves 12A of continuous current with excellent load and line regulation over a wide input supply range.

The output voltage level can be controlled on-the-fly through an I²C serial interface. The reference voltage range can be adjusted from 0.6V to 1.108V in 4mV steps. The voltage slew rate, frequency, current limit, hiccup/latch-off protection, enable, and power-saving mode are also selectable through the I²C interface.

Constant-on-time (COT) control operation provides fast transient response. An open-drain power good (PG) pin indicates when the output voltage is in the nominal range. Full protection features include over-voltage protection (OVP), over-current protection (OCP), and thermal shutdown.

The MPQ8861 is available in a QFN-14 (3mmx4mm) package with Wettable Flanks.

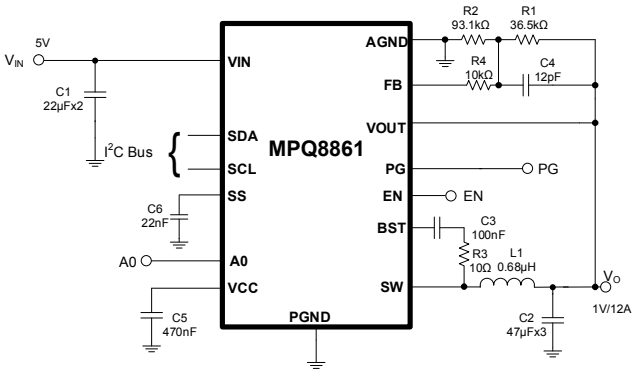
FEATURES

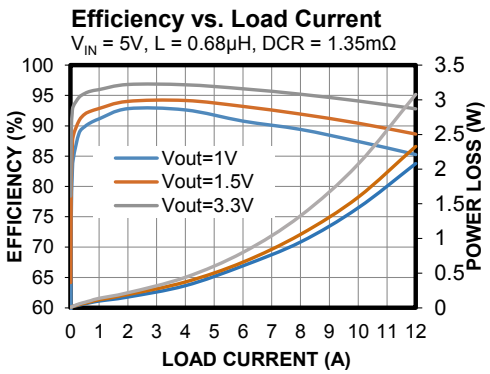
- 0.6V to 5.5V Output Voltage Range
- 2.9V to 18V Input Voltage Range
- 12A DC Output Current
- 1% Internal Reference Accuracy
- Supports dynamic Reference adjust in 4mV steps with slew rate control
- Selectable PFM/PWM Mode, Adjustable Frequency and Current Limit through I²C
- Four Different Selectable I²C Addresses
- Power Good Indication Output
- OVP, OCP and Thermal Shutdown Protection
- QFN-14(3mmx4mm) Package with Wettable Flanks
- AECQ-100 Grade 1 Qualified

APPLICATIONS

- Automotive Systems
- Industrial Systems

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MPQ8861GLE-AEC1	QFN-14 (3mmx4mm)	*See Below*	1

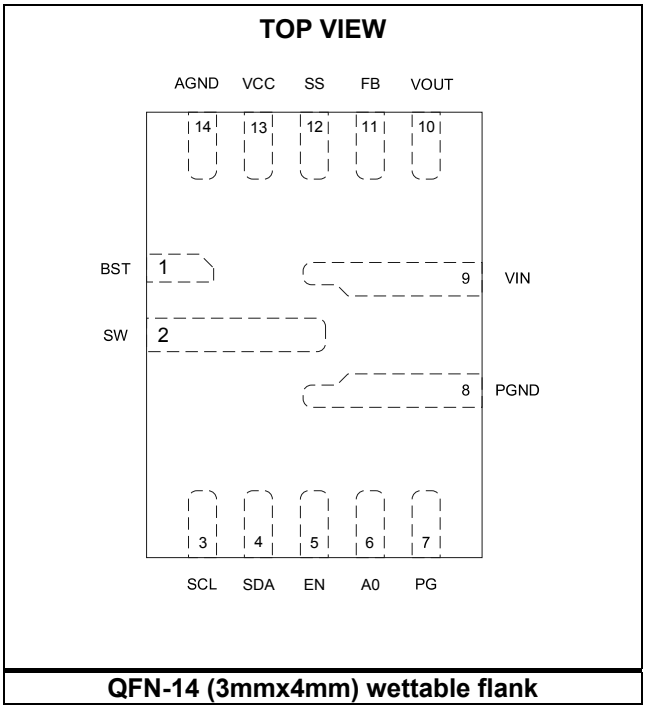
* For Tape & Reel, add suffix –Z (e.g. MPQ8861GLE-AEC1–Z)

TOP MARKING

MPYW
8861
LLL
E

MP: MPS prefix
Y: Year code
W: Week code
8861: First four digits of the part number
LLL: Lot number
E: Wettable flank

PACKAGE REFERENCE



QFN-14 (3mmx4mm) wettable flank

PIN FUNCTIONS

QFN-14 Pin#	Name	Description
1	BST	**Bootstrap.** A capacitor is required between SW and BST to form a floating supply across the high-side switch driver.
2	SW	**Switch output.** Connect SW using a wide PCB trace.
3	SCL	**I²C serial clock.**
4	SDA	**I²C serial data.**
5	EN	**Enable.** Drive EN high to enable the MPQ8861. EN has a 1.5MΩ internal pull-down resistor to GND. EN is a high-voltage pin, so it can be connected to VIN directly for auto start-up.
6	A0	**I²C address set-up.** Connect a resistor divider from VCC to A0 to set different I²C addresses.
7	PG	**Power good indication.** PG is an open-drain structure. PG is de-asserted if the output voltage is out of the regulation window.
8	PGND	**System power ground.** PGND is the reference ground of the regulated output voltage. PGND requires special consideration during the PCB layout. Connect PGND to the ground plane with copper traces and vias.
9	VIN	**Supply voltage.** The MPQ8861 operates from a 2.9V to 18V input rail. Decouple the input rail with a ceramic capacitor. Connect VIN using a wide PCB trace.
10	VOUT	**Output voltage sense.** Connect VOUT to the positive terminal of the load.
11	FB	**Feedback.** Connect FB to the tap of an external resistor divider from the output to GND to set the output voltage.
12	SS	**Soft-start set-up.** Connect a capacitor from SS to ground to set the soft-start time.
13	VCC	**Internal LDO regulator output.** Decouple VCC with a 0.47µF capacitor.
14	AGND	**Analog ground.** Connects to PGND through low impedance routing or ground plane.

ABSOLUTE MAXIMUM RATINGS (1)

VIN ..... -0.3V to 19V
V_{SW} ..... -0.6V (-7V for <10ns) to VIN + 0.7V (25V for <25ns)
V_{BST} ..... V_{SW} + 4V
V_{EN} 18V
VOUT 7V
All other pins ..... -0.3V to 4V
Continuous power dissipation (T_A = +25°C) (2) (6)
QFN-14 (3mmx4mm)……..3.91W
Junction temperature .....thermal shutdown
Lead temperature..... 260°C
Storage temperature .....-65°C to 150°C

ESD Rating (3)

All pins (HBM).....……±2kV
All pins (CDM).....±2kV

Recommended Operating Conditions (4)

Supply voltage (VIN)..... 2.9V to 18V
Output voltage (VOUT)..... 0.6V to 5.5V
Operating junction temp. (T_J)..... -40°C to thermal shutdown

Thermal Resistance θ_{JA} θ_{JC}

QFN-14 (3mmx4mm)		
EVQ8861-LE-00A(5)	29	3°C/W
JESD51-7(6)	48	11°C/W

Notes:

1) Absolute maximum ratings are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) HBM, per JEDEC specification JESD22-A114; CDM, per JEDEC specification JESD22-C101. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on a 4-layer PCB (85.5mmx63.5mm).
6) Measured on JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C, typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN} = 0V		2.1	8	μA
Supply current (quiescent)	I_q	No switching, FB = 105% V_{REF}, PFM mode		420	620	μA
EN rising threshold	V_{EN_RISING}		1.1	1.2	1.3	V
EN threshold hysteresis	V_{EN_HYS}			110		mV
EN to GND pull-down resistor	R_{EN}		1.1	1.5	1.9	MΩ
VCC voltage	V_{CC}	I_{CC} =0- 20mA	-5%	3.53	+5%	V
VIN under-voltage lockout threshold rising	$INUV_{Vth\_r}$		2.45	2.65	2.85	V
VIN under-voltage lockout threshold Falling	$INUV_{Vth\_f}$		2.3	2.5	2.7	V
HS switch on resistance	$HS_{RDS(ON)}$	$V_{BST - SW}$ = 3.3V		15	30	mΩ
LS switch on resistance	$LS_{RDS(ON)}$	VCC = 3.3V		4.5	10	mΩ
Switch leakage	SW_{LKG1}	V_{EN} = 0V, V_{SW} = 18V, T_J = +25°C			1	μA
	SW_{LKG2}	V_{EN} = 0V, V_{SW} = 18V, T_J = +125°C			14	μA
Low-side valley current limit	I_{LIMIT_L}	D[2:0]=010		14		A
Low-side negative current limit	I_{LIMIT_LN}	In forced PWM mode or OVP state		-3.5	-2	A
Switching frequency	f_{SW1}	VIN = 12V, VOUT = 1V, T_J = +25°C		500		kHz
	f_{SW2}	VIN = 12V, VOUT = 5V, T_J = +25°C		500		kHz
Maximum Duty Cycle	D_{MAX}			95		%
Minimum off time (7)	T_{OFF_MIN}			185		ns
Minimum on time (7)	T_{ON_MIN}	VOUT = 0.6V		50		ns
Reference voltage	V_{ref}	T_J = +25°C	-1%	720	+1%	mV
Power good UV threshold rising	PGVth-Hi	Good	0.86	0.9	0.94	V_{REF}
Power good UV threshold falling	PGVth-Lo	Fault	0.81	0.85	0.89	V_{REF}
Power good OV threshold rising	PGVth-Hi	Fault	1.11	1.15	1.19	V_{REF}
Power good OV threshold falling	PGVth-Lo	Good	1.01	1.05	1.09	V_{REF}
Power good deglitch time	PGTd	I²C programmable	20	30	45	μs
Power good sink current capability	V_{PG}	Sink 1mA			0.2	V
V_{OUT} OVP rising threshold	V_{OVP_Rise}		121%	125%	129%	V_{REF}
V_{OUT} OVP falling threshold	$V_{OVP\_Falling}$		106%	110%	114%	V_{REF}
V_{OUT} OVP delay	T_{OVP}		2.3	5.3	8.3	μs
Output pin absolute OV	V_{OVP2}		6	6.5	7	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
V_{OUT} UVP threshold	$V_{FB\_UV\_th}$	Hiccup entry	55%	60%	65%	V_{REF}
Soft-start current	I_{SS}		4	7	10	μA
Thermal shutdown (7)	T_{TSD}			150		°C
Thermal hysteresis (7)	T_{TSD_HYS}			20		°C
I²C Specification						
I²C Slave Address 1	ADD_1	A0 pin float		61H		
I²C Slave Address 2	ADD_2	Resistance Accuracy=1%, R_{A0_up} = 100kΩ, R_{A0_down} = 60.4kΩ		63H		
I²C Slave Address 3	ADD_3	Resistance Accuracy=1%, R_{A0_up} = 60.4kΩ, R_{A0_down} = 100kΩ		65H		
I²C Slave Address 4	ADD_4	R_{A0_up} = 100kΩ		67H		
A0 to GND pull-down resistor	R_{A0_PD}		1.5	2	2.5	MΩ
Input logic high	V_{IH}	I²C pull-up VDD can be 1.8V to 3.6V	1.4			V
Input logic low	V_{IL}				0.4	V
Output voltage logic low	V_{OUT_L}				0.4	V
SCL clock frequency	f_{SCL}			400	1000	kHz
SCL high time	t_{HIGH}		60			ns
SCL low time	t_{LOW}		160			ns
Data set-up time	$t_{SU.DAT}$		10			ns
Data hold time	$t_{HD.DAT}$		0	60		ns
Set-up time for (repeated) start condition	$t_{SU.STA}$		160			ns
Hold time for (repeated) start condition	$t_{HD.STA}$		160			ns
Bus free time between a start and a stop condition	t_{BUF}		160			ns
Set-up time for stop condition	$T_{SU.STO}$		160			ns
Rise time of SCL and SDA	t_R		10		300	ns
Fall time of SCL and SDA	t_F		10		300	ns
Pulse width of suppressed spike	t_{SP}		0		50	ns
Capacitance for each bus line	C_B				400	pF

Note:

7) Guaranteed by engineering sample characterization.

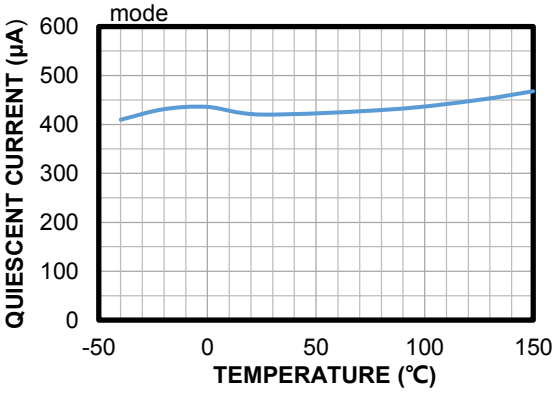
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board.

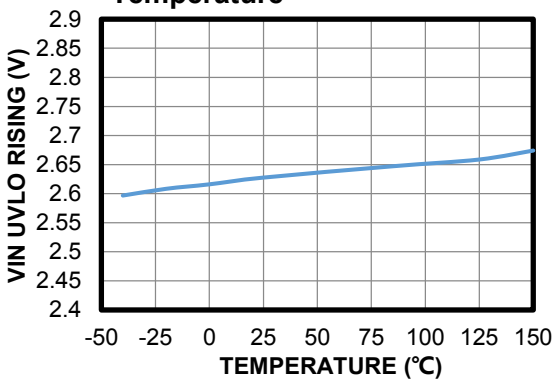
V_{IN} = 5V, V_{OUT} = 1V, L = 0.68µH, F_S = 500kHz, auto PFM/PWM mode, T_A = 25°C, unless otherwise noted.

Quiescent Current vs. Temperature

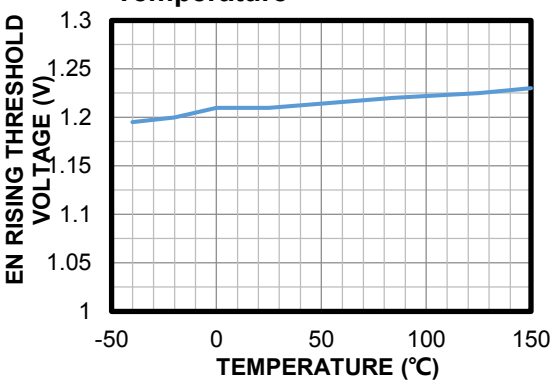
No switching, FB = 105% VREF, PFM mode



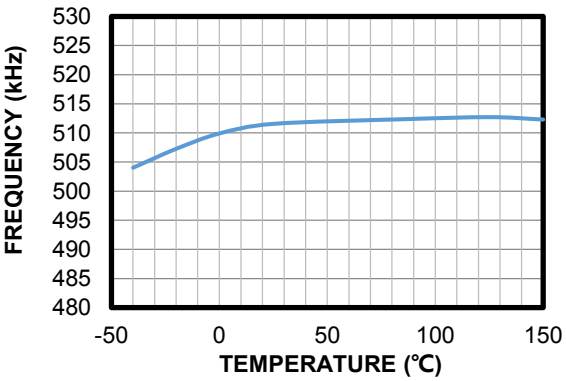
VIN UVLO Rising vs. Temperature



EN Rising Threshold Voltage vs. Temperature

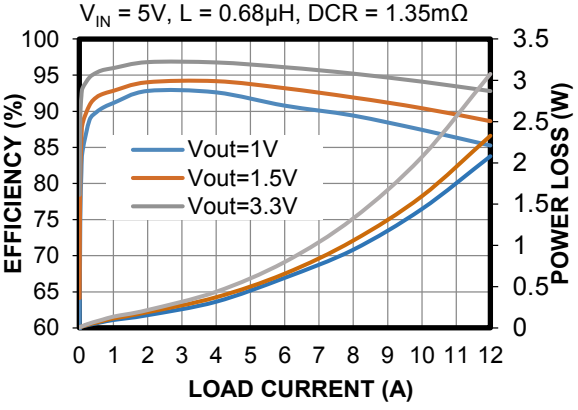


Frequency vs. Temperature



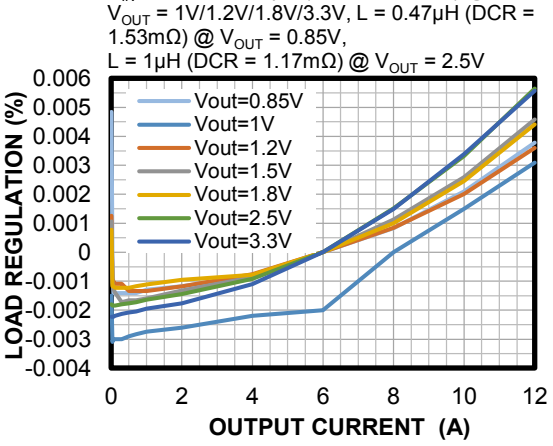
Efficiency vs. Load Current

V_{IN} = 5V, L = 0.68µH, DCR = 1.35mΩ



Load Regulaiton vs. Load Current

V_{IN} = 5V, L = 0.68µH (DCR = 1.35mΩ) @ V_{OUT} = 1V/1.2V/1.8V/3.3V, L = 0.47µH (DCR = 1.53mΩ) @ V_{OUT} = 0.85V,
L = 1µH (DCR = 1.17mΩ) @ V_{OUT} = 2.5V



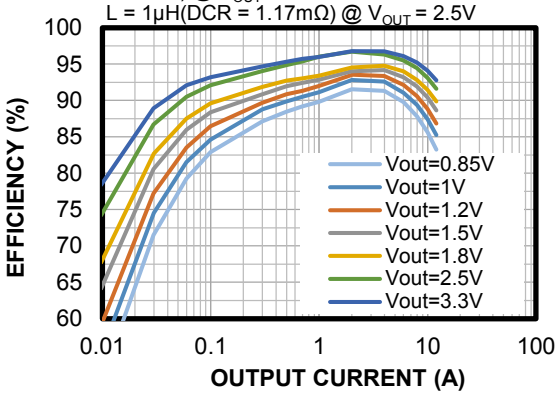
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board.

V_{IN} = 5V, V_{OUT} = 1V, L = 0.68µH, F_S = 500kHz, auto PFM/PWM mode, T_A = 25°C, unless otherwise noted.

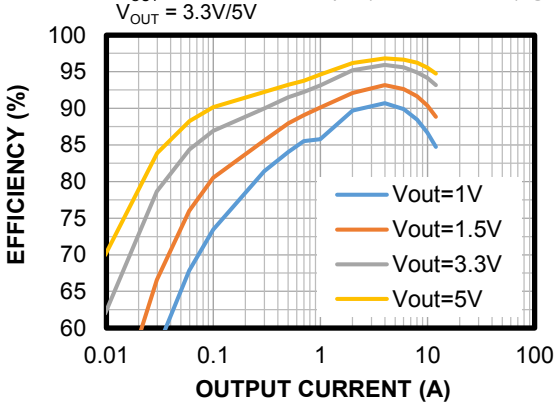
Efficiency vs. Load Current

V_{IN} = 5V, L = 0.68µH (DCR = 1.35mΩ) @ V_{OUT} = 1V/1.2V/1.8V/3.3V, L = 0.47µH (DCR = 1.53mΩ) @ V_{OUT} = 0.85V, L = 1µH(DCR = 1.17mΩ) @ V_{OUT} = 2.5V



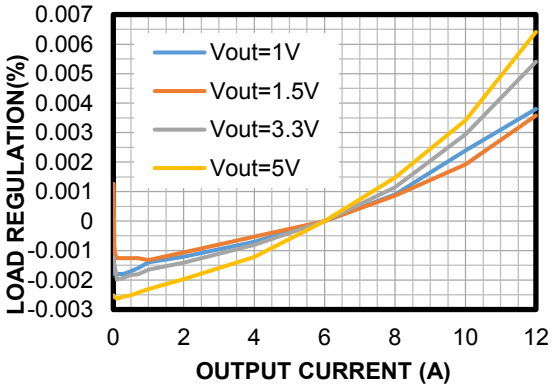
Efficiency vs. Load Current

V_{IN} = 12V, L = 1µH (DCR=1.17mΩ) @ V_{OUT} = 1V/1.5V, L = 2.2µH (DCR = 3.05mΩ) @ V_{OUT} = 3.3V/5V



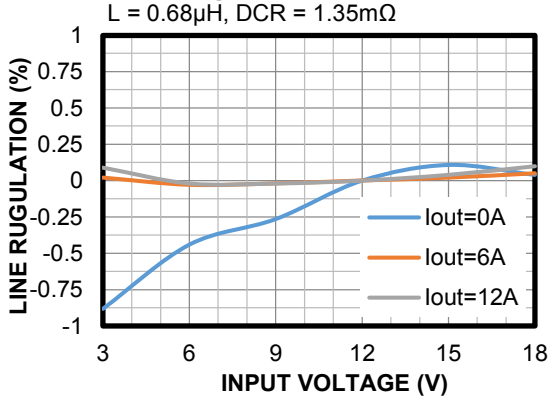
Load Regulation vs. Load Current

V_{IN} = 12V, L = 1µH (DCR = 1.17mΩ) @ V_{OUT} = 1V/1.5V, L = 2.2µH (DCR = 3.05mΩ) @ V_{OUT} = 3.3V/5V



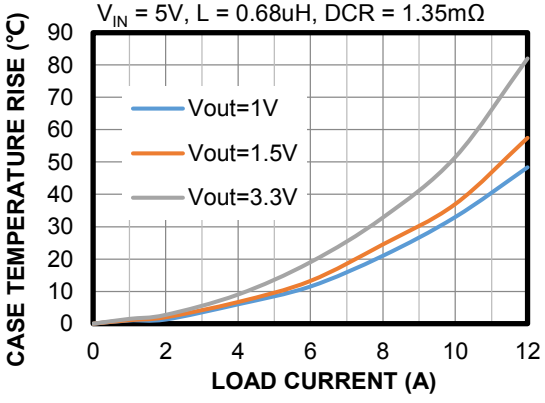
Line Regulation vs. Load Current

L = 0.68µH, DCR = 1.35mΩ



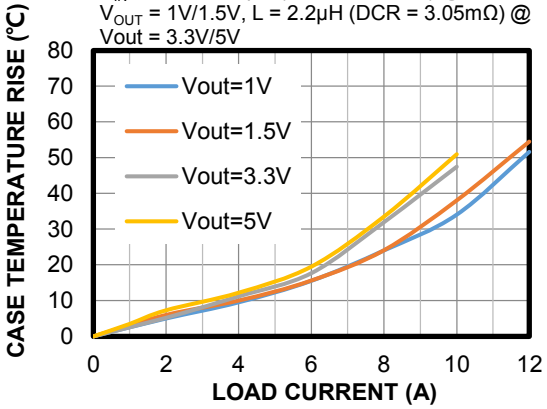
Case Temperature Rise vs. Load Current

V_{IN} = 5V, L = 0.68uH, DCR = 1.35mΩ



Case Temperature Rise vs. Load Current

V_{IN} = 12V, L = 1µH (DCR = 1.35mΩ) @ V_{OUT} = 1V/1.5V, L = 2.2µH (DCR = 3.05mΩ) @ Vout = 3.3V/5V



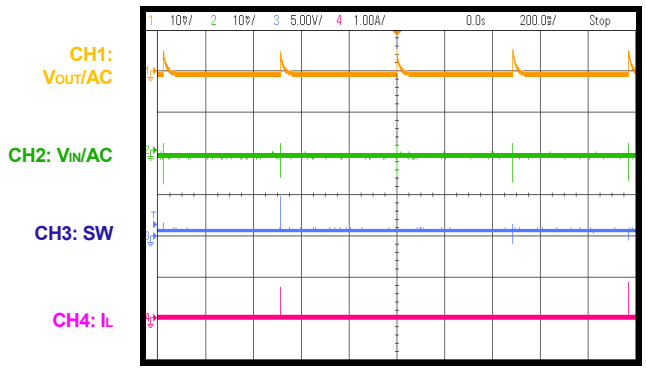
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board.

V_{IN} = 5V, V_{OUT} = 1V, L = 0.68µH, F_S = 500kHz, auto PFM/PWM mode, T_A = 25°C, unless otherwise noted.

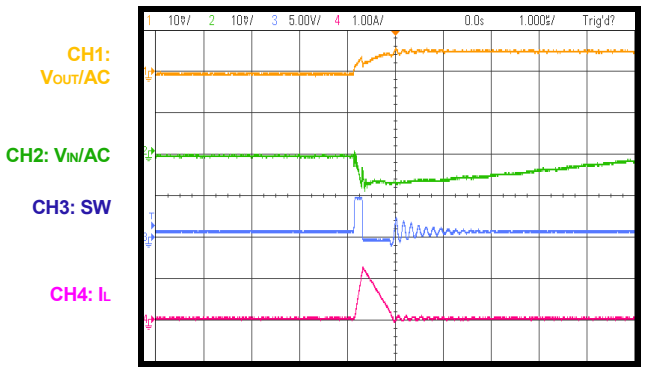
Steady state

Auto PFM/PWM mode, I_{OUT} = 0A



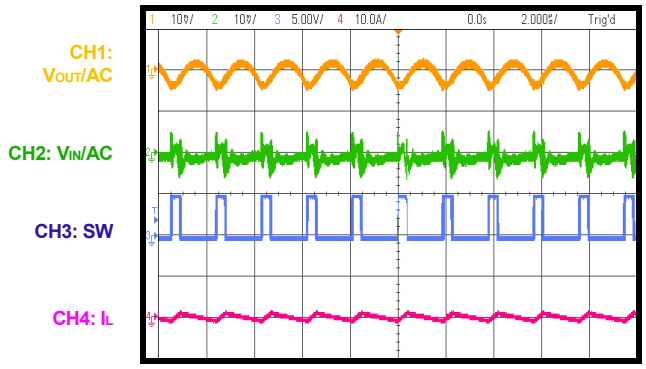
Steady state

Auto PFM/PWM mode, I_{OUT} = 0A



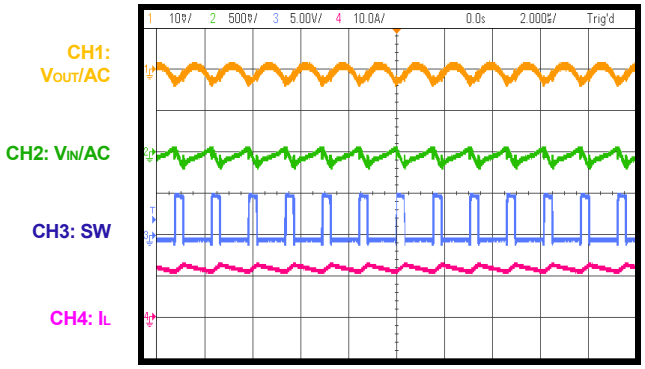
Steady state

Forced PWM Mode, I_{OUT} = 0A



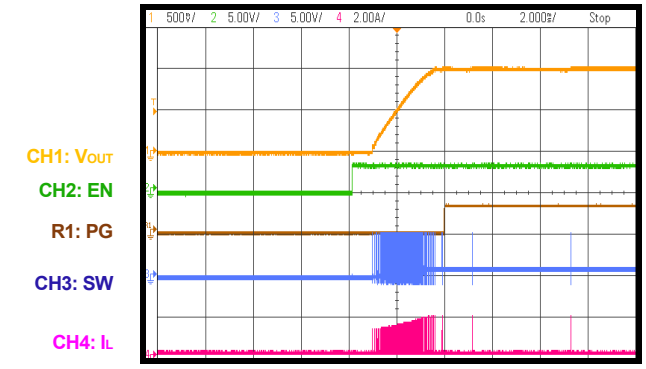
Steady state

I_{OUT} = 12A



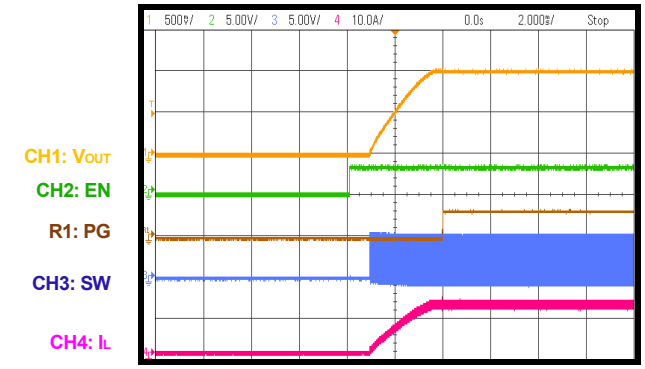
EN Start-Up

I_{OUT} = 0A



EN Start-Up

I_{OUT} = 12A

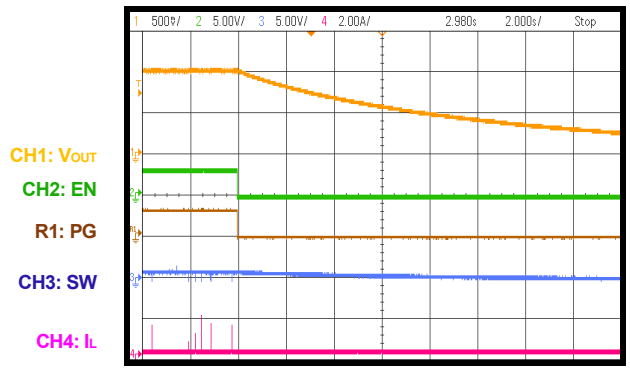


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

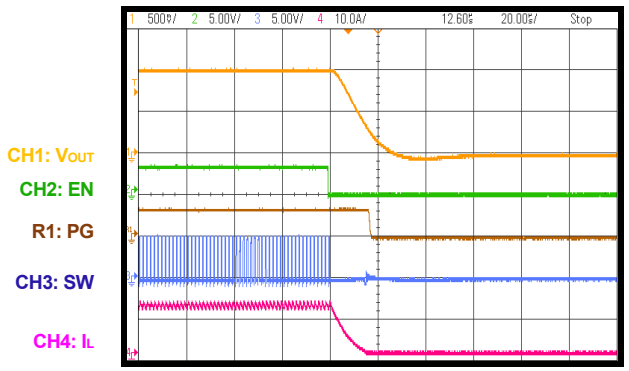
Performance waveforms are tested on the evaluation board.

V_{IN} = 5V, V_{OUT} = 1V, L = 0.68µH, F_S = 500kHz, auto PFM/PWM mode, T_A = 25°C, unless otherwise noted.

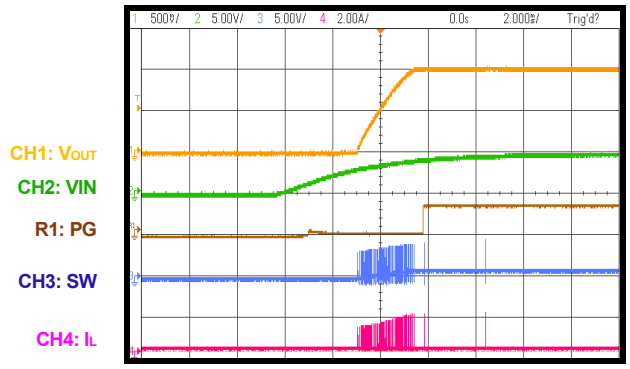
EN Shutdown
I_{OUT} = 0A



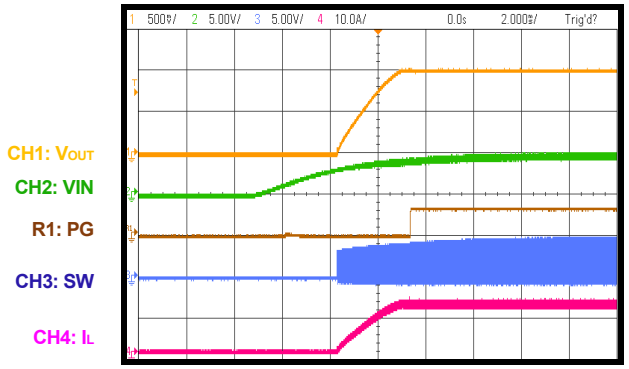
EN Shutdown
I_{OUT} = 12A



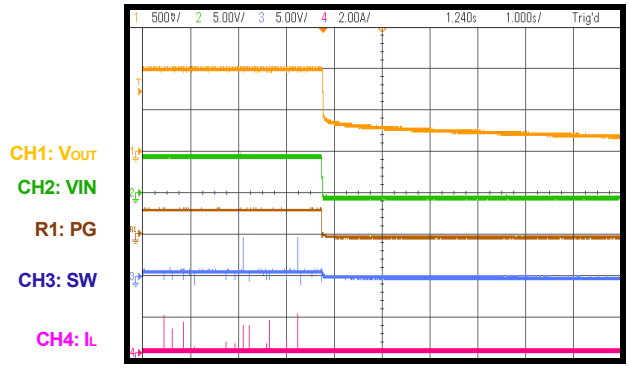
Power Start-Up
I_{OUT} = 0A



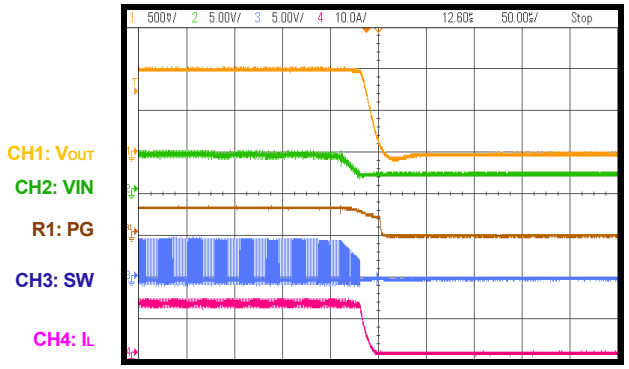
Power Start-Up
I_{OUT} = 12A



Power Shutdown
I_{OUT} = 0A



Power Shutdown
I_{OUT} = 12A



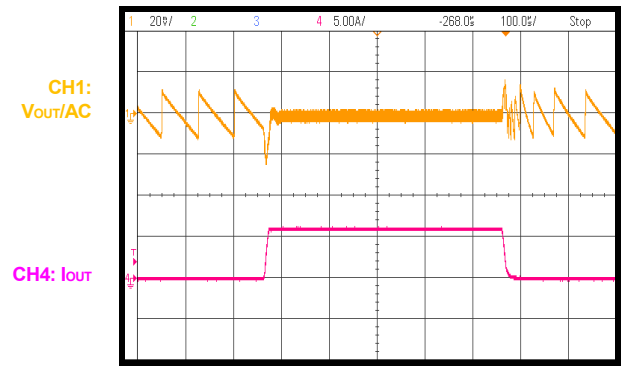
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board.

V_{IN} = 5V, V_{OUT} = 1V, L = 0.68µH, F_S = 500kHz, auto PFM/PWM mode, T_A = 25°C, unless otherwise noted.

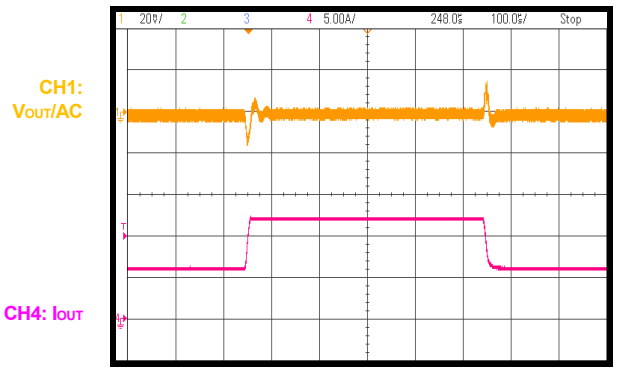
Load Transient

I_{OUT} = 0A to 6A, slew rate = 0.6A/µs



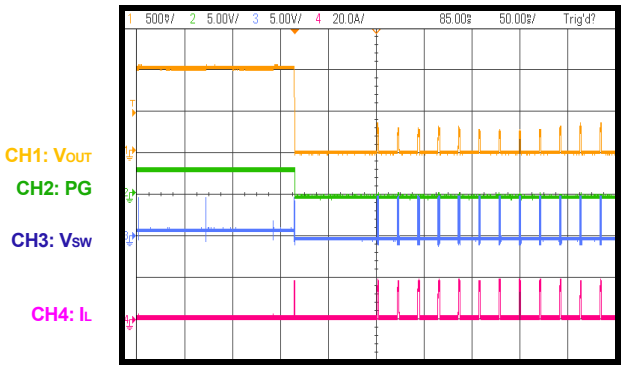
Load Transient

I_{OUT} = 6A to 12A, slew rate = 0.6A/µs



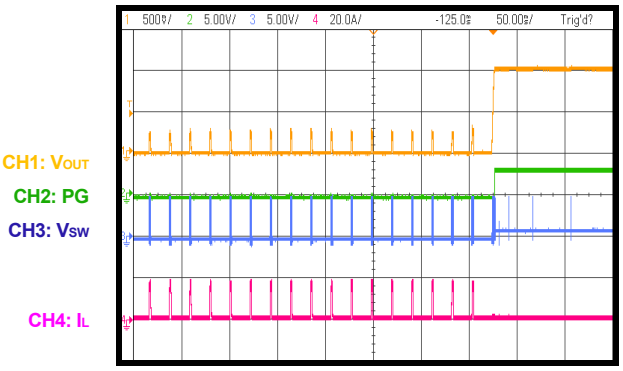
SCP Entry, Hiccup Mode

I_{OUT} = 0A



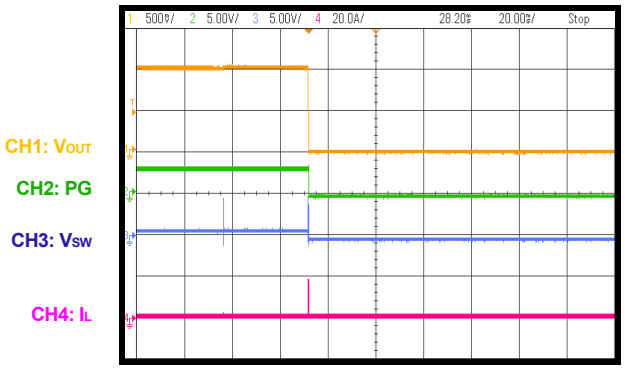
SCP Recovery, Hiccup Mode

I_{OUT} = 0A



SCP Entry, Latch Off Mode

I_{OUT} = 0A



Thermal Image

V_{IN} = 5V, V_{OUT} = 1V, I_{OUT} = 12A, Measured on 4-layer PCB, Size: 85.5mm*63.5mm, Top/Bottom Layer: 2Oz, Middle Layer 1/2: 1Oz, T_A = 25°C

BLOCK DIAGRAM

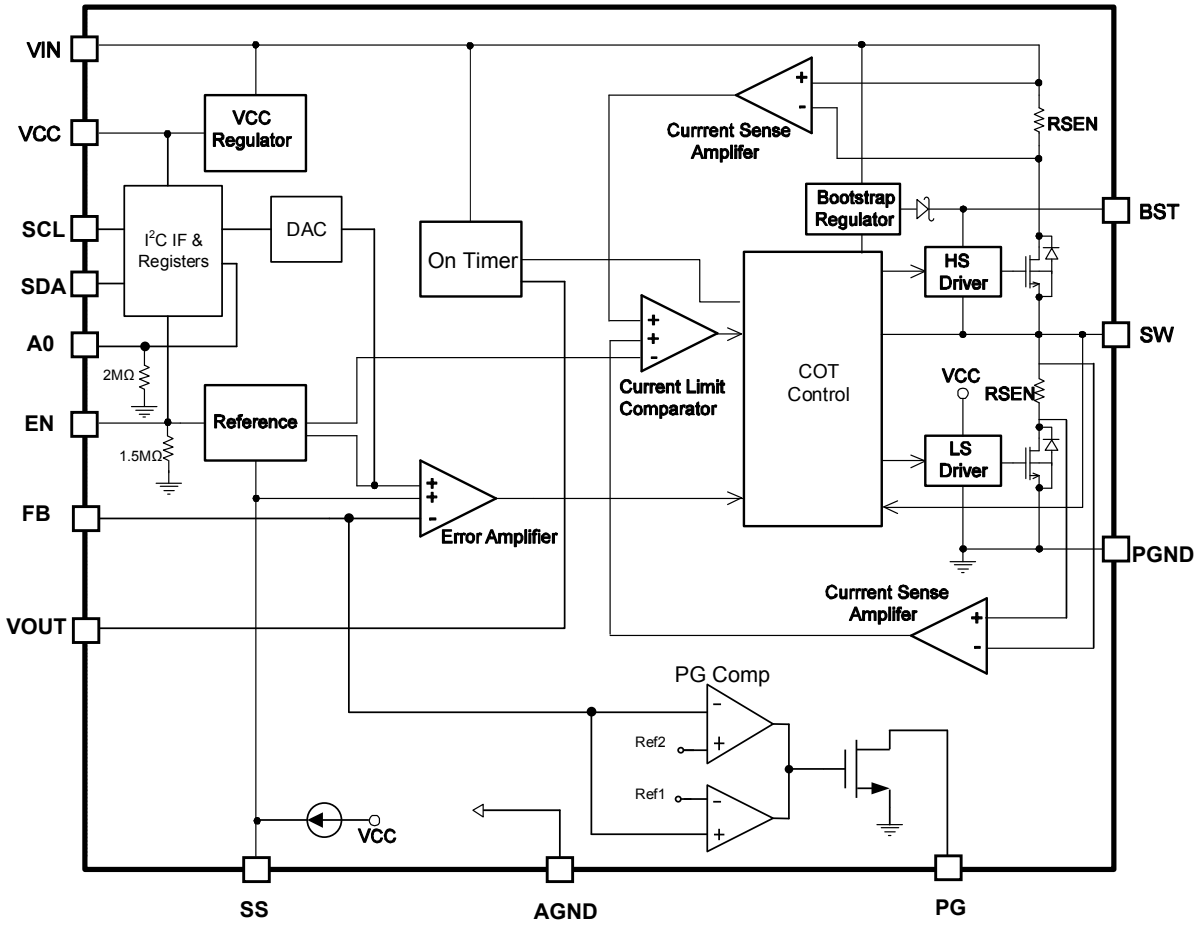


Figure 1: Functional Block Diagram

OPERATION

Pulse-Width Modulation (PWM) Operation

The MPQ8861 is a fully integrated, synchronous, rectified, step-down, switch-mode converter. The MPQ8861 uses constant-on-time (COT) control to provide fast transient response and ease loop stabilization. Figure 2 shows the simplified ramp compensation block.

At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on whenever the ramp voltage (V_{Ramp}) is below the error amplifier output voltage (V_{EAO}), which indicates an insufficient output voltage. The on period is determined by both the output voltage and input voltage to make the switching frequency fairly constant over the input voltage range.

After the on period elapses, the HS-FET enters the off state. By cycling the HS-FET between the on and off states, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is in its off state to minimize conduction loss.

Shoot-through occurs when both the HS-FET and LS-FET are on at the same time, causing a dead short between input and GND, reducing efficiency dramatically. The MPQ8861 prevents shoot-through by generating a dead-time (DT) internally between the HS-FET off and LS-FET on period and the LS-FET off and HS-FET on period. The MPQ8861 enters either heavy-load operation or light-load operation depending on the amplitude of the output current.

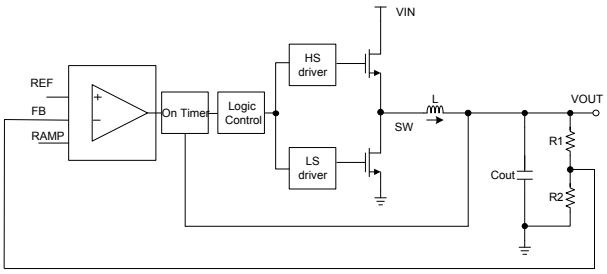


Figure 2: Simplified Compensation Block

Switching Frequency

The MPQ8861 uses constant-on-time (COT) control, and there is no dedicated oscillator in the IC. The input voltage is fed into the one-shot on-timer through the internal frequency resistor. The duty ratio is VOUT/VIN, and the switching frequency is fairly constant over the input voltage range.

The MPQ8861's switching frequency can be adjusted by setting the two bits D[5:4] in register 0x02 through I²C communication. When the output voltage setting is low and the input voltage is high, the switching on-time may be limited by the internal minimum on-time limit, and switching frequency decreases. Table 1 shows the maximum switching frequency vs. the output voltage when VIN = 12V and VIN = 5V.

Table 1: Maximum Frequency Selecting vs. Output Voltage

	Maximum Frequency Selecting	
Vo (V)	VIN = 12V	VIN = 5V
5	1.25MHz	/
3.3	1.25MHz	1.25MHz
2.5	1.25MHz	1.25MHz
1.8	1.25MHz	1.25MHz
1.5	1.25MHz	1.25MHz
1.2	1MHz	1.25MHz
1	750kHz	1.25MHz
0.9	750kHz	1.25MHz
0.6	500kHz	1.25MHz

Forced PWM Operation

When the MPQ8861 works in forced pulse-width modulation (PWM) mode, the MPQ8861 enters continuous conduction mode (CCM), where the HS-FET and LS-FET repeat the on/off operation, even if the inductor current is zero or a negative value. The switching frequency (f_{SW}) is fairly constant (see Figure 3).

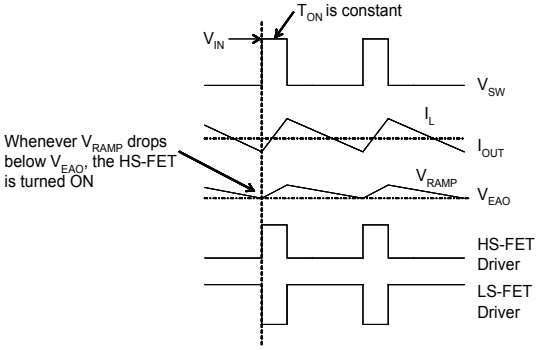


Figure 3: Forced PWM Operation

Light-Load Operation

When the MPQ8861 works in auto-PWM, auto-pulse-frequency modulation (PFM) mode, or

light-load operation, the MPQ8861 reduces the switching frequency automatically to maintain high efficiency, and the inductor current drops almost to zero. When the inductor current reaches zero, the LS-FET driver goes into tri-state (Hi-Z) (see Figure 4). The output capacitors discharge slowly to GND through R1 and R2. This operation improves device efficiency greatly when the output current is low.

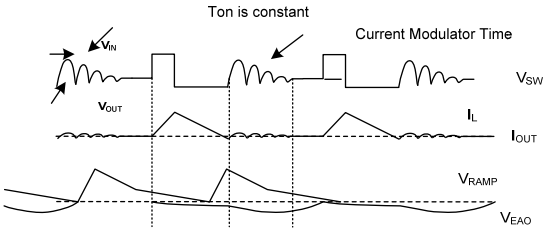


Figure 4: Light-Load Operation

Light-load operation is also called skip mode since the HS-FET does not turn on as frequently as it does during heavy-load condition. The frequency at which the HS-FET turns on is a function of the output current. As the output current increases, the current modulator regulation time period becomes shorter, the HS-FET turns on more frequently, and the switching frequency increases. The output current reaches critical levels when the current modulator time is zero and can be determined with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (1)$$

The MPQ8861 reverts to PWM mode once the output current exceeds the critical level. The switching frequency then remains fairly constant over the output current range.

The MPQ8861 can operate in PFM mode under light load to improve efficiency (low-power mode). The MPQ8861 can also operate in forced PWM mode at any load condition. This mode is selectable through the I²C control. To enable low-power mode, set the mode bit to 0. To disable low-power mode, set the mode bit to 1, and the converter will work in forced PWM mode. The mode bit is set to 0 (PFM) by default.

Operating without an External Ramp

The traditional COT control scheme is intrinsically unstable if the output capacitor's ESR is not large enough to be an effective current-sense resistor. Ceramic capacitors cannot be used as output capacitors, typically. The MPQ8861 has built-in, internal ramp compensation to ensure that the system is stable, even without the help of the output capacitor's ESR. The pure ceramic capacitor solution can reduce the output ripple, total BOM cost, and board area significantly.

VCC Regulator

A 3.5V internal regulator powers most of the internal circuitries. A 0.47uF decoupling capacitor is needed to stabilize the regulator and reduce ripple. This regulator takes the VIN input and operates in the full VIN range. After EN is pulled high and VIN is greater than 3.5V, the output of the regulator is in full regulation. When VIN is lower than 3.5V, the output voltage decreases and follows the input voltage. A 0.47µF ceramic capacitor is required for decoupling.

Enable (EN)

EN is a digital control pin that turns the regulator, including the I²C block, on and off. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. An internal 1.5MΩ resistor is connected from EN to ground. EN can operate with an 18V input voltage, which allows EN to be connected to VIN directly for automatic start-up. When the external EN is high, set the EN bit to 0 in register 0x01 to stop the HS-FET and LS-FET from switching. The MPQ8861 resumes switching by setting the EN bit to 1.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MPQ8861 UVLO comparator monitors the input voltage, VIN, and output voltage of the VCC regulator. The MPQ8861 is active when the voltages exceed the UVLO rising threshold.

Soft-Start (SS) and Pre-Bias Start-Up

Soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start current to charge the SS capacitor from 0V to VCC. When SS is lower than REF, the error amplifier uses SS as the

reference. When SS is higher than REF, the error amplifier uses REF as the reference.

The approximate typical soft-start time can be calculated with Equation (2):

$$t_{ss}(ms) = \frac{V_{ref}(V) \times C_{ss}(nF)}{7\mu A} \quad (2)$$

Where V_{ref} is reference voltage.

If the output of the MPQ8861 is pre-biased to a certain voltage during start-up, the IC disables the switching of both the HS-FET and LS-FET until the voltage on the internal SS capacitor exceeds the sensed output voltage at FB.

The MPQ8861 also provides a selectable soft-stop function which defines the output discharge behavior after an EN shutdown. By default, the output is not controlled after EN shutdown. If setting the soft-stop control bit D[3] to 1 in register 0x02 via the I²C, the output is discharged linearly to zero in a quarter of the soft-start time.

Over-Current Protection (OCP)

The MPQ8861 has a default, hiccup, cycle-by-cycle, over-current limiting control. The current-limit circuit employs both a high-side current limit and a low-side valley current-sensing algorithm. The MPQ8861 uses the $R_{DS(ON)}$ of the LS-FET as a current-sensing element for the valley current limit. If the magnitude of the high-side current-sense signal is above the current-limit threshold, the PWM on pulse is terminated, and the LS-FET is turned on. Afterward, the inductor current is monitored by the voltage between GND and SW. GND is used as the positive current sensing node, so GND should be connected to the source terminal of the bottom MOSFET. PWM is not allowed to initiate a new cycle before the inductor current falls to the valley threshold.

After the cycle-by-cycle over-current limit occurs, the output voltage drops until VOUT is below the under-voltage (UV) threshold (typically 60% below the reference). Once UV is triggered, the MPQ8861 enters hiccup mode to restart the part periodically. This protection mode is especially useful when the output is dead shorted to ground. The average short-circuit current is reduced greatly to alleviate thermal issues and protect the regulator. The MPQ8861 exits hiccup mode once the over-current condition is removed.

Short the output to ground first, and then power on the part. The MPQ8861's I²C is disabled in this condition. The I²C resumes operation after the short circuit is removed. When the hiccup over-current protection (OCP) bit D[1] in register 0x01 is set to 0 by the I²C, a latch-off occurs if OCP is triggered, and FB under-voltage protection (UVP) is triggered.

Power Good (PG)

The power good (PG) pin indicates whether the output voltage is in the normal range compared to the internal reference voltage. PG is an open-drain structure. An external pull-up supply is required. During power-up, the PG output is pulled low. This indicates to the system to remain off and keep the load on the output to a minimum. This helps reduce in-rush current at start-up.

When the output voltage is higher than 90% and lower than 115% of the internal reference voltage, and the soft start is finished, then the PG signal is pulled high. When the output voltage is lower than 85% after the soft start finishes, the PG signal remains low. When the output voltage is higher than 115% of the internal reference, PG is switched low. The PG signal rises back to high after the output voltage drops below 105% of the internal reference voltage.

PG implements an adjustable deglitch time via the I²C whenever VOUT crosses the under-voltage and over-voltage (UV, OV) rising and falling threshold. This guarantees the correct indication when the output voltage is scaled through the I²C.

The PG output is pulled low immediately when EN UVLO, input UVLO, OCP, or over-temperature protection (OTP) are triggered.

Input Over-Voltage Protection (VIN OVP)

The MPQ8861 monitors VIN to detect an input over-voltage event. This function is active only when the output is in OV or a soft-stop condition. When the output is in the over-voltage protection (OVP) state or soft stop is enabled, output discharge is enabled to charge the input voltage high. When the input voltage

exceeds the input OVP threshold (typically 18V), both the HS-FET and LS-FET stop switching.

Output Over-Voltage Protection (OVP)

The MPQ8861 monitors both FB and VOUT to detect an over-voltage event. When the FB voltage becomes higher than 125% of the internal reference voltage, an internal comparator monitors FB, and the controller enters dynamic regulation mode. The input voltage may be charged up during this time. When input OVP is triggered, the IC stops switching. If OVP mode is set to auto retry in the I²C, the IC begins switching once the input voltage drops below the VIN OVP recover threshold. Otherwise, the MPQ8861 latches off. OVP auto-retry mode or latch-off mode occurs only if the soft start has finished.

Dynamic regulation mode can be operated by turning on the low side until the low-side negative current limit is triggered. Then the body diode of the HS-FET free-wheels the current.

The output power charges the input, which may trigger the VIN OVP function. In VIN OVP, neither the HS-FET or LS-FET turn on and stop charging VIN. If the output is still over-voltage and the input voltage drops below the VIN OVP threshold, repeat the operation. If the output voltage is below 110% of the internal reference voltage, then output OVP is exited.

Output Absolute Over-Voltage Protection (OVP_ABS)

The MPQ8861's VOUT can be adjusted by the feedback reference voltage and the external resistor dividers. But MPQ8861's output voltage must be set lower than the absolute OVP threshold (typically 6.5V).

The MPQ8861 monitors VOUT to detect absolute OVP. When VOUT is larger than 6.5V, the controller enters dynamic regulation mode (For details, please see the description in the above Output Over-Voltage Protection). If the OVP retry bit is set to 1 in the I²C register 0x01. Otherwise, the MPQ8861 latches off when output OVP and input OVP are both triggered. Absolute OVP works once both the input voltage and EN are higher than their rising thresholds. This means that this function can work even during a soft start.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die reaches temperatures that exceed 160°C, the entire chip shuts down. When the temperature is less than its lower threshold (typically 140°C), the chip is enabled again.

The D[1] and D[2] bits can be monitored in register 0x06 for more information about the IC silicon temperature.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.4V with a 150mV hysteresis. The bootstrap capacitor voltage is regulated by VIN internally through D1, M1, C4, L1, and C2 (see Figure 5). If V_{BST} - V_{SW} exceeds 3.3V, U1 regulates M1 to maintain a 3.3V BST voltage across C4.

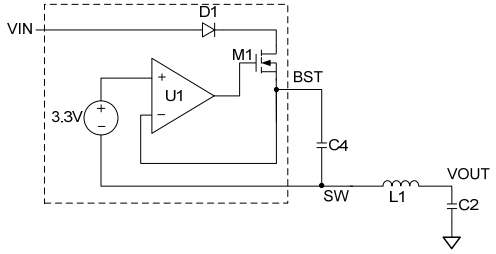


Figure 5: Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If VIN, VCC, and EN exceed their respective thresholds, the chip starts up. The reference block starts first, generating stable reference voltages and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Several events can shut down the chip: EN low, VIN low, VCC low, thermal shutdown, OVP latch, and OCP latch. In the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. VEAO and the internal supply rail are then pulled down.

I²C Control and Default Output Voltage

When the MPQ8861 is enabled, the output voltage is determined by the FB resistors with a programmed soft-start time. After that, the I²C

bus can communicate with the master. If the chip does not receive an I²C communication signal continuously, it can work well through FB and perform behavior similar to a traditional non-I²C part. The output voltage is determined by the resistor dividers R1, R2, and FB reference voltage. V_{OUT} can be calculated using Equation (3):

$$V_{OUT} = V_{REF} \times (\frac{R1+R2}{R2}) \quad (3)$$

Note that the output voltage cannot be set higher than an absolute OVP threshold (typically 6.5V).

I²C Slave Address

To support multiple devices used on the same I²C bus, A0 can be used to select four different addresses. A resistor divider from VCC to GND can achieve an accurate reference voltage. Connect A0 to this reference voltage to set a different I²C slave address (see Figure 6). The internal circuit changes the I²C address accordingly. When the master sends an 8-bit address value, the 7-bit I²C address should be followed by 0/1 to indicate a write/read operation. Table 2 shows the recommended I²C address selection by the A0 voltage.

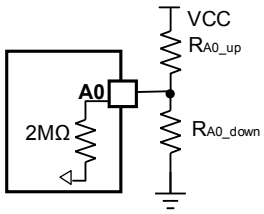


Figure 6: I²C Slave Address Selection Set-Up

Table 2: Recommended I²C Slave Address Selection by A0 Resistor Divider

A0 Upper Resistor R_{A0_up}(kΩ)	A0 Lower Resistor R_{A0_down}(kΩ)	I²C Slave Address	
		Binary	Hex
No connect	No connect	110 0001	61H
100	60.4	110 0011	63H
60.4	100	110 0101	65H
100	No connect	110 0111	67H

I²C INTERFACE

I²C Serial Interface Description

The I²C is a 2-wire, bidirectional, serial interface consisting of a data line (SDA) and a clock line (SCL). The lines are pulled to a bus voltage externally when they are idle. When connecting to the line, a master device generates the SCL signal and device address and arranges the communication sequence. The MPQ8861 interface is an I²C slave. The I²C interface adds flexibility to the power supply solution. The output voltage, transition slew rate, and other parameters can be controlled by the I²C interface instantaneously.

Data Validity

One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is low (see Figure 7).

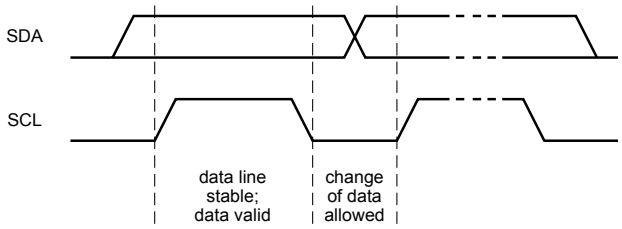


Figure 7: Bit Transfer on the I²C Bus

Start and stop are signaled by the master device, which signifies the beginning and the end of the I²C transfer. The start condition is defined as the SDA signal transitioning from high to low while the SCL is high. The stop condition is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 8).

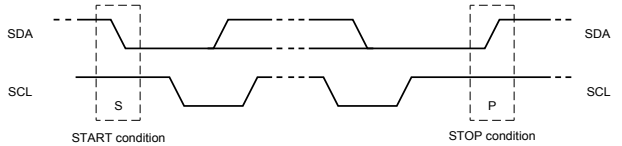


Figure 8: Start and Stop Conditions

Start (S) and stop (P) conditions are always generated by the master. The bus is considered to be busy after the start condition and is considered to be free again after a minimum of 4.7µs after the stop condition. The bus remains busy if a repeated start (Sr) is generated instead of a stop condition. The start and repeated start conditions are identical functionally.

Transfer Data

Every byte put on the SDA line must be eight bits long. Each byte must be followed by an acknowledge bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains at stable low during the high period of this clock pulse.

Data transfers follow the format shown in Figure 9. After the start condition, a slave address is sent. This address is seven bits long followed by an eighth bit data direction bit (r/w). A zero indicates a transmission (write), and a one indicates a request for data (read). A data transfer is always terminated by a stop condition generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated start condition and address another slave without first generating a stop condition.

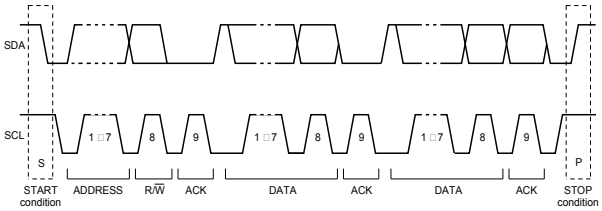
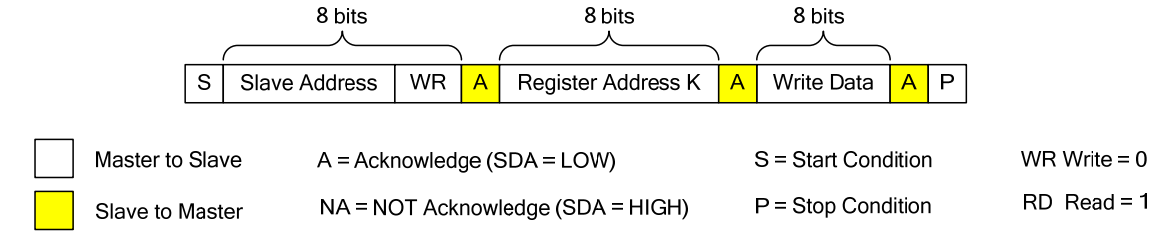


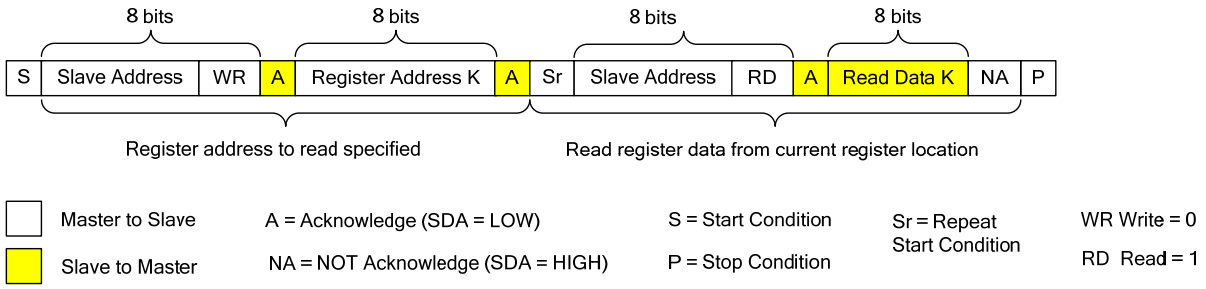
Figure 9: Complete Data Transfer

The MPQ8861 requires a start condition, a valid I²C address, a register address byte, and a data byte for a single data update. After receiving each byte, the MPQ8861 acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MPQ8861. The MPQ8861 performs an update on the falling edge of the LSB byte.

I²C WRITE AND READ SEQUENCE EXAMPLE



I²C Write Example–Write Single Register



I²C Read Example–Read Single Register

REGISER DESCRIPTION

Register Map

The MPQ8861 contains seven write or read registers. Register 00 is the feedback reference voltage selection register. Register 0x01 is the first system control register and can be used to set the slew rate, hiccup OCP, etc. Register 0x02 is the second system control register and can be used to set the switching frequency, current limit, etc.

Register 0x03 and register 0x04 are reserved for future use. Register 0x05 is the IC ID register. Register 0x06 is the IC status indication register and can be used to check if the IC is in over-current protection, over-temperature protection status, etc. The register map is shown below.

ADD	NAME	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0x00	VSEL	r/w	Reserved	Feedback reference						
0x01	SysCntlreg 1	r/w	EN	GO_BIT	Slew rate			Retry OVP	Hiccup OCP	Mode
0x02	SysCntlreg 2	r/w	PG deglitch time		Switching frequency		Soft stop	Current limit adjust		
0x03	Reserved	\	Reserved							
0x04	Reserved	\	Reserved							
0x05	ID1	r	Vendor ID				IC Revision ID			
0x06	Status	r	Reserved				OC	OTEW	OT	PG

1) Reg00 VSEL

Register 0x00 is the feedback reference voltage selection register. The MPQ8861 default feedback reference voltage is 0.72V, so the MPQ8861's default output voltage is determined by the FB resistor divider and 0.72V default reference after power start-up or EN start-up. The reference voltage is adjustable from 0.6V to 1.108V. Before adjusting the feedback reference voltage, the bit GO_BIT of the first system control register 0x01 should be set to 1, and then the reference voltage can be adjusted by the lower seven bits of register 0x00.

When the feedback reference voltage setting command is finished, GO_BIT auto-resets to 0 to prevent false operation of the VOUT scaling. GO_BIT should be set to 1 before adjusting the feedback reference voltage via the I^2C.

Table 3 shows the feedback reference voltage selection chart from 0.6V to 1.108V via the I^2C.

NAME	BITS	DEFAULT	DESCRIPTION
Reserved	D[7]	1	Reserved for further use.
Feedback reference	D[6:0]	001 1110	Set the feedback reference voltage from 0.6V to 1.108V (see Table 3). The default value is 0.72V.

Table 3: Feedback Reference Voltage Selection Chart

D[6:0]	VREF(V)	D[6:0]	VREF (V)	D[6:0]	VREF (V)	D[6:0]	VREF(V)
000 0000	0.6	010 0000	0.728	100 0000	0.856	110 0000	0.984
000 0001	0.604	010 0001	0.732	100 0001	0.86	110 0001	0.988
000 0010	0.608	010 0010	0.736	100 0010	0.864	110 0010	0.992
000 0011	0.612	010 0011	0.74	100 0011	0.868	110 0011	0.996
000 0100	0.616	010 0100	0.744	100 0100	0.872	110 0100	1
000 0101	0.62	010 0101	0.748	100 0101	0.876	110 0101	1.004
000 0110	0.624	010 0110	0.752	100 0110	0.88	110 0110	1.008
000 0111	0.628	010 0111	0.756	100 0111	0.884	110 0111	1.012
000 1000	0.632	010 1000	0.76	100 1000	0.888	110 1000	1.016
000 1001	0.636	010 1001	0.764	100 1001	0.892	110 1001	1.02
000 1010	0.64	010 1010	0.768	100 1010	0.896	110 1010	1.024
000 1011	0.644	010 1011	0.772	100 1011	0.9	110 1011	1.028
000 1100	0.648	010 1100	0.776	100 1100	0.904	110 1100	1.032
000 1101	0.652	010 1101	0.78	100 1101	0.908	110 1101	1.036
000 1110	0.656	010 1110	0.784	100 1110	0.912	110 1110	1.04
000 1111	0.66	010 1111	0.788	100 1111	0.916	110 1111	1.044
001 0000	0.664	011 0000	0.792	101 0000	0.92	111 0000	1.048
001 0001	0.668	011 0001	0.796	101 0001	0.924	111 0001	1.052
001 0010	0.672	011 0010	0.8	101 0010	0.928	111 0010	1.056
001 0011	0.676	011 0011	0.804	101 0011	0.932	111 0011	1.06
001 0100	0.68	011 0100	0.808	101 0100	0.936	111 0100	1.064
001 0101	0.684	011 0101	0.812	101 0101	0.94	111 0101	1.068
001 0110	0.688	011 0110	0.816	101 0110	0.944	111 0110	1.072
001 0111	0.692	011 0111	0.82	101 0111	0.948	111 0111	1.076
001 1000	0.696	011 1000	0.824	101 1000	0.952	111 1000	1.08
001 1001	0.7	011 1001	0.828	101 1001	0.956	111 1001	1.084
001 1010	0.704	011 1010	0.832	101 1010	0.96	111 1010	1.088
001 1011	0.708	011 1011	0.836	101 1011	0.964	111 1011	1.092
001 1100	0.712	011 1100	0.84	101 1100	0.968	111 1100	1.096
001 1101	0.716	011 1101	0.844	101 1101	0.972	111 1101	1.1
001 1110	0.72	011 1110	0.848	101 1110	0.976	111 1110	1.104
001 1111	0.724	011 1111	0.852	101 1111	0.98	111 1111	1.108

2) Reg01 SysCntlreg1

Register 0x01 is the first system control register.

The highest bit, EN, can be used to turn the part on or off when the external EN is high. When the external EN is high, the MPQ8861 shuts down by setting the EN bit to 0, and then the HS-FET and LS-FET stop switching. The MPQ8861 resumes switching by setting the EN bit to 1 again. When the external EN is low, the converter is off, and the I^2C shuts down.

Set GO_BIT to 1 to enable the I^2C's authority to write the feedback reference. When the command is finished, GO_BIT auto-resets to 0 to prevent false operation of the VOUT scaling.

The IC switches to forced PWM mode when GO_BIT is set to 1 to achieve a smooth output waveform during the output dynamic scaling. After the output scaling is complete, GO_BIT is set to 0 automatically, and the IC operation mode switches to the original mode set by the Mode bit.

The 3-bit slew rate D[5:3] is used for VOUT slew rate selection during the output voltage dynamic scaling. A proper slew rate reduces the inrush current, as well as voltage overshoot and undershoot. Eight different slew rate levels can be selected.

The bit retry OVP defines the protection mode when OVP is triggered. When retry OVP is set to 1, the part enters auto-recovery when OVP is removed. When retry OVP is set to 0, the MPQ8861 latches off once output OVP occurs, and VIN OVP is triggered until VIN or EN are toggled.

The bit hiccup OCP defines the OCP mode. When hiccup OCP is set to 1, the MPQ8861 enters hiccup mode when OCP and UVP are both triggered. When hiccup OCP is set to 0, the MPQ8861 enters latch-off when OCP and UVP are both triggered.

The lowest bit, mode, is used for selecting forced PWM or auto PFM/PWM mode at light load. When mode is set to 0, auto-PFM/PWM mode is enabled at light load. When mode is set to 1, forced PWM mode is enabled at light load.

<table>
<tr><th>NAME</th><th>BITS</th><th>DEFAULT</th><th>DESCRIPTION</th></tr>
<tr><td>EN</td><td>D[7]</td><td>1</td><td>I²C controlled turn-on or turn-off of the part. When the external EN is low, the converter is off, and the I²C shuts down. When EN is high, the EN bit takes over. The default EN bit is 1.</td></tr>
<tr><td>GO_BIT</td><td>D[6]</td><td>0</td><td>Switch bit of the I²C writing authority for the feedback reference command only. Set GO_BIT = 1 to enable the I²C's authority to write the feedback reference. When the command is finished, GO_BIT auto-resets to 0 to prevent false operation of the Vref scaling.
Voltage scaling examples:
1) Set GO_BIT = 1.
2) Write register 0x00: set the feedback reference.
3) Read back the GO_BIT value to see if the output scaling is finished. If GO_BIT = 0, the voltage scaling is done. Otherwise, Vref is still in adjustment.
4) Set GO_BIT = 1 if the output voltage scaling is needed a second time.
5) Write register 0x00: set the feedback reference.</td></tr>
<tr><td>Slew rate</td><td>D[5:3]</td><td>100</td><td>The slew rate during the I²C-controlled voltage changing is defined by three bits. The output voltage changes linearly from the previous voltage to the new set voltage with a VOUT slew rate (see below). This helps reduce inrush current, voltage overshoot, and voltage undershoot greatly.
<table>
<tr><th>D[5:3]</th><th>Slew Rate</th><th>D[5:3]</th><th>Slew Rate</th></tr>
<tr><td>000</td><td>19mV/µs</td><td>100</td><td>2.5mV/µs</td></tr>
<tr><td>001</td><td>15mV/µs</td><td>101</td><td>1.25mV/µs</td></tr>
<tr><td>010</td><td>10mV/µs</td><td>110</td><td>0.6mV/µs</td></tr>
<tr><td>011</td><td>5mV/µs</td><td>111</td><td>0.3mV/µs</td></tr>
</table></td></tr>
<tr><td>Retry OVP</td><td>D[2]</td><td>1</td><td>OVP mode selection bit. 1 means the part auto-recovers when OVP is removed. 0 means the part latches off once output OVP (including absolute OVP) and VIN OVP are both triggered until VIN or EN is power reset.</td></tr>
<tr><td>Hiccup OCP</td><td>D[1]</td><td>1</td><td>Over-current protection mode selection. 1 means hiccup mode OCP. 0 means latch-off type OCP.</td></tr>
<tr><td>Mode</td><td>D[0]</td><td>0</td><td>Set mode to 0 to enable PFM mode; set mode to 1 to disable auto-PFM/PWM mode. Default is auto-PFM/PWM mode for light load.</td></tr>
</table>

3) Reg02 SysCntlreg2

Register 0x02 is the second system control register.

The highest two bits of the PG deglitch time D[7:6] defines the PG signal rising and falling edge delay times. When output OVP or UVP is triggered, the PG signal turns low or high after a delay time. There are four levels of PG delay time that can be programmed by the I²C in different conditions.

The two switching frequency bits D[5:4] are used for switching frequency selection. The MPQ8861 supports up to 1.25MHz of switching frequency by setting the two bits to 11. The MPQ8861 maximum programmable switching frequency is limited by internal minimum on-time (see Table 1).

NAME	BITS	DEFAULT	DESCRIPTION			
PG Deglitch Time	D[7:6]	11	Power good signal rising and falling edges' delay time. When FB or VOUT is out of regulation window, the PG comparator is triggered, but needs a delay time before the PG signal can turn high or low.			
			D[7:6]	PG Deglitch	D[7:6]	PG Deglitch
			00	<1µs	10	12µs
			01	6µs	11	30µs
Switching Frequency	D[5:4]	00	Switching frequency set bit. There is no dedicated frequency oscillator inside the part. The switching frequency is fairly fixed by controlling the T_{ON} timer.			
			D[5:4]	Frequency	D[5:4]	Frequency
			00	500kHz	10	1MHz
			01	750kHz	11	1.25MHz
Soft Stop	D[3]	0	This bit defines the VOUT discharge behavior after EN shutdown. 0 means VOUT is not discharged after EN shutdown. 1 means VOUT is discharged linearly to zero with the set soft-stop time.			
Current Limit Adjust	D[2:0]	010	D[2:0]	Valley Current Limit (A)	D[2:0]	Valley Current Limit (A)
			000	19	100	10
			001	16	101	8.5
			010	14	110	7
			011	12	111	6

The bit soft stop defines the output voltage discharge behavior after EN shutdown. When soft stop is set to 0, the output voltage is not discharged after EN shutdown. When soft stop is set to 1, the output voltage is discharged linearly to zero with the set soft-stop time.

The lowest three bits, current limit adjust D[2:0], are used for peak and valley current-limit selection. There are eight levels of current limit that can be selected for different application conditions.

4) Reg03 and Reg04

Register 0x03 and register 0x04 are reserved for future use.

5) Reg05 ID1

Register 0x05 is the IC information indicating register. The highest four bits, vendor ID D[7:4], are set to 1000 internally.

The lowest four bits, IC Revision ID D[3:0], indicates IC revision information.

NAME	BITS	DESCRIPTION
Vendor ID	D[7:4]	1000.
IC Revision ID	D[3:0]	IC revision (0000).

6) Reg06 Status

Register 0x06 is a fault condition indicating register. The highest four bits, D[7:4], are reserved for future use.

The bit OC is the output over-current indication. When the bit is set to 1, the IC is in hiccup mode or OC latch-off.

The bit OTEW is the die temperature early warning indication. When the bit is set to 1, the IC die temperature is higher than 120°C.

The bit PG is output power good indication. When the bit is set to 1, the output power is normal.

NAME	BITS	DESCRIPTION
Reserved	D[7:4]	Reserved for future use.
OC	D[3]	Output over-current indication. When this bit is high, the IC is in hiccup mode or trips OC latch off.
OTEW	D[2]	Die temperature early warning bit. When the bit is high, the die temperature is higher than 120˚C. When the die temperature is less than 100°C, the bit returns to be low.
OT	D[1]	Over-temperature indication. When the bit is high the IC is in thermal shutdown
PG	D[0]	Output power good indication. When the bit is high the VOUT power is normal. This means VOUT is higher than 90% and lower than 115% of the designed regulation voltage. PG compares FB/VOUT with REF.

APPLICATION INFORMATION

Setting the Output Voltage in a FB Control Loop

The MPQ8861 can be controlled by the FB loop. The output voltage can be set by the external resistor dividers. The FB loop reference voltage is a default value (0.72V) and can be programmed by the I²C. The MPQ8861's output voltage must be below the absolute OVP threshold (typically 6.5V).

The FB loop network is shown in Figure 10.

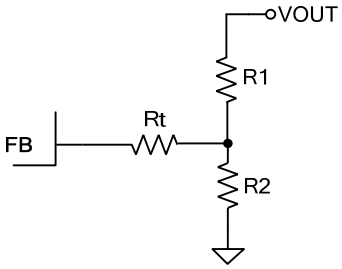


Figure 10: FB Loop Network

Calculate R1 and R2 with Equation (4):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.72V} - 1} \quad (4)$$

Table 4 lists the recommended feedback resistors value for common output voltages. The recommended parameters are based on 47µFx3 output capacitor. Different input voltage and output capacitor values may affect the selection of R1 and R2. For other components' parameters, please refer to the Typical Application Circuits

Table 4: Resistor Selection for Common Output Voltages

V_{IN}(V)	V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	Rt(kΩ)	L(µH)
5	0.85	16.5	90.9	10	0.47
5	1.0	36.5	93.1	10	0.68
5	1.2	36.5	54.9	10	0.68
5	1.5	36.5	33.2	10	0.68
5	1.8	36.5	24.3	10	0.68
5	2.5	36.5	14.7	10	1
5	3.3	36.5	10.2	10	0.68
12	0.85	16.5	90.9	10	1
12	1.0	36.5	93.1	10	1
12	1.2	36.5	54.9	10	1
12	1.5	36.5	33.2	10	1
12	1.8	80.6	53.6	10	1.5
12	2.5	80.6	32.4	10	1.5
12	3.3	80.6	22.6	10	2.2
12	5	80.6	13.7	10	2.2

Output Voltage Dynamic Scale

The output voltage dynamic scaling can be done only via the I²C. Refer to Figure 11 and follow the steps below.

1) Write GO_BIT (Reg01[6]) to 1.
2) Write Reg00 to set the reference voltage by feedback reference (Reg00 [6:0]) simultaneously. When the command is finished, GO_BIT auto-resets to 0 to prevent false operation of the VOUT scaling.

Repeat the above two steps if the output voltage must be changed to a different voltage.

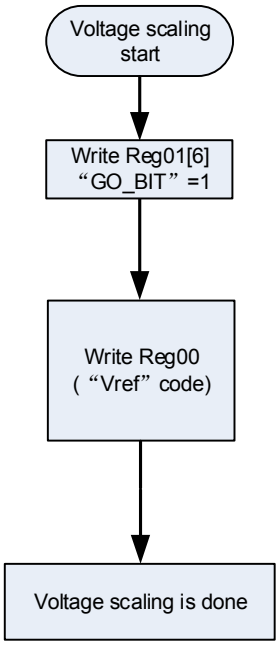


Figure 11: Output Voltage Dynamic Scale Flow Chart

Selecting the Inductor

Use a 0.47µH to 5µH inductor with a DC current rating at least 25% higher than the maximum load current for most applications. For the highest efficiency, use an inductor with a DC resistance less than 5mΩ. For most designs, the inductance value can be derived from Equation (5):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (5)$$

Where ΔI_L is the inductor ripple current. Choose the inductor ripple current to be approximately 30% of the maximum load current and be less than 4A PK to PK. The maximum inductor peak current can be calculated with Equation (6):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (6)$$

Use a larger inductor for improved efficiency under light-load conditions below 100mA.

Table 4 lists the recommended inductor for common output voltages and Common Input Voltages.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-downconverter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are recommended because of their low ESR and small temperature coefficients. For most applications, use two 22µF capacitors.

Since C1 absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (7):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (7)$$

The worst-case condition occurs at VIN = 2VOUT, shown in Equation (8):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (8)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g.: 0.1µF) placed as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (9):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (10)$$

Where L_1 is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (11)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (12)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MPQ8861 can be optimized for a wide range of capacitance and ESR values.

External Bootstrap Diode

An external bootstrap diode can enhance the efficiency of the regulator given the following conditions:

- VOUT is 5V or 3.3V
- Duty cycle is high: D > 50%

In these cases, add an external BST diode from VCC to BST (see Figure 12).

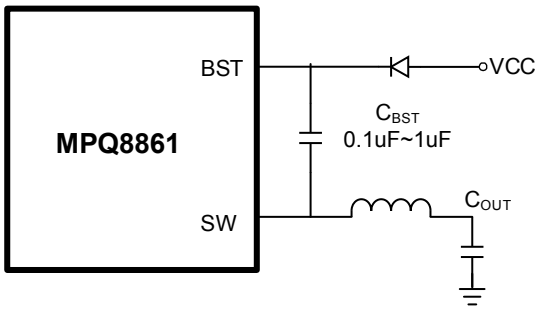


Figure 12: Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the recommended BST capacitor value is 0.1μF to 1μF.

Connect VCC to VIN at a Low Input Voltage

VCC can be connected to VIN directly when VIN is lower than 3.5V. This helps improve the MPQ8861's low input voltage efficiency performance. To use this application set-up, the VIN spike voltage must be limited below 4V, otherwise VCC may be damaged.

PCB Layout Guidelines [8]

Efficient PCB layout is critical for stable operation. A four-layer layout is strongly recommended to achieve better thermal performance. For best results, refer to Figure 13 and follow the guidelines below.

1. Place the high-current paths (PGND, VIN, and SW) very close to the device with short, direct, and wide traces.
2. Keep the VIN and PGND pads connected with large copper planes.
3. Use at least two layers for the VIN and PGND trace to achieve better thermal performance.
4. Add several vias close to the IN and PGND pads to help with thermal dissipation. Place more than one via adjacent to the inner edge of PGND pad which connects to AGND pad through low impedance routing or ground plane.
5. Place the input capacitors as close to VIN and PGND as possible.
6. Place the decoupling capacitor as close to VCC and PGND as possible.
7. Add several vias close the the AGND pad, and connect to PGND plane with Kelvin connection.
8. Place the external feedback resistors next to FB.
9. Ensure that there is no via on the FB trace.
10. Keep the switching node SW short and away from the feedback network.
11. Keep the BST voltage path (BST, C3, and SW) as short as possible.

Note:

8) The recommended layout is based on the Typical Application circuit on page 25.

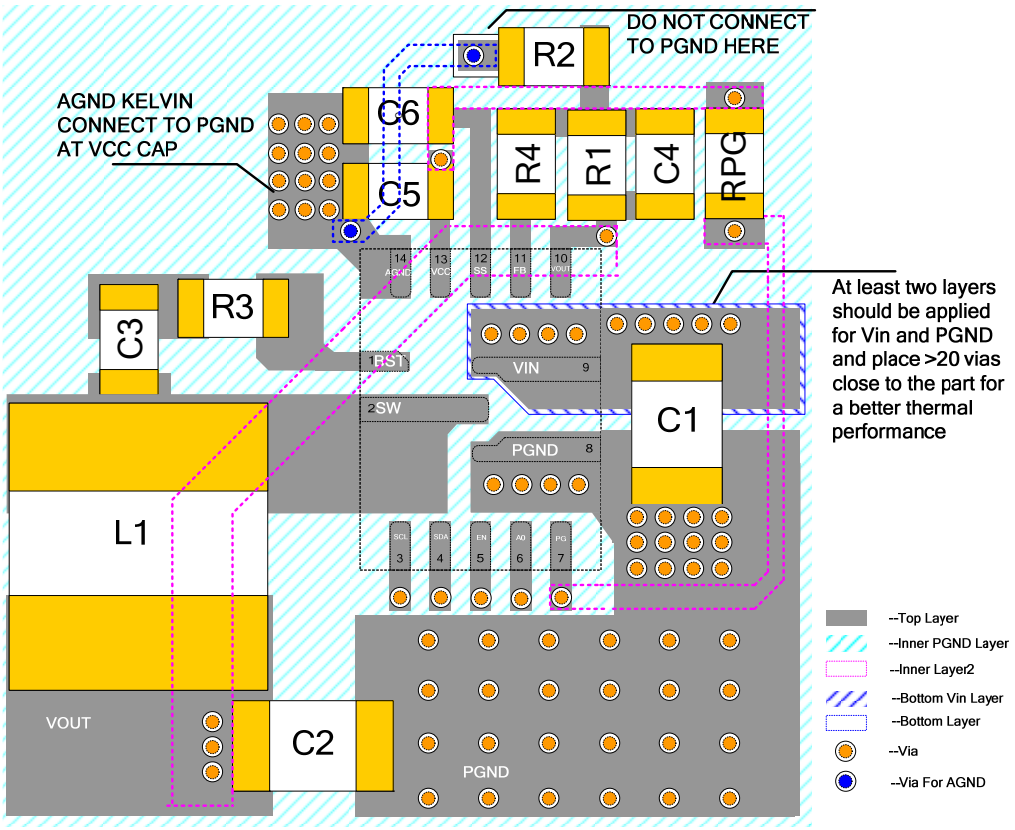


Figure 13: Recommended Layout

Design Example

Table 5 is a design example following the application guidelines for the specifications below.

Table 5: Design Example

V_{IN}	5V
V_{OUT}	1V
I_O	12A

The detailed application schematics are shown in Figure 14 though Figure 20. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section. For more device applications, please refer to the related evaluation board datasheets.

TYPICAL APPLICATION CIRCUITS (9)

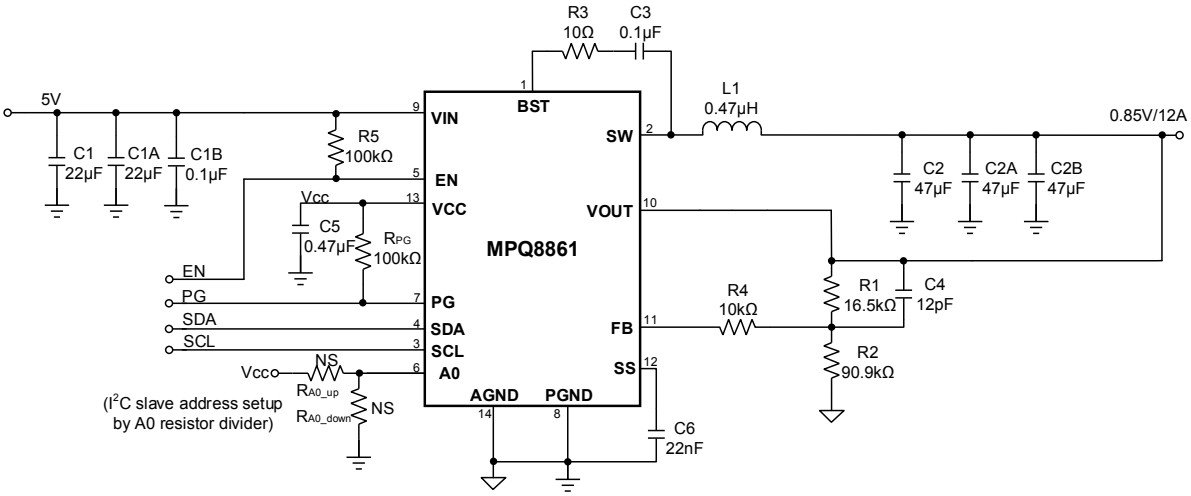


Figure 14: V_{IN} = 5V, V_{OUT} = 0.85V, I_{OUT} = 12A

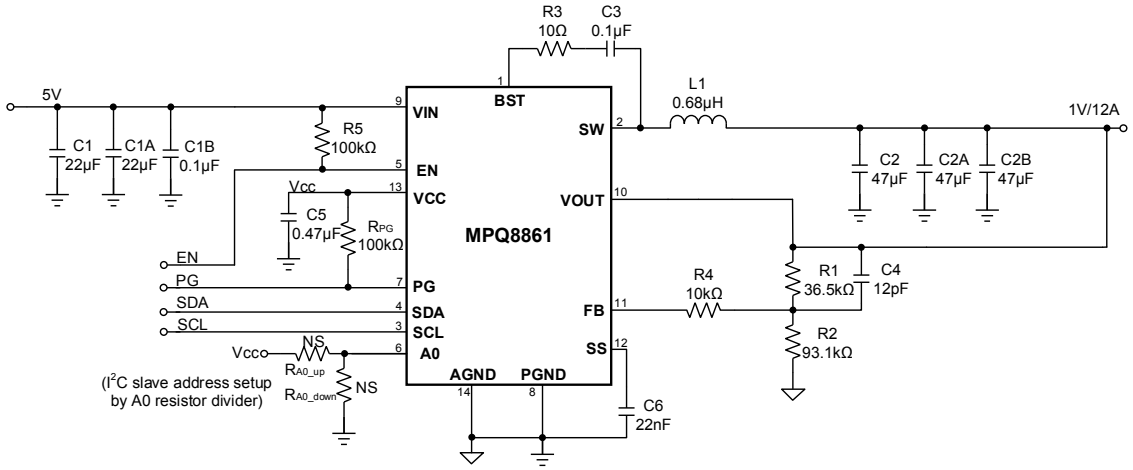


Figure 15: V_{IN} = 5V, V_{OUT} = 1V, I_{OUT} = 12A

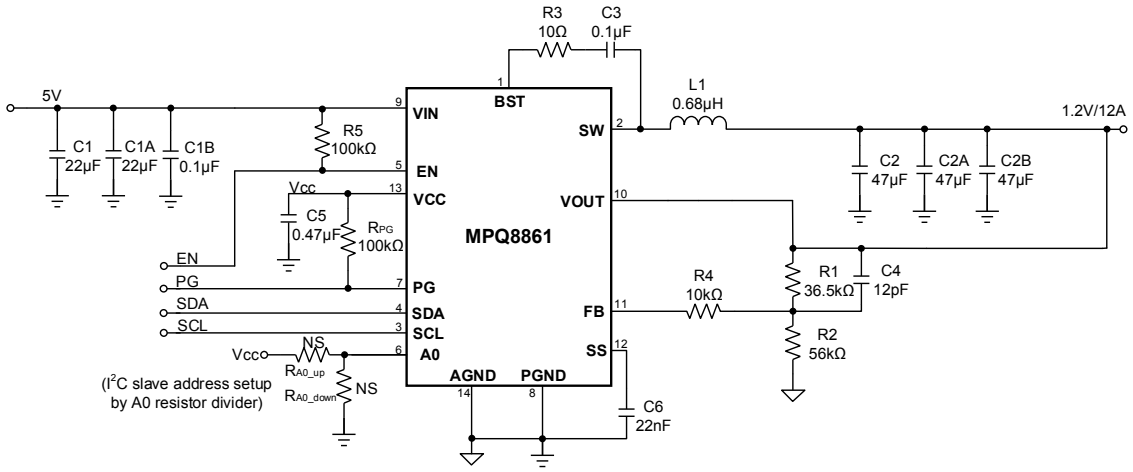


Figure 16: V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 12A

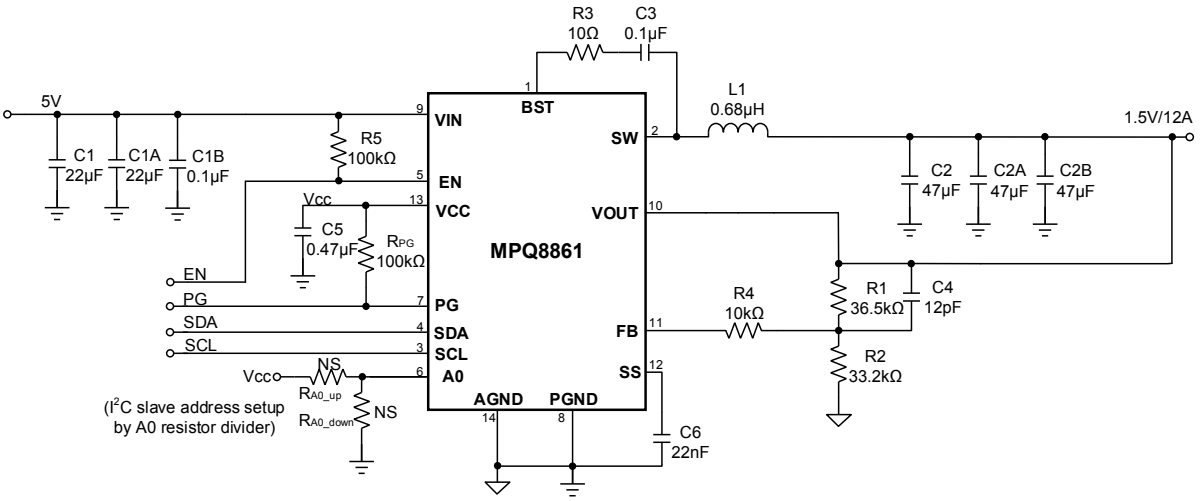


Figure 17: V_{IN} = 5V, V_{OUT} = 1.5V, I_{OUT} = 12A

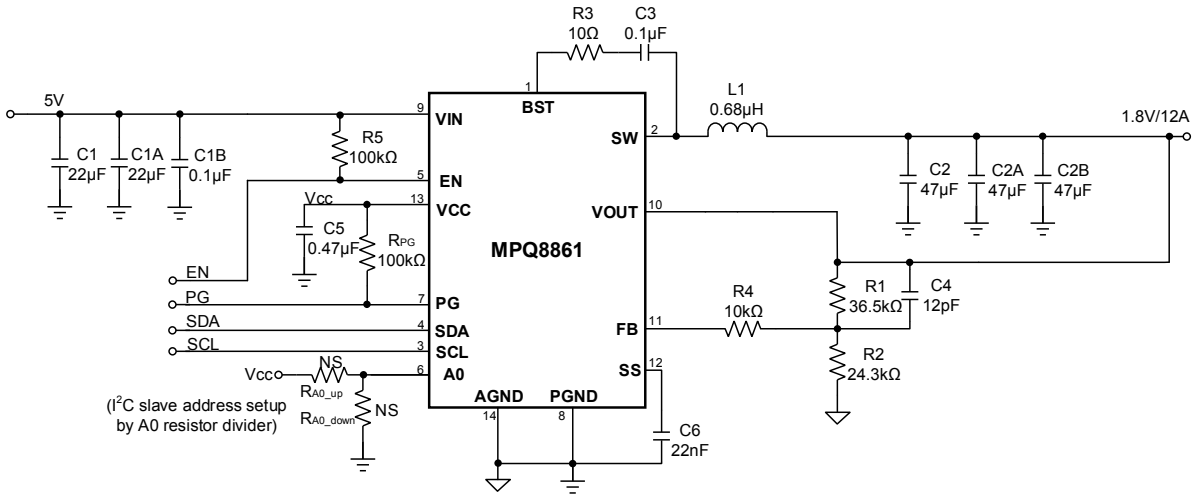


Figure 18: V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 12A

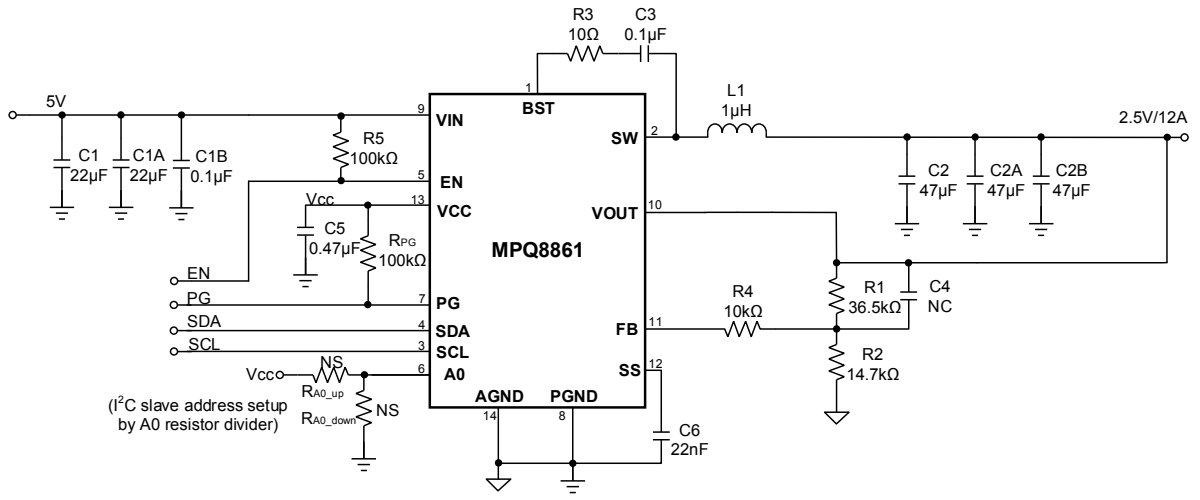


Figure 19: V_{IN} = 5V, V_{OUT} = 2.5V, I_{OUT} = 12A

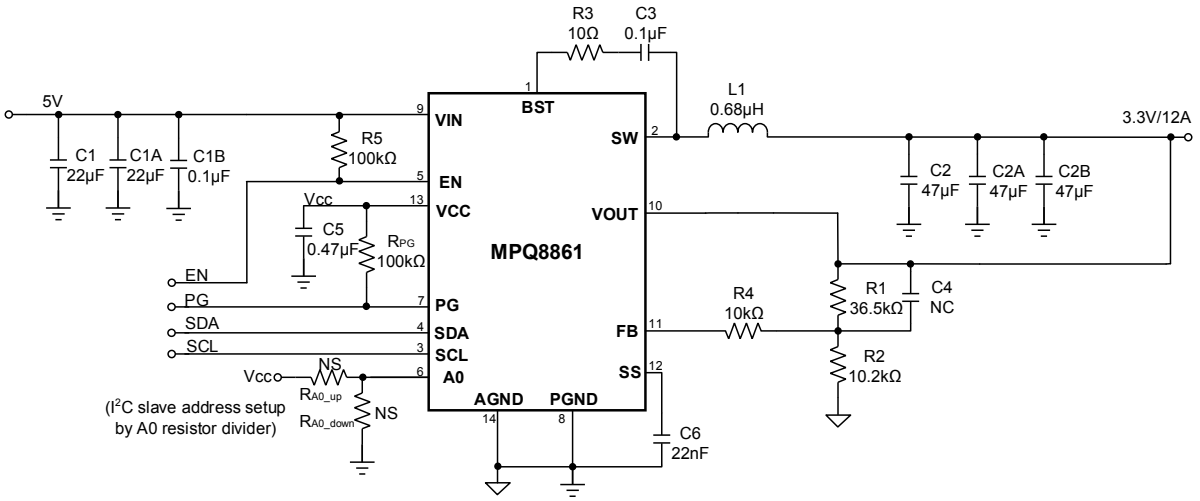


Figure 20: V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 12A

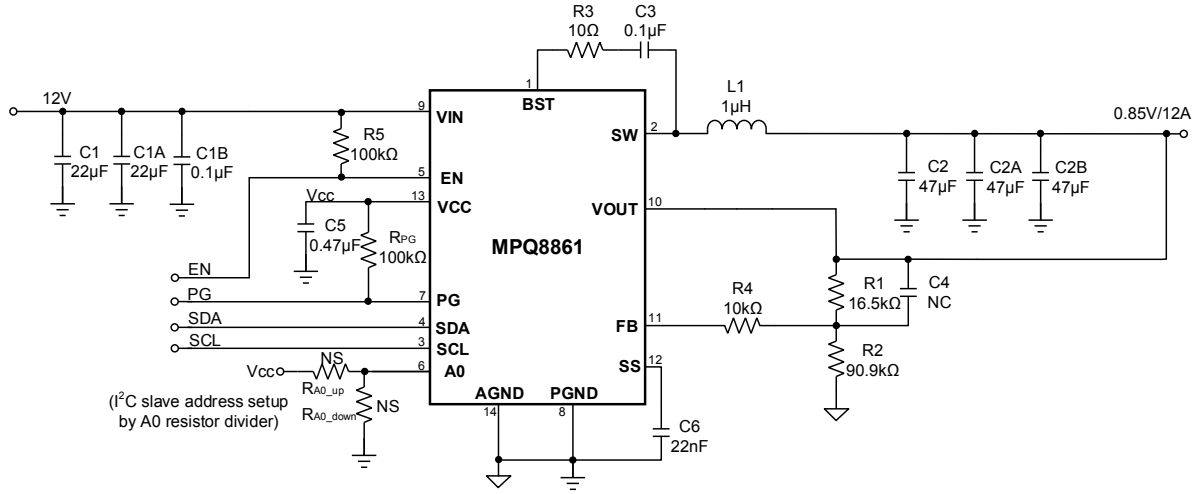


Figure 21: V_{IN} = 12V, V_{OUT} = 0.85V, I_{OUT} = 12A

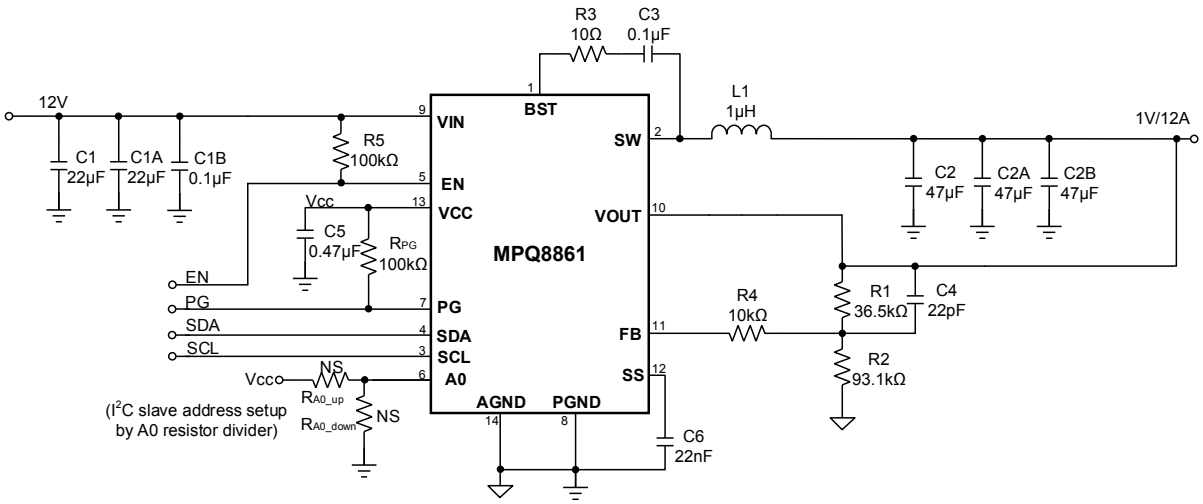


Figure 22: V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 12A

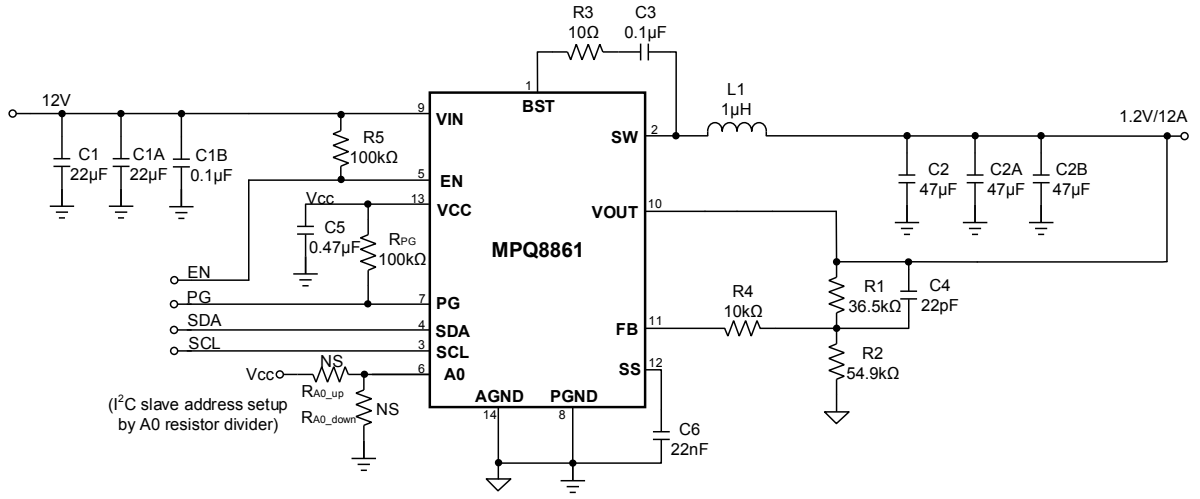


Figure 23: V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 12A

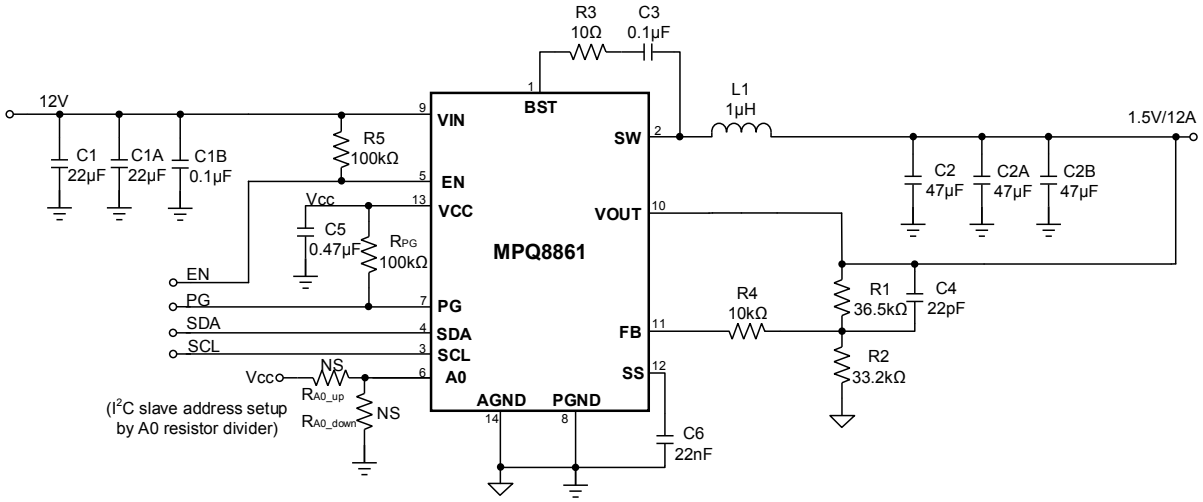


Figure 24: V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 12A

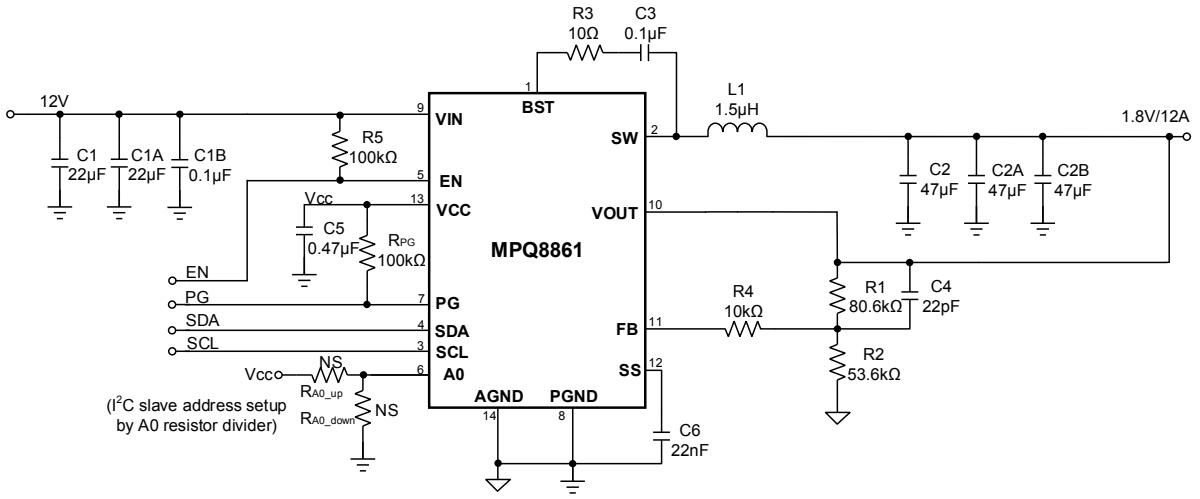


Figure 25: V_{IN} = 12V, V_{OUT} = 1.8V, I_{OUT} = 12A

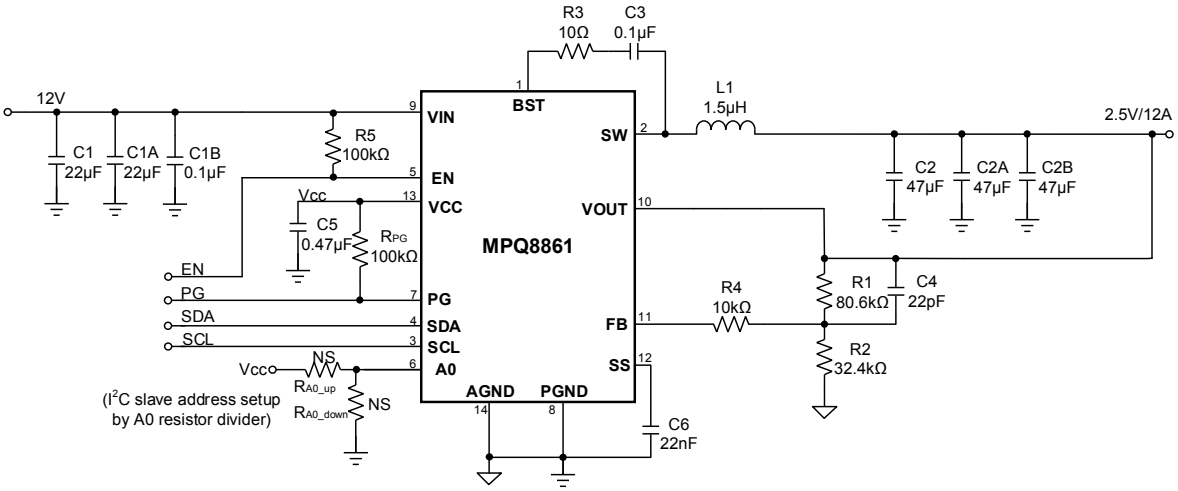


Figure 26: V_{IN} = 12V, V_{OUT} = 2.5V, I_{OUT} = 12A

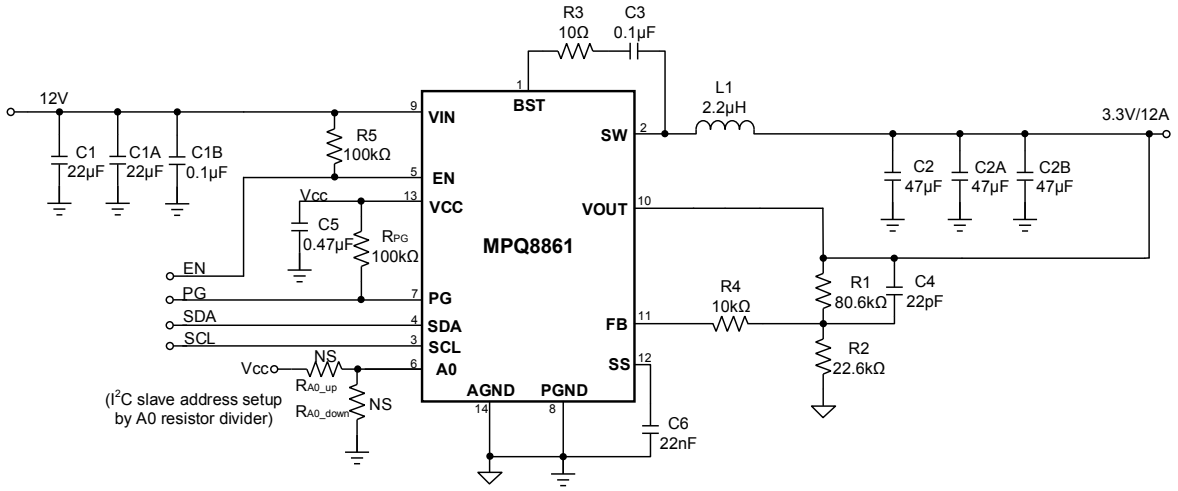


Figure 27: V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 10A

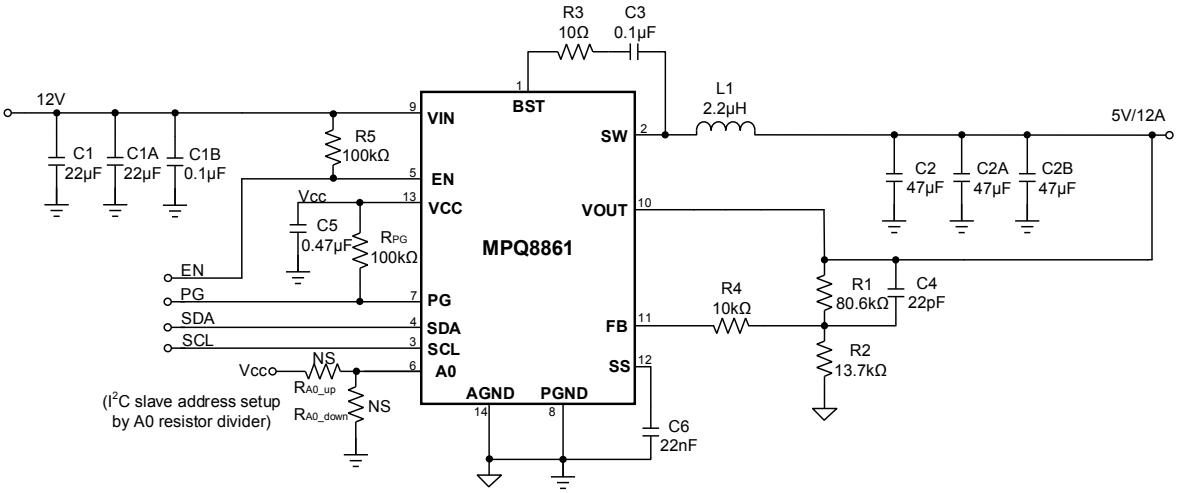


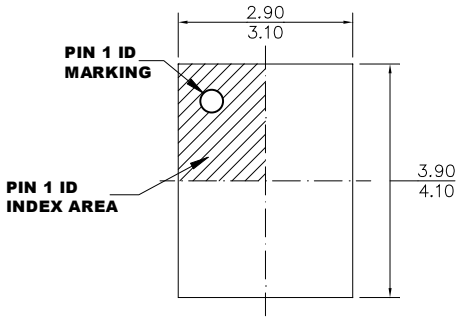
Figure 28: V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 10A

Note:

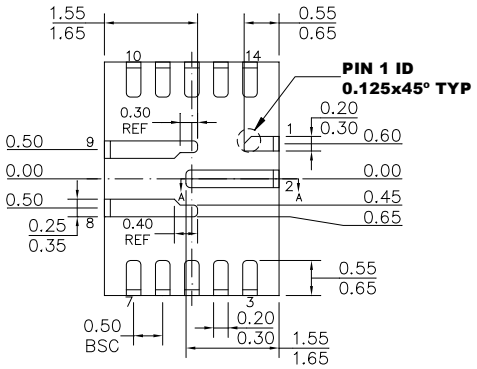
9) All circuits are based on a 0.72V default reference voltage. The MPQ8861's output voltage can be adjusted by the feedback reference voltage and external resistor dividers. However, the MPQ8861's output voltage must be set lower than the absolute over-voltage protection threshold (typically 6.5V). SCL/SDA should connect to VCC when i2c function is not used.

PACKAGE INFORMATION

QFN-14 (3mmx4mm)

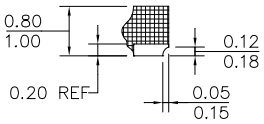


TOP VIEW

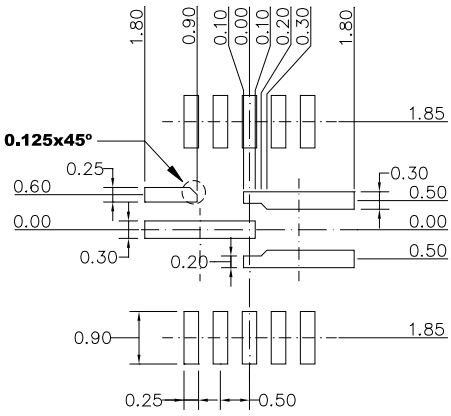


BOTTOM VIEW

SIDE VIEW



SECTION A-A

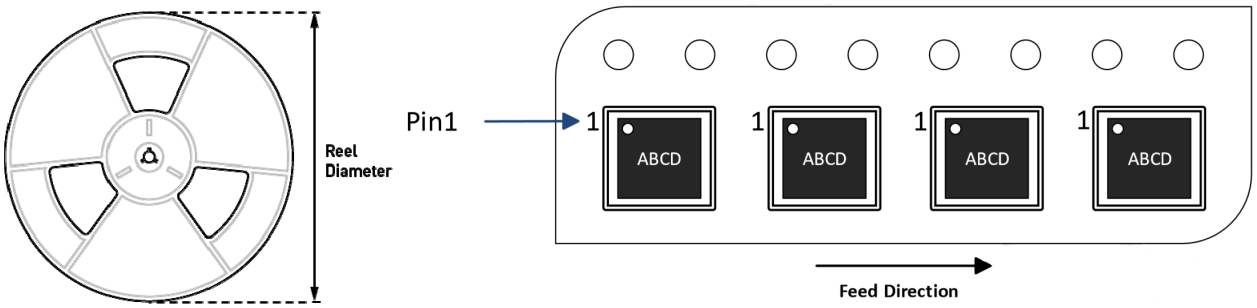


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity /Reel	Quantity /Tube	Quantity /Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ8861GLE-AEC1–Z	QFN-14 (3mmx4mm)	5000	N/A	N/A	13 in.	12 mm	8 mm