



The Future of Analog IC Technology®

MP9361

High Performance Regulated Charge Pump

DESCRIPTION

The MP9361 is a high performance, regulated charge pump converter. Its input voltage ranges from 2.8V to V_{out}. The output voltage is regulated to a fixed 5V. No external inductor is required for simplicity and compactness. Internal soft-start circuit effectively reduces the in-rush current both while start-up and mode change.

The MP9361 is available in a compact TSOT23-6 package

FEATURES

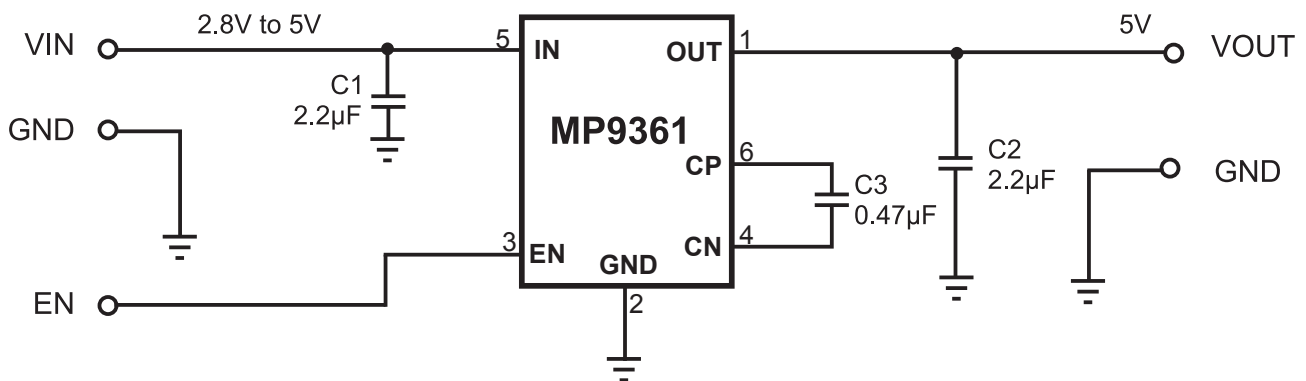
- Input Voltage Range: 2.8V to 5V
- Internal Soft-Start
- Output Maximum Current up to 110mA
- Fixed 5V Output Voltage with 30mV Ripple
- 2X Charge Pump
- Fixed 1.35MHz Switching Frequency
- Over Current Protection
- Short Circuit Protection
- In-rush Current limit
- TSOT23-6 package and Lead (pb)-Free

APPLICATIONS

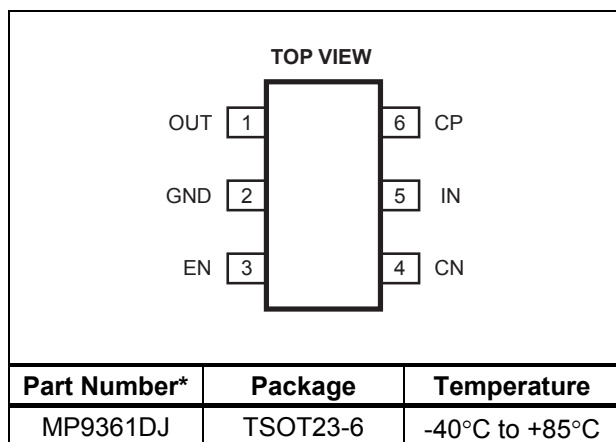
- Cell phone, Smart phone, LED backlight
- PDA or hand Held Computer
- Camera Flash White LED
- LCD Display Supply
- TV-Remote Control

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TYPICAL APPLICATION



PACKAGE REFERENCE



* For Tape & Reel, add suffix -Z (e.g. MP9361DJ-Z)
 For RoHS compliant packaging, add suffix -LF
 (e.g. MP9361DJ-LF-Z)

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Supply Input Voltage..... -0.3V to +6.0V
 All Other Pins -0.3V to +6.0V
 Storage Temperature..... -65°C to +150°C
 Junction Temperature..... +150°C
 Lead Temperature +260°C

Recommended Operating Conditions ⁽²⁾

Supply Voltage V_{IN} 2.8V to 5.0V
 Output Voltage V_{OUT} 5.0V
 Operating Temperature -40°C to +85°C

Thermal Resistance ⁽³⁾ θ_{JA} θ_{JC}

TSOT23-6 195 25 ... °C/W

Maximum Power Dissipation ⁽⁴⁾ ($T_A=25^\circ\text{C}$)

TSOT23-6 P_D 0.64 W

Notes:

- 1) Exceeding these ratings may damage the device.
- 2) The device is not guaranteed to function outside of its operating conditions.
- 3) Measured on JESD51-7 4-layer board.
- 4) Reduce 0.05 watts every 10°C increasing.

ELECTRICAL CHARACTERISTICS

$V_{IN}=3.7V$, $C_{IN}=C_{OUT}=2.2\mu F$, $C_P=0.22\mu F$, $T_A=25^\circ\text{C}$, Unless otherwise noted

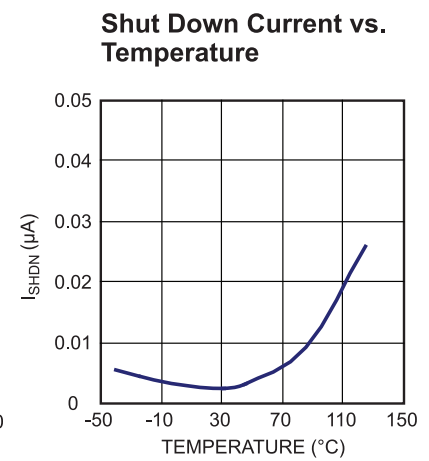
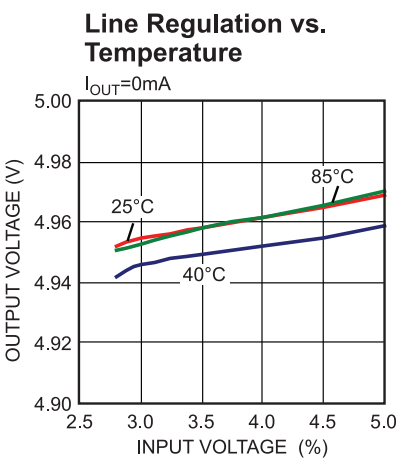
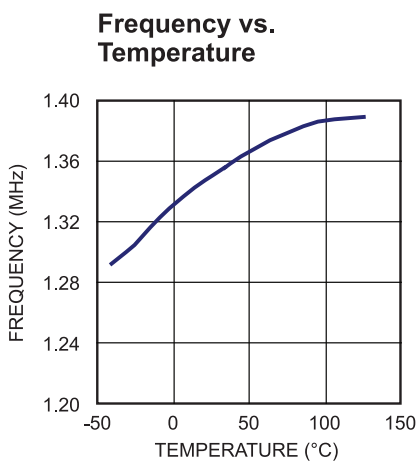
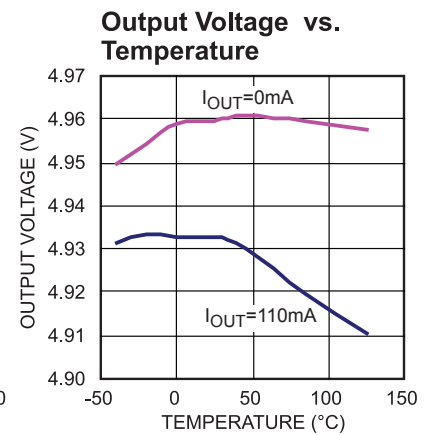
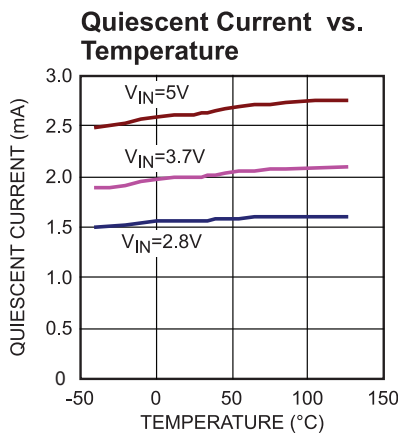
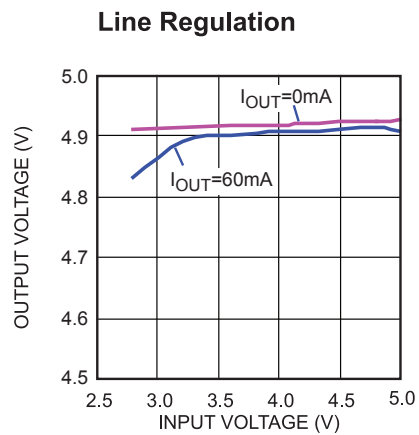
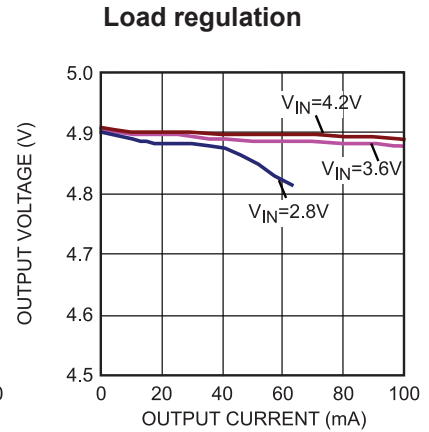
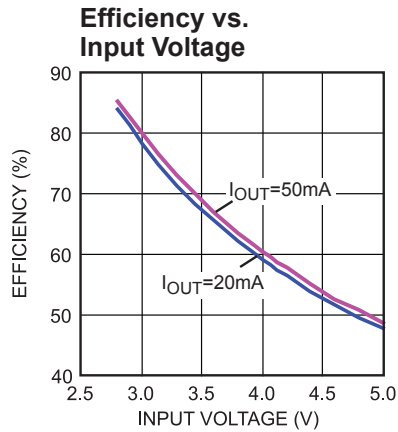
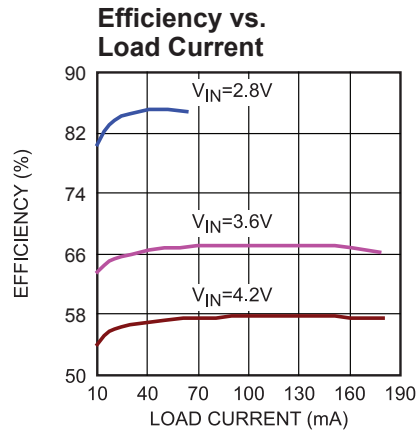
Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Supply Voltage	V_{IN}		2.8		5	V
Output Voltage	V_{OUT}	$V_{IN}>3.2V$, $I_{OUT}<110mA$	4.8	5	5.2	V
Quiescent Current	I_Q	$I_{OUT}=0$		2	4	mA
Maximum Output Current	I_O	$V_{IN}>3.2V$	110			mA
Over Current Protection	I_{OCP}	$V_{OUT}=5V$	250	350	500	mA
Short Circuit Protection	I_{SHORT}			60	90	mA
Output Ripple		$I_{OUT}=60mA$		30		mV
Shut Down Current	I_{SHDN}	$V_{IN}=4.5V$, $V_{EN}<0.4V$		0.1	1	μA
Operation Frequency	F_{OSC}		1.1	1.35	1.6	MHz
Enable Voltage, High	V_{EN} (HIGH)			1.5		V
Enable Voltage, Low	V_{EN} (LOW)			0.4		V
Enable Pin Leakage	I_{EN}	$V_{EN}=5V$		0.2	1	μA

PIN FUNCTIONS

Pin #	Name	Description
1	OUT	Output Voltage. Decoupled with a 2.2 μ F ceramic capacitor for a load current less than 60mA. For a load current greater than 60mA, use 10 μ F decoupling capacitor.
2	GND	Ground.
3	EN	Device Enable: A logic high input ($V_{EN}>1.5V$) turns on the regulator. A logic low input ($V_{EN}<0.4V$)
4	CN	Flying Capacitor Negative Terminal.
5	IN	Input.
6	CP	Flying Capacitor Positive Terminal.

TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN}=3.7V$, $V_{OUT}=5V$, $C1=C2=2.2\mu F$, $C3=0.47\mu F$. $T_A=25^\circ C$, unless otherwise noted.

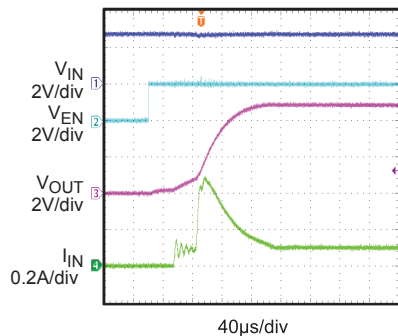


TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN}=3.7V$, $V_{OUT}=5V$, $C1=C2=2.2\mu F$, $C3=0.47\mu F$. $T_A=25^\circ C$ Unless otherwise noted. (continued)

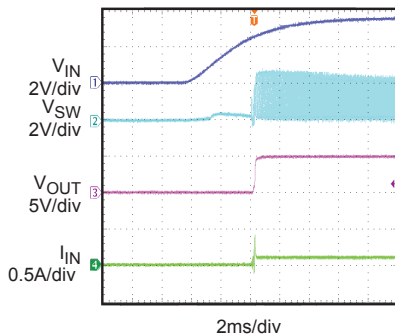
Inrush Current

$V_{IN}=2.8V$, $I_{OUT}=64mA$
with resistor load



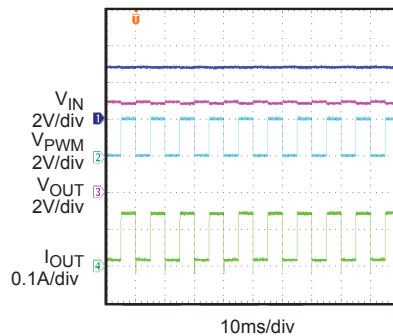
Inrush Current

$V_{GN}=V_{IN}=3.6V$, $I_{OUT}=64mA$
with resistor load



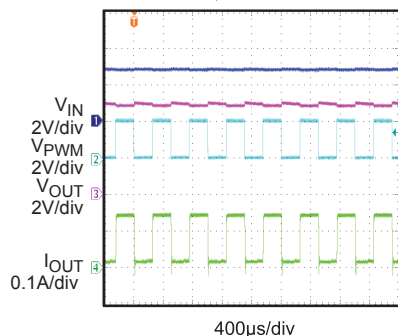
Load PWM Dimming Operation

$V_{EN}=V_{IN}=2.8V$, $F_{PWM}=100HZ$



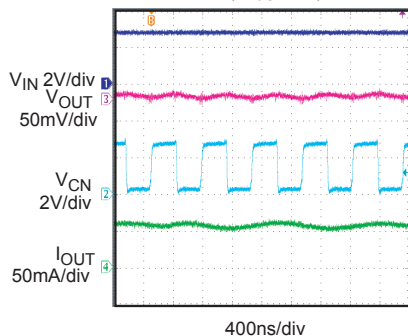
Load PWM Dimming Operation

$V_{EN}=V_{IN}=2.8V$, $F_{PWM}=2KHZ$



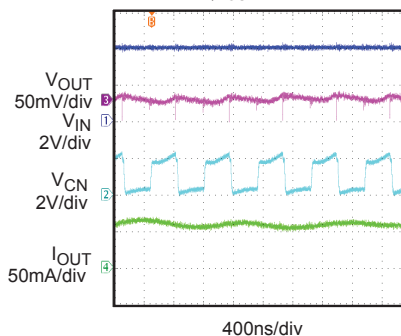
Normal Load Ripple

$V_{EN}=V_{IN}=2.8V$, $V_{OUT}=5V$, $I_{OUT}=60mA$



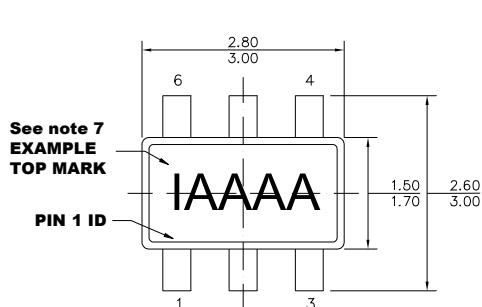
Normal Load Ripple

$V_{IN}=V_{EN}=4V$, $I_{OUT}=60mA$

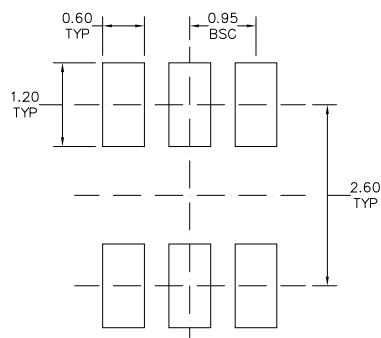


PACKAGE INFORMATION

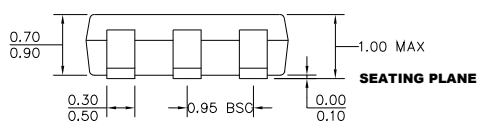
TSOT23-6



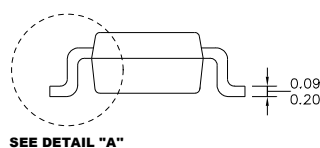
TOP VIEW



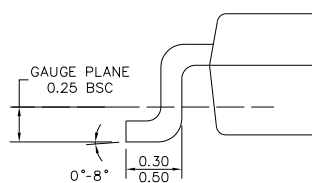
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
- 5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AB.
- 6) DRAWING IS NOT TO SCALE.
- 7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

**REVISION HISTORY**

Revision #	Revision Date	Description	Pages Updated
1.0	4/7/2021	Correct the description about EN logic.	Page 3

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