MP5402M

5A, 36V, Frequency Selectable Step-Down Converter with Smart Dual USB Charging Ports

The Future of Analog IC Technology

DESCRIPTION

The MP5402M integrates a monolithic, step-down, switch-mode converter with two USB current-limit switches and a charging port identification circuit. It achieves 5A of continuous output current over a wide input supply range with excellent load and line regulation.

The output of the USB switch is current limited. Both USB ports support DCP schemes for the battery charging specification (BC1.2), the divider mode, and the 1.2V/1.2V mode, eliminating outside user interaction.

The output voltage has programmable line drop compensation.

Fault condition protection includes hiccup current limiting, output OVP, and thermal shutdown (TSD).

The MP5402M requires a minimum number of readily available, standard, external components and is available in a QFN-26 (4mmx4mm) package.

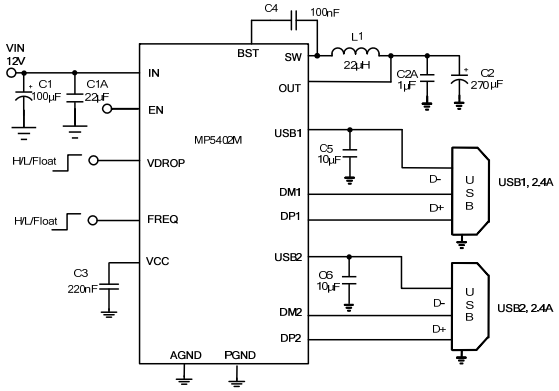
FEATURES

- EMI Reduction Technique
- Wide 7V to 36V Operating Input Voltage Range
- Fixed 5V Output Voltage with Line Drop Compensation
- Accurate USB1/USB2 Output Current Limit
- 40mΩ/32mΩ Low-$R_{DS(ON)}$ Internal Buck Power MOSFETs
- 24mΩ/24mΩ Low-$R_{DS(ON)}$ Internal USB1/USB2 Power MOSFETs
- 350kHz/250kHz/150kHz Frequency Selectable
- Programmable Line Drop Compensation
- Output Over-Voltage Protection
- Hiccup Current Limit
- Supports DCP Schemes for BC1.2, Divider Mode, and 1.2V/1.2V Mode
- ±8kV HBM ESD Rating for USB, DP, and DM
- Available in a QFN-26 (4mmx4mm) Package

APPLICATIONS

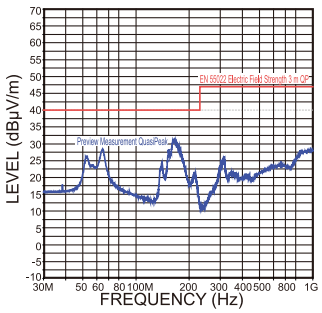
- USB Dedicated Charging Ports (DCP)
- Smart Cigarette Lighter Adapter USB Chargers

TYPICAL APPLICATION



Radiated EMI

V_{IN}=12V, f_S=150kHz, USB1_I_{OUT}=2.4A, USB2_I_{OUT}=2.4A, Quasi-peak detector



ORDERING INFORMATION

Part Number*	Package	Top Marking
MP5402MGR	QFN-26 (4mmx4mm)	*See Below*

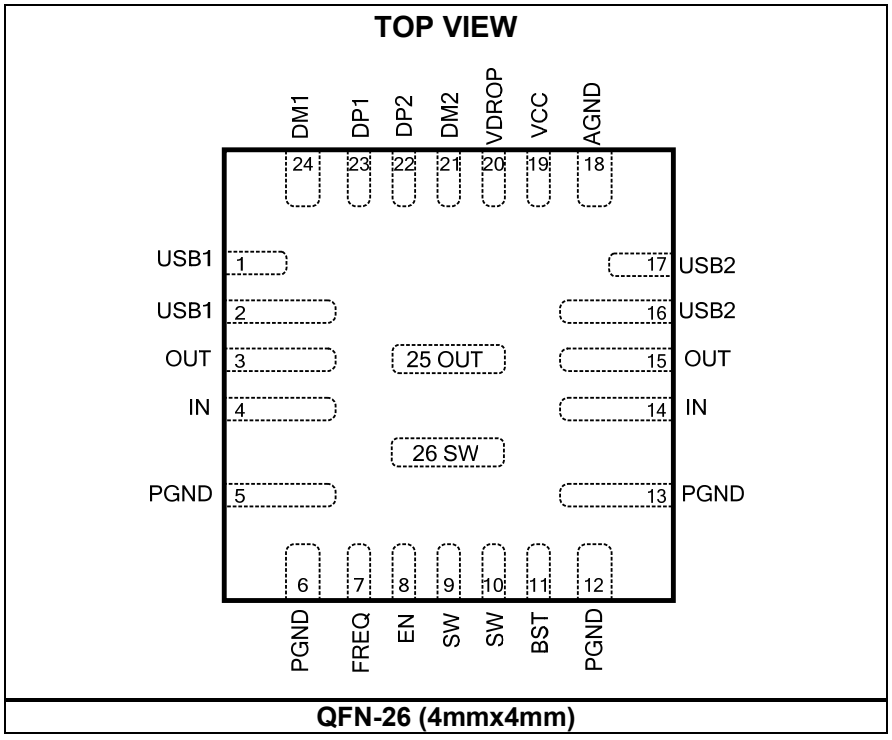
* For Tape & Reel, add suffix –Z (e.g. MP5402MGR–Z)

TOP MARKING

MPSYWW
M5402M
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
M5402M: Product code
LLLLLL: Lot number

PACKAGE REFERENCE



QFN-26 (4mmx4mm)

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 40V
V_{SW} .....
–0.3V (-5V for <10ns) to V_{IN} + 0.3V (43V for <10ns)
V_{BST} ..... V_{SW} + 6.5V
V_{EN} ..... -0.3V to 10V(2)
All other pins .....-0.3V to +6.5V
Continuous power dissipation (T_A = +25°C) (3)
QFN-26 (4mmx4mm) 2.8W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (4)

Operation input voltage range ..... 7V to 36V
Output current.....2.4A for USB1, 2.4A for USB2
Operating junction temp. (T_J). .. -40°C to +125°C

Thermal Resistance (5)	θ_{JA}	θ_{JC}
QFN-26 (4mmx4mm)	44	9 °C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) For details of the EN's ABS max rating, please refer to the EN control section on page 11.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will produce an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C(6). Typical value is tested at T_J = +25°C unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN} = 0V,T_J = +25°C			1	μA
		V_{EN} = 0V,T_J = -40°C to +125°C			5	
Supply current (quiescent)	I_{Q_OL}	No switching		1.6	2.5	mA
EN rising threshold	V_{EN_Rising}		1.33	1.43	1.52	V
EN hysteresis	$V_{EN\_Falling}$		110	140	170	mV
EN input current	I_{EN}	V_{EN} = 2V, T_J = +25°C	1.1	1.8	2.5	μA
		V_{EN} = 2V,T_J = -40°C to +125°C	0.8	1.8	3	
		V_{EN} = 0V		0		
Thermal shutdown(7)	T_{STD}			165		°C
Thermal hysteresis(7)	T_{STD_HYS}			20		°C
VCC regulator	V_{CC}		4.75	5.1	5.45	V
VCC load regulation	V_{CC_LOG}	I_{CC} = 5mA		1	2	%
Step-Down Converter						
V_{IN} under-voltage lockout threshold rising	V_{IN_UVLO}	T_J = +25°C	5.2	5.7	6.2	V
V_{IN} under-voltage lockout threshold hysteresis	V_{UVLO_HYS}			1		V
HS switch-on resistance	R_{DSON_HS}			40		mΩ
LS switch-on resistance	R_{DSON_LS}			32		mΩ
Output voltage	V_{OUT}	7V < V_{IN} < 36V, no load, T_J = +25°C	5	5.05	5.1	V
		7V < V_{IN} < 36V, no load, T_J = -40°C to +125°C	4.95	5.05	5.15	
Output over-voltage protection	V_{OVP_R}		5.65	6	6.4	V
OVP recovery	V_{OVP_F}	T_J = -40°C to +125°C	5.4	5.75	6.1	V
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 36V or 0V, T_J = +25°C			1	μA
		V_{EN} = 0V, V_{SW} = 36V or 0V, T_J = -40°C to +125°C			5	
Current limit(7)	I_{LIMIT}	40% duty cycle		8.5		A
Oscillator frequency	f_{SW1}	FREQ = high, T_J = +25°C	310	350	410	kHz
		FREQ = high, T_J = -40°C to +125°C	300	350	420	
	f_{SW2}	FREQ = low, T_J = +25°C	220	250	300	
		FREQ = low, T_J = -40°C to +125°C	190	250	330	
	f_{SW3}	FREQ = float, T_J = +25°C	125	150	180	
		FREQ = float, T_J = -40°C to +125°C	110	150	185	
Maximum duty cycle	D_{MAX}	FREQ = 350kHz	84	88		%
Minimum on time(7)	T_{ON_MIN}	T_J = +25°C		130		ns
Soft-start time	t_{SS}	Output from 10% to 90%,T_J = +25°C	1	1.65	2.3	ms
		Output from 10% to 90%,T_J = -40°C to +125°C	0.9	1.65	2.4	

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C[6]. Typical value is tested at T_J = +25°C unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
USB Switch						
Under-voltage lockout threshold rising	V_{USB_UVR}	T_J = +25°C	3.8	4	4.3	V
		T_J = -40°C to +125°C	3.75	4	4.33	
Under-voltage lockout threshold hysteresis	V_{USB_UVHYS}		220	270	320	mV
Switch-on resistance	R_{DSON_SW}			24		mΩ
Current limit	I_{Limit}	T_J = +25°C	2.6	2.75	2.9	A
Line drop compensation	V_{DROP_COM1}	Max load 2.4A, V_{DROP} = float, T_J = +25°C	300	400	500	mV
	V_{DROP_COM2}	Max load 2.4A, V_{DROP} = high		280		mV
	V_{DROP_COM3}	Max load 2.4A, V_{DROP} = GND		130		mV
FREQ, VDROP high level	V_{HIGH}		V_{CC}-0.4V			V
FREQ, VDROP middle level	V_{MIDDLE}			2.5		V
FREQ, VDROP low level	V_{LOW}				0.4	V
V_{BUS} soft-start time	T_{SS}	V_{OUT} = 5V, from 10% to 90%,T_J = +25°C	1	1.6	2.2	ms
		V_{OUT} = 5V, from 10% to 90%, T_J = -40°C to +125°C	0.9	1.6	2.4	
Discharge resistance	R_{DCHG}	T_J = +25°C		50	70	Ω
		T_J = -40°C to +125°C		50	75	
Hiccup mode on time	T_{HICP_ON1}	V_{OUT} = 5V, V_{BUS} connected to GND		3[7]		ms
	T_{HICP_ON2}	V_{OUT} = 5V, V_{BUS} > 2V, OC T_J = +25°C	3.5	5	6.5	
		V_{OUT} = 5V, V_{BUS} > 2V, OC T_J = -40°C to +125°C	3	5	7	
Hiccup mode off time	T_{HICP_OFF}	V_{OUT} = 5V, V_{BUS} connected to GND, T_J = +25°C	6.5	8.5	10.5	s
		V_{OUT} = 5V, V_{BUS} connected to GND, T_J = -40°C to +125°C	6	8.5	11	
BC1.2 DCP Mode						
DP and DM short resistance	R_{DP/DM_Short}	V_{DP} = 0.8V, I_{DM} = 1mA, T_J = +25°C		125	155	Ω
		V_{DP} = 0.8V, I_{DM} = 1mA, T_J = -40°C to +125°C		125	160	
Divider Mode						
DP/DM output voltage	$V_{DP/DM\_Divider}$	V_{OUT} = 5V, T_J = +25°C	2.54	2.7	2.82	V
		V_{OUT} = 5V, T_J = -40°C to +125°C	2.5	2.7	2.85	
DP/DM output impedance	$R_{DP/DM\_Divider}$	T_J = +25°C	20	22	23	kΩ
		T_J = -40°C to +125°C	18	22	28	

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C(6). Typical value is tested at T_J = +25°C unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
1.2V/1.2V Mode						
DP/DM output voltage	$V_{DP/DM\_1.2V}$	V_{OUT} = 5V, T_J = +25°C	1.16	1.25	1.34	V
		V_{OUT} = 5V, T_J = -40°C to +125°C	1.15	1.25	1.35	
DP/DM output impedance	$R_{DP/DM\_1.2V}$	T_J = +25°C	60	68	75	kΩ
		T_J = -40°C to +125°C	55	68	88	

NOTES:

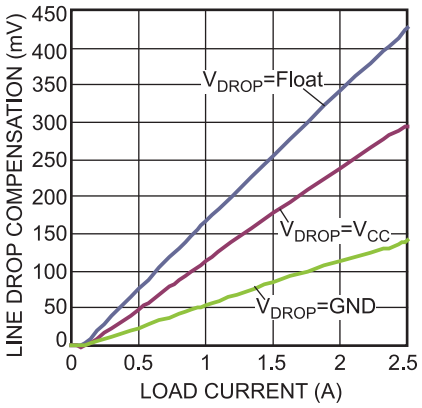
6) All min/max parameters are tested at T_J = 25°C. Limits over temperature are guaranteed by design, characterization, and correlation.

7) Guaranteed by design.

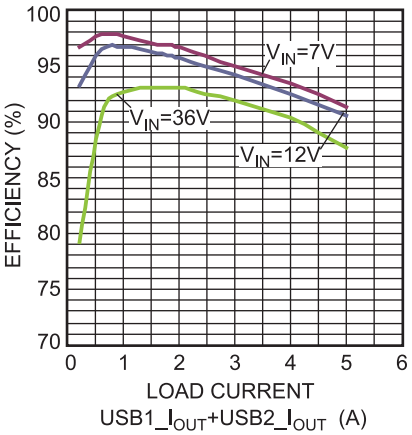
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 22µH, T_A = 25°C, unless otherwise noted.

Line Drop Compensation vs. Load Current

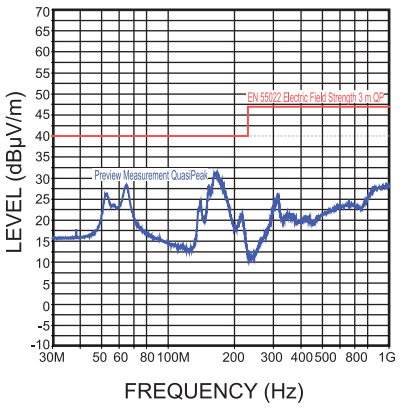


Efficiency vs. Load Current



Radiated EMI

V_{IN}=12V, f_S=150kHz, USB1_I_{OUT}=2.4A, USB2_I_{OUT}=2.4A, Quasi-Peak Detector

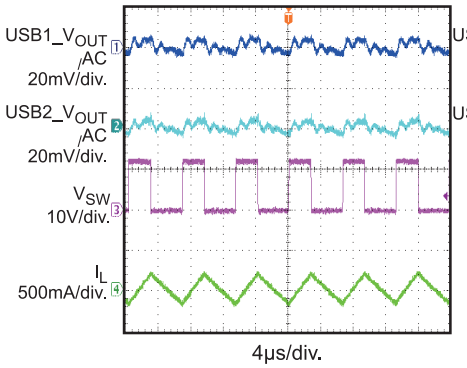


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 22µH, T_A = 25°C, unless otherwise noted.

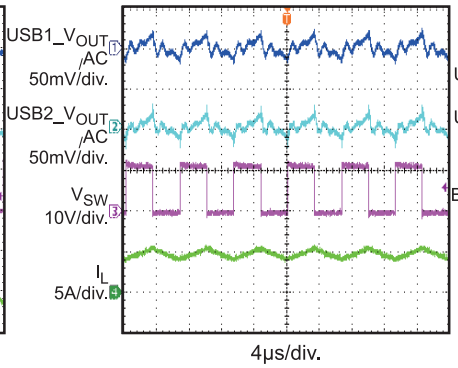
Output Ripple

V_{IN} = 12V, V_{OUT} = 5V,
USB1_I_{OUT} = USB2_I_{OUT} = 0A



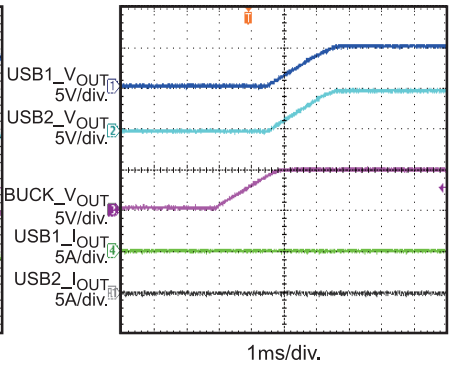
Output Ripple

V_{IN} = 12V, V_{OUT} = 5V,
USB1_I_{OUT} = USB2_I_{OUT} = 2.4A



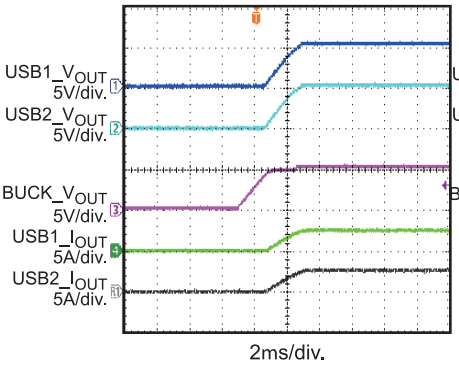
Power Start-Up

V_{IN} = 12V, V_{OUT} = 5V,
USB1_I_{OUT} = USB2_I_{OUT} = 0A



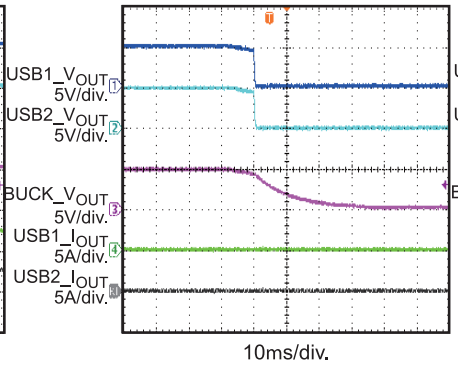
Power Start-Up

V_{IN} = 12V, V_{OUT} = 5V,
USB1_I_{OUT} = USB2_I_{OUT} = 2.4A,
CRL Load



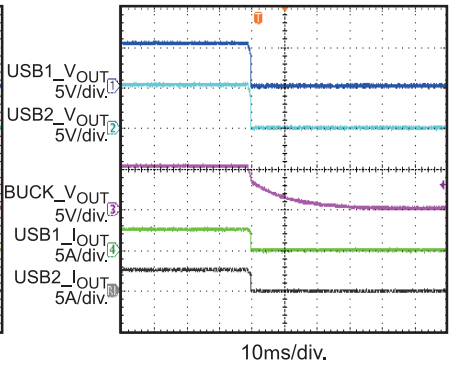
Power Shutdown

V_{IN} = 12V, V_{OUT} = 5V,
USB1_I_{OUT} = USB2_I_{OUT} = 0A

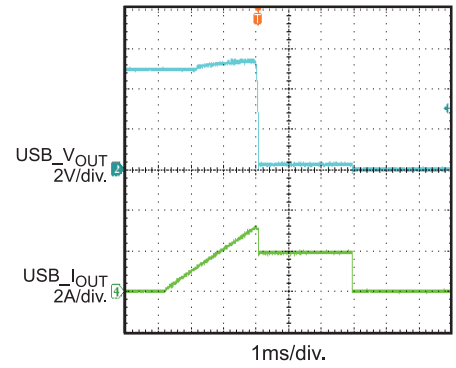


Power Shutdown

V_{IN} = 12V, V_{OUT} = 5V,
USB1_I_{OUT} = USB2_I_{OUT} = 2.4A,
CRL Load



USB Over-Current Protection



PIN FUNCTIONS

QFN 4x4 Pin #	Name	Description
1, 2	USB1	**USB1 output.**
3, 15, 25	OUT	**Buck output.** OUT is the power input for USB1 and USB2. The internal circuit senses OUT voltage and regulates it at 5V.
4, 14	IN	**Supply voltage.** The MP5402M operates from a 7V to 36V input voltage. C_{IN} prevents large voltage spikes at the input. Place C_{IN} as close to the IC as possible. IN is the drain of the internal power device and also provides the power supply for the entire chip.
5, 6, 12, 13	PGND	**Power ground.** PGND is the reference ground of the regulated output voltage. PGND requires extra care during PCB layout. Connect to GND with copper traces and vias.
7	FREQ	**Frequency selection.** Floating FREQ sets the frequency at 150kHz. Pulling FREQ to ground sets the frequency at 250kHz. Pulling FREQ to 5V sets the frequency at 350kHz.
8	EN	**On/off control input.**
9, 10, 26	SW	**Switch output.** Use a wide PCB trace to make the connection.
11	BST	**Bootstrap.** A 0.1μF capacitor is connected between SW and BST to form a floating supply across the high-side switch driver.
16, 17	USB2	**USB2 output.**
18	AGND	**Analog ground.** Connect AGND to PGND.
19	VCC	**Internal 5V LDO regulator output.** Decouple with a 0.22μF capacitor.
20	VDROP	**Line drop compensation selection.** Refer to the EC table for detailed specifications.
21	DM2	**D- data line to USB connector.** Input/output is used for handshaking with portable devices.
22	DP2	**D+ data line to USB connector.** Input/output is used for handshaking with portable devices.
23	DP1	**D+ data line to USB connector.** Input/output used for handshaking with portable devices.
24	DM1	**D- data line to USB connector.** Input/output is used for handshaking with portable devices.

FUNCTIONAL BLOCK DIAGRAM

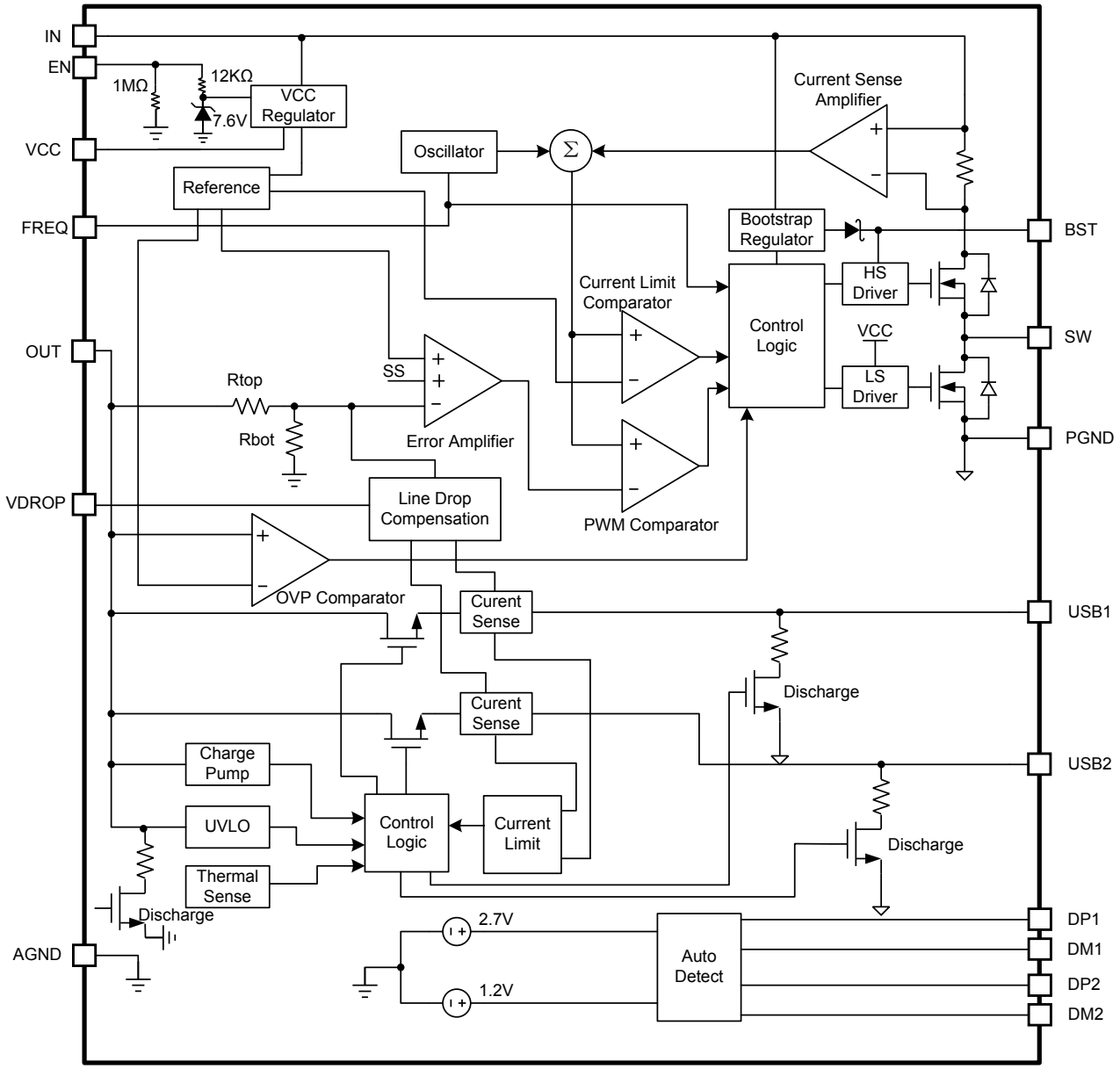


Figure 1: Functional Block Diagram

OPERATION

BUCK CONVERTER

The MP5402M integrates a monolithic, synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs and two USB current-limit switches with charging port auto-detection. It offers a compact solution to achieve 5A of continuous output current over a wide input supply range with excellent load and line regulation.

The MP5402M operates in a fixed frequency, peak-current-mode control to regulate the output voltage. The internal clock initiates the PWM cycle, which turns on the integrated high-side power MOSFET (HS-FET). The HS-FET remains on until its current reaches the value set by the COMP voltage. When the power switch is off, it remains off until the next clock cycle begins. If the duty cycle reaches 88% (350kHz switching frequency) in one PWM period, the current in the power MOSFET will not reach the COMP set current value, and the power MOSFET will turn off.

Error Amplifier (EA)

The error amplifier (EA) compares the internal feedback voltage against the internal 1V reference (REF) and outputs a COMP voltage. This COMP voltage controls the power MOSFET current. The optimized internal compensation network minimizes the external component count and simplifies the control loop design.

Internal VCC Regulator

The 5V internal regulator powers most of the internal circuitries. This regulator takes V_{IN} and operates in the full V_{IN} range. When V_{IN} exceeds 5.0V, the output of the regulator is in full regulation. If V_{IN} is less than 5.0V, the output decreases with V_{IN}. VCC requires an external 0.22µF ceramic decoupling capacitor.

Enable Control (EN)

The MP5402M has enable control (EN). Pulling EN high enables the IC; pulling EN low disables the IC. Connect EN to V_{IN} through a resistor for automatic start-up. An internal 1MΩ resistor from EN to GND allows EN to float to shut down the IC. EN is clamped internally using a 7.6V series Zener diode (see Figure 2). Connect EN through a pull-up resistor to any voltage connected to V_{IN}. This requires limiting the amplitude of the voltage source to below 10V and the EN input current to less than 230µA to prevent damage to the Zener diode.

For example, connecting 36V to V_{IN}, R_{PULLUP} ≥ (36V – 10V)/230µA = 113kΩ.

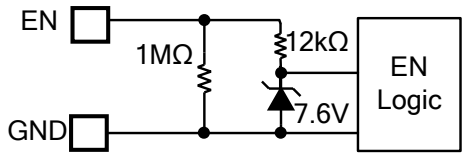


Figure 2: Zener Diode between EN and GND

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors the input voltage. The UVLO rising threshold is 5.7V, and its falling threshold is 4.7V.

Internal Soft Start (SS)

The soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates an SS voltage that ramps up from 0V to 5V. When SS is lower than REF, the error amplifier uses SS as the reference. When SS is higher than REF, the error amplifier uses REF as the reference. The SS time is set to 1.65ms internally.

If the output of the MP5402M is pre-biased to a certain voltage during start-up, the IC disables the switching of both the high-side and low-side switches until the voltage on the internal SS capacitor exceeds the internal feedback voltage.

Buck Over-Current Protection (OCP)

The MP5402M has a cycle-by-cycle, over-current limit when the inductor peak current exceeds the current-limit threshold, and FB voltage drops below the under-voltage (UV) threshold (70% below the reference, typically). Once UV is triggered, the MP5402M enters hiccup mode to restart the part periodically. This protection mode is especially useful when the output is dead-shorted to ground. This greatly reduces the average short-circuit current,

alleviates thermal issues, and protects the regulator. The MP5402M exits hiccup mode once the over-current condition is removed.

Buck Output Over-Voltage Protection (OVP)

The MP5402M has output over-voltage protection (OVP). If the output is higher than 6V, the high-side switch stops switching, and the low-side switch turns on to discharge the output voltage until the output decreases to 5.75V. The chip then returns to normal operation. If the output over voltage cannot be discharged to 5.75V, the low-side switch turns off after the inductor current reaches a negative current limit. The low-side switch turns on again when the next clock cycle begins.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. The UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by V_{IN} through D1, M1, C4, L1, and C2 (see Figure 3). If V_{BST}-V_{SW} exceeds 5V, U1 regulates M1 to maintain a 5V BST voltage across C4.

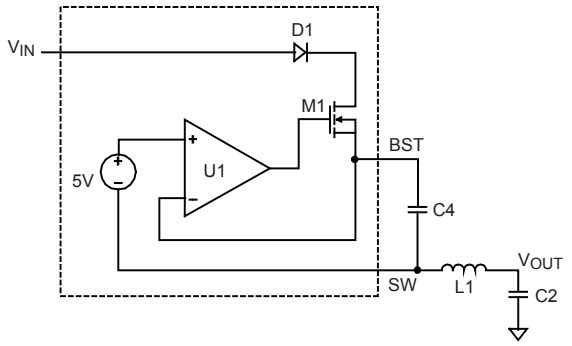


Figure 3: Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If both V_{IN} and EN exceed their respective thresholds, the chip is enabled. The reference block starts first, generating a stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Several events can shut down the chip: EN low, V_{IN} low, and thermal shutdown. In shutdown, the signaling path is blocked to avoid any fault triggering, and the COMP voltage and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command.

Buck Output Discharge

The buck portion of the device involves a discharge function that provides a resistive discharge path for the external output capacitor. The function is active when the part is disabled (input voltage is under UVLO, EN off) and is done in a very limited time. After VCC discharges below 1V, the buck output discharge resistor disconnects.

USB CURRENT-LIMIT SWITCH

Current-Limit Switch

The MP5402M integrates two USB current-limit switches. It provides a built-in soft-start circuitry, which controls the rising slew rate of the output voltage to limit the inrush current and voltage surges.

When the load current reaches the current-limit threshold (2.75A, typically), the USB power MOSFET switches into foldback current-limit mode, 70% of the current limit (see Figure 4). If the over-current limit condition lasts for more than 3ms, the USB channel enters hiccup mode with a 3ms on time and a 8.5s off time.

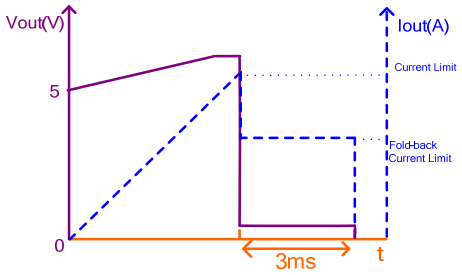


Figure 4: Over-Current Limit

During V_{IN} or EN start-up, ensure that the CC load current does not exceed 70% of the current limit to avoid triggering a foldback current limit and start-up failure.

Output Line Drop Compensation

The MP5402M can compensate an output-voltage drop—such as high impedance caused by a long trace—to keep a fairly constant 5V load-side voltage.

The internal comparator compares the current-sense output voltage of the two current-limit switches and uses the larger current-sense output voltage to compensate the line drop voltage.

Since the trace resistance is different for different cables, the MP5402M provides selectable line drop compensation through VDROP. The line drop compensation amplitude increases linearly as the load current increases; it also has an upper limitation.

USB Output Over-Voltage Protection

In order to protect the device at the cable terminal, each USB switch output has an independently dynamic over-voltage protection threshold. Based on different USB loading currents, the MP5402M adjusts the OVP threshold accordingly.

The intelligent line drop compensation and dynamic over-voltage protection control scheme ensure that the voltage at the cable terminal meets the 4.75V-5.25V specifications.

USB Output Discharge

Each USB portion involves a discharge function that provides a resistive discharge path for the external output capacitor. The function is active when the part is disabled (input voltage is under UVLO, EN off) and is done in a very limited time.

Auto Detection

The MP5402M integrates the USB dedicated charging port auto-detect function. This function recognizes most mainstream portable devices. It supports the following charging schemes:

- USB battery charging specification BC1.2/ Chinese telecommunications industry standard YD/T 1591-2009
- Divider mode
- 1.2V/1.2V mode

The auto-detect function is a state machine that supports all of the DCP charging schemes above.

SYSTEM

Thermal Shutdown (TSD)

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 165°C, the entire chip shuts down. When the temperature falls below its lower threshold (145°C, typically), the chip is enabled.

APPLICATION INFORMATION

COMPONENT SELECTION

Selecting the Inductor

For most applications, an inductor with a DC current rating at least 25% higher than the maximum load current is recommended. Select an inductor with small DC resistance for optimum efficiency. The inductor value for most designs can be derived from Equation (1):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (1)$$

Where ΔI_L is the inductor ripple current.

Set the inductor ripple current to approximately 30% of the maximum load current. The maximum inductor peak current is shown in Equation (2):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (2)$$

Typically, 22μH inductance is recommended to improve EMI.

Selecting the Buck Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply the AC current while maintaining the DC input voltage. Use low ESR capacitors for optimum performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For a CLA application, a 100μF electrolytic capacitor and two 10μF ceramic capacitors are recommended.

Since the input capacitor (C1) absorbs the input switching current, it requires an adequate ripple-current rating. The RMS current in the input capacitor can be estimated with Equation (3):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (3)$$

The worse case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (4):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (4)$$

For simplification, choose an input capacitor with an RMS current rating of greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using an electrolytic capacitor, place two additional high-quality ceramic capacitors as close to V_{IN} as possible. Estimate the input voltage ripple caused by the capacitance with Equation (5):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (5)$$

Selecting the Buck Output Capacitor

The device requires an output capacitor (C2) to maintain the DC output voltage. Estimate the output voltage ripple with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (6)$$

Where L_1 is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For an electrolytic capacitor, ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (7)$$

The characteristics of the output capacitor affect the stability of the regulatory system. A low ESR electrolytic capacitor is recommended for a low output ripple and good control loop stability. For a CLA application, a 1μF ceramic capacitor and a 270μF polymer/electrolytic capacitor with ~20mΩ ESR are recommended.

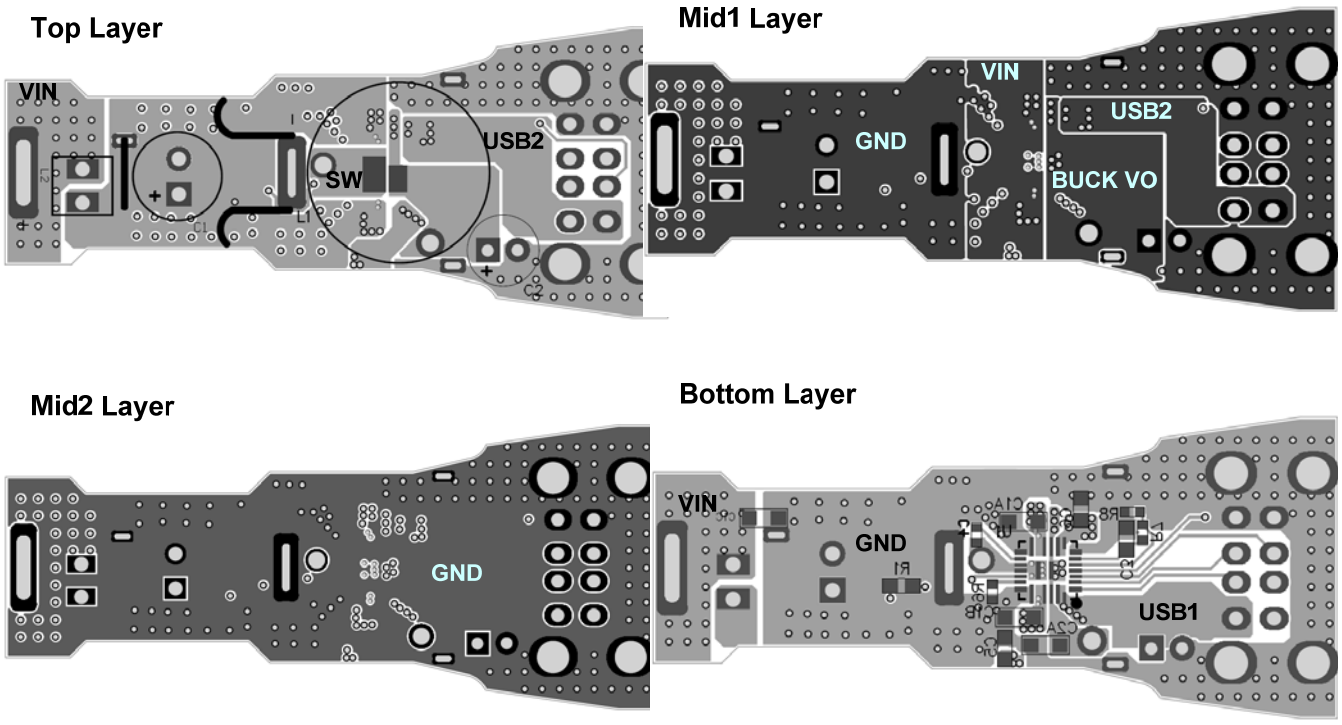
PCB Layout Guidelines[8]

Efficient PCB layout is critical for achieving stable operation and thermal dissipation. For best results, refer to Figure 5 and follow the guidelines below:

1. Use short, direct, and wide traces to connect OUT. Adding vias under the IC and routing the OUT trace on both PCB layers is highly recommended.
2. Use a large copper plane for PGND. Add multiple vias to improve thermal dissipation.
3. Connect AGND to PGND.

4. Use a large copper plane for SW, USB1, and USB2.
5. Route the USB1 and USB2 traces on both PCB layers.
6. Add multiple vias.
7. Place two ceramic input decoupling capacitors as close as possible to IN and PGND to improve EMI performance.
8. Place a VCC decoupling capacitor as close as possible to VCC.

NOTE:
8) The recommended layout is based on the typical application circuit on the next page (see Figure 6) .



(4.78cm x 1.38cm)

For CLA application (4 layer), 2Oz per layer PCBA is recommended

Figure 5: PC Board Layout

TYPICAL APPLICATION CIRCUITS

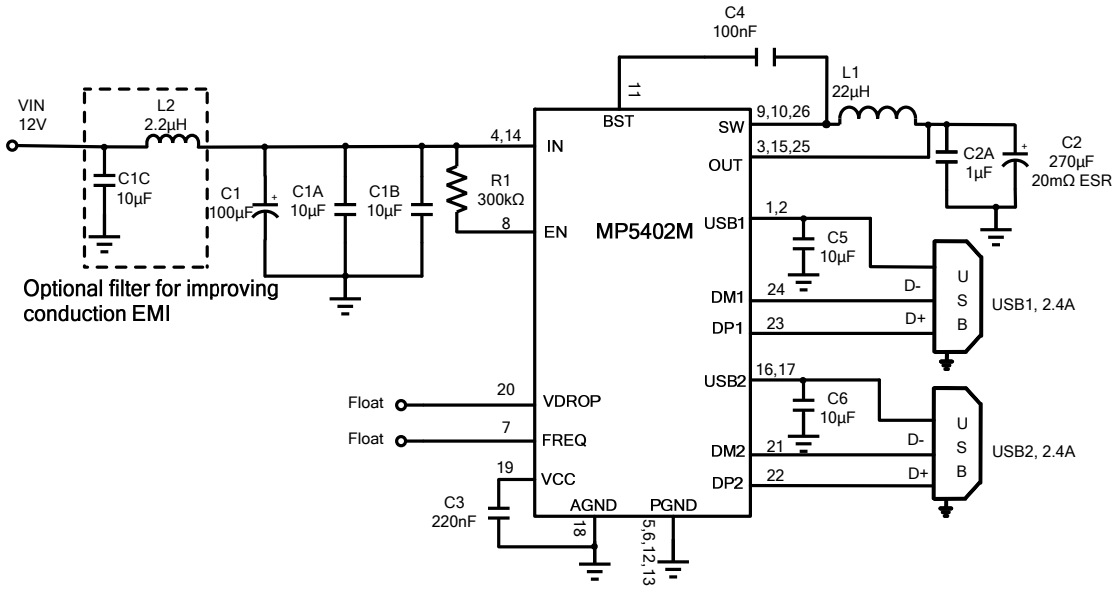
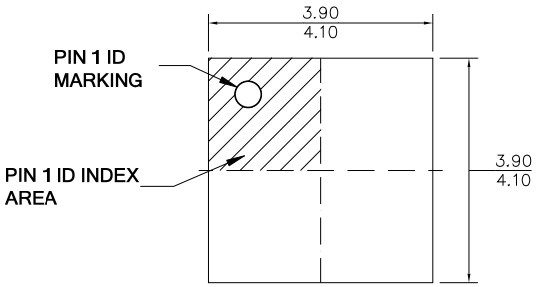


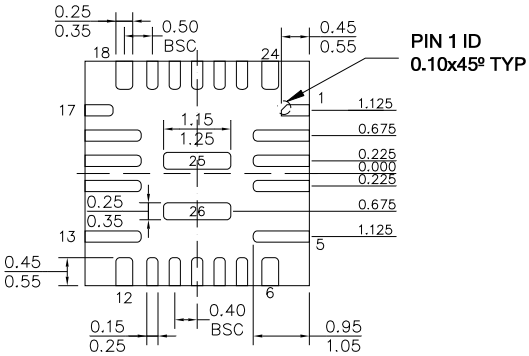
Figure 6: USB1 = 5V/2.4A, USB2 = 5V/2.4A

PACKAGE INFORMATION

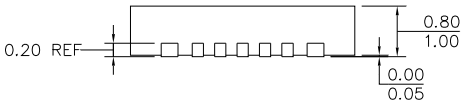
QFN-26 (4mmx4mm)



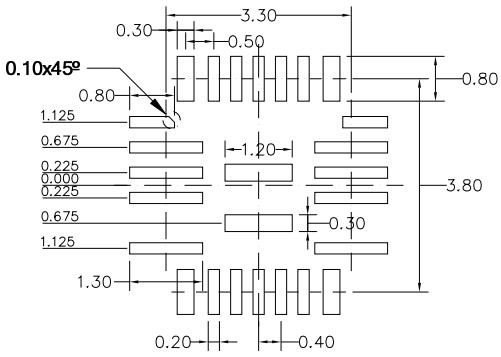
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.