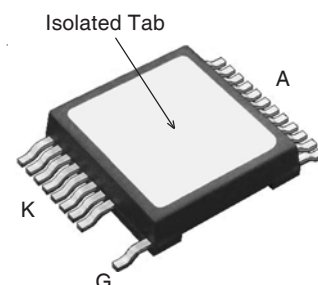
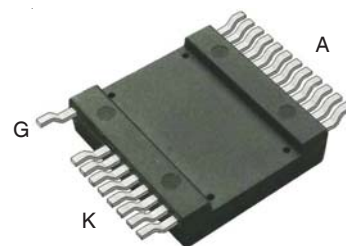


1500V MOS Gated Thyristor w/ Anti-Parallel Diode

MMIX1H60N150V1

 $V_{DM} = 1500V$

(Electrically Isolated Tab)



G = Gate
A = Anode

K = Cathode

Symbol	Test Conditions	Maximum Ratings	
V_{DM}	$T_J = 25^\circ\text{C to } 150^\circ\text{C}$	1500	V
V_{GK}	Continuous	± 30	V
V_{GK}	Transient	± 40	V
I_{TSM}	$T_C = 25^\circ\text{C}, 1\mu\text{s}$	32.0	kA
	$T_C = 25^\circ\text{C}, 10\mu\text{s}$	11.8	kA
P_D	$T_C = 25^\circ\text{C}$	446	W
T_J		-55 ... +150	$^\circ\text{C}$
T_{JM}		150	$^\circ\text{C}$
T_{stg}		-55 ... +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering	300	$^\circ\text{C}$
T_{SOLD}	1.6 mm (0.062 in.) from Case for 10s	260	$^\circ\text{C}$
V_{ISOL}	50/60Hz, 1 minute	2500	V~
F_C	Mounting Force	50..200/11..45	N/lb
Weight		8	g

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
V_{BR}	$I_A = 250\mu\text{A}, V_{GK} = 0V$	1500		V
$V_{GK(th)}$	$I_A = 250\mu\text{A}, V_{AK} = V_{GK}$	2.5		5.0 V
V_T	$I_T = 1000A, V_{GK} = 15V$		4.6	6.0 V
r_T	$I_T > I_L, V_{GK} = 15V$		1.2	m Ω
V_{BO}	$V_{GK} = 15V$		4.8	V
I_D	$V_{AK} = 1500V, V_{GK} = 0V$ $T_J = 125^\circ\text{C}$			15 μA 1.5 mA
I_L			400	A
I_H			350	A
I_{GKS}	$V_{AK} = 0V, V_{GK} = \pm 30V$			± 200 nA

Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Mounting Surface
- Anti-Parallel Diode
- 2500V~ Electrical Isolation
- Very High Current Capability

Advantages

- High Power Density
- Low Gate Drive Requirement

Applications

- Capacitive Discharge Circuits
- Ignition Circuits
- Solid State Surge Protection

Symbol Test Conditions

($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)

Characteristic Values

Min. Typ. Max.

C_{iks}	$V_{AK} = 25V, V_{GK} = 0V, f = 1\text{MHz}$	5120	pF
C_{oks}		340	pF
C_{rks}		84	pF
$Q_{g(on)}$	$I_C = 60A, V_{GK} = 15V, V_{AK} = 600V$	180	nC
Q_{gk}		33	nC
Q_{ga}		62	nC
t_{ri}	Capacitive Discharge, $T_J = 25^\circ\text{C}$ $I_A = 2000A, V_{GK} = 15V, R_G = 1\Omega$ $V_{AK} = 1000V, L < 20\text{nH}$, Notes 2 & 3	100	ns
t_d		50	ns
t_{ri}	Capacitive Discharge, $T_J = 125^\circ\text{C}$ $I_A = 2000A, V_{GK} = 15V, R_G = 1\Omega$ $V_{AK} = 1000V, L < 20\text{nH}$, Notes 2 & 3	100	ns
t_d		50	ns
R_{thJC}	0.05	0.28	$^\circ\text{C/W}$
R_{thCS}			$^\circ\text{C/W}$
R_{thJA}		19	$^\circ\text{C/W}$

Reverse Diode (FRED)

Symbol Test Conditions

($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)

Characteristic Values

Min. Typ. Max.

V_F	$I_F = 100A, V_{GK} = 0V$, Note 1		1.8 V
I_{RM}	$I_F = 50A, V_{GK} = 0V$, $-di_F/dt = 200A/\mu\text{s}, V_R = 300V$	20	A
t_{rr}		700	ns
R_{thJC}			0.50 $^\circ\text{C/W}$

Notes:

1. Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.
2. It is recommended to use a gate driver capable of supplying more than 4Amps and $\geq 15V$ gate voltage.
3. Refer to fig. 9 & 10.

PRELIMINARY TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:

4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
4,860,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

Fig. 1. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

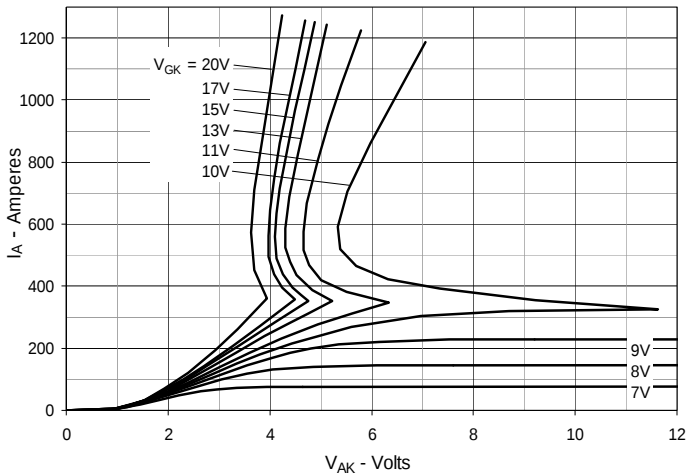


Fig. 2. Extended Output Characteristics @ $T_J = 125^\circ\text{C}$

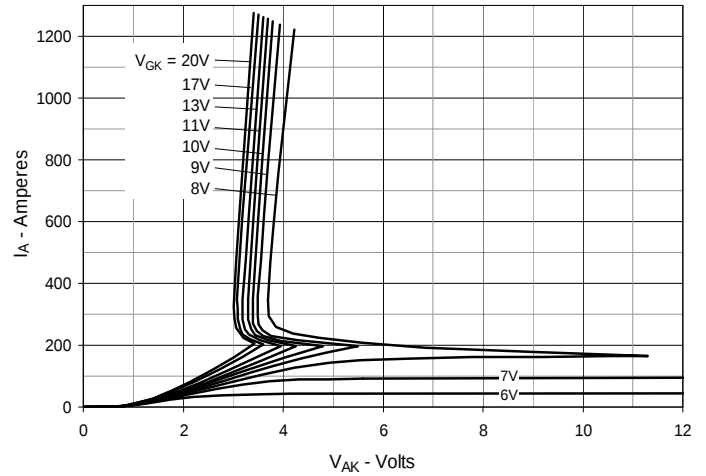


Fig. 3. Extended Output Characteristics @ $T_J = -40^\circ\text{C}$

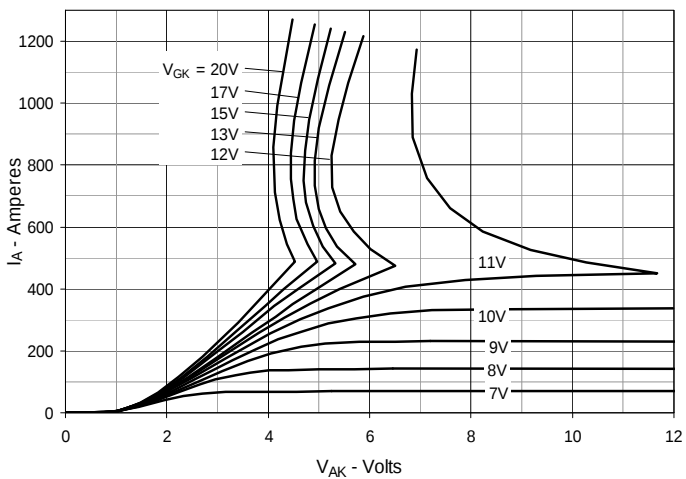


Fig. 4. Gate Charge

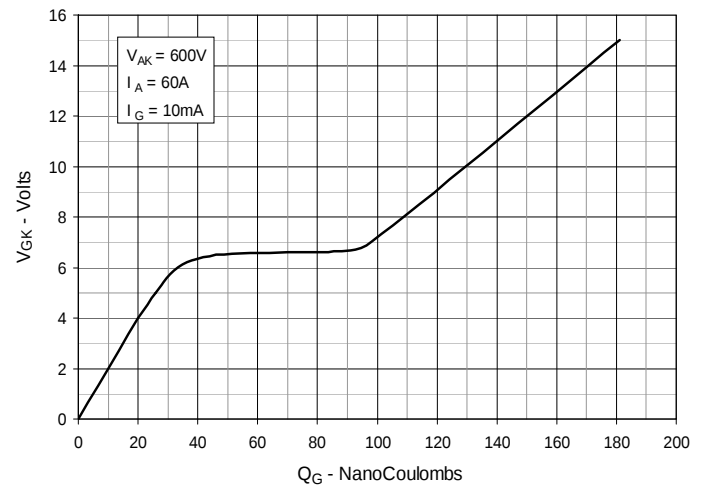


Fig. 5. Capacitance

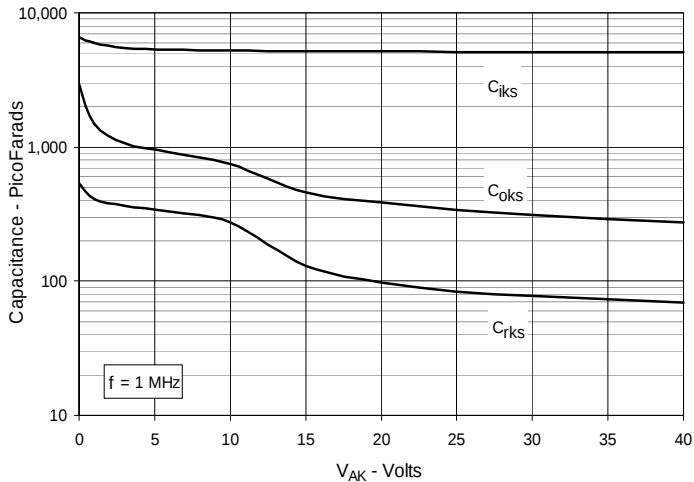


Fig. 6. Forward Voltage Drop of Intrinsic Diode

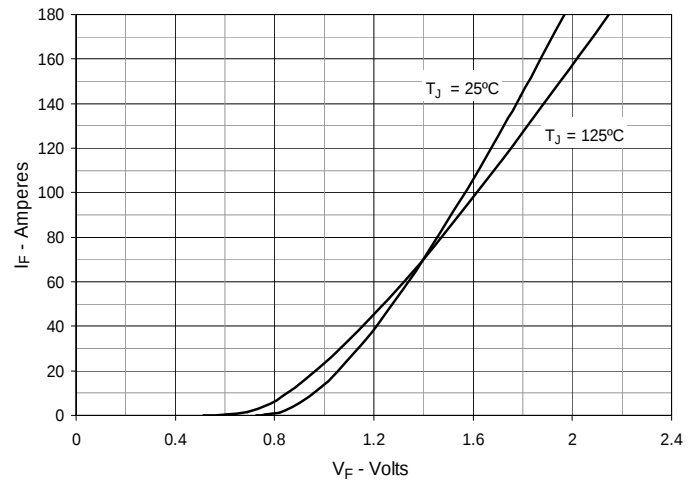


Fig. 7. Maximum Transient Thermal Impedance

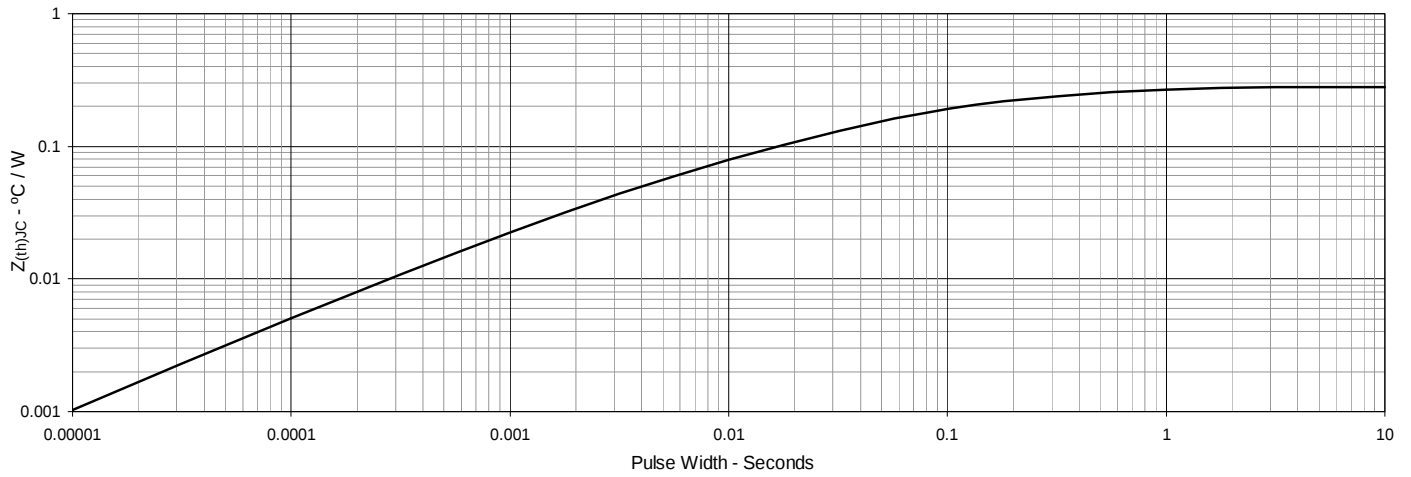
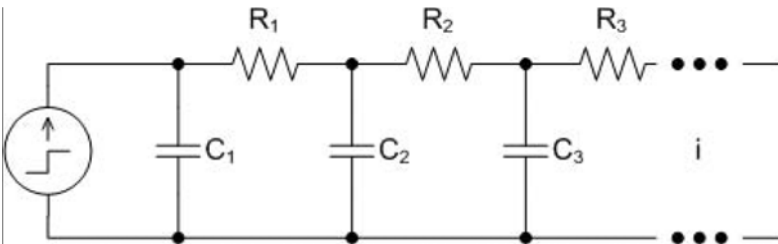


Fig. 8. Cauer Thermal Network



i	R_i (Ω)	C_i (F)
1	0.018327	0.024851
2	0.052439	0.058268
3	0.099100	0.208110
4	0.048364	4.000000

Fig. 9. Capacitive Discharge Circuit

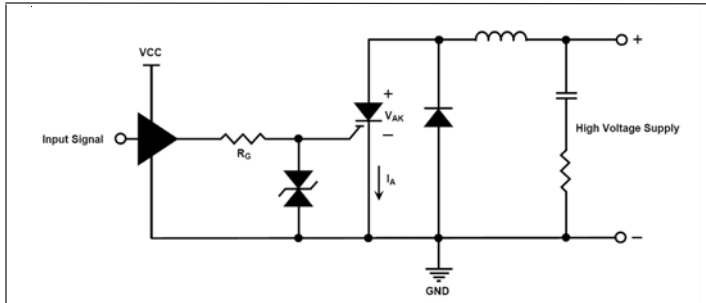
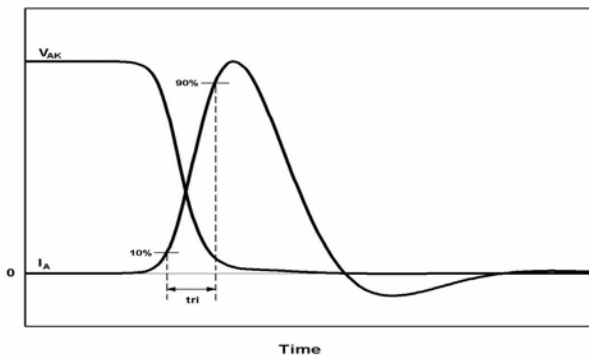
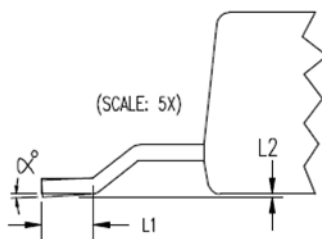
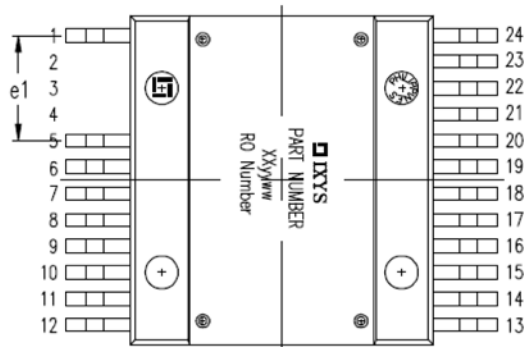
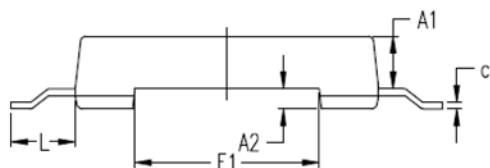
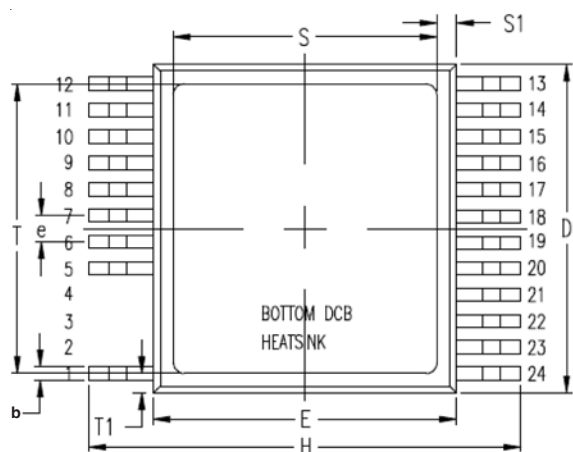


Fig. 10. Capacitive Discharge Waveform





PIN: 1 = Gate
5-12 = Cathode
13-24 = Anode

Dim.	Millimeter		Inches	
	min	max	min	max
A	5.30	5.70	0.209	0.224
A1	3.90	4.10	0.154	0.161
A2	1.40	1.60	0.055	0.063
b	0.90	1.15	0.035	0.045
c	0.45	0.65	0.018	0.026
D	24.80	25.25	0.976	0.994
E	22.80	23.25	0.898	0.915
E1	13.80	14.20	0.543	0.559
e	2.00	BSC	0.079	BSC
e1	8.00	BSC	0.315	BSC
H	32.30	33.30	1.272	1.311
L	4.60	5.30	0.181	0.209
L1	1.30	1.70	0.051	0.067
L2	0.00	0.15	0.000	0.006
S	18.85	20.12	0.742	0.792
S1	1.45	2.08	0.057	0.082
T	20.90	22.17	0.823	0.873
T1	1.42	2.03	0.056	0.080
a	4°	-	4°	-



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