MLKHN1501

Fully compliant IEEE 1901 HD-PLC Power line Communications (PLC) IC with “Multi-hop”

Preliminary Datasheet

KDS-HANFF03EAA

Rev. 1.0.0

MegaChips

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Contents

Revision History

Date	Revision	Changes
2016/8/5	0.2.0	Initial Release
2016/8/26	0.3.0	Modified the errors in pinout table in Figure 2: Pinout / page 9 Unified the word “Turbo-MII” into TMII and added the description “TMII (Turbo-MII)” in page 9 Modified the errors and K_SDCKE, K_SDCSN description in Table 3: List of SDRAM Connection Pins / page 10 Added VDD33_K’s explanation in Table 14: List of Power Supply and VSS Pins / page 15 Added VDD33_K’s Absolute maximum ratings and modified parameters description in Table 16: Absolute Maximum Ratings / page 16 Modified AGCGAIN to REVISION in Section 4.9.1 Special Pin Settings / page 28 Modified D12VDD to CVDD in Section 5.2 Specifications Removed “4.2.5 SDRAM Interface Functions” Removed “Figure- 8 SDRAM Connection Pins Timing Chart” Removed “KS8721BL”, “KSZ8051MNL” from recommended device in Section 8.2 Ethernet PHY Specifications / page 9
2016/9/12	0.4.0	Editorial changes
2016/9/26	0.4.1	Modified package name to “LBGA 238 pin” / page 5
2016/11/16	0.5.0	Modified the description about TXC, RXC, COL, CRS in Table 2: List of Ethernet Connection Pins / page 9 Changed from Tc to Ambient temperature in Table 17: Power Supply Specifications/ page 19
2016/12/01	0.6.0	Editorial changes
2017/01/20	0.7.0	Modified 1.1 Function overview
2017/02/16	0.8.0	Modified 3.2 Power supply specifications Modified Allowable deviation of Oscillation
2017/02/17	0.8.1	Editorial changes
2017/02/21	0.8.2	Remove table 32
2017/03/01	0.8.3	Add power consumption value Add refresh cycle of SDRAM
2017/03/23	0.8.5	Change order number typo “MLMLKHNxxx” to “MLKHNxxx”
2017/03/28	1.0.0	Official release version

1. Product Overview

1.1. Function Overview

MegaChips MLKHN1501 is a state-of-the-art single-chip broadband over power line (BPL) solution based on IEEE 1901 standard (HD-PLC). It delivers bi-directional, IP based, high-speed communication over AC/DC power lines, COAX and twisted pair wiring where wider bandwidths, robustness, long-range, support for larger number of nodes, and highly secure network is required.

The highly integrated MLKHN1501 combines the physical (PHY) and media access control (MAC) layers using an ARM946E microcontroller, 128Mbit (MLKHN1501A) or 256Mbit SDRAM (MLKHN1501B), UART, MII/RMII, and integrated analog-front-end (AFE) in a single compact package to reduce cost, size and complexity.

The MLKHN1501 uses a high-performance wavelet conversion OFDM modulation and advanced forward error correction (FEC) schemes to enable robust data communication using the existing electrical lines. With 432 sub-carriers in the 2 MHz - 28 MHz operating frequency band, the MLKHN1501 provides a maximum PHY rate of 240Mbps. A channel estimation technique is used to determine the optimal data rate according to the power line channel characteristics with the multi-level modulation for each sub-carrier. Optional sub-carrier masking function is adapted to meet individual country's regulations.

The MLKHN1501 uses ITU-T G.9905, Centralized Matrix based Source Routing (CMSR) mechanism designed specifically to improve robustness, extended range, and wider coverage, while putting minimum load on the network. The multi-hop functionality extends the communication range up to 10 time. In addition, it uses a 128-bit AES encryption engine for the highest security at every node meeting today’s Internet-of-Things (IoT) requirements.

1.1.1. Key Features

- Support multi-hop up to 10-hops
- Supports up to 1024 nodes on a single network
- HD-PLC/Ethernet bridge functionality
- Supports IPv4/IPv6 internet protocol
- Lowest power in the industry
- On-chip PLL multiplier and synthesizer provides a single clock source

- Network construction and optimization
- Advanced network diagnostics and management
- HD-PLC network bridge function compatible with Ethernet address system.
- Ethernet⇔Ethernet, RS485⇔RS485 bridge function
- Industrial operating temperature (-40°C to +85°C)
- Package LBGA 238pin (15 mm x 18 mm)
- Meets EN50561-1 EMC regulations

1.1.2. Applications

- Smart Grid/AMI/Solar/EV
- Smart Cities/Outdoor, Public Lighting
- Smart Buildings/HVAC/Backbone
- Security/Video-Entry Systems
- Surveillance Cameras
- Industrial Automation (M2M)

1.2. Block Diagram

The figure below is a block diagram of the MLKHN1501.

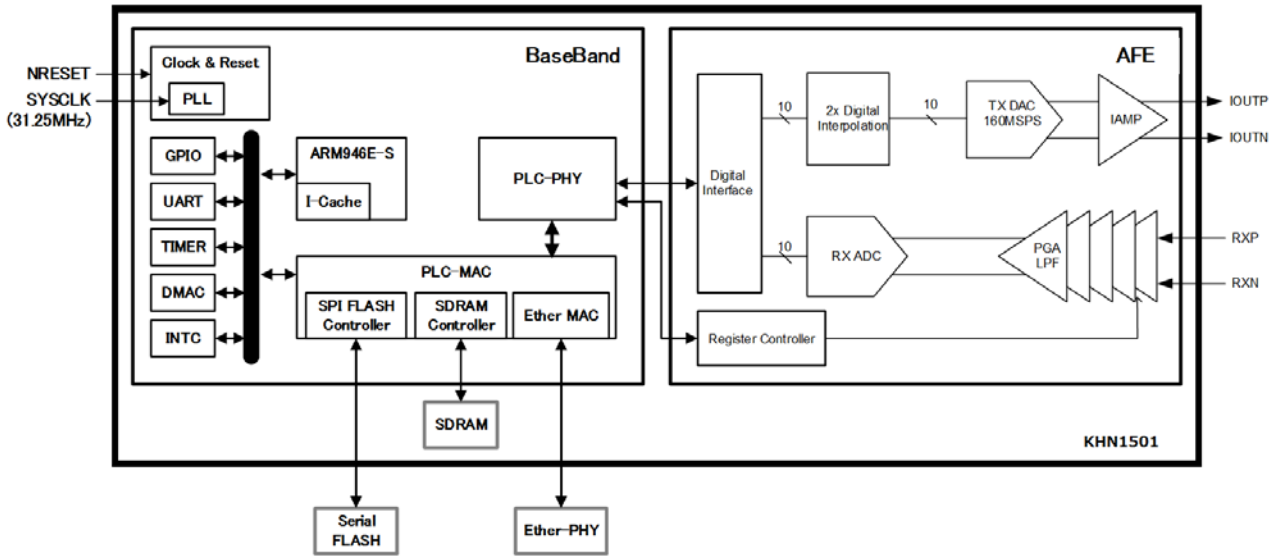


Figure 1: MLKHN1501 Block Diagram

2. Pins

2.1. Pinout

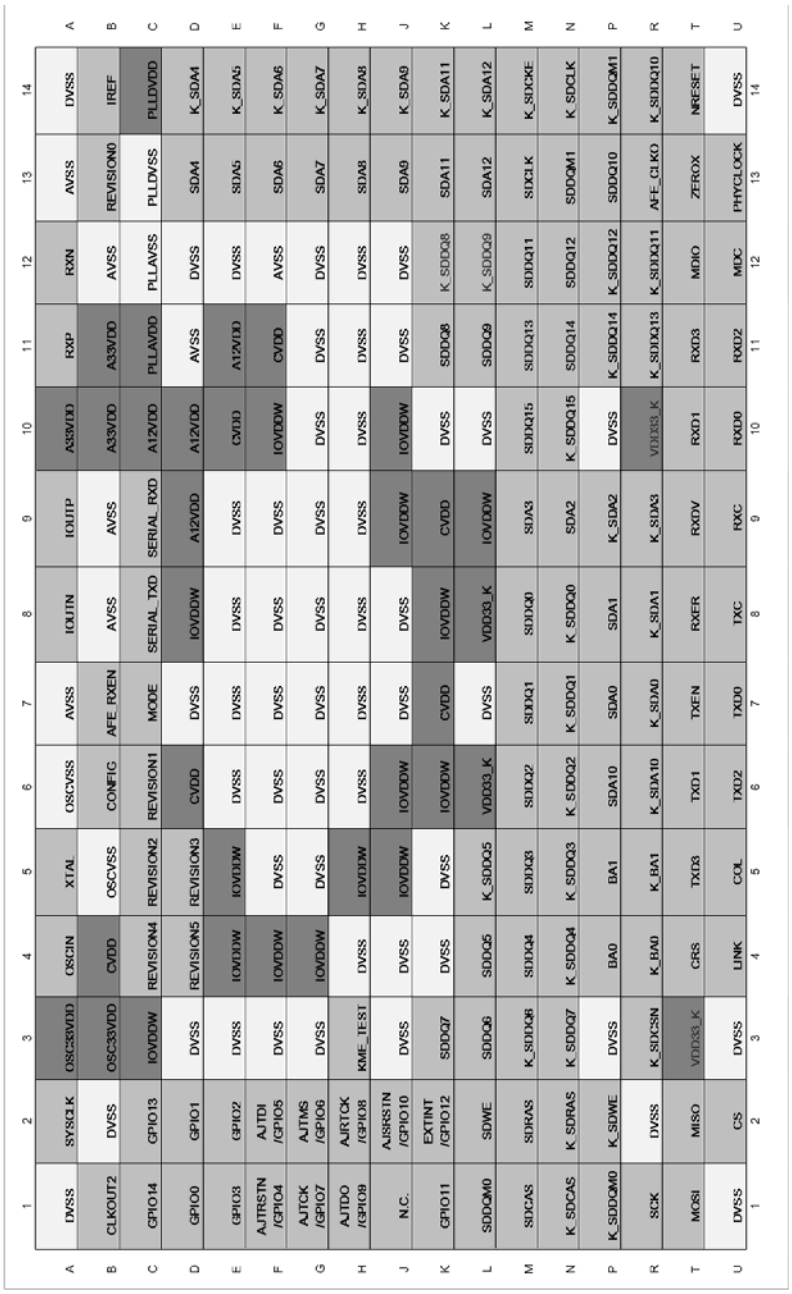


Figure 2: Pinout

2.2. Pin Descriptions

This section describes the MLKHN1501's pins. In the pin list, initial values for pins are given as “RST initial value”, and "---" indicates that the initial values are undefined since those pins are inputs in the initial state (following reset de-assertion). “Pull-up/Pull-down” column shows internal PU/PD information.

Pins names that are followed by "(shared)" are shared pins and are not shown in the pinout.

Pin name which are marked with (*) are 5V Tolerant.

2.2.1. Analog Front-end Connection Pins

The table below shows a list of analog front-end connection pins.

Table 1: List of Analog Front-end Connection Pins

No.	Pin Name	I/O	RST Initial Value	Pull-up/ Pull-down	Description
R13	AFE_CLKO	O	Low	---	A/D / D/A sampling clock output.(62.5MHz)
B7	AFE_RXEN (*)	O	Low	Pull-down	Active high receive enable output.

2.2.2. Ethernet Connection Pins

The MLKHN1501's Ethernet connection pins comply with MII and RMII specifications and also support TMII (Turbo-MII) specification. Register settings can be used to select the desired specification set.

The table below shows a list of Ethernet connection pins.

Table 2: List of Ethernet Connection Pins

No.	Pin Name	I/O	RST Initial Value	Pull-up/ Pull-down	Description
U7	TXD0	O	Low	---	When MII/TMII is selected, act as 4-bit transmission data output. When RMII is selected, TXD0 and TXD1 act as 2-bit transmission data output pins. Do not connect anything to TXD2 or TXD3 in this configuration.
T6	TXD1		Low	---	
U6	TXD2		Low	---	
T5	TXD3		Low	---	

No.	Pin Name	I/O	RST Initial Value	Pull-up/ Pull-down	Description
T7	TXEN	O	Low	---	Active high transmission data enable output.
U8	TXC (*)	I	---	---	Transmission clock input. When RMII is selected and connects w/ Ether PHY LSI, Pull-down resistor is required externally.
U10	RXD0 (*)	I	---	---	When MII/TMII is selected, act as 4-bit receive data input. When RMII is selected, RXD0 and RXD1 act as 2-bit receive data input. RXD2 and RXD3 act as monitor pins as described below: RXD2 : 10M/100M communications mode information RXD3 : LINK status
T10	RXD1 (*)		---	---	
U11	RXD2 (*)		---	---	
T11	RXD3 (*)		---	---	
T9	RXDV (*)	I	---	---	Active high receive data valid input. When RMII is selected, connect to the Ether PHY LSI's CRS_DV pin.
U9	RXC (*)	I	---	---	Receive clock input. When RMII is selected and connects w/ Ether PHY LSI, Pull-down resistor is required externally.
T8	RXER (*)	I	---	---	Active high receive error indicator input.
U5	COL (*)	I	---	Pull-down	Active high collision detection input. Not used when RMII is selected. Requires pull-down.
T4	CRS (*)	I	---	Pull-down	Active high carrier sense input. Not used when RMII is selected. Requires pull-down.
T12	MDIO (*)	IO	---	Pull-down	Control data input/output.
U12	MDC	O	Low	---	Control data clock output.
U13	PHYCLOCK	O	Low	---	Acts as the Ethernet clock output. The clock precision is the same as for the clock input to the SYSCLK pin. When MII is selected, outputs 25MHz. When RMII, TMII are selected, outputs 50MHz.
U4	LINK (*)	I	---	Pull-up	Acts as the link state input. For more information about the pin level (indicating the presence of the link state), see the specifications for the EtherPHY LSI to which the pin will be connected. A toggle signal indicates that communications are in progress.

2.2.3. SDRAM Connection Pins

The table below shows a list of SDRAM connection pins, which are supposed to connect to internal SDRAM externally. These pins are used in MP test only.

Table 3: List of SDRAM Connection Pins

No.	Pin Name	I/O	RST Initial Value	Pull-up/ Pull-down	Connected SDRAM Pin No.	Connected SDRAM Pin Name	Description

No.	Pin Name	I/O	RST Initial Value	Pull-up/ Pull-down	Connected SDRAM Pin No.	Connected SDRAM Pin Name	Description
M8	SDDQ0	IO	---	---	N8	K_SDDQ0	16-bit data bus input/output for SDRAM.
M7	SDDQ1		---	---	N7	K_SDDQ1	
M6	SDDQ2		---	---	N6	K_SDDQ2	
M5	SDDQ3		---	---	N5	K_SDDQ3	
M4	SDDQ4		---	---	N4	K_SDDQ4	
L4	SDDQ5		---	---	L5	K_SDDQ5	
L3	SDDQ6		---	---	M3	K_SDDQ6	
K3	SDDQ7		---	---	N3	K_SDDQ7	
K11	SDDQ8		---	---	K12	K_SDDQ8	
L11	SDDQ9		---	---	L12	K_SDDQ9	
P13	SDDQ10		---	---	R14	K_SDDQ10	
M12	SDDQ11		---	---	R12	K_SDDQ11	
N12	SDDQ12		---	---	P12	K_SDDQ12	
M11	SDDQ13		---	---	R11	K_SDDQ13	
N11	SDDQ14		---	---	P11	K_SDDQ14	
M10	SDDQ15		---	---	N10	K_SDDQ15	
P7	SDA0	O	Low	---	R7	K_SDA0	13-bit address bus output for SDRAM.
P8	SDA1		Low	---	R8	K_SDA1	
N9	SDA2		Low	---	P9	K_SDA2	
M9	SDA3		Low	---	R9	K_SDA3	
D13	SDA4		Low	---	D14	K_SDA4	
E13	SDA5		Low	---	E14	K_SDA5	
F13	SDA6		Low	---	F14	K_SDA6	
G13	SDA7		Low	---	G14	K_SDA7	
H13	SDA8		Low	---	H14	K_SDA8	
J13	SDA9		Low	---	J14	K_SDA9	
P6	SDA10		Low	---	R6	K_SDA10	
K13	SDA11		Low	---	K14	K_SDA11	
L13	SDA12		Low	---	L14	K_SDA12	
P4	BA0	O	Low	---	R4	K_BA0	Bank address output for SDRAM.
P5	BA1		Low	---	R5	K_BA1	
M13	SDCLK	O	Low	---	N14	K_SDCLK	SDRAM transfer clock output.
M2	SDRAS	O	High	---	N2	K_SDRAS	Bank select / row address strobe output.
M1	SDCAS	O	High	---	N1	K_SDCAS	Command select / column address strobe output.

No.	Pin Name	I/O	RST Initial Value	Pull-up/ Pull-down	Connected SDRAM Pin No.	Connected SDRAM Pin Name	Description
L2	SDWE	O	High	---	P2	K_SDWE	Write enable output.
L1	SDDQM0	O	Low	---	P1	K_SDDQM0	Data mask control output.
N13	SDDQM1	O	Low	---	P14	K_SDDQM1	
-	-	-	-	---	M14	K_SDCKE	SDRAM Clock Enable, **Tied to 3.3V externally**
-	-	-	-	---	R3	K_SDCSN	SDRAM Chip Select, **Tied to GND externally**

2.2.4. Serial Flash Connection Pins

The table below shows a list of serial flash connection pins.

Table 4: List of Serial Flash Connection Pins

No.	Pin Name	I/O	RST Initial Value	Pull-up/ Pull-down	Description
U2	CS	O	High	---	Chip select output.
T2	MISO (*)	I	---	Pull-down	Serial data input.
R1	SCK	O	Low	---	Serial clock output. (50MHz)
T1	MOSI (*)	O	Low	Pull-down	Serial data output

2.2.5. Serial Communication Connection Pins

The table below shows a list of serial communication connection pins.

Table 5: List of Serial Communications Connection Pins

No.	Pin Name	I/O	RST Initial Value	Pull-up/ Pull-down	Description
C9	SERIAL_RXD (*)	I	---	Pull-up	Serial data input.
C8	SERIAL_TXD (*)	O	Low	---	Serial data output.

2.2.6. General-purpose Ports

The table below shows a list of general-purpose ports.

Table 6: List of General-purpose ports

No.	Pin Name	I/O	RST Initial Value	Pull-up/ Pull-down	Description
D1	GPIO0 (*)	IO	---	Pull-down	General-purpose port.
D2	GPIO1 (*)	IO	---	Pull-down	General-purpose port.
E2	GPIO2 (*)	IO	---	Pull-down	General-purpose port.
E1	GPIO3 (*)	IO	---	Pull-down	General-purpose port.
F1	GPIO4 (*)	IO	---	Pull-up	General-purpose port. (*1) Shared with AJTRSTN pin.
F2	GPIO5 (*)	IO	---	Pull-up	General-purpose port. (*1) Shared with AJTDI pin.
G2	GPIO6 (*)	IO	---	Pull-up	General-purpose port. (*1) Shared with AJTMS pin.
G1	GPIO7 (*)	IO	---	Pull-up	General-purpose port. (*1) Shared with AJTCK pin.
H2	GPIO8 (*)	IO	---	Pull-up	General-purpose port. (*1) Shared with AJRTCK pin.
H1	GPIO9 (*)	IO	---	Pull-up	General-purpose port. (*1) Shared with AJTDO pin.
J2	GPIO10 (*)	IO	---	Pull-up	General-purpose port. (*1) Shared with AJSRSTN pin.
K1	GPIO11 (*)	IO	---	Pull-up	General-purpose port.
K2	GPIO12 (*)	IO	---	Pull-up	General-purpose port. (*2) Shared with EXTINT pin.
C2	GPIO13 (*)	IO	---	Pull-up	General-purpose port.
C1	GPIO14 (*)	IO	---	Pull-up	General-purpose port.
J1	N.C.	-	---	---	(Not Connected). Leave this pin open.

Note: In normal mode, all ports are configured as input ports.

**1 : When ICE mode is selected, acts as the ICE JTAG pin.*

**2 : Enabled by register settings.*

2.2.7. CPU Peripheral Connection Pin

The table below shows a list of CPU peripheral connection pin.

Table 7: List of CPU Peripheral Connection Pin

No.	Pin Name	I/O	RST Initial Value	Pull-up/ Pull-down	Description
K2	EXTINT (*)	I	---	Pull-up	Active Low external interrupt input. * Shared with GPIO12.

2.2.8. AC Synchronous Detection Pin

The table below shows a list of AC synchronous detection pin.

Table 8: List of AC Synchronous Detection Pin

No.	Pin Name	I/O	RST Initial Value	Pull-up/ Pull-down	Description
T13	ZEROX (*)	I	---	Pull-up	AC synchronous detection input.

2.2.9. Clock and Reset Pins

The table below shows a list of clock and reset connection pins.

Table 9: List of Clock and Reset Connection Pins

No.	Pin Name	I/O	RST Initial Value	Pull-up/ Pull-down	Description
A2	SYSCLK (*)	I	---	---	System clock input. (31.25MHz)
A5	XTAL	O	---	---	Crystal Oscillator Inverter Output
A4	OSCIN	I	---	---	Crystal Oscillator Inverter Input
B1	CLKOUT2	O	---	---	f_{osc}/L Clock Output (L=1,2,4,8)
T14	NRESET (*)	I	---	Pull-up	Active low asynchronous reset input.

2.2.10. DAC Pins

The table below shows a list of DAC connection pins.

Table 10: List of DAC Connection Pins

No.	Pin Name	I/O	RST Initial Value	Pull-up/ Pull-down	Description
A9	IOUTP	O	---	---	IAMP+ Current Output Sink
A8	IOUTN	O	---	---	IAMP- Current Output Sink
B14	IREF	I	---	---	Reference Current DAC, **connect to 8.2k ohm resistor**

2.2.11. ADC Pins

The table below shows a list of ADC connection pins.

Table 11: List of ADC Connection Pins

No.	Pin Name	I/O	RST Initial Value	Pull-up/ Pull-down	Description
A11	RXP	I	---	---	Receive Path Analog Input pin
A12	RXN	I	---	---	Receive Path Analog Input pin

2.2.12. Test Setting Pin

The table below shows a list of test pins.

Table 12: List of Test Setting Pin

No.	Pin Name	I/O	RST Initial Value	Pull-up/ Pull-down	Description
H3	KME_TEST (*)	I	---	Pull-down	Production test mode setting input. In normal operation, this input should be tied to low.
C7	MODE	I	---	---	Vendor test purpose only, Fixed to “Low”
B6	CONFIG	I	---	---	Vendor test purpose only, Fixed to “Low”

2.2.13. Debugger Connection Pins

The table below shows a list of debugger connection pins.

Table 13: List of Debugger Connection Pins

No.	Pin Name	I/O	RST Initial Value	Pull-up/ Pull-down	Description
F1	AJTRSTN(Shared)	I	---	Pull-up	JTAG reset signal. * Shared with GPIO4.
F2	AJTDI(Shared)	I	---	Pull-up	JTAG test data input. * Shared with GPIO5.
G2	AJTMS(Shared)	I	---	Pull-up	JTAG TAP controller mode selection signal. *Shared with GPIO6.
G1	AJTCK(Shared)	I	---	Pull-up	JTAG test clock. * Shared with GPIO7.
H2	AJRTCK(Shared)	O	Low	Pull-up	JTAG Return TCK output to ICE.

No.	Pin Name	I/O	RST Initial Value	Pull-up/ Pull-down	Description
					*Shared with GPIO8.
H1	AJTDO(Shared)	O	Hi-Z	Pull-up	JTAG test data output. * Shared with GPIO9.
J2	AJSRSTN(Shared)	I	---	Pull-up	JTAG system reset signal. *Shared with GPIO10.

Note: GPIO10 to GPIO4 cannot be used as general-purpose ports during ICE mode operation.

2.2.14. Hardware Revision Setting Pins

The table below shows a list of hardware revision setting pins. For more information, see Section 4.9.1 Special Pin Settings.

Table 14: List of Hardware Revision Setting Pins

No.	Pin Name	I/O	RST Initial Value	Pull-up/ Pull-down	Description
B13	REVISION0 (*)	I	---	---	Revision setting
C6	REVISION1 (*)	I	---	---	Revision setting
C5	REVISION2 (*)	I	---	---	Revision setting
D5	REVISION3 (*)	I	---	---	Revision setting
C4	REVISION4 (*)	I	---	---	Used as ICEMODE setting pin
D4	REVISION5 (*)	I	---	---	Reserved. **Fixed to "Low"**

Note: Do not open these pins. Pull-up or pull-down resistors are required externally.

2.2.15. Power Supply and VSS Pins

The table below shows a list of power supply and VSS pins.

Table 15: List of Power Supply and VSS Pins

No.	Pin Name	Description
C3,D8,E4,E5,F4,F10,G4,H5, J5,J6,J9,J10,K6,K8,L9	IOVDDW	3.3-V I/O Buffer power supply pins
L6,L8,R10,T3	VDD33_K	3.3V SDRAM power supply
B4,D6,E10,F11,K7,K9	CVDD	1.2-V (core) power supply pins
A1,A14,B2,D3,D7,D12,E3, E6,E7,E8,E9,E12,F3,F5,F6, F7,F8,F9,G3,G5,G6,G7,G8,	DVSS	Digital Ground

No.	Pin Name	Description
G9,G10,G11,G12,H4,H6,H7, H8,H9,H10,H11,H12,J3,J4, J7,J8,J11,J12,K4,K5,K10,L7, L10,P3,P10,R2,U1,U3,U14		
A10,B10,B11	A33VDD	3.3V Analog Power Supply pins
C10,D9,D10,E11	A12VDD	1.2V Analog Power Supply pins
A7,A13,B8,B9,B12,D11,F12	AVSS	Analog Ground
C11	PLLAVDD	1.2V Analog VDD pin for Baseband PLL
C12	PLLAVSS	Analog Ground pin for Baseband PLL
C14	PLLDVDD	1.2V Digital VDD pin for Baseband PLL
C13	PLLDVSS	Digital Ground for Baseband PLL
A3,B3	OSC33VDD	Crystal Oscillator Buffer 3.3V Power Supply pin
A6,B5	OSCVSS	Crystal Oscillator Buffer Ground

2.2.16. Shared Pins

The table below shows a list of shared pins.

Table 16: List of Shared Pins

No.	Pin Name	Shared Pin Name	Description
F1	GPIO4	AJTRSTN	Switchable with normal mode/ICE mode settings.
F2	GPIO5	AJTDI	Switchable with normal mode/ICE mode settings.
G2	GPIO6	AJTMS	Switchable with normal mode/ICE mode settings.
G1	GPIO7	AJTCK	Switchable with normal mode/ICE mode settings.
H2	GPIO8	AJRTCK	Switchable with normal mode/ICE mode settings.
H1	GPIO9	AJTDO	Switchable with normal mode/ICE mode settings.
J2	GPIO10	AJSRSTN	Switchable with normal mode/ICE mode settings.
K2	GPIO12	EXTINT	Can be switched with GPIO selection register settings.

3. Operating Conditions

3.1. Absolute Maximum Ratings

The table below shows absolute maximum ratings.

Table 17: Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
3.3V supply voltage for I/O	V_{IOVDDW}	-0.3 to 4.0	V
3.3V supply voltage for SDRAM	V_{VDD33_K}	-0.3 to 4.0	V
3.3V supply voltage for Analog	V_{A33VDD}	-0.3 to 4.0	V
3.3V supply voltage for OSC	$V_{OSC33VDD}$	-0.3 to 4.0	V
1.2V supply voltage for Baseband, AFE digital	V_{CVDD}	-0.3 to 1.32	V
1.2V supply voltage for AFE analog	V_{A12VDD}	-0.3 to 1.6	V
Input pin voltage Standard SDRAM signals (Vendor test purpose only)	V_I	 -0.3 to V_{IOVDDW} + 0.3 (≤4.0) -0.3 to V_{VDD33_K} + 0.3 (≤4.0)	V
Input pin voltage (5V tolerant) (3.0V ≤ V_{IOVDDW} ≤ 3.6V)	V_I	-0.3 to 5.6	V
Input pin voltage (5V tolerant) (V_{IOVDDW} < 3.0V)	V_I	-0.3 to 4.0	V
Analog Input/Output Voltage RXP,RXN,IREF IOUTP, IOUTN OSCIN, XTAL	 V_{A1} V_{A2} V_{A3}	 -0.3 to V_{A33VDD} +0.3 -0.3 to 6.0 -0.3 to $V_{OSC33VDD}$ +0.3	 V V V
Output current (2mA)	I_O	-5.2/+15.9	mA
Output current (4mA)	I_O	-10.6/+31.7	mA
Output current (8mA)	I_O	-21.2/+63.4	mA

Note: The absolute maximum ratings are the limit values beyond which the IC may be damaged. Operation is not guaranteed under these conditions.

Directly connect all VDD pins to external power supplies and ground all VSS pins.

Ensure that the junction temperature (Tj) is 125°C or less during use.

3.2. Power Supply Specifications

Table 18: Power Supply Specifications

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
3.3V supply voltage	V_{IOVDDW} V_{A33VDD} $V_{OSC33VDD}$ V_{VDD33_K}	---	3.1	3.3	3.5	V
1.2V supply voltage	V_{CVDD} V_{D12VDD}	---	1.1	1.2	1.3	V
Idle Mode Current	Iidle	3.3V 1.2V	--- ---	82 226	--- ---	mA mA
Tx Mode Current	Itx	3.3V 1.2V	--- ---	111 226	--- ---	mA mA
Rx Mode Current	Irx	3.3V 1.2V	--- ---	92 237	--- ---	mA mA
Sleep Mode Current	Islp	3.3V 1.2V	--- ---	29 62	--- ---	mA mA
Standby Mode Current	Istby	3.3V 1.2V	--- ---	20 13	--- ---	mA mA

Note: Typical values are at Ta = +25°C.

The current is measured with MLKHN1501B (256Mbit), Terminal mode.

3.3. Thermal Information

Table 19: Thermal Information

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Storage temperature	T_{stg}	---	-55	---	125	°C
Operating case temperature (Top of case)	Tc	JESD51-7 (2s2p, 76.2mm x 114.3mm) P=0.81W	-40	---	105	°C

4. Baseband Part

4.1. Block Diagram

The figure below provides a block diagram for the MLKHN1501 Baseband part.

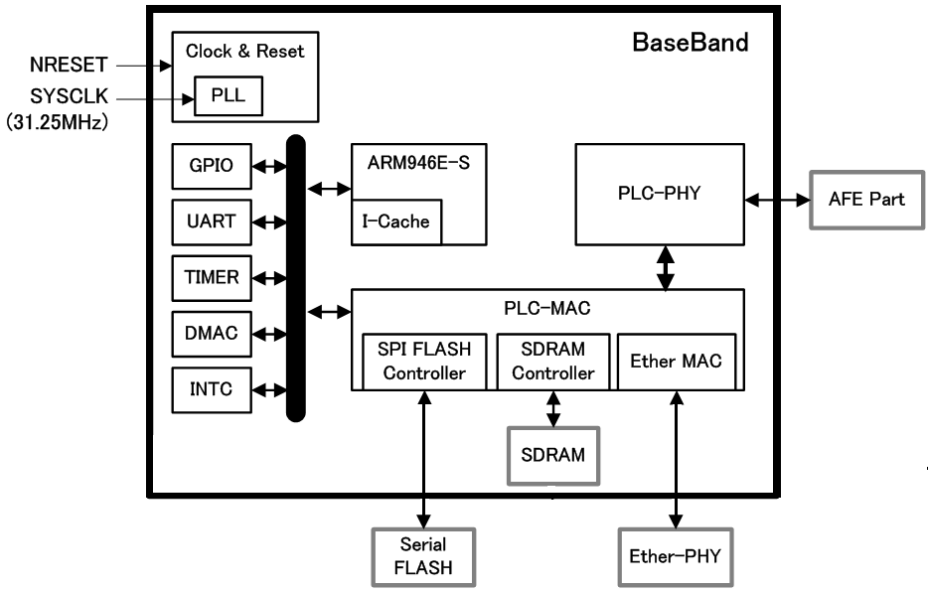


Figure 3: MLKHN1501 Block Diagram

4.2. List of Functions

4.2.1. Microcontroller and Peripherals

- CPU: ARM946E-S with 16 Kbyte Instruction Cache
- System Clock: 125MHz
- Interrupt Controller
- 16bit Timer: 8 Channels
- Serial Communication Controller: 1 Channel
- GPIO
- DMAC
- Debug Function: Embedded ICE

4.2.2. PLC-PHY Function

- Frequency bandwidth: 2 MHz to 28 MHz
- Transmission scheme: Wavelet OFDM
- Sampling frequency: 62.5 MHz
- Sub carrier: 360 carriers (without notch filter: 432 carriers) including flexible notch function
- Primary modulation scheme: 32-PAM to 2-PAM
- Transmission speed: 240Mbps
- Error correction schemes: LDPC-CC, Reed-Solomon encoding and decoding / convolutional encoding +Viterbi decoding

4.2.3. PLC-MAC Processing Function

- Multiple access control method: CSMA/CA
- Data encryption functionality: 128bit AES
- Channel estimation control functionality
- Integrated IEEE 802.3 compliant MAC
- Integrated SDRAM controller

4.2.4. SPI FLASH Interface Function

- SPI (Serial Peripheral Interface): Flash memory control functionality
- Clock frequency: 50MHz
- Boot RAM: 4Kbyte integrated boot RAM

4.2.5. Ethernet PHY Interface Functions

- Supported interface: MII/RMII/TMII
- Clock frequency: 25MHz(MII)/50MHz(RMII, TMII)

4.2.6. Clock and Reset Control Functions

- Clock generation: 25MHz / 31.25MHz / 50MHz / 62.5MHz / 125MHz / 250MHz
- Reset control functionality

- Low-power mode control functionality
- Link signal monitoring function

4.3. Example System Architectures

This section illustrates example normal mode and ICE mode system architectures for the MLKHN1501. For more information about these modes, see Section 4.6.1 Normal and Test Modes.

4.3.1. Normal Mode

The figure below illustrates an example of normal mode system architecture.

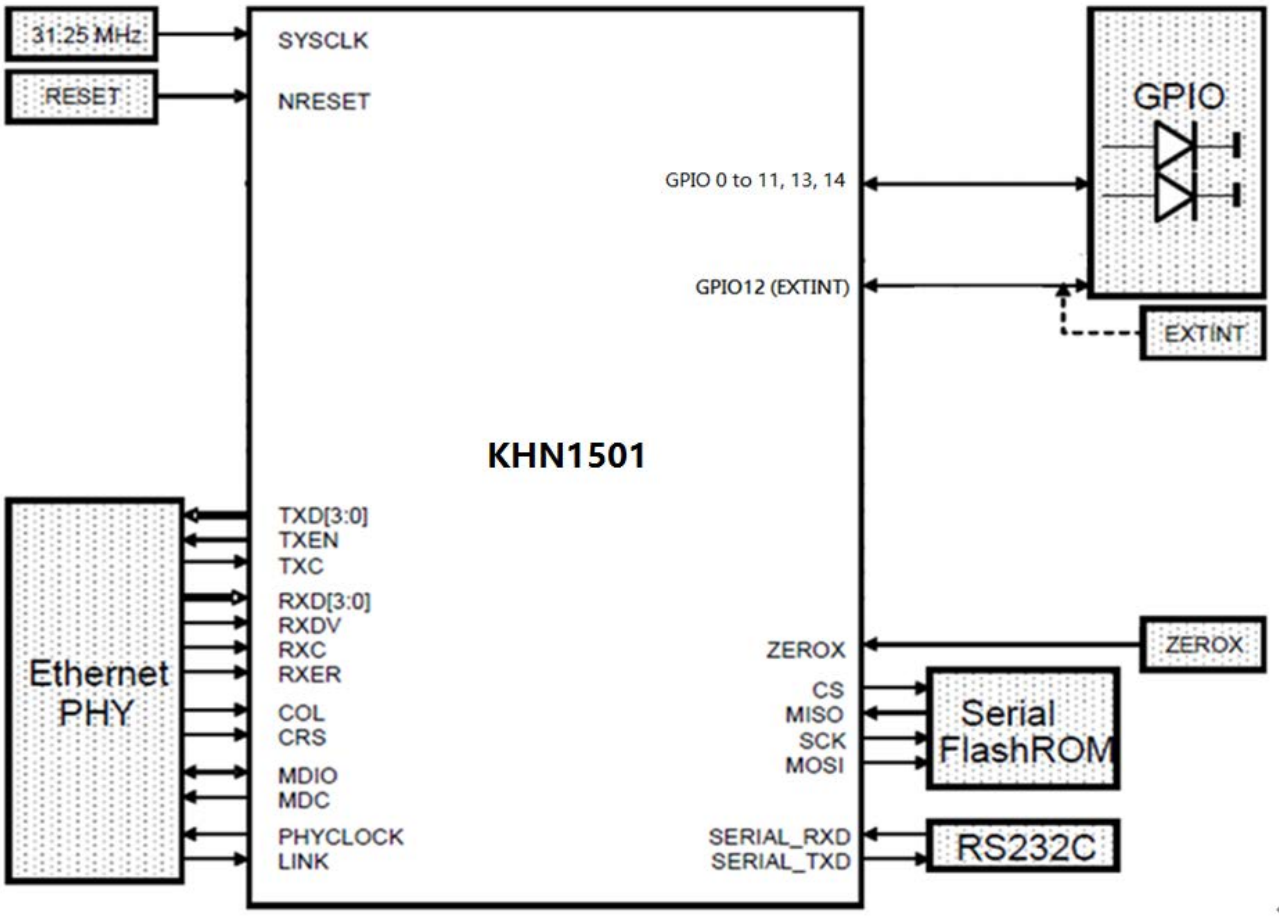


Figure 4: Normal Mode Connection Diagram

4.3.2. ICE Mode

The figure below illustrates an example of ICE mode system architecture. See Section 4.9.2 for Normal mode/ICE mode settings.

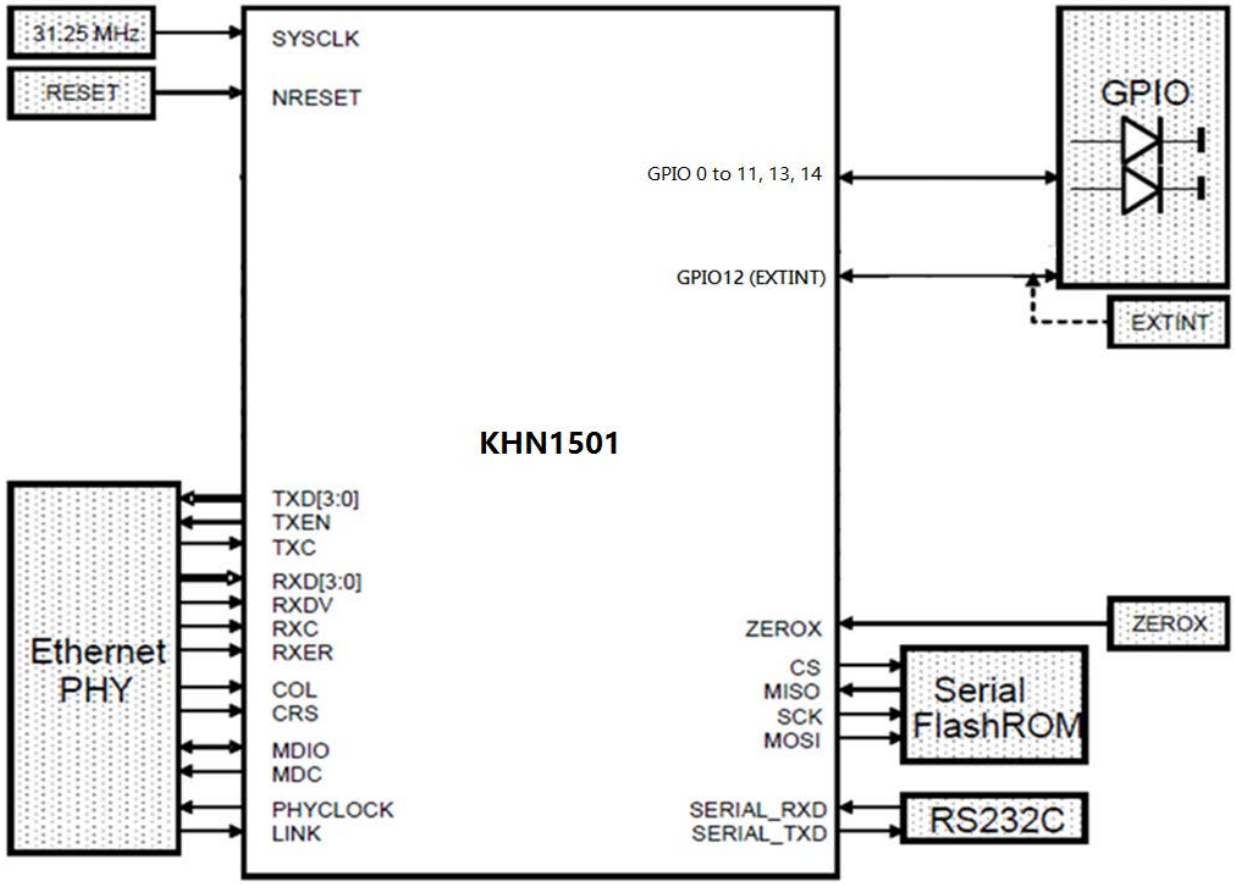


Figure 5: ICE Mode Connection Diagram

Note: GPIO10 to GPIO4 cannot be used as general-purpose ports during ICE mode operation.
The rest of GPIO can be used as GPO, but not as GPI.
After reset, GPIO is set to the input, and turn into the output immediately.
**GPIO12's EXTINT function is available even during ICE mode operation.*

4.4. Electrical Characteristics

The table below show electrical characteristics.

Table 20: Electrical Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input high voltage	V_{IH}	---	2.0	---	---	V
Input low voltage	V_{IL}	---	---	---	0.8	V
Input threshold voltage	V_T	---	1.30	1.40	1.50	V
Schmitt Trigger Input threshold voltage	V_{T+}	Low to High	1.56	1.68	1.77	V
	V_{T-}	High to Low	1.14	1.23	1.33	V
Input leakage current	I_{LI}	$V_I = V_{IOVDDW}$ or V_{SS}	---	---	±10	µA
Pull-up resistor	R_{IH}	$V_I = V_{SS}$	26	38	59	kΩ
Pull-down resistor	R_{IL}	$VI = V_{IOVDDW}$ or V_{SS}	33	47	81	kΩ
Output high voltage	V_{OH}	---	2.4	---	---	V
Output low voltage	V_{OL}	---	---	---	0.4	V
Output leakage current	O_{LI}	$V_I = V_{IOVDDW}$ or V_{SS} $V_O = V_{IOVDDW}$ or V_{SS}	---	---	±10	µA
Power dissipation	Pd	---	---	*590	---	mW

*Note: *includes whole blocks' (AFE, BB, SDRAM, etc) power dissipation*

Conditions: VIOVDDW = VVDD33_K = VA33VDD = VOSC33VDD = 3.3 V ± 0.3 V

VCVDD = VA12VDD = 1.2 V ± 0.12 V

-40°C < Tj < 125°C

4.5. AC Characteristics

The following shows AC characteristics.

Note: 5pF load capacitance is assumed.

4.5.1. Ethernet Connection Pins (MII/TMII Specification) Timing

Table 21: Ethernet Connection Pins (MII Specification) Timing Parameters

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
MII clock cycle time (TXC)	t_{TXCCYC}	---	---	40.0	---	ns
MII signal output delay time (TXEN)	t_{TXENOD}	---	3.5	---	10.5	ns
MII signal output hold time (TXEN)	t_{TXENOH}	---	3.5	---	---	ns
MII signal output delay time (TXD3 to TXD0)	t_{TXDOD}	---	3.5	---	10.5	ns
MII signal output hold time (TXD3 to TXD0)	t_{TXDOH}	---	3.5	---	---	ns
MII signal input setup time (CRS, COL)	t_{TXDIS}	---	---	---	---	ns
MII signal input hold time (CRS, COL)	t_{TXDIH}	---	---	---	---	ns
MII clock cycle time (RXC)	t_{RXCCYC}	---	---	40.0	---	ns
MII signal input setup time (RXD3 to RXD0, RXDV, RXER)	t_{RXDIS}	---	5.0	---	---	ns
MII signal input hold time (RXD3 to RXD0, RXDV, RXER)	t_{RXDIH}	---	5.0	---	---	ns
MII signal drive delay time (MDIO)	t_{MDOZ2D}	---	30.0	---	33.0	ns
MII signal disable delay time (MDIO)	t_{MDOD2Z}	---	30.0	---	33.0	ns
MII signal output delay time (MDIO)	t_{MDOOD}	---	30.0	---	33.0	ns
MII signal output hold time (MDIO)	t_{MDOOH}	---	30.0	--	---	ns
MII signal input setup time (MDIO)	t_{MDIIS}	---	3.0	---	---	ns
MII signal input hold time (MDIO)	t_{MDIIH}	---	0.0	---	---	ns

Table 22: Ethernet Connection Pins (TMII Specification) Timing Parameters

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
MII clock cycle time (TXC)	t_{TXCCYC}	---	---	20.0	---	ns
MII signal output delay time (TXEN)	t_{TXENOD}	---	3.5	---	10.5	ns
MII signal output hold time (TXEN)	t_{TXENOH}	---	3.5	---	---	ns
MII signal output delay time (TXD3 to TXD0)	t_{TXDOD}	---	3.5	---	10.5	ns
MII signal output hold time (TXD3 to TXD0)	t_{TXDOH}	---	3.5	---	---	ns
MII clock cycle time (RXC)	t_{RXCCYC}	---	---	20.0	---	ns
MII signal input setup time (RXD3 to RXD0, RXDV, RXER)	t_{RXDIS}	---	5.0	---	---	ns
MII signal input hold time (RXD3 to RXD0, RXDV, RXER)	t_{RXDIH}	---	5.0	---	---	ns
MII signal drive delay time (MDIO)	t_{MDOZ2D}	---	30.0	---	33.0	ns
MII signal disable delay time (MDIO)	t_{MDOD2Z}	---	30.0	---	33.0	ns
MII signal output delay time (MDIO)	t_{MDOOD}	---	30.0	---	33.0	ns
MII signal output hold time (MDIO)	t_{MDOOH}	---	30.0	--	---	ns
MII signal input setup time (MDIO)	t_{MDIIS}	---	3.0	---	---	ns
MII signal input hold time (MDIO)	t_{MDIIH}	---	0.0	---	---	ns

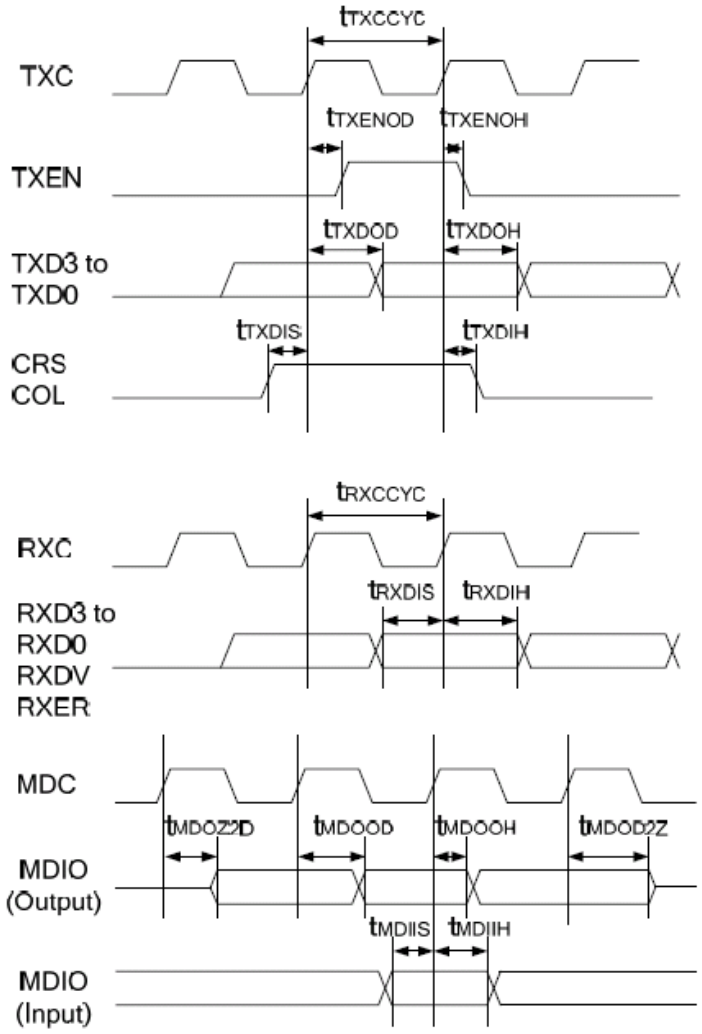


Figure 6: Ethernet Connection Pins (MII/TMII Specifications) Timing Chart

4.5.2. Ethernet Connection Pins (RMII Specification) Timing

Table 23: Ethernet Connection Pins (RMII Specification) Timing Parameters

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
RMII clock cycle time (PHYCLOCK)	$t_{RTXCCYC}$	---	---	20.0	---	ns
RMII signal output delay time (TXEN)	$t_{RTXENOD}$	---	2.0	---	7.5	ns
RMII signal output hold time (TXEN)	$t_{RTXENOH}$	---	2.0	---	---	ns

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
RMII signal output delay time (TXD1, TXD0)	t_{RTXDOD}	---	2.0	---	7.5	ns
RMII signal output hold time (TXD1, TXD0)	t_{RTXDOH}	---	2.0	---	---	ns
RMII signal input setup time (RXDV)	t_{RTXDIS}	---	2.5	---	---	ns
RMII signal input hold time (RXDV)	t_{RTXDIH}	---	1.5	---	---	ns
RMII signal input setup time (RXD1, RXD0, RXER)	t_{RRXDIS}	---	2.5	---	---	ns
RMII signal input hold time (RXD1, RXD0, RXER)	t_{RRXDIH}	---	2.0	---	---	ns

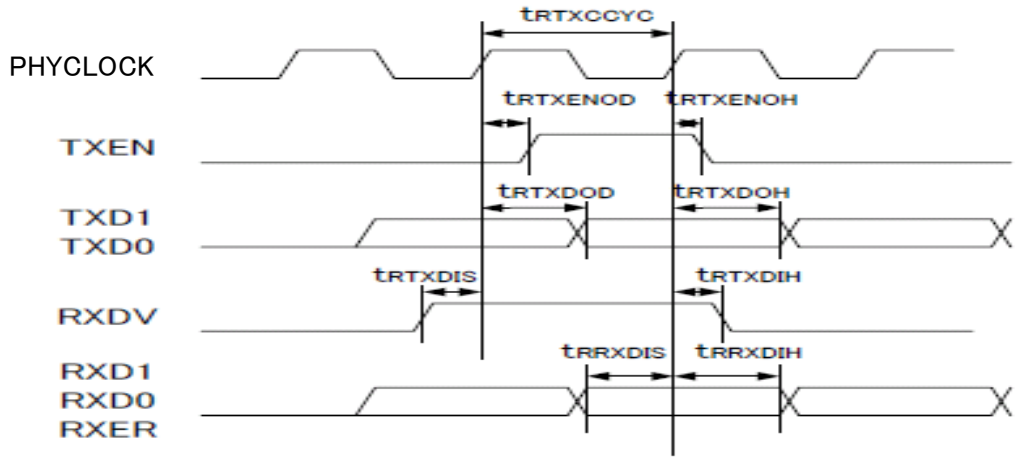


Figure 7: Ethernet Connection Pins (RMII Specifications) Timing Chart

4.5.3. Serial Flash Connection Pins Timing (Write)

Table 24: Serial Flash Connection Pins Timing (Write) Parameters

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Flash serial clock cycle time (SCK)	T_{CLKCYC}	---	---	20.0	---	ns
Flash serial clock duty (SCK)	T_{CLKWH}/ T_{CLKCYC} T_{CLKWL}/ T_{CLKCYC}	---	45	---	55	%
Flash Chip Select output	T_{CSDD} (*1)	---	-1.0	---	2.0	ns

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Delay time						
Flash Chip Select output Hold time	T_{CSDH} (*1)		-1.0	---	---	ns
Flash serial data output delay time (MOSI)	T_{MOSIDD} (*1)	---	-2.0	---	4.6	ns
Flash serial data output hold time (MOSI)	T_{MOSIDH} (*1)	---	-2.0	---	---	ns

*Note: (*1) Minus values may prior to the negative edge of SCK.*

4.5.4. Serial Flash Connection Pins Timing (Read)

Table 25: Serial Flash Connection Pins Timing (Read) Parameters

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Flash serial clock cycle time (SCK)	T_{CLKCYC}	---	---	20.0	---	ns
Flash serial clock duty (SCK)	T_{CLKWH}/ T_{CLKCYC} T_{CLKWL}/ T_{CLKCYC}	---	45	---	55	%
Flash serial data input setup time (MISO)	T_{MISODS}	---	9.5	---	---	ns
Flash serial data input hold time (MISO)	T_{MISODH}	---	0.0	---	---	ns

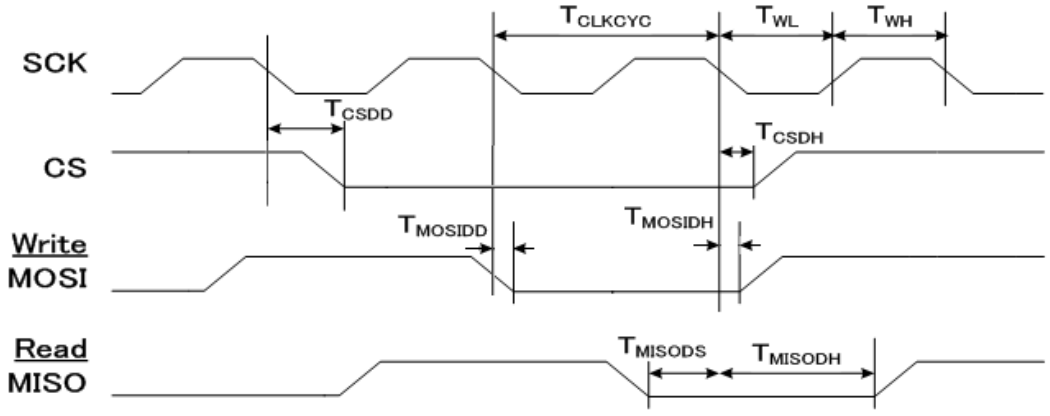


Figure 8: Serial Flash Connection Pins Timing Chart

4.6. Description of Operating Modes

4.6.1. Normal and Test Modes

Lists the modes provided by the MLKHN1501.

Table 26: List of Normal and Test Modes

Normal / Test Mode	Description
Normal mode	This mode is used to operate the system.
ICE mode	This mode is used to troubleshoot issues experienced.

4.6.2. Normal Mode

Normal mode is used to operate the system. Use this mode during normal operation.

4.6.3. ICE Mode

ICE mode is used to troubleshoot issues experienced during normal mode operation. GPIO [10:4] are connected to an ICE during ICE mode operation and cannot be used as general-purpose ports in this configuration. For this reason, functionality utilizing GPIO [10:4] cannot be debugged. For more information, see Section 2.2.16 Shared Pins and Section 4.9.2 Normal and Test Modes Setting.

Note: If the AJTRSTN pin is pulled down, it will be continuously in the reset assert state while no debugger is connected in ICE mode, effectively disabling MLKHN1501 operation.

4.7. Power Supply Activation

Activate the 3.3V and 1.2V power supplies simultaneously.

* As a guideline, allow no more than 100ms between the activation of the 3.3V and 1.2V power supplies.

Note: The upper limit of 100ms is a sample value derived from internal evaluations.

4.8. Reset Sequence

The figure below provides a power-on reset timing chart. Assert reset pin (NRESET) input for at least 1µs after AVDD/DVDD power supplies are stable.

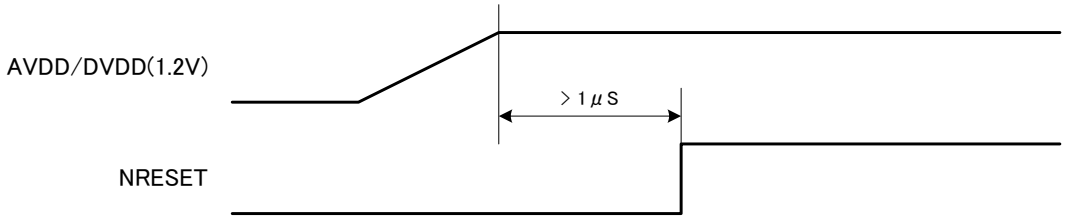


Figure 9: Power-on reset timing chart

4.9. Setting Methods

4.9.1. Special Pin Settings

These settings are implemented by connecting external pull-up or pull-down resistors to the REVISION5 to REVISION0 pins. They are used to set the LSI version as well as pin settings for user applications (for use in managing board versions, etc.).

When a reset is activated (NRESET = “L” level), initial values for REVISION5 to REVISION0 pins (the states of their external pull-up/pull-down resistors) are loaded internally. The loaded values can be accessed using the initial value loading register.

Table 27: Special Pin Settings

Pin Name	Description
REVISION5	Fix this pin’s setting as follows: External pull-down
REVISION4	Set ICEMODE.(see 4.9.2) Set as desired. Pull-down or Pull-up
REVISION3	Set as desired. Pull-down or Pull-up
REVISION2	Set as desired. Pull-down or Pull-up
REVISION1	Set as desired. Pull-down or Pull-up
REVISION0	Set as desired. Pull-down or Pull-up

Note: Connect external pull-up or pull-down resistors to all 6 pins. REVISION5 should always be pulled down as described in the table above.

4.9.2. Normal and Test Modes Setting

The setting of the normal and test modes is controlled by REVISION4 input. These settings are sampled during internal reset state. So these pins should remain stable after 300µs from NRESET is de-asserted.

The table below shows Normal mode/ICE mode settings by REVISION4 input.

Table 28: Test Mode Setting by REVISION4 input

Normal / Test Mode	ICEMODE
Normal mode	"L" level
ICE mode	"H" level

5. Analog Front-End(AFE) Part

5.1. General Description

The MLKHN1501 has highly integrated analog front-end part for PLC. Data rate is supported up to 80 MSPS and 160 MSPS in Rx path and Tx path, respectively. Interfacing can be either binary or twos compliment, LSB or MSB first. A serial peripheral interface (SPI) allows software programmability of the front-end. An on-chip PLL multiplier and synthesizer provide all the required clock signals from a single crystal or clock source.

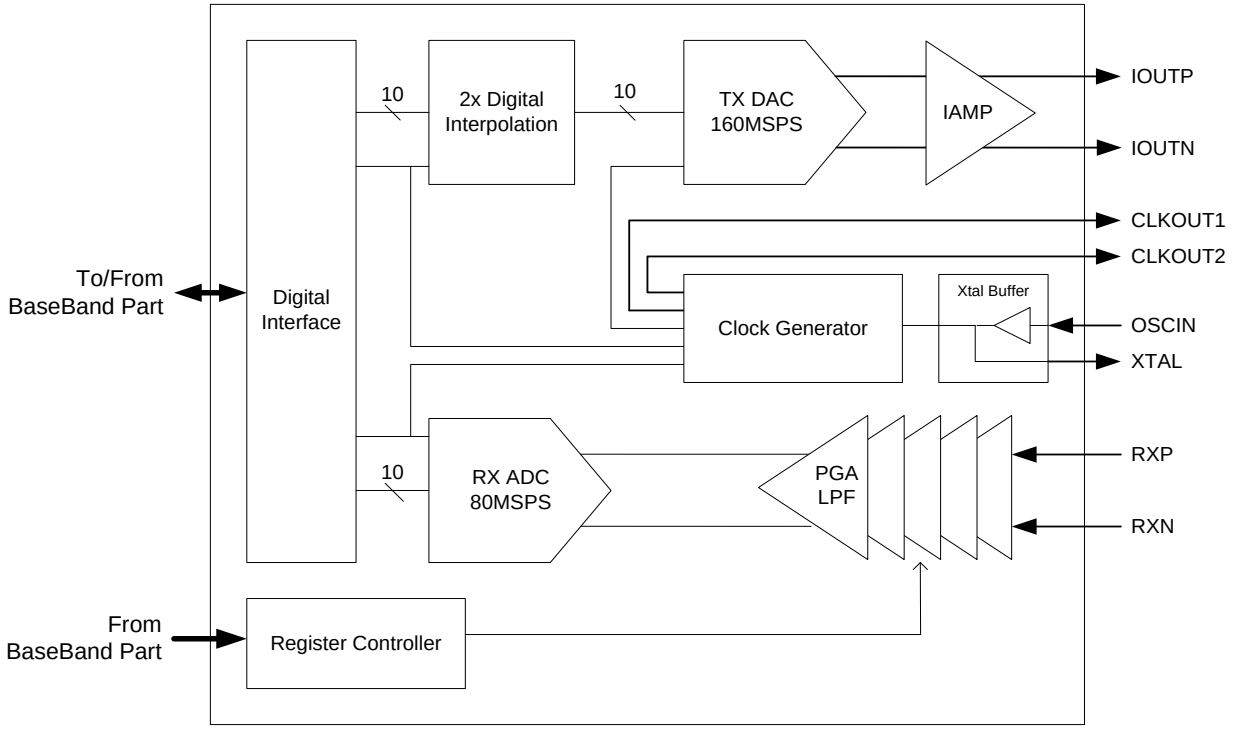


Figure 10: AFE Functional Block Diagram

The functional block diagram of the AFE part is shown in the figure above. The Tx signal path consists of a bypassable 2x low pass interpolation filter, a 10-bit TxDAC and a current amplifier (IAMP). The transmit signal path bandwidth is qualified up to frequencies of 36MHz.

The current amplifier can deliver up to 20mA signal power. Tx power can be controlled over a 7.5dB range with 0.5dB steps.

The Rx signal path consists of a programmable amplifier (RxPGA), a low pass filter (LPF) and a 10 bit ADC. The low-noise RxPGA has a programmable gain range of -18dB to +41dB in 1dB steps. Its input referred noise is less than 7.5nV/rtHz for gain settings beyond 30dB. The cutoff frequency of LPF is programmable.

5.2. Specifications

5.2.1. TX Path specifications

Table 29: TX Path Specifications

Parameter	Temp	Min	Typ	Max	Unit
Tx DAC DC CHARACTERISTICS					
Resolution	Full		10		Bits
Update Rate	Full			160	MSPS
Full-Scale Output Current	Full		2		mA
Gain Error	Full			±6.5	% of FS
Offset Error	Full			±0.1	% of FS
IAMP OUTPUT CHARACTERISTICS					
Output Capacitance	25°C		6.7		pF
Tx DC CHARACTERISTICS					
Full-Scale Output Current (IFS)	Full	8.4		20	mA
DC offset current(dc_off)			0.4		mA
AC Voltage Compliance Range		1.15		6	V
Tx CONTROL CHARACTERISTICS					
Minimum Gain	25°C		-7.5		dB
Maximum Gain	25°C		0		dB
Gain Step Size	25°C		0.5		dB
Gain Step Accuracy	Full		Monotonic		dB
Gain Range Error	Full			0.5	dB
Tx AC CHARACTERISTICS					
(160 MSPS, 20 mA IFS, Fout = 10 MHz, 0 dBFS)					
Signal-to-Noise and Distortion Ratio (SNDR)	Full	49	52		dBc
Signal-to-Noise Ratio (SNR)	Full	52	57		dBc
Total Harmonic Distortion (THD)	Full		-53	-50	dBc
Spurious Free Dynamic Range(SFDR)	Full	51	54		dBc
Tx DIGIRAL FILTER SPECIFICATIONS					
2x Interpolation(low pass)					
Latency(Relative to $1/f_{DAC}$)	Full		30		Cycles
-0.2dB Bandwidth	Full		0.2292		f_{out}/f_{DAC}
-3dB Bandwidth	Full		0.2435		f_{out}/f_{DAC}
Stop-Band Rejection(0.289 to 0.789 f_{DAC})	Full		51.9		dB
Interpolation Off(bypass)					
Latency	Full		2		Cycles

Note: IOVDDW=OSC33VDD=A33VDD=3.3V ±0.2V, A12VDD=CVDD=1.2V ± 0.1V
FDAC=160MSPS, UNLESS OTHERWISE NOTED

5.2.2. RX Path Specifications

Table 30: Rx Path Specifications

Parameter	Temp	Min	Typ	Max	Unit
Rx INPUT CHARACTERISTICS					
Input Voltage Span (RxPGA gain = −18 dB)	Full		6.33		Vp-p
Input Voltage Span (RxPGA gain = 41 dB)	Full		7.4		mVp-p
Input Common-Mode Voltage	25°C		1.47		V
Differential Input Impedance	25°C		400 || 4.0		Ω || pF
Input Voltage Noise Density (RxPGA Gain = 27 dB, f−3 dBF = 26 MHz)	Full		6.0	7.5	nV/rtHz
Input Voltage Noise Density (RxPGA Gain = 41 dB, f−3 dBF = 40 MHz)	Full		3.8	5.0	nV/rtHz
RxPGA CHARACTERISTICS					
Minimum Gain	25°C		-18		dB
Maximum Gain	25°C		41		dB
Gain Step Size (coarse / fine)	25°C		6 / 1		dB
Gain Step Accuracy	Full		Monotonic		dB
Gain Range Error	Full		1.5	2.6	dB
Rx LPF CHARACTERISTICS					
Cutoff Frequency range (f−3dBF = 38 MHz , f_{ADC}=62.5MSPS, LPFTUNE coefficient: 7'b0110100)	Full	32.3	38.0	43.7	MHz
Pass-Band Ripple	25°C		±1		dB
Settling Time to 5 dB RxPGA Gain Step @ f_{ADC} = 80 MSPS	Full			470	ns
Settling Time to 59 dB RxPGA Gain Step @ f_{ADC} = 80 MSPS	Full			470	ns
ADC DC CHARACTERISTICS					
Resolution	NA		10		Bits
Update Rate	Full	8		80	MSPS
Rx PATH COMPOSITE AC PERFORMANCE (f_{ADC} = 80 MSPS, f_{IN} = 10 MHz)					
RxPGA Gain = 41 dB (Full-Scale = 7.4 mVp-p)					
Signal-to-Noise Ratio (SNR)	25°C	38	40		dBc
Total Harmonic Distortion (THD)	25°C		-57	-53	dBc
RxPGA Gain = 18 dB (Full-Scale = 104 mVp-p)					
Signal-to-Noise Ratio (SNR)	25°C	51	53		dBc
Total Harmonic Distortion (THD)	25°C		-64	-53	dBc
RxPGA Gain = -6 dB (Full-Scale = 1.65 Vp-p)					
Signal-to-Noise Ratio (SNR)	25°C	51	53		dBc
Total Harmonic Distortion (THD)	25°C		-64	-53	dBc
RxPGA Gain = -16 dB (Full-Scale = 5.23 Vp-p)					
Signal-to-Noise Ratio (SNR)	25°C	51	53		dBc

Parameter	Temp	Min	Typ	Max	Unit
Total Harmonic Distortion (THD)	25°C		-64	-53	dBc

Note: IOVDDW=OSC33VDD=A33VDD=3.3V ±0.2V, A12VDD=CVDD=1.2V ± 0.1V UNLESS OTHERWISE NOTED

5.2.3. PLL Specifications

Table 31: PLL Specifications

Parameter	Temp	Min	Typ	Max	Unit
PLL CLK GENERATOR					
OSCIN Input Leakage Current Tolerance	Full			0.5	uA
OSCIN Frequency Range	Full	16		80	MHz
Internal VCO Frequency Range	Full	120		320	MHz
CLKOUT1 Duty Cycle	Full	40	50	60	%
CLKOUT1 Jitter	Full		24		ps rms
CLKOUT2 Duty Cycle	Full	30	50	70	%
CLKOUT2 Jitter	Full		14		ps rms
Settling time (within 1% of its frequency)	Full			60	us

Note: IOVDDW=OSC33VDD=A33VDD=3.3V ±0.2V, A12VDD=CVDD=1.2V ± 0.1V unless otherwise noted

5.2.4. Digital Interface Specifications

Table 32: Digital Interface Specifications

Parameter	Temp	Min	Typ	Max	Unit
CMOS LOGIC INPUTS					
High Level Input Voltage	Full	2.0			V
Low Level Input Voltage	Full			0.8	V
Input Leakage Current	Full			10	µA
Input Capacitance	Full		3		pF
CMOS LOGIC OUTPUTS (C_{LOAD} = 5 pF)					
High Level Output Voltage (I_{OH} = 2 mA)	Full	2.4			V
Low Level Output Voltage (I_{OH} = 2 mA)	Full			0.4	V
Output Rise/Fall Time (C_{LOAD} = 16 pF)	Full		2.2/2.2		ns
Output Rise/Fall Time (C_{LOAD} = 5 pF)	Full		1.2/1.1		ns
RESET					
Minimum Low Pulse Width (Relative to f_{ADC})		1			Clock cycles

Note: IOVDDW=OSC33VDD=A33VDD=3.3V ±0.2V, A12VDD=CVDD=1.2V ± 0.1V UNLESS OTHERWISE NOTED

5.3. Function Descriptions

The functioning of the Rx- and Tx path is explained in the following section. The programmable settings are listed.

5.3.1. Rx Path

The receive signal path, as shown in the figure below, consists of a 3-stage RxPGA, a low pass filter (LPF) and a 10-bit ADC. Gain stages are software programmable over a wide range. Working in conjunction with the receive path is a DC correction circuit that automatically calibrates the RxPGA chain during startup. In normal mode the RX chain is always on.

In the next section the typical performance of the RxPath will be explained and the different blocks of the Rx chain will be presented.

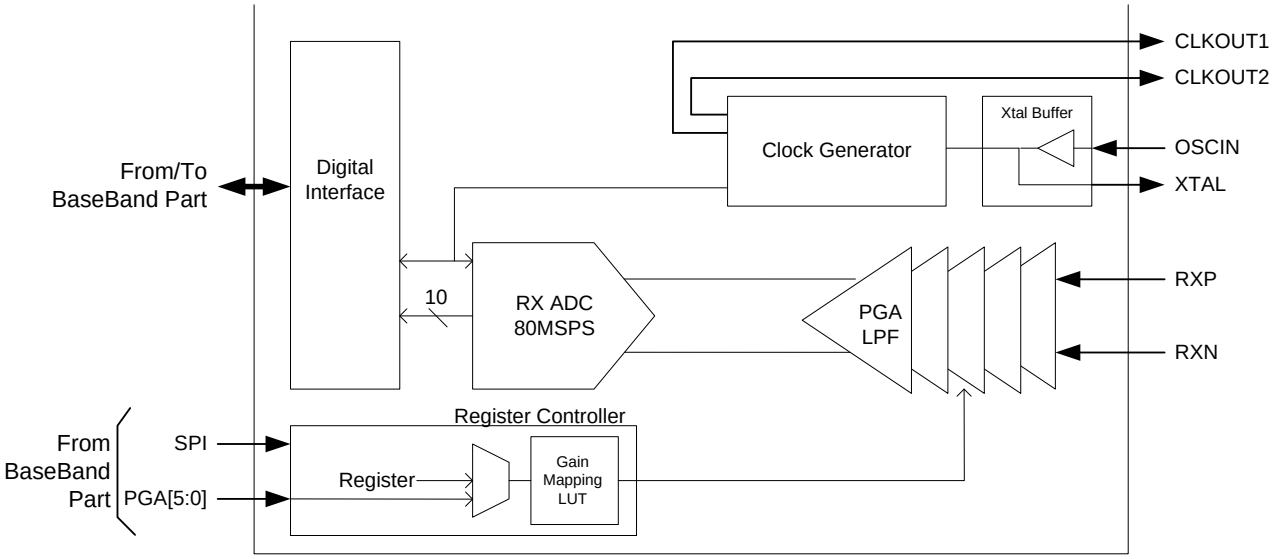


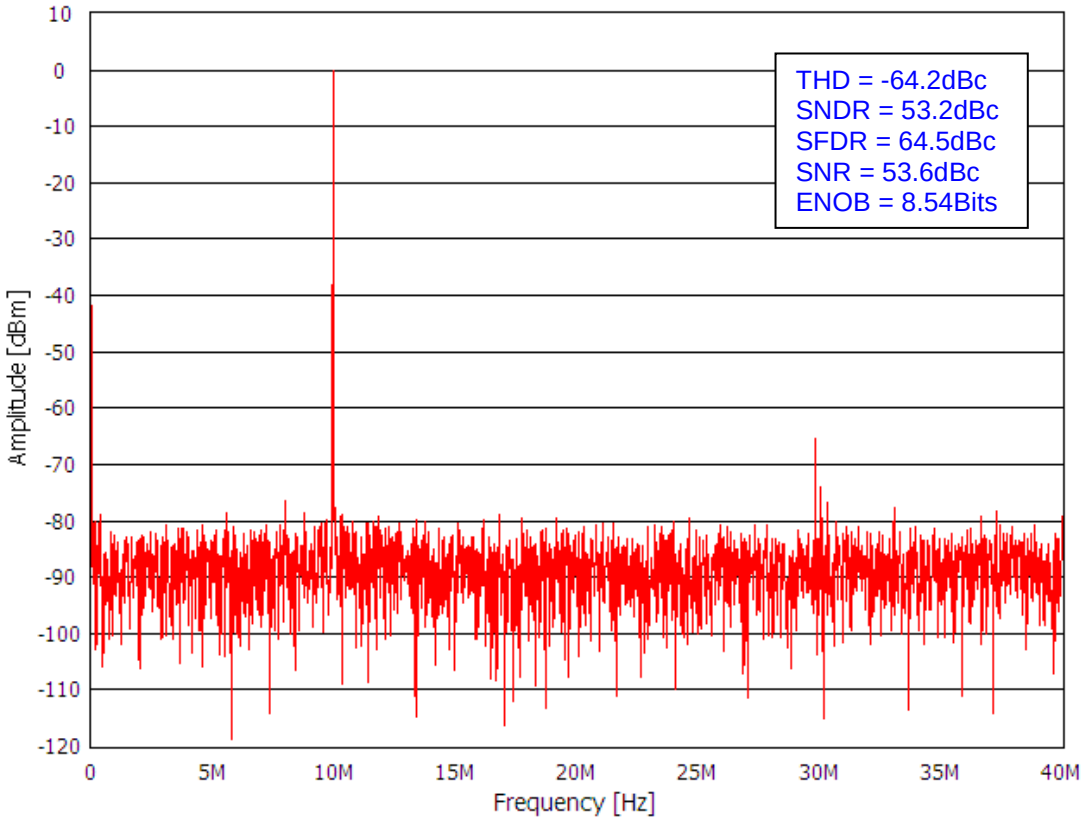
Figure 11: Functional Block Diagram of the Rx Path

Typical Performance Characteristics

Verifications will include SINAD vs. PGA gain at the following conditions specified below:

Table 33: Verification for Rx Path

Tones	f_{ADC}
10MHz	80MHz
(1) For a -1dBFS sine wave (1dB below full scale input ADC).	



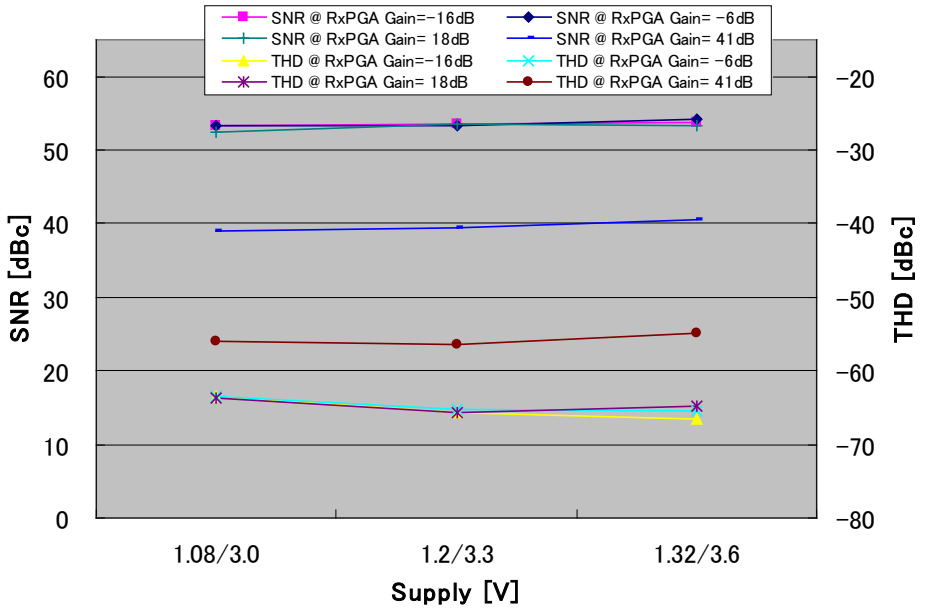


Figure 13: SNR and THD vs. Supply Voltage

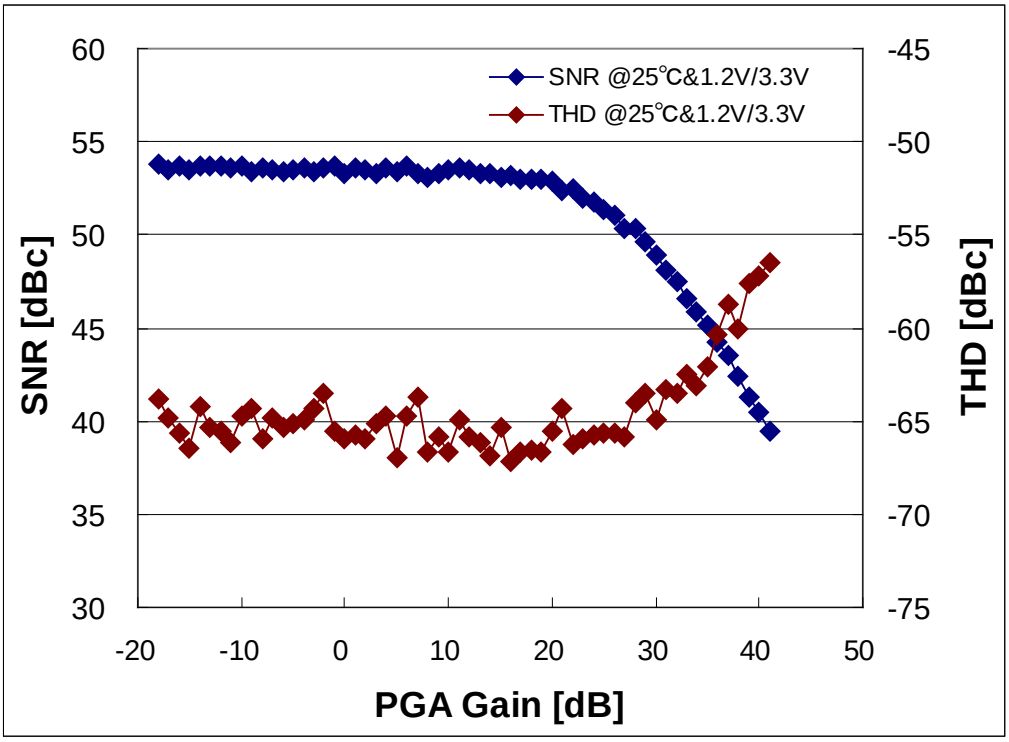


Figure 14: SNR and THD vs. RxPGA Gain (Supply=1.2V/3.3V and Temperature=25℃)

Rx Programmable Gain Amplifier

The RxPGA consist of gain stages. The RxPGA features low-noise preamplification

(< 6nV/√Hz) for optimal noise performance of the Rx chain. The RxPGA chain has coarse and fine gain settings. In total the gain can be set from -18 to +41dB. One gain stages offers fine gain setting from 0 to 6dB with 1dB resolution, the other gain stages offer -18 to +36 dB in 6dB resolution.

The nominal differential input impedance (seen between RxP and RxN pins) is 400Ω//4pF. The RxPGA input is self-biased at 1.47V common mode level, allowing a maximum differential input voltage swing of 1.5V at RXP and RXN. When transmitting, the RxPGA input is maintained at 1.47V common mode level. The DC offset of the different stage in the RxPGA are countered by the DC correction circuit. Although the offset varies for gain settings, the offset is limited to ±5% of the ADC's full scale. The calibration of the DC correction is performed automatically after power up and can also be initiated via SPI. The DC offset word can also be overruled via SPI as will be explained in following section on RxPGA control.

The gain of the RxPGA should be set to minimize clipping of the ADC while utilizing most of its dynamic range. The maximum peak-to-peak voltage at the ADC input is 0.83 Vp-p. The input of the RxPGA itself is limited to 6.33 Vp-p to prevent turning on ESD circuitry. The optimal distribution of the gain over the different stages in the RxPGA is preprogrammed and should normally not be changed. For testing purpose it can be overruled as described below in the section on RxPGA control.

RxPGA Control

The RxPGA is programmable over a -18dB to +41dB with a 1 dB resolution using a 6 bit word. The 0dB setting corresponds to -1%FS input of the ADC, being 0.83 Vp-p. The 6-bit word steers a LUT that contains optimal gain distribution over the different stages.

Upon power-up, the RxPGA register is set to its minimum gain of -18dB. The RxPGA mapping is shown below. The register setting over +41 dB is clumped to +41dB.

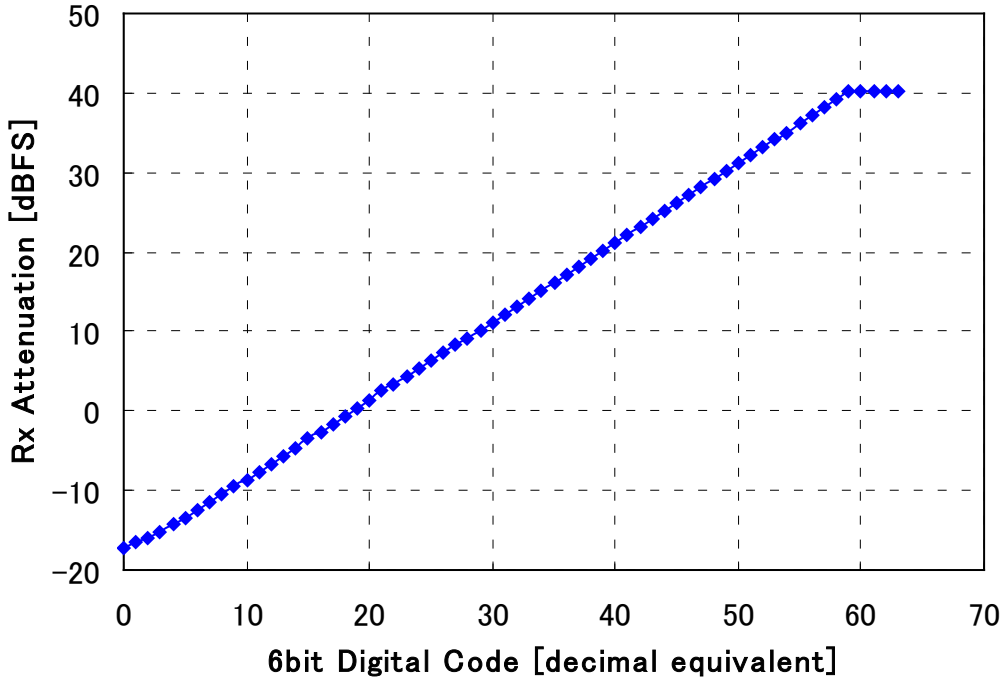


Figure 15: Digital Gain mapping of RxPGA

Table 34: SPI Register RxPGA

Address	Bit	Description
0x07	[5]	Initiate DCTUNE
0x09	[6]	Enable RxPGA update via SPI
	[5:0]	RxPGA gain code
0x0B	[5]	Select RxPGA via PGA[5:0]

The RxPGA gain setting can be set through either the PGA[5:0] port or via SPI. The first options are to be used for applications requiring fast closed-loop response. The SPI port allows direct update and read back of the RxPGA gain register via register 0x09 with an update rate of 32MHz (SCLK).

The RxPGA gain can be changed via the PGA[5:0] port. This port is connected directly to the RxPGA[5:0] / TxPGA[3:0] register, no gating signals are required. In case the PGA port is to be used to switch from

RxPGA to TxPGA setting, care should be taken to deselect the RxPGA register first, then update the PGA[5:0] port and finally select the TxPGA gain register.

The RxPGA has a DC offset calibration which is started after startup or when triggered through SPI. During DC offset trimming, the RxP and RxN input ports are shorted. By setting bit [5] of SPI Register 0x07, the DC calibration is triggered. The DC calibration takes 3 msec.

Low Pass Filter

The low pass filter (LPF) provides a third order response with a cutoff frequency. The cutoff frequency, f-3dB, depends on ADC's sample rate, fADC, and LPFTUNE Coefficient, but can't be set under around 20MHz.

$$f_{-3dB} = f_{ADC} \times \frac{113 - Coefficient}{100}$$

The recommended value of LPFTUNE Coefficient is 52, 0x10[6:0]=0110100. The f-3dB is typically 38 MHz when the fADC is 62.5 MSPS and the LPFTUNE Coefficient is 52. Actually, the change in f-3dB into the LPFTUNE Coefficient is not linear. Moreover, the use range of the LPFTUNE Coefficient is 64±20. It is necessary to actually confirm the f-3dB by the measurement. LPF keeps the corner frequency within 15% over process, supply voltage and temperature variations. LPF tuning operates after power up and when initiated through SPI. LPF tuning takes 1 msec. Because the target frequency changes by ±15%, it is necessary to set it with room temperature. An overview of the SPI registers that control LPF is given below :

Table 35: SPI Register RxLPF

Address	Bit	Description
0x07	[7]	Initiate LPFTUNE
	[3]	Enable LPFTUNE
	[2]	Bypass LPF and PGA
	[0]	Bypass LPF
0x10	[6:0]	LPFTUNE Coefficient

Analog-to-Digital Converter (ADC)

A 10-bit pipeline ADC with update rate up to 80MSPS convert the filtered data in the Rx chain. The ADC has a full-scale input span of 0.83Vp-p. The conversion rate of the ADC is controlled by the PLL settings (see also section 5.3.3). The ADC has a duty cycle restore, which ensures that the ADC gets a near 50% duty cycle. The power of the ADC scales automatically with the sampling frequency. The ADC can be set in power down mode by setting bit 2 of Register 0x01 or 0x02 without PGA set in active mode.

Table 36: SPI Register RxADC

Address	Bit	Description
0x01	[2]	Power down ADC (PWD=0)
0x02	[2]	Power down ADC (PWD=1)

5.3.2. Tx Path

The Tx path comprises a selectable 2x digital low-pass filter, a 10-bit DAC and a current amplifier (IAMP) as shown in the figure below. DAC is software programmable, the gain spans a 0 to -7.5dB gain range.

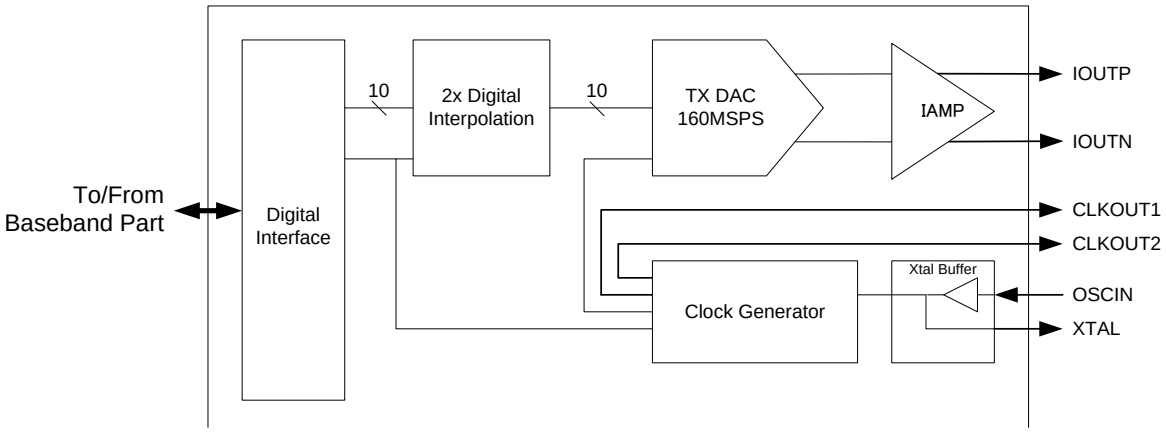


Figure 16: Functional Block Diagram of the Tx Path

In the following sections, the programmability and functioning of the digital interpolation filter and the DAC and the IAMP will be discussed in detail.

TxPGA Control

The input data from the Tx port can be fed into a 2x low pass interpolation filter. The filter can be switched to bypass mode. These settings are determined by bit 6 in the SPI Register 0x0C as listed below

Table 37: SPI Register DIGITAL INTERPOLATION FILTER

Address	Bit	Description
0x0A	[6]	Enable TxPGA update via SPI
	[3:0]	Tx Gain Code
0x0B	[6]	Select TxPGA via PGA[3:0]
0x0C	[6]	Enable Interpolation Filter
	[4]	Invert TXEN/TXSYNC

Digital Interpolation Filters

The digital filter behaves as a half-band low pass filter. The half-band filter is composed of 55 symmetrical taps.

The frequency responses, normalized to fDATA, are shown below:

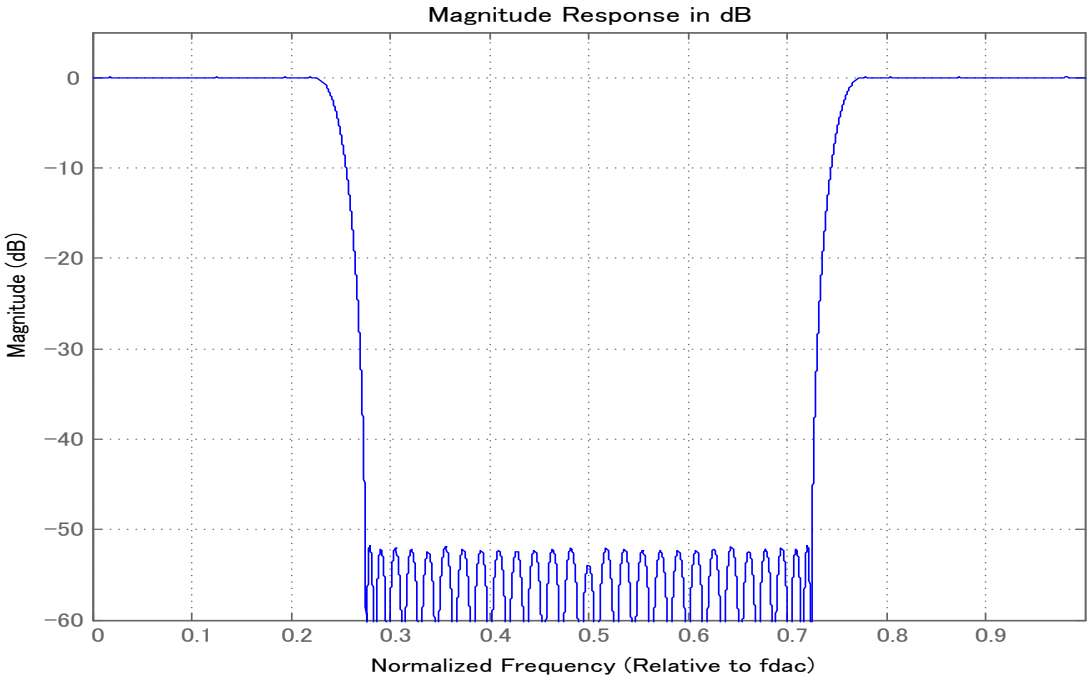


Figure 17: Frequency response of the 2x interpolation filter (normalized to fDATA).

The pipeline delays of the 2x interpolation filter is 55 clock cycles relative to fDATA.

Digital-to-Analog Converter (DAC) and IAMP

The TxDAC reconstructs the output of the digital interpolation filter and sources a differential output signal that is fed into the IAMP for further current amplification. The composite overall gain of the Tx path can be programmed from 0 to -7.5 dB with an increment of 0.5dB. The gain applied through the 4-bit TxPGA gain word, is mapped to a gain setting for the IAMP and a fine gain setting for the DAC. A coarse gain setting for the DAC is fixed to 2 mA. The different gain setting is listed below.

Table 38: GAIN SETTINGS IAMP

Gain [code]	Gain change [times]	Comment
0000	0x	sleep mode
1000	4x	
1001	5x	
1010	6x	
1011	7x	
1100	8x	
1101	9x	
1110	10x	

Table 39: FINE GAIN SETTINGS DAC

FG_CTRL [code]	Gain Change (IFS)
1111	-10.0%
1000	0
0000	0
0111	10.0%

The gain mapping is listed below:

Table 40: TxDAC Look-Up Table

TxPGA gain [3:0]	Gain [dB]	IAMP GAIN[3:0]	FG_CTRL[3:0]
0000	-7.5	1000	0100
0001	-7.0	1000	0111
0010	-6.5	1001	1100
0011	-6.0	1001	0000
0100	-5.5	1001	0100
0101	-5.0	1010	1101
0110	-4.5	1010	1001
0111	-4.0	1010	0011
1000	-3.5	1011	1011
1001	-3.0	1011	0001
1010	-2.5	1011	0101
1011	-2.0	1100	1000
1100	-1.5	1100	0011

TxPGA gain [3:0]	Gain [dB]	IAMP GAIN[3:0]	FG_CTRL[3:0]
1101	-1.0	1101	1001
1110	-0.5	1101	0011
1111	0.0	1110	0000

The maximum current delivered to the load can be calculated as follows. The full-scale current IFS,DAC is equal to the sum of the differential currents labeled 'I' in the figure below. This full scale current of the TxDAC is set by IFS and FG_CTRL setting. This current is then fed into the IAMP which offers an additional gain of N=IAMP_GAIN[3:0]. This result in a total output current given by:

IOUTFS=N x (IFS,DAC + dc_off)

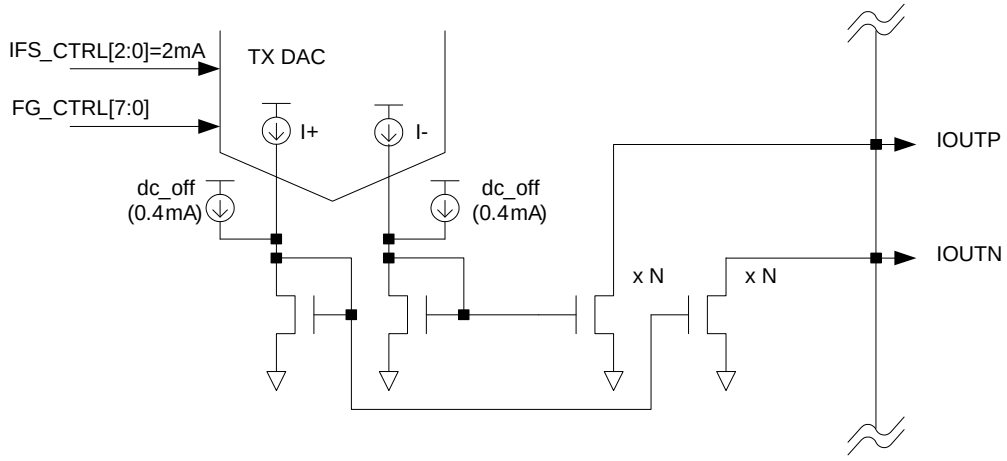


Figure 18: Equivalent Schematic of TxDAC

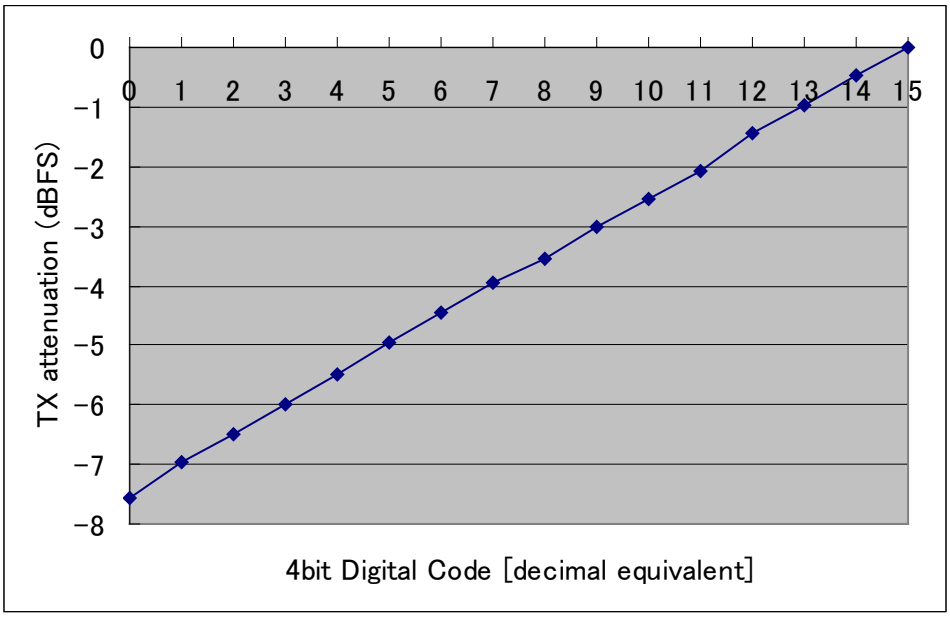


Figure 19: Digital Gain Mapping of TxPGA: (a)Tx Attenuation

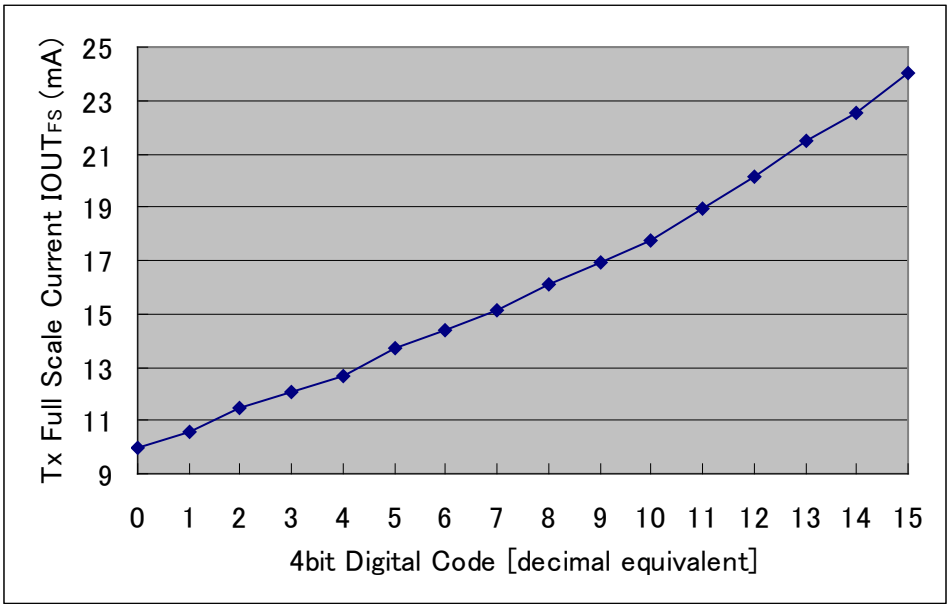


Figure 20: Digital Gain Mapping of TxPGA: (b) Tx Full Scale Output Current.

Typical Tx Path Operation

For loads that remain relatively constant, the IAMP can be operated as shown in the figure below. In this operation, the signal-dependent current from the IAMP is delivered to the load resistance Rload via a center-

tapped transformer, as this result in the best linearity performance. Because the current mirrors in the IAMP exhibit high output impedance, they can be easily back-terminated if needed. The transformer should be able to handle the DC standing current IOUTFS, drawn by the IAMP. If needed a series resistance can be inserted in front of the center tap of the transformer to lower the common mode output level of the IAMP. This voltage should not exceed 6V.

Depending on the load resistance and the transformation ratio, a bigger voltage excursion will be seen at the IOUTN and IOUTP nodes. Voltages swing above 5.8 V will degrade the linearity.

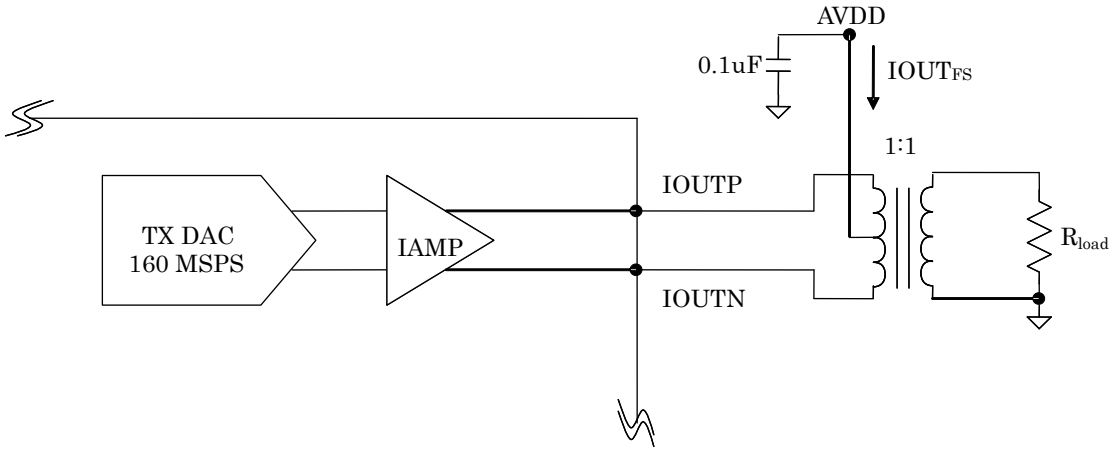


Figure 21: Typical Tx Path Operation

5.3.3. Clock Synthesizer

The clock generation module includes a phase-locked loop and the clock generation circuitry necessary to provide required clocks to various parts of the chip.The input of the clock generation block is the output of the crystal oscillator buffer. This signal is directly connected the power-on reset block which starts the reset sequence as soon as oscillation is detected.

Architecture Overview

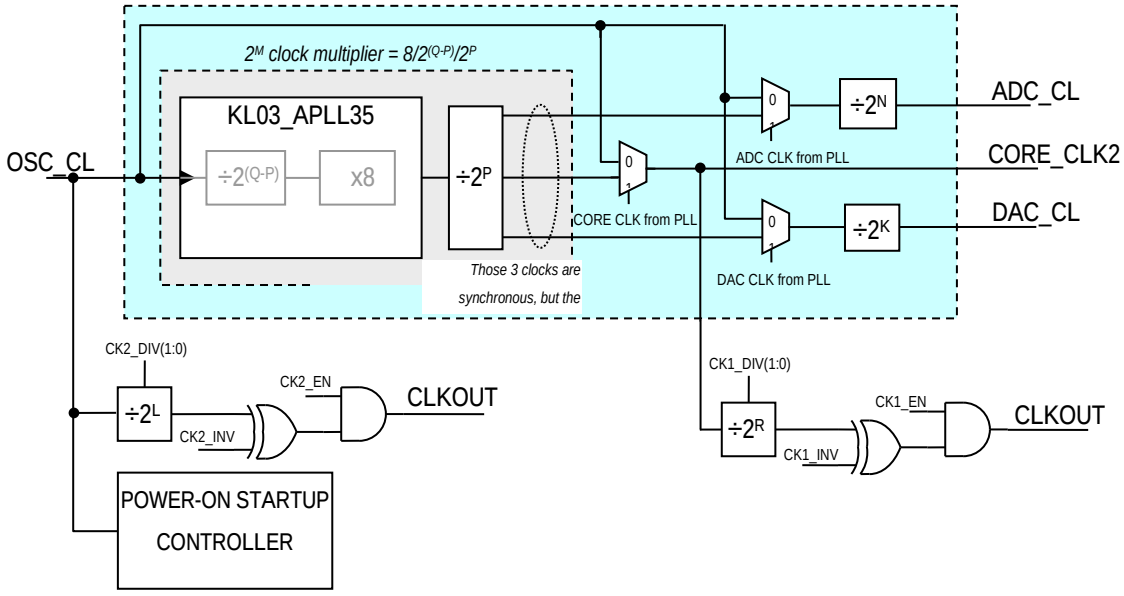


Figure 22: Top-level block diagram of clock generation

Functional Description

Multiplication and division selection

The clock generation circuit is designed to support various crystal oscillator frequencies, fOSCIN. According to the architecture presented in Section 5.3.3 Clock Synthesizer, the clock frequencies for the Tx path (DAC), Rx path (ADC) and core can be calculated as followed:

fCORE = fOSCIN * 2M

fDAC = fCORE / 2K

fADC = fCORE / 2N

2M = 8 / 2(Q-P) / 2P

fVCO = fOSCIN * 8 / 2(Q-P)

The data rate, fDR, for the Tx and Rx paths must always be equal. The ADC's sample rate, fADC, is always equal to fDR. The Tx path update rate, fDAC, is a factor of 1 or 2 of fDR, depending on the interpolation OFF or ON, respectively.

The fOSCIN multiplier, 2M, is a multiple of 1, 2, 4, or 8 of fOSCIN, and contains a PLL and VCO functions. The 2P should be set to 2 usually. The input frequency range of fOSCIN is between 16 MHz and 80 MHz, then the frequency range of fVCO is between 32 MHz and 1280 MHz. But, the real frequency range of fVCO is 100 to 350 MHz. For the best phase noise/jitter characteristics, the fVCO should be set between 120 MHz and 320 MHz.

The table below shows the example of fOSCIN=16MHz/32MHz/80MHz. Other configuration can be applied for each desired crystal frequency.

Table 41: PLL Configuration Example

f_{OSCIN} (MHz)	PLL Multiplier-M		f_{CORE} (MHz)	PLL Frequency Mode		f_{VCO} (MHz)	DAC clock divide-K		f_{DAC} (MSPS)	ADC clock divide-N		f_{ADC} (MSPS)
	2^M	0x04[1:0]		2^P	0x04[7]		2^K	0x04[3]		2^N	0x04[2]	
16	4	10	64	2	1	128	2	1	32	2	1	32
16	4	10	64	2	1	128	1	0	64	2	1	32
16	4	10	64	2	1	128	1	0	64	1	0	64
32	2	01	64	2	1	128	2	1	32	2	1	32
32	2	01	64	2	1	128	1	0	64	2	1	32
32	2	01	64	2	1	128	1	0	64	1	0	64
32	4	10	128	2	1	256	2	1	64	2	1	64
32	4	10	128	2	1	256	1	0	128	2	1	64
80	1	00	80	2	1	160	2	1	40	2	1	40
80	1	00	80	2	1	160	1	0	80	2	1	40
80	1	00	80	2	1	160	1	0	80	1	0	80
80	2	01	160	2	1	320	2	1	80	2	1	80
80	2	01	160	2	1	320	1	0	160	2	1	80

5.3.4. Serial Peripheral Interface (SPI)

Overview

The serial peripheral interface is a serial interface connected to a register bank that contains all the control and test signals of AFE part of MLKHN1501. This register is accessed thru a 3- or 4-wire serial interface, at a maximum update rate of 2 MSPS (SCLK = 32 MHz), either in write or read mode.

The register contains a maximum of 20 bytes (0x00 to 0x13), as shown in Section 5.3.4 Serial Peripheral Interface (SPI). The serial peripheral interface supports both single- and multi-byte update (up to 4 consecutive bytes). Upon reset, the register is configured depending on the state of MODE and CONFIG.

Special register bank for RxPGA (0x09)

In addition to being configurable through the Serial Peripheral Interface, the RxPGA code stored in the register bank can also be accessed thru the PGA input (asynchronously). Due to this requirement, the register bank unit for the RxPGA needs to be different than the standard one.

The SPI register has 3 bit settings that control the way the PGA register is updated. These 3 bits are: enable RxPGA update via SPI and select RxPGA via PGA(5:0). They are configured as followed.

Table 42: SPI Register for RxPGA

Enable RxPGA update via SPI	Select RxPGA via PGA[5:0]	Mode of operation
SPI 0x09(6)	SPI 0x0B(5) [1]	
0	1	RxPGA updated via PGA(5:0) [3]
1	X	RxPGA updated via SPI [2]
X	0	RxPGA updated via SPI [2]

Note 1: It is important to note that when SPI 0x09(6) is high, the RxPGA cannot be updated via PGA(5:0), even if their respective enable signals are high.

Note 2: When SPI 0x09(6) goes from low to high, the value of SPI 0x09(5:0) of the same SPI cycle will be stored in the RxPGA gain register.

Note 3: When SPI 0x09(6) goes from high to low, the registered value of SPI 0x09(5:0) will be directly updated to the value of PGA(5:0) if SPI 0x0B(5) is high. This means that the gain value must be present at the PGA(5:0) input when SPI 0x0B(5)=1 prior to updating SPI 0x09(6) otherwise the value stored in the PGA register will be unknown.

Special register bank for TxPGA (0x0A)

In addition to being configurable through the Serial Peripheral Interface, the TxPGA code stored in the register bank can also be accessed thru the PGA input asynchronously. Due to this requirement, the register bank unit for the TxPGA needs to be different than the standard one.

The SPI register has 2 bit settings that control the way the TxPGA register is updated. These 2 bits are: enable TxPGA update via SPI and select TxPGA via PGA(3:0). Since the datasheet doesn't indicate which setting takes control when both are active, the following has been used:

Table 43: SPI Register for TxPGA

Enable TxPGA update via SPI	Select TxPGA via PGA[3:0]	Mode of operation
SPI 0x0A(6)	SPI 0x0B(6) [1]	
0	1	TxPGA updated via PGA(3:0) [3]
1	X	TxPGA updated via SPI [2]
X	0	TxPGA updated via SPI [2]

Note 1: It is important to note that when SPI 0x0A(6) is high, the TxPGA cannot be updated via PGA(3:0).

Note 2: When SPI 0x0A(6) goes from low to high, the value of SPI 0x0A(3:0) of the same SPI cycle will be stored in the TxPGA gain register

Note 3: When SPI 0x0A(6) goes from high to low, the registered value of SPI 0x0A(3:0) will be directly updated to the value of PGA(3:0) if SPI 0x0B(6) is high. This means that the gain value must be present at the PGA(3:0) input when SPI 0x0B(6)=1 prior to updating SPI 0x0A(6) otherwise the value stored in the PGA register will be unknown.

Functional description and timings

Regular modes of operations

The serial peripheral interface of MLKHN1501 AFE part is either a 3-wire or a 4wire interface. In 3-wire mode, serial communication consists of a clock (SCLK), an enable signal (SENZ) and a bidirectional data signal (SDIO). In 4-wire mode, the output data appears on a 3-stated output pin (SDO) instead of SDIO.

Serial communication starts when SENZ=0. For the next 8 SCLK cycles after a falling edge of SENZ, an instruction header is read on SDIO. The 8-bit instruction header is defined as followed:

MSB							LSB
7	6	5	4	3	2	1	0
R/$\overline{W}$	N1	N0	A4	A3	A2	A1	A0

N1	N0	Nb. bytes
0	0	1
0	1	2
1	0	3

1	1	4

The MSB is a R/$\overline{W}$ (read/write) signal with bit logic 1 indicating a read operation. The following two bits, N1 and N0, indicate how many bits are going to be transferred during the cycle. The last 5 bits, A4 to A0, specify the address of the first register to be accessed. The address is binary coded, as followed:

A4..A0	Register	A4..A0	Register	A4..A0	Register
00000	0x00	01000	0x08	10000	0x10
00001	0x01	01001	0x09	10001	0x11
00010	0x02	01010	0x0A	10010	0x12
00011	0x03	01011	0x0B	10011	0x13
00100	0x04	01100	0x0C		
00101	0x05	01101	0x0D		
00110	0x06	01110	0x0E		
00111	0x07	01111	0x0F		

The serial peripheral interface also supports both MSB first and LSB first data format. The bit order is controlled by the signal stored in Register 0, Bit 6. A low-level indicates MSB first. After the address has been read, the serial interface will either start a read or a write sequence.

In case of a read sequence, the eight data bits stored in the register specified by the address A4..A0 will be shifted out on either SDIO or SDO on the falling edge of the serial clock SCLK. In case of a multi-byte operation, the address is either decremented (if the mode is MSB first) or incremented (if the mode is LSB first) and the eight bit data of the register specified by the new address is shifted out. The process repeats itself until all the bytes specified in the instruction header (N1, N0) have been read.

In case of a write sequence, the input SDIO is shifted in on the rising edge if SCLK and the 8-bit data are stored into the register specified by the address A4..A0 at the end of the sequence. In case of a multi-byte operation, the address is either decremented (if the mode is MSB first) or incremented (if the mode is LSB first) and the input data is shifted into the register specified by the new address. The process repeats itself until all the bytes specified in the instruction header (N1, N0) have been written and the register is finally updated after all bytes have been read.

If the enable signal SENZ stays low at the end of the sequence, then a new cycle (starting with instruction header) is started. Otherwise, if SENZ goes high, the serial port interface is disabled.

Register Mapping

The following table lists the SPI register mapping for MLKHN1501. The colors indicate:

Light-blue: same mapping as AD9866

Light-yellow: functionality is different from AD9866, but no firmware change is required and signal is enabled also

Light-green: SPI-register is read-only

Please note that setting CONFIG has been abbreviated CFG for readability. Only setting MODE=0 is available.

Table 44: SPI Register Mapping

Address	Bit	Description	Power-up default				Comments
			MODE=0		MODE=1		
			CFG 0	CFG 1	CFG 0	CFG 1	
SPI PORT CONFIGURATION AND SOFTWARE RESET							
0x00	7	4-wire SPI	0	0			By default, SPI configuration is 3-wire MSB First.
	6	LSB First	0	0			
	5	S/W reset	0	0			Global reset.
	4	Tx path reset	0	0			reset Interpolation Filter and TxFIFO
	3	Rx path reset	0	0			reset RxFIFO
	2						
	1						
	0						
POWER CONTROL REGISTERS (PWD=0)							
0x01	7	Clock Syn.	0	0			When PWD=0, SPI0x01 settings are enabled (All blocks are powered on by default).

Address	Bit	Description	Power-up default				Comments
	6	TxDAC	0	0			1: powered off / 0:powered on
	5	Tx Digital	0	0			
	4	Bias generator	0	0			
	3	IAMP	0	0			
	2	ADC	0	0			
	1	Rx Digital	0	0			
	0	RxPGA	0	0			
POWER CONTROL REGISTERS (PWD=1)							
0x02	7	Clock Syn.	0	0			When PWD=1, SPI0x02 settings are enabled. (All blocks are powered off, except PLL). 1: powered off / 0:powered on
	6	TxDAC	1	1			
	5	Tx Digital	1	1			
	4	Bias generator	1	1			
	3	IAMP	1	1			
	2	ADC	1	1			
	1	Rx Digital	1	1			
	0	RxPGA	1	1			
HALF-DUPLEX POWER CONTROL							
0x03	7	Tx OFF Delay[4]	1	1			Tx OFF Delay[4:0] sets delay from TxDigital disable to TxAnalog(DAC,IAMP) powered down. Default setting is 31 TxCLK cycle delay.
	6	Tx OFF Delay[3]	1	1			

Address	Bit	Description	Power-up default				Comments
	5	Tx OFF Delay[2]	1	1			
	4	Tx OFF Delay[1]	1	1			
	3	Tx OFF Delay[0]	1	1			
	2	Rx_TXEN / Tx_TXQUIETZ	1	1			1: Rx/Tx path power control can be done through only TXEN under RXEN Low. 0:Rx path power control by RXEN / Tx path by TXEN *:in any cases of this setting, if both RXEN and TXEN are set High, the both paths are powered on and digital data interface ADIO is set to an output mode(RX mode)
	1	Tx PWRDN	1	1			0: TxPath cannot be powered down through TXEN/RXEN
	0	Rx PWRDN	1	1			0: RxPath cannot be powered down through TXEN/RXEN
PLL CLOCK MULTIPLIER CONTROL							
0x04	7	PLL Frequency Mode	1	1			1: HF mode(2^P=2), 0: LF mode(2^P=1)
	6	f_{DAC} from PLL	0	1			DAC clock select. 1: from PLL, 0: from OCSIN
	5	Duty Cycle Enable	0	0			Default setting is Duty Cycle Restore disabled
	4	f_{ADC} from PLL	0	1			ADC clock select. 1: from PLL, 0: from OCSIN
	3	DAC clock divide-K	0	0			1: divide-by-2, (*4)
	2	ADC clock divide-N	1	1			1: divide-by-2, (*4)
	1	PLL Multiplier-M (1,2,4 and 8) [1]	0	1			00: x1, 01: x2, 10: x4, 11: x8 Configurable using strap-in function
	0	PLL Multiplier-M (1,2,4 and 8) [0]	1	0			
CLOCK SYNTHESIZER CONTROL							

Address	Bit	Description	Power-up default				Comments
0x05	7	f_{CORE} from PLL	1	1			Core clock select. 1: from PLL, 0: from OCSIN
	6						
	5						
	4						
	3						
	2	OSCIN to RXCLK_OUT	N/A	N/A			
	1	Invert RXCLK_OUT	N/A	N/A			
	0	Disabled RXCLK_OUT	N/A	N/A			
CLOCKOUT CONTROL							
0x06	7	CLKOUT2 Divide [1]	0	0			00: no divide, 01: divide-by-2, 10: divide-by-4, 11:divide-by-8.
	6	CLKOUT2 Divide [0]	0	0			
	5	CLKOUT2 Invert	0	0			
	4	CLKOUT2 Disable	0	0			
	3	CLKOUT1 Divide [1]	0	0			00: no divide, 01: divide-by-2, 10: divide-by-4, 11:divide-by-8
	2	CLKOUT1 Divide [0]	1	1			
	1	CLKOUT1 Invert	0	0			
	0	CLKOUT1 Disable	0	0			
Rx CONTROL AND TUNING							
0x07	7	Initiate LPFTUNE	0	0			restart LPFTUNE
	6						
	5	Initiate DCTUNE	0	0			restart DCTUNE
	4	Enable DCTUNE	1	1			0:Disable(initialize) / 1:Enable
	3	Enable LPFTUNE	1	1			0:Disable(initialize) / 1:Enable
	2	Bypass LPF and PGA	0	0			1:connect RXP/RXN pin input to ADC input

Address	Bit	Description	Power-up default				Comments
							directly
	1						
	0	Bypass LPF	0	0			1:disable LPF function on PGA
0x08	7						
	6						
	5						
	4						
	3						
	2						
	1						
	0						
Rx GAIN CONTROL							
0x09	7						
	6	Enable RxPGA update via SPI	0	0			Default setting is for hardware Rx gain code via PGA
	5	RxPGA Gain Code [5]	0	0			
	4	RxPGA Gain Code [4]	0	0			
	3	RxPGA Gain Code [3]	0	0			
	2	RxPGA Gain Code [2]	0	0			
	1	RxPGA Gain Code [1]	0	0			
	0	RxPGA Gain Code [0]	0	0			
Tx GAIN CONTROL							
0x0A	7						
	6	Enable TxPGA update via SPI	1	1			Default setting is for Tx gain via SPI control
	5	Bypass IAMP	0	0			1:Bypass DAC output to IOUTP/IOUTN
	4	DAC Current Up	0	0			DAC output current. 0: 2mA, 1: 3.143mA
	3	TxPGA Gain Code [3]	1	1			
	2	TxPGA Gain Code [2]	1	1			
	1	TxPGA Gain Code [1]	1	1			
	0	TxPGA Gain Code [0]	1	1			

Address	Bit	Description	Power-up default				Comments
Tx AND RxPGA CONTROL							
0x0B	7						
	6	Select TxPGA via PGA[3:0]	0	0			Default setting is RxPGA control active.
	5	Select RxPGA via PGA[5:0]	1	1			
	4						
	3						
	2						
	1						
	0	Invert IOUTN.IOUTP polarity	0	0			Active High
Tx DIGITAL FILTER AND INTERFACE							
0x0C	7						
	6	Enable Interpolation Filter	1	1			Default is 2x interpolation
	5						
	4	Invert TXEN/TXSYNC	0	0			Active High
	3						
	2	Tx LS Nibble First	N/A	N/A			
	1	TXCLK neg. edge	0	0			
	0	Twos complement	0	0			0: straight binary 1:twos complement
Rx INTERFACE AND ANALOG/DIGITAL LOOPBACK							
0x0D	7	Analog Loopback	0	0			
	6	Legacy Digital Loopback	0	0			
	5	Rx Port 3-State	N/A	N/A			
	4	Invert RXEN/RXSYNC	0	0			
	3						

Address	Bit	Description	Power-up default				Comments
	2	Rx LS Nibble First	N/A	N/A			
	1	RXCLK neg. edge	0	0			
	0	Twos complement	0	0			
TxDAC OUTPUT AND FIFO BYPASS							
0x0E	7						
	6						
	5						
	4						
	3						
	2	Bypass TXFIFO	0	0			
	1	Bypass RxFIFO	0	0			
	0	Bypass Loopback FIFO	0	0			
REVISION ID							
0x0F	7	AFE status [2]					xtal buffer is stable
	6	AFE status [1]					all the clocks are stable
	5	AFE status [0]					Rx path is ready, which means ADC is ready and DCTUNE and LPFTUNE has done.
	4	Rev. ID Number [4]	1	1			
	3	Rev. ID Number [3]	1	1			
	2	Rev. ID Number [2]	0	0			
	1	Rev. ID Number [1]	1	1			
	0	Rev. ID Number [0]	0	0			
Rx LPF COEFFICIENT for CUT-OFF FREQUENCY CONTROL							
0x10	7						

Address	Bit	Description	Power-up default				Comments
	6	LPFTUNE Coefficient [6]	1	1			This setting can be updated to LPF if SPI0x07[0](Bypass LPF) is 0 and SPI0x07[3](Enable LPFTUNE) is 1. LPFTUNE Coefficient[6:0] is a multiplication factor for LPF cut-off frequency in enabled LPFTUNE. Its data type is unsigned fixed point number. [6] is an integer number part. [5:0] is a decimal number part. ex) 7'b1000000 : x1 7'b0100000 : x0.5 7'b0010000 : x0.25 7'b1110000 : x1.75
	5	LPFTUNE Coefficient [5]	0	0			
	4	LPFTUNE Coefficient [4]	0	0			
	3	LPFTUNE Coefficient [3]	0	0			
	2	LPFTUNE Coefficient [2]	0	0			
	1	LPFTUNE Coefficient [1]	0	0			
	0	LPFTUNE Coefficient [0]	0	0			
SLEEP MODE CONDITION							
0x11	7	DAC sleep in RX	1	1			1:When powering down Tx path, DAC is set to sleep mode
	6						
	5	ADC sleep in TX	1	1			1:When powering down Rx path, ADC is set to sleep mode
	4						
	3						
	2						
	1						
	0						
PLL SETTINGS							
0x12	7						
	6						
	5						

Address	Bit	Description	Power-up default				Comments
	4	Bypass PLL	0	0			1: SPI0x04[4],[6], 0x05[7] setting are ignored and f_{ADC}, f_{DAC}, f_{CORE} clock from OSCIN 0: SPI0x04[4],[6], 0x05[7] setting are enabled
	3						
	2						
	1						
	0						
PLL SETTINGS							
0x13	7						
	6						
	5	ADC Clock Phase Selection [2]	0	0			
	4	ADC Clock Phase Selection [1]	0	0			
	3	ADC Clock Phase Selection [0]	0	0			
	2	DAC Clock Phase Selection [2]	0	0			
	1	DAC Clock Phase Selection [1]	0	0			
	0	DAC Clock Phase Selection [0]	0	0			
Address Space Selection and Revision ID							
0x1F	7	Register Access Control [2]	0	0			000: access to control registers 111: access to status registers Others: K-Micro use only
	6	Register Access Control [1]	0	0			
	5	Register Access Control [0]	0	0			
	4	Revision ID Bit [4]	0	0			Read Only
	3	Revision ID Bit [3]	0	0			
	2	Revision ID Bit [2]	0	0			
	1	Revision ID Bit [1]	0	0			
	0	Revision ID Bit [0]	1	1			

6. Package

The figure below shows the package outline of MLKHN1501 (LBGA-238 pins).

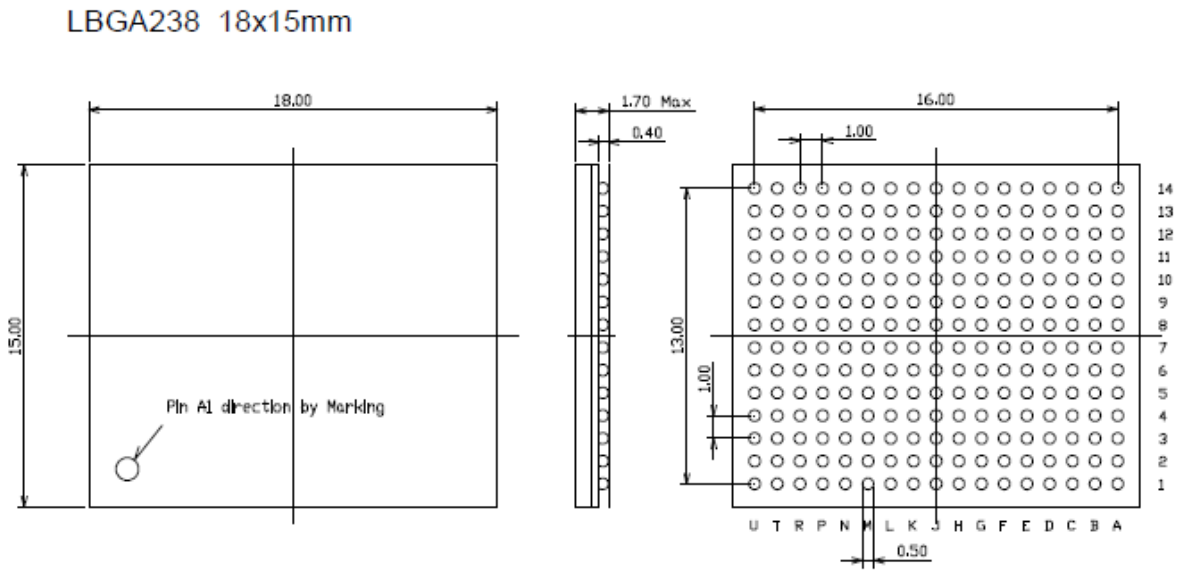


Figure 23:MLKHN1501 package outline (LBGA-238 pins)

7. Ordering Information

Part Number	Package	Description	Refresh cycle
MLKHN1501A	LBGA-238 pins	HD-PLC Data Processing SiP w/ 128Mbit SDRAM	4K refresh cycles/16mS
MLKHN1501B	LBGA-238 pins	HD-PLC Data Processing SiP w/ 256Mbit SDRAM	8K refresh cycles/16mS

The refresh cycle must be changed in Boot ROM.

8. Appendix

8.1. Serial Flash ROM Specifications

- Capacity Min. 2Mbytes

Recommended Device:

- Macronix "MX25L series"
- WinBond "W25Q series"
- STMicroelectronics "M25P series"

8.2. Ethernet PHY Specifications

- 10 BASE-T and 100 BASE-TX supported
- MII specification supported
- RMII specification supported
- TMII specification supported

Recommended Device:

- Microchips(Micrel) Inc. "KSZ8041NL", "KSZ8081MNX"

8.3. Crystal Oscillator Specifications

- Output frequency 31.25 MHz
- Allowable deviation Within ± 25 ppm (recommended)

8.4. PLL Board Design Recommendations

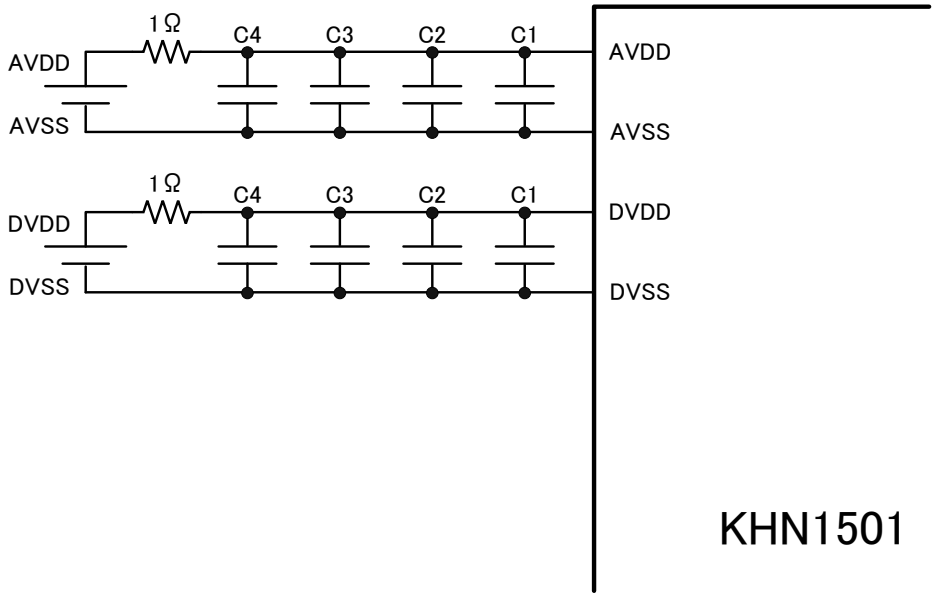


Figure 24: PCB Recommendation circuit

Minimum required PLL power supply filters are indicated in the figure above and board components must be implemented to meet the following requirement.

- For IR drop consideration, 1Ω register of the filter is recommended for loading PLL current only.
- Choose SMD ceramic high-frequency capacitors:
  - Choose SMD ceramic high-frequency capacitors C1 which serial resonance frequency (SRF) is close to 500MHz.
  - Choose SMD ceramic high-frequency capacitors C2 and C3 by the relationship with C1. (C1, C2 and C3 must be the same produce series and dimension.)

    C2 = C1×2, C3 = C2×2

  - Choose SMD ceramic high-frequency capacitors C4 by composing C_Total to form a less than 100KHz pole of power supply filter.

    Fc_filter = 1/(2×pi×C_Total) < 100KHz

  - All SMD ceramic high-frequency capacitors best be placed as close as to power and ground pins and shorten the current loop as short as possible.
  - Use wide traces for power and ground path.

- Minimize the loop area from AVDD to AVSS and from DVDD to DVSS. Besides, take care of layout to avoid coupling noise from adjacent digital signals or digital power traces.

8.5. Power Up/Down Sequence

This section explains power up and down sequence. Ideally, all the power supplies have to be stable at the same time to prevent the direct feed-through current. However, there will be a time difference among the power supplies in reality. So this section will explain the restrictions of the time difference among the power supplies.

1. Power On : 1.2V Core Power Supply is on first.

   Power Off : 1.2V Core Power Supply is off last.

   Refer to the figure below. In this case, the restrictions are as follows:

   Tlag1, Tlag2 < 500ms

   Ton, Toff < 500ms

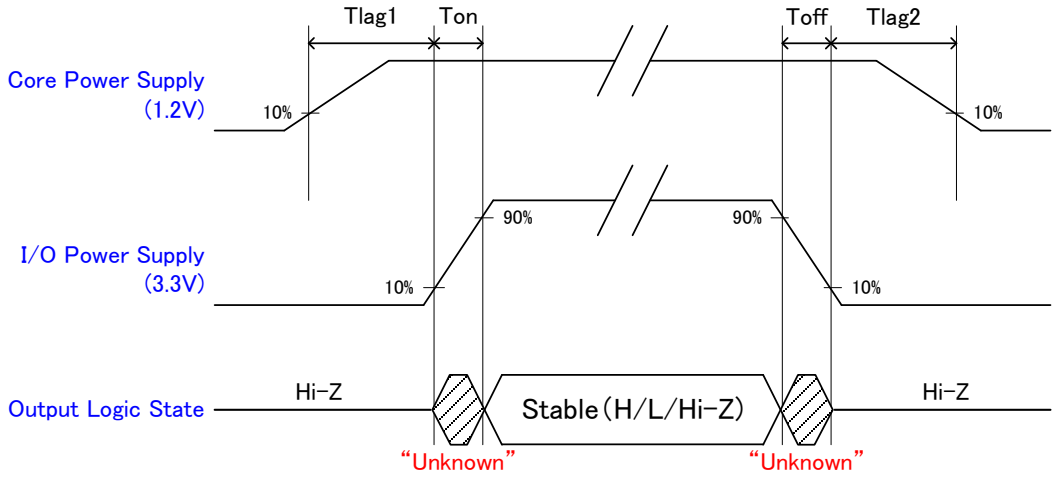


Figure 25: Power Up/Down Sequence - 1

   * The output logic at the Tlag1 period and Tlag2 period are "Hi-Z".

   * The output logic at the Ton period and the Toff period are unknown.

2. Power On : 3.3V I/O Power Supply is on first.

   Power Off : 3.3V I/O Power Supply is off last.

   Refer to the figure below. In this case, the restrictions are as follows:

Tlag1, Tlag2 < 500ms

Ton, Toff < 500ms

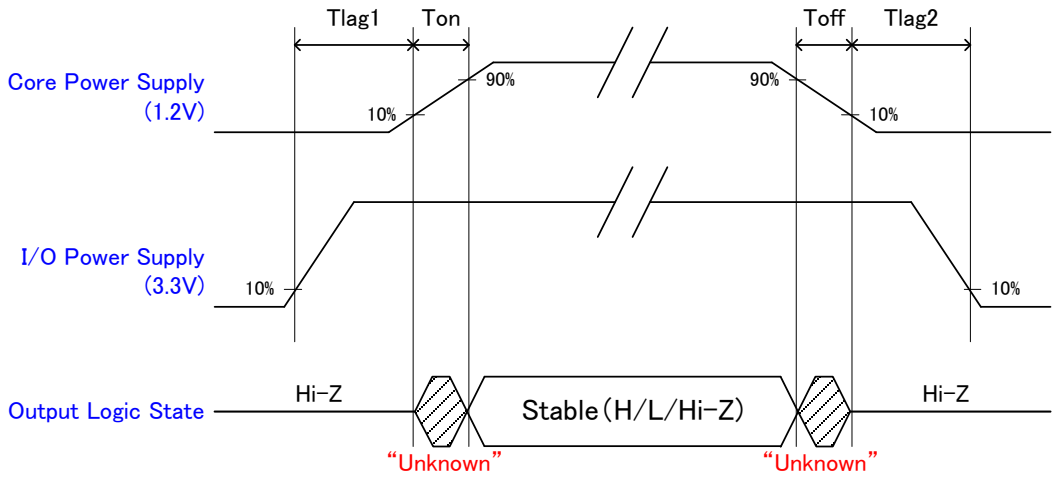


Figure 26: Power Up/Down Sequence - 2

* The output logic at the Tlag1 period and Tlag2 period are "Hi-Z".

* The output logic at the Ton period and Toff period are unknown.

3. Other Case

Please follow the restrictions in accordance with Case.1 and 2.

(1) Power On : 1.2V Core Power Supply is on first.

Power Off : 1.2V Core Power Supply is off first.

In this case, you should follow Case.1 for Power Up and Case.2 for Power Down.

(2) Power On : 3.3V I/O Power Supply is on first.

Power Off : 3.3V I/O Power Supply is off first.

In this case, you should follow Case.2 for Power Up and Case.1 for Power Down.

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