

MC14027B

Dual J-K Flip-Flop

The MC14027B dual J-K flip-flop has independent J, K, Clock (C), Set (S) and Reset (R) inputs for each flip-flop. These devices may be used in control, register, or toggle functions.

Features

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Swing Independent of Fanout
- Logic Edge-Clocked Flip-Flop Design
- Logic State is Retained Indefinitely with Clock Level Either High or Low; Information is Transferred to the Output Only on the Positive-Going Edge of the Clock Pulse
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4027B
- Pb-Free Packages are Available*

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	± 10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	-55 to +125	$^{\circ}C$
T_{stg}	Storage Temperature Range	-65 to +150	$^{\circ}C$
T_L	Lead Temperature (8-Second Soldering)	260	$^{\circ}C$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}C$ From 65 $^{\circ}C$ To 125 $^{\circ}C$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

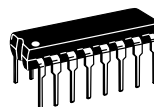
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



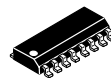
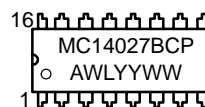
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<http://onsemi.com>

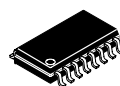
MARKING DIAGRAMS



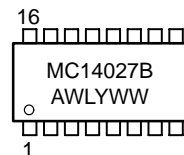
PDIP-16
P SUFFIX
CASE 648



SOIC-16
D SUFFIX
CASE 751B



SOEIAJ-16
F SUFFIX
CASE 966



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

MC14027B

TRUTH TABLE

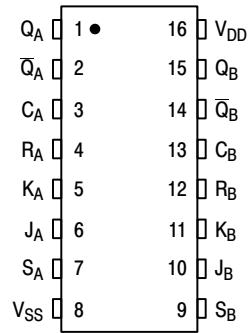
Inputs					Outputs*		
C†	J	K	S	R	Q _n ‡	Q _{n+1}	Q̄ _{n+1}
↗	1	X	0	0	0	1	0
↗	X	0	0	0	1	1	0
↗	0	X	0	0	0	0	1
↗	X	1	0	0	1	0	1
↗	1	1	0	0	Q ₀	Q̄ ₀	Q ₀
↘	X	X	0	0	X	Q _n	Q̄ _n
X	X	X	1	0	X	1	0
X	X	X	0	1	X	0	1
X	X	X	1	1	X	1	1

X = Don't Care
† = Level Change

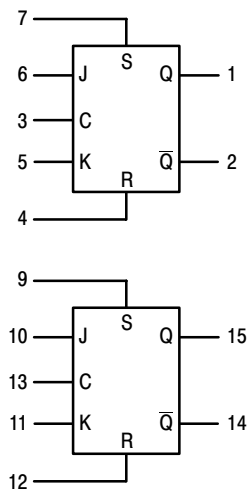
‡ = Present State
* = Next State

No
Change

PIN ASSIGNMENT



BLOCK DIAGRAM



V_{DD} = PIN 16
V_{SS} = PIN 8