

3.3 V ECL Programmable Delay Chip



MC100EP195

The MC100EP195 is a Programmable Delay Chip (PDC) designed primarily for clock deskewing and timing adjustment. It provides variable delay of a differential NECL/PECL input transition.

The delay section consists of a programmable matrix of gates and multiplexers as shown in the logic diagram, Figure 3. The delay increment of the EP195 has a digitally selectable resolution of about 10 ps and a net range of up to 10.2 ns. The required delay is selected by the 10 data select inputs D[9:0] values and controlled by the LEN (pin 10). A LOW level on LEN allows a transparent LOAD mode of real time delay values by D[9:0]. A LOW to HIGH transition on LEN will LOCK and HOLD current values present against any subsequent changes in D[10:0]. The approximate delay values for varying tap numbers correlating to D0 (LSB) through D9 (MSB) are shown in Table 6 and Figure 4.

Because the EP195 is designed using a chain of multiplexers it has a fixed minimum delay of 2.2 ns. An additional pin D10 is provided for controlling Pins 14 and 15, CASCADE and $\overline{\text{CASCADE}}$, also latched by LEN, in cascading multiple PDCs for increased programmable range. The cascade logic allows full control of multiple PDCs. Switching devices from all “1” states on D[0:9] with SETMAX LOW to all “0” states on D[0:9] with SETMAX HIGH will increase the delay equivalent to “D0”, the minimum increment.

Select input pins D[10:0] may be threshold controlled by combinations of interconnects between V_{EF} (pin 7) and V_{CF} (pin 8) for LVCMOS, ECL, or LVTTL level signals. For LVCMOS input levels, leave V_{CF} and V_{EF} open. For ECL operation, short V_{CF} and V_{EF} (Pins 7 and 8). For LVTTL level operation, connect a 1.5 V supply reference to V_{CF} and leave open V_{EF} pin. The 1.5 V reference voltage to V_{CF} pin can be accomplished by placing a 2.2 k Ω resistor between V_{CF} and V_{EE} for a 3.3 V power supply.

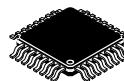
The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The 100 Series contains temperature compensation.

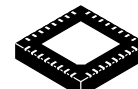
- Maximum Input Clock Frequency >1.2 GHz Typical
- Programmable Range: 0 ns to 10 ns
- Delay Range: 2.2 ns to 12.2 ns
- 10 ps Increments
- PECL Mode Operating Range:
 - $V_{CC} = 3.0 \text{ V to } 3.6 \text{ V with } V_{EE} = 0 \text{ V}$
- NECL Mode Operating Range:
 - $V_{CC} = 0 \text{ V with } V_{EE} = -3.0 \text{ V to } -3.6 \text{ V}$
- Open Input Default State
- Safety Clamp on Inputs
- A Logic High on the $\overline{\text{EN}}$ Pin Will Force Q to Logic Low
- D[10:0] Can Accept Either ECL, LVCMOS, or LVTTL Inputs
- V_{BB} Output Reference Voltage
- These are Pb-Free Devices

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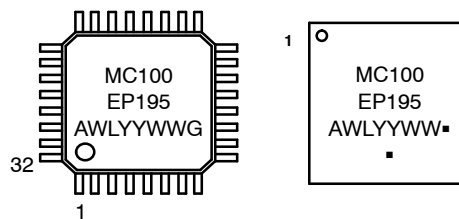


**LQFP-32
FA SUFFIX
CASE 561AB**



**QFN32
MN SUFFIX
CASE 488AM**

MARKING DIAGRAMS*



- A = Assembly Location
- WL, L = Wafer Lot
- YY, Y = Year
- WW, W = Work Week
- G or ■ = Pb-Free Package

(Note: Microdot may be in either location)
*For additional marking information, refer to Application Note [AND8002/D](#).

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 15 of this data sheet.

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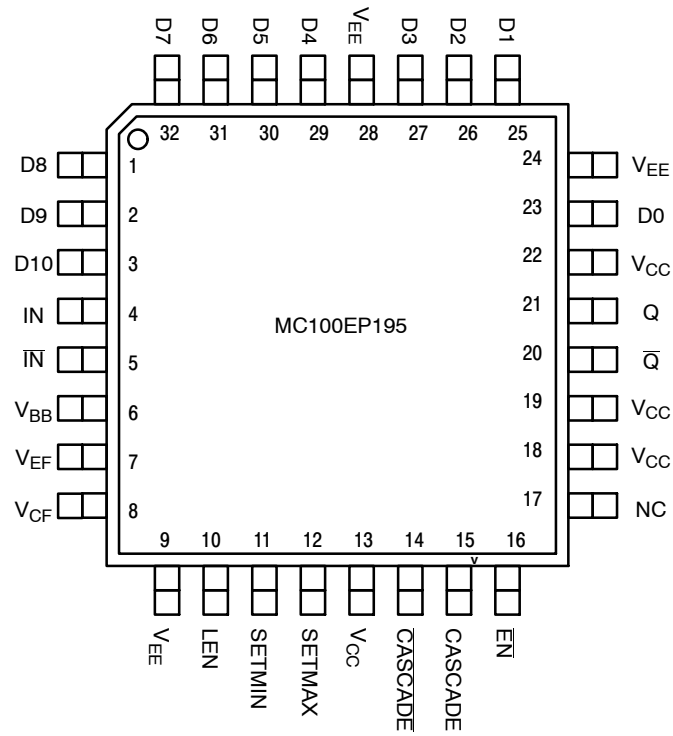


Figure 1. 32-Lead LQFP Pinout (Top View)

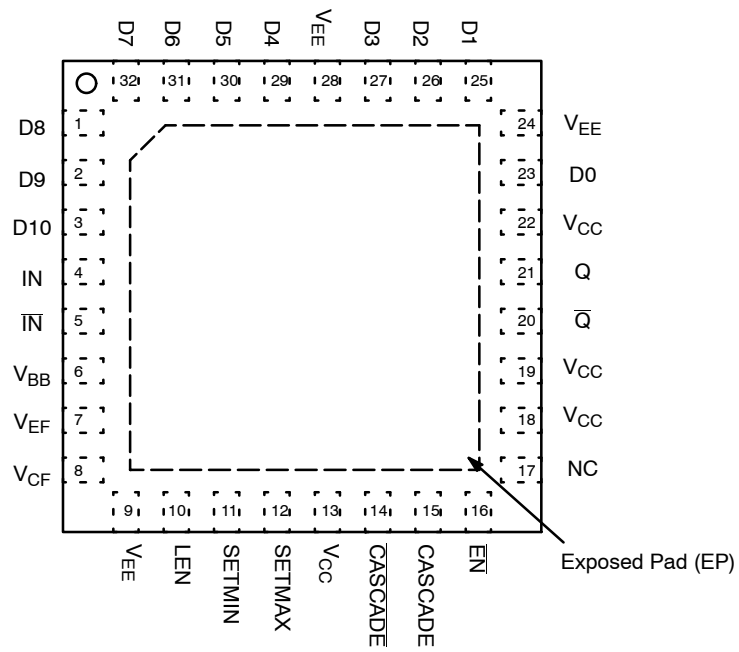


Figure 2. 32-Lead QFN (Top View)

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Table 1. PIN DESCRIPTION

| Pin | Name | I/O | Default State | Description |
|--------------------------------------|-----------------------------|----------------------------|---------------|--|
| 23, 25, 26, 27, 29, 30, 31, 32, 1, 2 | D[0:9] | LVC MOS, LV TTL, ECL Input | Low | Single-Ended Parallel Data Inputs [0:9]. Internal 75 k Ω to V _{EE} . (Note 1) |
| 3 | D[10] | LVC MOS, LV TTL, ECL Input | Low | Single-Ended CASCADE/CASCADE Control Input. Internal 75 k Ω to V _{EE} . (Note 1) |
| 4 | IN | ECL Input | Low | Noninverted Differential Input. Internal 75 k Ω to V _{EE} . |
| 5 | $\overline{\text{IN}}$ | ECL Input | High | Inverted Differential Input. Internal 75 k Ω to V _{EE} and 36.5 k Ω to V _{CC} . |
| 6 | V _{BB} | - | - | ECL Reference Voltage Output |
| 7 | V _{EF} | - | - | Reference Voltage for ECL Mode Connection |
| 8 | V _{CF} | - | - | LVC MOS, ECL, OR LV TTL Input Mode Select |
| 9, 24, 28 | V _{EE} | - | - | Negative Supply Voltage. All V _{EE} Pins must be Externally Connected to Power Supply to Guarantee Proper Operation. (Note 2) |
| 13, 18, 19, 22 | V _{CC} | - | - | Positive Supply Voltage. All V _{CC} Pins must be externally Connected to Power Supply to Guarantee Proper Operation. (Note 2) |
| 10 | LEN | ECL Input | Low | Single-ended D pins LOAD / HOLD input. Internal 75 k Ω to V _{EE} . |
| 11 | SETMIN | ECL Input | Low | Single-ended Minimum Delay Set Logic Input. Internal 75 k Ω to V _{EE} . (Note 1) |
| 12 | SETMAX | ECL Input | Low | Single-ended Maximum Delay Set Logic Input. Internal 75 k Ω to V _{EE} . (Note 1) |
| 14 | $\overline{\text{CASCADE}}$ | ECL Output | - | Inverted Differential Cascade Output for D[10]. Typically Terminated with 50 Ω to V _{TT} = V _{CC} - 2 V. |
| 15 | CASCADE | ECL Output | - | Noninverted Differential Cascade Output. for D[10] Typically Terminated with 50 Ω to V _{TT} = V _{CC} - 2 V. |
| 16 | $\overline{\text{EN}}$ | ECL Input | Low | Single-ended Output Enable Pin. Internal 75 k Ω to V _{EE} . |
| 17 | NC | - | - | No Connect. The NC Pin is Electrically Connected to the Die and "MUST BE" Left Open. |
| 21 | Q | ECL Output | - | Noninverted Differential Output. Typically Terminated with 50 Ω to V _{TT} = V _{CC} - 2 V. |
| 20 | $\overline{\text{Q}}$ | ECL Output | - | Inverted Differential Output. Typically Terminated with 50 Ω to V _{TT} = V _{CC} - 2 V. |

1. SETMIN will override SETMAX if both are high. SETMAX and SETMIN will override all D[0:10] inputs.
2. All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

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Table 2. CONTROL PIN

| Pin | State | Function |
|--------|--------------|--|
| EN | LOW (Note 3) | Input Signal is Propagated to the Output |
| | HIGH | Output Holds Logic Low State |
| LEN | LOW (Note 3) | Transparent or LOAD mode for real time delay values present on D[0:10]. |
| | HIGH | LOCK and HOLD mode for delay values on D[0:10]; further changes on D[0:10] are not recognized and do not affect delay. |
| SETMIN | LOW (Note 3) | Output Delay set by D[0:10] |
| | HIGH | Set Minimum Output Delay |
| SETMAX | LOW (Note 3) | Output Delay set by D[0:10] |
| | HIGH | Set Maximum Output Delay |
| D10 | LOW (Note 3) | CASCADE Output LOW, CASCADE Output HIGH |
| | HIGH | CASCADE Output LOW, CASCADE Output HIGH |

3. Internal pulldown resistor will provide a logic LOW if pin is left unconnected.

Table 3. CONTROL D[0:10] INTERFACE

| | | |
|----------|-----------------------|---------------------|
| V_{CF} | V_{EF} Pin (Note 4) | ECL Mode |
| V_{CF} | No Connect | LVC MOS Mode |
| V_{CF} | 1.5 V \pm 100 mV | LVTTL Mode (Note 5) |

4. Short V_{CF} (pin 8) and V_{EF} (pin 7).

5. When Operating in LVTTL Mode, the reference voltage can be provided by connecting an external resistor, R_{CF} (suggested resistor value is 2.2 k Ω \pm 5%), between V_{CF} and V_{EE} pins.

Table 4. DATA INPUT ALLOWED OPERATING VOLTAGE MODE TABLE

| POWER SUPPLY | CONTROL DATA SELECT INPUTS PINS (D [0:10]) | | | |
|---------------------------|--|-------|--------|--------|
| | LVC MOS | LVTTL | LVPECL | LVNECL |
| PECL Mode Operating Range | YES | YES | YES | N/A |
| NECL Mode Operating Range | N/A | N/A | N/A | YES |

Table 5. ATTRIBUTES

| Characteristics | Value |
|---|-----------------------------|
| Internal Input Pulldown Resistor (R1) | 75 k Ω |
| ESD Protection Human Body Model Machine Model Charged Device Model | > 2 kV > 100 V > 2 kV |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 6) | Pb-Free Pkg |
| LQFP-32 | Level 2 |
| QFN-32 | Level 1 |
| Flammability Rating Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in |
| Transistor Count | 1217 Devices |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | |

6. For additional information, see Application Note [AND8003/D](#).

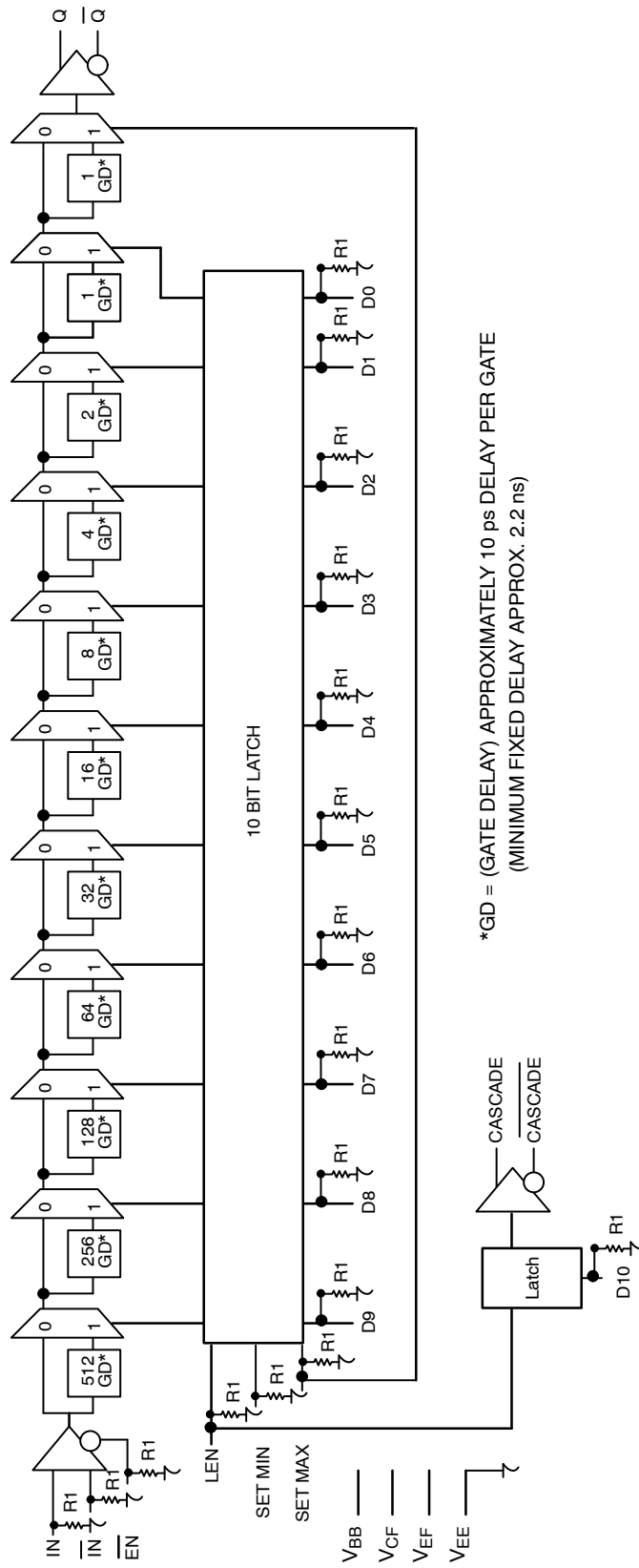


Figure 3. Logic Diagram

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Table 6. THEORETICAL DELAY VALUES

| D(9:0) Value | SETMIN | SETMAX | Programmable Delay* |
|--------------|--------|--------|---------------------|
| XXXXXXXXXX | H | L | 0 ps |
| 000000000 | L | L | 0 ps |
| 000000001 | L | L | 10 ps |
| 000000010 | L | L | 20 ps |
| 000000011 | L | L | 30 ps |
| 000000100 | L | L | 40 ps |
| 000000101 | L | L | 50 ps |
| 000000110 | L | L | 60 ps |
| 000000111 | L | L | 70 ps |
| 000001000 | L | L | 80 ps |
| 000010000 | L | L | 160 ps |
| 000100000 | L | L | 320 ps |
| 001000000 | L | L | 640 ps |
| 010000000 | L | L | 1280 ps |
| 100000000 | L | L | 5120 ps |
| 111111111 | L | L | 10230 ps |
| XXXXXXXXXX | L | H | 10240 ps |

*Fixed minimum delay not included.

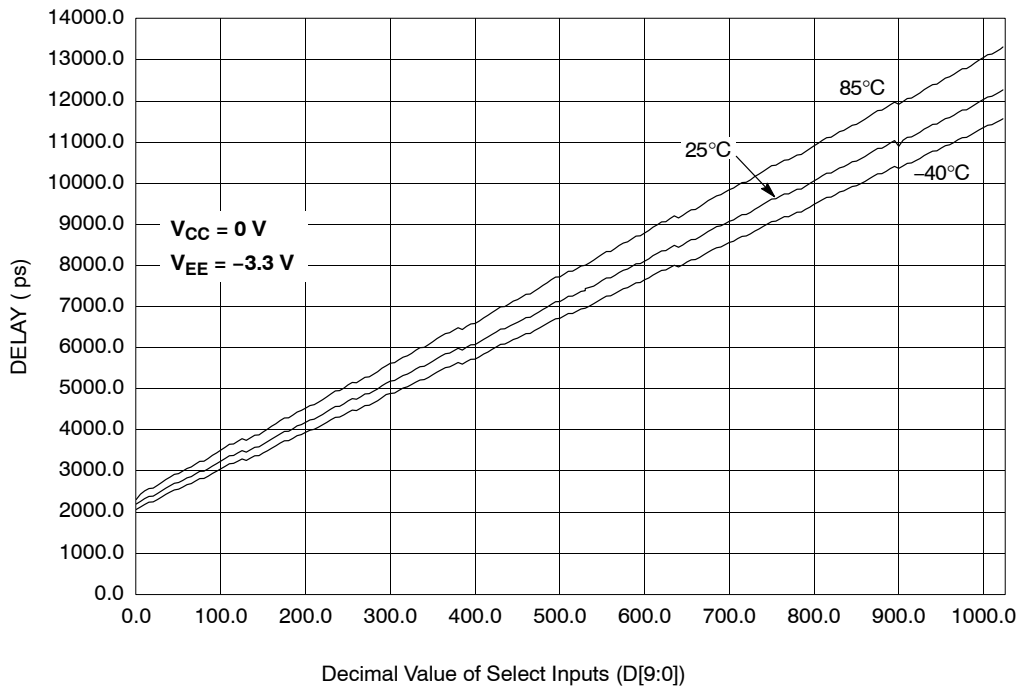


Figure 4. Measured Delay vs. Select Inputs

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Table 7. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|---------------|--|-----------------------|--------------------------------------|-------------|-----------------------------|
| V_{CC} | Positive Mode Power Supply | $V_{EE} = 0\text{ V}$ | | 6 | V |
| V_{EE} | Negative Mode Power Supply | $V_{CC} = 0\text{ V}$ | | -6 | V |
| V_I | Positive Mode Input Voltage | $V_{EE} = 0\text{ V}$ | $V_I \leq V_{CC}$ | 6 | V |
| | Negative Mode Input Voltage | $V_{CC} = 0\text{ V}$ | $V_I \geq V_{EE}$ | -6 | V |
| I_{out} | Output Current | Continuous Surge | | 50 | mA |
| | | | | 100 | mA |
| I_{BB} | V_{BB} Sink/Source | | | ± 0.5 | mA |
| T_A | Operating Temperature Range | | | -40 to +85 | $^{\circ}\text{C}$ |
| T_{stg} | Storage Temperature Range | | | -65 to +150 | $^{\circ}\text{C}$ |
| θ_{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lfpm | LQFP-23 | 80 | $^{\circ}\text{C}/\text{W}$ |
| | | 500 lfpm | LQFP-23 | 55 | $^{\circ}\text{C}/\text{W}$ |
| θ_{JC} | Thermal Resistance (Junction-to-Case) | Standard Board | LQFP-23 | 12 to 17 | $^{\circ}\text{C}/\text{W}$ |
| θ_{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lfpm | QFN-32 | 31 | $^{\circ}\text{C}/\text{W}$ |
| | | 500 lfpm | QFN-32 | 27 | $^{\circ}\text{C}/\text{W}$ |
| θ_{JC} | Thermal Resistance (Junction-to-Case) | 2S2P | QFN-32 | 12 | $^{\circ}\text{C}/\text{W}$ |
| T_{sol} | Wave Solder | Pb-Free | <2 to 3 sec @ 260 $^{\circ}\text{C}$ | 265 | $^{\circ}\text{C}$ |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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Table 9. 100EP DC CHARACTERISTICS, NECL $V_{CC} = 0\text{ V}$, $V_{EE} = -3.3\text{ V}$ (Note 10)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|---|--------------|-------------|-------|--------------|-------------|-------|--------------|-------------|-------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Negative Power Supply Current (Note 11) | 100 | 135 | 160 | 100 | 140 | 170 | 100 | 145 | 175 | mA |
| V_{OH} | Output HIGH Voltage (Note 12) | -1145 | -1020 | -895 | -1145 | -1020 | -895 | -1145 | -1020 | -895 | mV |
| V_{OL} | Output LOW Voltage (Note 12) | -1995 | -1820 | -1695 | -1995 | -1820 | -1695 | -1995 | -1820 | -1695 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) LVNECL | -1225 | | -880 | -1225 | | -880 | -1225 | | -880 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) LVNECL | -1995 | | -1625 | -1995 | | -1625 | -1995 | | -1625 | mV |
| V_{BB} | ECL Output Voltage Reference | -1525 | -1425 | -1325 | -1525 | -1425 | -1325 | -1525 | -1425 | -1325 | mV |
| V_{EF} | Reference Voltage for ECL Mode Connection | -1380 | -1280 | -1180 | -1380 | -1280 | -1180 | -1380 | -1280 | -1180 | mV |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 13) | $V_{EE}+2.0$ | | 0.0 | $V_{EE}+2.0$ | | 0.0 | $V_{EE}+2.0$ | | 0.0 | V |
| I_{IH} | Input HIGH Current (@ V_{IH}) | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current (@ V_{IL}) | | 0.5 -150 | | | 0.5 -150 | | | 0.5 -150 | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

10. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.3 V to -0.3 V.

11. Recommended $V_{CC} - V_{EE}$ operation at $3.0\text{ V} \leq 3.6\text{ V}$.

12. All loading with $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$.

13. V_{IHCMR} min varies 1:1 with V_{EE} . V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

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Table 10. AC CHARACTERISTICS $V_{CC} = 0\text{ V}$; $V_{EE} = -3.0\text{ V to }-3.6\text{ V}$ or $V_{CC} = 3.0\text{ V to }3.6\text{ V}$; $V_{EE} = 0\text{ V}$ (Note 14)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|------------------------|--|-----------------------------|---|------------------------------|------------------------------|---|------------------------------|------------------------------|--|------------------------------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| f_{max} | Maximum Frequency | | 1.2 | | | 1.2 | | | 1.2 | | GHz |
| t_{PLH} t_{PHL} | Propagation Delay IN to Q; D(0-10) = 0 IN to Q; D(0-10) = 1023 \overline{EN} to Q; D(0-10) = 0 D0 to CASCADE | 1650 9500 1600 300 | 2050 11500 2150 420 | 2450 13500 2600 500 | 1800 10000 1800 350 | 2200 12200 2300 450 | 2600 14000 2800 550 | 1950 10800 2000 425 | 2350 13300 2500 525 | 2750 15800 3000 625 | ps |
| t_{RANGE} | Programmable Range $t_{PD}(\text{max}) - t_{PD}(\text{min})$ | 7850 | 9450 | | 8200 | 10000 | | 8850 | 10950 | | ps |
| Δt | Step Delay (Note 15) D0 High D1 High D2 High D3 High D4 High D5 High D6 High D7 High D8 High D9 High | | 13 27 44 90 130 312 590 1100 2250 4500 | | | 14 30 47 97 140 335 650 1180 2400 4800 | | | 41 100 145 360 690 1300 2650 5300 | | ps |
| mono | Monotonicity (Note 21) | | | | | TBD | | | | | |
| t_{SKEW} | Duty Cycle Skew (Note 16) $ t_{PHL} - t_{PLH} $ | | 25 | | | 25 | | | 25 | | ps |
| t_s | Setup Time D to LEN D to IN (Note 17) EN to IN (Note 18) | 200 300 300 | 0 140 150 | | 200 300 300 | 0 160 170 | | 200 300 300 | 0 180 180 | | ps |
| t_h | Hold Time LEN to D IN to \overline{EN} (Note 19) | 200 400 | 60 250 | | 200 400 | 100 280 | | 200 400 | 80 300 | | ps |
| t_R | Release Time \overline{EN} to IN (Note 20) SET MAX to LEN SET MIN to LEN | 150 400 350 | -25 200 275 | | 150 400 350 | -75 250 200 | | 150 400 350 | -50 300 225 | | ps |
| t_{jitter} | RMS Random Clock Jitter @ 1.2 GHz IN to Q; D(0:10) = 0 or SETMIN IN to Q; D(0:10) = 1023 or SETMAX | | 0.86 0.89 | | | 1.16 1.09 | | | 1.12 1.02 | | ps |
| V_{PP} | Input Voltage Swing (Differential Configuration) | 150 | 800 | 1200 | 150 | 800 | 1200 | 150 | 800 | 1200 | mV |
| t_r t_f | Output Rise/Fall Time @ 50 MHz 20-80% (Q) 20-80% (CASCADE) | 85 100 | 100 140 | 135 200 | 85 110 | 110 150 | 135 200 | 95 130 | 125 170 | 155 220 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm.

14. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 Ω to $V_{CC} - 2.0\text{ V}$.
15. Specification limits represent the amount of delay added with the assertion of each individual delay control pin. The various combinations of asserted delay control inputs will typically realize D0 resolution steps across the specified programmable range.
16. Duty cycle skew guaranteed only for differential operation measured from the cross point of the input to the cross point of the output.
17. This setup time defines the amount of time prior to the input signal the delay tap of the device must be set.
18. This setup time is the minimum time that \overline{EN} must be asserted prior to the next transition of IN/ \overline{IN} to prevent an output response greater than $\pm 75\text{ mV}$ to that IN/ \overline{IN} transition.
19. This hold time is the minimum time that \overline{EN} must remain asserted after a negative going IN or positive going \overline{IN} to prevent an output response greater than $\pm 75\text{ mV}$ to that IN/ \overline{IN} transition.
20. This release time is the minimum time that \overline{EN} must be deasserted prior to the next IN/ \overline{IN} transition to ensure an output response that meets the specified IN to Q propagation delay and transition times.
21. The monotonicity indicates the increasing delay value for each binary count increment on the control inputs D[9:0].

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An expansion of the latch section of the block diagram is pictured in Figure 7. Use of this diagram will simplify the explanation of how the cascade circuitry works. When D10 of chip #1 in Figure 6 is LOW this device's CASCADE output will also be low while the CASCADE output will be high. In this condition the SET MIN pin of chip #2 will be asserted HIGH and thus all of the latches of chip #2 will be reset and the device will be set at its minimum delay.

Chip #1, on the other hand, will have both SET MIN and SET MAX deasserted so that its delay will be controlled entirely by the address bus A0–A9. If the delay needed is greater than can be achieved with 1023 gate delays

(111111111 on the A0–A9 address bus) D10 will be asserted to signal the need to cascade the delay to the next EP195 device. When D10 is asserted, the SET MIN pin of chip #2 will be deasserted and SET MAX pin asserted resulting in the device delay to be the maximum delay. Table 11 shows the delay time of two EP195 chips in cascade.

To expand this cascading scheme to more devices, one simply needs to connect the D10 pin from the next chip to the address bus and CASCADE outputs to the next chip in the same manner as pictured in Figure 6. The only addition to the logic is the increase of one line to the address bus for cascade control of the second programmable delay chip.

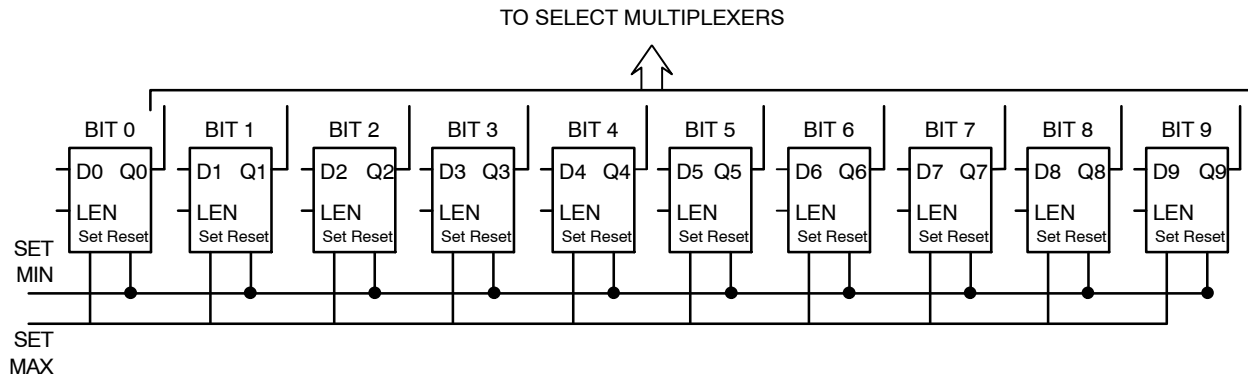


Figure 7. Expansion of the Latch Section of the EP195 Block Diagram

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Table 11. Delay Value of Two EP195 Cascaded

| VARIABLE INPUT TO CHIP #1 AND SETMIN FOR CHIP #2 | | | | | | | | | | | | |
|--|----|----|----|----|----|----|----|----|----|----|-------------|----------------------|
| INPUT FOR CHIP #1 | | | | | | | | | | | Delay Value | Total Delay Value |
| D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 ps | 4400 ps |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 10 ps | 4410 ps |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 20 ps | 4420 ps |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 30 ps | 4430 ps |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 40 ps | 4440 ps |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 50 ps | 4450 ps |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 60 ps | 4460 ps |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 70 ps | 4470 ps |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 80 ps | 4480 ps |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 160 ps | 4560 ps |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 220 ps | 4720 ps |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 640 ps | 5040 ps |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1280 ps | 5680 ps |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 2560 ps | 6960 ps |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 5120 ps | 9520 ps |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 10230 ps | 14630 ps |

| VARIABLE INPUT TO CHIP #1 AND SETMAX FOR CHIP #2 | | | | | | | | | | | | |
|--|----|----|----|----|----|----|----|----|----|----|-------------|----------------------|
| INPUT FOR CHIP #1 | | | | | | | | | | | Delay Value | Total Delay Value |
| D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 10240 ps | 14640 ps |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 10250 ps | 14650 ps |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 10260 ps | 14660 ps |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 10270 ps | 14670 ps |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 10280 ps | 14680 ps |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 10290 ps | 14690 ps |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 10300 ps | 14700 ps |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 10310 ps | 14710 ps |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 10320 ps | 14720 ps |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10400 ps | 14800 ps |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 10560 ps | 14960 ps |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 10880 ps | 15280 ps |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 11520 ps | 15920 ps |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 12800 ps | 17200 ps |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 15360 ps | 19760 ps |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 20470 ps | 24870 ps |

MC100EP195

Multi-Channel Deskewing

The most practical application for EP195 is in multiple channel delay matching. Slight differences in impedance and cable length can create large timing skews within a high-speed system. To deskew multiple signal channels, each channel can

be sent through each EP195 as shown in Figure 8. One signal channel can be used as reference and the other EP195s can be used to adjust the delay to eliminate the timing skews. Nearly any high-speed system can be fine-tuned (as small as 10 ps) to reduce the skew to extremely tight tolerances.

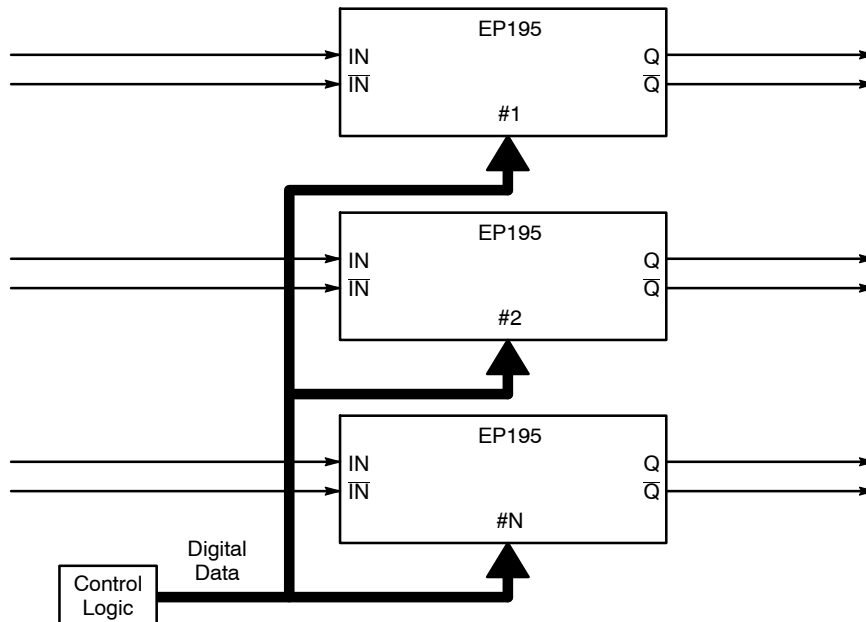


Figure 8. Multiple Channel Deskewing Diagram

Measure Unknown High Speed Device Delays

EP195s provide a possible solution to measure the unknown delay of a device with a high degree of precision. By combining two EP195s and EP31 as shown in Figure 9, the delay can be measured. The first EP195 can be set to SETMIN and its output is used to drive the unknown delay device, which in turn drives the input of a D flip-flop of EP31. The second EP195 is triggered along with the first EP195 and its output provides a clock signal for EP31. The programmed delay of the second EP195 is varied to detect the output edge from the unknown delay device.

If the programmed delay through the second EP195 is too long, the flip-flop output will be at logic high. On the other hand, if the programmed delay through the second EP195 is too short, the flip-flop output will be at a logic low. If the programmed delay is correctly fine-tuned in the second EP195, the flip-flop will bounce between logic high and logic low. The digital code in the second EP195 can be directly correlated into an accurate device delay.

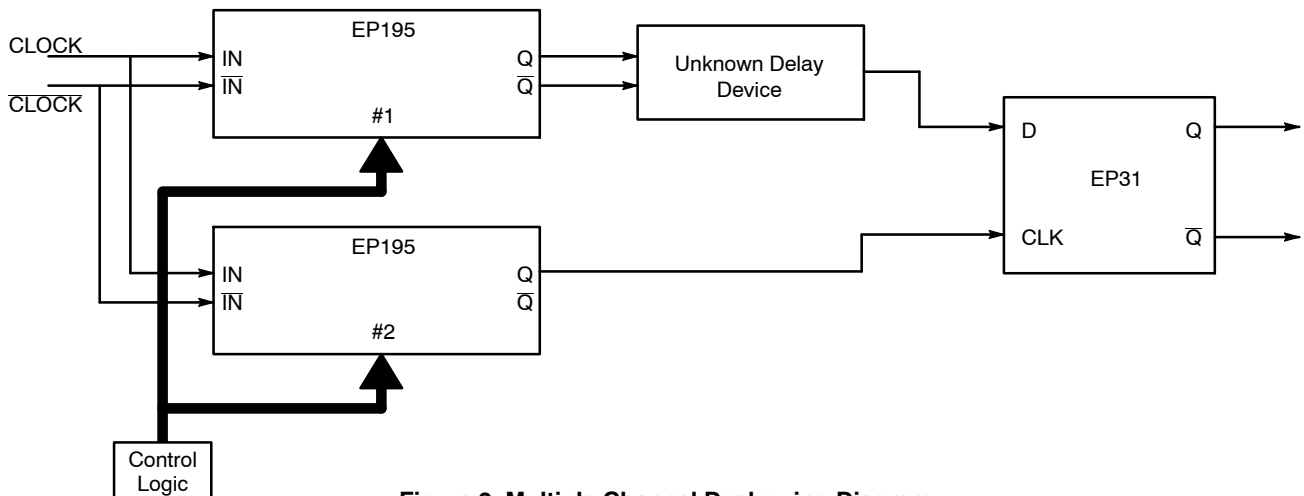


Figure 9. Multiple Channel Deskewing Diagram

MC100EP195

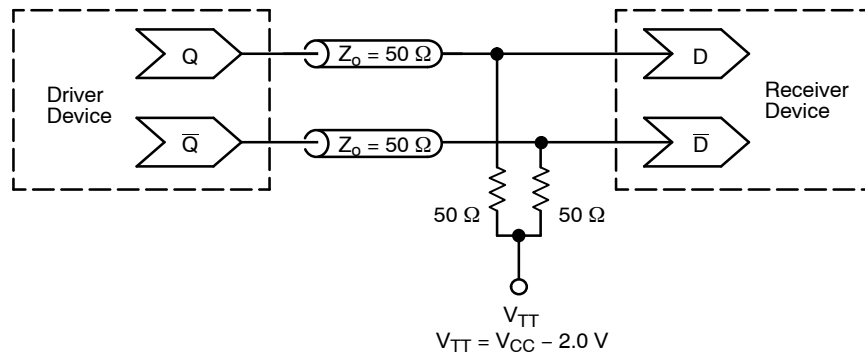


Figure 10. Typical Termination for Output Driver and Device Evaluation
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices.)

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|-----------------|----------------------|-----------------------|
| MC100EP195FAG | LQFP-32 (Pb-Free) | 250 Units / Tray |
| MC100EP195FAR2G | LQFP-32 (Pb-Free) | 2000 / Tape & Reel |
| MC100EP195MNG | QFN-32 (Pb-Free) | 74 Units / Tube |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

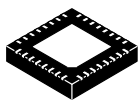
Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

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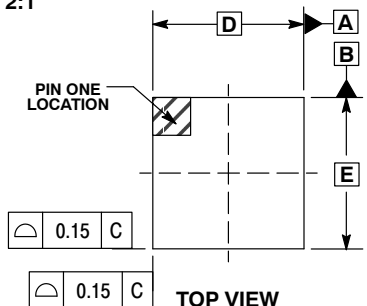


1 32

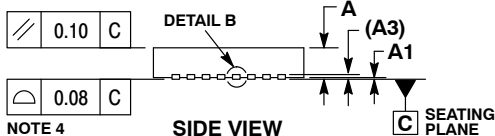
SCALE 2:1

QFN32 5x5, 0.5P
CASE 488AM
ISSUE A

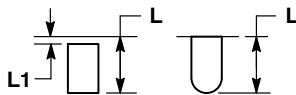
DATE 23 OCT 2013



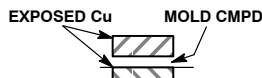
TOP VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL
CONSTRUCTIONS



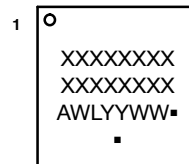
DETAIL B
ALTERNATE
CONSTRUCTION

NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

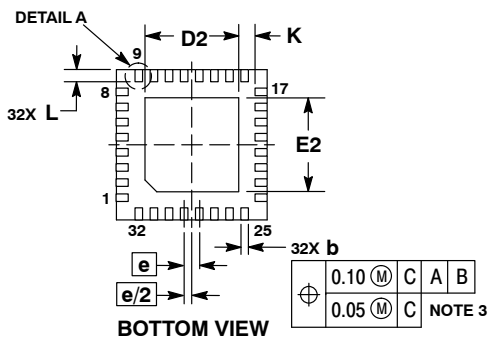
| MILLIMETERS | | |
|-------------|------|------|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | --- | 0.05 |
| A3 | 0.20 | REF |
| b | 0.18 | 0.30 |
| D | 5.00 | BSC |
| D2 | 2.95 | 3.25 |
| E | 5.00 | BSC |
| E2 | 2.95 | 3.25 |
| e | 0.50 | BSC |
| K | 0.20 | --- |
| L | 0.30 | 0.50 |
| L1 | --- | 0.15 |

GENERIC MARKING DIAGRAM*



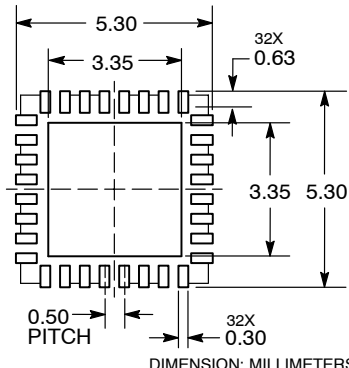
- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)
*This information is generic. Please refer to device data sheet for actual part marking.
Pb-Free indicator, "G" or microdot "▪", may or may not be present.



BOTTOM VIEW

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
|------------------|----------------|--|
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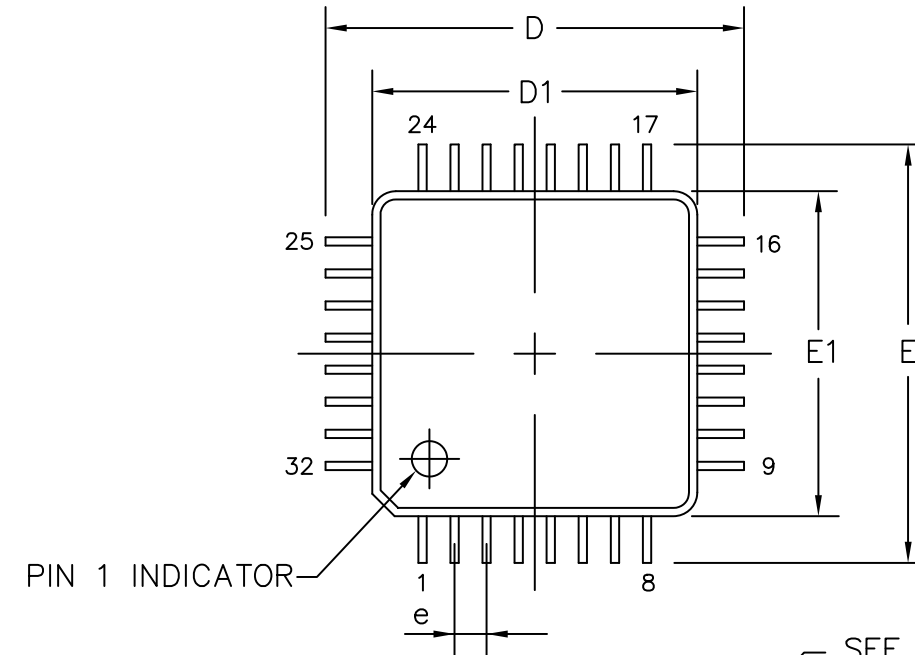
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

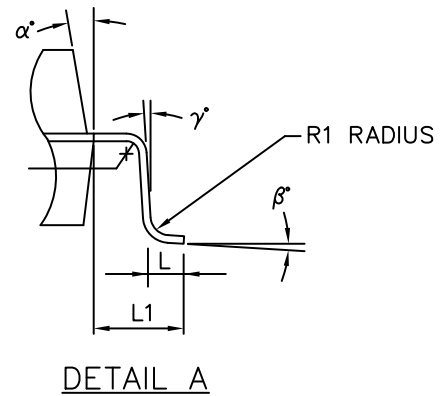
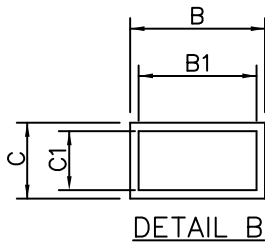
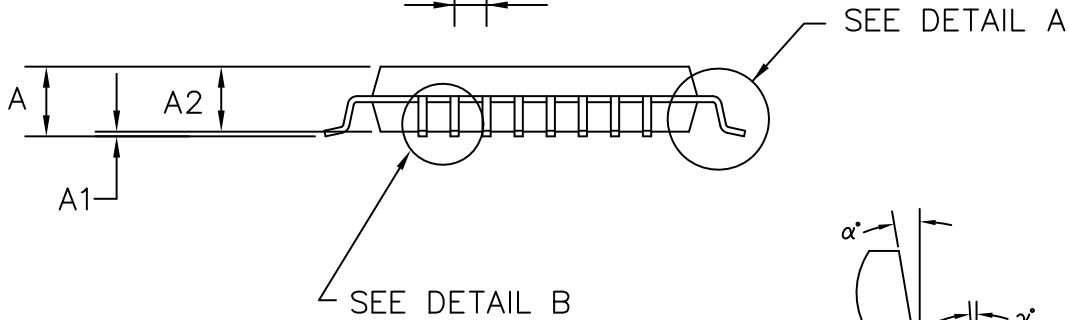


LQFP-32, 7x7
CASE 561AB-01
ISSUE O

DATE 19 JUN 2008




| SYMBOL | MIN | NOM | MAX |
|----------------|----------|------|------|
| A | — | — | 1.60 |
| A1 | 0.05 | — | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| B | 0.30 | 0.37 | 0.45 |
| B1 | 0.30 | 0.35 | 0.40 |
| C | 0.09 | — | 0.20 |
| C1 | 0.09 | — | 0.16 |
| D | 9.00 BSC | | |
| D1 | 7.00 BSC | | |
| E | 9.00 BSC | | |
| E1 | 7.00 BSC | | |
| e | 0.80 BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.00 | | |
| R1 | 0.08 | — | 0.20 |
| α° | 11 | — | 13 |
| β° | 0 | — | 7 |
| γ° | 0 | — | — |



ALL DIMENSIONS IN MM

| | | |
|-------------------------|--------------------------|--|
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| DESCRIPTION: | 32 LEAD LQFP, 7X7 | PAGE 1 OF 1 |

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