

2-Input NAND Schmitt-Trigger with Open Drain Output

NLV74VHC1G135

The NLV74VHC1G135 is a single gate CMOS Schmitt NAND trigger with an open drain output fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffered 3-state output which provides high noise immunity and stable output.

The input structures provide protection when voltages up to 5.5 V are applied, regardless of the supply voltage. This allows the device to be used to interface 5 V circuits to 3 V circuits. Some output structures also provide protection when $V_{CC} = 0$ V and when the output voltage exceeds V_{CC} . These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

Features

- Designed for 2.0 V to 5.5 V V_{CC} Operation
- 4.9 ns t_{PD} at 5 V (typ)
- Inputs/Outputs Over-Voltage Tolerant up to 5.5 V
- I_{OFF} Supports Partial Power Down Protection
- Source/Sink 8 mA at 3.0 V
- Available in SC-88A and TSOP-5 Packages
- Chip Complexity < 100 FETs
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

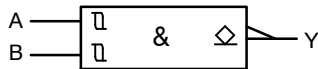
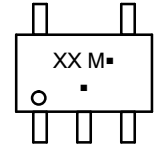


Figure 1. Logic Symbol

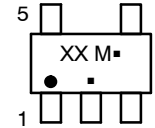
MARKING DIAGRAMS



SC-88A
DF SUFFIX
CASE 419A



TSOP-5
DT SUFFIX
CASE 483



XX = Specific Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 7 of this data sheet.

NLV74VHC1G135

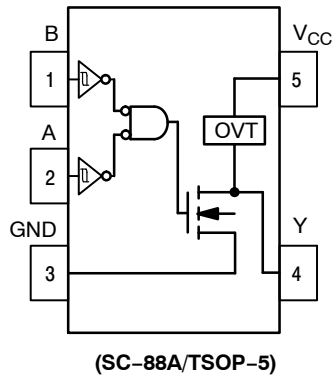


Figure 2. Pinout (Top View)

PIN ASSIGNMENT (SC-88A/TSOP-5)

Pin	Function
1	B
2	A
3	GND
4	Y
5	V _{CC}

FUNCTION TABLE

Input		Output
A	B	Y
L	L	Z
L	H	Z
H	L	Z
H	H	L

NLV74VHC1G135

MAXIMUM RATINGS

Symbol	Characteristics	Value	Unit
V _{CC}	DC Supply Voltage	-0.5 to +7.0	V
V _{IN}	DC Input Voltage	-0.5 to +7.0	V
V _{OUT}	DC Output Voltage	1Gxx	-0.5 to V _{CC} + 0.5
		1GTxx Active-Mode (High or Low State) Tri-State Mode (Note 1) Power-Down Mode (V _{CC} = 0 V)	-0.5 to V _{CC} + 0.5 -0.5 to +7.0 -0.5 to +7.0
I _{IK}	DC Input Diode Current V _{IN} < GND	-20	mA
I _{OK}	DC Output Diode Current	1Gxx V _{OUT} > V _{CC} ; V _{OUT} < GND	±20
		1GTxx V _{OUT} < GND	-20
I _{OUT}	DC Output Source/Sink Current	±25	mA
I _{CC} or I _{GND}	DC Supply Current per Supply Pin or Ground Pin	±50	mA
T _{STG}	Storage Temperature Range	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 secs	260	°C
T _J	Junction Temperature Under Bias	+150	°C
θ _{JA}	Thermal Resistance (Note 2)	SC-88A	377
		TSOP-5	320
P _D	Power Dissipation in Still Air	SC-88A	332
		TSOP-5	390
MSL	Moisture Sensitivity	Level 1	-
F _R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	-
V _{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model	2000
		Charged Device Model	1000
I _{Latchup}	Latchup Performance (Note 4)	±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri-stated.
2. Measured with minimum pad spacing on an FR4 board, using 10mm-by-1inch, 2 ounce copper trace no air flow per JESD51-7.
3. HBM tested to ANSI/ESDA/JEDEC JS-001-2017. CDM tested to EIA/JESD22-C101-F. JEDEC recommends that ESD qualification to EIA/JESD22-A115-A (Machine Model) be discontinued per JEDEC/JEP172A.
4. Tested to EIA/JESD78 Class II.

NLV74VHC1G135

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit		
V_{CC}	Positive DC Supply Voltage	2.0	5.5	V		
V_{IN}	DC Input Voltage	0	5.5	V		
V_{OUT}	DC Output Voltage	1Gxx	0	V_{CC}	V	
		1GTxx	Active-Mode (High or Low State)	0		V_{CC}
			Tri-State Mode	0		5.5
	Power-Down Mode ($V_{CC} = 0$ V)	0	5.5			
T_A	Operating Temperature Range	-55	+125	°C		
t_r, t_f	Input Rise and Fall Time			ns/V		
		$V_{CC} = 3.0$ V to 3.6 V	0	No Limit		
		$V_{CC} = 4.5$ V to 5.5 V	0	No Limit		

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$		$-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		Unit	
				Min	Typ	Max	Min	Max	Min	Max		
V_{T+}	Positive Input Threshold Voltage		3.0	1.2	2.0	2.2	-	2.2	-	2.2	V	
			4.5	1.75	3.0	3.15	-	3.15	-	3.15		
			5.5	2.15	3.6	3.85	-	3.85	-	3.85		
V_{T-}	Negative Input Threshold Voltage		3.0	0.9	1.5	1.9	0.9	-	0.9	-	V	
			4.5	1.35	2.3	2.75	1.35	-	1.35	-		
			5.5	1.65	2.9	3.35	1.65	-	1.65	-		
V_H	Hysteresis Voltage		3.0	0.30	0.85	1.60	0.30	1.60	0.30	1.60	V	
			4.5	0.40	1.05	2.00	0.40	2.00	0.40	2.00		
			5.5	0.50	1.20	2.25	0.50	2.25	0.50	2.25		
V_{OL}	Maximum Low-Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50 \mu\text{A}$	2.0	-	0.0	0.1	-	0.1	-	0.1	V	
			3.0	-	0.0	0.1	-	0.1	-	0.1		
			4.5	-	0.0	0.1	-	0.1	-	0.1		
			$I_{OL} = 4$ mA $I_{OL} = 8$ mA	3.0	-	-	0.36	-	0.44	-	0.52	V
				4.5	-	-	0.36	-	0.44	-	0.52	
I_{IN}	Maximum Input Leakage Current	$V_{IN} = 5.5$ V or GND	2.0 to 5.5	-	-	± 0.1	-	± 1.0	-	± 1.0	μA	
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5	-	-	1.0	-	20	-	40	μA	
I_{OFF}	Power Off Leakage Current	$V_{IN} = 5.5$ V	0.0	-	-	1.0	-	10	-	10	μA	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NLV74VHC1G135

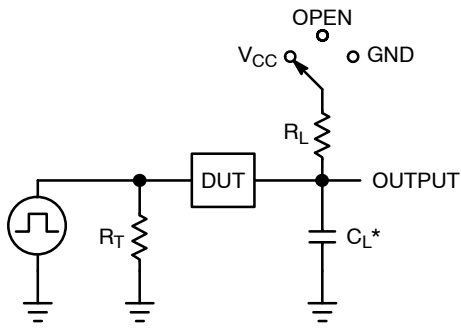
AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25°C			-40°C ≤ T _A ≤ 85°C		-55°C ≤ T _A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t _{PZL}	Propagation Delay, (A or B) to Y (Figures 3 and 4)	C _L = 15 pF	3.0 to 3.6	-	7.6	11.9	-	14.0	-	16.1	ns
		C _L = 50 pF		-	10.1	15.4	-	17.5	-	19.6	
		C _L = 15 pF	4.5 to 5.5	-	4.9	7.7	-	9.0	-	10.3	
		C _L = 50 pF		-	6.4	9.7	-	11.0	-	12.3	
t _{PLZ}	Propagation Delay, (A or B) to Y (Figures 3 and 4)	C _L = 15 pF	3.0 to 3.6	-	7.6	11.9	-	14.0	-	16.1	ns
		C _L = 50 pF		-	10.1	15.4	-	17.5	-	19.6	
		C _L = 15 pF	4.5 to 5.5	-	4.9	7.7	-	9.0	-	10.3	
		C _L = 50 pF		-	6.4	9.7	-	11.0	-	12.3	
C _{IN}	Maximum Input Capacitance			-	5.0	10	-	10	-	10	pF

C _{PD}	Power Dissipation Capacitance (Note 5)	Typical @ 25°C, V _{CC} = 5.0 V	
			16.0

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

NLV74VHC1G135



C_L includes probe and jig capacitance
 R_T is Z_{OUT} of pulse generator (typically 50 Ω)
 $f = 1$ MHz

Figure 3. Test Circuit

Test	Switch Position	C_L , pF	R_L , Ω
t_{PLH} / t_{PHL}	Open	See AC Characteristics Table	X
t_{PLZ} / t_{PZL}	V_{CC}		1 k
t_{PHZ} / t_{PZH}	GND		1 k

X = Don't Care



Figure 4. Switching Waveforms

V_{CC} , V	V_{mi} , V	V_{mo} , V		V_Y , V
		t_{PLH}, t_{PHL}	$t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}$	
3.0 to 3.6	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	0.3
4.5 to 5.5	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	0.3

NLV74VHC1G135

ORDERING INFORMATION

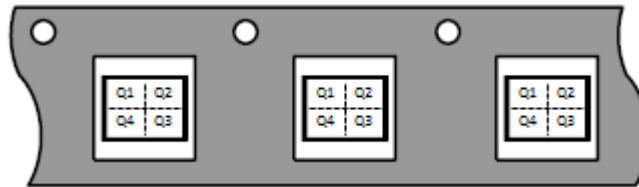
Device	Packages	Specific Device Code	Pin 1 Orientation (See below)	Shipping [†]
M74VHC1G135DFT1G-L22038	SC-88A	VZ	Q2	3000 / Tape & Reel
M74VHC1G135DFT2G-L22038	SC-88A	VZ	Q4	3000 / Tape & Reel
NLVVHC1G135DFT2G*	SC-88A	VZ	Q4	3000 / Tape & Reel
M74VHC1G135DFT1G	TSOP-5	VZ	Q4	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

PIN 1 ORIENTATION IN TAPE AND REEL

Direction of Feed



MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 2:1

SC-88A (SC-70-5/SOT-353) CASE 419A-02 ISSUE M

DATE 11 APR 2023



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.1016MM PER SIDE.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.95	1.10
A1	---	---	0.10
A3	0.20 REF		
b	0.10	0.20	0.30
c	0.10	---	0.25
D	1.80	2.00	2.20
E	2.00	2.10	2.20
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.10	0.15	0.30

GENERIC MARKING DIAGRAM*



*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

XXX = Specific Device Code

M = Date Code

■ = Pb-Free Package

(Note: Microdot may be in either location)

STYLE 1:

1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:

1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 3:

1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:

1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:

1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 6:

1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR
5. COLLECTOR 2/BASE 1

STYLE 7:

1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:

1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

STYLE 9:

1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

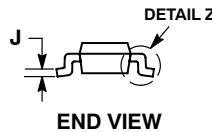
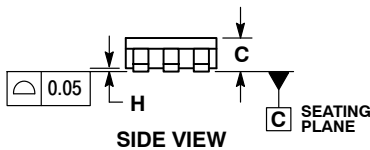
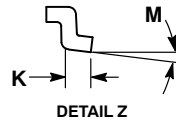
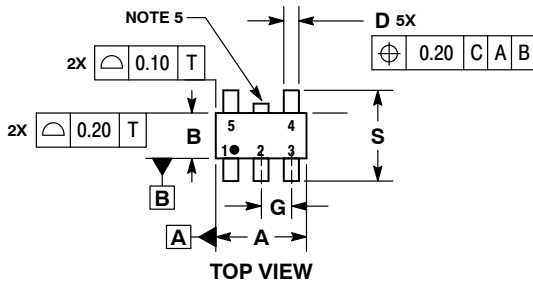
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SCALE 2:1

TSOP-5 CASE 483 ISSUE N

DATE 12 AUG 2020

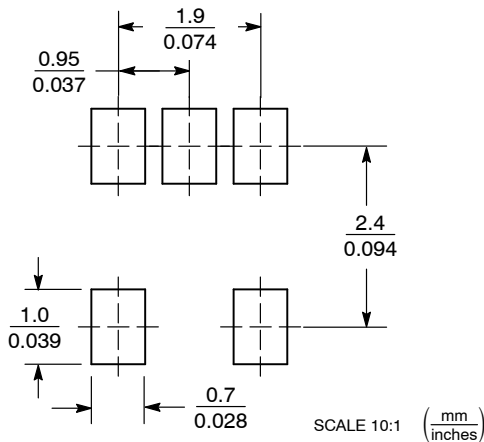


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

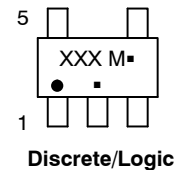
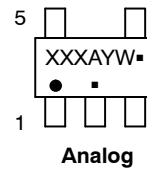
DIM	MILLIMETERS	
	MIN	MAX
A	2.85	3.15
B	1.35	1.65
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0°	10°
S	2.50	3.00

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



- XXX = Specific Device Code XXX = Specific Device Code
 A = Assembly Location M = Date Code
 Y = Year ▪ = Pb-Free Package
 W = Work Week
 ▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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