LX7720

Motor Driver with Four Half-Bridge Drivers, Rotation and Position Sensing for Space

Description

The LX7720 is a spacecraft motor driver that is radiation-hardened by design and works with either a space FPGA controller such as RTG4, RT PolarFire and RTAX-S/SL, or a space MCU such as SAMRH71F20, SAMRH707F18, SAMV71Q21RT, and SAM3X8ERT.

The LX7720 contains four half-bridge drivers with floating current sense for motor coil driving, six bi-level inputs for sensing Hall effect sensors or rotary encoders, and a resolver or LVDT interface to digital with primary coil driver.

The LX7720 works with an FPGA or MCU system controller to provide a complete closed loop motor driver with coil current feedback and rotation or linear position sensing. With flexible programming, the combined system can provide motor control for stepper motors, brushless DC and permanent magnet motors. Position sensing supports encoders, Hall effect sensors, resolvers, synchros, and LVDTs.

FPGA and MCU IP modules are available to support motor driving functions from open loop cardinal step driving to space vector modulation using field-oriented control.

The LX7720 contains 7 sigma delta modulators for analog sampling. Sinc³ filtering and decimation is performed in the FPGA or microcontroller with available IP modules. Four of the modulators sample the voltage across floating current sense inputs and three modulators sample differential analog inputs such as the outputs of a resolver transformer. Speed versus accuracy tradeoffs can be exploited.

The LX7720 supports a ground potential difference between the motor and signal grounds in the range of -10V to +8V and motor supply voltages up to 60V. Resolver or LVDT carrier frequencies from 360Hz to 20kHz are supported.

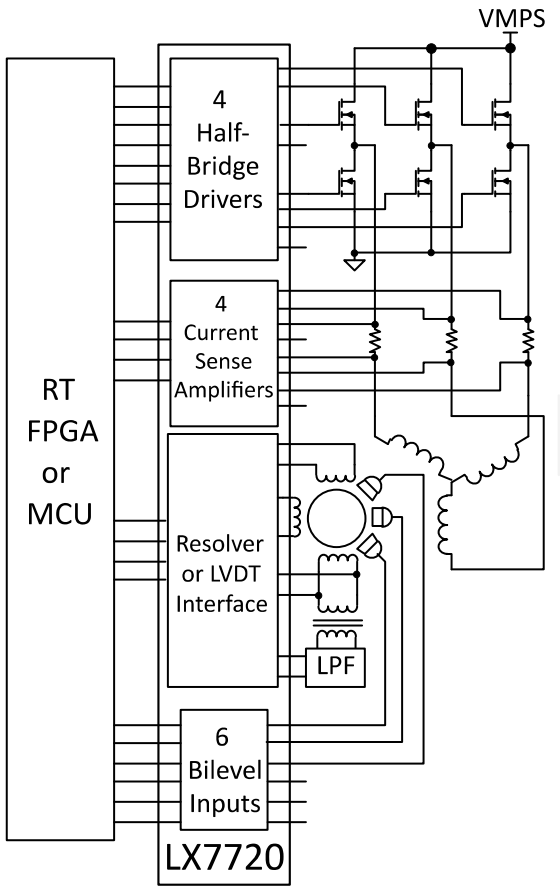
The LX7720MFQ is packaged in a 132 pin hermetic ceramic quad flat pack. The LX7720MLF is packaged in a lead-free 160 pin non-hermetic plastic quad flat pack qualified to JESD47. Both parts operate over a -55°C to 125°C temperature range, and are radiation tolerant to a minimum of 100krad(Si) TID and a minimum of 100krad(Si) ELDRS, as well as single event effects.

Features

- Four half-bridge N-channel MOSFET drivers
- Four floating differential current sensors
- Pulse modulated resolver/LVDT transformer driver
- Three differential resolver/LVDT sense inputs
- Six threshold adjustable bi-level logic inputs for Hall effect sensor/encoder interfaces
- Fault detection
- Radiation tolerant: 100krad(Si) TID, 100krad(Si) ELDRS, Single Event Latch-up immune to 80MeV.cm²/mg

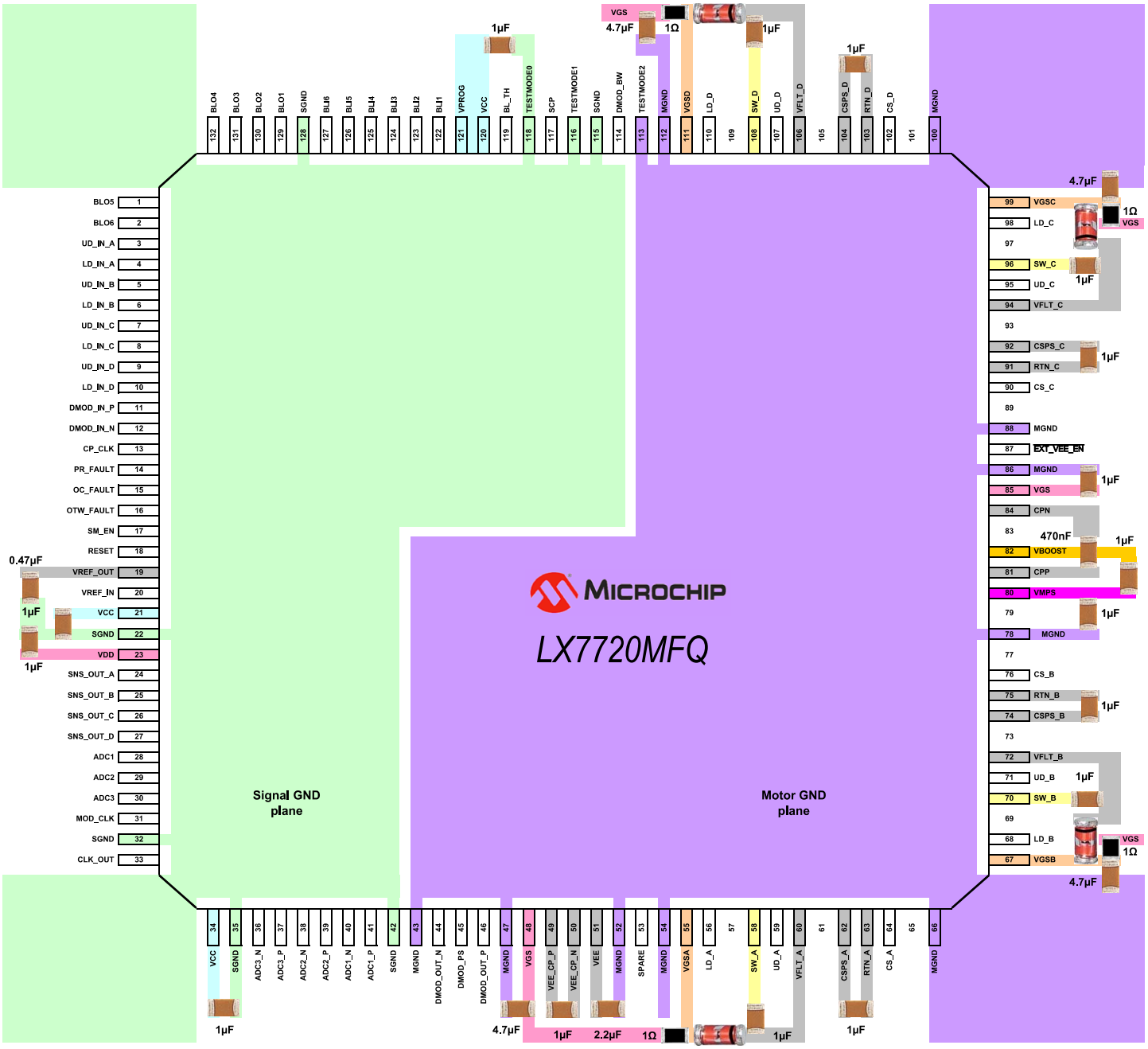
Applications

- Motor driver servo control
- Linear actuator servo control
- Stepper, BLDC, PMSM motor driver
- Robotics



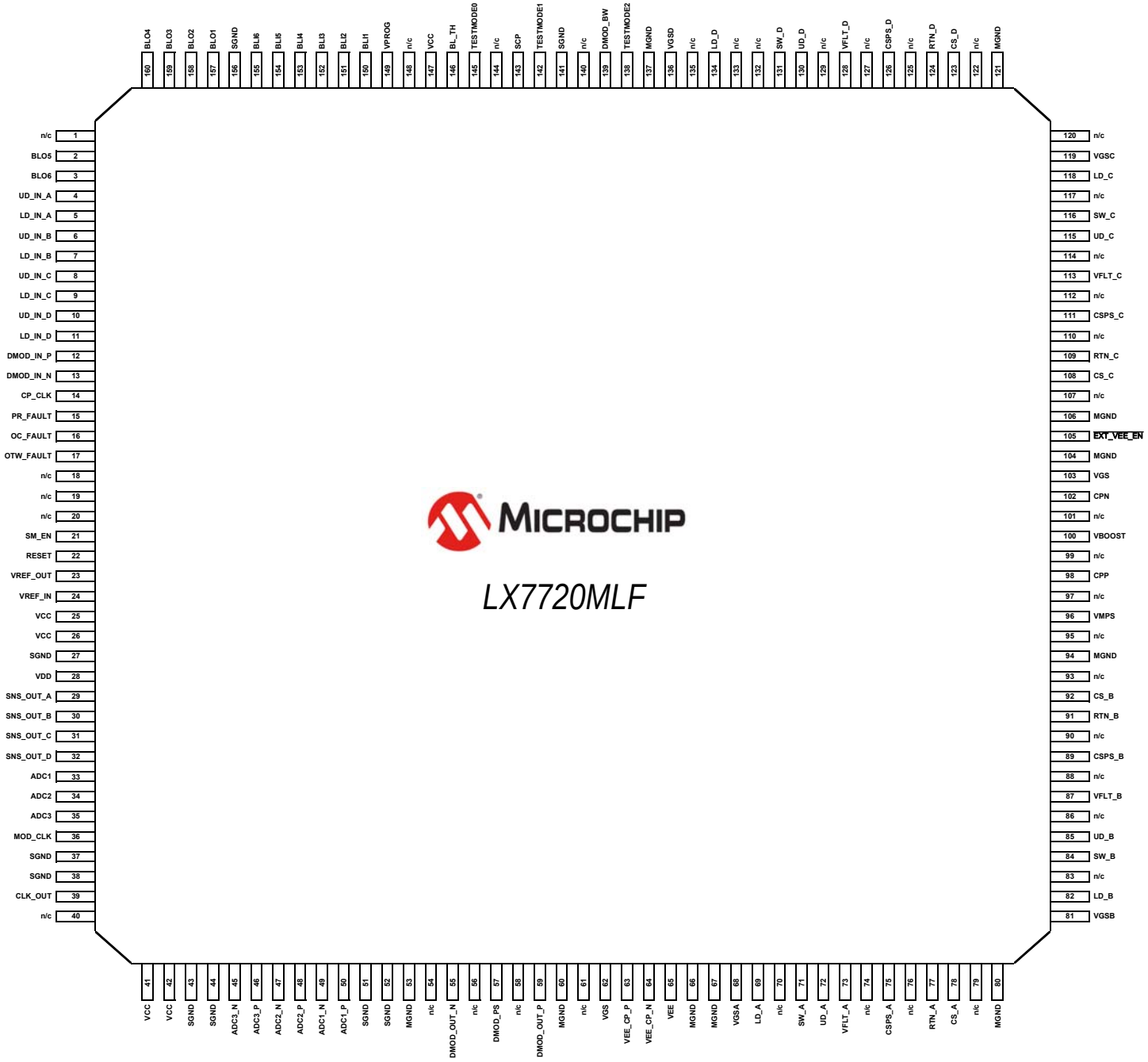
Typical Motor Drive System

1 CQFP-132 Pin Configuration and Pinout with Recommended Layout



Note 1. The layout example shows split planes for SGND and MGND. Separate SGND and MGND planes can be used
Note 2. Capacitors are shown as ▭. Resistors are shown as ■. Diodes are shown as ▭
Note 3. The pins marked n/c on the LQFP-160 pinout are not bonded internally
Note 4. Connect the LQFP-160 exposed pad to the SGND signal ground pins 27, 37, 38, 43, 44, 51, 52, 141 and 156

2 LQFP-160 Pin Configuration and Pinout



3 Ordering Information (subject to export compliance under EAR9A515.e)

Operating Temperature	Package Type	Package	Part Number	SMD Number	Flow	Shipping Type
-55°C to 125°C	Hermetic Ceramic	CQFP 132L	LX7720MFQ-V	5962-2120201VXC	MIL-PRF-38535 Class V	Tray
			LX7720MFQ-Q	5962-2120201QXC	MIL-PRF-38535 Class Q	
	Ceramic		LX7720-ES[1]	-	Engineering Sample	
			MECH-SAMPLE-CQFP132	-	Empty package sample	
	Plastic	LQFP 160L	LX7720MLF	-	Single temperature	
			MECH-SAMPLE-LQFP160	-	Empty package sample	

Note 1. Engineering samples are tested at room temperature only, and do not undergo thermal, environmental, or hermeticity testing
Note 2. All products use the same die and so all offer the same radiation hardness qualities described on page 1
Note 3. The product flows for all packaged parts including hermetic QML certified and non-hermetic packages are available here

4 CQFP-132 Pin Numbering and Pin Descriptions

Pin	Name	Pin Type	Pin Function	Description
1	BLO5	Logic Output	Bi-Level Output 5	Output of fixed threshold bi-level monitor (comparator) input BLI5 at pin 126
2	BLO6	Logic Output	Bi-Level Output 6	Output of fixed threshold bi-level monitor (comparator) input BLI6 at pin 127
3	UD_IN_A	Logic Input	High-side FET A	Active high enable for upper N-channel MOSFET of the phase A half bridge
4	LD_IN_A	Logic Input	Low-side FET A	Active high enable for lower N-channel MOSFET of the phase A half bridge
5	UD_IN_B	Logic Input	High-side FET B	Active high enable for upper N-channel MOSFET of the phase B half bridge
6	LD_IN_B	Logic Input	Low-side FET B	Active high enable for lower N-channel MOSFET of the phase B half bridge
7	UD_IN_C	Logic Input	High-side FET C	Active high enable for upper N-channel MOSFET of the phase C half bridge
8	LD_IN_C	Logic Input	Low-side FET C	Active high enable for lower N-channel MOSFET of the phase C half bridge
9	UD_IN_D	Logic Input	High-side FET D	Active high enable for upper N-channel MOSFET of the phase D half bridge
10	LD_IN_D	Logic Input	Low-side FET D	Active high enable for lower N-channel MOSFET of the phase D half bridge
11	DMOD_ IN_P	Logic Input	PWM Exciter Input	Resolver or LVDT transformer primary differential drive input signal working with DMOD_IN_N (pin 12). DMOD_IN_P is buffered and level shifted and output as DMOD_OUT_P (pin 46) with output swing between DMOD_PS (pin 45) and MGND
12	DMOD_ IN_N	Logic Input	PWM Exciter Input	Resolver or LVDT transformer primary differential drive input signal working with DMOD_IN_P (pin 11). DMOD_IN_N is buffered and level shifted and output as DMOD_OUT_N (pin 44) with output swing between DMOD_PS (pin 45) and MGND
13	CP_CLK	Logic Input	Charge Pump Clock	Connect a square wave clock (150kHz ±50kHz recommended) to operate the charge pumps for both the negative rail VEE and the floating high-side supply VBOOST for the half-bridge high-side MOSFET drivers
14	PR_ FAULT	Logic Output	Power Rail Fault	Active high when one or more of the power rails is below its under voltage threshold or either the VGS or DMOD_PS supply is overloaded
15	OC_ FAULT	Logic Output	Over Current Fault	Active high when an over-current fault condition is detected at one of the floating current sensor amplifiers
16	OTW_ FAULT	Logic Output	Over Temperature Warning	Active high when the die temperature is has exceeded the over temperature warning threshold
17	SM_EN	Logic Input (1MΩ to VDD)	Safe Mode Enable	To enable automatic protection countermeasures when faults are detected, either leave SM_EN open or tie SM_EN to VDD. To disable automatic protection countermeasures, tie SM_EN to SGND. Faults are reported regardless of the SM_EN setting
18	RESET	Logic Input (1MΩ to SGND)	Fault Reset	Active high input when SM_EN = 1 resets Safe Mode latched fault conditions
19	VREF_ OUT	Analog Output	Internal VREF Output	Internal +2.5V ±0.8% reference voltage output. Connect a 0.47µF or greater capacitor from VREF to SGND pin 22
20	VREF_IN	Analog Input	External VREF Input	Reference voltage for the ADC sigma delta modulators. To use the internal +2.5V ±0.8% reference voltage, connect VREF_IN to VREF_OUT pin 19. Alternatively, connect to an external 2.5V ±0.2V reference voltage
21	VCC	Power	Signal Supply	Connect to the signal power supply (4.75V to 5.25V). All VCC pins 21, 34, and 120 must be used. Bypass close to the pin with a 1µF capacitor to SGND
22	SGND	Power	Signal Ground	All SGND pins 22, 32, 35, 42, 115, and 128 must be used, connected together via a plane or split-plane on the PCB, for the signal ground. SGND may vary from -10V to +8V with respect to MGND
23	VDD	Power	I/O Supply	Connect to the external logic controller's (FPGA, MCU) I/O power supply (2.1V to 5.5V) to set the I/O logic level for all logic I/Os. Bypass close to the pin with a 1µF capacitor to SGND
24	SNS_ OUT_A	Logic Output	Phase A Current Sense Data	Pulse train output of 2nd order Σ-Δ modulator where the output pulse train represents the magnitude and polarity of the differential voltage potential between CS_A pin 64 and RTN_A pin 63
25	SNS_ OUT_B	Logic Output	Phase B Current Sense Data	Pulse train output of 2nd order Σ-Δ modulator where the output pulse train represents the magnitude and polarity of the differential voltage potential between CS_B pin 76 and RTN_B pin 75
26	SNS_ OUT_C	Logic Output	Phase C Current Sense Data	Pulse train output of 2nd order Σ-Δ modulator where the output pulse train represents the magnitude and polarity of the differential voltage potential between CS_C pin 90 and RTN_C pin 91

Pin	Name	Pin Type	Pin Function	Description
27	SNS_ OUT_D	Logic Output	Phase D Current Sense Data	Pulse train output of 2nd order Σ-Δ modulator where the output pulse train represents the magnitude and polarity of the differential voltage potential between CS_D pin 102 and RTN_D pin 103
28	ADC1	Logic Output	ADC 1 Data	Pulse train output of 2nd order Σ-Δ modulator where the output pulse train represents the magnitude and polarity of the differential voltage potential between ADC1_P pin 41 and ADC1_N pin 40
29	ADC2	Logic Output	ADC 2 Data	Pulse train output of 2nd order Σ-Δ modulator where the output pulse train represents the magnitude and polarity of the differential voltage potential between ADC2_P pin 39 and ADC2_N pin 38
30	ADC3	Logic Output	ADC 3 Data	Pulse train output of 2nd order Σ-Δ modulator where the output pulse train represents the magnitude and polarity of the differential voltage potential between ADC3_P pin 37 and ADC3_N pin 36
31	MOD_CLK	Logic Input	Σ-Δ Mod Clock	Connect a 24MHz to 32MHz sample rate clock for the Σ-Δ modulators
32	SGND	Power	Signal Ground	All SGND pins 22, 32, 35, 42, 115, and 128 must be used, connected together via a plane or split-plane on the PCB, for the signal ground. SGND may vary from -10V to +8V with respect to MGND
33	CLK_OUT	Logic Output	Σ-Δ Output Clock	Output clock for the SNS_OUT_A, SNS_OUT_B, SNS_OUT_C, SNS_OUT_D, ADC1, ADC2, ADC3 Σ-Δ modulators, rising edge active
34	VCC	Power	Signal Supply	Connect to the signal power supply (4.75V to 5.25V). All VCC pins 21, 34, and 120 must be used. Bypass close to the pin with a 1µF capacitor to SGND
35	SGND	Power	Signal Ground	All SGND pins 22, 32, 35, 42, 115, and 128 must be used, connected together via a plane or split-plane on the PCB, for the signal ground. SGND may vary from -10V to +8V with respect to MGND
36	ADC3_N	Analog Input	ADC3 differential input	ADC3_P and ADC3_N form a differential analog signal feeding into the ADC3 sigma delta modulator
37	ADC3_P	Analog Input		
38	ADC2_N	Analog Input	ADC2 differential input	ADC2_P and ADC2_N form a differential analog signal feeding into the ADC2 sigma delta modulator
39	ADC2_P	Analog Input		
40	ADC1_N	Analog Input	ADC1 differential input	ADC1_P and ADC1_N form a differential analog signal feeding into the ADC1 sigma delta modulator
41	ADC1_P	Analog Input		
42	SGND	Power	Signal Ground	All SGND pins 22, 32, 35, 42, 115, and 128 must be used, connected together via a plane or split-plane on the PCB, for the signal ground. SGND may vary from -10V to +8V with respect to MGND
43	MGND	Ground	Motor Ground	All MGND pins 43, 47, 52, 54, 66, 78, 86, 88, 100, and 112 must be used, connected together via a plane or split-plane on the PCB, for the return rail to the lower MOSFET drivers. MGND connects to the return rail of the motor and resolver/LVDT power supplies. MGND may vary from -10V to +8V with respect to SGND
44	DMOD_ OUT_N	Analog Output	PWM Exciter Output	Resolver or LVDT transformer primary differential drive output working with DMOD_OUT_P (pin 46). Input is PWM signal at DMOD_IN_N (pin 12). Output swing is between DMOD_PS (pin 45) and MGND
45	DMOD_PS	Power	PWM Exciter Supply	Connect to the demodulator driver power supply (10V to 18V), typically VGS. Bypass close to the pin with a 10µF capacitor to MGND DMOD_PS provides power to the DMOD_OUT_P (pin 46) and DMOD_OUT_N (pin 44) differential drivers. Tie DMOD_PS to MGND if not used
46	DMOD_ OUT_P	Analog Output	PWM Exciter Output	LVDT transformer primary differential drive output working with DMOD_OUT_N (pin 44). Input is PWM signal at DMOD_IN_P (pin 11). Output swing is between DMOD_PS (pin 45) and MGND
47	MGND	Ground	Motor Ground	All MGND pins 43, 47, 52, 54, 66, 78, 86, 88, 100, and 112 must be used, connected together via a plane or split-plane on the PCB, for the return rail to the lower MOSFET drivers. MGND connects to the return rail of the motor and resolver/LVDT power supplies. MGND may vary from -10V to +8V with respect to SGND
48	VGS	Power	VEE Charge Pump Supply Rail	Connect to the VGS MOSFET gate driver power supply (10V to 18V). This VGS pin powers to the VEE inverting charge pump, pins 49-51. Bypass close to the pin with a 10µF capacitor (shared with pin 55 via 1Ω) to MGND
49	VEE_ CP_P	Output	Charge Pump Flying Capacitor inverting	Flying capacitor positive node for the internal VEE inverting charge pump. Connect a 1µF capacitor between this pin and VEE_CP_N pin 50. VEE_CP_P swings between MGND and VGS. See section 14.2 on page 24
50	VEE_ CP_N	Output	Charge Pump Flying Capacitor inverting	Flying capacitor negative node for the internal VEE inverting charge pump. Connect a 1µF capacitor between this pin and VEE_CP_P pin 49. VEE_CP_N swings between MGND and VEE. See section 14.2 on page 24

Pin	Name	Pin Type	Pin Function	Description
51	VEE	Power	Negative power rail	To use the internal VEE charge pump, tie $\overline{\text{EXT\_VEE\_EN}}$ pin 87 to VGS. Alternatively, connect an external negative supply in the range -VGS to -8V to VEE and tie $\overline{\text{EXT\_VEE\_EN}}$ pin 87 to MGND to disable the VEE charge pump. Connect a 2.2µF capacitor between this pin and MGND at pin 52
52	MGND	Ground	Motor Ground	All MGND pins 43, 47, 52, 54, 66, 78, 86, 88, 100, and 112 must be used, connected together via a plane or split-plane on the PCB, for the return rail to the lower MOSFET drivers. MGND connects to the return rail of the motor and resolver/LVDT power supplies. MGND may vary from -10V to +8V with respect to SGND
53	SPARE	-	Unused pin	Leave open or connect to MGND
54	MGND	Ground	Motor Ground	All MGND pins 43, 47, 52, 54, 66, 78, 86, 88, 100, and 112 must be used, connected together via a plane or split-plane on the PCB, for the return rail to the lower MOSFET drivers. MGND connects to the return rail of the motor and resolver/LVDT power supplies. MGND may vary from -10V to +8V with respect to SGND
55	VGS_A	Power	FET Gate Drive Rail	Connect to the MOSFET gate driver power supply VGS (10V to 18V) at pin 48 via a 1Ω series resistor between this pin and the 10µF capacitor at pin 48
56	LD_A	FET Driver	Low-side FET Driver	Phase A lower N-channel MOSFET gate driver. Connect through a resistor such as 20Ω to the MOSFET's gate. MGND provides the return current path
57	-	-	-	Pin is not fitted to the package
58	SW_A	FET Switch	MOSFET Source	Phase A upper N-channel MOSFET gate driver source connection
59	UD_A	FET Driver	High-side FET Driver	Phase A upper N-channel MOSFET gate driver. Connect through a resistor such as 20Ω to the MOSFET's gate. MGND provides the return current path
60	VFLT_A	Power	High-side FET Gate Drive Rail	Floating gate drive power rail for upper N-channel MOSFET gate driver A. Bypass close to the pin with a 1µF capacitor to SW_A. Connect a silicon or Schottky diode such as 1N5809US, 1N5811US or 1N6864US between VFLT_A and VGS_A pin 55
61	-	-	-	Pin is not fitted to the package
62	CSPS_A	Power	Phase A Current Sense Supply	Power to phase A floating current sense. Connect to either VFLT_A pin 60 for SW_A sensing or to VGS for low-side sensing. Connect a 1µF capacitor between this pin and RTN_A pin 63
63	RTN_A	Signal/Power	Phase A Current Sense Return	Ground reference for phase A floating current sense and current measurement power rail
64	CS_A	Analog Input	Phase A current sense	Current measurement input for phase A floating current sensing, with a ±250mV linear range across the phase A sense resistor
65	-	-	-	Pin is not fitted to the package
66	MGND	Ground	Motor Ground	All MGND pins 43, 47, 52, 54, 66, 78, 86, 88, 100, and 112 must be used, connected together via a plane or split-plane on the PCB, for the return rail to the lower MOSFET drivers. MGND connects to the return rail of the motor and resolver/LVDT power supplies. MGND may vary from -10V to +8V with respect to SGND
67	VGS_B	Power	FET Gate Drive Rail	Connect to the MOSFET gate driver power supply VGS (10V to 18V) via a 1Ω series resistor close to the pin. Bypass VGS (not pin 67) at the series resistor with a 10µF capacitor to MGND
68	LD_B	FET Driver	Low-side FET Driver	Phase B lower N-channel MOSFET gate driver. Connect through a resistor such as 20Ω to the MOSFET's gate. MGND provides the return current path
69	-	-	-	Pin is not fitted to the package
70	SW_B	FET Switch	MOSFET Source	Phase B upper N-channel MOSFET gate driver source connection
71	UD_B	FET Driver	High-side FET Driver	Phase B upper N-channel MOSFET gate driver. Connect through a resistor such as 20Ω to the MOSFET's gate. MGND provides the return current path
72	VFLT_B	Power	High-side FET Gate Drive Rail	Floating gate drive power rail for upper N-channel MOSFET gate driver B. Bypass close to the pin with a 1µF capacitor to SW_B. Connect a silicon or Schottky diode such as 1N5809US, 1N5811US or 1N6864US between VFLT_B and VGS_B pin 67
73	-	-	-	Pin is not fitted to the package
74	CSPS_B	Power	Phase B Current Sense Supply	Power to phase B floating current sense. Connect to either VFLT_B pin 72 for SW_B sensing or to VGS for low-side sensing. Connect a 1µF capacitor between this pin and RTN_B pin 75
75	RTN_B	Signal/Power	Phase B Current Sense Return	Ground reference for phase B floating current sense and current measurement power rail

Pin	Name	Pin Type	Pin Function	Description
76	CS_B	Analog Input	Phase B current sense	Current measurement input for phase B floating current sensing, with a ±250mV linear range across the phase B sense resistor
77	-	-	-	Pin is not fitted to the package
78	MGND	Ground	Motor Ground	All MGND pins 43, 47, 52, 54, 66, 78, 86, 88, 100, and 112 must be used, connected together via a plane or split-plane on the PCB, for the return rail to the lower MOSFET drivers. MGND connects to the return rail of the motor and resolver/LVDT power supplies. MGND may vary from -10V to +8V with respect to SGND
79	-	-	-	Pin is not fitted to the package
80	VMPS	Power	Motor Power supply	Motor power rail, used for the upper MOSFET drivers charge pump, VBOOST pin 82. Connect a 1µF capacitor between this pin and MGND
81	CPP	Output	Charge Pump Flying Capacitor inverting	Flying capacitor negative node for the internal VBOOST charge pump. Connect a 0.47µF capacitor between this pin and CPN pin 84. CPP swings between VMPS and (VMPS + VGS)
82	VBOOST	Power	Upper MOSFET Driver Charge Pump	Charge pump output which is VGS volts above VMPS, unloaded. Connect a 1µF capacitor between this pin and VMPS pin 80
83	-	-	-	Pin is not fitted to the package
84	CPN	Output	Charge Pump Flying Capacitor inverting	Flying capacitor negative node for the internal VBOOST charge pump. Connect a 0.47µF capacitor between this pin and CPP pin 81. CPN swings between MGND and VGS
85	VGS	Power	VBOOST Charge Pump Supply Rail	Connect to the VGS MOSFET gate driver power supply (10V to 18V). This VGS pin powers to the VBOOST charge pump, pins 81-84. Bypass close to the pin with a 1µF capacitor to MGND
86	MGND	Ground	Motor Ground	All MGND pins 43, 47, 52, 54, 66, 78, 86, 88, 100, and 112 must be used, connected together via a plane or split-plane on the PCB, for the return rail to the lower MOSFET drivers. MGND connects to the return rail of the motor and resolver/LVDT power supplies. MGND may vary from -10V to +8V with respect to SGND
87	$\overline{\text{EXT\_VEE\_EN}}$	Control Input (1MΩ to VGS)	External VEE Enable	Active high (leave open or tie to VGS) to enable the VEE charge pump. Connect to MGND to disable the VEE charge pump, and connect a negative supply in the range -VGS to -8V to VEE pin 51
88	MGND	Ground	Motor Ground	All MGND pins 43, 47, 52, 54, 66, 78, 86, 88, 100, and 112 must be used, connected together via a plane or split-plane on the PCB, for the return rail to the lower MOSFET drivers. MGND connects to the return rail of the motor and resolver/LVDT power supplies. MGND may vary from -10V to +8V with respect to SGND
89	-	-	-	Pin is not fitted to the package
90	CS_C	Analog Input	Phase C current sense	Current measurement input for phase C floating current sensing, with a ±250mV linear range across the phase C sense resistor
91	RTN_C	Signal/Power	Phase C Current Sense Return	Ground reference for phase C floating current sense and current measurement power rail
92	CSPS_C	Power	Phase C Current Sense Supply	Power to phase C floating current sense. Connect to either VFLT_C pin 94 for SW_C sensing or to VGS for low-side sensing. Connect a 1µF capacitor between this pin and RTN_C pin 91
93	-	-	-	Pin is not fitted to the package
94	VFLT_C	Power	High-side FET Gate Drive Rail	Floating gate drive power rail for upper N-channel MOSFET gate driver C. Bypass close to the pin with a 1µF capacitor to SW_C. Connect a silicon or Schottky diode such as 1N5809US, 1N5811US or 1N6864US between VFLT_C and VGS_C pin 99
95	UD_C	FET Driver	High-side FET Driver	Phase C upper N-channel MOSFET gate driver. Connect through a resistor such as 20Ω to the MOSFET's gate. MGND provides the return current path
96	SW_C	FET Switch	MOSFET Source	Phase C upper N-channel MOSFET gate driver source connection
97	-	-	-	Pin is not fitted to the package
98	LD_C	FET Driver	Low-side FET Driver	Phase C lower N-channel MOSFET gate driver. Connect through a resistor such as 20Ω to the MOSFET's gate. MGND provides the return current path
99	VGS_C	Power	FET Gate Drive Rail	Connect to the MOSFET gate driver power supply VGS (10V to 18V) via a 1Ω series resistor close to the pin. Bypass VGS (not pin 99) at the series resistor with a 10µF capacitor to MGND

Pin	Name	Pin Type	Pin Function	Description
100	MGND	Ground	Motor Ground	All MGND pins 43, 47, 52, 54, 66, 78, 86, 88, 100, and 112 must be used, connected together via a plane or split-plane on the PCB, for the return rail to the lower MOSFET drivers. MGND connects to the return rail of the motor and resolver/LVDT power supplies. MGND may vary from -10V to +8V with respect to SGND
101	-	-	-	Pin is not fitted to the package
102	CS_D	Analog Input	Phase D current sense	Current measurement input for phase D floating current sensing, with a ±250mV linear range across the phase D sense resistor
103	RTN_D	Signal/Power	Phase D Current Sense Return	Ground reference for phase D floating current sense and current measurement power rail
104	CSPS_D	Power	Phase D Current Sense Supply	Power to phase D floating current sense. Connect to either VFLT_D pin 106 for SW_D sensing or to VGS for low-side sensing. Connect a 1µF capacitor between this pin and RTN_D pin 103
105	-	-	-	Pin is not fitted to the package
106	VFLT_D	Power	High-side FET Gate Drive Rail	Floating gate drive power rail for upper N-channel MOSFET gate driver D. Bypass close to the pin with a 1µF capacitor to SW_D. Connect a silicon or Schottky diode such as 1N5809US, 1N5811US or 1N6864US between VFLT_D and VGS_D pin 111
107	UD_D	FET Driver	High-side FET Driver	Phase D upper N-channel MOSFET gate driver. Connect through a resistor such as 20Ω to the MOSFET's gate. MGND provides the return current path
108	SW_D	FET Switch	MOSFET Source	Phase D upper N-channel MOSFET gate driver source connection
109	-	-	-	Pin is not fitted to the package
110	LD_D	FET Driver	Low-side FET Driver	Phase D lower N-channel MOSFET gate driver. Connect through a resistor such as 20Ω to the MOSFET's gate. MGND provides the return current path
111	VGS_D	Power	FET Gate Drive Rail	Connect to the MOSFET gate driver power supply VGS (10V to 18V) via a 1Ω series resistor close to the pin. Bypass VGS (not pin 111) at the series resistor with a 10µF capacitor to MGND
112	MGND	Ground	Motor Ground	All MGND pins 43, 47, 52, 54, 66, 78, 86, 88, 100, and 112 must be used, connected together via a plane or split-plane on the PCB, for the return rail to the lower MOSFET drivers. MGND connects to the return rail of the motor and resolver/LVDT power supplies. MGND may vary from -10V to +8V with respect to SGND
113	TEST MODE2	Factory Use	Test	Internally bonded test node. Tie this pin to MGND
114	DMOD_ BW	Logic Input (1MΩ to SGND)	DMOD Driver Bandwidth	To select a shorter exciter propagation delay (recommended for 100krad TID lifetime), tie DMOD_BW to VDD. To select an increased exciter propagation delay and lower current consumption, either leave DMOD_BW open or tie DMOD_BW to SGND
115	SGND	Power	Signal Ground	All SGND pins 22, 32, 35, 42, 115, and 128 must be used, connected together via a plane or split-plane on the PCB, for the signal ground. SGND may vary from -10V to +8V with respect to MGND
116	TEST MODE1	Factory Use	Test	Internally bonded test node. Tie this pin to SGND
117	SCP	Logic Input (1MΩ to VDD)	Simultaneous Conduction Protection	To prevent both UD# and LD# for any switch pair from being held on simultaneously, either leave SCP open or tie SCP to VDD. To allow UD# and LD# to operate independently, tie SCP to SGND
118	TEST MODE0	Factory Use	Test	Internally bonded test node. Tie this pin to SGND
119	BL_TH	Analog Input	Bi-Level (-) threshold input	Negative (-) threshold voltage between 0.5V and 4.5V for the fixed threshold bi-level monitors (comparators) BL1 to BLI6
120	VCC	Power	Signal Supply	Connect to the signal power supply (4.75V to 5.25V). All VCC pins 21, 34, and 120 must be used. Bypass close to the pin with a 1µF capacitor to SGND
121	VPROG	Factory Use	Test	Internally bonded test node. Tie this pin to VCC
122	BLI1	Analog Input	Bi-Level (+) input 1	Fixed threshold bi-level monitor (comparator) positive (+) input 1 which is compared against an external voltage between 0.5V and 4.5V on the BL_TH pin 119. The output is BLO1 pin 129
123	BLI2	Analog Input	Bi-Level (+) input 2	Fixed threshold bi-level monitor (comparator) positive (+) input 2 which is compared against an external voltage between 0.5V and 4.5V on the BL_TH pin 119. The output is BLO2 pin 130

Pin	Name	Pin Type	Pin Function	Description
124	BLI3	Analog Input	Bi-Level (+) input 3	Fixed threshold bi-level monitor (comparator) positive (+) input 3 which is compared against an external voltage between 0.5V and 4.5V on the BL_TH pin 119. The output is BLO3 pin 131
125	BLI4	Analog Input	Bi-Level (+) input 4	Fixed threshold bi-level monitor (comparator) positive (+) input 4 which is compared against an external voltage between 0.5V and 4.5V on the BL_TH pin 119. The output is BLO4 pin 132
126	BLI5	Analog Input	Bi-Level (+) input 5	Fixed threshold bi-level monitor (comparator) positive (+) input 5 which is compared against an external voltage between 0.5V and 4.5V on the BL_TH pin 119. The output is BLO5 pin 1
127	BLI6	Analog Input	Bi-Level (+) input 6	Fixed threshold bi-level monitor (comparator) positive (+) input 6 which is compared against an external voltage between 0.5V and 4.5V on the BL_TH pin 119. The output is BLO6 pin 2
128	SGND	Power	Signal Ground	All SGND pins 22, 32, 35, 42, 115, and 128 must be used, connected together via a plane or split-plane on the PCB, for the signal ground. SGND may vary from -10V to +8V with respect to MGND
129	BLO1	Logic Output	Bi-Level Output 1	Output of fixed threshold bi-level monitor (comparator) input BLI1 at pin 122
130	BLO2	Logic Output	Bi-Level Output 2	Output of fixed threshold bi-level monitor (comparator) input BLI2 at pin 123
131	BLO3	Logic Output	Bi-Level Output 3	Output of fixed threshold bi-level monitor (comparator) input BLI3 at pin 124
132	BLO4	Logic Output	Bi-Level Output 4	Output of fixed threshold bi-level monitor (comparator) input BLI4 at pin 125

5 LQFP-160 Pin Numbering and Pin Descriptions

Pin	Name	Pin Type	Pin Function	Description
1	n/c	-	-	Pin is not bonded
2	BLO5	Logic Output	Bi-Level Output 5	Output of fixed threshold bi-level monitor (comparator) input BLI5 at pin 154
3	BLO6	Logic Output	Bi-Level Output 6	Output of fixed threshold bi-level monitor (comparator) input BLI6 at pin 155
4	UD_IN_A	Logic Input	High-side FET A	Active high enable for upper N-channel MOSFET of the phase A half bridge
5	LD_IN_A	Logic Input	Low-side FET A	Active high enable for lower N-channel MOSFET of the phase A half bridge
6	UD_IN_B	Logic Input	High-side FET B	Active high enable for upper N-channel MOSFET of the phase B half bridge
7	LD_IN_B	Logic Input	Low-side FET B	Active high enable for lower N-channel MOSFET of the phase B half bridge
8	UD_IN_C	Logic Input	High-side FET C	Active high enable for upper N-channel MOSFET of the phase C half bridge
9	LD_IN_C	Logic Input	Low-side FET C	Active high enable for lower N-channel MOSFET of the phase C half bridge
10	UD_IN_D	Logic Input	High-side FET D	Active high enable for upper N-channel MOSFET of the phase D half bridge
11	LD_IN_D	Logic Input	Low-side FET D	Active high enable for lower N-channel MOSFET of the phase D half bridge
12	DMOD_IN_P	Logic Input	PWM Exciter Input	Resolver or LVDT transformer primary differential drive input signal working with DMOD_IN_N (pin 13). DMOD_IN_P is buffered and level shifted and output as DMOD_OUT_P (pin 59) with output swing between DMOD_PS (pin 57) and MGND
13	DMOD_IN_N	Logic Input	PWM Exciter Input	Resolver or LVDT transformer primary differential drive input signal working with DMOD_IN_P (pin 12). DMOD_IN_N is buffered and level shifted and output as DMOD_OUT_N (pin 55) with output swing between DMOD_PS (pin 57) and MGND
14	CP_CLK	Logic Input	Charge Pump Clock	Connect a square wave clock (150kHz ±50kHz recommended) to operate the charge pumps for both the negative rail VEE and the floating high-side supply VBOOST for the half-bridge high-side MOSFET drivers
15	PR_FAULT	Logic Output	Power Rail Fault	Active high when one or more of the power rails is below its under voltage threshold or either the VGS or DMOD_PS supply is overloaded
16	OC_FAULT	Logic Output	Over Current Fault	Active high when an over-current fault condition is detected at one of the floating current sensor amplifiers
17	OTW_FAULT	Logic Output	Over Temperature Warning	Active high when the die temperature is has exceeded the over temperature warning threshold
18-20	n/c	-	-	Pins are not bonded
21	SM_EN	Logic Input (1MΩ to VDD)	Safe Mode Enable	To enable automatic protection countermeasures when faults are detected, either leave SM_EN open or tie SM_EN to VDD. To disable automatic protection countermeasures, tie SM_EN to SGND. Faults are reported regardless of the SM_EN setting
22	RESET	Logic Input (1MΩ to SGND)	Fault Reset	Active high input when SM_EN = 1 resets Safe Mode latched fault conditions
23	VREF_OUT	Analog Output	Internal VREF Output	Internal +2.5V ±0.8% reference voltage output. Connect a 0.47µF or greater capacitor from VREF to SGND pin 27
24	VREF_IN	Analog Input	External VREF Input	Reference voltage for the ADC sigma delta modulators. To use the internal +2.5V ±0.8% reference voltage, connect VREF_IN to VREF_OUT pin 23. Alternatively, connect to an external 2.5V ±0.2V reference voltage
25-26	VCC	Power	Signal Supply	Connect to the signal power supply (4.75V to 5.25V). All VCC pins 25, 26, 41, 42, and 147 must be used. Bypass close to the pin-pair with a 1µF capacitor to SGND
27	SGND	Power	Signal Ground	All SGND pins 27, 37, 38, 43, 44, 51, 52, 141 and 156 must be used, connected together and to the exposed pad for the signal ground. SGND may vary from -10V to +8V with respect to MGND
28	VDD	Power	I/O Supply	Connect to the external logic controller's (FPGA, MCU) I/O power supply (2.1V to 5.5V) to set the I/O logic level for all logic I/Os. Bypass close to the pin with a 1µF capacitor to SGND
29	SNS_OUT_A	Logic Output	Phase A Current Sense Data	Pulse train output of 2nd order Σ-Δ modulator where the output pulse train represents the magnitude and polarity of the differential voltage potential between CS_A pin 78 and RTN_A pin 77

Pin	Name	Pin Type	Pin Function	Description
30	SNS_ OUT_B	Logic Output	Phase B Current Sense Data	Pulse train output of 2nd order Σ-Δ modulator where the output pulse train represents the magnitude and polarity of the differential voltage potential between CS_B pin 92 and RTN_B pin 91
31	SNS_ OUT_C	Logic Output	Phase C Current Sense Data	Pulse train output of 2nd order Σ-Δ modulator where the output pulse train represents the magnitude and polarity of the differential voltage potential between CS_C pin 108 and RTN_C pin 109
32	SNS_ OUT_D	Logic Output	Phase D Current Sense Data	Pulse train output of 2nd order Σ-Δ modulator where the output pulse train represents the magnitude and polarity of the differential voltage potential between CS_D pin 123 and RTN_D pin 124
33	ADC1	Logic Output	ADC 1 Data	Pulse train output of 2nd order Σ-Δ modulator where the output pulse train represents the magnitude and polarity of the differential voltage potential between ADC1_P pin 50 and ADC1_N pin 49
34	ADC2	Logic Output	ADC 2 Data	Pulse train output of 2nd order Σ-Δ modulator where the output pulse train represents the magnitude and polarity of the differential voltage potential between ADC2_P pin 48 and ADC2_N pin 47
35	ADC3	Logic Output	ADC 3 Data	Pulse train output of 2nd order Σ-Δ modulator where the output pulse train represents the magnitude and polarity of the differential voltage potential between ADC3_P pin 46 and ADC3_N pin 45
36	MOD_CLK	Logic Input	Σ-Δ Mod Clock	Connect a 24MHz to 32MHz sample rate clock for the Σ-Δ modulators
37-38	SGND	Power	Signal Ground	All SGND pins 27, 37, 38, 43, 44, 51, 52, 141 and 156 must be used, connected together and to the exposed pad for the signal ground. SGND may vary from -10V to +8V with respect to MGND
39	CLK_OUT	Logic Output	Σ-Δ Output Clock	Output clock for the SNS_OUT_A, SNS_OUT_B, SNS_OUT_C, SNS_OUT_D, ADC1, ADC2, ADC3 Σ-Δ modulators, rising edge active
40	n/c	-	-	Pin is not bonded
41-42	VCC	Power	Signal Supply	Connect to the signal power supply (4.75V to 5.25V). All VCC pins 25, 26, 41, 42, and 147 must be used. Bypass close to the pin-pair with a 1µF capacitor to SGND
43-44	SGND	Power	Signal Ground	All SGND pins 27, 37, 38, 43, 44, 51, 52, 141 and 156 must be used, connected together and to the exposed pad for the signal ground. SGND may vary from -10V to +8V with respect to MGND
45	ADC3_N	Analog Input	ADC3 differential input	ADC3_P and ADC3_N form a differential analog signal feeding into the ADC3 sigma delta modulator
46	ADC3_P	Analog Input		
47	ADC2_N	Analog Input	ADC2 differential input	ADC2_P and ADC2_N form a differential analog signal feeding into the ADC2 sigma delta modulator
48	ADC2_P	Analog Input		
49	ADC1_N	Analog Input	ADC1 differential input	ADC1_P and ADC1_N form a differential analog signal feeding into the ADC1 sigma delta modulator
50	ADC1_P	Analog Input		
51-52	SGND	Power	Signal Ground	All SGND pins 27, 37, 38, 43, 44, 51, 52, 141 and 156 must be used, connected together and to the exposed pad for the signal ground. SGND may vary from -10V to +8V with respect to MGND
53	MGND	Ground	Motor Ground	All MGND pins 53, 60, 66, 67, 80, 94, 104, 106, 121, and 137 must be used, connected together via a plane or split-plane on the PCB, for the return rail to the lower MOSFET drivers. MGND connects to the return rail of the motor and resolver/LVDT power supplies. MGND may vary from -10V to +8V with respect to SGND
54	n/c	-	-	Pin is not bonded
55	DMOD_ OUT_N	Analog Output	PWM Exciter Output	Resolver or LVDT transformer primary differential drive output working with DMOD_OUT_P (pin 59). Input is PWM signal at DMOD_IN_N (pin 13). Output swing is between DMOD_PS (pin 57) and MGND
56	n/c	-	-	Pin is not bonded
57	DMOD_PS	Power	PWM Exciter Supply	Connect to the demodulator driver power supply (10V to 18V), typically VGS. Bypass close to the pin with a 10µF capacitor to MGND DMOD_PS provides power to the DMOD_OUT_P (pin 59) and DMOD_OUT_N (pin 55) differential drivers. Tie DMOD_PS to MGND if not used
58	n/c	-	-	Pin is not bonded
59	DMOD_ OUT_P	Analog Output	PWM Exciter Output	LVDT transformer primary differential drive output working with DMOD_OUT_N (pin 55). Input is PWM signal at DMOD_IN_P (pin 12). Output swing is between DMOD_PS (pin 57) and MGND

Pin	Name	Pin Type	Pin Function	Description
60	MGND	Ground	Motor Ground	All MGND pins 53, 60, 66, 67, 80, 94, 104, 106, 121, and 137 must be used, connected together via a plane or split-plane on the PCB, for the return rail to the lower MOSFET drivers. MGND connects to the return rail of the motor and resolver/LVDT power supplies. MGND may vary from -10V to +8V with respect to SGND
61	n/c	-	-	Pin is not bonded
62	VGS	Power	VEE Charge Pump Supply Rail	Connect to the VGS MOSFET gate driver power supply (10V to 18V). This VGS pin powers to the VEE inverting charge pump, pins 63-65. Bypass close to the pin with a 10µF capacitor (shared with pin 68 via 1Ω) to MGND
63	VEE_ CP_P	Output	Charge Pump Flying Capacitor inverting	Flying capacitor positive node for the internal VEE inverting charge pump. Connect a 1µF capacitor between this pin and VEE_CP_N pin 64. VEE_CP_P swings between MGND and VGS. See section 14.2 on page 24
64	VEE_ CP_N	Output	Charge Pump Flying Capacitor inverting	Flying capacitor negative node for the internal VEE inverting charge pump. Connect a 1µF capacitor between this pin and VEE_CP_P pin 63. VEE_CP_N swings between MGND and VEE. See section 14.2 on page 24
65	VEE	Power	Negative power rail	To use the internal VEE charge pump, tie $\overline{\text{EXT\_VEE\_EN}}$ pin 105 to VGS. Alternatively, connect an external negative supply in the range -VGS to -8V to VEE and tie $\overline{\text{EXT\_VEE\_EN}}$ pin 105 to MGND to disable the VEE charge pump. Connect a 2.2µF capacitor between this pin and MGND at pins 66-67
66-67	MGND	Ground	Motor Ground	All MGND pins 53, 60, 66, 67, 80, 94, 104, 106, 121, and 137 must be used, connected together via a plane or split-plane on the PCB, for the return rail to the lower MOSFET drivers. MGND connects to the return rail of the motor and resolver/LVDT power supplies. MGND may vary from -10V to +8V with respect to SGND
68	VGS_A	Power	FET Gate Drive Rail	Connect to the MOSFET gate driver power supply VGS (10V to 18V) at pin 62 via a 1Ω series resistor between this pin and the 10µF capacitor at pin 62
69	LD_A	FET Driver	Low-side FET Driver	Phase A lower N-channel MOSFET gate driver. Connect through a resistor such as 20Ω to the MOSFET's gate. MGND provides the return current path
70	n/c	-	-	Pin is not bonded
71	SW_A	FET Switch	MOSFET Source	Phase A upper N-channel MOSFET gate driver source connection
72	UD_A	FET Driver	High-side FET Driver	Phase A upper N-channel MOSFET gate driver. Connect through a resistor such as 20Ω to the MOSFET's gate. MGND provides the return current path
73	VFLT_A	Power	High-side FET Gate Drive Rail	Floating gate drive power rail for upper N-channel MOSFET gate driver A. Bypass close to the pin with a 1µF capacitor to SW_A. Connect a silicon or Schottky diode such as 1N5809US, 1N5811US or 1N6864US between VFLT_A and VGS_A pin 68
74	n/c	-	-	Pin is not bonded
75	CSPS_A	Power	Phase A Current Sense Supply	Power to phase A floating current sense. Connect to either VFLT_A pin 73 for SW_A sensing or to VGS for low-side sensing. Connect a 1µF capacitor between this pin and RTN_A pin 77
76	n/c	-	-	Pin is not bonded
77	RTN_A	Signal/Power	Phase A Current Sense Return	Ground reference for phase A floating current sense and current measurement power rail
78	CS_A	Analog Input	Phase A current sense	Current measurement input for phase A floating current sensing, with a ±250mV linear range across the phase A sense resistor
79	n/c	-	-	Pin is not bonded
80	MGND	Ground	Motor Ground	All MGND pins 53, 60, 66, 67, 80, 94, 104, 106, 121, and 137 must be used, connected together via a plane or split-plane on the PCB, for the return rail to the lower MOSFET drivers. MGND connects to the return rail of the motor and resolver/LVDT power supplies. MGND may vary from -10V to +8V with respect to SGND
81	VGS_B	Power	FET Gate Drive Rail	Connect to the MOSFET gate driver power supply VGS (10V to 18V) via a 1Ω series resistor close to the pin. Bypass VGS (not pin 81) at the series resistor with a 10µF capacitor to MGND
82	LD_B	FET Driver	Low-side FET Driver	Phase B lower N-channel MOSFET gate driver. Connect through a resistor such as 20Ω to the MOSFET's gate. MGND provides the return current path
83	n/c	-	-	Pin is not bonded
84	SW_B	FET Switch	MOSFET Source	Phase B upper N-channel MOSFET gate driver source connection
85	UD_B	FET Driver	High-side FET Driver	Phase B upper N-channel MOSFET gate driver. Connect through a resistor such as 20Ω to the MOSFET's gate. MGND provides the return current path

Pin	Name	Pin Type	Pin Function	Description
86	n/c	-	-	Pin is not bonded
87	VFLT_B	Power	High-side FET Gate Drive Rail	Floating gate drive power rail for upper N-channel MOSFET gate driver B. Bypass close to the pin with a 1µF capacitor to SW_B. Connect a silicon or Schottky diode such as 1N5809US, 1N5811US or 1N6864US between VFLT_B and VGS_B pin 81
88	n/c	-	-	Pin is not bonded
89	CSPS_B	Power	Phase B Current Sense Supply	Power to phase B floating current sense. Connect to either VFLT_B pin 87 for SW_B sensing or to VGS for low-side sensing. Connect a 1µF capacitor between this pin and RTN_B pin 91
90	n/c	-	-	Pin is not bonded
91	RTN_B	Signal/Power	Phase B Current Sense Return	Ground reference for phase B floating current sense and current measurement power rail
92	CS_B	Analog Input	Phase B current sense	Current measurement input for phase B floating current sensing, with a ±250mV linear range across the phase B sense resistor
93	n/c	-	-	Pin is not bonded
94	MGND	Ground	Motor Ground	All MGND pins 53, 60, 66, 67, 80, 94, 104, 106, 121, and 137 must be used, connected together via a plane or split-plane on the PCB, for the return rail to the lower MOSFET drivers. MGND connects to the return rail of the motor and resolver/LVDT power supplies. MGND may vary from -10V to +8V with respect to SGND
95	n/c	-	-	Pin is not bonded
96	VMPS	Power	Motor Power supply	Motor power rail, used for the upper MOSFET drivers charge pump, VBOOST pin 100. Connect a 1µF capacitor between this pin and MGND
97	n/c	-	-	Pin is not bonded
98	CPP	Output	Charge Pump Flying Capacitor inverting	Flying capacitor negative node for the internal VBOOST charge pump. Connect a 0.47µF capacitor between this pin and CPN pin 102. CPP swings between VMPS and (VMPS + VGS)
99	n/c	-	-	Pin is not bonded
100	VBOOST	Power	Upper MOSFET Driver Charge Pump	Charge pump output which is VGS volts above VMPS, unloaded. Connect a 1µF capacitor between this pin and VMPS pin 96
101	n/c	-	-	Pin is not bonded
102	CPN	Output	Charge Pump Flying Capacitor inverting	Flying capacitor negative node for the internal VBOOST charge pump. Connect a 0.47µF capacitor between this pin and CPP pin 98. CPN swings between MGND and VGS
103	VGS	Power	VBOOST Charge Pump Supply Rail	Connect to the VGS MOSFET gate driver power supply (10V to 18V). This VGS pin powers to the VBOOST charge pump, pins 98-102. Bypass close to the pin with a 1µF capacitor to MGND
104	MGND	Ground	Motor Ground	All MGND pins 53, 60, 66, 67, 80, 94, 104, 106, 121, and 137 must be used, connected together via a plane or split-plane on the PCB, for the return rail to the lower MOSFET drivers. MGND connects to the return rail of the motor and resolver/LVDT power supplies. MGND may vary from -10V to +8V with respect to SGND
105	$\overline{\text{EXT\_VEE\_EN}}$	Control Input (1MΩ to VGS)	External VEE Enable	Active high (leave open or tie to VGS) to enable the VEE charge pump. Connect to MGND to disable the VEE charge pump, and connect a negative supply in the range -VGS to -8V to VEE pin 65
106	MGND	Ground	Motor Ground	All MGND pins 53, 60, 66, 67, 80, 94, 104, 106, 121, and 137 must be used, connected together via a plane or split-plane on the PCB, for the return rail to the lower MOSFET drivers. MGND connects to the return rail of the motor and resolver/LVDT power supplies. MGND may vary from -10V to +8V with respect to SGND
107	n/c	-	-	Pin is not bonded
108	CS_C	Analog Input	Phase C current sense	Current measurement input for phase C floating current sensing, with a ±250mV linear range across the phase C sense resistor
109	RTN_C	Signal/Power	Phase C Current Sense Return	Ground reference for phase C floating current sense and current measurement power rail
110	n/c	-	-	Pin is not bonded
111	CSPS_C	Power	Phase C Current Sense Supply	Power to phase C floating current sense. Connect to either VFLT_C pin 113 for SW_C sensing or to VGS for low-side sensing. Connect a 1µF capacitor between this pin and RTN_C pin 109

Pin	Name	Pin Type	Pin Function	Description
112	n/c	-	-	Pin is not bonded
113	VFLT_C	Power	High-side FET Gate Drive Rail	Floating gate drive power rail for upper N-channel MOSFET gate driver C. Bypass close to the pin with a 1µF capacitor to SW_C. Connect a silicon or Schottky diode such as 1N5809US, 1N5811US or 1N6864US between VFLT_C and VGS_C pin 119
114	n/c	-	-	Pin is not bonded
115	UD_C	FET Driver	High-side FET Driver	Phase C upper N-channel MOSFET gate driver. Connect through a resistor such as 20Ω to the MOSFET's gate. MGND provides the return current path
116	SW_C	FET Switch	MOSFET Source	Phase C upper N-channel MOSFET gate driver source connection
117	n/c	-	-	Pin is not bonded
118	LD_C	FET Driver	Low-side FET Driver	Phase C lower N-channel MOSFET gate driver. Connect through a resistor such as 20Ω to the MOSFET's gate. MGND provides the return current path
119	VGS_C	Power	FET Gate Drive Rail	Connect to the MOSFET gate driver power supply VGS (10V to 18V) via a 1Ω series resistor close to the pin. Bypass VGS (not pin 119) at the series resistor with a 10µF capacitor to MGND
120	n/c	-	-	Pin is not bonded
121	MGND	Ground	Motor Ground	All MGND pins 53, 60, 66, 67, 80, 94, 104, 106, 121, and 137 must be used, connected together via a plane or split-plane on the PCB, for the return rail to the lower MOSFET drivers. MGND connects to the return rail of the motor and resolver/LVDT power supplies. MGND may vary from -10V to +8V with respect to SGND
122	n/c	-	-	Pin is not bonded
123	CS_D	Analog Input	Phase D current sense	Current measurement input for phase D floating current sensing, with a ±250mV linear range across the phase D sense resistor
124	RTN_D	Signal/Power	Phase D Current Sense Return	Ground reference for phase D floating current sense and current measurement power rail
125	n/c	-	-	Pin is not bonded
126	CSPS_D	Power	Phase D Current Sense Supply	Power to phase D floating current sense. Connect to either VFLT_D pin 128 for SW_D sensing or to VGS for low-side sensing. Connect a 1µF capacitor between this pin and RTN_D pin 124
127	n/c	-	-	Pin is not bonded
128	VFLT_D	Power	High-side FET Gate Drive Rail	Floating gate drive power rail for upper N-channel MOSFET gate driver D. Bypass close to the pin with a 1µF capacitor to SW_D. Connect a silicon or Schottky diode such as 1N5809US, 1N5811US or 1N6864US between VFLT_D and VGS_D pin 136
129	n/c	-	-	Pin is not bonded
130	UD_D	FET Driver	High-side FET Driver	Phase D upper N-channel MOSFET gate driver. Connect through a resistor such as 20Ω to the MOSFET's gate. MGND provides the return current path
131	SW_D	FET Switch	MOSFET Source	Phase D upper N-channel MOSFET gate driver source connection
132	n/c	-	-	Pin is not bonded
133	n/c	-	-	Pin is not bonded
134	LD_D	FET Driver	Low-side FET Driver	Phase D lower N-channel MOSFET gate driver. Connect through a resistor such as 20Ω to the MOSFET's gate. MGND provides the return current path
135	n/c	-	-	Pin is not bonded
136	VGS_D	Power	FET Gate Drive Rail	Connect to the MOSFET gate driver power supply VGS (10V to 18V) via a 1Ω series resistor close to the pin. Bypass VGS (not pin 136) at the series resistor with a 10µF capacitor to MGND
137	MGND	Ground	Motor Ground	All MGND pins 53, 60, 66, 67, 80, 94, 104, 106, 121, and 137 must be used, connected together via a plane or split-plane on the PCB, for the return rail to the lower MOSFET drivers. MGND connects to the return rail of the motor and resolver/LVDT power supplies. MGND may vary from -10V to +8V with respect to SGND
138	TEST MODE2	Factory Use	Test	Internally bonded test node. Tie this pin to MGND
139	DMOD_ BW	Logic Input (1MΩ to SGND)	DMOD Driver Bandwidth	To select a shorter exciter propagation delay (recommended for 100krad TID lifetime), tie DMOD_BW to VDD. To select an increased exciter propagation delay and lower current consumption, either leave DMOD_BW open or tie DMOD_BW to SGND
140	n/c	-	-	Pin is not bonded

Pin	Name	Pin Type	Pin Function	Description
141	SGND	Power	Signal Ground	All SGND pins 27, 37, 38, 43, 44, 51, 52, 141 and 156 must be used, connected together and to the exposed pad for the signal ground. SGND may vary from -10V to +8V with respect to MGND
142	TEST MODE1	Factory Use	Test	Internally bonded test node. Tie this pin to SGND
143	SCP	Logic Input (1MΩ to VDD)	Simultaneous Conduction Protection	To prevent both UD# and LD# for any switch pair from being held on simultaneously, either leave SCP open or tie SCP to VDD. To allow UD# and LD# to operate independently, tie SCP to SGND
144	n/c	-	-	Pin is not bonded
145	TEST MODE0	Factory Use	Test	Internally bonded test node. Tie this pin to SGND
146	BL_TH	Analog Input	Bi-Level (-) threshold input	Negative (-) threshold voltage between 0.5V and 4.5V for the fixed threshold bi-level monitors (comparators) BL1 to BLI6
147	VCC	Power	Signal Supply	Connect to the signal power supply (4.75V to 5.25V). All VCC pins 25, 26, 41, 42, and 147 must be used. Bypass close to the pin with a 1µF capacitor to SGND
148	n/c	-	-	Pin is not bonded
149	VPROG	Factory Use	Test	Internally bonded test node. Tie this pin to VCC
150	BLI1	Analog Input	Bi-Level (+) input 1	Fixed threshold bi-level monitor (comparator) positive (+) input 1 which is compared against either an external voltage between 0.5V and 4.5V on the BL_TH pin 119. The output is BLO1 pin 157
151	BLI2	Analog Input	Bi-Level (+) input 2	Fixed threshold bi-level monitor (comparator) positive (+) input 2 which is compared against either an external voltage between 0.5V and 4.5V on the BL_TH pin 119. The output is BLO2 pin 158
152	BLI3	Analog Input	Bi-Level (+) input 3	Fixed threshold bi-level monitor (comparator) positive (+) input 3 which is compared against either an external voltage between 0.5V and 4.5V on the BL_TH pin 119. The output is BLO3 pin 159
153	BLI4	Analog Input	Bi-Level (+) input 4	Fixed threshold bi-level monitor (comparator) positive (+) input 4 which is compared against either an external voltage between 0.5V and 4.5V on the BL_TH pin 119. The output is BLO4 pin 160
154	BLI5	Analog Input	Bi-Level (+) input 5	Fixed threshold bi-level monitor (comparator) positive (+) input 5 which is compared against either an external voltage between 0.5V and 4.5V on the BL_TH pin 119. The output is BLO5 pin 2
155	BLI6	Analog Input	Bi-Level (+) input 6	Fixed threshold bi-level monitor (comparator) positive (+) input 6 which is compared against either an external voltage between 0.5V and 4.5V on the BL_TH pin 119. The output is BLO6 pin 3
156	SGND	Power	Signal Ground	All SGND pins 27, 37, 38, 43, 44, 51, 52, 141 and 156 must be used, connected together and to the exposed pad for the signal ground. SGND may vary from -10V to +8V with respect to MGND
157	BLO1	Logic Output	Bi-Level Output 1	Output of fixed threshold bi-level monitor (comparator) input BLI1 at pin 150
158	BLO2	Logic Output	Bi-Level Output 2	Output of fixed threshold bi-level monitor (comparator) input BLI2 at pin 151
159	BLO3	Logic Output	Bi-Level Output 3	Output of fixed threshold bi-level monitor (comparator) input BLI3 at pin 152
160	BLO4	Logic Output	Bi-Level Output 4	Output of fixed threshold bi-level monitor (comparator) input BLI4 at pin 153
EP	Exposed Pad			Connect the exposed pad to the SGND signal ground pins 27, 37, 38, 43, 44, 51, 52, 141 and 156

Notes

1. Pins that are shown as not bonded may be connected to any potential, such as an adjacent pin or GND, subject to the creepage and clearance requirements of the PCB layout

6 Absolute Maximum Ratings

Stresses above those listed in ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Parameter	Min	Max	Units
Motor Power Supply (VMPS) to MGND	-0.5	80	V
Switch (SW_# and RTN_#) to MGND	-1.0	80	V
Signal Power Supply (VCC) to SGND	-0.5	7	V
Logic Supply Voltage (VDD) to SGND	-0.5	7	V
Signal Ground (SGND) to Motor Ground (MGND) Potential Difference	-10	10	V
Gate Driver Power Supply (VGS) to MGND	-0.5	22	V
Negative Power Supply (VEE_IN) to MGND	-22	0.5	V
Voltage Reference (VREF_IN) to SGND	-0.5	7	V
Resolver Power Supply (DMOD_PS) to MGND	-0.5	22	V
Current Sense Power Supply (CSPS_#) to RTN_#	-0.5	22	V
Current Sense Inputs (CS_#) to RTN_#	-5	5	V
System Controller Interface (BLO#, UD_IN_#, LD_IN_#, DMOD_IN_#, CP_CLK, #_FAULT, SM_EN, RESET, SNS_OUT_#, ADC#, MOD_CLK, CLK_OUT, SCP) to SGND	-0.5	(VDD + 0.5), <7	V
Bi-Level Inputs (BLI1 to BLI6, BL_TH) to SGND	-0.5	7	V
Bi-Level Inputs Clamp Current	-3	3	mA
ADC#_P, ADC#_N to SGND	-0.5	7	V
SW_# Slew Rate	0	10	kV/µs
Operating Junction Temperature	-55	150	°C
Storage Junction Temperature	-65	160	°C
Peak Lead Solder Temperature (10 seconds)		260 (+0, -5)	°C

7 Electrostatic Discharge Ratings

JEDEC JEP155 and JEP157 state that 500V HBM and 250V CDM respectively allows safe manufacturing with a standard ESD controlled process. ESD ratings apply to all pins.

ESD Test	Minimum Capability
HBM: Human Body Model, per MIL-STD-883 TM3015	±500V
CDM: Charged Device Model, per ANSI/ESDA/JEDEC JS-002	±250V

8 Operating Ratings

Performance is generally guaranteed over this range as further detailed below under Electrical Characteristics.

Parameter	Min	Max	Units
Motor Power Supply (VMPS) and Switch (SW_# and RTN_#) to MGND	20	60	V
Signal Power Supply (VCC) to SGND	4.75	5.25	V
Logic Supply Voltage (VDD) to SGND	2.1	5.5	V
Gate Driver Power Supply (VGS) to MGND (with VGS to SGND > 7V)	10	18	V
Negative voltage reference (VEE_IN). See Table 2 on page 24	-VGS or -18	-8	V
VGS voltage if using internally generated VEE	12	18	V
VFLT_# bootstrap diode forward DC current	0	100	mA
VFLT_# bootstrap diode peak repetitive current	-1	1	A
VFLT_# bootstrap diode forward current at hard switching to reverse bias	0	50	mA
VFLT_# bootstrap diode maximum dissipated power	0	120	mW
Voltage reference (VREF_IN) to SGND	2.3	2.7	V
DMOD_PS exciter voltage to MGND (with DMOD_PS to SGND > 7V)	10	18	V
DMOD_PS exciter current	0	100	mA
One MOSFET driver average source/sink (Qg x Fsw)	0	25	mA
Current sense power supply (CSPS_#) to RTN_#	10	18	V
Current sense (CS_#) to RTN_#	-250	250	mV
Ground potential difference (MGND to SGND)	-10	8	V
CP_CLK frequency range	100	300	kHz
MOD_CLK frequency range	24	32	MHz

9 Electrical Characteristics

The following specifications apply over the operating ambient temperature of -55°C ≤ T_A ≤ 125°C except where otherwise noted with the following test conditions: V_{VCC}= 5V, V_{VDD} = 3.3V; V_{VREF_IN} = 2.5V; V_{VGS} = 15V; V_{VEE} = -15V ($\overline{EXT\_VEE}$=GND); V_{DMOD_PS} = 15V; V_{BL_TH} = 2.5V; MOD_CLK = 32MHz; CP_CLK = 200kHz, V_{VMPS} = 50V.Typical parameters refer to T_J = 25°C. Positive currents flow into pins. THD is measured based on fundamental and harmonics up to seventh order. Specifications apply to both ceramic and plastic packaged parts unless otherwise stated.

Symbol	Parameter	Test Conditions/Comments	Min	Typ	Max	Units
Operating Current						
I_{VCC}	VCC Current (total for all VCC pins)	All ADCs off, all current sense off	5	15	20	mA
		All ADCs on, all current sense off	25	46	55	mA
		All ADCs off, all current sense on	35	67	80	mA
		All ADCs on, all current sense on	60	98	120	mA
I_{VGS}	VGS Current (total for all VGS pins)	All UD_IN# and LD_IN# low	10	20	26	mA
		All LD_IN# and UD_IN# high	15	26	33	mA
I_{VEE}	VEE Current	All UD_IN# and LD_IN# low	-12	-8	-4	mA
		All UD_IN# and LD_IN# low; VEE = -15V; no load on DMOD_OUT_N/P; DMOD_IN_P high; DMOD_IN_N low; DMOD_BW low; DMOD_PS = 15V	-21	-14	-6	mA
I_{DMOD_PS}	DMOD_PS Current	No load on DMOD_OUT_N/P; DMOD_IN_P and DMOD_IN_N low; DMOD_BW low; DMOD_PS = 15V	0.2	1	1.5	mA
		No load on DMOD_OUT_N/P; DMOD_IN_P high; DMOD_IN_N low; DMOD_BW low; DMOD_PS = 15V	2	6	11	mA
		No load on DMOD_OUT_N/P; DMOD_IN_P high; DMOD_IN_N low; DMOD_BW high; DMOD_PS = 15V	4	10	17	mA
I_{VDD}	VDD Current	All LD_IN# = HI and UD_IN# = HI	0	25	42	mA
Internally Regulated Voltages and Currents						
$V_{VREF\_OUT(ceramic)}$	VREF reference		2.48	2.5	2.52	V
$V_{VREF\_OUT(plastic)}$			2.47			
V_{VEE}	Inverting charge pump	No external load; $\overline{EXT\_VEE}$ = open; V_{VGS} -|V_{VEE}|	1.0	1.9	2.4	V
V_{VBOOST}	Charge pump	Boot strap not connected;10mA load [V_{VGS} + V_{VMPS}] - V_{VBOOST}	0.5	1.6	2.1	V
V_{VBOOST} - $V_{VFLT\#}$	VBOOST switch	With UD_IN_# high	0.05	0.3	0.6	V
I_{VREF_OUT}	VREF reference	Short Circuit Current	25	50		mA
$I_{VGS\#(ceramic)}$	Fault threshold	VGS_A, VGS_B, VGS_C and VGS_D fault current threshold	110		360	mA
$I_{VGS\#(plastic)}$			90		370	
$I_{VGS\#}$	Fault blanking	VGS# spike duration to trigger fault (400mA load)	1.5	3.5		µs
$I_{DMOD\_PS(ceramic)}$	Fault threshold	DMOD_PS fault current threshold	110		360	mA
$I_{DMOD\_PS(plastic)}$			90		370	
I_{DMOD_PS}	Fault blanking	DMOD_PS spike duration to trigger fault (400mA load)	1.5	3.5		µs
Under Voltage Detection						
V_{VCC}	VCC UVLO	Voltage rising; 200mV Hysteresis	4	4.25	4.5	V
V_{VDD}	VDD UVLO	Voltage rising; 200mV Hysteresis	1.6	1.8	2.0	V
V_{VGS} to MGND	VGS UVLO to MGND	Voltage falling; 200mV Hysteresis	9.1	9.4	9.8	V
V_{VGS} to SGND	VGS UVLO to SGND	Voltage rising; 120mV Hysteresis	6.2	6.4	6.6	V
V_{VEE}	VEE_IN UVLO	Voltage falling; 350mV Hysteresis	-8	-7	-6	V
Clocks						
F_{MOD_CLK}	MOD_CLK	Frequency range	24		32	MHz
P_{MOD_CLK}	MOD_CLK missing	Minimum non-transition dead time		200		ns
P_{CLK_OUT}	CLK_OUT	Delay CLK_OUT to ADC# and SENS_OUT_#	0.5	7	15	ns
F_{CP_CLK}	CP_CLK	Frequency range	100	200	300	kHz

Symbol	Parameter	Test Conditions/Comments	Min	Typ	Max	Units
Logic Levels						
$V_{LOG\_IN\_VDD}$	Input logic threshold for VDD related inputs: UD_IN_#, DMOD_IN_#, SM_EN, RESET, MOD_CLK, SCP	V_{IH}	70			%VDD
		V_{IL}			30	%VDD
		Hysteresis at VDD = 3.3V	100	160	220	mV
$I_{LOG\_IN\_VDD}$	Input current for above VDD related inputs	V_{LOG_IN} = 3.3V (with pull down resistor)	1.5	4	7	µA
		V_{LOG_IN} = 0V (with pull up resistor)	-7	-4	-1.5	
$V_{LOG\_IN\_EXT\_VEE}$	Input logic threshold for EXT_VEE	V_{IH}	1.2			V
		V_{IL}			0.25	
$I_{LOG\_IN\_EXT\_VEE}$	Input current for EXT_VEE	V_{LOG_IN} = 0V	-80	-38	-10	µA
$V_{LOG\_IN\_DMOD\_BW}$	Input logic threshold for DMOD_BW	V_{IH}	1.8			V
		V_{IL}			0.4	
$I_{LOG\_IN\_DMOD\_BW}$	Input current for DMOD_BW	V_{LOG_IN} = 3.3V	10	37	80	µA
		V_{LOG_IN} = 0V	-1	0	1	
$V_{LOG\_OUT\_VDD}$	Logic output levels for VDD related outputs: BLO_#, PR_FAULT, OC_FAULT, OTW_FAULT, CLK_OUT, SNS_OUT_#, ADC#	High logic level (100µA source)	VDD - 0.3	VDD - 0.06	VDD	V
		Low logic level (100µA sink)	0	0.03	0.3	
Fixed Threshold Bi-Level Inputs						
$V_{BL\_TH\#}$	Threshold, rising voltage		2.4	2.5	2.6	V
$V_{BL\_HYS\#}$	Hysteresis	Rising threshold = $V_{BL\_TH\#}$ Falling threshold = ($V_{BL\_TH\#}$ - $V_{BL\_HYS\#}$)	80	150	200	mV
$V_{BLI\#}$	Voltage Clamp	Clamp Current = 1mA into pin	6.5	10	13	V
		Clamp Current = -1mA out of pin	-1.9	-1.4	-0.9	
$I_{BLI\#}$	Bias Current	$V_{BLI\#}$ = 0V to 5V	-2	0	2	µA
	Leakage Current	$V_{BLI\#}$ = 0V to 5V; IC powered off	-1	0	1.2	µA
$t_{BLI\#}$	Propagation Delay		10	40	80	ns
I_{BL_TH}	Threshold Pin Leakage	V_{BL_TH}= 0V to 5V	-1	0	1.5	µA
Internal bootstrap diodes						
V_{ON_B}	Forward voltage	I_F = 100mA, T_j = 25°C	0.9		1.1	V
		I_F = 100mA, T_j = -55°C and 125°C	0.8		1.2	V
t_{RR_B}	Reverse recovery time	I_F = 100mA, V_R=9V, dI_F/dt = 1A/µs		600		ns
I_{RM_B}	Peak reverse recovery current	I_F = 100mA, V_R=9V, dI_F/dt = 1A/µs		90		mA
MOSFET DRIVER (C_{load} = 1000pF)						
$R_{UD\#}$	Upper driver impedance	VFLT# to UD_#; UD_IN_# = high	0.85		10.0	Ω
		UD_# to SW_#; UD_IN_# = low	0.85		10.0	
		UD_# to SW_#, VGS = 0 to UVLO			20k	
$R_{LD\#}$	Lower driver impedance	VGS_OUT to UD_#; LD_IN_# = high	0.85		10.0	Ω
		LD_# to MGND; LD_IN_# = low	0.85		10.0	
		LD_# to MGND; VGS = 0 to UVLO			20k	
$t_{PHL, PLH}$	Propagation delay	Upper driver; UD_IN_# to UD_A	140	250	400	ns
		Lower driver; LD_IN_# to LD_A	140	250	400	
		Matching all drivers, all edges			150	
$t_{R,F}$	Rise time and fall time	10% to 90%	20	60	120	ns
t_{PWH}, t_{PWL}	Minimum input pulse width (high or low)	Output reaches 67% VGS for t_{PWH} and 1V for t_{PWL}			300	ns
$I_{UD\#}$	Leakage current with VGS and VCC = 0V	UD_#, SW_#, VFLT_# wired together; $V_{SW\_\#}$ = 0V to 80V ref to MGND	-50		50	µA
$V_{UD\#}$	Upper drive voltage with 100% duty cycle	UD_IN# held high, UD_# loaded with 4mA. Measured relative to VMPS	11.5		15	V

Symbol	Parameter	Test Conditions/Comments	Min	Typ	Max	Units
Demodulator driver (differential load of 100Ω)						
$V_{DMOD\_OUT\_P, N}$	Voltage Range	Either output relative to MGND	10		18	V
$R_{DMOD\_OUT\_P, N}$	Source Impedance	With respect to DMOD_PS; Sourcing current	0.8	2	4	Ω
		With respect to MGND; Sinking current	0.8	2	4	
t_{PHL}	Propagation Delay H to L	DMOD_IN_# to DMOD_OUT_#; DMOD_BW = HI	65		145	ns
		DMOD_IN_# to DMOD_OUT_#; DMOD_BW = LOW	75		155	
t_{PLH}	Propagation Delay L to H	DMOD_IN_# to DMOD_OUT_#; DMOD_BW = HI	65		145	ns
		DMOD_IN_# to DMOD_OUT_#; DMOD_BW = LOW	75		155	
$t_{PHL, PLH}$	Propagation Delay	Matching between DMOD_OUT_P and MOD_OUT_N; HL to HL and LH to LH		7	20	ns
t_R	Rise time	10% to 90%	4	17	30	ns
t_F	Fall time	10% to 90%	6	33	60	ns
ADC Converters (with sinc³ filter and OSR = 256, input common mode = 2.1V unless otherwise specified)						
$FSR_{ADC\_\#}$	Max differential input	Extrapolated clipping points of PDM output		±1400		mV
$SLR_{ADC\_\#}$	Specified linear range			±800		mV
$V_{CMR\_ADC\_\#}$	Input common mode	With Vdiff = ±800mV and THD < $THD24/32_{ADC}$(Max) - 3dB	0.5		VCC - 2.1V	V
$V_{CMR\_ADC\_\#(ceramic)}$	Common mode rejection	0.5V to 2.9V	43			dB
$V_{CMR\_ADC\_\#(plastic)}$			41			dB
$BW_{ADC\_\#}$	Max frequency	With attenuation < 0.1dB	20			kHz
	Min frequency	By design			0	Hz
$AV_{ADC\_\#(ceramic)}$	Gain error from ±1400mV full scale	T_j = 25°C and 125°C	-0.65		0.65	%
		T_j = -55°C	-0.8		0.8	%
$AV_{ADC\_\#(plastic)}$		T_j = 25°C and 125°C	-0.75		0.75	%
		T_j = -55°C	-1		1	%
V_{OS_ADC}	Offset error	Equivalent input for code measured to shorted inputs. T_j = 25°C	-0.05		0.05	%FSR
		Equivalent input for code measured to shorted inputs. T_j = 125°C	-0.12		0.12	%FSR
		Equivalent input for code measured to shorted inputs. T_j = -55°C	-0.5		0.5	%FSR
$INL24_{ADC}$	Integral Non-Linearity	Gain error from straight line at 24MHz (±800mV signal)	-0.03	±0.01	0.03	%FSR
$INL32_{ADC}$	Integral Non-Linearity	Gain error from straight line at 32MHz (±800mV signal)	-0.06	±0.02	0.06	%FSR
$RES24_{ADC}$	No missing codes resolution at 24MHz	Histogram test using triangular wave	14	15		bits
$RES32_{ADC}$	No missing codes resolution at 32MHz	Histogram test using triangular wave	13	14		bits
$SNR24_{ADC}$	Signal to Noise Ratio at 24MHz clock	Full scale sinewave RMS / noise RMS in 1kHz bandwidth	93	100		dB
$THD24_{ADC}$	Total Harmonic Distortion at 24MHz clock	Input frequency = 1kHz, amplitude = ±800mV		-79	-73	dB
$SNR32_{ADC}$	Signal to Noise Ratio at 32MHz clock	Full scale sinewave RMS / noise RMS in 1kHz bandwidth	92	98		dB
$THD32_{ADC}$	Total Harmonic Distortion at 32MHz clock	Input frequency = 1kHz, amplitude = ±800mV		-78	-70	dB
t_{SWTO}	ADC Timeout	ADC#_P = ADC#_N > V_{SWTO} to cause ADC modulator sleep mode	225		325	µs
V_{SWTO}	ADC timeout threshold		VCC - 0.25	VCC - 0.1	VCC	V
$C_{ADC\#}$	Diff input capacitance			10		pF
$R_{ADC\#}$	Diff input resistance		50	250		kΩ

Symbol	Parameter	Test Conditions/Comments	Min	Typ	Max	Units
Floating Current Sense (with sinc³ filter and OSR = 256, input common mode = 0V unless otherwise specified)						
$FSR_{CS\_\#}$	Max differential input	Clipping points of PDM output		±350		mV
$SLR_{CS\_\#}$	Specified linear range			±250		mV
E_{CMR_CS}	Input common mode induced gain error	Input common mode from 0 to 50V	-0.15		0.15	%
V_{CMR_CS}	Input common mode rejection	CM = 50V	85			dB
$BW_{CS\_\#}$	Max frequency	With attenuation < 3dB	75			kHz
	Min frequency	With attenuation < 0.1dB			0	Hz
$AV_{CS\_\#}$	Gain error from ±350mV full scale	T_j = 25°C	-0.5		0.5	%
		T_j = -55°C and 125°C	-1.3		1.3	%
$V_{OS\_CS(ceramic)}$	Offset error	$V_{CS\_\#} = V_{RTN\_\#}$, T_j = 25°C	-0.4		0.4	%FSR
		$V_{CS\_\#} = V_{RTN\_\#}$, T_j = -55°C and 125°C	-1.2		1.2	%FSR
$V_{OS\_CS(plastic)}$		$V_{CS\_\#} = V_{RTN\_\#}$, T_j = 25°C	-1		1	%FSR
		$V_{CS\_\#} = V_{RTN\_\#}$, T_j = -55°C and 125°C	-2		2	%FSR
$RES24_{CS}$	No missing codes resolution at 24MHz	Histogram test using triangular wave	14	14		bits
$RES32_{CS}$	No missing codes resolution at 32MHz	Histogram test using triangular wave	13	14		bits
$INL24_{CS}$	Integral Non-Linearity at 24MHz clock.	Gain error from straight line (±200mV signal)	-0.06	±0.03	0.06	%FSR
$INL32_{CS}$	Integral Non-Linearity at 32MHz clock	Gain error from straight line (±200mV signal)	-0.06	±0.03	0.06	%FSR
$SNR24_{CS}$	Signal to Noise Ratio at 24MHz clock	Full scale sinewave RMS / noise RMS in 4kHz bandwidth, OSR = 64	74	78		dB
$THD24_{CS}$	Total Harmonic Distortion at 24MHz clock	Input frequency = 1kHz, amplitude = ±200mV, OSR = 64		-75	-65	dB
$SNR32_{CS}$	Signal to Noise Ratio at 32MHz clock	Full scale sinewave RMS / noise RMS in 4kHz bandwidth, OSR = 64	73	77		dB
$THD32_{CS}$	Total Harmonic Distortion at 32MHz clock	Input frequency = 1kHz, amplitude = ±200mV, OSR = 64		-75	-65	dB
Z_{IN_CS}	Differential Input Impedance	CS_# to RTN_#	0.1	2		MΩ
	Common Mode Input Impedance	RTN_# or CS_# to MGND	50	150		kΩ
$I_{BIAS\_CS\#}$	CS_# bias current		-0.2		0.2	mA
$I_{BIAS\_RTN\#}$	RTN_# bias current		-1		1	mA
$V_{CS\_\#}$	Over Current Sense Threshold	Current flow into SW_# pin	260	320	380	mV
		Current flow out of SW_# pin	-380	-320	-260	
	Over Current Blanking	Spike filter pole	10		20	µs
$I_{CS\_\#}$	Leakage current with VCPS_# and VCC = 0V	CPS_#, RTN_#, CS_# wired together; V_{CS} = 0V to 80V referenced to MGND	-50		50	µA
Thermal Shutdown						
OT_SDN	Thermal shutdown threshold; SM_EN = 1	Threshold Temperature, T_{SD}	135	150	165	°C
OTW_FAULT	Over temperature warning threshold	Warning Temperature (T_{SD} - T_{OTW})	15	25	35	
		Hysteresis	10	15	25	
	Logic output levels. Logic low level is untested at 125°C because output is typically high at 125°C	High logic level (100µA source)	VDD - 0.3		VDD	V
		Low logic level (100µA sink)	0		0.3	

10 Thermal Properties

Thermal resistance, θ_{JB}, is provided from die to the back surface of the package. Junction temperature T_J is calculated using $T_J = T_B + (PD \times \theta_{JB})$, where T_B is the temperature maintained on the back surface of the package.

Package	Thermal Resistance	Typ	Units
CQFP-132	θ_{JA}	39.8	°C/W
LQFP-160		9.9	
CQFP-132	θ_{JB}	1.93	°C/W
LQFP-160		1	

11 Heatsink Recommendations

The base of the plastic package has an exposed pad to be used as the heat conducting surface. The heat dissipater can be copper layers within a multilayer circuit board.

It is strongly recommended to use the base of the ceramic package as the surface for conducting heat from the package. The metal package top is attached to the package body at the top of relatively thin cavity walls, and so has a much higher thermal resistance from the die than the base of the package. The leads can be formed to mount the part upside down if necessary.

It is also recommended to apply a thermal interface material between the base of the package and the heat dissipater. The heat dissipater can be copper layers within a multilayer circuit board to spread heat laterally across the board, or a direct mounted dissipation element.

The steady-state thermal model (Figure 1) shows the localized temperature rises when the base of the package is maintained at 25°C while dissipating 2.07W.

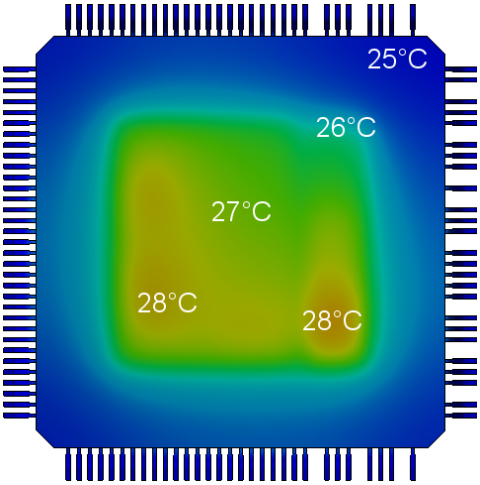


Figure 1. Ceramic Package Steady-State Thermal Model

12 Typical Application

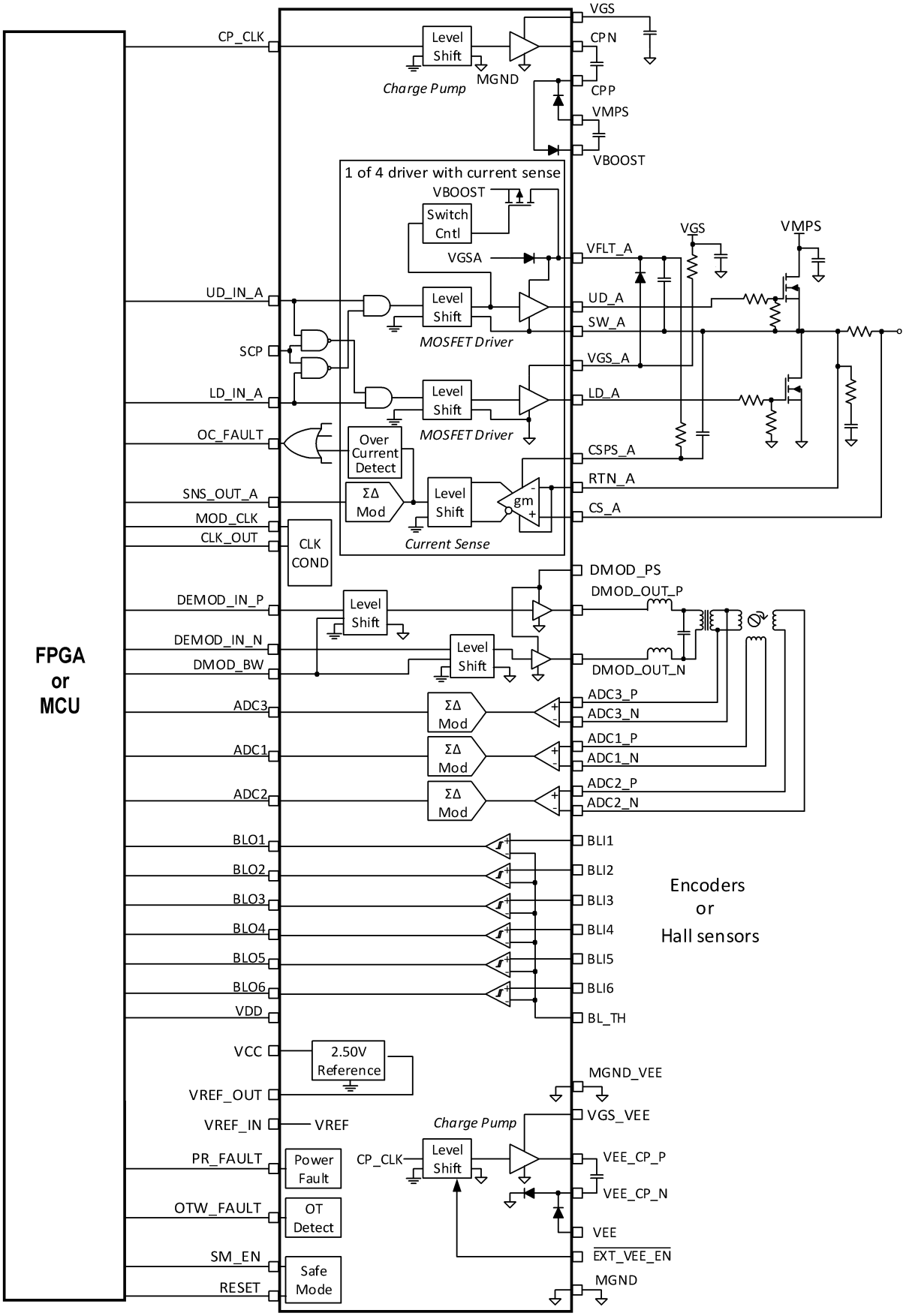


Figure 2. Typical Application

13 Introduction to the LX7720

The LX7720 targets motors that can be managed by 4 independent low-side FET drivers and 4 independent high-side FET drivers, with PWM control up to 40kHz. Typical motor applications include:

- A 3-phase star-connected Permanent Magnet Synchronous Motor (PMSM) or Brushless DC Motor (BLDC)
  - Each of the 3 motor phase windings is driven by a half-bridge
  - The 4th half-bridge drive is available for an electromagnetic brake
- A 2-winding bipolar stepper motor, operated in full-step, half-step, or micro-stepping mode
  - Each winding is driven by an H-bridge comprising a half-bridge at each side of the winding

Position feedback options built in to the LX7720 allow any combination of the interfaces below:

- One or more optical encoder using the 6 built in BLI/BLO comparators
- Up to six Hall effect sensors using some of the 6 built in BLI/BLO comparators
- An LVDT, RVDT, or resolver using the built-in primary driver and dual ADCs for the two secondaries

User guides for available Microchip IP for FPGA motor drives system controllers are here.

Higher end microcontrollers with embedded PWM peripherals are also capable of managing the LX7720. For example, the radiation-hardened SAMRH71F20, SAMRH707F18 and the radiation-tolerant SAMV71Q21RT ARM-based MCUs include two 16-bit PWM blocks. Each PWM block provides 4 complementary outputs with dead-time control, enough to control 4 half-bridges driving a motor. One of these MCUs can therefore manage two independent motor-driving LX7720s. Motor control support projects for SAM MCUs can be found on Microchip MPLAB Harmony.

The support materials provided on a USB stick with LX7720 evaluation boards can be downloaded here.

14 Power Supplies, Sequencing, and Voltage Reference

14.1 Power Supply Configurations and Decoupling

The LX7720 requires several supply voltages (Table 1) and generates floating high-side gate drive rails for the external half-bridges (section 15.1 on page 26). A negative supply rail, VEE, is generated by an internal charge pump or supplied externally as selected by the EXT_VEE_EN pin (Table 2 on page 23).

Table 1. Power Supplies and Recommended Decoupling Capacitors

Supply Pin	Voltage Range	Notes	Capacitor	Ground
VMPS	20V to 60V	Motor supply, as reference for the upper MOSFET drivers. Current draw is typically 0.65mA, 1.4mA, 2.2mA at 25°C for VMPS=20V, 40V, 60V with all 4 UD_IN# inputs low. An extra 1mA typical at 25°C, 1.2mA at 125°C is drawn for each UD_IN# input that is high (circuit of Figure 10)	1µF	MGND
VCC	4.75V to 5.25V	Main circuitry positive power supply	3x 1µF	SGND
VDD	2.1V to 5.5V	External FPGA or MCU controller's I/O power supply	1µF	SGND
VEE	-VGS to -8V	Main circuitry negative power supply (see Table 2)	1µF or 2.2µF	MGND
DMOD_PS	10V to 18V	Resolver or LVDT power supply	10µF	MGND
VREF_OUT	2.5V	Internal voltage reference	0.47µF	SGND
VGS	12V to 18V (using internal VEE charge pump), or 10V to 18V (external VEE)	Charge pump rails. Use 4.7µF on VGS pin 48/62 (ceramic/plastic), and 1µF on VGS pin 85/103 (ceramic/plastic)	4.7µF and 1µF	MGND
VGS_A, VGS_B, VGS_C, VGS_D		Individual FET gate drivers. Connect VGS_A, VGS_B, VGS_C, and VGS_D pins to VGS via an individual 1Ω series resistor at the pin (see Figure 10 on page 27). Decouple VGS (not the pin) with 4.7µF close by the resistor	3x 4.7µF (VGS_A shares 4.7µF at VGS pin 85/103)	MGND
Between CPN and CPP	VMPS + VGS	High side gate drivers charge pump flying capacitor	470nF	-
VBOOST	VGS	High side gate drivers charge pump output capacitor	1µF	VMPS
VFLT_A, VFLT_B, VFLT_C, VFLT_D	VGS	High side gate drivers individual power rails	4x 1µF	SW_#
CSPS_A, CSPS_B, CSPS_C, CSPS_D	VFLT_#, VBOOST, or VGS	Floating, high-side, or low-side current sense power rails. Fit capacitor close to CSPS_x pin, and connect to supply via 10Ω series resistor to filter supply noise. Each CSPS pin draws typically 1.3mA	4x 1µF 4x 10Ω	RTN_#

14.2 VEE Options

The negative supply, VEE, is generated by default by an internal inverting charge pump using CP_CLK as the charge pump clock (Figure 3 below). VEE is nominally -VGS, unloaded. The 4.7µF capacitor shown decoupling VGS in Figure 3 is also the decoupling capacitor for the nearby VGA_A pin. The VEE rail is used by the half-bridge gate drivers, the DMOD_OUT_x resolver/LVDT primary bridge drivers, and the VBOOST charge pump.

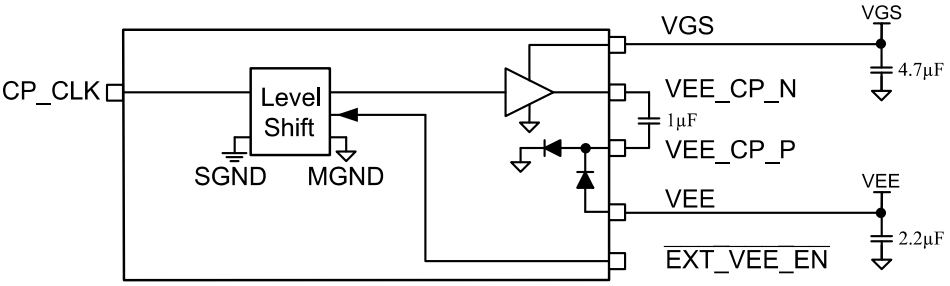


Figure 3. Internally Generated VEE Negative Supply Rail

The charge pump can be disabled and an external supply used instead (Table 2). Using an external VEE supply saves the flying capacitor, reduces the size of the VEE capacitor, and lowers the VGS minimum recommended voltage from 12V to 10V. Note that both VEE and its enable input $\overline{\text{EXT\_VEE\_EN}}$ are with respect to motor MGND, not SGND.

Table 2. VEE Supply Methods

VEE Supply Method	$\overline{\text{EXT\_VEE\_EN}}$ pin	Capacitor Between VEE_CP_P pin and VEE_CP_N pin	Capacitor on VEE pin
VEE internally generated by inverting charge pump from VGS	Open or VGS	1µF	2.2µF to MGND
VEE externally supplied (-VGS to -8V) directly to VEE pin	MGND	1µF	
VEE externally supplied (-18V to -8V) directly to VEE pin		Not fitted. VEE_CP_P and VEE_CP_N pins can be left open or a 1µF capacitor fitted between	

14.3 Power Rail Sequencing

Any combination of supply rails can be up or down safely without damaging the LX7720 itself. However, a minimal power rail sequencing strategy is necessary to ensure that the LX7720's half-bridge gate drivers are reset from random start-up states to their off states before current can flow through the external MOSFETs. The half-bridge gate drivers are reset when the VDD rail rises above 1V. This needs to occur before VMPS, VCC and VGS are all powered up to avoid inadvertent MOSFET turn-on. If a half-bridge channel's random start-up state is on for both the high-side and low-side MOSFET, then the VMPS motor drive supply is shorted through the half-bridge.

Sequencing recommendations are either:

- Ensure that VDD is not the last rail to come up: power VDD before one or more of the VCC, VGS, or VMPS rails
  - VCC has a 300µs power-on-reset, so VDD can be brought up safely coincident with VCC
- Ensure that VDD is biased to at least 1V by one of the VCC, VGS, or VMPS rails
  - VDD can be biased from the 5V VCC rail by fitting a Zener from VCC (+5V) to VDD. If a moderate power rated Zener is used, the voltage drop will be lower than the nominal zener voltage rating due to the relatively low operating current. For example, a 4.3V 1W 1N4731A Zener is specified at 58mA. When used in the circuit of Figure 4 below, the voltage drop was 3.5V with 0.5mA current, therefore biasing VDD to 1.5V
  - Figure 4 shows VDD being fed through a Schottky diode D2 to isolate other 3.3V loads (and their capacitance) from the Zener D1. If the LX7720 has its own independent 3.3V supply, D2 can be omitted

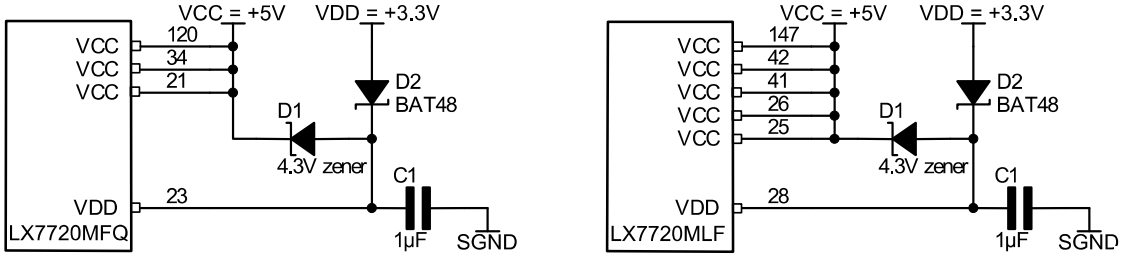


Figure 4. Zener diode VDD biasing for fast start-up with VCC

14.4 Voltage Reference

The LX7720 includes a 2.5V ±0.8% voltage reference, available at the VREF_OUT pin. To use this reference, connect VREF_OUT to the adjacent VREF_IN pin. Alternatively, connect an external 2.3V to 2.7V reference to VREF_IN. In either case, connect a 0.47µF capacitor from VREF_OUT to SGND.

14.5 SGND and MGND

The LX7720 uses two internal ground domains, the Signal Ground (SGND), and the Motor Ground (MGND), with level shifters managing the crossing of the ground domains:

- SGND is used for the digital and analog signals (the control circuitry)
  - The VCC, VDD, and VREF supplies use SGND
- MGND is used for circuitry associated with the half-bridges - the FET drives, current sensing, and the motor load itself
  - The VMPS, VGS, DMOD_PS, and VEE supplies use MGND.

If a motor controller board design locates the motor drive half-bridge FETs on the same PCB as the LX7720 itself, then the two grounds SGND and MGND can be joined together directly on the PCB, and therefore will be at the same potential.

For high power motor designs, it can be more practical not to route the VMPS high voltage and/or high current paths on the controller PCB. In this case, the motor drive half-bridge FETs will be on a separate module or PCB, with a wiring harness providing the motor supply VMPS and its associated power ground return. The LX7720 still needs a connection to these external motor supply rail (VMPS) and motor ground rail (MGND). Note that now SGND is not directly connected to MGND but relies on the system ground path external to the PCB that the LX7720 is on. However, since the motor's power wiring is carrying high current motor waveforms, there will be ground bounce between external MGND at the motor and the LX7720's local SGND. The allowed potential difference between MGND and SGND is -10V to +8V. If analysis of the end system shows that this might be exceeded during transients, a back-to-back zener diode pair between SGND and MGND may be enough to clamp these occurrences (Figure 5 below).

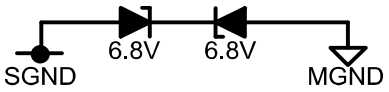


Figure 5. Clamping SGND and MGND with Back-To-Back Zener Diodes

14.6 SGND Supply Pin Interconnections

The SGND rail is separated internally as a digital ground domain and an analog ground domain to minimize digital noise coupling into the analog circuitry. The ground domains are, however, interconnected radially by back-to-back diodes (Figure 6 below) to constrain transient voltage differences between grounds. Ensure that all SGND pins are connected to the board's low-impedance SGND rail.

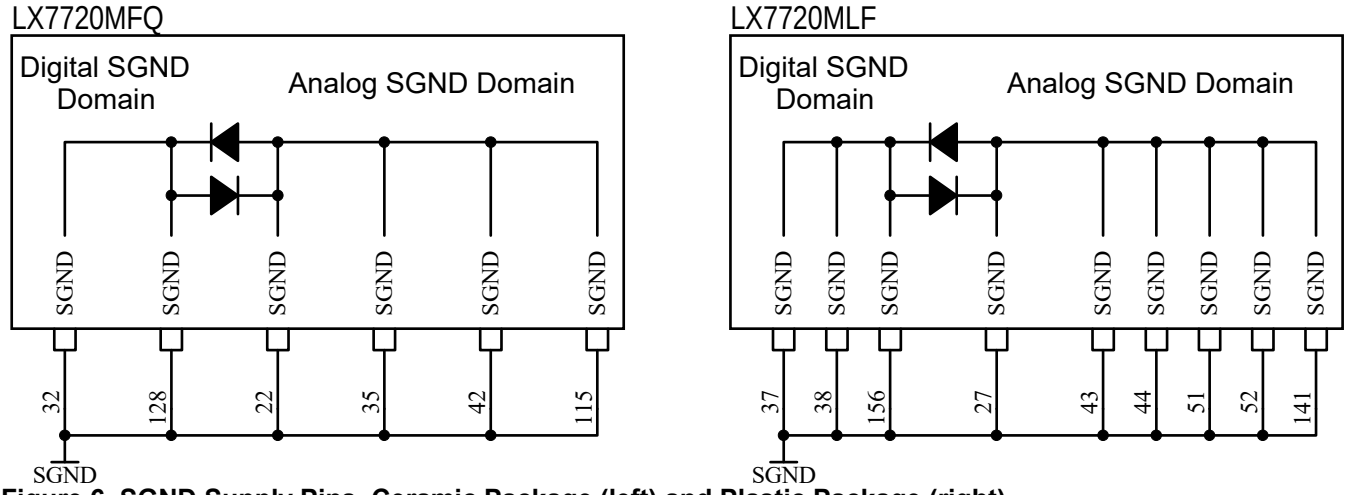


Figure 6. SGND Supply Pins, Ceramic Package (left) and Plastic Package (right)

15 Half-Bridge MOSFET Drivers

The LX7720 contains four high speed N channel MOSFET half bridge drivers with independent high-side and low-side controls. Isolation up to -10V and +8V is provided between the system ground (SGND) and the motor ground (MGND).

Slew rate control is recommended to keep dV/dt at the SW_# pins under 3kV/µs to manage EMI and to minimize ringing. Control is typically achieved via the half-bridge NFETs gate drive series resistors (R1U, R1L in Figure 10 on page 27) and/or RC filters from SW_# to MGND (R3, C3 in Figure 10 on page 27).

The MOSFET drivers provide a pull-down impedance to bias the MOSFETs into the off state if power is lost. The drivers continue to float relative to MGND if power is removed from the LX7720. The SCP logic input enables optional shoot-through protection that prevents the high-side and low-side switches from conducting simultaneously.

15.1 Half-Bridge MOSFET Gate Drive Supplies VGS, VBOOST, and VFLT

The two VGS pins are directly connected to the VGS supply, and power the VEE and VBOOST charge pumps. The four half-bridge VGS supply pins VGS_A, VGS_B, VGS_C, and VGS_D are connected to VGS via individual 1Ω resistors.

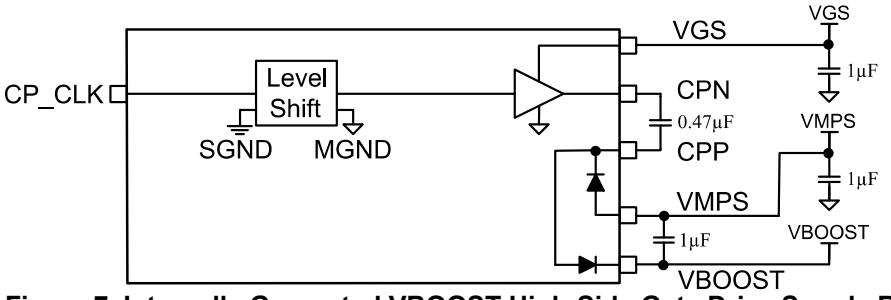


Figure 7. Internally Generated VBOOST High-Side Gate Drive Supply Rail

Decoupling is detailed in Table 1 on page 23. Note that VGS is with respect to motor MGND, not SGND. See section 15.2 on page 29 discussing how VGS pins are interconnected by back-to-back diodes. If a half-bridge stage is unused, its VGS_# pin can either be left open or connected to VGS (Figure 22 on page 33) without needing a decoupling capacitor.

The low-side MOSFET drivers are directly powered from the VGS supply. Each high-side MOSFET driver derives its individual gate drive supply, VFLT_# to SW_#, from VGS. The primary supply for each high-side driver is a bootstrap diode to provide a floating gate drive supply while off and during turn-on. Additionally, a charge pump generates a gate drive supply, VBOOST, which is nominally VGS volts above VMPS. VBOOST maintains the gate supply for high-side MOSFET drivers once they are on. Recommended values for the VBOOST charge pump are given in Table 1 on page 23.

Figure 8 below shows the typical variation in MOSFET driver output impedance with temperature for the half-bridge high side MOSFET driver at UD_#, following the conditions in the Electrical Characteristics table. The upper driver switches UD_# to VFLT_# to turn on the half-bridge high side MOSFET, and the lower driver switches UD_# to SW_# to turn the half-bridge high side MOSFET off. Data for Figure 8 and the following Figure 9 is taken from characterization builds with both 'fast' and 'slow' process corners to show the expected manufacturing spread.

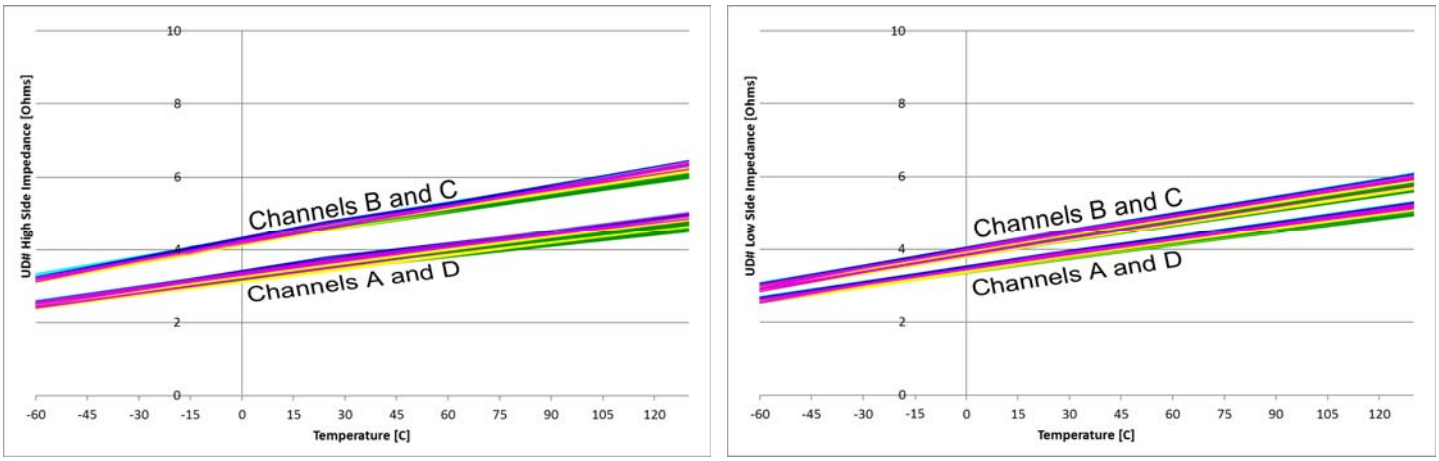


Figure 8. High Side MOSFET Driver Upper (Left) and Lower (Right) Output Impedance

Figure 9 below shows the typical variation in MOSFET driver output impedance with temperature for the half-bridge low side MOSFET driver at LD_#. The upper driver switches LD_# to VGS# to turn on the half-bridge low side MOSFET, and the lower driver switches LD_# to MGND to turn the half-bridge low side MOSFET off.

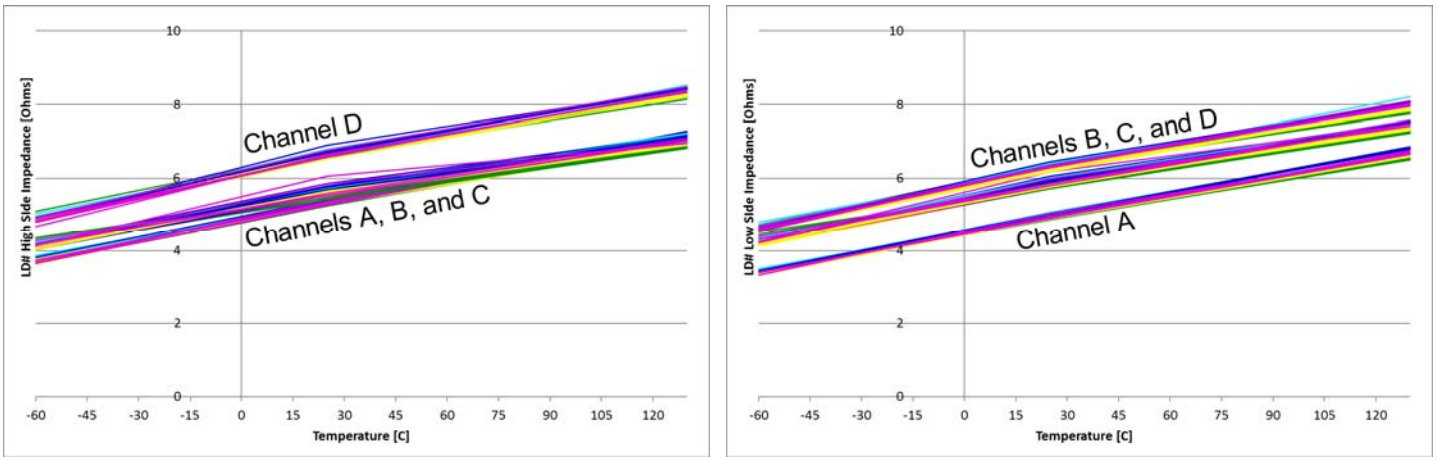


Figure 9. Low Side MOSFET Driver Upper (Left) and Lower (Right) Output Impedance

Figure 10 below shows a typical application circuit for a half-bridge stage. The driver for the high-side MOSFET QU is powered during turn-on by its individual bootstrap supply VFLT_# that follows the QU's source as it slews from MGND to VMPS. The bootstrap supply uses a typically 1µF storage capacitor C2 from VFLT_# to the half-bridge's output, SW_#. C2 charges up through diode DFLT from the gate supply VGS_# to VFLT_#. The path to MGND is either through an attached grounded load winding, or through the low-side MOSFET when on. When the half-bridge is operating as a PWM output, this bootstrap supply maintains a VFLT_# voltage at a little less than (VGS + $V_{SW\_\#}$), stored by capacitor C2. C2 charges when LD_IN_# = 1, and discharges otherwise.

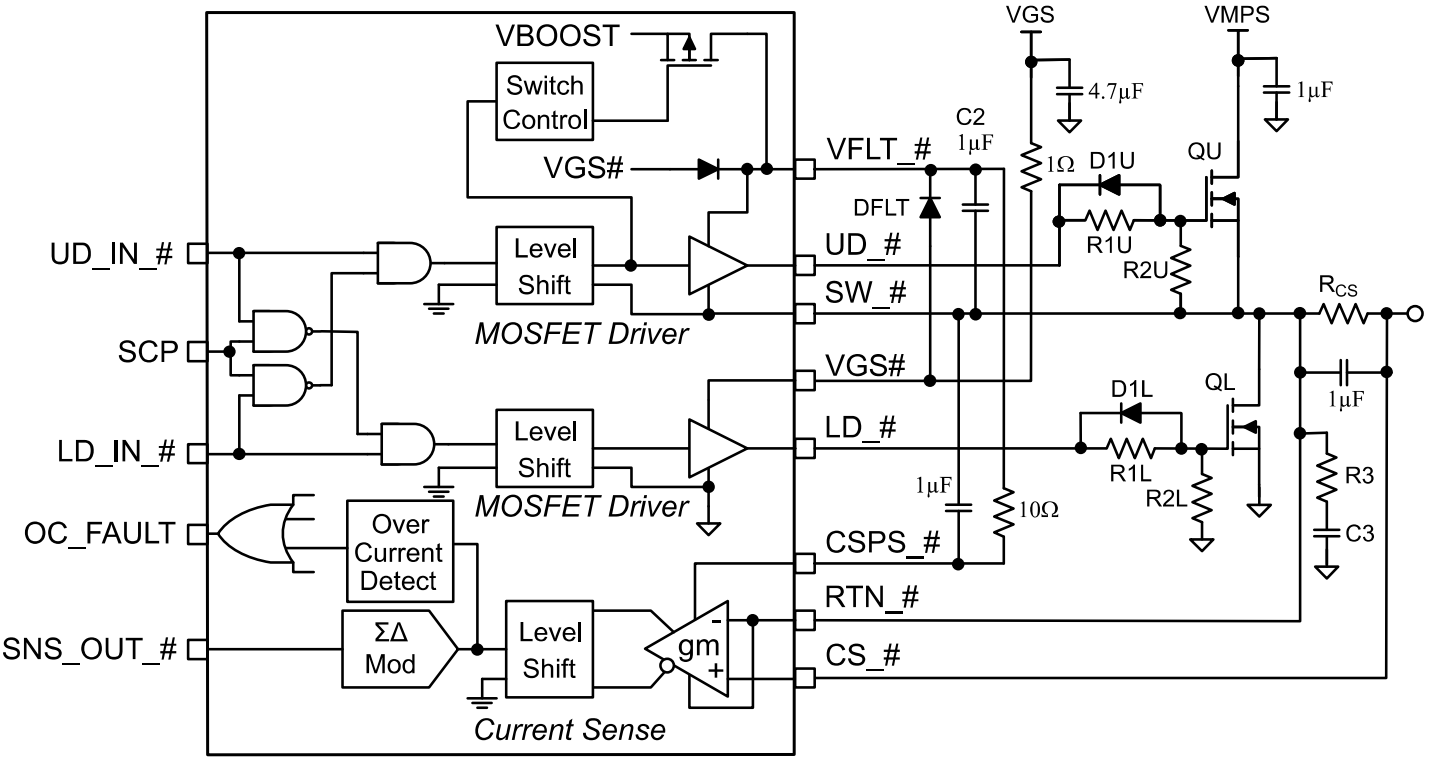


Figure 10. Typical Application Circuit One of Four Half-Bridge Stages

The external bootstrap diodes, DFLT, are in parallel with internal bootstrap diodes. The internal diodes have relatively slow reverse recovery time (t_{rr} = 600ns) and limited power rating (120mW). Applications with relatively low switching speeds and VMPS voltage could use the internal diodes alone. Be sure to confirm that the diode forward current and dissipation (during both forward conduction and reverse recovery) are within ratings. In general, it is recommended to use

external parallel DFLT diodes, such as the JANS qualified ultrafast (t_{rr} = 30ns) 1N5809US. Schottky diodes such as JANS1N6864US are suitable too, but exhibit higher reverse leakage at elevated temperatures.

The initial charging current for the bootstrap capacitor C2 on VFLT is limited by a recommended 1Ω resistor shown in Figure 10 to protect the internal bootstrap diode. Capacitor C2 charges up when the SW pin goes to MGND, thus when the lower FET is on. Including the series 1Ω isn't necessary if either the parallel diode DFLT is used. Alternative approaches to reduce the peak initial current are:

1. Implement a soft start procedure after power-up to manage the charging slope for the charge pump capacitors. A typical procedure is to modulate the low side drivers (LD_IN_#) building up from a low duty up to 100%. An example sequence is to ramp a 10kHz 8-bit PWM from 1/256 duty to 256/256 duty over 256 periods. The initial on-time is 390ns, and the complete sequence takes 25.6ms
2. At the end of a motor drive session, leave the low side drivers on (LD_IN_# = 1) to maintain the voltage on the charge pump capacitors. Subsequent motor drive sessions will therefore not need the soft start procedure

The 10V LX7720 VGS supply minimum is too high for many low threshold MOSFETs and enhancement mode GaN FETs. Figure 11 below shows a Zener clamp (D2) being used to limit the gate voltage at the MOSFET. The series resistor R1 limits the current through the Zener diode when the MOSFET is switched on, per Equation 2 below. Per the LX7720 Operating Ratings, the limit for each FET driver's average source/sink current is 25mA.

$$I_{SOURCE} = \frac{VGS - V_{ZENER}}{R1}.$$

Equation 1. Continuous Gate Driver Source Current Using Zener Clamp

For example, a 4.3V Zener diode may be chosen for MOSFETs with VGS(max)=6V. Setting R1=470Ω limits the continuous current when a FET driver is high to under 16mA, using a 12V VGS supply. The 470Ω series resistor will also slow down the MOSFET turn-on time due to gate capacitance. An optional speed-up capacitor C1 in parallel with R1 can be used to help balance the NFET's gate-charge and speed up the NFET's initial turn-on to the Miller plateau. The balancing speed-up capacitance, C1, is set per Equation 2, where Q_g is the NFET's specified typical gate-source charge in nC. Diode D1 ensures a fast turn-off by providing a low resistance path when the gate driver output falls.

$$C1 = \frac{12nC}{12V} = 1nF.$$

Equation 2. Speed-Up Capacitor Balancing Gate Capacitance

For example, using MOSFETs with a 12nC gate-source charge and a 12V VGS supply gives C1 = 12nC / 12V = 1nF.

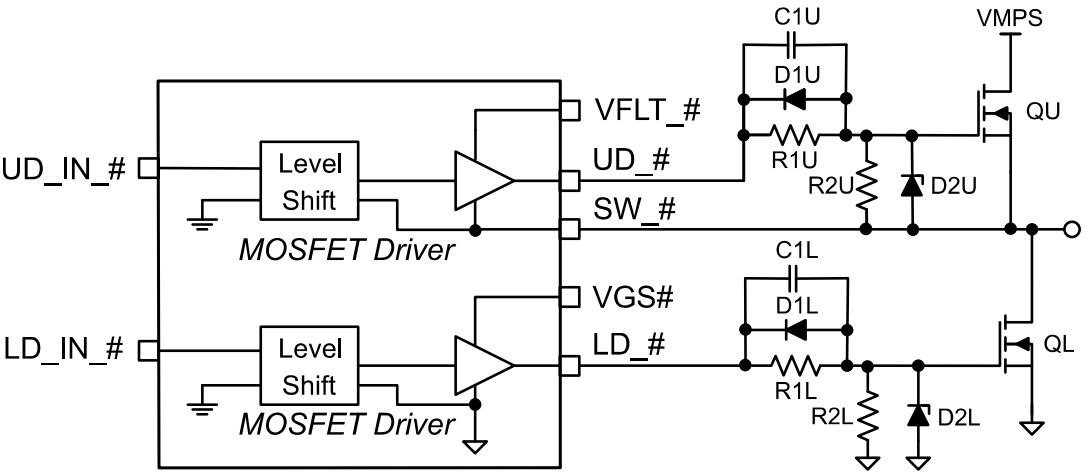


Figure 11. Half-Bridge Stage Using Low Gate-Voltage MOSFETs

Figure 12 on page 29 shows the typical variation in MOSFET driver propagation delay with temperature for the half-bridge high side MOSFET driver at UD_#, following the conditions in the Electrical Characteristics table. The left curves show the propagation delay from logic input UD_IN_# rising (L→H) to the upper MOSFET driver switching UD_# from SW_# to VFLT_# to turn on the half-bridge high side MOSFET. The right curves show the propagation delay from logic input UD_IN_# falling (H→L) to the upper MOSFET driver switching UD_# from VFLT_# to SW_# to turn off the half-bridge high side MOSFET.

Figure 13 below shows the typical variation in MOSFET driver propagation delay with temperature for the half-bridge low side MOSFET driver at LD_#. The left curves show the propagation delay from logic input LD_IN_# rising (L→H) to the lower MOSFET driver switching LD_# from MGND to VGS_# to turn on the half-bridge low side MOSFET. The right curves show the propagation delay from logic input LD_IN_# falling (H→L) to the lower MOSFET driver switching LD_# from VGS_# to MGND to turn off the half-bridge low side MOSFET. Data for Figure 12 and Figure 13 is taken from characterization builds with both 'fast' and 'slow' process corners to show the expected manufacturing spread.

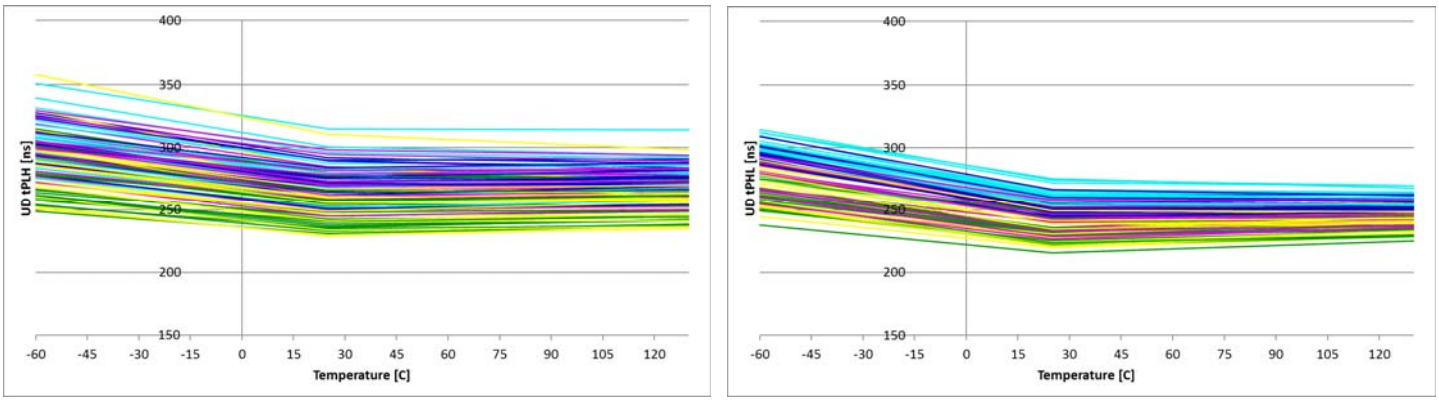


Figure 12. High Side MOSFET Driver Low-to-High (Left) and High-to-Low (Right) Propagation Delays

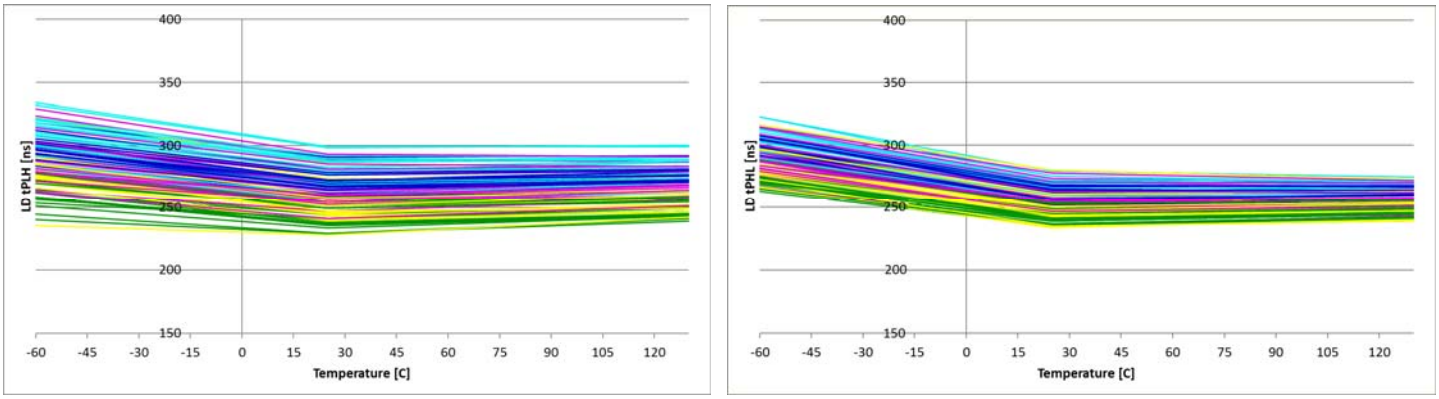


Figure 13. Low Side MOSFET Driver Low-to-High (Left) and High-to-Low (Right) Propagation Delays

15.2 VGS Supply Pin Interconnections

The 6 VGS supply pins are not interconnected by metal internally, to provide a degree of isolation between sections drawing impulse currents. The pins are, however, interconnected radially by back-to-back diodes (Figure 14 below) to constrain transient voltage differences between pin voltages. The under-voltage lockout detector monitors the voltage on only pin 85 (ceramic), pin 103 (plastic). If a half-bridge is unused, it's VGS pin (VGSA, VGSB, VGSC, or VGSD) can be left floating. However, since any unused half-bridge's VGS pin will be powered anyway via back-to-back diodes, suggested practice is to connect it to the VGS supply, and simply omit the decoupling capacitor for that pin.

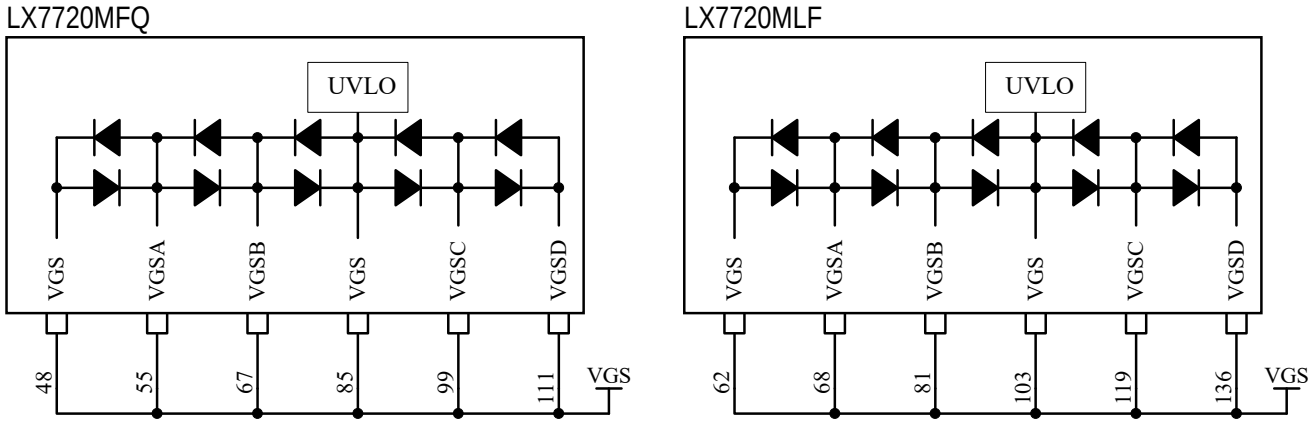


Figure 14. VGS Supply Pins, Ceramic Package (left) and Plastic Package (right)

16 Sigma-Delta ADCs

The 7 ADCs in the LX7720 (4 for motor phase current, 3 for LVDT/resolver primary and secondary voltages) are independent 2nd order sigma delta (Σ-Δ) modulators operating simultaneously. The LX7720 only provides the modulation portion of a complete sigma delta conversion, and outputs a PDM (pulse-density modulated) output data stream for each ADC channel (SNS_OUT_A, SNS_OUT_B, SNS_OUT_C, SNS_OUT_D, ADC1, ADC2, ADC3). The modulator sample rate is the externally provided Σ-Δ modulator clock, MOD_CLK, in the range 24MHz to 32MHz. The 7 PDM outputs are synchronized to the clock at the CLK_OUT pin, which is MOD_CLK plus internal delays.

The density of the pulses (proportion of 1s) within each PDM stream corresponds to the analog signal's amplitude. All 7 ADC inputs are bipolar, so continuous 0s indicates negative full scale (or lower), and continuous 1s indicates positive full scale (or higher). A matching density of 0s and 1s indicates zero input. Feeding a PDM stream into an analog low pass filter gives an output of VDD (the logic supply voltage) for positive full scale, VDD/2 for zero, and 0V for negative full scale.

The host FPGA or MCU performs sinc³ filtering and decimation of the PDM bit streams. The sinc³ filtering moves noise out of band, and the choice of oversampling ratio (OSR) trades latency through the filter against SNR and therefore effective resolution (Figure 15 below). IP documentation for Microchip's radiation hardened FPGAs is available here. Example code for the Microchip's SAMRH family of radiation hardened MCUs is available here.

The four current sense Σ-Δ modulators have a linear working range of ±250mV, and PDM output streams (SNS_OUT_A, SNS_OUT_B, SNS_OUT_C, and SNS_OUT_D) as follows:

- The Σ-Δ bit stream is high for full scale positive current sense voltage where V_{CS} - V_{RTN} = +350mV typically
- The Σ-Δ bit stream is low for full scale negative current sense voltage where V_{CS} - V_{RTN} = -350mV typically
- A zero current sense voltage will produce a bit stream that's 50% high, 50% low on average

The delay from a moderate to large step in current sense voltage (-50mV to +50mV, or -250mV to +250mV) to seeing a change in the corresponding modulator output is typically 800ns (MOD_CLK=32MHz), and settling within typically 2µs.

A current sense Σ-Δ modulator will enter sleep mode if the logic inputs UD_IN_# and LD_IN_# to its associated half-bridge driver are both logic low for more than 8192 MOD_CLK cycles.

The three LVDT/resolver Σ-Δ modulators have a linear working range of ±800mV, and PDM output streams (ADC1, ADC2, and ADC3) as follows:

- The Σ-Δ bit stream is high for full scale positive voltage where $V_{ADC\#\_P}$ - $V_{ADC\#\_N}$ = +1400mV typically
- The Σ-Δ bit stream is low for full scale negative voltage where $V_{ADC\#\_P}$ - $V_{ADC\#\_N}$ = -1400mV typically
- A zero voltage will produce a bit stream that's 50% high, 50% low on average

An ADC# Σ-Δ modulator will enter sleep mode if ADC#_P and ADC#_N are both held to VCC for more than 8192 MOD_CLK cycles.

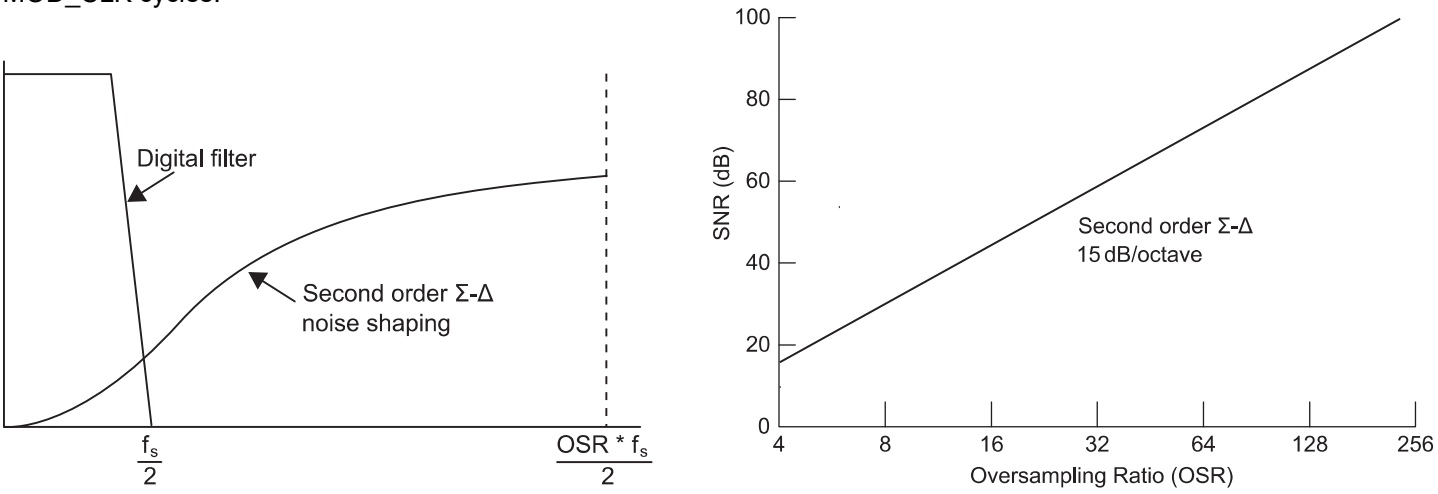


Figure 15. Noise Shaping in 2nd order Σ-Δ modulator, and Ideal SNR with sinc³ Filtering and Decimation

17 Resolver/LVDT Interface

The resolver interface consists of a differential driver output DMOD_OUT_P and DMOD_OUT_N to drive a resolver or LVDT primary, plus three differential analog acquisition inputs ADC1, ADC2, and ADC3.

17.1 Resolver/LVDT Primary Drive

The DMOD_OUT_P and DMOD_OUT_N outputs are half-bridge drivers normally used together to form a full-bridge differential driver to a resolver/LVDT primary winding. The corresponding logic inputs are DMOD_IN_P and DMOD_IN_N. If both DMOD_IN_P and DMOD_IN_N remain low for more than 65536 MOD_CLK cycles, the DMOD_OUT_P and DMOD_OUT_N outputs both go high impedance.

The DMOD_OUT_P and DMOD_OUT_N output drivers are powered from a separate rail, DMOD_PS. DMOD_PS is typically the same voltage as VGS. Like VGS, the DMOD_PS rail is referenced to MGND. Tie DMOD_PS to MGND if DMOD_OUT_P and DMOD_OUT_N are unused. The driver bias current can be reduced by grounding the DMOD_BW input, which also slightly reduces the maximum pulse rate of the driver.

A resolver/LVDT primary is typically driven with a sinusoidal voltage with a frequency of a few kHz. The usual drive method is to synthesize the sine waveform using PWM modulation up to 1MHz at the DEMOD_IN_P and DEMOD_IN_N inputs. The DMOD_OUT_P and DMOD_OUT_N full-bridge output is typically L-C filtered similar to a class-D audio signal before feeding the resolver/LVDT primary to remove the PWM modulation carrier.

17.2 ADC1-3 and Resolver/LVDT Secondaries Signal Acquisition

ADC1 and ADC2 are typically used to sense the two secondary output voltages. A decimation ratio of 64 to 256 provides accuracies from 10 to 14 bits. ADC3 is typically used to sense the primary drive voltage (after the L-C filtering). This can be used to calibrate amplitude or fine-tune the sinewave envelope by pre-distorting the waveform synthesis PWM values.

The ADC1, ADC2, and ADC3 differential inputs are referred to SGND and have a common mode input range from 0.5V to VCC - 2.1V. Since the resolver/LVDT primary drive is with respect to MGND, primary drive signal monitoring will typically be AC coupled to ADC3's differential inputs to cross the MGND-SGND ground domains. The resolver/LVDT secondaries are floating, and so can be referred to the SGND ground domain. One way to manage the biasing is to generate a nominal 1.7V rail to SGND (mid common mode input range), and use this as the reference for the signal conditioning networks. Figure 16 below shows an example conditioning network for an AMCI R11X-A10/7 resolver.

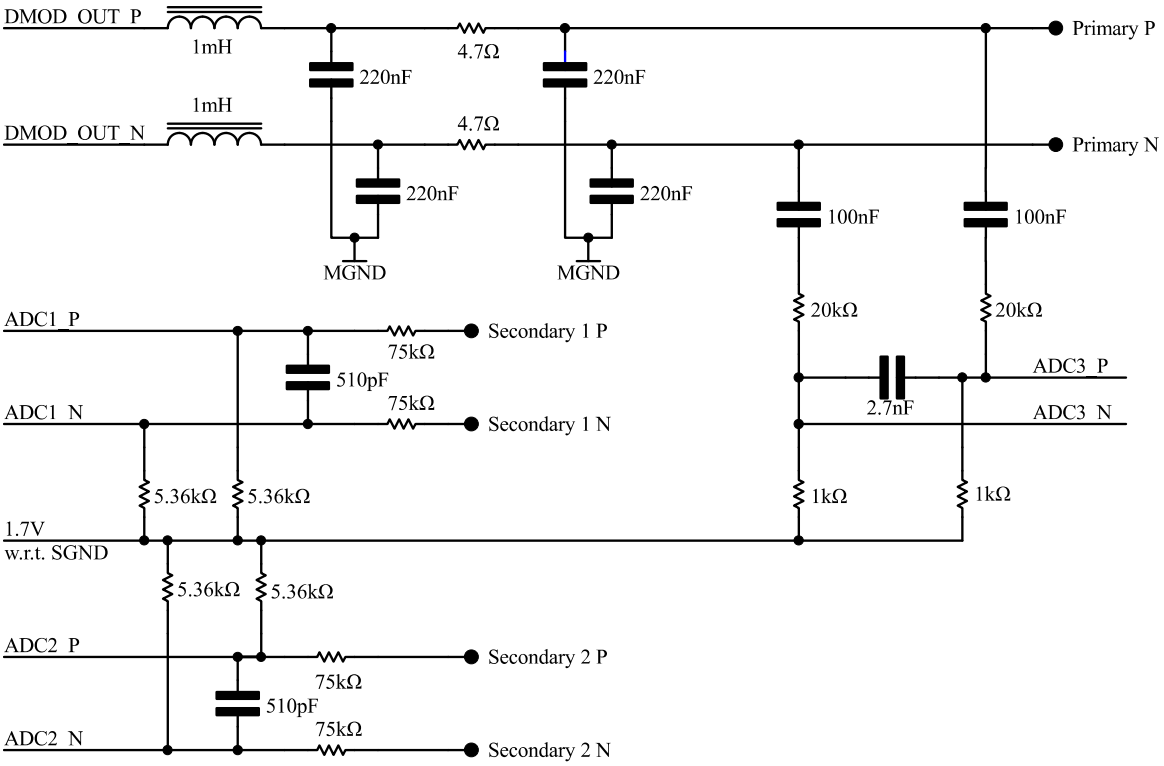


Figure 16. Resolver ADC Input Biasing and Filtering Example

18 Floating Current Sense

Each current sense amplifier has an independent supply rail, CSPS_#, with the same 10V to 18V allowed voltage range as the VGS gate drive supply. Figure 17 below shows the current sense block, with RC decoupling for the supply pin, CSPS_#, and the current sense resistor, R_{CS}. An optional capacitor across R_{CS} filters very fast current transients during commutation. The RTN_# pin is both the inverting current sense input and the current sense amplifier's supply ground.

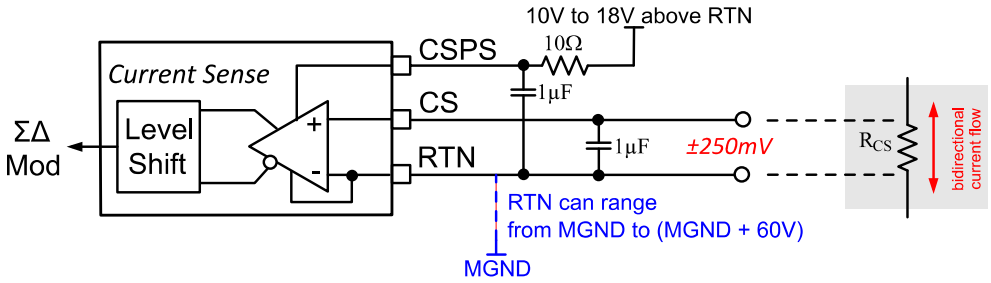


Figure 17. Current Sense Amplifier Topology

Current sensing is usually configured in a half-bridge output to a motor winding, as shown in Figure 10 on page 27. The common mode voltage at the current sense resistor is either at about MGND (when the low-side half-bridge FET is switched on), at about VMPS (when the high-side half-bridge FET is switched on), or transitioning between the two. The CSPS supply used is the high-side gate driver's VFLT supply, which is always about VGS above the half-bridge output.

Current sensing can also be configured in either a load's ground return (low-side sensing), a load's supply (high-side sensing), or a half-bridge output to a motor winding. Figure 18 on page 32 shows a typical connection for low-side current sensing. The CSPS supply is shown as VGS, but it can be an independent supply instead. Figure 19 on page 32 shows a typical connection for high-side current sensing. Here, the CSPS supply is shown as the VBOOST charge pump output, which is at VMPS + VGS, unloaded. Since VBOOST is with respect to the VMPS motor supply, using VBOOST means that the high-side current sensing must also be with respect to VMPS.

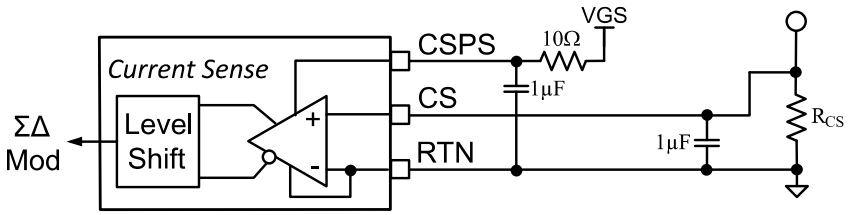


Figure 18. Low-Side Current Sensing

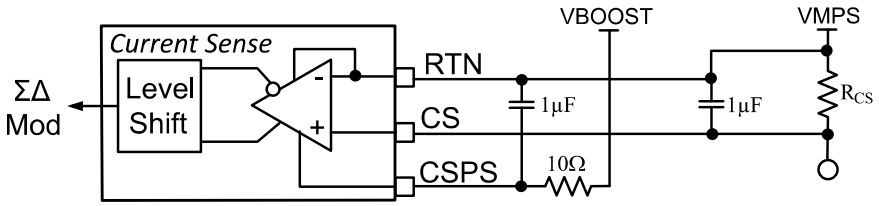


Figure 19. High-Side Current Sensing

If half-bridge output current measurement is used, it is recommended to apply a median filter to the output of the current sense sinc³ filter (Figure 20 below) before the data is used by the motor control algorithm. The median filter rejects artifacts in the current sense Σ-Δ modulator output pulse train due to transitions at the SW_# pin. An *n* order median filter is a rolling or sliding window filter which sorts the most recent *n* samples and outputs the value of the median sample.

OSR	Median Order *n*
16	13
32	9
64	7
128	5
256	3

Figure 20. Median Filter Recommendation

19 Connections to Common Motor Types

19.1 3-phase BLDC or PMSM

Figure 21 below shows the common way to drive a 3-phase brushless DC or permanent magnet synchronous motor. Supplies are shown at the simplest level without the necessary decoupling. The differential current sensing in the three phase drives can be simplified to two windings only, and the current calculated for the third winding as the sum of the other two windings' currents, observing polarity.

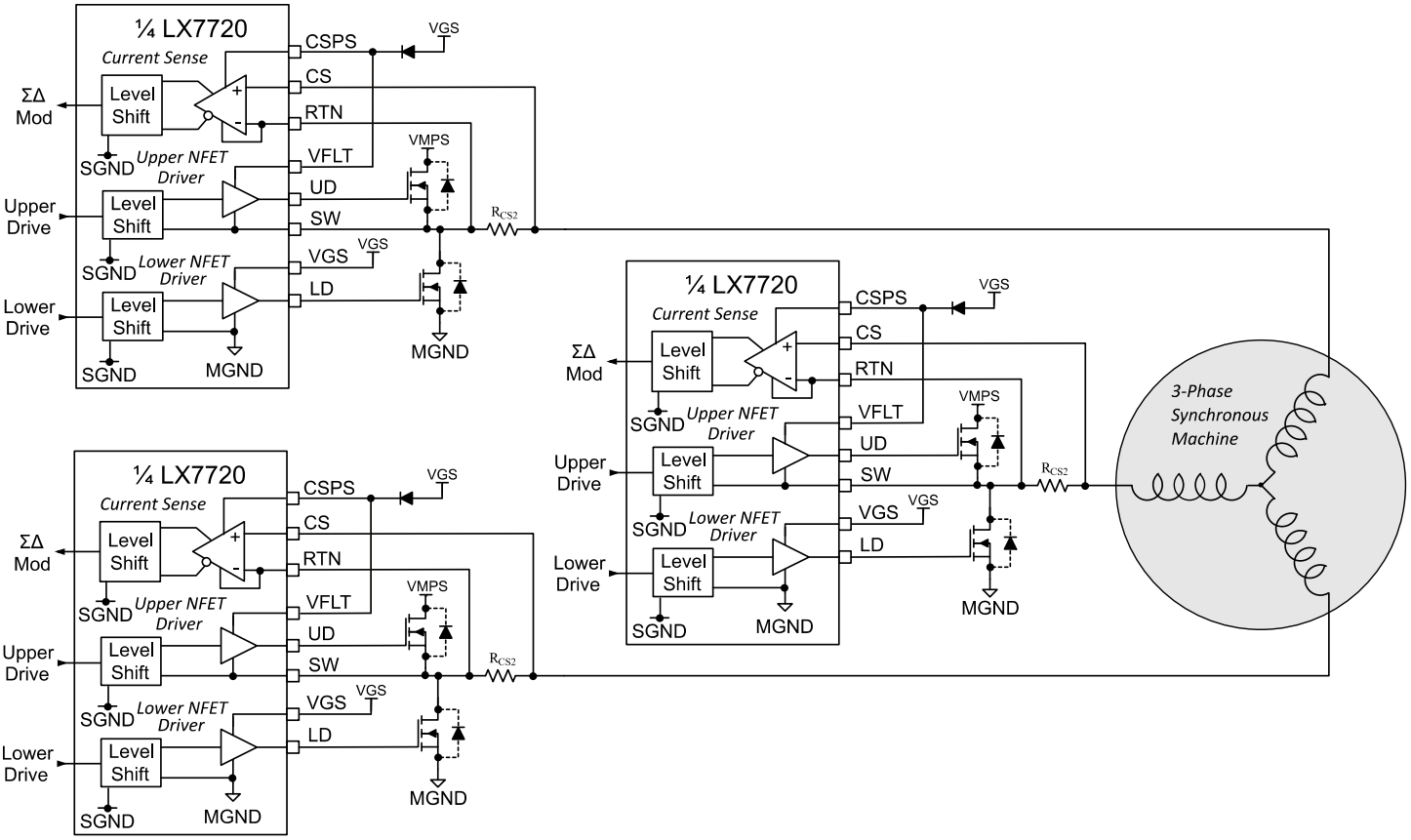


Figure 21. Three-Phase Motor Driver with Phase Output Current Sensing

19.2 Disabling an Unused Half-Bridge

If a half-bridge stage is not going to be used, such as a 3-phase motor application, then the high-side and/or low-side driver can be disabled as shown in Figure 22 below. An unused half-bridge stage's VGS_# pin can either be connected to VGS, as shown below, or left open. VGS pins are internally interconnected to their neighboring VGS pins through diodes.

Each half-bridge stage's current sense amplifier enters power saving sleep mode if neither FET driver is turned on for 8192 MOD_CLK cycles. The left hand circuit below ties the lower driver input high to allow the current sense circuit to be used. The right hand circuit ties both driver inputs low, allowing the current sense circuit to enter sleep mode.

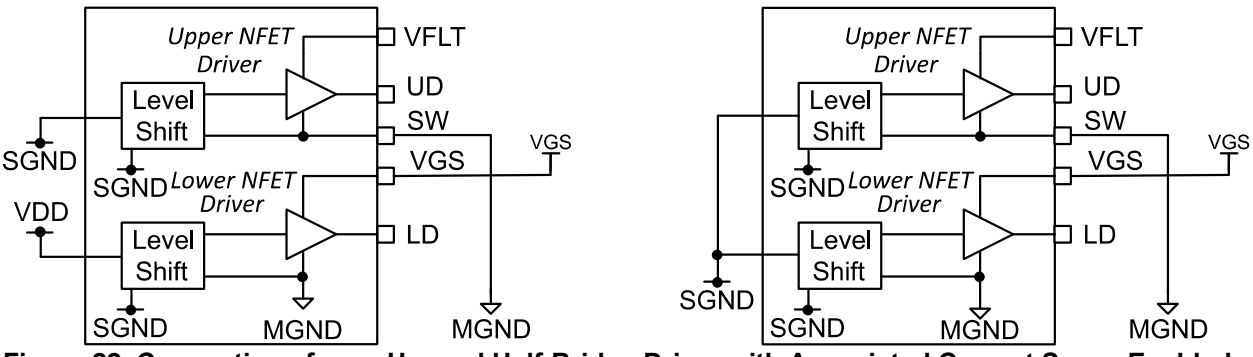


Figure 22. Connections for an Unused Half-Bridge Driver with Associated Current Sense Enabled or Disabled

Although Figure 22 shows the high-side and low-side drivers being disabled together, either or both drivers may be used independently. However, all drivers must use the same VGS supply, and the high-side driver can only be used to switch a load connected to VMPS, since the VBOOST high side gate supply is also common to all drivers and is relative to VMPS.

Figure 23 below shows how to wire the inputs to an unused current sense amplifier.

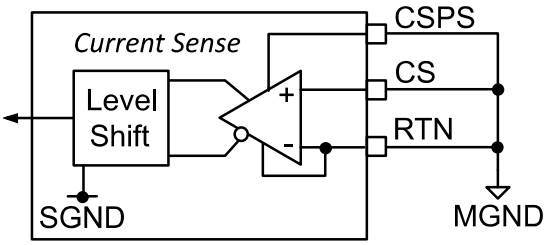


Figure 23. Connections for an Unused Current Sense Amplifier

19.3 2-Phase Bipolar Stepper Motor

Each winding in a bipolar stepper motor is driven by a full-bridge, comprising two half-bridges feeding into a common current sense. The current sensing shown in Figure 24 below is low-side sensing (Figure 18 on page 32), but high-side or half-bridge output sensing could be used instead. Only one current sense circuit is needed per winding.

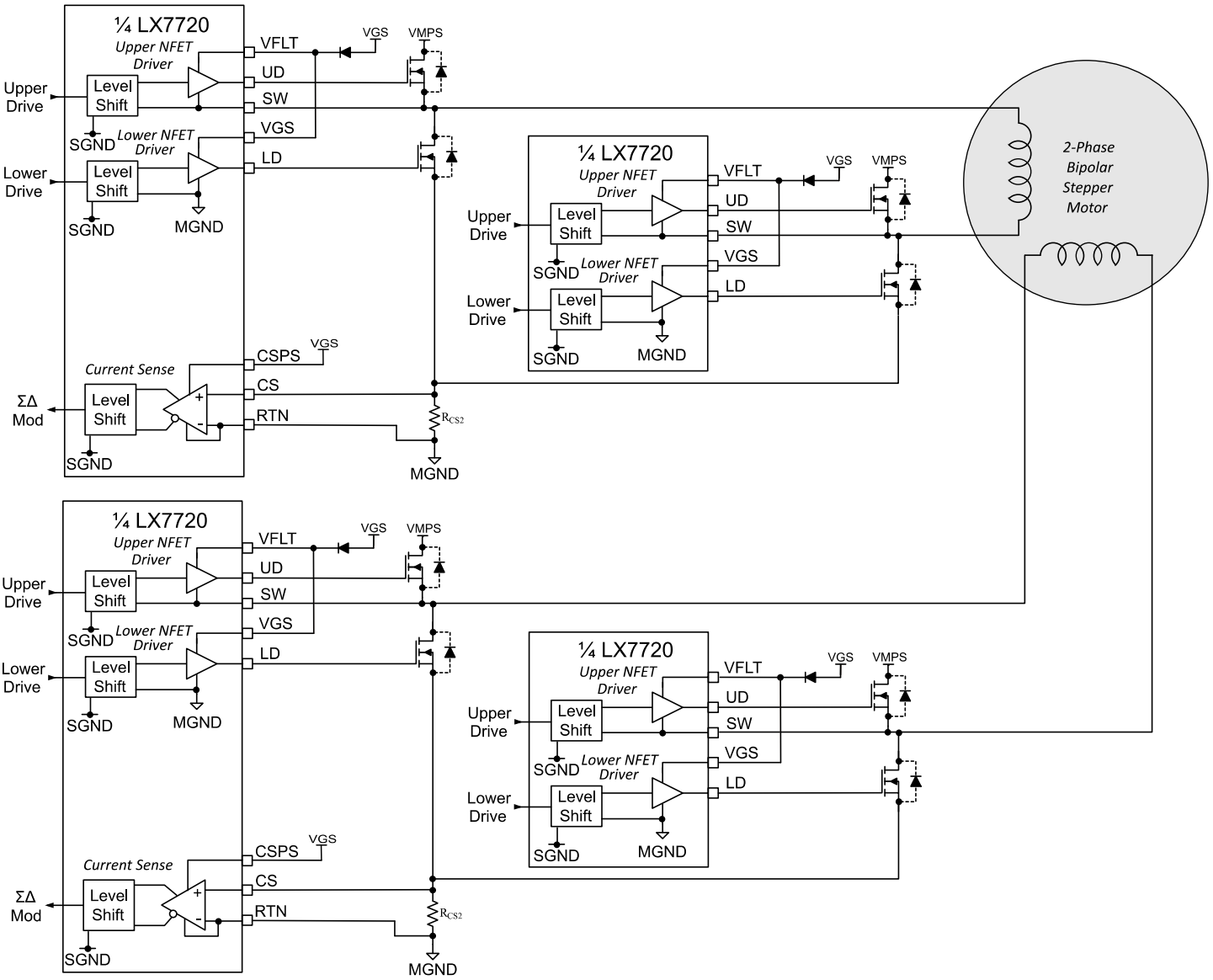


Figure 24. Two-Phase Bipolar Stepper Motor Driver with Ground-Side Current Sensing

19.4 2-Phase Unipolar Stepper Motor

Figure 25 below shows a 2-phase unipolar stepper motor being driven by four low-side drivers operating in pairs. Again, supplies are shown at the simplest level without the necessary decoupling. Each low-side driver pair has current sensing in one of its half-bridge outputs. Since only one half of each unipolar winding is powered at a time, only one current sense circuit is needed per winding.

The motor windings' center-taps are connected to the motor supply, VMOTOR. Since VMOTOR has no connection to the LX7720, this voltage can be different to the LX7720's VMPS motor supply, if desired.

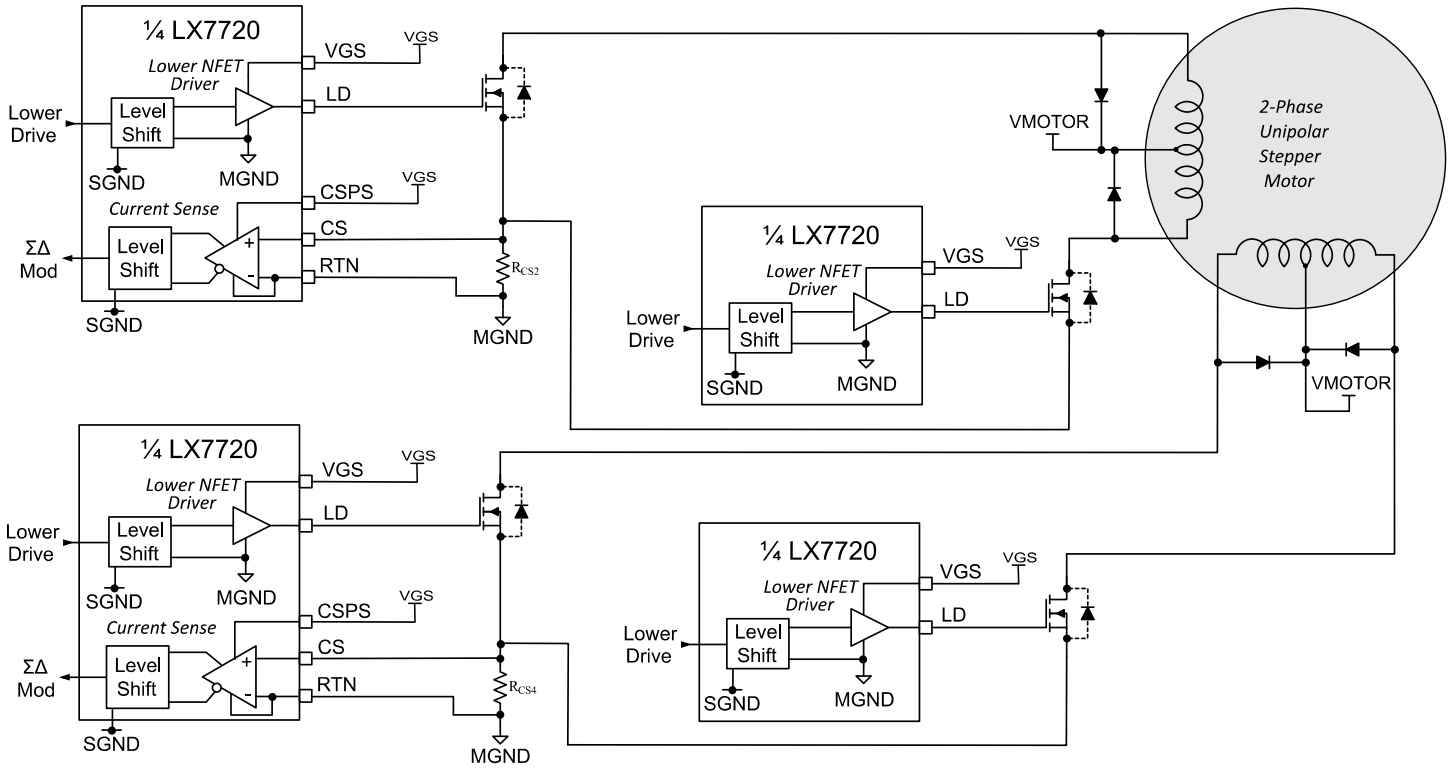


Figure 25. Two-Phase Unipolar Stepper Motor Driver With Ground Current Sensing

Figure 26 on page 36 shows the alternative configuration for a 2-phase unipolar stepper motor, now being driven by four high-side drivers instead of low-side drivers. The motor supply must be the LX7720's normal 20V to 60V VMPS motor supply since the VBOOST high side gate supply is relative to VMPS. Each high-side driver pair has current sensing in one of its half-bridge outputs. Since only one half of each unipolar winding is powered at a time, only one current sense circuit is needed per winding.

The LX7720 contains four half-bridge driver stages and four current sense amplifiers, which is enough to drive two 2-phase unipolar stepper motors with full current sensing. One motor uses the four high-side drivers and two current sense amplifiers, and is limited to the 20V to 60V VMPS range for the motor supply. The other motor uses the four low-side drivers and the two remaining current sense amplifiers, with no constraint on motor supply voltage. Since each motor is using half of each half-bridge, all four current sense amplifiers will be active (not in sleep mode) when either motor is being operated, and all four amplifiers will enter sleep mode after both motors are stopped (all FET drivers off) for 8192 MOD_CLK cycles.

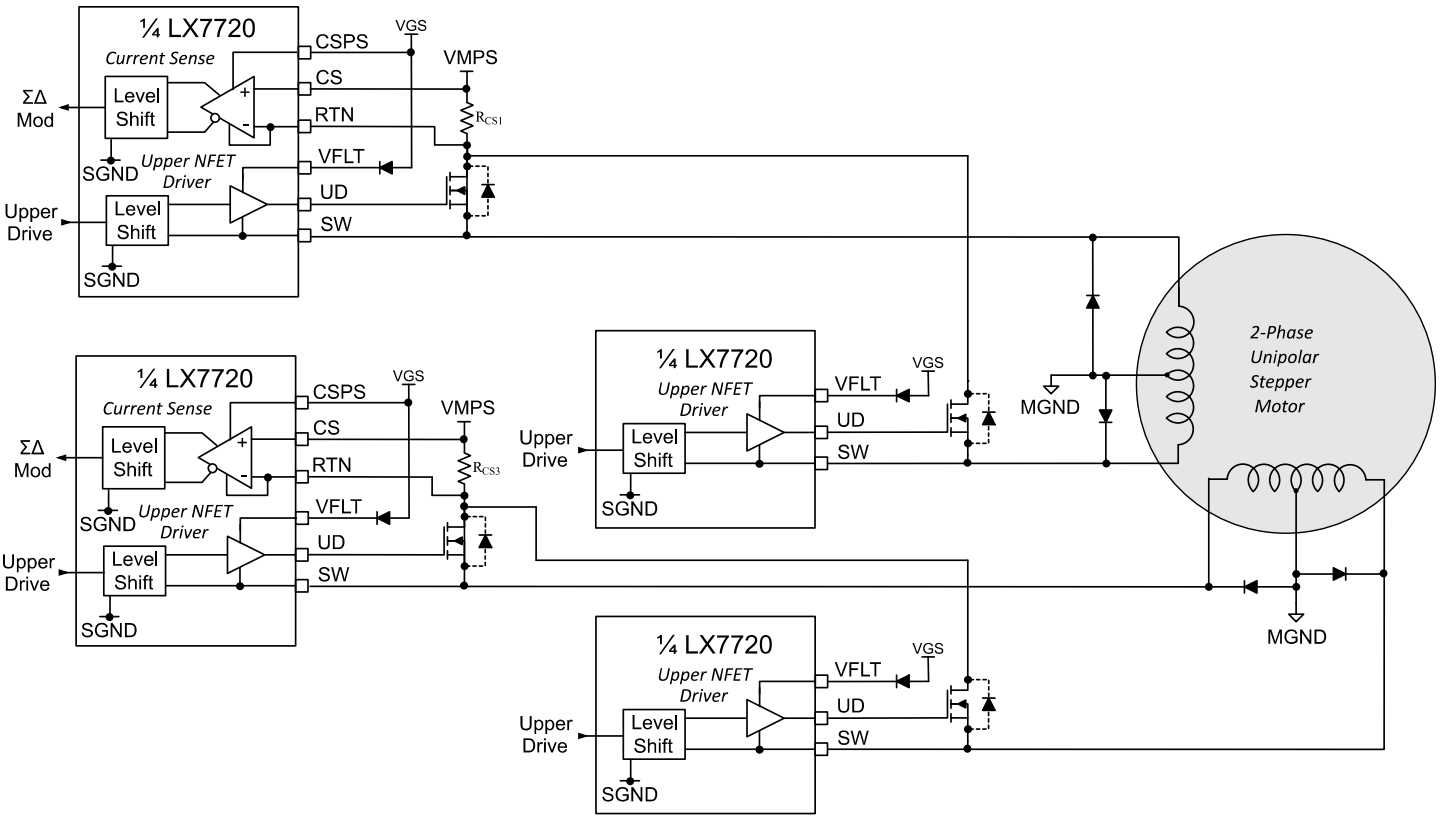


Figure 26. Two-Phase Unipolar Stepper Motor Driver with Supply Current Sensing

20 Bi-Level Comparators - Hall Effect Sensors and Encoders

The bi-level comparators comprise 6 comparators with non-inverting inputs at pins BLI1 to BLI6, and logic outputs at pins BLO1 to BLO6. The 6 inverting inputs share a common rising-input trip threshold at the BL_TH pin. Bias BL_TH between 0.5V and 4.5V. The hysteresis is typically 150mV on falling edges. Low pass input filters and threshold hysteresis provides high frequency noise rejection. The bi-level inputs are cold spared.

The bi-level comparators just require VCC and VDD to operate. However, if Safe Mode is enabled (SM_EN logic input is either logic high or open), then the BLO outputs are forced low for the duration of a MOD_CLK failure (section 22.2 on page 37). A MOD_CLK failure when Safe Mode is enabled will also latch the PR_FAULT output high, but the BLO functionality is restored when MOD_CLK is restored, independent of PR_FAULT output status or RESET input. level.

21 FPGA/MCU Controller Interface

I/O logic levels are set by the voltage at the VDD logic supply pin, in the range 2.1V to 5.5V. Logic input pins have an internal 1MΩ pull down resistor to ground. If the system FPGA or MCU is powered up before the LX7720's VDD supply, then its control outputs should be either logic low or high impedance. Logic output resistance is typically 300Ω (low) and 600Ω (high) with VDD=3.3V. The recommended maximum DC load current for logic outputs is ±8mA.

21.1 Interfacing 1.8V Logic

The LX7720 can interface 1.8V logic by providing a toleranced VDD supply meeting 2.1V minimum. For example, a 2.165V ±3% ranges from 2.1V to 2.23V. The maximum input threshold for the LX7720 logic inputs is 70% of VDD, so 2.23V x 0.7 = 1.56V in this example. This is capable of operation from 1.8V logic outputs. For the LX7720's logic outputs, no special consideration is required for controller inputs that are over-voltage tolerant to at least 2.23V. Otherwise each LX7720 logic output voltage will have to be reduced with a resistive divider to meet the controller's 1.8V limit.

22 Fault Detection and Fault Management

The LX7720 detects a variety of supply voltage and drive over-current faults, die over-temperature, and MOD_CLK failure. Fault status is provided on the PR_FAULT, OC_FAULT, and OTW_FAULT logic outputs.

The optional Safe Mode causes certain detected faults to latch the LX7720 into a safe operating condition, which can be cleared by toggling the RESET logic input. RESET is only active when Safe Mode is enabled. When Safe Mode is disabled, faults are not latched and fault status outputs clear automatically once the fault situation is resolved. Safe Mode is enabled when the SM_EN logic input is either logic high or open.

If Safe Mode is not enabled, the LX7720 will rely exclusively on the system FPGA or MCU to manage fault mitigation such as shutting off the external MOSFETs or disconnecting a power rail.

Safe Mode, if enabled, is only activated after power-up once the LX7720's VCC, VGS, VDD, and VEE power rails have passed their under-voltage (UVLO) thresholds. This avoids latching a PR_FAULT during normal supply sequencing. However the PR_FAULT output will still alert any lack of rail(s) during power-up. The VMPS motor supply is not monitored, but if it rises once Safe Mode has activated then it may trigger a PR_FAULT unless its slew rate is slow. This can be cleared by toggling RESET, or the issue avoided by ensuring that VMPS is not the last rail to be sequenced.

22.1 Power Rail Faults

The PR_FAULT logic output goes high to indicate that one or more of the VCC, VGS, VDD, and VEE voltage rails has fallen below its UVLO threshold levels specified in the electrical characteristics table. If VEE is generated by the internal charge pump operating from VGS ($\overline{\text{EXT\_VEE\_EN}}$ pin tied to VGS), then a failure (stuck high or low) of the external CP_CLK charge pump clock will show as a PR_FAULT when VEE collapses.

If Safe Mode is enabled (SM_EN logic input is logic high or open), then for a VCC, VGS, VDD, or VEE power rail fault:

- PR_FAULT is latched high
  - If the VDD logic supply fails then a logic high cannot be signaled. When VDD recovers, PR_FAULT will be high
- The DMOD_OUT_N and DMOD_OUT_P resolver/LVDT drivers and all half-bridge MOSFETs are turned off
- PR_FAULT is cleared low (once the supply fault situation is resolved) by either an active-high level on the RESET logic input or by disabling Safe Mode

If Safe Mode is disabled (SM_EN logic input is logic low), then for a VCC, VGS, VDD, or VEE power rail fault:

- PR_FAULT remains high for the duration of the under-voltage detection event(s)
- The DMOD_OUT_N and DMOD_OUT_P resolver/LVDT drivers are turned off
- The half-bridge MOSFETs are turned off for VCC, VGS, and/or VDD power rail faults, but not for solely a VEE power rail fault

22.2 MOD_CLK Failure

If Safe Mode is enabled, then a failure (stuck high or low) of the external Σ-Δ modulator clock, MOD_CLK, for longer than typically 200ns will cause the following actions:

- PR_FAULT is latched high
- The DMOD_OUT_N and DMOD_OUT_P resolver/LVDT drivers and all half-bridge MOSFETs are turned off
- The LX7720 enters a low power state with both the VEE and VBOOST charge pumps disabled and the BLO outputs forced low
- The LX7720 exits the low power state (with the VEE and VBOOST charge pumps restarted, and BLO outputs restored) as soon as MOD_CLK is restored, independent of the status of the PR_FAULT output and RESET input.
- PR_FAULT is cleared low (once MOD_CLK is restored) by either an active-high level on the RESET logic input or by disabling Safe Mode.

After power-up with Safe Mode enabled, the initial lack of a MOD_CLK signal will cause PR_FAULT to go high temporarily until MOD_CLK appears. After that, any further MOD_CLK faults will be latched as described above.

22.3 Over-Current Detection in the Current Sense Amplifiers

The OC_FAULT logic output goes high to indicate over-current detection in one or more of the four floating current sense circuits. The current sense detection circuitry trips at typically ±320mV across a current sense resistor. A low pass filter prevents short duration spikes (under typically 15µs) from triggering over-current detection.

If Safe Mode is enabled, then for an over-current fault:
- OC_FAULT is latched high
- All half-bridge MOSFETs are turned off
  - The DMOD_OUT_N and DMOD_OUT_P resolver/LVDT drivers are unaffected
- OC_FAULT is cleared low (once the fault situation is resolved) by either an active-high level on the RESET logic input or by disabling Safe Mode

If Safe Mode is disabled, then for an over-current fault:
- OC_FAULT remains high for the duration of over-current detection
- No other action is taken

22.4 Overload Detection in the Half-Bridge MOSFET Drivers or Resolver/LVDT Drivers

The half-bridge MOSFET drivers set the PR_FAULT logic output if the average supply current drawn from any of VGS_A, VGS_B, VGS_C, or VGS_D exceeds the fault threshold and fault blanking time given in the electrical characteristics table.

The full-bridge driver outputs DMOD_OUT_N and DMOD_OUT_P set the PR_FAULT logic output if the average supply current from DMOD_PS exceeds the fault threshold and fault blanking time given in the electrical characteristics table.

If Safe Mode is enabled, then for an overload fault:
- PR_FAULT is latched high
- The DMOD_OUT_N and DMOD_OUT_P resolver/LVDT drivers and all half-bridge MOSFETs are turned off
- PR_FAULT is cleared low (once the fault situation is resolved) by an active-high level on the RESET logic input or by disabling Safe Mode

If Safe Mode is disabled, then for an overload fault:
- PR_FAULT remains high for the duration of over-current detection
- No other action is taken

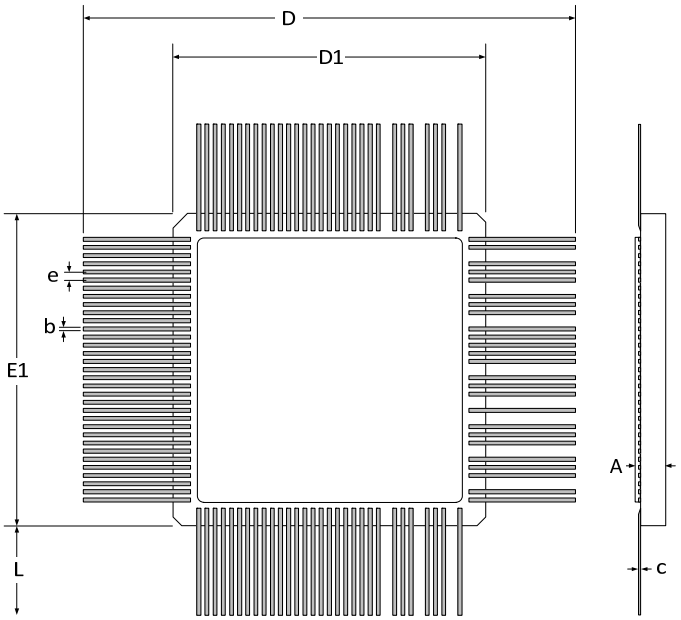
22.5 Over-Temperature Warning

The OTW_FAULT logic output goes high to indicate that the die temperature exceeds the over-temperature warning threshold, T_{OTW}. This warning allows a small operating window (typically 25°C) before the die temperature reaches the over-temperature shutdown threshold, T_{SD} (typically 150°C).

If Safe Mode is enabled, then for an over-temperature warning:
- OTW_FAULT is latched high
- The DMOD_OUT_N and DMOD_OUT_P resolver/LVDT drivers and all half-bridge MOSFETs are turned off
- The LX7720 enters a low power state with both the VEE and VBOOST charge pumps disabled and the BLO outputs forced low
- OTW_FAULT is cleared low (once the temperature has dropped by nominally 15°C from the over-temperature warning threshold) by either an active-high level on the RESET logic input or by disabling Safe Mode

If Safe Mode is disabled, then for an over-temperature warning:
- OTW_FAULT remains high while the over-temperature warning threshold is exceeded
- No other action is taken

23 CQFP-132 (Ceramic Quad Flat Pack) Dimensions



Dim	Millimeters		Inches	
	MIN	MAX	MIN	MAX
A	1.93	2.39	0.076	0.094
b	0.23	0.33	0.009	0.013
c	0.125	0.20	0.0049	0.0079
D	39.37 typ		1.55 typ	
D1	24.00	24.26	0.945	0.955
e	0.635 BSC		0.025 BSC	
E	39.37 typ		1.55 typ	
E1	24.00	24.25	0.945	0.955
L	7.62 typ		0.30 typ	

Figure 27. CQFP-132 Package Dimensions

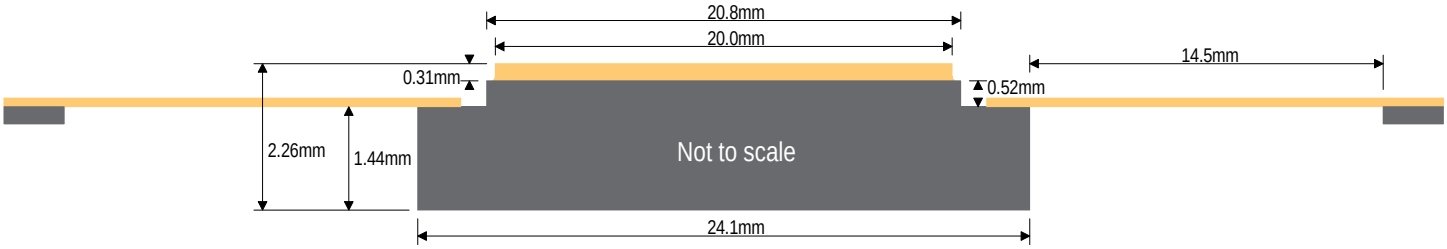


Figure 28. Package Cross-Section Nominal Dimensions as Shipped with Tie-Bars

CQFP-132 Packaging Notes

1. Controlling dimensions are in mm. Imperial (inch) equivalents are shown for general information
2. Package includes non-conductive ceramic tie-bars mechanically connected to all pins
3. Parts are shipped with untrimmed and unformed leads
4. Package mass is 4.6g typical with 14mm leads (trimmed flush with ceramic tie-bars, tie bars discarded)
5. Lead material is Kovar with NiAu plating (nickel under-plate followed by gold plating)
6. Lid material is Kovar or Alloy 42 with NiAu plating (nickel under-plate followed by gold plating)
7. Lid is electrically isolated from the leads, and is bonded hermetically to the ceramic body using AuSn solder
8. Use the (electrically non-conductive) base of the package as the surface for conducting heat from the package

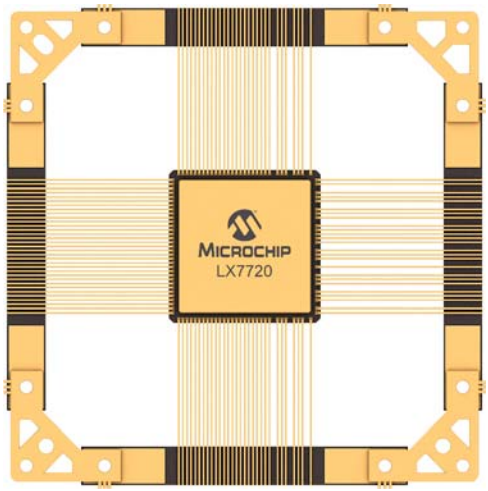
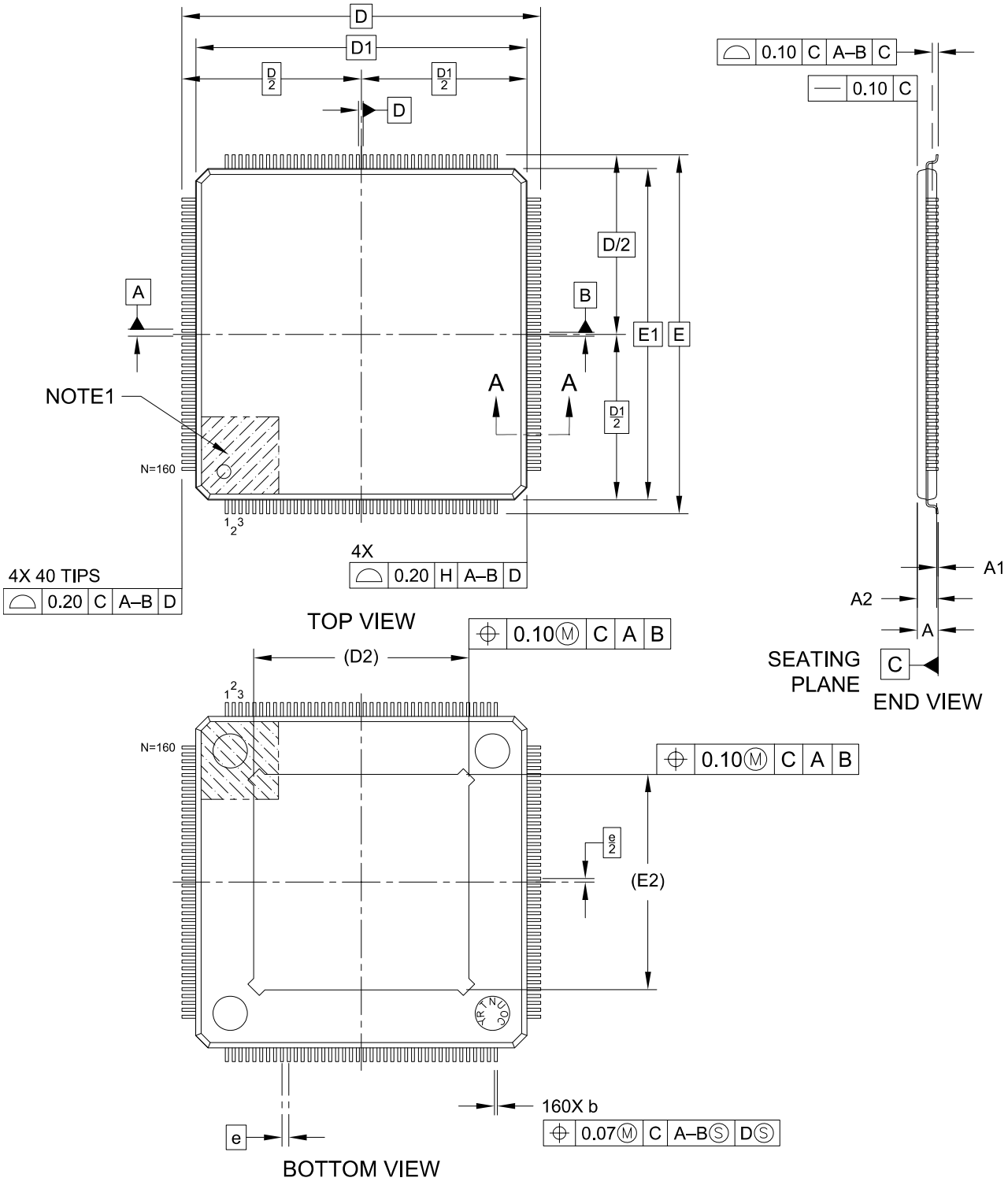


Figure 29. Package as shipped with non-conductive ceramic tie-bars, untrimmed and unformed leads

24 LQFP-160 Dimensions

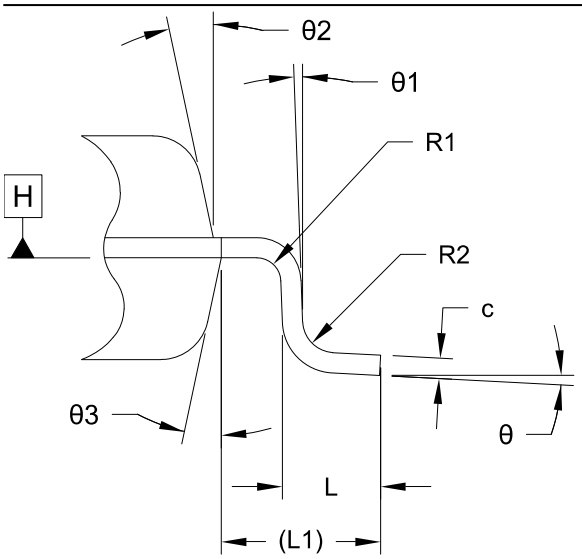
160-Lead Plastic Low Profile Quad Flat Pack (G9C) - 24x24x1.4 mm Body [LQFP] With 15.6x15.6mm Exposed Pad.

Notes:
1. The package drawing can be downloaded by searching for code G9C on the Package Outline Drawings webpage
2. The moisture sensitivity level for the LQFP-160 package as defined by IPC/JEDEC J-STD-020 is MSL-3

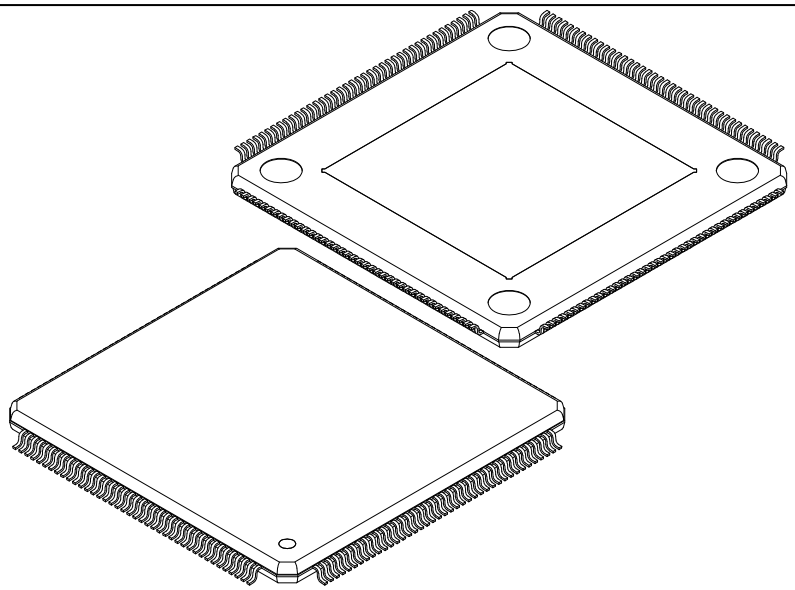


Microchip Technology Drawing C04-25652 Rev A Sheet 1 of 2

Figure 30. 160-Lead Plastic Quad Flat Pack Package Dimensions (1 of 2)



SECTION A–A



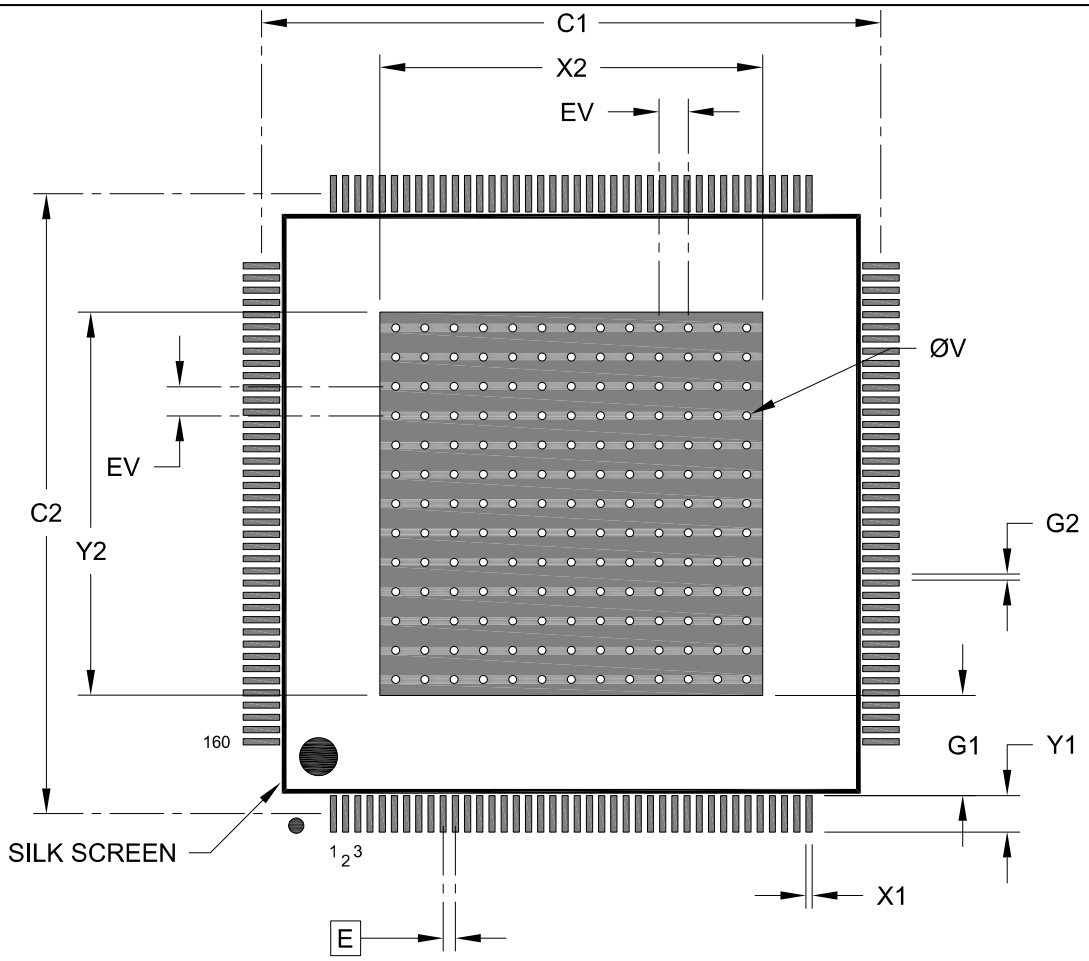
Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		160	
Pitch	e		0.50 BSC	
Overall Height	A	-	-	1.60
Standoff	A1	0.05	-	0.15
Molded Package Thickness	A2	1.30	1.40	1.45
Overall Length	D		26.00 BSC	
Molded Package Length	D1		24.00 BSC	
Overall Width	E		26.00 BSC	
Molded Package Width	E1		24.00 BSC	
Exposed Pad Length	D2		15.60 REF	
Exposed Pad Width	E2		15.60 REF	
Terminal Width	b	0.17	0.22	0.27
Terminal Thickness	c	0.09	-	0.20
Terminal Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Lead Bend Radius	R1	0.08	-	-
Lead Bend Radius	R2	0.08	-	0.20
Foot Angle	θ	0°	3.5°	7°
Lead Angle	θ1	0°	-	-
Mold Draft Angle	θ2	11°	12°	13°
Mold Draft Angle	θ3	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-25652 Rev A Sheet 2 of 2

Figure 31. 160-Lead Plastic Quad Flat Pack Package Dimensions (2 of 2)



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Center Pad Width	X2			15.70
Center Pad Length	Y2			15.70
Contact Pad Spacing	C1		25.40	
Contact Pad Spacing	C2		25.40	
Contact Pad Width (Xnn)	X1			0.25
Contact Pad Length (Xnn)	Y1			1.50
Contact Pad to Center Pad (Xnn)	G1	4.10		
Contact Pad to Contact Pad (Xnn)	G2	0.25		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-27652 Rev A

Figure 32. 160-Lead Plastic Quad Flat Pack Recommended Land Pattern

24.1 LQFP-160 Packaging Notes

1. Package mass is 1.6g typical
2. Lead frame material is Cu
3. Lead finish is NiPdAu
4. Bond wires are Au
5. Mold compound is Sumitomo G700X with the following outgassing properties:
   a. Total Mass Loss (TML): 0.08
   b. Recovered Mass Loss/Water Vapor Regained (RML/WVR): 0.03
   c. Collected Volatile Condensable Material (CVCM): 0.01
6. Connect the exposed pad on the package underside to SGND and use the pad to conduct heat from the package

25 Dual-Footprinting the CQFP-132 and LQFP-160 Packages

While there is no factory recommendation for lead forming the CQFP-132 package, Figure 33 below shows the forming used for the LX7720 daughter board. Figure 34 shows a corresponding typical footprint, with pads 1mm longer than and centered under each foot. Comparing the CQFP-132 and LQFP-160 footprints shows the considerations to be taken when planning a possible PCB layout change between packages. The main concern is allowing for the exposed pad under the LQFP-160 package, which must be connected to SGND. Since the underside of the CQFP-132 package is electrically non-conductive ceramic, a split SGND plus MGND arrangement can be used. This is shown in the pinout in section 1 on page 2. Note that a dual-layout can be made possible by forming the CQFP-132 leads further apart than shown in Figure 33 below, so that the correspondingly modified CQFP-132 footprint no longer overlaps the LQFP-160 footprint.

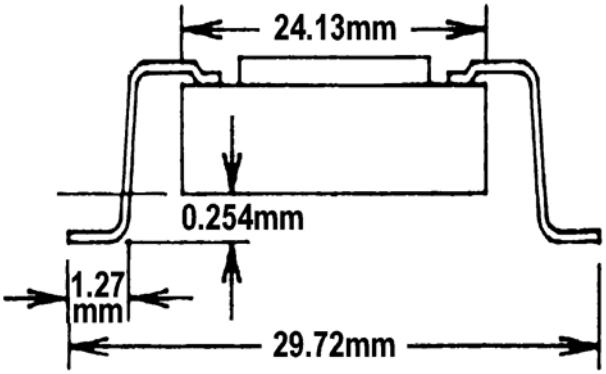


Figure 33. CQFP-132 Forming Specification used on the LX7720-DB

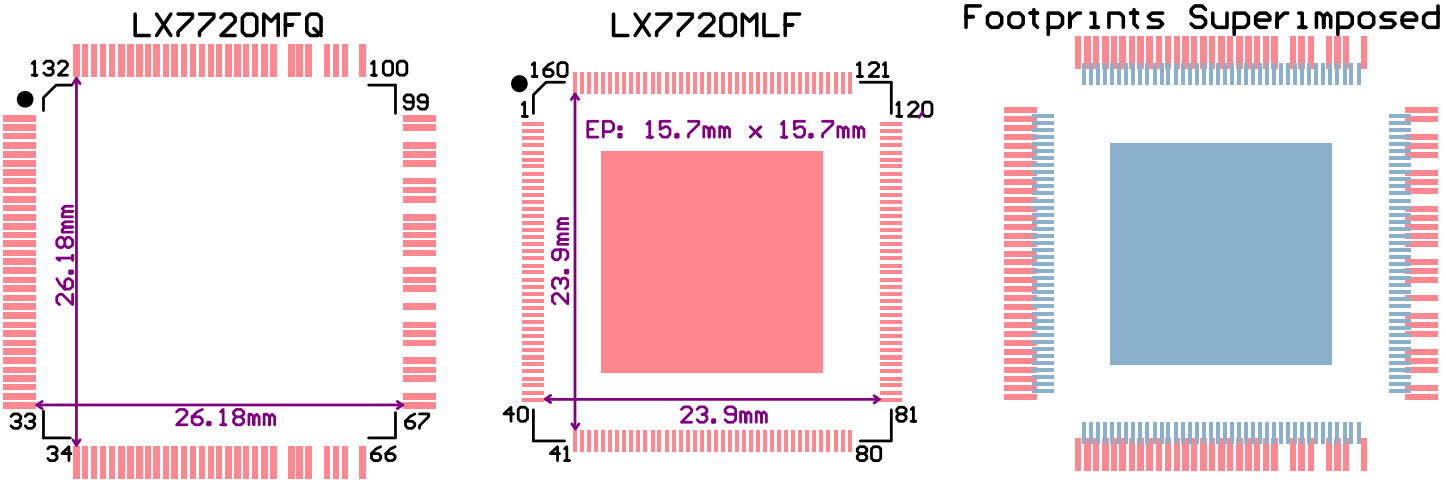


Figure 34. Comparing CQFP-132 and LQFP-160 Footprints

26 Revision History

26.1 Revision 1 - November 2019

First release.

26.2 Revision 1.1 - June 2020

Added plastic package.
Added CQFP-132 ES part is not hermetic, lid and lead material is Kovar, lid is isolated, θJB = 1.93°C/W from package back.
Added CDM ESD, moved ESD ratings to separate section.
Updated ceramic pinout drawing to show ground planes and decoupling.
Shipping type updated to tray in order table.
Added introduction section.
Added power supply section including sequencing recommendations.
Section 11 text cleanup for clarity.
Corrected omitted package pins in Figure 2 and Figure 3.
Corrected pin descriptions: VGS pins mislabeled ground instead of power, diodes go to VGS_# not SW_#, swapped pin 91/92 and pins 103/104 text, VFLT_# capacitors go to SW_# not MGND, VBOOST capacitor goes to VMPS not MGND, CPP swing, VEE_CP_N swing.
Added description for SPARE pin 53. Corrected pin reference numbers in description for pins 11, 12, 44, 46.
Added gate drive resistor value to pin descriptions.
Added gate drive resistors to block diagram.
Updated EC table to show that OTW_FAULT output can not be tested at +125°C.
-2V pin renamed TESTMODE0.
Clarified krad to krad(Si), added SAM3X8ERT to first page.

26.3 Revision 1.2 - December 2020

Branding moved from Microsemi to Microchip, and some terminology changed.
Added hot links to product page on front page.
Pin configuration and layout drawing updated to show VGS resistors.
Pin description updated to include VGS resistors and decoupling capacitor connections.
Noted in pin description that RESET input has 1MΩ pulldown to SGND.
Corrected QFP-208 pin 81 description VEE_CP_P swings between MGND and VGS.
Separated some specifications in electrical characteristics table as different for plastic packaged vs ceramic packaged parts.
SW_# maximum slew rate specification moved to absolute maximum ratings table.
CP_CLK, MOD_CLK specifications moved from electrical characteristics table to recommended operating conditions table.
Updated current sense CS_# to RTN_# in recommended operating conditions table from ±200mV to ±250mV to match guaranteed linear range in electrical characteristics table. Signal amplitudes added to INL entries for clarity.
Added minimum current for logic input internal pullup and pulldown resistors to electrical characteristics table.
Changed pin references in absolute maximum and electrical characteristics tables from numbers to names.
Updated Figure 2. Typical Application to include VFLT peak current limiting resistor and other half-bridge passives.
Table 1: added VBOOST components, updated the VEE and VGS recommendations.
Added section 15.1 covering the FET gate drive supplies.
Added section 21.1 covering interfacing 1.8V logic.
Added cross-section dimensions to CQFP-132 package, clarified lead & lid plating.
Added figure title to QFP-208 dimensions.

26.4 Revision 1.3 - March 2021

Added SMD numbers to ordering table, changed suffixes -EV to -V, and -EQ to -Q to correlate.
Corrected pin 120 and pin 121 pins swapped for QFP-208 plastic package.
Fixed some subscripts in Logic Levels and Bi-Level Inputs sections of electrical characteristics table.
Corrected Table 1 "CS_A, ... CS_D" to "CSPS_A, ... CSPS_D", DMOD_PS ground from SGND to MGND, VFLT_x voltage from VMPS + VGS to VGS, separated CPN/CPP capacitor from VBOOST capacitor for clarity.

26.5 Revision 1.4 - September 2021

Updated front page single event latch-up immunity to 80MeV.cm²/mg, ELDRS radiation tolerance to 100krad(Si).
Replaced 208 pin plastic package with 160 pin version.
Fixed pin function descriptions which referred to BLI1-6 all as 1.
Clarified that an external VEE supply can extend to -18V if the VEE_CP_P and VEE_CP_N pins are left open.
Added typical output resistance and maximum DC load current for logic outputs in section 21.

26.6 Revision 2 - June 2023

Updated weblinks from Microsemi to Microchip, and updated firmware support links in section 13.
Clarified that the plastic package qualification flow is JESD47.
Added Switch (SW_# and RTN_#) to Motor Power Supply (VMPS) for 20V to 60V operating rating
Updated CP_CLK pin descriptions to clarify that this is the clock source for both VEE and VBOOST charge pumps.
Updated DMOD_PS pin descriptions and section 17 to tie DMOD_PS to MGND if not used.
Updated VGS pin 48 (ceramic) and 62 (plastic) descriptions to clarify that this pin powers the VEE inverting charge pump.
Updated VGS pin 85 (ceramic) and 103 (plastic) descriptions to clarify that this pin powers the VBOOST charge pump.
Added ceramic and plastic package mechanical samples to ordering table.
EC Table: VREF lower limit for plastic package changed from 2.48V to 2.47V. V_{VEE} and V_{VBOOST} subscripting corrected.
Added typical VMPS supply currents to Table 1. Clarified that two VGS pins are charge pump rails. Reduced the recommendation for VGS decoupling from 10µF to 4.7µF.
Improved VEE section 14.2 description adding a figure, corrected $\overline{\text{EXT\_VEE\_EN}}$ input is MGND referred.
Updated rail sequencing section 14.3 to clarify that sequencing is not mandatory. Corrected Figure 4 MMF to MLF package and GND to SGND.
Added section 14.5 detailing the SGND and MGND ground domains.
Updated VGS section 15.1 regarding internal interconnection diodes and VGS connection for unused half-bridges and added more detail to typical half-bridge Figure 10.
Added section 16 covering the sigma-delta architecture.
Expanded the resolver/lvdt section 17.
Expanded the current sense amplifier section 18.
Added section 19 showing common motor and current sensing topologies.
Updated bi-level comparator section 20 with required rails to operate and behavior in Safe Mode on MOD_CLK failure.
Added expanded section 22 collating fault detection and management and clarifying Safe Mode behavior.
Noted in packaging section that the base of the CQFP-132 package is electrically non-conductive.
Added section after packaging discussing dual package layout options.

26.7 Revision 2.1 - June 2023

Updated Figure 21, Figure 24, Figure 25, and Figure 26 to show supply connections.

26.8 Revision 2.2 - September 2023

DMOD_PS fault current threshold specification in electrical characteristics table loosened from 110mA min, 360mA max to 90mA min, 370mA max for plastic packaged part.

26.9 Revision 2.3 - April 2024

Added explanation at start of section 18 for the optional capacitor across R_{CS} showing in Figure 18 and Figure 19. Added the capacitor to Figure 17.

26.10 Revision 2.4 - December 2024

Added θ_{JA} for ceramic package and both thermal resistance values for plastic package to section 10.
Added more detail about initial charging of bootstrap capacitor C2 on VFLT in section 15.1.
Added detail about VGS and SGND pin diode protections in section 14.6 and section 15.2.
Updated the plastic package drawings link and added the plastic package moisture sensitivity level (MSL) in section 24.
Added LQFP-160 packaging notes section 24.1 with material details.

26.11 Revision 3 - January 2025

Corrected CQFP-132 pin diagram on page 2 to show the four VGS recommended capacitors to be 4.7µF not 10µF.
Added notes under the ordering table where to find manufacturing product flow information, and clarified that all products offer the same radiation hardness.
Corrected section 14.2 to show recommended capacitor on VGS to be 4.7µF not 10µF.
Added typical MOSFET driver propagation delay and output impedance data to section 15.
Updated figures style.
Corrected typo in Figure 14: VREF to VGS.

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