

LP8758-E0 Four Output Step-Down DC-DC Regulator

1 Features

- Four High-Efficiency Step-Down DC-DC Converter Cores:
 - Maximum Output Current 4 A Per Core
 - Auto PWM-PFM and Forced-PWM Operations
 - Programmable Output Voltage Slew-Rate from 30 mV/μs to 0.5 mV/μs
 - Input Voltage Range = 2.5 V to 5.5 V
 - V_{OUT} Range = 0.5 V to 3.36 V with DVS
- Programmable Start-up and Shutdown Sequencing With Enable Signal
- I²C-Compatible Interface Which Supports Standard (100 kHz), Fast (400 kHz), Fast+ (1 MHz), and High-Speed (3.4 MHz) Modes
- Interrupt Function with Programmable Masking
- Load Current Measurement
- Output Short-Circuit and Overload Protection
- Spread-Spectrum Mode for EMI Reduction
- The Four Cores Operate 90° out of Phase Thereby Reducing Input Ripple Current
- Over-Temperature Warning and Protection
- Undervoltage Lockout (UVLO)

2 Applications

- Smart Phones, eBooks and Tablets
- Network Processor Cards (NPCs), Wireless and DSL Modems
- Solid State Drives
- Gaming Devices

3 Description

The LP8758-E0 is designed to meet the power management requirements for low-power processors in mobile phones, network cards, and similar applications. The device contains four step-down DC-DC converter cores, which provides four output voltage rails. The device is controlled by an I²C-compatible serial interface.

The automatic PWM-PFM (AUTO mode) operation maximizes efficiency over a wide output-current range.

The LP8758-E0 supports programmable start-up and shutdown sequencing synchronized to Enable signal.

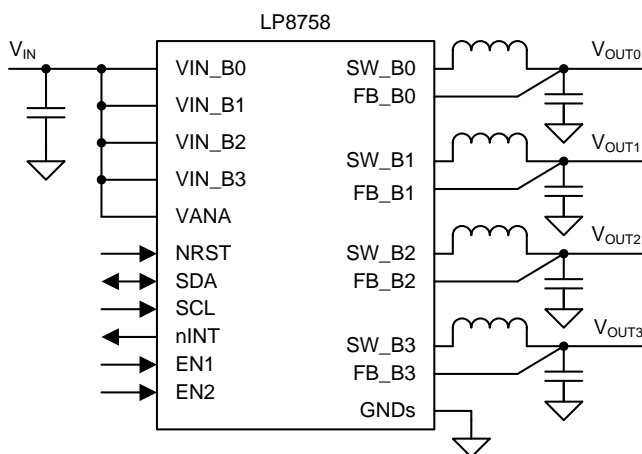
The protection features include short-circuit protection, current limits, input supply UVLO, and temperature warning and shutdown functions. Several error flags are provided for status information of the device. In addition, the LP8758-E0 device supports load current measurement without the addition of external current sense resistors. During start-up and voltage change, the device controls the output slew rate to minimize output voltage overshoot and the inrush current.

Device Information(1)

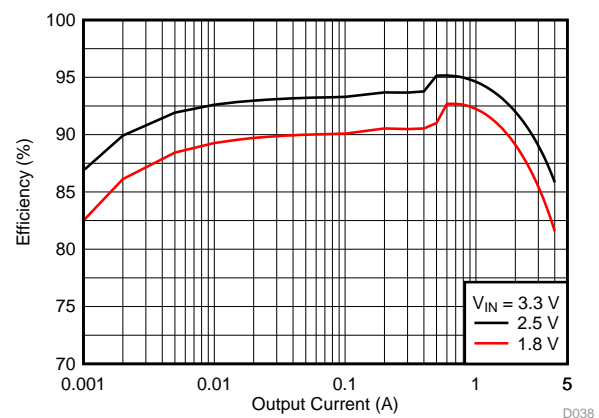
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP8758-E0	DSBGA (35)	2.88 mm x 2.13 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



Efficiency vs Output Current



D038



4 Device and Documentation Support

4.1 Documentation Support

4.1.1 Related Documentation

For related documentation, see the following:

Texas Instruments Application Note 1112 *DSBGA Wafer Level Chip Scale Package* ([SNVA009](#))

4.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

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4.3 Trademarks

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4.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

4.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

5 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP8758A1E0YFFR	PREVIEW	DSBGA	YFF	35	3000	TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

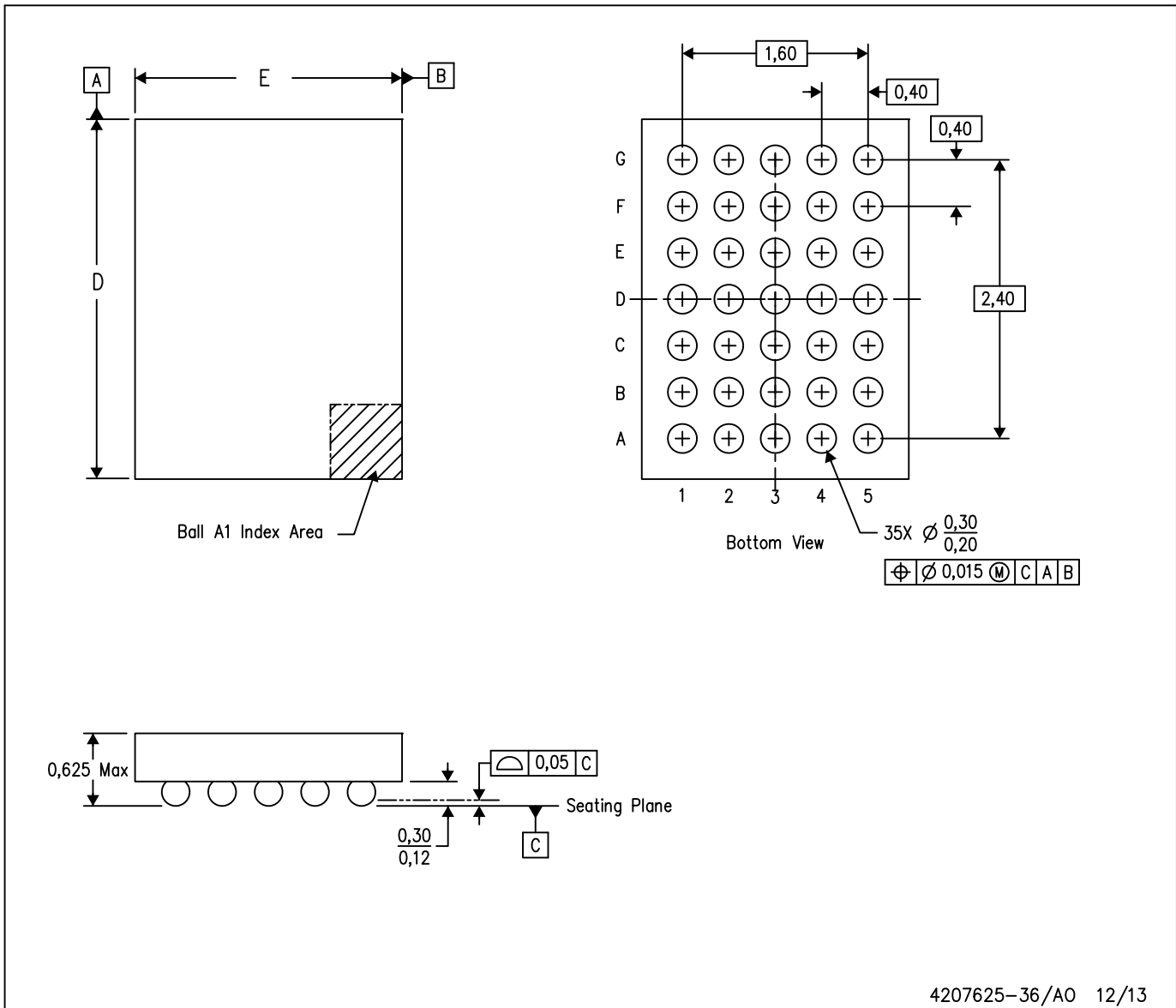
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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YFF (R-XBGA-N35)

DIE-SIZE BALL GRID ARRAY



- NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 B. This drawing is subject to change without notice.
 C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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