

## LP8758-B0 Four-Phase DC-DC Step-Down Converter

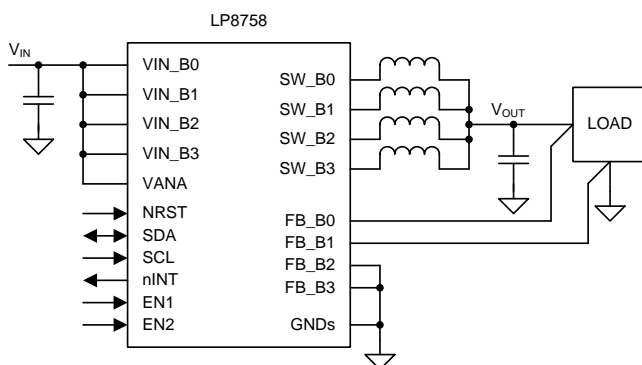
### 1 Features

- High-Efficiency Step-Down Four-Phase DC-DC Converter Cores:
  - Maximum Output Current 16 A
  - Auto PWM-PFM and Forced-PWM Operations
  - Auto Phase Adding/Shedding and Force Multi-Phase Operations
  - Remote Differential Feedback Voltage Sensing
  - Programmable Output Voltage Slew-Rate from 30 mV/μs to 0.5 mV/μs
  - $V_{OUT}$  Range = 0.5 V to 3.36 V with DVS
- Programmable Start-up and Shutdown Delays with Enable Signal
- I<sup>2</sup>C-Compatible Interface which Supports Standard (100 kHz), Fast (400 kHz), Fast+ (1 MHz), and High-Speed (3.4 MHz) Modes
- Interrupt Function with Programmable Masking
- Load Current Measurement
- Output Short-Circuit and Overload Protection
- Spread-Spectrum Mode and Phase Interleaving for EMI Reduction
- Overtemperature Warning and Protection
- Undervoltage Lockout (UVLO)

### 2 Applications

- Smart Phones, eBooks and Tablets
- Gaming Devices

### 4 Simplified Schematic



### 3 Description

The LP8758 is designed to meet the power management requirements of the latest application processors in mobile phones and similar portable applications. The device contains four step-down DC-DC converter cores, which are bundled together in a single 4-phase buck converter. The device is controlled by an I<sup>2</sup>C-compatible serial interface.

The automatic PWM-PFM (AUTO mode) operation, together with the automatic phase adding/shedding, maximizes efficiency over a wide output-current range. The LP8758 supports remote differential voltage sensing to compensate IR drop between the regulator output and the point-of-load, thus improving the accuracy of the output voltage.

The LP8758 supports programmable start-up and shutdown delays synchronized to Enable signal.

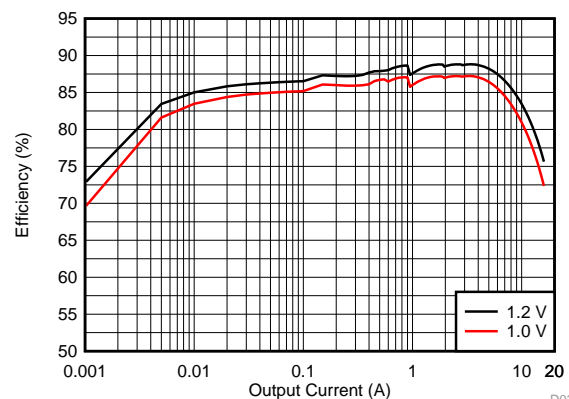
The protection features include short-circuit protection, current limits, input supply UVLO, and temperature warning and shutdown functions. Several error flags are provided for status information of the device. In addition, the LP8758 device supports load current measurement without the addition of external current sense resistors. During start-up and voltage change, the device controls the output slew rate to minimize output voltage overshoot and the inrush current.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP8758-B0	DSBGA (35)	2.88 mm x 2.13 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

#### Efficiency vs Output Current



D038



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## 5 Revision History

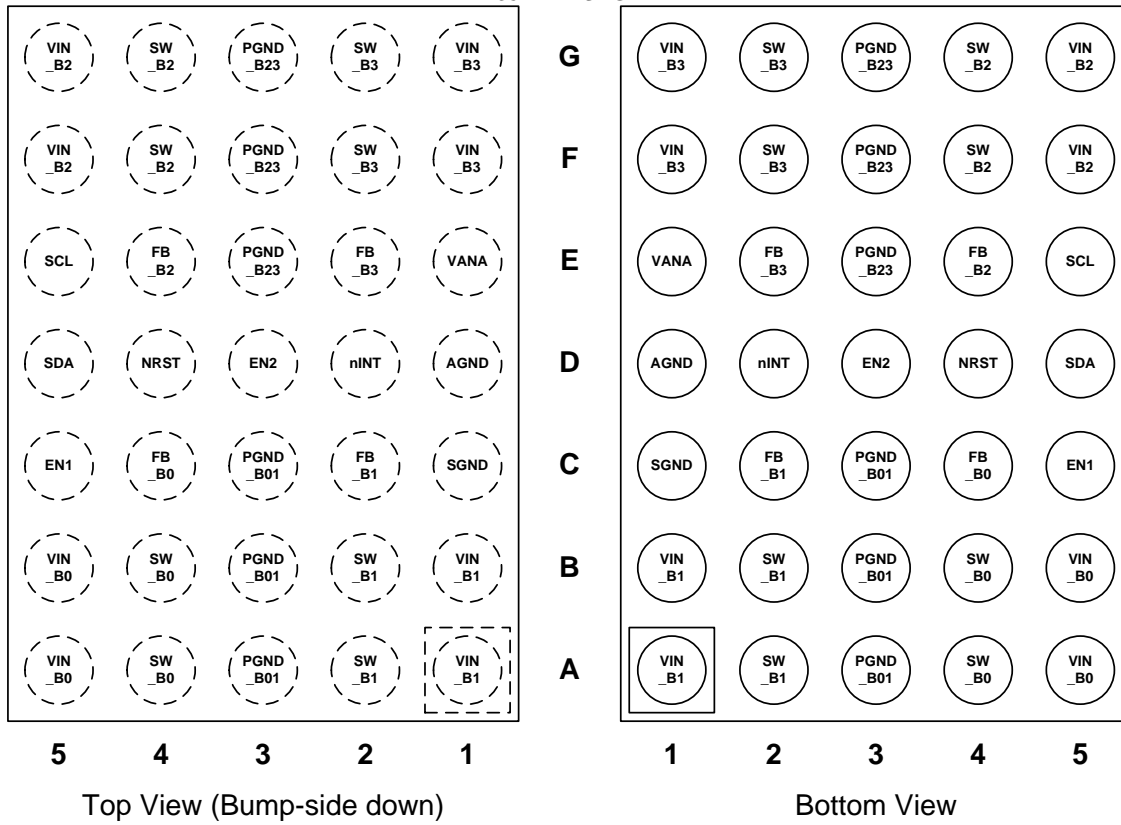
### Changes from Original (March 2015) to Revision A

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• first WEB release .....	1
• Added <i>Community Resources</i> section .....	49

## 6 Pin Configuration and Functions

YFF Package  
35-Pin DSBGA



### Pin Functions

PIN		TYPE	DESCRIPTION
NUMBER	NAME		
A1, B1	VIN_B1	P	Input for Buck 1. The separate power pins VIN_Bx are not connected together internally - VIN_Bx pins must be connected together in the application and be locally bypassed.
A2, B2	SW_B1	A	Buck 1 switch node.
A3, B3, C3	PGND_B01	G	Power Ground for Buck 0 and Buck 1.
A4, B4	SW_B0	A	Buck 0 switch node.
A5, B5	VIN_B0	P	Input for Buck 0. The separate power pins VIN_Bx are not connected together internally - VIN_Bx pins must be connected together in the application and be locally bypassed.
C1	SGND	G	Substrate Ground.
C2	FB_B1	A	Output ground feedback (negative) for Buck 0.
C4	FB_B0	A	Output voltage feedback (positive) for Buck 0.
C5	EN1	D/I	Programmable Enable signal for Buck regulator. Can be also configured to switch between two output voltage levels.
D1	AGND	G	Ground.
D2	nINT	D/O	Open-drain interrupt output. Active LOW.
D3	EN2	D/I	Programmable Enable signal for Buck regulator. Can be also configured to switch between two output voltage levels.
D4	NRST	D/I	Reset signal for the device.
D5	SDA	D/I/O	Serial interface data input and output for system access. Connect a pull-up resistor.
E1	VANA	P	Supply voltage for Analog and Digital blocks. VANA pin must be connected to same voltage as VIN_Bx pins.
E2	FB_B3	A	Output voltage feedback (positive) for Buck 3 - Connect to ground in 4-phase configuration.
E4	FB_B2	A	Output voltage feedback (positive) for Buck 2. - Connect to ground in 4-phase configuration.
E5	SCL	D/I	Serial interface clock input for system access. Connect a pull-up resistor.
F1, G1	VIN_B3	P	Input for Buck 3. The separate power pins VIN_Bx are not connected together internally - VIN_Bx pins must be connected together in the application and be locally bypassed.
F2, G2	SW_B3	A	Buck 3 switch node.
E3, F3, G3	PGND_B23	G	Power Ground for Buck 2 and Buck 3.
F4, G4	SW_B2	A	Buck 2 switch node.
F5, G5	VIN_B2	P	Input for Buck 2. The separate power pins VIN_Bx are not connected together internally - VIN_Bx pins must be connected together in the application and be locally bypassed.

A: Analog Pin, D: Digital Pin, G: Ground Pin, P: Power Pin, I: Input Pin, O: Output Pin

## 7 Specifications

### 7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)<sup>(1)(2)</sup>

		MIN	MAX	UNIT
<b>INPUT VOLTAGE</b>				
VIN_Bx, VANA	Voltage on power connections	-0.3	6	V
SW_Bx	Voltage on buck switch nodes	-0.3	(VIN_Bx + 0.3 V) with 6 V max	V
FB_Bx	Voltage on buck voltage sense nodes	-0.3	(VANA + 0.3 V) with 6 V max	V
NRST	Voltage on NRST input	-0.3	3.6	V
ENx, SDA, SCL, nINT	Voltage on logic pins (input or output pins)	-0.3	3.6	
<b>CURRENT</b>				
VIN_Bx, SW_Bx, PGND_Bx	Current on power pins (average current over 100k hour lifetime, T <sub>J</sub> = 125°C)		0.62	A/pin
<b>TEMPERATURE</b>				
T <sub>J-MAX</sub>	Junction temperature	-40	150	°C
	Storage temperature, T <sub>stg</sub>	-65	150	°C
	Maximum lead temperature (soldering, 10 sec.) <sup>(3)</sup>		260	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground.
- (3) For detailed soldering specifications and information, please refer to Application Note 1112: *DSBGA Wafer Level Chip Scale Package (SNVA009)*.

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
<b>INPUT VOLTAGE</b>				
VIN_Bx, VANA	Voltage on power connections	2.5	5.5	V
NRST	Voltage on NRST	1.65	1.95	
ENx, SDA, SCL, nINT	Voltage on logic pins (input or output pins)	0	1.95	
<b>TEMPERATURE</b>				
T <sub>J</sub>	Junction temperature	-40	125	°C
T <sub>A</sub>	Ambient temperature	-40	85	

## 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LP8758	UNIT
		YFF	
		35 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	56.1	°C/W
R <sub>θJctop</sub>	Junction-to-case (top) thermal resistance	0.2	
R <sub>θJB</sub>	Junction-to-board thermal resistance	8.5	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.9	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	8.4	
R <sub>θJcbot</sub>	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

Limits apply over the junction temperature range  $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ , specified  $V_{(VANA)}$ ,  $V_{IN}$ ,  $V_{(NRST)}$ ,  $V_{OUT}$  and  $I_{OUT}$  range, unless otherwise noted. Typical values are at  $T_J = 25^{\circ}\text{C}$ ,  $f_{SW} = 3\text{ MHz}$ ,  $V_{(VANA)} = V_{IN} = 3.7\text{ V}$  and  $V_{OUT} = 1\text{ V}$  unless otherwise noted.<sup>(1)(2)</sup>

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
<b>EXTERNAL COMPONENTS</b>							
C <sub>IN</sub>	Input filtering capacitance	Connected from VIN_Bx to PGND_Bx		1.9	10	μF	
C <sub>OUT</sub>	Output filtering capacitance, local	Capacitance per phase		10	22	μF	
C <sub>OUT-TOTAL</sub>	Output capacitance, total (local and remote)	Total output capacitance, 4-phase configuration		40	200	μF	
ESR <sub>C</sub>	Input and output capacitor ESR	[1-10] MHz			2	10	mΩ
L	Inductor	Inductance of the inductor			0.33 or 0.47		μH
				-30%		30%	
DCR <sub>L</sub>	Inductor DCR	TOKO, DFE252010F-R33M			16		mΩ
<b>BUCK REGULATOR</b>							
V <sub>IN</sub>	Input voltage range	Voltage between VIN_Bx and ground pins. VANA must be connected to the same supply as VIN_Bx.		2.5	3.7	5.5	V
V <sub>OUT</sub>	Output voltage	Programmable voltage range		0.5	1	3.36	V
		Step size, $0.5\text{ V} \leq V_{OUT} < 0.73\text{ V}$			10		mV
		Step size, $0.73\text{ V} \leq V_{OUT} < 1.4\text{ V}$			5		
		Step size, $1.4\text{ V} \leq V_{OUT} \leq 3.36\text{ V}$			20		
I <sub>OUT</sub>	Output current	Output current, 4-phase configuration				12 <sup>(3)</sup>	A
		Output current, 4-phase configuration, $V_{IN} > 3\text{ V}$ , $V_{OUT} < 2\text{ V}$				16 <sup>(3)</sup>	
	Dropout voltage	$V_{IN} - V_{OUT}$		0.7			V
	DC output voltage accuracy, includes voltage reference, DC load and line regulations, process and temperature	Forced PWM mode, $0.8\text{ V} \leq V_{OUT} \leq 1.2\text{ V}$ , $2.5\text{ V} \leq V_{IN} \leq 4.5\text{ V}$ , $T_J = 25^{\circ}\text{C}$ , $0 \leq I_{OUT} \leq I_{OUT(max)}$		-1%		1.5%	
		PFM mode, the average output voltage level is increased by max. 20 mV		min (-2%, -15 mV)		max (2%, 15 mV) 20 mV	

- (1) All voltage values are with respect to network ground.
- (2) Minimum (MIN) and maximum (MAX) limits are specified by design, test, or statistical analysis. Typical (TYP) numbers are not verified, but do represent the most likely norm.
- (3) The maximum output current is also limited by the junction temperature and maximum average current over lifetime. The power dissipation inside the die increases the junction temperature and limits the maximum current depending of the length of the current pulse, efficiency, board and ambient temperature. The maximum average current/pin over lifetime is described in [Absolute Maximum Ratings](#).

## Electrical Characteristics (continued)

Limits apply over the junction temperature range  $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ , specified  $V_{(VANA)}$ ,  $V_{IN}$ ,  $V_{(NRST)}$ ,  $V_{OUT}$  and  $I_{OUT}$  range, unless otherwise noted. Typical values are at  $T_J = 25^{\circ}\text{C}$ ,  $f_{SW} = 3 \text{ MHz}$ ,  $V_{(VANA)} = V_{IN} = 3.7 \text{ V}$  and  $V_{OUT} = 1 \text{ V}$  unless otherwise noted.<sup>(1)(2)</sup>

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Ripple, 4-phase configuration	PWM mode, $L = 0.33 \mu\text{H}$		10		$\text{mV}_{\text{p-p}}$
	PFM mode, $L = 0.33 \mu\text{H}$		10		
$\text{DC}_{\text{LNR}}$	DC line regulation $I_{OUT} = I_{OUT(\text{max})}$		$\pm 0.05$		$\%/V$
$\text{DC}_{\text{LDR}}$	DC load regulation in PWM mode $I_{OUT}$ from 0 to $I_{OUT(\text{max})}$		0.3%		
$T_{\text{LDSR}}$	Undershoot for transient load step response, 4-phase configuration	$I_{OUT} = 1 \text{ A to } 8 \text{ A}$ , $T_R = 400 \text{ ns}$ , PWM mode, $C_{OUT} = 100 \mu\text{F}$ , $L = 0.33 \mu\text{H}$		-45	mV
		$2.5 \text{ V} \leq V_{IN} \leq 4.5 \text{ V}$ , $0.8 \text{ V} \leq V_{OUT} \leq 1.2 \text{ V}$ , $I_{OUT} = 0.1 \text{ A to } 4.1 \text{ A}$ , $T_R = 100 \text{ ns}$ , AUTO mode, $C_{OUT} = 100 \mu\text{F}$ , $L = 0.33 \mu\text{H}$		-35	mV
		$3 \text{ V} \leq V_{IN} \leq 4.5 \text{ V}$ , $0.8 \text{ V} \leq V_{OUT} \leq 1.2 \text{ V}$ , $I_{OUT}$ from 1 A to 12 A, $T_R = 1000 \text{ ns}$ , $C_{OUT} = 100 \mu\text{F}$ , $L = 0.33 \mu\text{H}$		-45	mV
	Overshoot for transient load step response, 4-phase configuration	$I_{OUT} = 8 \text{ A to } 1 \text{ A}$ , $T_F = 400 \text{ ns}$ , PWM mode, $C_{OUT} = 100 \mu\text{F}$ , $L = 0.33 \mu\text{H}$		45	mV
		$2.5 \text{ V} \leq V_{IN} \leq 4.5 \text{ V}$ , $0.8 \text{ V} \leq V_{OUT} \leq 1.2 \text{ V}$ , $I_{OUT} = 4.1 \text{ A to } 0.1 \text{ A}$ , $T_F = 100 \text{ ns}$ , AUTO mode, $C_{OUT} = 100 \mu\text{F}$ , $L = 0.33 \mu\text{H}$		25	mV
		$3 \text{ V} \leq V_{IN} \leq 4.5 \text{ V}$ , $0.8 \text{ V} \leq V_{OUT} \leq 1.2 \text{ V}$ , $I_{OUT}$ from 12 A to 1 A, $T_F = 1000 \text{ ns}$ , $C_{OUT} = 100 \mu\text{F}$ , $L = 0.33 \mu\text{H}$		50	mV
$T_{\text{LNSR}}$	Transient line response $V_{IN}$ stepping $2.5 \text{ V} \leftrightarrow 3 \text{ V}$ , $T_R = T_F = 10 \mu\text{s}$ , $I_{OUT} = I_{OUT(\text{max})}$		$\pm 20$		mV
$I_{\text{LIM FWD}}$	Forward current limit (peak for every switching cycle)	Programmable range	1.5	5	A
		Step size		0.5	
		Accuracy, $3 \text{ V} \leq V_{IN} \leq 5.5 \text{ V}$ , $I_{\text{LIM}} = 5 \text{ A}$	-5%	7.5%	20%
		Accuracy, $2.5 \text{ V} \leq V_{IN} < 3 \text{ V}$ , $I_{\text{LIM}} = 5 \text{ A}$	-20%	7.5%	20%
$I_{\text{LIM NEG}}$	Negative current limit	1.6	2	2.4	A
$R_{\text{DS(ON) HS FET}}$	On-resistance, high-side FET Each phase, between $V_{IN\_Bx}$ and $SW\_Bx$ pins ( $I = 1 \text{ A}$ )		40	90	$\text{m}\Omega$
$R_{\text{DS(ON) LS FET}}$	On-resistance, low-side FET Each phase, between $SW\_Bx$ and $PGND\_Bx$ pins ( $I = 1 \text{ A}$ )		33	50	$\text{m}\Omega$
	Current balancing $I_{OUT} > 1000 \text{ mA / phase}$ , $0.8 \text{ V} \leq V_{OUT} \leq 1.2 \text{ V}$			10%	
	Overshoot during Start-up $V_{OUT} = 1 \text{ V}$ , Slew rate = $10 \text{ mV}/\mu\text{s}$			50	mV
$I_{\text{PFM-PWM}}$	PFM-to-PWM transition - current threshold <sup>(4)</sup>		600		mA
$I_{\text{PWM-PFM}}$	PWM-to-PFM transition - current threshold <sup>(4)</sup>		240		mA
$I_{\text{ADD}}$	Phase-adding level	From 1-phase to 2-phase		1000	mA
		From 2-phase to 3-phase		2000	
		From 3-phase to 4-phase		3000	
$I_{\text{SHED}}$	Phase-shedding level	From 2-phase to 1-phase		750	mA
		From 3-phase to 2-phase		1500	
		From 4-phase to 3-phase		2300	

(4) The final PFM-to-PWM and PWM-to-PFM transition current varies slightly and is dependant on the output voltage, input voltage and the magnitude of inductor's ripple current.

## Electrical Characteristics (continued)

Limits apply over the junction temperature range  $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ , specified  $V_{(VANA)}$ ,  $V_{IN}$ ,  $V_{(NRST)}$ ,  $V_{OUT}$  and  $I_{OUT}$  range, unless otherwise noted. Typical values are at  $T_J = 25^{\circ}\text{C}$ ,  $f_{SW} = 3\text{ MHz}$ ,  $V_{(VANA)} = V_{IN} = 3.7\text{ V}$  and  $V_{OUT} = 1\text{ V}$  unless otherwise noted.<sup>(1)(2)</sup>

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output pulldown resistance	Regulator disabled	150	250	350	$\Omega$
Powergood threshold for interrupt BUCKx_INT(BUCKx_SC_INT), difference from final voltage	Rising ramp voltage, enable or voltage change	-23	-17	-10	mV
	Falling ramp, voltage change	10	17	23	
Powergood threshold for status signal BUCKx_STAT(BUCKx_PG_S TAT)	During operation, status signal is forced to '0' during voltage change	-23	-17	-10	mV
<b>PROTECTION FEATURES</b>					
Thermal warning	Temperature rising, CONFIG(TDIE_WARN_LEVEL) = 0		125		$^{\circ}\text{C}$
	Temperature rising, CONFIG(TDIE_WARN_LEVEL) = 1		105		
	Hysteresis		15		
Thermal shutdown	Temperature rising		150		$^{\circ}\text{C}$
	Hysteresis		15		
VANA <sub>UVLO</sub> VANA undervoltage lockout	Voltage falling	2.3	2.4	2.5	V
	Hysteresis		50		mV
<b>LOAD CURRENT MEASUREMENT</b>					
Current measurement range	Maximum code		20.46		A
Resolution	LSB		20		mA
Measurement accuracy	$I_{OUT} \geq 2\text{ A}$		<10%		
<b>CURRENT CONSUMPTION</b>					
Shutdown current consumption	$V_{(NRST)} = 0\text{ V}$		1		$\mu\text{A}$
Standby current consumption, regulator disabled	$V_{(NRST)} = 1.8\text{ V}$		6		$\mu\text{A}$
Active current consumption during PFM operation	$V_{(NRST)} = 1.8\text{ V}$ , $I_{OUT} = 0\text{ mA}$ , not switching		71		$\mu\text{A}$
Active current consumption during PWM operation	$V_{(NRST)} = 1.8\text{ V}$ , $I_{OUT} = 0\text{ mA}$		18		mA

## Electrical Characteristics (continued)

Limits apply over the junction temperature range  $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ , specified  $V_{(VANA)}$ ,  $V_{IN}$ ,  $V_{(NRST)}$ ,  $V_{OUT}$  and  $I_{OUT}$  range, unless otherwise noted. Typical values are at  $T_J = 25^{\circ}\text{C}$ ,  $f_{SW} = 3\text{ MHz}$ ,  $V_{(VANA)} = V_{IN} = 3.7\text{ V}$  and  $V_{OUT} = 1\text{ V}$  unless otherwise noted.<sup>(1)(2)</sup>

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
<b>DIGITAL INPUT SIGNALS NRST, ENx, SCL, SDA</b>							
$V_{IL}$	Input low level			0.4	V		
$V_{IH}$	Input high level	1.2			V		
$V_{HYS}$	Hysteresis of Schmitt trigger inputs (SCL, SDA)	10	80	160	mV		
	ENx pulldown resistance	ENx_PD = 1		500	k $\Omega$		
	NRST pulldown resistance	Always present		800	1200	1700	k $\Omega$
<b>DIGITAL OUTPUT SIGNALS nINT, SDA</b>							
$V_{OL}$	Output low level	$I_{SOURCE} = 2\text{ mA}$		0.4	V		
$R_P$	External pullup resistor for nINT	To VIO Supply		10	k $\Omega$		
<b>ALL DIGITAL INPUTS</b>							
$I_{LEAK}$	Input current	All logic inputs over pin voltage range		-1	1	$\mu\text{A}$	

## 7.6 I<sup>2</sup>C Serial Bus Timing Parameter

See <sup>(1)</sup> and <a href="#">Figure 1</a> .		MIN	MAX	UNIT	
$f_{SCL}$	Serial clock frequency	Standard mode	100	kHz	
		Fast mode	400	kHz	
		Fast mode +	1	MHz	
		High-speed mode, $C_b = 100\text{ pF}$	3.4	MHz	
		High-speed mode, $C_b = 400\text{ pF}$	1.7	MHz	
$t_{LOW}$	SCL low time	Standard mode	4.7	$\mu\text{s}$	
		Fast mode	1.3		
		Fast mode +	0.5		
		High-speed mode, $C_b = 100\text{ pF}$	160	ns	
		High-speed mode, $C_b = 400\text{ pF}$	320		
$t_{HIGH}$	SCL high time	Standard mode	4	$\mu\text{s}$	
		Fast mode	0.6		
		Fast mode +	0.26		
		High-speed mode, $C_b = 100\text{ pF}$	60	ns	
		High-speed mode, $C_b = 400\text{ pF}$	120		
$t_{SU,DAT}$	Data setup time	Standard mode	250	ns	
		Fast mode	100		
		Fast mode +	50		
		High-speed mode	10		
$t_{HD,DAT}$	Data hold time	Standard mode	0	3.45	$\mu\text{s}$
		Fast mode	0	0.9	
		Fast mode +	0		
		High-speed mode, $C_b = 100\text{ pF}$	0	70	ns
		High-speed mode, $C_b = 400\text{ pF}$	0	150	
$t_{SU,STA}$	Setup time for a start or a repeated start condition	Standard mode	4.7	$\mu\text{s}$	
		Fast mode	0.6		
		Fast mode +	0.26		
		High-speed mode	160	ns	

(1)  $C_b$  refers to the capacitance of one bus line.  $C_b$  is expressed in pF units.

**I<sup>2</sup>C Serial Bus Timing Parameter (continued)**

See <sup>(1)</sup> and Figure 1.		MIN	MAX	UNIT	
$t_{HD;STA}$	Hold time for a start or a repeated start condition	Standard mode	4	$\mu$ s	
		Fast mode	0.6		
		Fast mode +	0.26		
		High-speed mode	160	ns	
$t_{BUF}$	Bus free time between a stop and start condition	Standard mode	4.7	$\mu$ s	
		Fast mode	1.3		
		Fast mode +	0.5		
$t_{SU;STO}$	Setup time for a stop condition	Standard mode	4	$\mu$ s	
		Fast mode	0.6		
		Fast mode +	0.26		
		High-speed mode	160	ns	
$t_{rDA}$	Rise time of SDA signal	Standard mode		1000	ns
		Fast mode	$20+0.1 C_b$	300	
		Fast mode +		120	
		High-speed mode, $C_b = 100$ pF	10	80	
		High-speed mode, $C_b = 400$ pF	20	160	
$t_{fDA}$	Fall time of SDA signal	Standard mode		250	ns
		Fast mode	$20+0.1 C_b$	250	
		Fast mode +	$20+0.1 C_b$	120	
		High-speed mode, $C_b = 100$ pF	10	80	
		High-speed mode, $C_b = 400$ pF	20	160	
$t_{rCL}$	Rise time of SCL signal	Standard mode		1000	ns
		Fast mode	$20+0.1 C_b$	300	
		Fast mode +		120	
		High-speed Mode, $C_b = 100$ pF	10	40	
		High-speed Mode, $C_b = 400$ pF	20	80	
$t_{rCL1}$	Rise time of SCL signal after a repeated start condition and after an acknowledge bit	Standard mode		1000	ns
		Fast mode	$20+0.1 C_b$	300	
		Fast mode +		120	
		High-speed mode, $C_b = 100$ pF	10	80	
		High-speed mode, $C_b = 400$ pF	20	160	
$t_{fCL}$	Fall time of a SCL signal	Standard mode		300	ns
		Fast mode	$20+0.1 C_b$	300	
		Fast mode +	$20+0.1 C_b$	120	
		High-speed mode, $C_b = 100$ pF	10	40	
		High-speed mode, $C_b = 400$ pF	20	80	
$C_b$	Capacitive load for each bus line (SCL and SDA)		400	pF	
$t_{SP}$	Pulse width of spike suppressed in SCL and SDA lines (spikes that are less than the indicated width are suppressed)	Fast mode, fast mode +		50	ns
		High-speed mode		10	

### 7.7 Switching Characteristics

Limits apply over the junction temperature range  $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ , specified  $V_{(VANA)}$ ,  $V_{IN}$ ,  $V_{(NRST)}$ ,  $V_{OUT}$  and  $I_{OUT}$  range, unless otherwise noted. Typical values are at  $T_J = 25^{\circ}\text{C}$ ,  $f_{SW} = 3\text{ MHz}$ ,  $V_{(VANA)} = V_{IN} = 3.7\text{ V}$  and  $V_{OUT} = 1\text{ V}$  unless otherwise noted.<sup>(1)</sup>

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{SW}$	Switching frequency, PWM mode	2.7	3	3.3	MHz
$f_{SW-MAX}$	Maximum switching frequency, PWM mode $V_{OUT} \geq 0.6\text{ V}$	2.7	3	3.3	MHz
	Automatically limited to smaller of $f_{SW}$ and $f_{SW-MAX}$ $V_{OUT} < 0.6\text{ V}$	1.8	2	2.2	
Regulator start-up time (soft start)	From ENx to $V_{OUT} = 0.225\text{ V}$ (slew-rate control begins), $C_{OUT-TOTAL} = 88\text{ }\mu\text{F}$ , no load		90		$\mu\text{s}$
Output voltage slew-rate <sup>(2)</sup>	SLEW_RATEx[2:0] = 000, $V_{OUT} \geq 0.5\text{ V}$	-15%	30	15%	mV/ $\mu\text{s}$
	SLEW_RATEx[2:0] = 001, $V_{OUT} \geq 0.5\text{ V}$	-15%	15	15%	
	SLEW_RATEx[2:0] = 010, $V_{OUT} \geq 0.5\text{ V}$	-15%	10	15%	
	SLEW_RATEx[2:0] = 011, $V_{OUT} \geq 0.5\text{ V}$	-15%	7.5	15%	
	SLEW_RATEx[2:0] = 100, $V_{OUT} \geq 0.5\text{ V}$	-15%	3.8	15%	
	SLEW_RATEx[2:0] = 101, $V_{OUT} \geq 0.5\text{ V}$	-15%	1.9	15%	
	SLEW_RATEx[2:0] = 110, $V_{OUT} \geq 0.5\text{ V}$	-15%	0.94	15%	
Load current measurement time	PFM mode (automatically changing to PWM mode for the measurement)		50		$\mu\text{s}$
	PWM mode		4		

- (1) Minimum (MIN) and maximum (MAX) limits are specified by design, test, or statistical analysis. Typical (TYP) numbers are not verified, but do represent the most likely norm.
- (2) The slew-rate can be limited by the current limit (forward or negative current limit), output capacitance and load current.

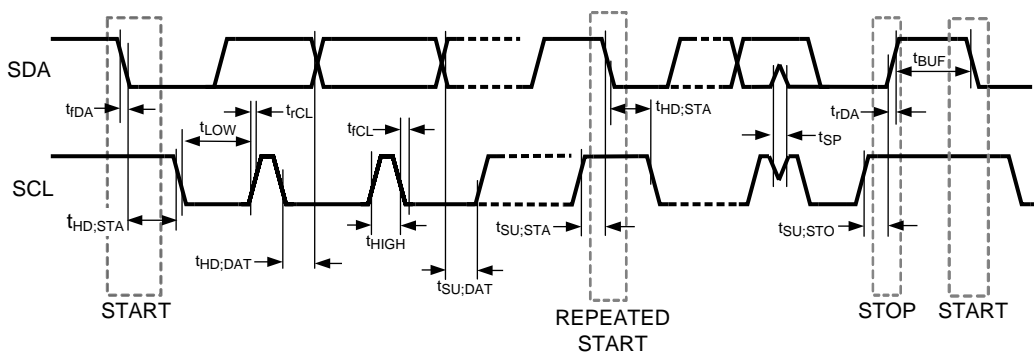
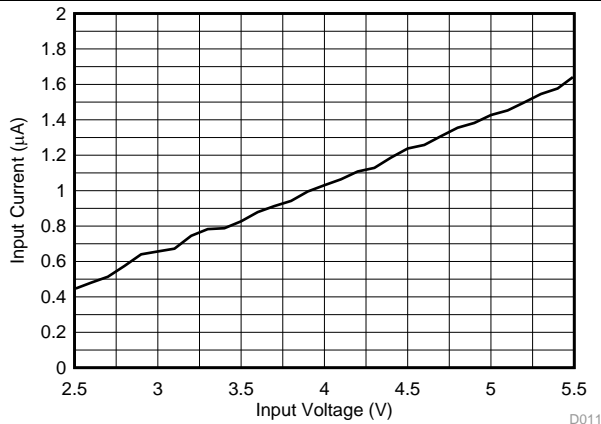


Figure 1. I<sup>2</sup>C Timing

## 7.8 Typical Characteristics

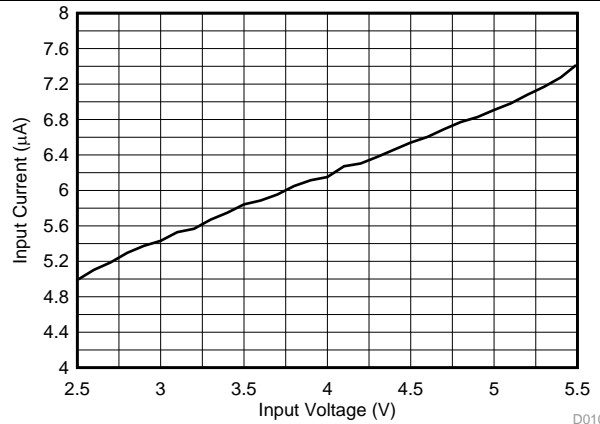
Unless otherwise specified:  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{IN} = 3.7\text{ V}$ ,  $f_{SW} = 3\text{ MHz}$ .



$V_{(NRST)} = 0\text{ V}$

D011

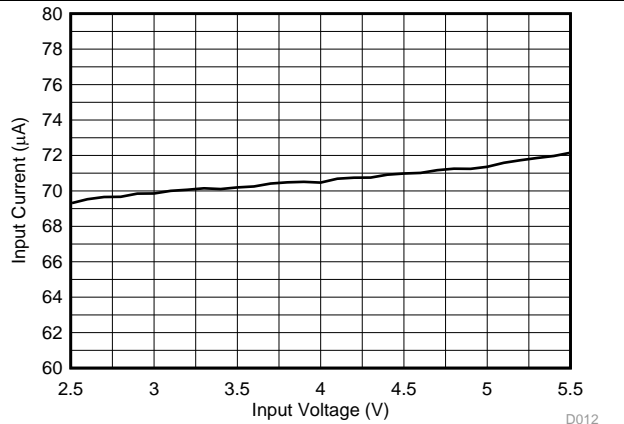
Figure 2. Shutdown Current Consumption vs Input Voltage



$V_{(NRST)} = 1.8\text{ V}$  Regulator disabled

D010

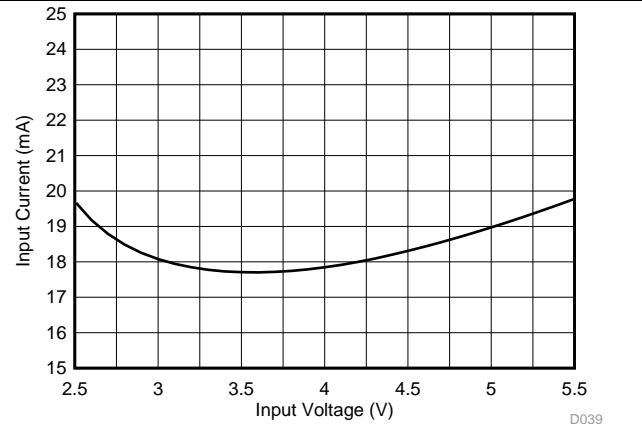
Figure 3. Standby Current Consumption vs Input Voltage



$V_{(NRST)} = 1.8\text{ V}$   $V_{(EN1)} = 1.8\text{ V}$   $V_{OUT} = 1\text{ V}$   
Load = 0 mA  $L = 330\text{ nH}$

D012

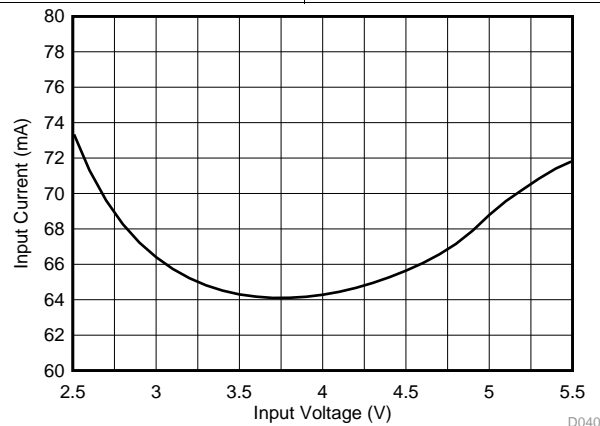
Figure 4. PFM Mode Current Consumption vs Input Voltage



$V_{(NRST)} = 1.8\text{ V}$   $V_{(EN1)} = 1.8\text{ V}$   $V_{OUT} = 1\text{ V}$   
Load = 0 mA 1 phase active  $L = 330\text{ nH}$

D039

Figure 5. PWM Mode Current Consumption vs Input Voltage



$V_{(NRST)} = 1.8\text{ V}$   $V_{(EN1)} = 1.8\text{ V}$   $V_{OUT} = 1\text{ V}$   
Load = 0 mA 4 phases active  $L = 330\text{ nH}$

D040

Figure 6. Forced Multi-Phase Current Consumption vs Input Voltage

## 8 Detailed Description

### 8.1 Overview

The LP8758 is a high-efficiency, high-performance power supply device with four step-down DC-DC converter cores. The cores are configured for a single 4-phase configuration. The device delivers 0.5-V to 3.36-V regulated voltage rail from 2.5-V to 5.5-V battery or supply voltage to portable devices such as cell phones, tablets, and PDAs.

There are two modes of operation for the converter, depending on the output current required: Pulse-Width Modulation (PWM) and Pulse-Frequency Modulation (PFM). The converter operates in PWM mode at high load currents of approximately 400 mA or higher. When operating in PWM mode the phases are automatically added/shedded based on the load current level. Lighter output current loads will cause the converter to automatically switch into PFM mode for reduced current consumption and a longer battery life when Forced PWM mode is disabled. The Forced multi-phase mode can be enabled for highest transient performance.

Additional features include soft-start, undervoltage lockout, overload protection, thermal warning, and thermal shutdown.

#### 8.1.1 Buck Information

The LP8758 has four integrated high-efficiency buck converter cores. The cores are designed for flexibility; most of the functions are programmable, thus giving a possibility to optimize the regulator operation for each application.

##### 8.1.1.1 Operating Modes

- OFF: Output is isolated from the input voltage rail in this mode. Output has an optional pull-down resistor.
- PWM: Converter operates in buck configuration with fixed switching frequency.
- PFM: Converter switches only when output voltage decreases below programmed threshold. Inductor current is discontinuous.

##### 8.1.1.2 Features

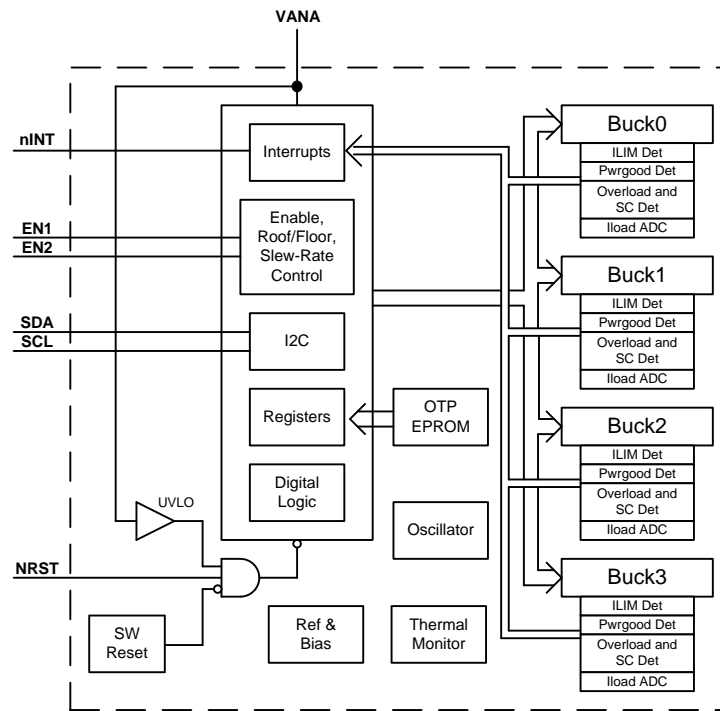
- Output voltage
- Forced PWM operation
- Forced multi-phase operation (forces also the PWM operation)
- Switch current limit
- Output voltage slew rate
- Enable and disable delays

##### 8.1.1.3 Programmability

The following parameters can be programmed via registers:

- DVS support with programmable slew-rate
- Automatic mode control based on the loading
- Synchronous rectification
- Current mode loop with PI compensator
- Optional spread spectrum technique to reduce EMI
- Soft start
- Power good flag with maskable interrupt
- Phase control for optimized EMI
- Average output current sensing (for PFM entry, phase shedding/adding, and load current measurement)
- Current balancing between the phases of the converter
- Differential voltage sensing from point of the load
- Dynamic phase shedding/adding, each output being phase shifted

## 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Multi-Phase DC-DC Converters

#### 8.3.1.1 Overview

A multi-phase synchronous buck converter offers several advantages over a single power stage converter. For application processor power delivery, lower ripple on the input and output currents and faster transient response to load steps are the most significant advantages. Also, since the load current is evenly shared among multiple channels, the heat generated is greatly reduced for each channel due to the fact that power loss is proportional to square of current. Physical size of the output inductor shrinks significantly due to this heat reduction. A block diagram of a single core is shown in [Figure 7](#).

Interleaving switching action of the converters and channels in a four-phase configuration is illustrated in [Figure 8](#).

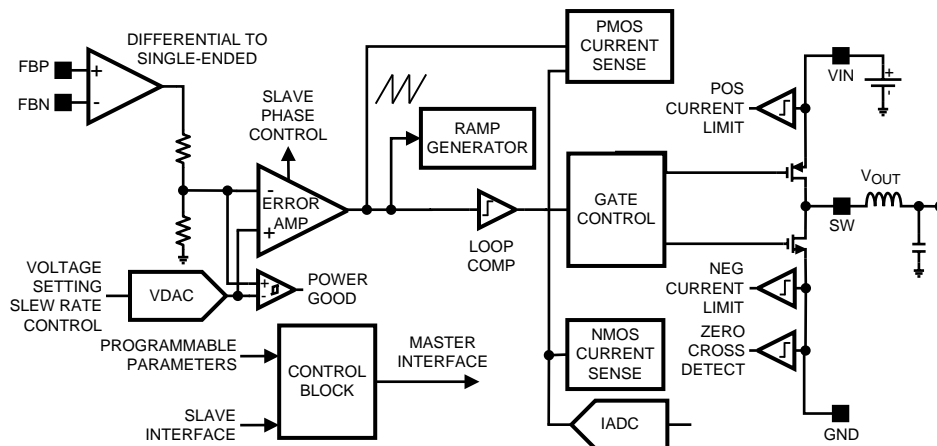


Figure 7. Detailed Block Diagram Showing One Core

Feature Description (continued)

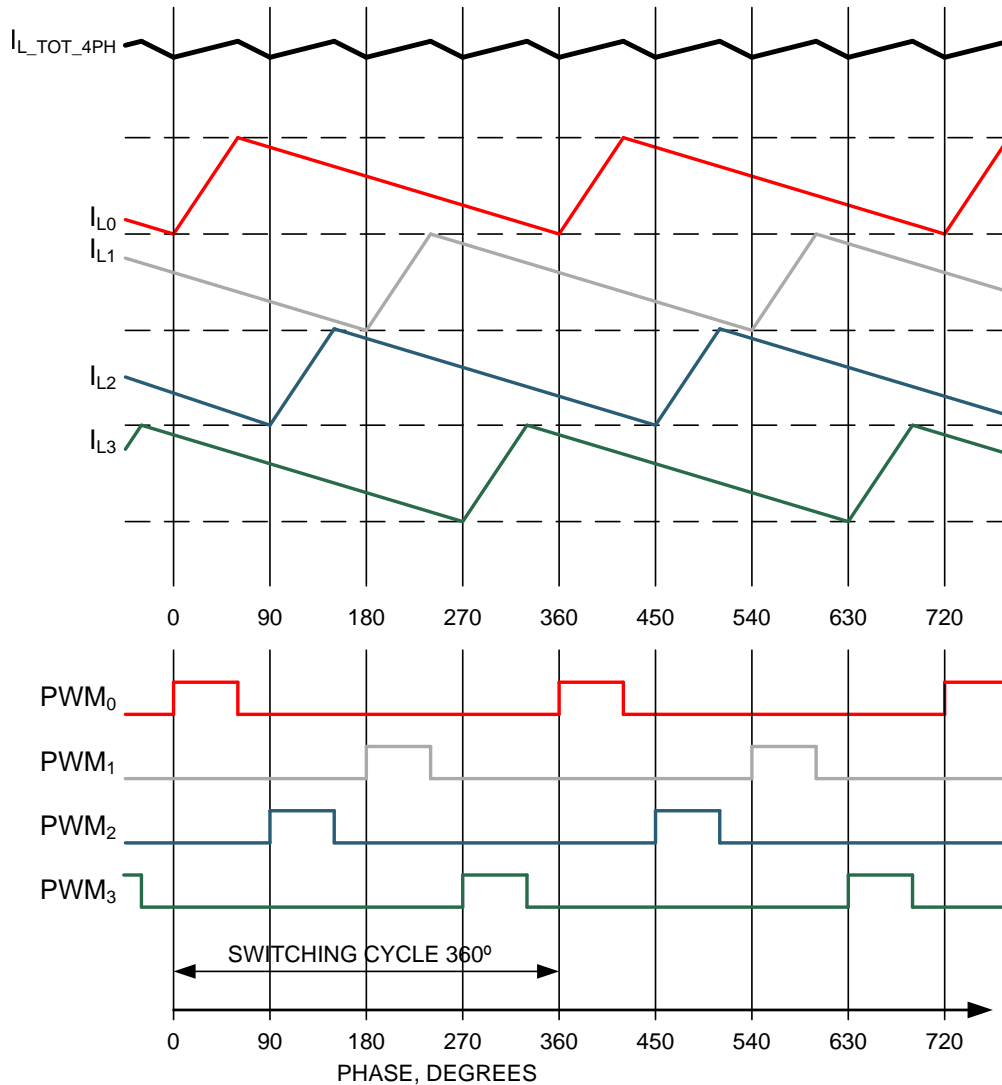


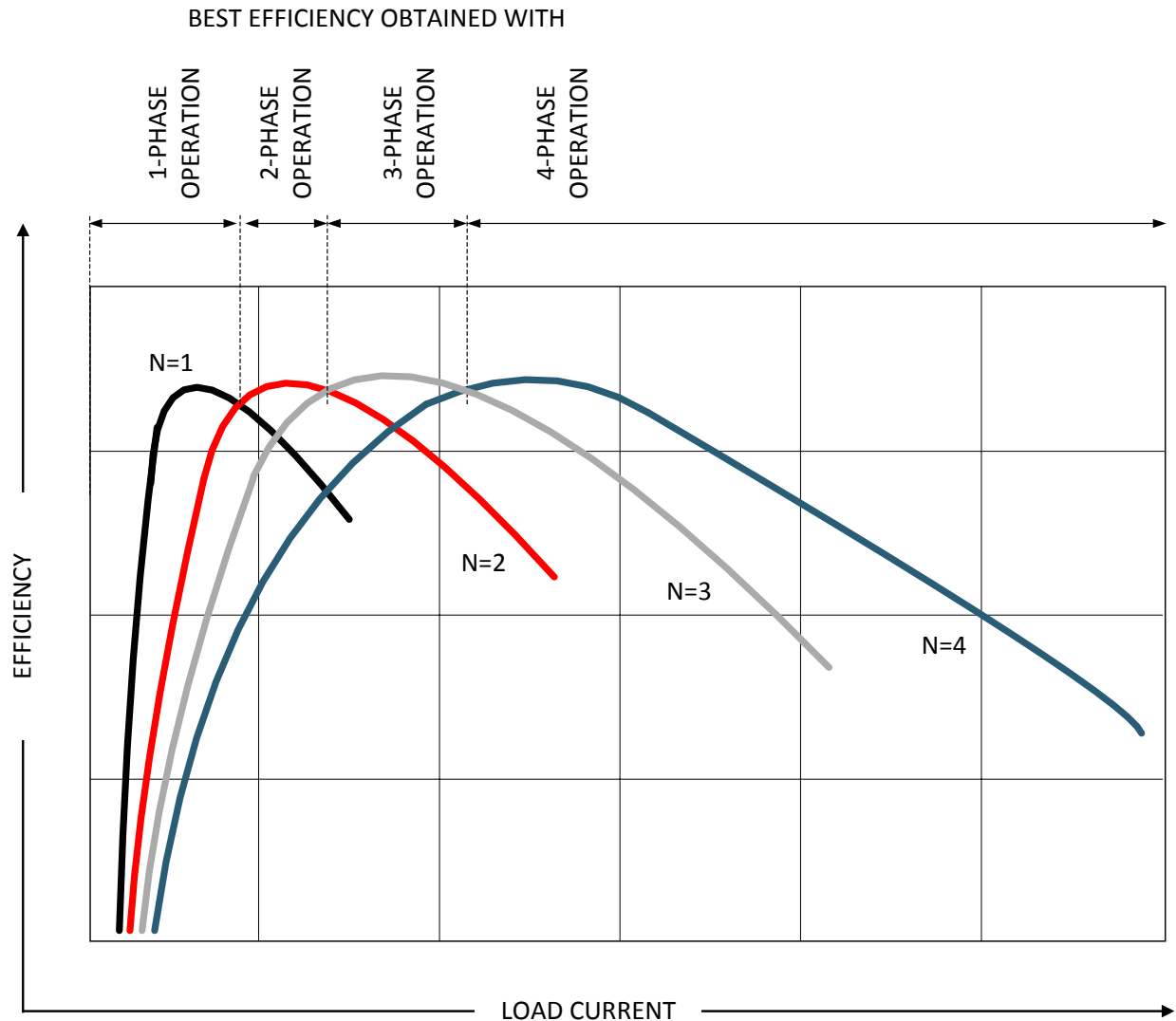
Figure 8. PWM Timings and Inductor Current Waveforms in 4-phase Configuration <sup>(1)</sup>

8.3.1.2 Multi-Phase Operation and Phase Adding/Shedding

Under heavy load conditions, the 4-phase converter switches each channel 90° apart. As a result, the 4-phase converter has an effective ripple frequency four times greater than the switching frequency of any one phase. However, the parallel operation decreases the efficiency at light load conditions. In order to overcome this operational inefficiency, the LP8758 can change the number of active phases to optimize efficiency for the variations of the load. This is called phase adding/shedding. The concept is illustrated below in Figure 9.

The converter can be forced to multi-phase operation by the BUCK0\_CTRL1.BUCK0\_FPWM\_MP bit. If the regulator operates in forced multi-phase mode the forced PWM operation is automatically used. If the multi-phase operation is not forced, the number of phases are added and shedded automatically to follow the required output current.

(1) Graph is not in scale and is for illustrative purposes only.

**Feature Description (continued)**


**Figure 9. Multi-Phase Buck Converter Efficiency vs Number of Phases - All Converters in PWM Mode <sup>(2)</sup>**

**8.3.1.3 Transition between PWM and PFM Modes**

Normal PWM mode operation with phase-adding or phase-shedding optimizes efficiency at mid-to-full load at the expense of light-load efficiency. The LP8758 converter operates in PWM mode at load current of about 400 mA or higher. At lighter load current levels the device automatically switches into PFM mode for reduced current consumption when Forced PWM mode is disabled (AUTO mode operation). By combining the PFM and the PWM modes a high efficiency is achieved over a wide output-load current range.

**8.3.1.4 Multi-phase Switcher Configurations**

In the multi-phase configuration the control of the multi-phase regulator settings is done using the control registers of the master buck. The following slave registers are ignored:

- BUCKx\_CTRL1
- BUCKx\_CTRL2, except ILIMx[2:0] bits
- interrupt bits related to the slave buck, except BUCKx\_ILIM\_INT

(2) Graph is not in scale and is for illustrative purposes only.

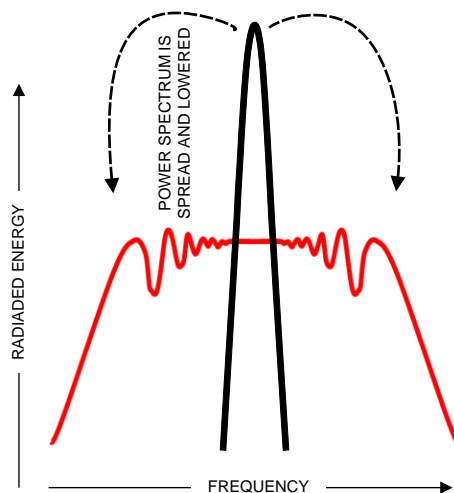
## Feature Description (continued)

### 8.3.1.5 Buck Converter Load Current Measurement

Buck load current can be monitored via I<sup>2</sup>C registers. The monitored buck converter is selected with the SEL\_I\_LOAD.LOAD\_CURRENT\_BUCK\_SELECT[1:0] register bits. A write to this selection register starts a current measurement sequence. The measurement sequence is typically 50  $\mu$ s long. The LP8758 device can be configured to give out an interrupt INT\_TOP.I\_LOAD\_READY after the load current measurement sequence is finished. Load current measurement interrupt can be masked with TOP\_MASK.I\_LOAD\_READY\_MASK bit. The measurement result can be read from registers I\_LOAD\_1 and I\_LOAD\_2. Register I\_LOAD\_1 bits BUCK\_LOAD\_CURRENT[7:0] give out the LSB bits and register I\_LOAD\_2 bits BUCK\_LOAD\_CURRENT[9:8] the MSB bits. The measurement result BUCK\_LOAD\_CURRENT[9:0] LSB is 20 mA, and maximum value of the measurement is 20.46 A. The measured current is the total value of the master and slave phases.

### 8.3.1.6 Spread-Spectrum Mode

Systems with periodic switching signals may generate a large amount of switching noise in a set of narrowband frequencies (the switching frequency and its harmonics). The usual solution to reduce noise coupling is to add EMI-filters and shields to the boards. The LP8758's register selectable spread-spectrum mode minimizes the need for output filters, ferrite beads, or chokes. In spread spectrum mode, the switching frequency varies randomly by  $\pm 5\%$  (depending on selected switching frequency) about the center frequency, reducing the EMI emissions radiated by the converter and associated passive components and PCB traces (see Figure 10). This feature is enabled with the CONFIG.EN\_SPREAD\_SPEC bit, and it affects all the buck cores.



Where a fixed frequency converter exhibits large amounts of spectral energy at the switching frequency, the spread spectrum architecture of the LP8758 spreads that energy over a large bandwidth.

**Figure 10. Spread-Spectrum Modulation**

### 8.3.2 Power-Up

The power-up sequence for the LP8758 is as follows:

- VANA (and VIN\_Bx) reach min recommended levels ( $V_{(VANA)} > VANA_{UVLO}$ ).
- NRST is set to high level. This initiates Power-On-Reset (POR), OTP reading and enables the system I/O interface. The I<sup>2</sup>C host should allow at least 700  $\mu$ s before writing or reading data to the LP8758.
- Device enters STANDBY-mode.
- The host can change the default register setting by I<sup>2</sup>C if needed.
- The regulator can be enabled/disabled by ENx pin(s) and by I<sup>2</sup>C interface.

### 8.3.3 Regulator Control

#### 8.3.3.1 Enabling and Disabling Regulator

The regulator can be enabled when the device is in STANDBY state. There are two ways for enable and disable the regulator:

**Feature Description (continued)**

- Using BUCK0\_CTRL1.EN\_BUCK0 register bit (BUCK0\_CTRL1.EN\_PIN\_CTRL0 register bit is '0').
- Using EN1/2 control pins (BUCK0\_CTRL1.EN\_BUCK0 register bit is '1' AND BUCK0\_CTRL1.EN\_PIN\_CTRL0 register bit is '1').

If the EN1/2 control pins are used for enable and disable then the delay from the control signal rising edge to startup is set by BUCK0\_DELAY.BUCK0\_STARTUP\_DELAY[3:0] bits and the delay from control signal falling edge to shutdown is set by BUCK0\_DELAY.BUCK0\_SHUTDOWN\_DELAY[3:0] bits. The delays are valid only for EN1/2 signal and not for control with BUCK0\_CTRL1.EN\_BUCK0 bit.

The control of the regulator (with 0 ms delays) is shown in [Table 1](#). The multi-phase regulator is controlled with registers of the master phase.

**Table 1. Regulator Control**

CONTROL METHOD	ROW	EN_BUCKx0	BUCK0_CTRL1 EN_PIN_CTRL0	BUCK0_CTRL1 EN_PIN_SELECT0	BUCK0_CTRL1 EN_ROOF_FLOOR0	EN1 PIN	EN2 PIN	BUCK0 OUTPUT VOLTAGE
Enable/disable control with EN_BUCK0 bit	1	0	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Disabled
	2	1	0	Don't Care	Don't Care	Don't Care	Don't Care	BUCK0_VOUT.BUCK0_VSET[7:0]
Enable/disable control with EN1 pin	3	1	1	0	0	Low	Don't Care	Disabled
	4	1	1	0	0	High	Don't Care	BUCK0_VOUT.BUCK0_VSET[7:0]
Enable/disable control with EN2 pin	5	1	1	1	0	Don't Care	Low	Disabled
	6	1	1	1	0	Don't Care	High	BUCK0_VOUT.BUCK0_VSET[7:0]
Roof/floor control with EN1 pin	7	1	1	0	1	Low	Don't Care	BUCK0_FLOOR_VOUT.BUCK0_FLOOR_VSET[7:0]
	8	1	1	0	1	High	Don't Care	BUCK0_VOUT.BUCK0_VSET[7:0]
Roof/floor control with EN2 pin	9	1	1	1	1	Don't Care	Low	BUCK0_FLOOR_VOUT.BUCK0_FLOOR_VSET[7:0]
	10	1	1	1	1	Don't Care	High	BUCK0_VOUT.BUCK0_VSET[7:0]

The following configuration allows the enable/disable control using ENx pin:

- BUCK0\_CTRL1.EN\_BUCK0 = 1
- BUCK0\_CTRL1.EN\_PIN\_CTRL0 = 1
- BUCK0\_CTRL1.EN\_ROOF\_FLOOR0 = 0
- BUCK0\_VOUT.BUCK0\_VSET[7:0] = Required voltage when ENx is high
- The enable pin for control is selected with BUCK0\_CTRL1.EN\_PIN\_SELECT0

When the ENx pin is low, [Table 1](#) row 3 (or 5) is valid, and the regulator is disabled. By setting ENx pin high, [Table 1](#) row 4 (or 6) is valid, and the regulator is enabled with required voltage.

If the regulator is enabled all the time, and the ENx pin controls selection between two voltage level, the following configuration is used:

- BUCK0\_CTRL1.EN\_BUCK0 = 1
- BUCK0\_CTRL1.EN\_PIN\_CTRL0 = 1
- BUCK0\_CTRL1.EN\_ROOF\_FLOOR0 = 1
- BUCK0\_VOUT.BUCK0\_VSET[7:0] = Required voltage when ENx is high
- The enable pin for control is selected with BUCK0\_CTRL1.EN\_PIN\_SELECT0

When the ENx pin is low, [Table 1](#) row 7(or 9) is valid, and the regulator is enabled with a voltage defined by BUCK0\_FLOOR\_VOUT.BUCK0\_FLOOR\_VSET[7:0] bits. Setting the ENx pin high, [Table 1](#) row 8 (or 10) is valid, and the regulator is enabled with a voltage defined by BUCK0\_VOUT.BUCK0\_VSET[7:0] bits.

If the regulator is controlled by I<sup>2</sup>C writings, the BUCK0\_CTRL1.EN\_PIN\_CTRL0 bit is set to 0. The enable/disable is controlled by the BUCK0\_CTRL1.EN\_BUCK0 bit, and when the regulator is enabled, the output voltage is defined by the BUCK0\_VOUT.BUCK0\_VSET[7:0] bits. The [Table 1](#) rows 1 and 2 are valid for I<sup>2</sup>C controlled operation (ENx pins are ignored).

The regulator is enabled by the ENx pin or by I<sup>2</sup>C writing as shown in Figure 11. The soft-start circuit limits the in-rush current during start-up. Output voltage increase rate is around 30 mV/μsec during soft-start. When the output voltage rises to approximately 0.3 V, the output voltage becomes slew-rate controlled. If there is a short circuit at the output, and the output voltage does not increase above a 0.35-V level in 1 ms, the regulator is disabled, and interrupt is set. When the output voltage reaches the powergood threshold level the INT\_BUCK\_0\_1.BUCK0\_PG\_INT interrupt flag is set. The powergood interrupt flag can be masked using BUCK\_0\_1\_MASK.BUCK0\_PG\_MASK bit.

The ENx input pins have integrated pull-down resistors. The pull-down resistors are enabled by default and host can disable those with CONFIG.ENx\_PD bits.

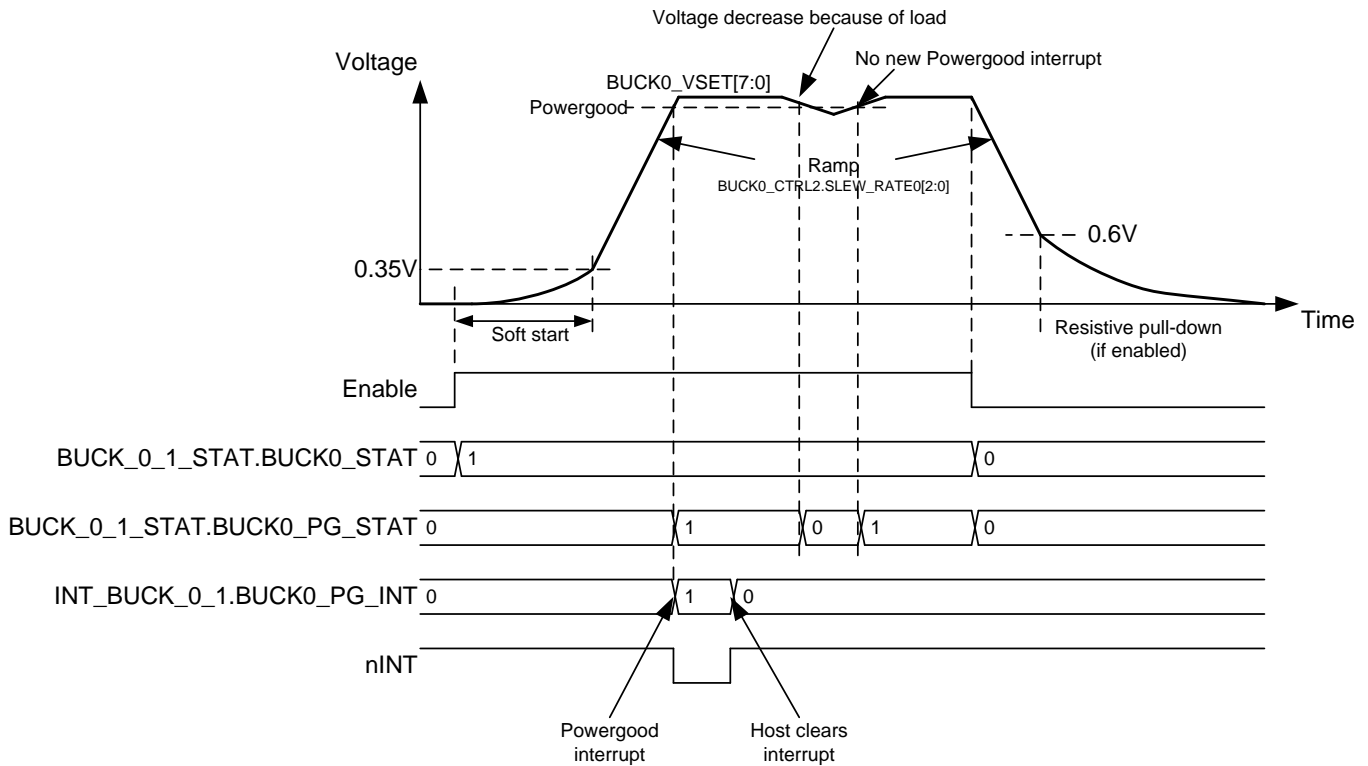


Figure 11. Regulator Enable and Disable

### 8.3.3.2 Changing Output Voltage

The regulator's output voltage can be changed by the ENx pin (voltage levels defined by the BUCK0\_VOUT and BUCK0\_FLOOR\_VOUT registers) or by writing to the BUCK0\_VOUT and BUCK0\_FLOOR\_VOUT registers. The voltage change is always slew-rate controlled, and the slew-rate is defined by the BUCKx\_CTRL2.SLEW\_RATE[2:0] bits. During voltage change the Forced PWM mode is used automatically. If the multi-phase operation is forced by the BUCK0\_CTRL1.BUCK0\_FPWM\_MP bit, the regulator operates in multi-phase mode (four phases active). If the multi-phase operation is not forced, the number of phases are added and shedded automatically to follow the required slew rate. When the programmed output voltage is achieved, the mode becomes the one defined by load current, and the BUCK0\_CTRL1.BUCK0\_FPWM and BUCK0\_CTRL1.BUCK0\_FPWM\_MP bits.

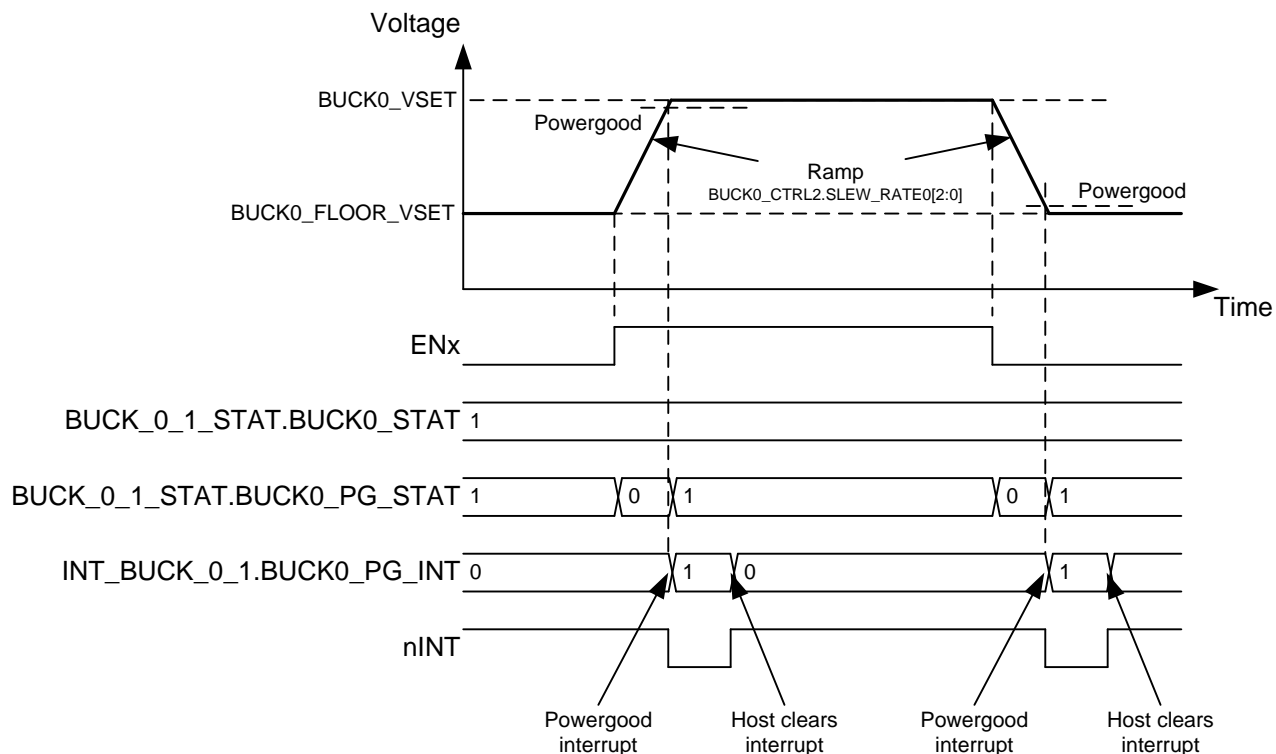


Figure 12. Regulator Output Voltage Change

### 8.3.4 Device Reset Scenarios

There are three reset methods implemented on the LP8758:

- Software reset with `RESET.SW_RESET` register bit
- Reset from low logic level of `NRST` signal
- Undervoltage lockout (UVLO) reset from `VANA` supply

An SW reset occurs when `RESET.SW_RESET` bit is written '1'. The bit is automatically cleared after writing. This event disables the regulator immediately, resets all the register bits to the default values and OTP bits are loaded (see Figure 14). I<sup>2</sup>C interface is not reset during software reset.

If `VANA` supply voltage falls below UVLO threshold level or `NRST` signal is set low, then the regulator is disabled immediately, and all the register bits are reset to the default values. When the `VANA` supply voltage is above UVLO threshold level and `NRST` signal rises above threshold level an internal power-on reset (POR) occurs. OTP bits are loaded to the registers, and a start-up is initiated according to the register settings.

### 8.3.5 Diagnosis and Protection Features

The LP8758 is capable of providing three levels of protection features:

- Warnings for diagnosis which sets interrupt;
- Protection events which are disabling the regulator; and
- Faults which are causing the device to shutdown.

When the device detects warning/protection condition(s), the LP8758 sets the flag bits indicating what protection or warning conditions have occurred, and the `nINT` pin will be pulled low. `nINT` will be released again after a clear of flags is complete. The `nINT` signal stays low until all the pending interrupts are cleared.

When a fault is detected, it is indicated by a `INT_TOP.RESET_REG` interrupt flag after next start-up.

**Table 2. Summary of Interrupt Signals**

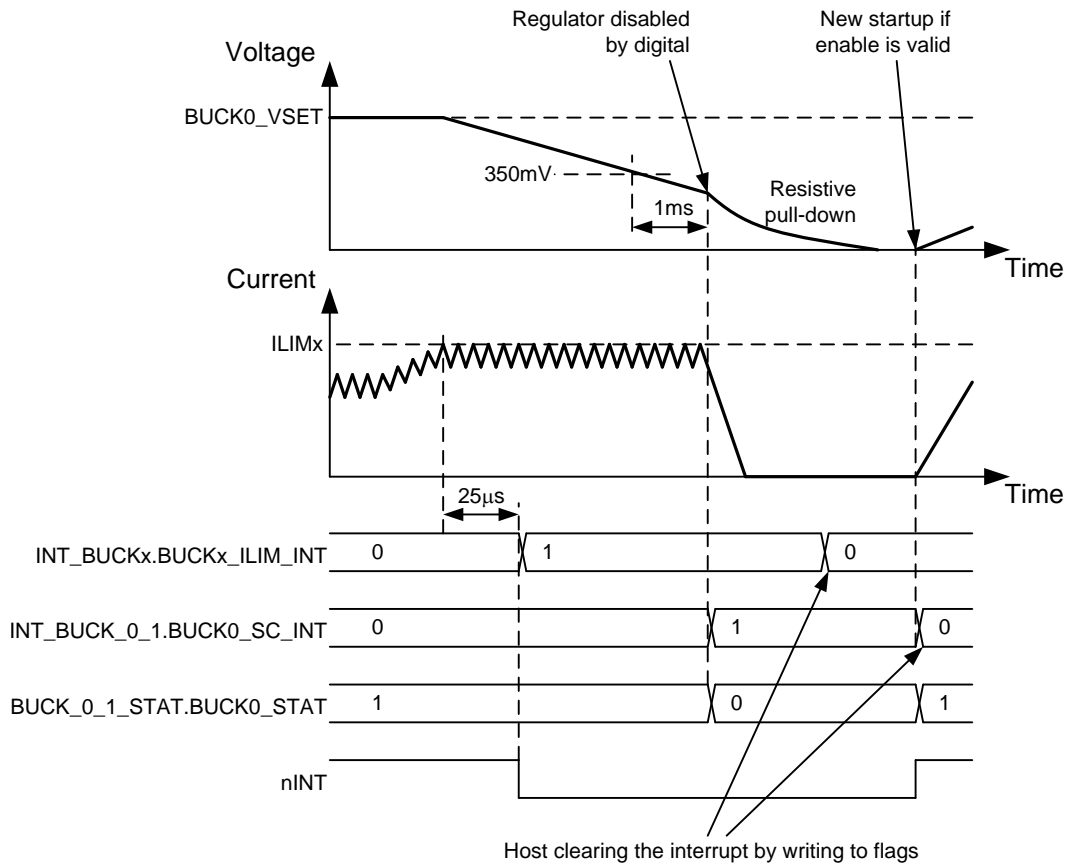
EVENT	RESULT	INTERRUPT REGISTER AND BIT	INTERRUPT MASK	STATUS BIT	RECOVERY / INTERRUPT CLEAR
Current limit triggered (20 $\mu$ s debounce)	No effect	INT_TOP.INT_BUCKx = 1 INT_BUCKx.BUCKx_ILIM_INT = 1	BUCKx_MASK.BUCKx_ILIM_MASK	BUCKx_STAT.BUCKx_ILIM_STAT	Write 1 to INT_BUCKx.BUCKx_ILIM_INT bit Interrupt is not cleared if current limit is active
Short circuit ( $V_{OUT} < 0.35$ V at 1 ms after enable) or Overload ( $V_{OUT}$ decreasing below 0.35V during operation, 1 ms debounce)	Regulator disable	INT_TOP.INT_BUCK0 = 1 INT_BUCK_0_1.BUCK0_SC_INT = 1	N/A	N/A	Write 1 to INT_BUCK_0_1.BUCK0_SC_INT bit
Thermal Warning	No effect	INT_TOP.TDIE_WARN = 1	TOP_MASK.TDIE_WARN_MASK	TOP_STAT.TDIE_WARN_STAT	Write 1 to INT_TOP.TDIE_WARN bit Interrupt is not cleared if temperature is above thermal warning level
Thermal Shutdown	Regulator disabled	INT_TOP.TDIE_SD = 1	N/A	TOP_STAT.TDIE_SD_STAT	Write 1 to INT_TOP.TDIE_SD bit Interrupt is not cleared if temperature is above thermal shutdown level
Powergood, output voltage reaches the programmed value	No effect	INT_TOP.INT_BUCK0 = 1 INT_BUCK_0_1.BUCK0_PG_INT = 1	BUCK_0_1_MASK.BUCK0_PG_MASK	BUCK_0_1_STAT.BUCK0_PG_STAT	Write 1 to INT_BUCK_0_1.BUCK0_PG_INT bit
Load current measurement ready	No effect	INT_TOP.I_LOAD_READY = 1	TOP_MASK.I_LOAD_READY_MASK	N/A	Write 1 to INT_TOP.I_LOAD_READY bit
Start-up (NRST rising edge)	Device ready for operation, registers reset to default values	INT_TOP.RESET_REG = 1	TOP_MASK.RESET_REG_MASK	N/A	Write 1 to INT_TOP.RESET_REG bit
Glitch on supply voltage and UVLO triggered (VANA falling and rising)	Immediate shutdown followed by powerup, registers reset to default values	INT_TOP.RESET_REG = 1	TOP_MASK.RESET_REG_MASK	N/A	Write 1 to INT_TOP.RESET_REG bit
Software requested reset	Immediate shutdown followed by powerup, registers reset to default values	INT_TOP.RESET_REG = 1	TOP_MASK.RESET_REG_MASK	N/A	Write 1 to INT_TOP.RESET_REG bit

### 8.3.5.1 Warnings for Diagnosis (Interrupt)

#### 8.3.5.1.1 Output Current Limit

The buck regulators have programmable output peak current limits. The limits are individually programmed for all buck regulators with BUCKx\_CTRL2.ILIMx[2:0] bits. The current limit settings of master and slave regulators used for the same output voltage rail must be identical. If the load current is increased so that the current limit is triggered, the regulator continues to regulate to the limit current level (current peak regulation). The voltage may decrease if the load current is higher than limit current. If the current regulation continues for 20  $\mu$ s, the LP8758 device sets the INT\_BUCKx.BUCKx\_ILIM\_INT bit and pulls the nINT pin low. The host processor can read BUCKx\_STAT.BUCKx\_ILIM\_STAT bits to see if the regulator is still in peak current regulation mode.

If the load is so high that the output voltage decreases below a 350-mV level, the LP8758 device disables the regulator and sets the INT\_BUCK\_0\_1.BUCK0\_SC\_INT bit. In addition the BUCK\_0\_1\_STAT.BUCK0\_STAT bit is set to 0. The interrupt is cleared when the host processor writes 1 to INT\_BUCK\_0\_1.BUCK0\_SC\_INT bit. The overload situation is shown in [Figure 13](#).



**Figure 13. Overload Situation**

### 8.3.5.1.2 Thermal Warning

The LP8758 device includes protection feature against over-temperature by setting an interrupt for host processor. The threshold level of the thermal warning is selected with CONFIG.TDIE\_WARN\_LEVEL bit.

If the LP8758 device temperature increases above thermal warning level the device sets INT\_TOP.TDIE\_WARN bit and pulls nINT pin low. The status of the thermal warning can be read from TOP\_STAT.TDIE\_WARN\_STAT bit and the interrupt is cleared by writing 1 to INT\_TOP.TDIE\_WARN bit.

### 8.3.5.2 Protection (Regulator Disable)

If the regulator is disabled because of protection or fault (short-circuit protection, overload protection, thermal shutdown, or undervoltage lockout), the output power FETs are set to high-impedance mode, and the output pull-down resistor is enabled (if enabled with BUCKx\_CTRL1.EN\_RDISx bits). The turn-off time of the output voltage is defined by the output capacitance, load current, and the resistance of the integrated pulldown resistor.

#### 8.3.5.2.1 Short-Circuit and Overload Protection

A short-circuit protection feature allows the LP8758 to protect itself and external components against short circuit at the output or against overload during start-up. The fault threshold is 350 mV, and the protection is triggered, and the regulator disabled, if the output voltage is below the threshold level 1 ms after the regulator is enabled.

In a similar way the overload situation is protected during normal operation. If the regulator's feedback-pin voltage falls below 0.35 V, and remains below the threshold level for 1 ms, the regulator is disabled.

In the short-circuit and overload situations the INT\_BUCK\_0\_1.BUCK0\_SC\_INT and the INT\_TOP.INT\_BUCK0 bits are set to 1, the BUCK\_0\_1\_STAT.BUCK0\_STAT bit is set to 0 and the nINT signal is pulled low. The host processor clears the interrupt by writing 1 to the INT\_BUCK\_0\_1.BUCK0\_SC\_INT bit. Upon clearing the interrupt the regulator makes a new start-up attempt if the enable register bits and/or ENx control signal is valid.

### 8.3.5.2.2 Thermal Shutdown

The LP8758 has an overtemperature protection function that operates to protect itself from short-term misuse and overload conditions. When the junction temperature exceeds around 150°C, the regulator is disabled, the INT\_TOP.TDIE\_SD bit is set to 1, the nINT signal is pulled low, and the device enters STANDBY. nINT will be cleared by writing 1 to the INT\_TOP.TDIE\_SD bit. If the temperature is above thermal shutdown level the interrupt is not cleared. The host can read the status of the thermal shutdown from the TOP\_STAT.TDIE\_SD\_STAT bit. Regulator cannot be enabled as long as the junction temperature is above thermal shutdown level or the thermal shutdown interrupt is pending.

### 8.3.5.3 Fault (Power Down)

#### 8.3.5.3.1 Undervoltage Lockout

When the input voltage falls below  $V_{ANA_{UVLO}}$  at the VANA pin, the buck converters are disabled immediately, and the output capacitor is discharged using the pulldown resistor and the LP8758 device enters SHUTDOWN. When VANA voltage is above UVLO threshold level and NRST signal is high, the device powers up to STANDBY state.

If the reset interrupt is unmasked by default ( $TOP\_MASK.RESET\_REG\_MASK = 0$ ) the INT\_TOP.RESET\_REG interrupt indicates that the device has been in SHUTDOWN. The host processor must clear the interrupt by writing 1 to the INT\_TOP.RESET\_REG bit. If the host processor reads the INT\_TOP.RESET\_REG flag after detecting an nINT low signal, it knows that the input supply voltage has been below UVLO level (or the host has requested reset), and the registers are reset to default values.

### 8.3.6 Digital Signal Filtering

The digital signals have a debounce filtering. The signal/supply is sampled with a clock signal and a counter. This results as an accuracy of one clock period for the debounce window.

**Table 3. Digital Signal Filtering**

EVENT	SIGNAL / SUPPLY	RISING EDGE LENGTH	FALLING EDGE LENGTH
Enable/Disable/Voltage Select for BUCK0	EN1	3µs <sup>(1)</sup>	3µs <sup>(1)</sup>
Enable/Disable/Voltage Select for BUCK0	EN2	3µs <sup>(1)</sup>	3µs <sup>(1)</sup>
VANA undervoltage lockout	VANA	Immediate	Immediate
Thermal warning	TDIE_WARN	20 µs	20 µs
Thermal shutdown	TDIE_SD	20 µs	20 µs
Current limit	VOUTx_ILIM	20 µs	20 µs
Overload	FB_B0 - FB_B1, FB_B2 - FB_F3	1 ms	1 ms
Powergood	FB_B0 - FB_B1, FB_B2 - FB_F3	20 µs	20 µs

(1) No glitch filtering, only synchronization.

## 8.4 Device Functional Modes

### 8.4.1 Modes of Operation

**SHUTDOWN:** The  $V_{(NRST)}$  voltage is below threshold level. All switch, reference, control and bias circuitry of the LP8758 device are turned off.

**WAIT-ON:** The  $V_{(NRST)}$  voltage is above threshold level. The reference and bias circuitry are enabled. The regulator of the LP8758 device is turned off.

**READ OTP:** The main supply voltage  $V_{(VANA)}$  is above  $V_{ANA_{UVLO}}$  level and  $V_{(NRST)}$  voltage is above threshold level. The regulator is disabled and the reference and bias circuitry of the LP8758 are enabled. The OTP bits are loaded to registers.

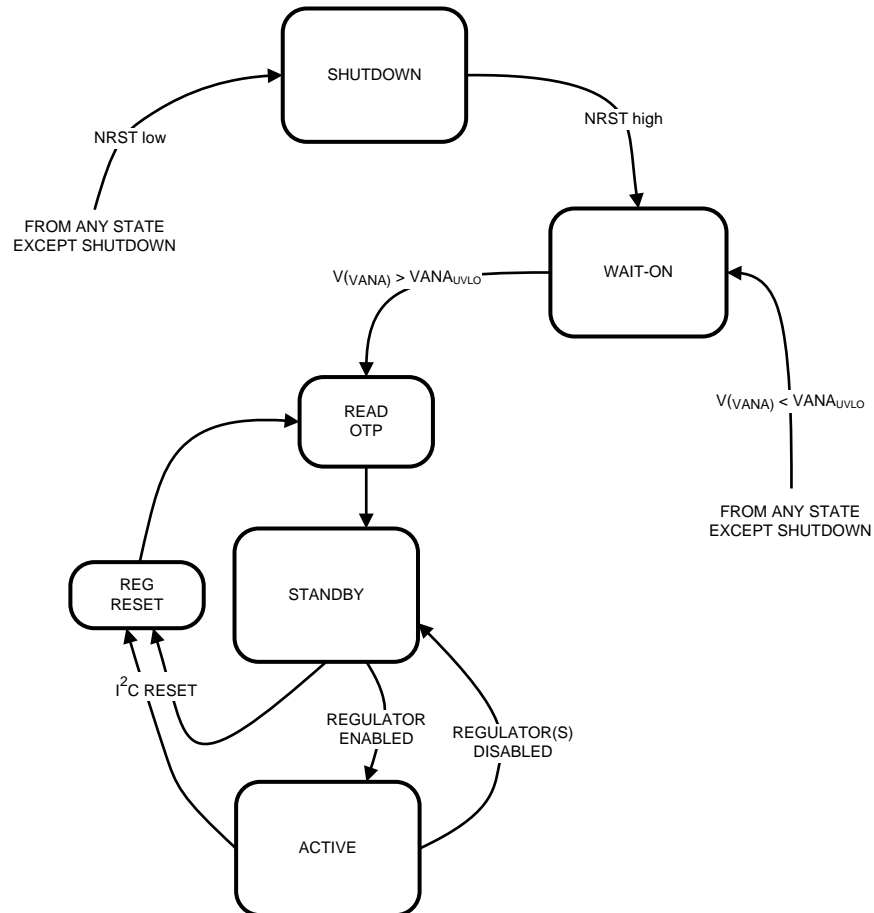
**STANDBY:** The main supply voltage  $V_{(VANA)}$  is above  $V_{ANA_{UVLO}}$  level and  $V_{(NRST)}$  voltage is above threshold level. The regulator is disabled and the reference, control and bias circuitry of the LP8758 are

**Device Functional Modes (continued)**

enabled. All registers can be read or written by the host processor via the system serial interface. The regulator can be enabled if needed.

**ACTIVE:** The main supply voltage  $V_{(VANA)}$  is above  $VANA_{UVLO}$  level and  $V_{(NRST)}$  voltage is above threshold level. At least one regulated DC-DC converter is enabled. All registers can be read or written by the host processor via the system serial interface.

The operating modes and transitions between the modes are shown in [Figure 14](#).



**Figure 14. Device Operation Modes**

## 8.5 Programming

### 8.5.1 I<sup>2</sup>C-Compatible Interface

The I<sup>2</sup>C-compatible synchronous serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the devices connected to the bus. The two interface lines are the Serial Data Line (SDA), and the Serial Clock Line (SCL). Every device on the bus is assigned a unique address and acts as either a Master or a Slave depending on whether it generates or receives the serial clock SCL. The SCL and SDA lines should each have a pullup resistor placed somewhere on the line and remain HIGH even when the bus is idle. The LP8758 supports standard mode (100 kHz), fast mode (400 kHz), fast mode plus (1 MHz), and high-speed mode (3.4 MHz).

#### 8.5.1.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, the state of the data line can only be changed when clock signal is LOW.

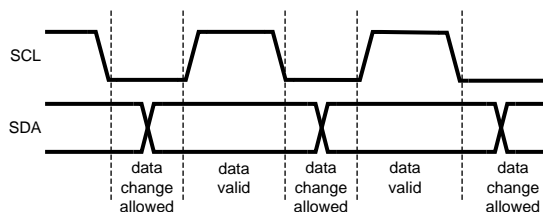


Figure 15. Data Validity Diagram

#### 8.5.1.2 Start and Stop Conditions

The LP8758 is controlled via an I<sup>2</sup>C-compatible interface. START and STOP conditions classify the beginning and end of the I<sup>2</sup>C session. A START condition is defined as SDA transitions from HIGH to LOW while SCL is HIGH. A STOP condition is defined as SDA transition from LOW to HIGH while SCL is HIGH. The I<sup>2</sup>C master always generates the START and STOP conditions.

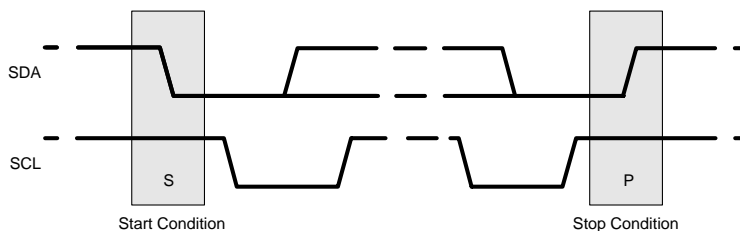
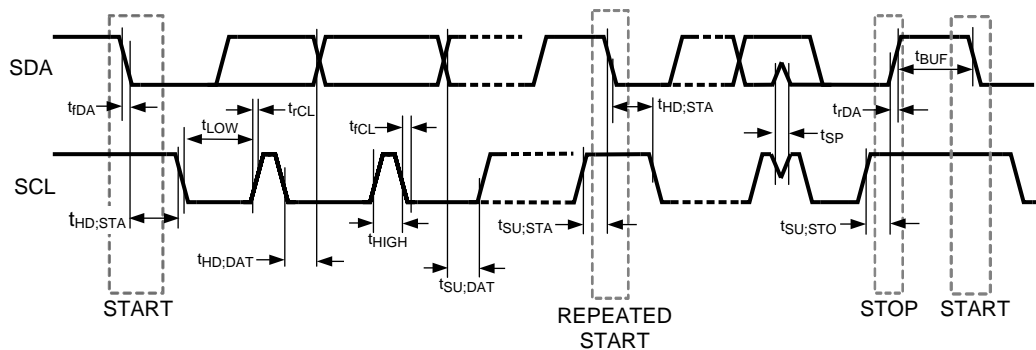


Figure 16. Start and Stop Sequences

The I<sup>2</sup>C bus is considered busy after a START condition and free after a STOP condition. During data transmission the I<sup>2</sup>C master can generate repeated START conditions. A START and a repeated START condition are equivalent function-wise. The data on SDA must be stable during the HIGH period of the clock signal (SCL). In other words, the state of SDA can only be changed when SCL is LOW. [Figure 17](#) shows the SDA and SCL signal timing for the I<sup>2</sup>C-Compatible Bus. See the [I<sup>2</sup>C Serial Bus Timing Parameter](#) for timing values.

**Programming (continued)**



**Figure 17. I<sup>2</sup>C-Compatible Timing**

**8.5.1.3 Transferring Data**

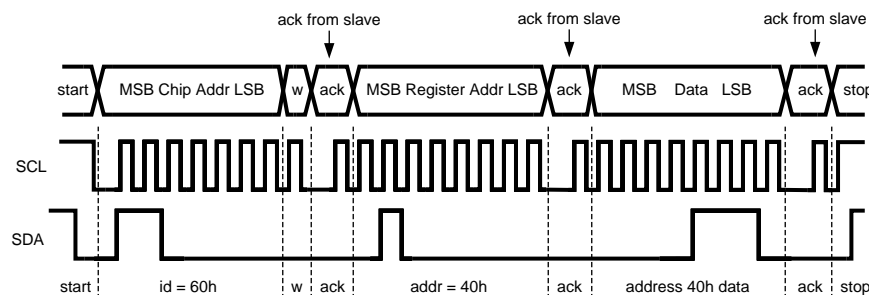
Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the acknowledge clock pulse. The LP8758 pulls down the SDA line during the 9th clock pulse, signifying an acknowledge. The LP8758 generates an acknowledge after each byte has been received.

There is one exception to the “acknowledge after every byte” rule. When the master is the receiver, it must indicate to the transmitter an end of data by not-acknowledging (“negative acknowledge”) the last byte clocked out of the slave. This “negative acknowledge” still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

**NOTE**

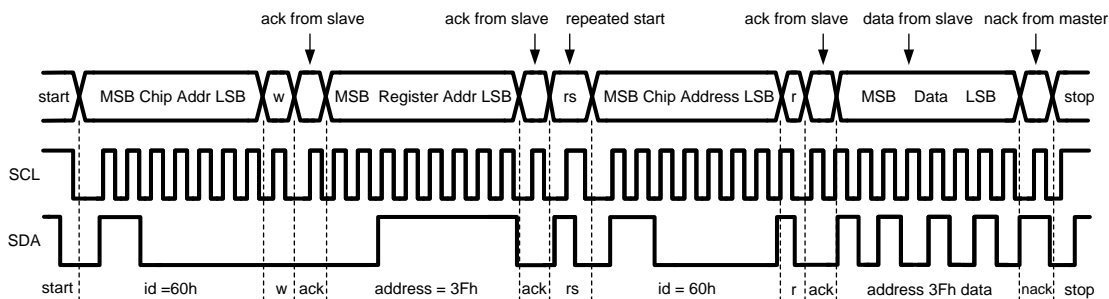
If the NRST signal is low during I<sup>2</sup>C communication the LP8758 device does not drive SDA line. The ACK signal and data transfer to the master is disabled at that time.

After the START condition, the bus master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (READ or WRITE). For the eighth bit, a “0” indicates a WRITE and a “1” indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.



**Figure 18. Write Cycle (w = write; SDA = '0'), id = Device Address = 60Hex for LP8758**

Programming (continued)

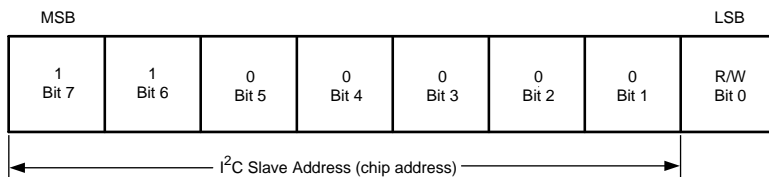


When READ function is to be accomplished, a WRITE function must precede the READ function as shown above.

Figure 19. Read Cycle ( r = read; SDA = '1'), id = Device Address = 60Hex for LP8758

8.5.1.4 I<sup>2</sup>C-Compatible Chip Address

The device address for the LP8758 is 0x60. After the START condition, the I<sup>2</sup>C master sends the 7-bit address followed by an eighth bit, read or write (R/W). R/W = 0 indicates a WRITE and R/W = 1 indicates a READ. The second byte following the device address selects the register address to which the data will be written. The third byte contains the data for the selected register.



Here device address is 110 0000Bin = 60Hex.

Figure 20. Device Address

8.5.1.5 Auto Increment Feature

The auto-increment feature allows writing several consecutive registers within one transmission. Every time an 8-bit word is sent to the LP8758, the internal address index counter will be incremented by one and the next register will be written. Table 4 below shows writing sequence to two consecutive registers. Note that the auto-increment feature does not work for read.

Table 4. Auto-Increment Example

Master Action	Start	Device Address = 60H	Write		Register Address		Data		Data		Stop
LP8758 Action				ACK		ACK		ACK		ACK	

## 8.6 Register Maps

### 8.6.1 Register Descriptions

The LP8758 is controlled by a set of registers through the system serial interface port. The device registers, their addresses and their abbreviations are listed in [Table 5](#). A more detailed description is given in sections [DEV\\_REV](#) to [I\\_LOAD\\_1](#).

**Table 5. Summary of LP8758 Control Registers**

Addr	Register	Read / Write	D7	D6	D5	D4	D3	D2	D1	D0	
0x00	DEV_REV	R	DEVICE_ID[1:0]		ALL_LAYER[1:0]		METAL_LAYER[3:0]				
0x01	OTP_REV	R	OTP_ID[7:0]								
0x02	BUCK0_CTRL1	R/W	EN_BUCK0	EN_PIN_CTRL0	EN_PIN_SELECT0	EN_ROOF_FLOOR0	EN_RDIS0	Reserved	BUCK0_FPWM	BUCK0_FPWM_MP	
0x03	BUCK0_CTRL2	R/W	Reserved		ILIM0[2:0]		SLEW_RATE0[2:0]				
0x05	BUCK1_CTRL2	R/W	Reserved		ILIM1[2:0]		Reserved				
0x07	BUCK2_CTRL2	R/W	Reserved		ILIM2[2:0]		Reserved				
0x09	BUCK3_CTRL2	R/W	Reserved		ILIM3[2:0]		Reserved				
0x0A	BUCK0_VOUT	R/W	BUCK0_VSET[7:0]								
0x0B	BUCK0_FLOOR_VOUT	R/W	BUCK0_FLOOR_VSET[7:0]								
0x12	BUCK0_DELAY	R/W	BUCK0_SHUTDOWN_DELAY[3:0]				BUCK0_STARTUP_DELAY[3:0]				
0x16	RESET	R/W	Reserved								SW_RESET
0x17	CONFIG	R/W	Reserved				TDIE_WARN_LEVEL	EN2_PD	EN1_PD	EN_SPREAD_SPEC	
0x18	INT_TOP	R/W	INT_BUCK3	INT_BUCK2	INT_BUCK1	INT_BUCK0	TDIE_SD	TDIE_WARN	RESET_REG	I_LOAD_READY	
0x19	INT_BUCK_0_1	R/W	Reserved			BUCK1_ILIM_INT	Reserved	BUCK0_PG_INT	BUCK0_SC_INT	BUCK0_ILIM_INT	
0x1A	INT_BUCK_2_3	R/W	Reserved			BUCK3_ILIM_INT	Reserved			BUCK2_ILIM_INT	
0x1B	TOP_STAT	R	Reserved				TDIE_SD_STAT	TDIE_WARN_STAT	Reserved		
0x1C	BUCK_0_1_STAT	R	Reserved			BUCK1_ILIM_STAT	BUCK0_STAT	BUCK0_PG_STAT	Reserved	BUCK0_ILIM_STAT	
0x1D	BUCK_2_3_STAT	R	Reserved			BUCK3_ILIM_STAT	Reserved			BUCK2_ILIM_STAT	
0x1E	TOP_MASK	R/W	Reserved					TDIE_WARN_MASK	RESET_REG_MASK	I_LOAD_READY_MASK	
0x1F	BUCK_0_1_MASK	R/W	Reserved			BUCK1_ILIM_MASK	Reserved	BUCK0_PG_MASK	Reserved	BUCK0_ILIM_MASK	
0x20	BUCK_2_3_MASK	R/W	Reserved			BUCK3_ILIM_MASK	Reserved			BUCK2_ILIM_MASK	
0x21	SEL_I_LOAD	R/W	Reserved							LOAD_CURRENT_BUCK_SELECT[1:0]	
0x22	I_LOAD_2	R/W	Reserved							BUCK_LOAD_CURRENT[9:8]	
0x23	I_LOAD_1	R/W	BUCK_LOAD_CURRENT[7:0]								

### 8.6.1.1 DEV\_REV

Address: 0x00

D7		D6		D5		D4		D3		D2		D1		D0	
DEVICE_ID[1:0]				ALL_LAYER[1:0]				METAL_LAYER[3:0]							
Bits	Field	Type	Default	Description											
7:6	DEVICE_ID[1:0]	R	00	Device specific ID code.											
5:4	ALL_LAYER[1:0]	R	00	Shows the all layer version of the device: 00 - First all layer version 01 - Second all layer version 10 - Third all layer version 11 - Fourth all layer version											
3:0	METAL_LAYER [3:0]	R	0001	Shows the metal layer version of the device: 0000 - All layer version 0001 - First metal layer spin ... 1111 - 15 <sup>th</sup> metal layer spin											

### 8.6.1.2 OTP\_REV

Address: 0x01

D7		D6		D5		D4		D3		D2		D1		D0	
OTP_ID[7:0]															
Bits	Field	Type	Default	Description											
7:0	OTP_ID[7:0]	R	1011 0000	Identification Code of the OTP EPROM Version.											

### 8.6.1.3 BUCK0\_CTRL1

Address: 0x02

D7		D6		D5		D4		D3		D2		D1		D0	
EN_BUCK0		EN_PIN_CTRL0		EN_PIN_SELECT0		EN_ROOF_FLOOR0		EN_RDIS0		Reserved		BUCK0_FPWM		BUCK0_FPWM_MP	
Bits	Field	Type	Default	Description											
7	EN_BUCK0	R/W	1	Enable BUCK0 regulator: 0 - BUCK0 regulator is disabled 1 - BUCK0 regulator is enabled.											
6	EN_PIN_CTRL0	R/W	1	Enable EN1/2 pin control for BUCK0: 0 - only EN_BUCK0 bit controls BUCK0 1 - EN_BUCK0 bit AND EN1/2 pin control BUCK0.											
5	EN_PIN_SELECT0	R/W	0	Select which ENx pin controls BUCK0 if EN_PIN_CTRL0 = 1: 0 - EN1 pin 1 - EN2 pin.											
4	EN_ROOF_FLOOR0	R/W	0	Enable Roof/Floor control of EN1/2 pin if EN_PIN_CTRL0 = 1: 0 - Enable/Disable (1/0) control 1 - Roof/Floor (1/0) control.											
3	EN_RDIS0	R/W	1	Enable output discharge resistor when BUCK0 is disabled: 0 - Discharge resistor disabled 1 - Discharge resistor enabled.											
2	Reserved	R/W	0												
1	BUCK0_FPWM	R/W	0	Forces the BUCK0 regulator to operate in PWM mode: 0 - Automatic transitions between PFM and PWM modes (AUTO mode). 1 - Forced to PWM operation.											
0	BUCK0_FPWM_MP	R/W	0	Forces the BUCK0 regulator to operate always in multi-phase and forced PWM operation mode: 0 - Automatic phase adding and shedding. 1 - Forced to multi-phase operation, 2 phases in the 2-phase configuration, 3 phases in the 3-phase configuration and 4 phases in the 4-phase configuration.											

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**8.6.1.4 BUCK0\_CTRL2**

Address: 0x03

D7		D6		D5		D4		D3		D2		D1		D0	
Reserved				ILIM0[2:0]				SLEW_RATE0[2:0]							
Bits	Field	Type	Default	Description											
7:6	Reserved	R/W	00												
5:3	ILIM0[2:0]	R/W	111	Sets the switch current limit of BUCK0. Can be programmed at any time during operation: 000 - 1.5 A 001 - 2.0 A 010 - 2.5 A 011 - 3.0 A 100 - 3.5 A 101 - 4.0 A 110 - 4.5 A 111 - 5.0 A (Default)											
2:0	SLEW_RATE0[2:0]	R/W	010	Sets the output voltage slew rate for BUCK0 regulator (rising and falling edges): 000 - 30 mV/μs 001 - 15 mV/μs 010 - 10 mV/μs (Default) 011 - 7.5 mV/μs 100 - 3.8 mV/μs 101 - 1.9 mV/μs 110 - 0.94 mV/μs 111 - 0.47 mV/μs											

**8.6.1.5 BUCK1\_CTRL2**

Address: 0x05

D7		D6		D5		D4		D3		D2		D1		D0	
Reserved				ILIM1[2:0]				Reserved							
Bits	Field	Type	Default	Description											
7:6	Reserved	R/W	00												
5:3	ILIM1[2:0]	R/W	111	Sets the switch current limit of BUCK1. Can be programmed at any time during operation: 000 - 1.5 A 001 - 2.0 A 010 - 2.5 A 011 - 3.0 A 100 - 3.5 A 101 - 4.0 A 110 - 4.5 A 111 - 5.0 A (Default)											
2:0	Reserved	R/W	010												

### 8.6.1.6 BUCK2\_CTRL2

Address: 0x07

D7		D6		D5		D4		D3		D2		D1		D0	
Reserved				ILIM2[2:0]				Reserved							
Bits	Field	Type	Default	Description											
7:6	Reserved	R/W	00												
5:3	ILIM2[2:0]	R/W	111	Sets the switch current limit of BUCK2. Can be programmed at any time during operation: 000 - 1.5 A 001 - 2.0 A 010 - 2.5 A 011 - 3.0 A 100 - 3.5 A 101 - 4.0 A 110 - 4.5 A 111 - 5.0 A (Default)											
2:0	Reserved	R/W	010												

### 8.6.1.7 BUCK3\_CTRL2

Address: 0x09

D7		D6		D5		D4		D3		D2		D1		D0	
Reserved				ILIM3[2:0]				Reserved							
Bits	Field	Type	Default	Description											
7:6	Reserved	R/W	00												
5:3	ILIM3[2:0]	R/W	111	Sets the switch current limit of BUCK3. Can be programmed at any time during operation: 000 - 1.5 A 001 - 2.0 A 010 - 2.5 A 011 - 3.0 A 100 - 3.5 A 101 - 4.0 A 110 - 4.5 A 111 - 5.0 A (Default)											
2:0	Reserved	R/W	010												

### 8.6.1.8 BUCK0\_VOUT

Address: 0x0A

D7		D6		D5		D4		D3		D2		D1		D0	
BUCK0_VSET[7:0]															
Bits	Field	Type	Default	Description											
7:0	BUCK0_VSET[7:0]	R/W	0110 0001	Sets the output voltage of BUCK0 regulator <b>0.5 V - 0.73 V, 10 mV steps</b> 0000 0000 - 0.5V ... 0001 0111 - 0.73 V <b>0.73 V - 1.4 V, 5 mV steps</b> 0001 1000 - 0.735 V ... 1001 1101 - 1.4 V <b>1.4 V - 3.36 V, 20 mV steps</b> 1001 1110 - 1.42 V ... 1111 1111 - 3.36 V											

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**8.6.1.9 BUCK0\_FLOOR\_VOUT**

Address: 0x0B

D7	D6	D5	D4	D3	D2	D1	D0
BUCK0_FLOOR_VSET[7:0]							
Bits	Field	Type	Default	Description			
7:0	BUCK0_FLOOR_VSET[7:0]	R/W	0000 0000	Sets the output voltage of BUCK0 regulator when Floor state is used <b>0.5 V - 0.73 V, 10 mV steps</b> 0000 0000 - 0.5V ... 0001 0111 - 0.73 V <b>0.73 V - 1.4 V, 5 mV steps</b> 0001 1000 - 0.735 V ... 1001 1101 - 1.4 V <b>1.4 V - 3.36 V, 20 mV steps</b> 1001 1110 - 1.42 V ... 1111 1111 - 3.36 V			

**8.6.1.10 BUCK0\_DELAY**

Address: 0x12

D7	D6	D5	D4	D3	D2	D1	D0
BUCK0_SHUTDOWN_DELAY[3:0]				BUCK0_STARTUP_DELAY[3:0]			
Bits	Field	Type	Default	Description			
7:4	BUCK0_SHUTDOWN_DELAY[3:0]	R/W	0000	Shutdown delay of BUCK0 from falling edge of ENx signal: 0000 - 0 ms 0001 - 1 ms ... 1111 - 15 ms			
3:0	BUCK0_STARTUP_DELAY[3:0]	R/W	0000	Startup delay of BUCK0 from rising edge of ENx signal: 0000 - 0 ms 0001 - 1 ms ... 1111 - 15 ms			

### 8.6.1.11 RESET

Address: 0x16

D7	D6	D5	D4	D3	D2	D1	D0
Reserved							SW_RESET

Bits	Field	Type	Default	Description
7:1	Reserved	R/W	000 0000	
0	SW_RESET	R/W	0	Software commanded reset. When written to 1, the registers will be reset to default values, OTP memory is read, and the I <sup>2</sup> C interface is reset. The bit is automatically cleared.

### 8.6.1.12 CONFIG

Address: 0x17

D7	D6	D5	D4	D3	D2	D1	D0
Reserved				TDIE_WARN_LEVEL	EN2_PD	EN1_PD	EN_SPREAD_SPEC

Bits	Field	Type	Default	Description
7:4	Reserved	R/W	0000	
3	TDIE_WARN_LEVEL	R/W	0	Thermal warning threshold level. 0 - 125°C 1 - 105°C.
2	EN2_PD	R/W	1	Selects the pull down resistor on the EN2 input pin. 0 - Pull-down resistor is disabled. 1 - Pull-down resistor is enabled.
1	EN1_PD	R/W	1	Selects the pull down resistor on the EN1 input pin. 0 - Pull-down resistor is disabled. 1 - Pull-down resistor is enabled.
0	EN_SPREAD_SPEC	R/W	0	Enable spread spectrum feature: 0 - Disabled 1 - Enabled

### 8.6.1.13 INT\_TOP

Address: 0x18

D7	D6	D5	D4	D3	D2	D1	D0
INT_BUCK3	INT_BUCK2	INT_BUCK1	INT_BUCK0	TDIE_SD	TDIE_WARN	RESET_REG	I_LOAD_READY

Bits	Field	Type	Default	Description
7	INT_BUCK3	R	0	Interrupt indicating that output BUCK3 has a pending interrupt. The reason for the interrupt is indicated in INT_BUCK3 register. This bit is cleared automatically when INT_BUCK3 register is cleared to 0x00.
6	INT_BUCK2	R	0	Interrupt indicating that output BUCK2 has a pending interrupt. The reason for the interrupt is indicated in INT_BUCK2 register. This bit is cleared automatically when INT_BUCK2 register is cleared to 0x00.
5	INT_BUCK1	R	0	Interrupt indicating that output BUCK1 has a pending interrupt. The reason for the interrupt is indicated in INT_BUCK1 register. This bit is cleared automatically when INT_BUCK1 register is cleared to 0x00.
4	INT_BUCK0	R	0	Interrupt indicating that output BUCK0 has a pending interrupt. The reason for the interrupt is indicated in INT_BUCK0 register. This bit is cleared automatically when INT_BUCK0 register is cleared to 0x00.
3	TDIE_SD	R/W	0	Latched status bit indicating that the die junction temperature has exceeded the thermal shutdown level. The regulator has been disabled if it was enabled. The regulator cannot be enabled if this bit is active. The actual status of the thermal warning is indicated by TOP_STAT.TDIE_SD_STAT bit. Write 1 to clear interrupt.

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Bits	Field	Type	Default	Description
2	TDIE_WARN	R/W	0	Latched status bit indicating that the die junction temperature has exceeded the thermal warning level. The actual status of the thermal warning is indicated by TOP_STAT.TDIE_WARN_STAT bit. Write 1 to clear interrupt.
1	RESET_REG	R/W	0	Latched status bit indicating that either startup (NRST rising edge) has done, VANA supply voltage has been below undervoltage threshold level or the host has requested a reset (RESET.SW_RESET). The regulator has been disabled, and registers are reset to default values and the normal startup procedure is done. Write 1 to clear interrupt.
0	I_LOAD_READY	R/W	0	Latched status bit indicating that the load current measurement result is available in I_LOAD_1 and I_LOAD_2 registers. Write 1 to clear interrupt.

**8.6.1.14 INT\_BUCK\_0\_1**

Address: 0x19

D7	D6	D5	D4	D3	D2	D1	D0
Reserved			BUCK1_ILIM_INT	Reserved	BUCK0_PG_INT	BUCK0_SC_INT	BUCK0_ILIM_INT

Bits	Field	Type	Default	Description
7:5	Reserved	R/W	000	
4	BUCK1_ILIM_INT	R/W	0	Latched status bit indicating that output current limit has been active. Write 1 to clear.
3	Reserved	R/W	0	
2	BUCK0_PG_INT	R/W	0	Latched status bit indicating that BUCK0 output voltage has reached powergood threshold level. Write 1 to clear.
1	BUCK0_SC_INT	R/W	0	Latched status bit indicating that the BUCK0 output voltage has fallen below 0.35V level during operation or BUCK0 output didn't reach 0.35 V level in 1 ms from enable. Write 1 to clear.
0	BUCK0_ILIM_INT	R/W	0	Latched status bit indicating that output current limit has been active. Write 1 to clear.

**8.6.1.15 INT\_BUCK\_2\_3**

Address: 0x1A

D7	D6	D5	D4	D3	D2	D1	D0
Reserved			BUCK3_ILIM_INT	Reserved		BUCK2_ILIM_INT	

Bits	Field	Type	Default	Description
7:5	Reserved	R/W	000	
4	BUCK3_ILIM_INT	R/W	0	Latched status bit indicating that output current limit has been active. Write 1 to clear.
3:1	Reserved	R/W	000	
0	BUCK2_ILIM_INT	R/W	0	Latched status bit indicating that output current limit has been active. Write 1 to clear.

### 8.6.1.16 TOP\_STAT

Address: 0x1B

D7	D6	D5	D4	D3	D2	D1	D0
Reserved				TDIE_SD_STAT	TDIE_WARN_STAT	Reserved	

Bits	Field	Type	Default	Description
7:4	Reserved	R	0000	
3	TDIE_SD_STAT	R	0	Status bit indicating the status of thermal shutdown: 0 - Die temperature below thermal shutdown level 1 - Die temperature above thermal shutdown level.
2	TDIE_WARN_STAT	R	0	Status bit indicating the status of thermal warning: 0 - Die temperature below thermal warning level 1 - Die temperature above thermal warning level.
1:0	Reserved	R	00	

### 8.6.1.17 BUCK\_0\_1\_STAT

Address: 0x1C

D7	D6	D5	D4	D3	D2	D1	D0
Reserved			BUCK1_ILIM_STAT	BUCK0_STAT	BUCK0_PG_STAT	Reserved	BUCK0_ILIM_STAT

Bits	Field	Type	Default	Description
7:5	Reserved	R	000	
4	BUCK1_ILIM_STAT	R	0	Status bit indicating BUCK1 current limit status (raw status) 0 - BUCK1 output current is below current limit level 1 - BUCK1 output current limit is active.
3	BUCK0_STAT	R	0	Status bit indicating the enable/disable status of BUCK0: 0 - BUCK0 regulator is disabled 1 - BUCK0 regulator is enabled.
2	BUCK0_PG_STAT	R	0	Status bit indicating BUCK0 output voltage validity (raw status) 0 - BUCK0 output is above powergood threshold level 1 - BUCK0 output is below powergood threshold level.
1	Reserved	R	0	
0	BUCK0_ILIM_STAT	R	0	Status bit indicating BUCK0 current limit status (raw status) 0 - BUCK0 output current is below current limit level 1 - BUCK0 output current limit is active.

### 8.6.1.18 BUCK\_2\_3\_STAT

Address: 0x1D

D7	D6	D5	D4	D3	D2	D1	D0
Reserved			BUCK3_ILIM_STAT	Reserved		BUCK2_ILIM_STAT	

Bits	Field	Type	Default	Description
7:5	Reserved	R	000	
4	BUCK3_ILIM_STAT	R	0	Status bit indicating BUCK3 current limit status (raw status) 0 - BUCK3 output current is below current limit level 1 - BUCK3 output current limit is active.
3:1	Reserved	R	000	
0	BUCK2_ILIM_STAT	R	0	Status bit indicating BUCK2 current limit status (raw status) 0 - BUCK2 output current is below current limit level 1 - BUCK2 output current limit is active.

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**8.6.1.19 TOP\_MASK**

Address: 0x1E

D7		D6		D5		D4		D3		D2		D1		D0	
Reserved										TDIE_WARN_MASK		RESET_REG_MASK		I_LOAD_READY_MASK	
Bits	Field	Type	Default	Description											
7:3	Reserved	R/W	0 0000												
2	TDIE_WARN_MASK	R/W	0	Masking for thermal warning interrupt INT_TOP.TDIE_WARN: 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect TOP_STAT.TDIE_WARN_STAT status bit.											
1	RESET_REG_MASK	R/W	1	Masking for register reset interrupt INT_TOP.RESET_REG: 0 - Interrupt generated 1 - Interrupt not generated.											
0	I_LOAD_READY_MASK	R/W	0	Masking for load current measurement ready interrupt INT_TOP.I_LOAD_READY. 0 - Interrupt generated 1 - Interrupt not generated.											

**8.6.1.20 BUCK\_0\_1\_MASK**

Address: 0x1F

D7		D6		D5		D4		D3		D2		D1		D0	
Reserved						BUCK1_ILIM_MASK		Reserved		BUCK0_PG_MASK		Reserved		BUCK0_ILIM_MASK	
Bits	Field	Type	Default	Description											
7:5	Reserved	R/W	000												
4	BUCK1_ILIM_MASK	R/W	1	Masking for BUCK1 current limit detection interrupt INT_BUCK_0_1.BUCK1_ILIM_INT: 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect BUCK_0_1_STAT.BUCK1_ILIM_STAT status bit.											
3	Reserved	R/W	0												
2	BUCK0_PG_MASK	R/W	0	Masking for BUCK0 power good interrupt INT_BUCK_0_1.BUCK0_PG_INT: 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect BUCK_0_1_STAT.BUCK1_PG_STAT status bit.											
1	Reserved	R	0												
0	BUCK0_ILIM_MASK	R/W	0	Masking for BUCK0 current limit detection interrupt INT_BUCK_0_1.BUCK0_ILIM_INT: 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect BUCK_0_1_STAT.BUCK1_ILIM_STAT status bit.											

### 8.6.1.21 BUCK\_2\_3\_MASK

Address: 0x20

Bits	Field	Type	Default	Description
7:5	Reserved	R/W	000	
4	BUCK3_ILIM_MASK	R/W	1	Masking for BUCK3 current limit detection interrupt INT_BUCK_2_3.BUCK3_ILIM_INT: 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect BUCK_2_3_STAT.BUCK3_ILIM_STAT status bit.
3:1	Reserved	R/W	000	
0	BUCK2_ILIM_MASK	R/W	1	Masking for BUCK2 current limit detection interrupt INT_BUCK_2_3.BUCK2_ILIM_INT: 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect BUCK_2_3_STAT.BUCK1_ILIM_STAT status bit.

### 8.6.1.22 SEL\_I\_LOAD

Address: 0x21

Bits	Field	Type	Default	Description
7:2	Reserved	R/W	00 0000	
1:0	LOAD_CURRENT_BUCK_SELECT [1:0]	R/W	00	Start the current measurement on the selected regulator: 00 - BUCK0 01 - BUCK1 10 - BUCK2 11 - BUCK3 The measurement is started when register is written. If the selected buck is master, the measurement result is a sum current of master and slave bucks. If the selected buck is slave, the measurement result is a current of the selected slave bucks.

Bits	Field	Type	Default	Description
7:2	Reserved	R	00 0000	
1:0	BUCK_LOAD_CURRENT [9:8]	R	00	This register describes 3 MSB bits of the average load current on selected regulator with a resolution of 20 mA per LSB and max 20 A current.

### 8.6.1.23 I\_LOAD\_2

Address: 0x22

Bits	Field	Type	Default	Description
7:2	Reserved	R	00 0000	
1:0	BUCK_LOAD_CURRENT [9:8]	R	00	This register describes 3 MSB bits of the average load current on selected regulator with a resolution of 20 mA per LSB and max 20 A current.

Bits	Field	Type	Default	Description
7:2	Reserved	R	00 0000	
1:0	BUCK_LOAD_CURRENT [9:8]	R	00	This register describes 3 MSB bits of the average load current on selected regulator with a resolution of 20 mA per LSB and max 20 A current.

### 8.6.1.24 I\_LOAD\_1

Address: 0x23

Bits	Field	Type	Default	Description
7:2	Reserved	R	00 0000	
1:0	BUCK_LOAD_CURRENT [9:8]	R	00	This register describes 3 MSB bits of the average load current on selected regulator with a resolution of 20 mA per LSB and max 20 A current.

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Bits	Field	Type	Default	Description
7:0	BUCK_LOAD_CURRENT[7:0]	R	0000 0000	This register describes 8 LSB bits of the average load current on selected regulator with a resolution of 10 mA per LSB and max 20 A current.

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The LP8758 is a multi-phase step-down converter with four switcher cores bundled together.

### 9.2 Typical Application

#### 4-Phase configuration

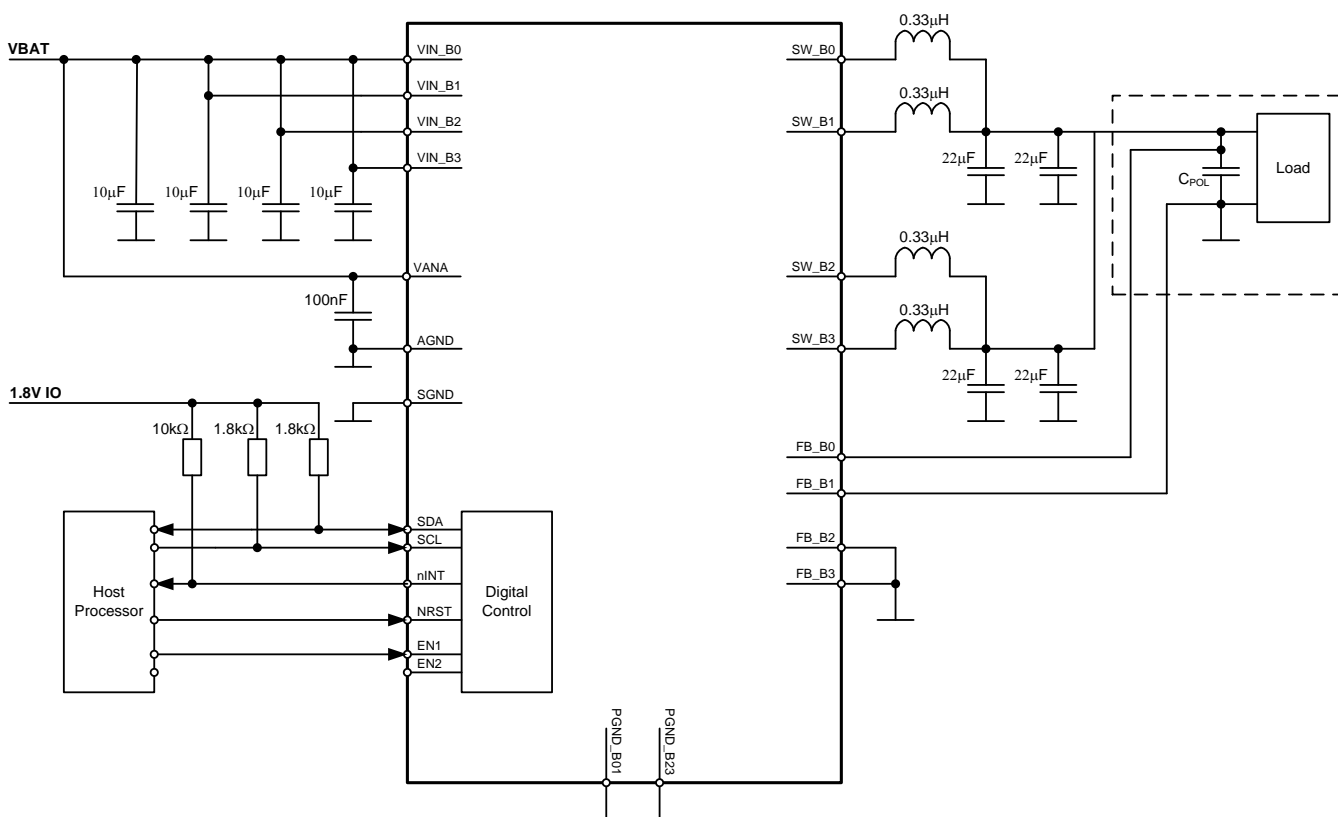


Figure 21. LP8758 Typical Application Circuit

#### 9.2.1 Design Requirements

Table 6. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.5 V to 5.5 V
Output voltage	1.1 V
Converter operation mode	Auto mode (PWM-PFM)
Maximum load current	16 A
Inductor current limit	5 A

## 9.2.2 Detailed Design Procedure

The performance of the LP8758 device depends greatly on the care taken in designing the Printed Circuit Board (PCB). The use of low-inductance and low serial-resistance ceramic capacitors is strongly recommended, while proper grounding is crucial. Attention should be given to decoupling the power supplies. Decoupling capacitors must be connected close to the device and between the power and ground pins to support high peak currents being drawn from System Power Rail during turn-on of the switching MOSFETs. Keep input and output traces as short as possible, because trace inductance, resistance, and capacitance can easily become the performance limiting items. The separate power pins VIN\_Bx are not connected together internally. The VIN\_Bx power connections shall be connected together outside the package using power plane construction.

### 9.2.2.1 Application Components

#### 9.2.2.1.1 Inductor Selection

DC bias current characteristics of inductors must be considered. Different manufacturers follow different saturation current rating specifications, so attention must be given to details. DC bias curves should be requested from them as part of the inductor selection process. Minimum effective value of inductance to ensure good performance is 0.22  $\mu\text{H}$  at 4-A bias current over the inductor's operating temperature range. The inductor's DC resistance should be less than 0.05  $\Omega$  for good efficiency at high current condition. The inductor AC loss (resistance) also affects conversion efficiency. Higher Q factor at switching frequency usually gives better efficiency at light load to middle load. See [Table 7](#). Shielded inductors are preferred as they radiate less noise.

**Table 7. Recommended Inductors**

MANUFACTURER	PART NUMBER	VALUE	DIMENSIONS LxWxH (mm)	DCR (m $\Omega$ )
TOKO	DFE252010F-R33M	0.33 $\mu\text{H}$	2.5 x 2.0 x 1.0	16 (typ), 21 (max)
TDK	VLS252010HBX-R33M	0.33 $\mu\text{H}$	2.5 x 2.0 x 1.0	25 (typ), 31 (max)
TDK	VLS252010HBX-R47M	0.47 $\mu\text{H}$	2.5 x 2.0 x 1.0	29 (typ), 35 (max)
TDK	TFM2016GHM-0R47M	0.47 $\mu\text{H}$	2.0 x 1.6 x 1.0	46 (max)
TOKO	DFE322512C R47	0.47 $\mu\text{H}$	3.2 x 2.5 x 1.2	21 (typ), 31 (max)

#### 9.2.2.1.2 Input Capacitor Selection

A ceramic input capacitor of 10  $\mu\text{F}$ , 6.3 V is sufficient for most applications. Place the power input capacitor as close as possible to the VIN\_Bx pin and PGND\_Bx pin of the device. A larger value or higher voltage rating may be used to improve input voltage filtering. Use X7R or X5R types, do not use Y5V or F. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0402. Minimum effective input capacitance to ensure good performance is 1.9  $\mu\text{F}$  per buck input at maximum input voltage DC bias including tolerances and over ambient temp range, assuming that there are at least 22  $\mu\text{F}$  of additional capacitance common for all the power input pins on the system power rail. See [Table 8](#).

The input filter capacitor supplies current to the high-side FET switch in the first half of each cycle and reduces voltage ripple imposed on the input power source. A ceramic capacitor's low equivalent series resistance (ESR) provides the best noise filtering of the input voltage spikes due to this rapidly changing current. Select an input filter capacitor with sufficient ripple current rating.

The VANA input is used to supply analog and digital circuits in the device. See recommended components from [Table 9](#) for VANA input supply filtering.

**Table 8. Recommended Power Input Capacitors (X5R Dielectric)**

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	DIMENSIONS LxWxH (mm)	VOLTAGE RATING
Murata	GRM188R60J106ME47	10 $\mu\text{F}$ (20%)	0603	1.6 x 0.8 x 0.8	6.3 V

**Table 9. Recommended VANA Supply Filtering Components**

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	DIMENSIONS LxWxH (mm)	VOLTAGE RATING
Samsung	CL03A104KP3NNNC	100 nF (10%)	0201	0.6 x 0.3 X 0.3	10 V
Murata	GRM033R61A104KE84	100 nF (10%)	0201	0.6 x 0.3 x 0.3	6.3 V

### 9.2.2.1.3 Output Capacitor Selection

Use ceramic capacitors, X7R or X5R types; do not use Y5V or F. DC bias voltage characteristics of ceramic capacitors must be considered. DC bias characteristics vary from manufacturer to manufacturer, and DC bias curves should be requested from them as part of the capacitor selection process. The output filter capacitor smooths out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR and ESL to perform these functions. Minimum effective output capacitance to ensure good performance is 10  $\mu$ F per phase at the output voltage DC bias including tolerances and over ambient temp range.

The output voltage ripple is caused by the charging and discharging of the output capacitor and also due to its  $R_{ESR}$ . The  $R_{ESR}$  is frequency dependent (as well as temperature dependent); make sure the value used for selection process is at the switching frequency of the part. See [Table 10](#).

A higher output capacitance improves the load step behavior and reduces the output voltage ripple as well as decreases the PFM switching frequency. For most 4-phase applications 4 x 22  $\mu$ F 0603 capacitors for  $C_{OUT}$  are suitable. A Point-Of-Load (POL) capacitance  $C_{POL}$  can be added with remove feedback as shown in [Figure 21](#). Although a converter's loop compensation can be programmed to adapt to virtually several hundreds of microfarads  $C_{OUT}$ , it is preferable for  $C_{OUT}$  to be < 200  $\mu$ F (4-phase configuration). Choosing higher than that is not necessarily of any benefit. Note that the output capacitor may be the limiting factor in the output voltage ramp, especially for very large (> 100  $\mu$ F) output capacitors. For large output capacitors, the output voltage might be slower than the programmed ramp rate at voltage transitions, because of the higher energy stored on the output capacitance. Also at start-up, the time required to charge the output capacitor to target value might be longer. At shutdown, if the output capacitor is discharged by the internal discharge resistor, more time is required to settle  $V_{OUT}$  down as a consequence of the increased time constant.

**Table 10. Recommended Output Capacitors (X5R Dielectric)**

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	DIMENSIONS LxWxH (mm)	VOLTAGE RATING
Samsung	CL10A226MP8NUNE	22 $\mu$ F (20%)	0603	1.6 x 0.8 x 0.8	10 V
Murata	GRM188R60J226MEA0	22 $\mu$ F (20%)	0603	1.6 x 0.8 x 0.8	6.3 V

### 9.2.3 Application Curves

Unless otherwise specified:  $V_{IN} = 3.7\text{ V}$ ,  $V_{OUT} = 1\text{ V}$ ,  $V_{(NRST)} = 1.8\text{ V}$ ,  $T_A = 25\text{ }^\circ\text{C}$ ,  $f_{SW} = 3\text{ MHz}$ ,  $L = 330\text{ nH}$  (TOKO DFE252010F-R33M),  $C_{POL} = 22\text{ }\mu\text{F}$ . Measurements done with connections in [Figure 21](#).

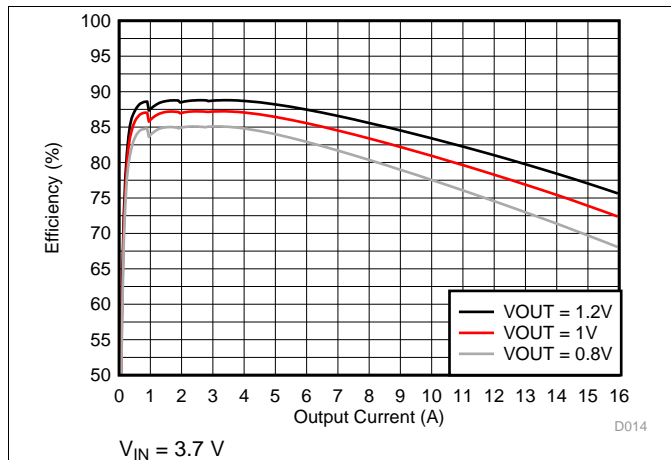


Figure 22. Efficiency in Forced PWM Mode

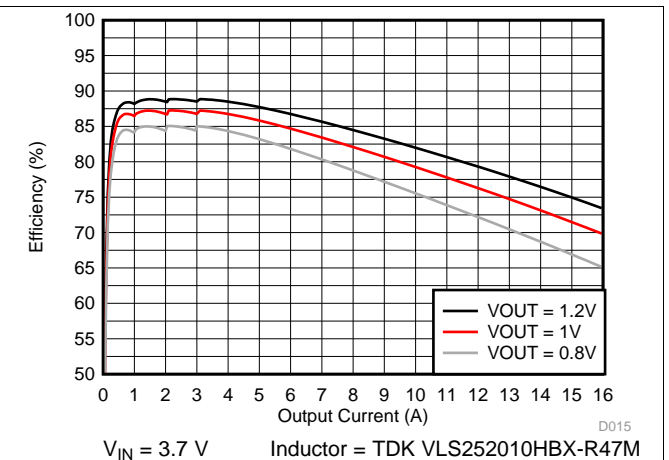


Figure 23. Efficiency in Forced PWM Mode

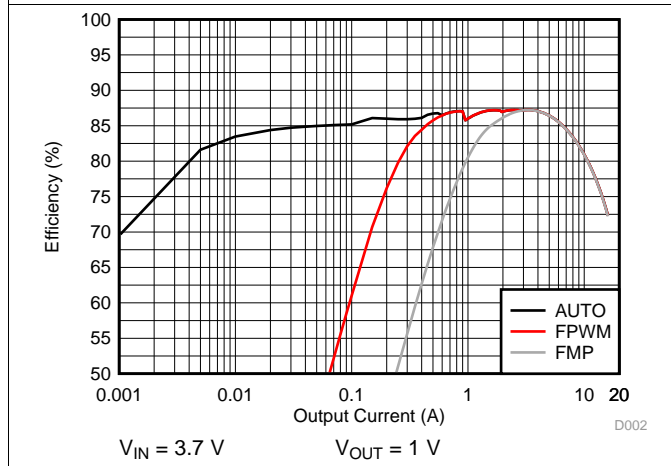


Figure 24. Efficiency in PFM, PWM and Forced Multi-Phase Mode

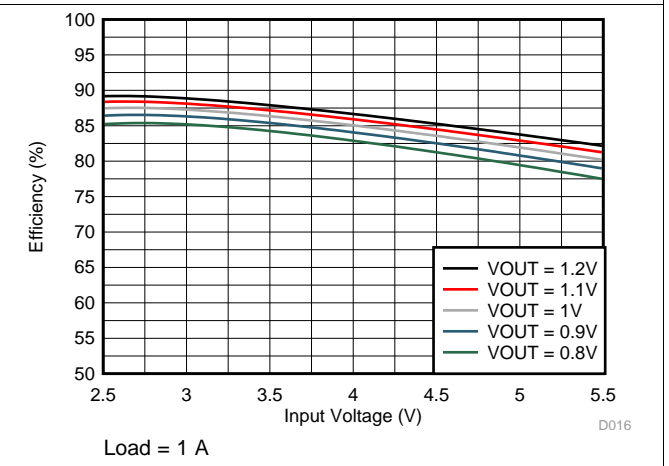


Figure 25. Efficiency vs Input Voltage

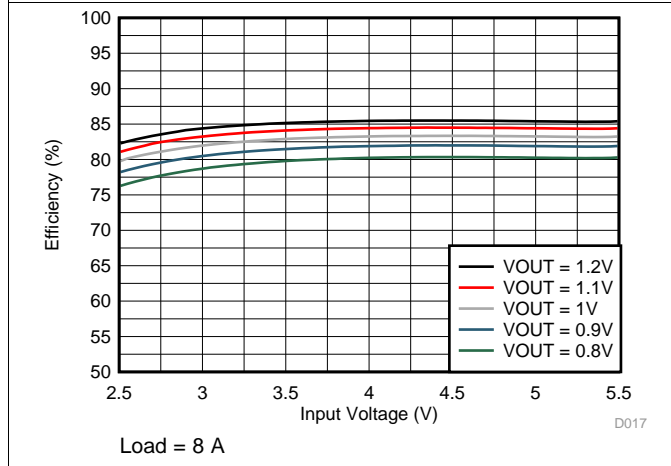


Figure 26. Efficiency vs Input Voltage

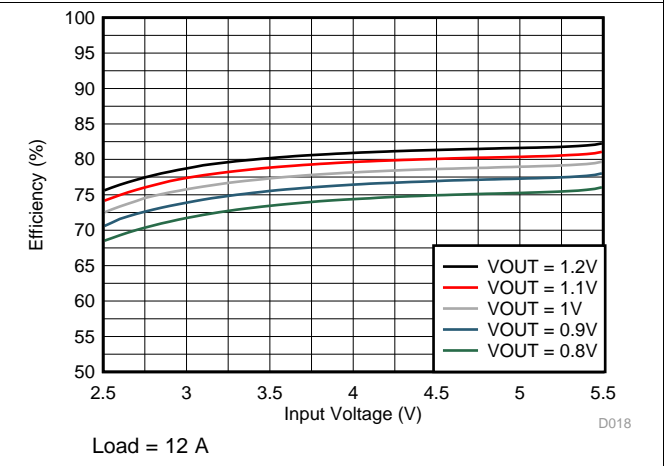


Figure 27. Efficiency vs Input Voltage

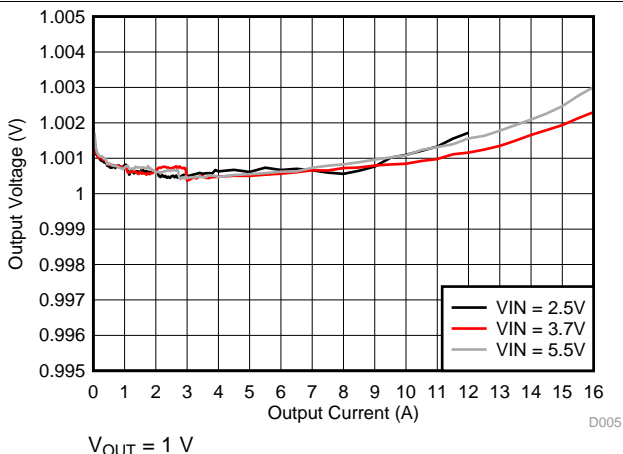


Figure 28. Output Voltage vs Load Current in Forced PWM Mode

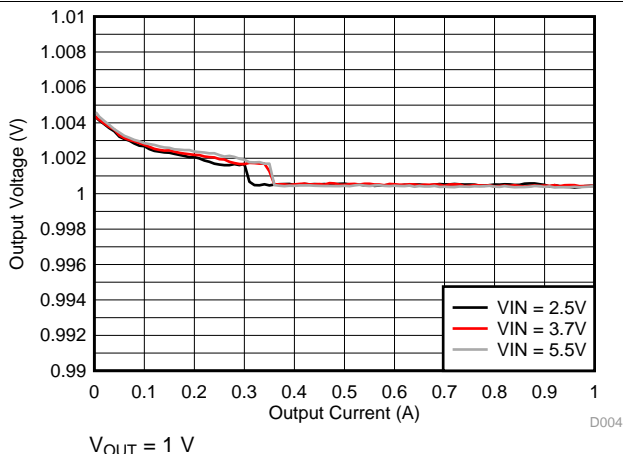


Figure 29. Output Voltage vs Load Current in PWM-PFM Mode

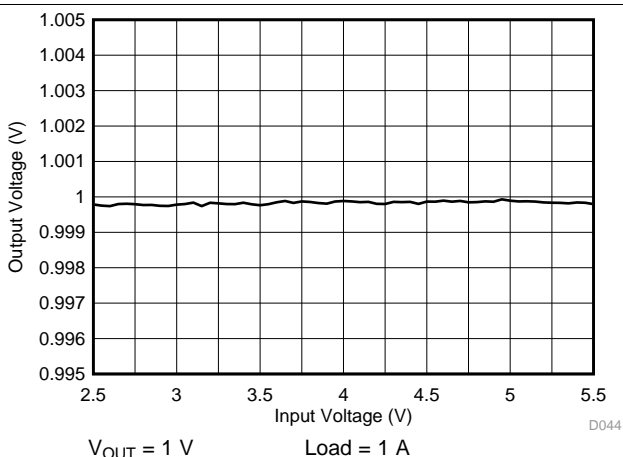


Figure 30. Output Voltage vs Input Voltage in PWM Mode

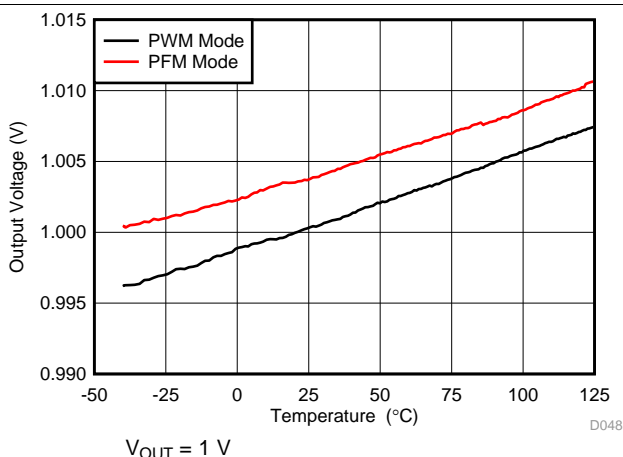


Figure 31. Output Voltage vs Temperature

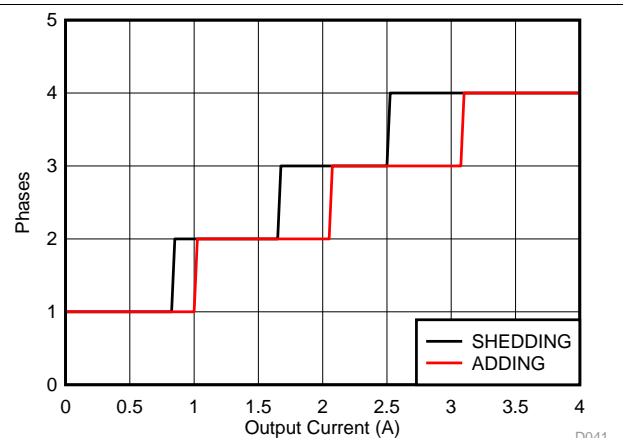


Figure 32. Phase Adding and Shedding vs Load Current

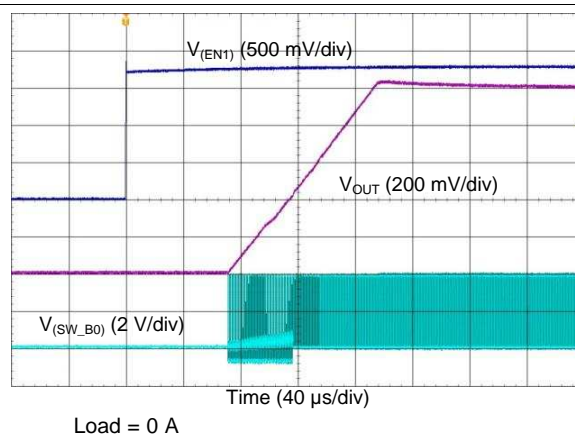
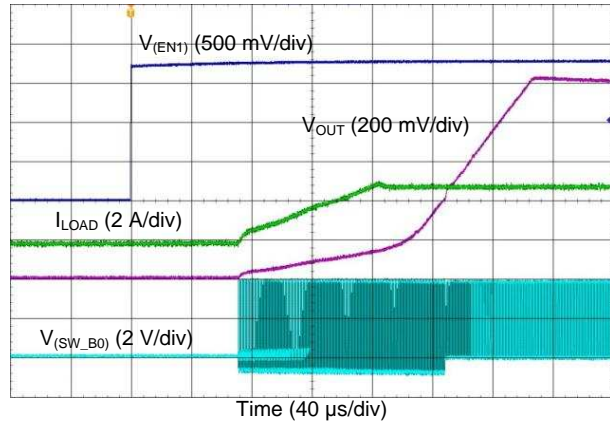
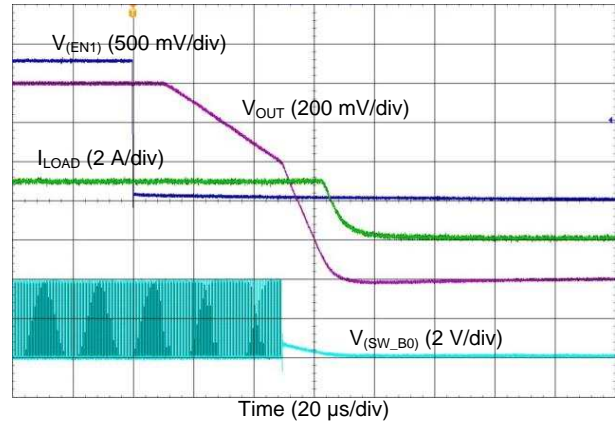


Figure 33. Start-up with EN1, Forced PWM



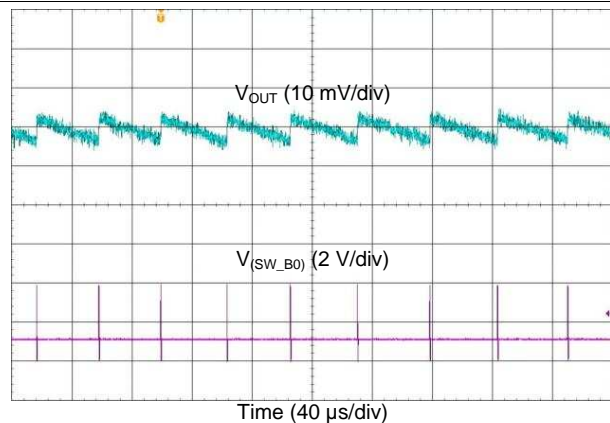
Load = 3 A

Figure 34. Start-up with EN1, Forced PWM



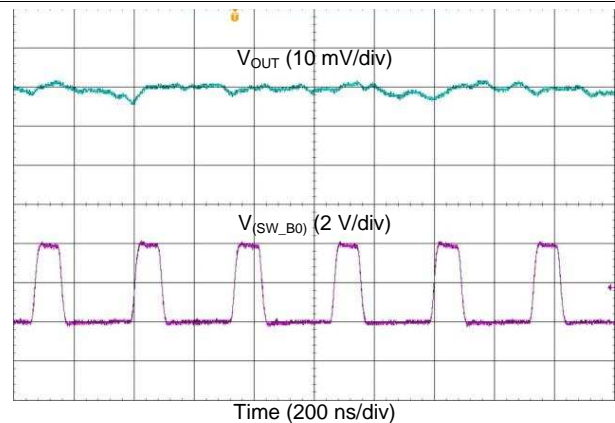
Load = 3 A

Figure 35. Shutdown with EN1, Forced PWM



Load = 10 mA

Figure 36. Output Voltage Ripple, PFM Mode



Load = 200 mA

Figure 37. Output Voltage Ripple, Forced PWM Mode

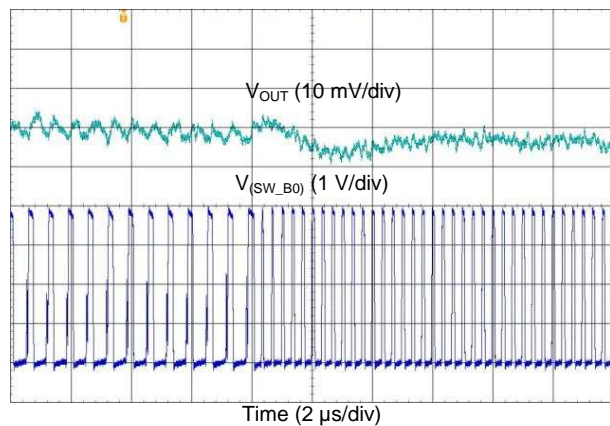


Figure 38. Transient from PFM-to-PWM Mode

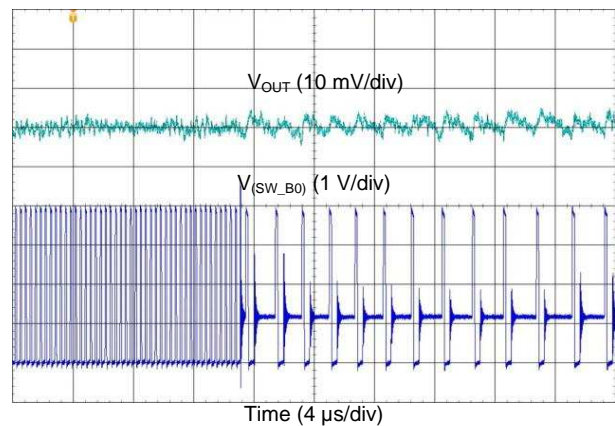


Figure 39. Transient from PWM-to-PFM Mode

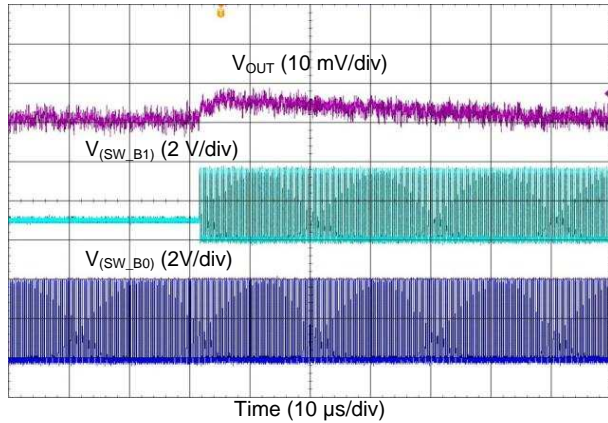


Figure 40. Transient from 1-Phase to 2-Phase Operation

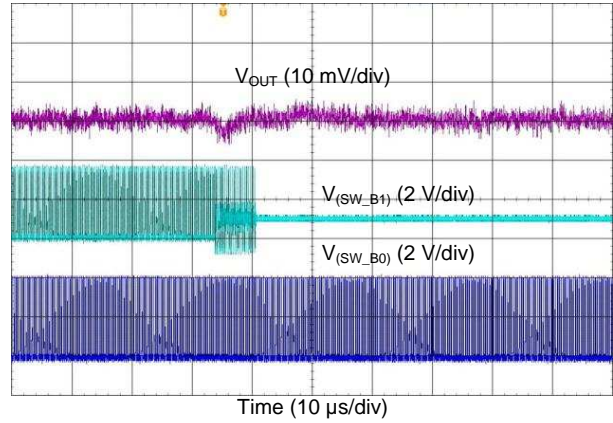


Figure 41. Transient from 2-Phase to 1-Phase Operation

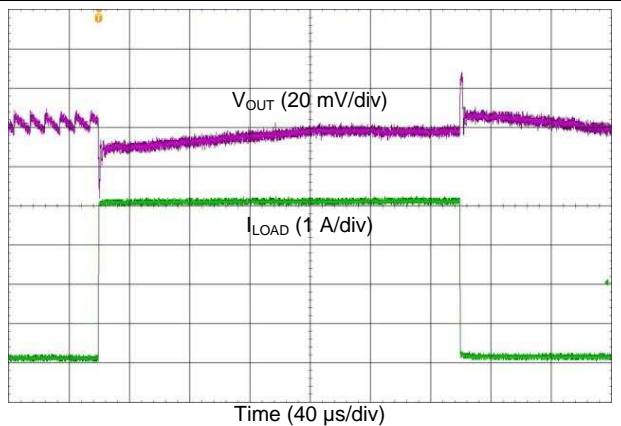


Figure 42. Transient Load Step Response, AUTO Mode  
Load = 0.1 A → 4.1 A → 0.1 A     $T_R = T_F = 100$  ns

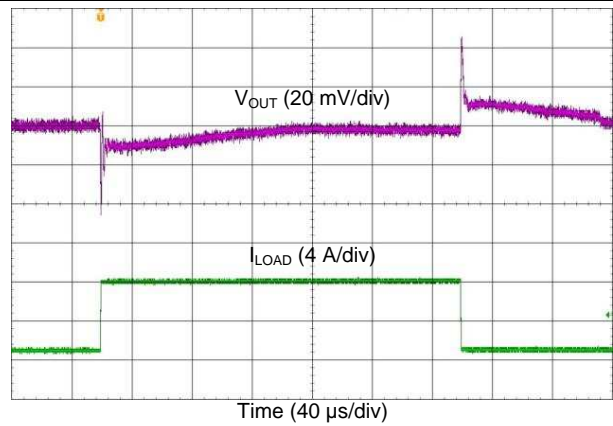


Figure 43. Transient Load Step Response, FPWM Mode  
Load = 1 A → 8 A → 1 A     $T_R = T_F = 400$  ns

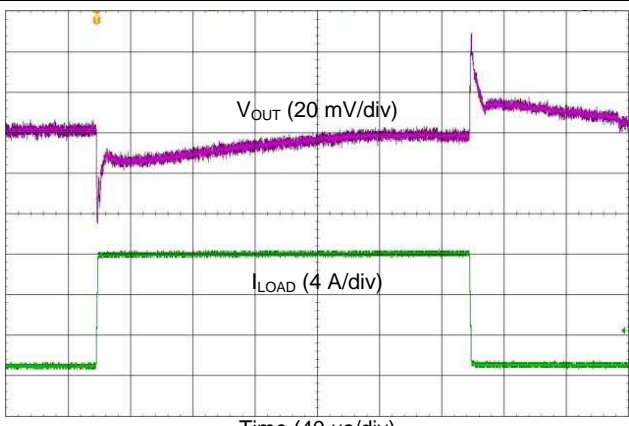


Figure 44. Transient Load Step Response, FPWM Mode  
Load = 1 A → 12 A → 1 A     $T_R = T_F = 1$  μs

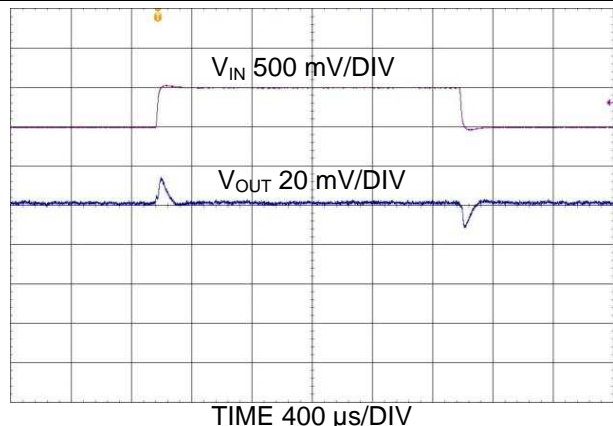
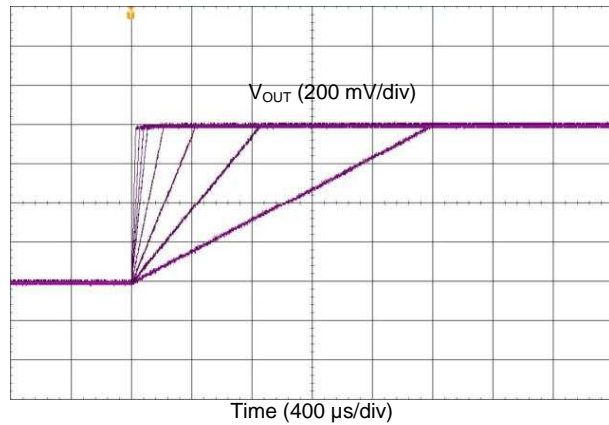
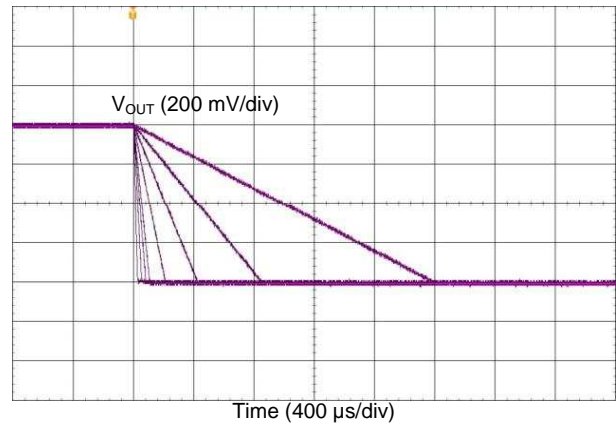


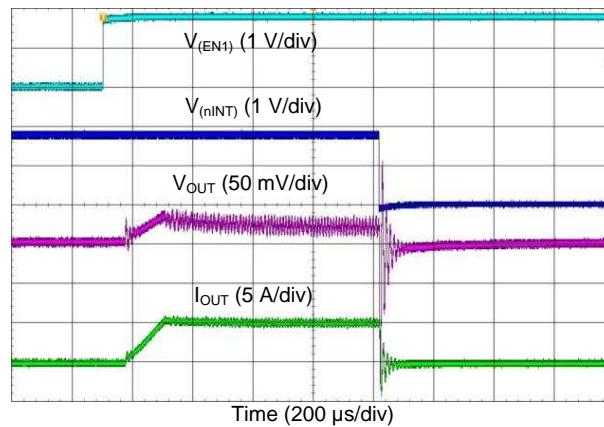
Figure 45. Transient Line Response  
Load = 12 A     $T_R = T_F = 10$  μs  
 $V_{IN} = 2.5$  V → 3 V → 2.5 V



**Figure 46.  $V_{OUT}$  Transition from 0.6 V to 1.4 V with Different Slew Rate Settings**



**Figure 47.  $V_{OUT}$  Transition from 1.4 V to 0.6 V with Different Slew Rate Settings**



**Figure 48. Start-up with Short on Output**

## 10 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.5 V and 5.5 V. This input supply should be well-regulated and able to withstand maximum input current and maintain stable voltage without voltage drop even at load transition condition. The resistance of the input supply rail should be low enough that the input current transient does not cause too high drop in the LP8758 supply voltage that can cause false UVLO fault triggering. If the input supply is located more than a few inches from the LP8758 additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

## 11 Layout

### 11.1 Layout Guidelines

The high frequency and large switching currents of the LP8758 make the choice of layout important. Good power supply results will only occur when care is given to proper design and layout. Layout will affect noise pickup and generation and can cause a good design to perform with less-than-expected results. With a range of output currents from milliamps to 10 A and over, good power supply layout is much more difficult than most general PCB design. The following steps should be used as a reference to ensure the device is stable and maintains proper voltage and current regulation across its intended operating voltage and current range.

1. Place  $C_{IN}$  as close as possible to the VIN\_Bx pin and the PGND\_Bxx pin. Route the  $V_{IN}$  trace wide and thick to avoid IR drops. The trace between the input capacitor's positive node and LP8758's VIN\_Bx pin(s) as well as the trace between the input capacitor's negative node and power PGND\_Bxx pin(s) must be kept as short as possible. The input capacitance provides a low-impedance voltage source for the switching converter. The inductance of the connection is the most important parameter of a local decoupling capacitor - parasitic inductance on these traces must be kept as tiny as possible for proper device operation.
2. The output filter, consisting of  $L_x$  and  $C_{OUTx}$ , converts the switching signal at SW\_Bx to the noiseless output voltage. It should be placed as close as possible to the device keeping the switch node small, for best EMI behavior. Route the traces between the LP8758's output capacitors and the load's input capacitors direct and wide to avoid losses due to the IR drop.
3. Input for analog blocks (VANA and AGND) should be isolated from noisy signals. Connect VANA directly to a quiet system voltage node and AGND to a quiet ground point where no IR drop occurs. Place the decoupling capacitor as close to the VANA pin as possible. VANA must be connected to the same power node as VIN\_Bx pins.
4. If the processor load supports remote voltage sensing, connect the LP8758's feedback pins FB\_Bx to the respective sense pins on the processor. The sense lines are susceptible to noise. They must be kept away from noisy signals such as PGND\_Bxx, VIN\_Bx, and SW\_Bx, as well as high bandwidth signals such as the  $I^2C$ . Avoid both capacitive as well as inductive coupling by keeping the sense lines short, direct and close to each other. Run the lines in a quiet layer. Isolate them from noisy signals by a voltage or ground plane if possible. Running the signal as a differential pair is recommended.
5. PGND\_Bxx, VIN\_Bx and SW\_Bx should be routed on thick layers. They must not surround inner signal layers which are not able to withstand interference from noisy PGND\_Bxx, VIN\_Bx and SW\_Bx.

Due to the small package of this converter and the overall small solution size, the thermal performance of the PCB layout is important. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component. Proper PCB layout, focusing on thermal performance, results in lower die temperatures. Wide power traces come with the ability to sink dissipated heat. This can be improved further on multi-layer PCB designs with vias to different planes. This results in reduced junction-to-ambient ( $R_{\theta JA}$ ) and junction-to-board ( $R_{\theta JB}$ ) thermal resistances, thereby reducing the device junction temperature,  $T_J$ . Performing a careful system-level 2D or full 3D dynamic thermal analysis at the beginning product design process is strongly recommended, using a thermal modeling analysis software.

## 11.2 Layout Example

- Via to GND plane
- ⊗ Via to  $V_{IN}$  plane

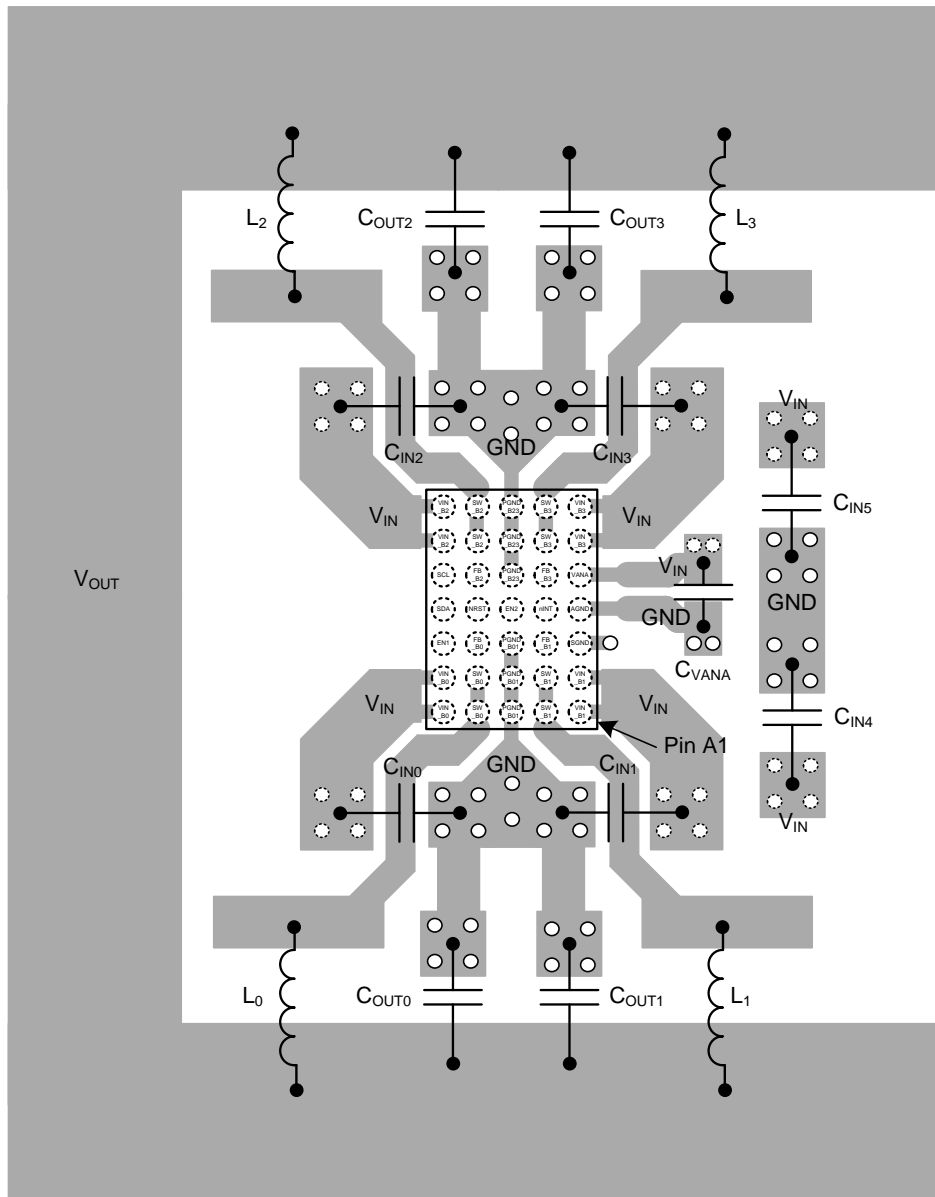


Figure 49. LP8758 Board Layout

## 12 Device and Documentation Support

### 12.1 Device Support

#### 12.1.1 Third-Party Products Disclaimer

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### 12.2 Documentation Support

#### 12.2.1 Related Documentation

For related documentation, see the following:

Application Note 1112: *DSBGA Wafer Level Chip Scale Package* ([SNVA009](#)).

### 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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### 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP8758A1B0YFFR	PREVIEW	DSBGA	YFF	35		Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	8758A1B0	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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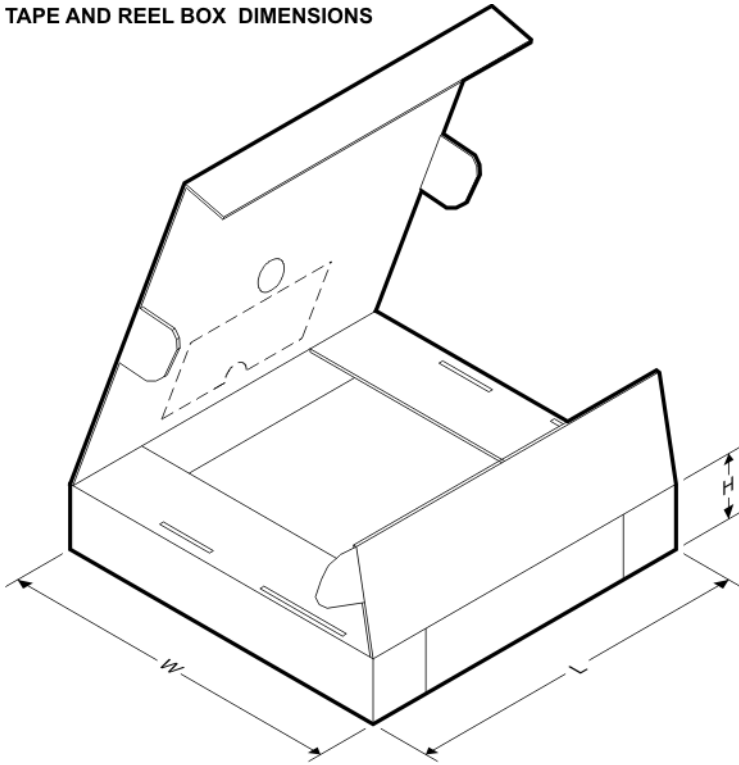


### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP8758A1B0YFFR	DSBGA	YFF	35	0	180.0	8.4	2.28	3.03	0.74	4.0	8.0	Q1

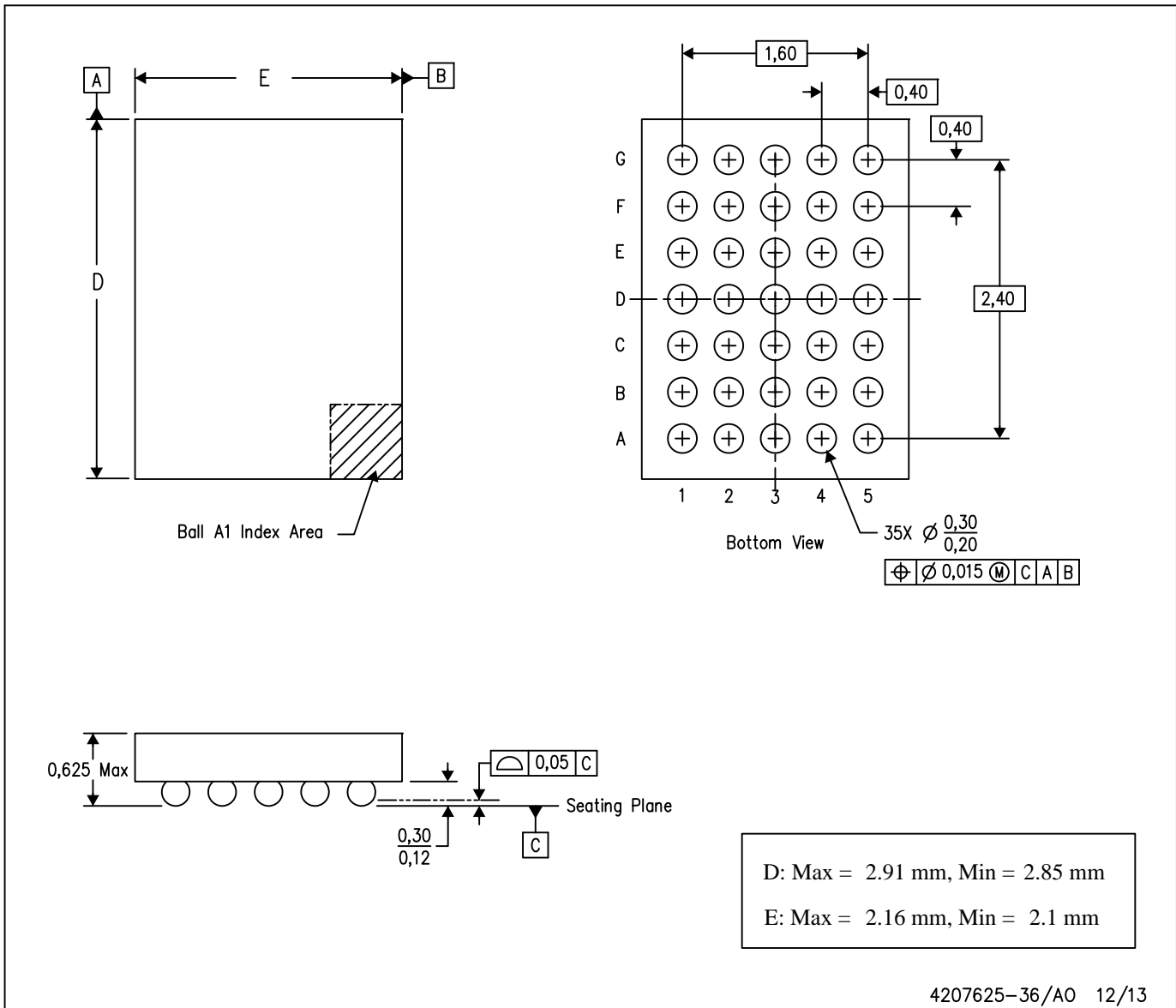
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP8758A1B0YFFR	DSBGA	YFF	35	0	182.0	182.0	17.0

YFF (R-XBGA-N35)

DIE-SIZE BALL GRID ARRAY



- NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.  
 B. This drawing is subject to change without notice.  
 C. NanoFree™ package configuration.

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