

# LP5521

## Programmable Three Channel LED Driver

### General Description

The LP5521 is a three channel LED driver designed to produce variety of lighting effects for mobile devices. High efficiency charge pump enables LED driving over full Li-Ion battery voltage range. The device has a program memory for creating variety of lighting sequences. When program memory has been loaded, LP5521 can operate independently without processor control.

LP5521 maintains excellent efficiency over a wide operating range by automatically selecting proper charge pump gain based on LED forward voltage requirements. LP5521 is able to automatically enter power-save mode, when LED outputs are not active and thus lowering current consumption.

Three independent LED channels have accurate programmable current sources and PWM control. Each channel has program memory for creating desired lighting sequences with PWM control.

LP5521 has a flexible digital interface. Trigger I/O and 32 kHz clock input allow synchronization between multiple devices. Interrupt output can be used to notify processor, when LED sequence has ended. LP5521 has four pin selectable I<sup>2</sup>C addresses. This allows connecting up to four parallel devices in one I<sup>2</sup>C bus. GPO and INT pins can be used as a digital control pin for other devices.

LP5521 requires only four small and low cost ceramic capacitors.

LP5521 is available in tiny 2.1x1.7x0.6 mm microSMD-20 package and in 4.0x5.0x0.8 mm bumped LLP-24 package.

Comprehensive application tools are available, including command compiler for easy LED sequence programming.

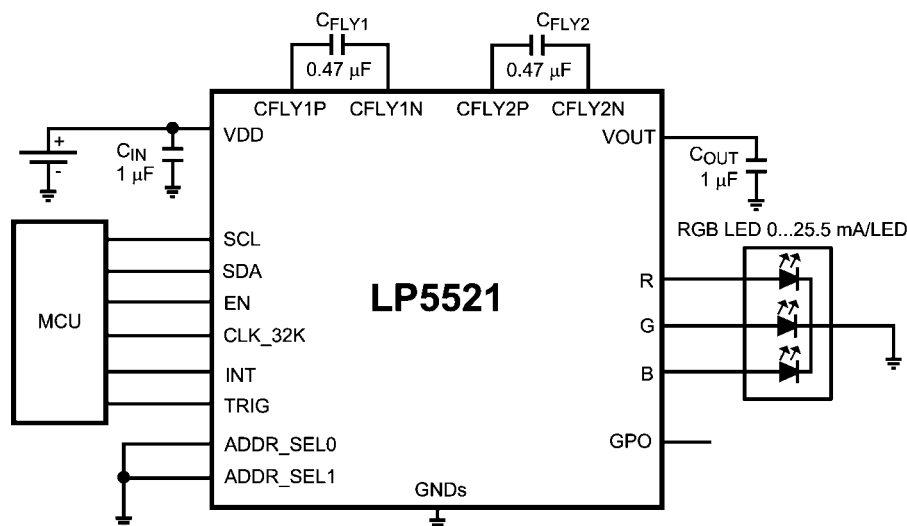
### Features

- Adaptive charge pump with 1x and 1.5x gain provides up to 95% LED drive efficiency
- Charge pump with soft start and overcurrent/short circuit protection
- Low input ripple and EMI
- Very small solution size, no inductor or resistors required
- 200 nA typical shutdown current
- Automatic power save mode
- I<sup>2</sup>C compatible interface
- Independently programmable constant current outputs with 8-bit current setting and 8-bit PWM control
- Typical LED output saturation voltage 50 mV and current matching 1%
- Three program execution engines with flexible instruction set
- Autonomous operation without external control
- Large SRAM program memory
- Two general purpose digital outputs
- microSMD-20 package, 0.4 mm pitch
- Bumped LLP-24 package, 0.5 mm pitch

### Applications

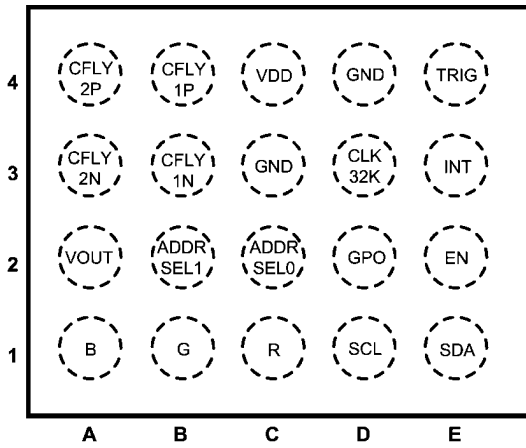
- Fun / indicator lights
- LCD sub-display backlighting
- Keypad RGB backlighting and phone cosmetics
- Vibra, speakers, waveform generator

### Typical Application



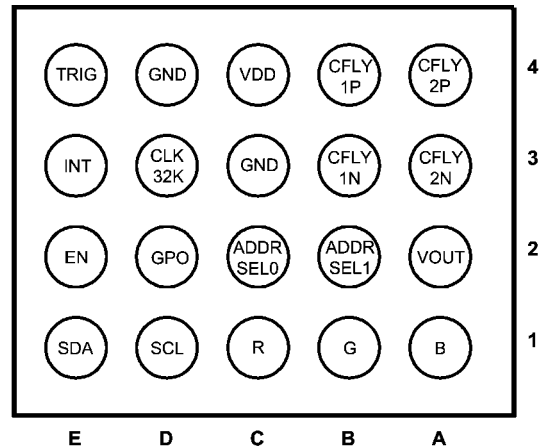
# Connection Diagrams and Package Mark Information

Thin microSMD-20 Package (2.1 x 1.7 x 0.6 mm, 0.4 mm pitch)  
 NS Package Number TMD20ECA



Top View

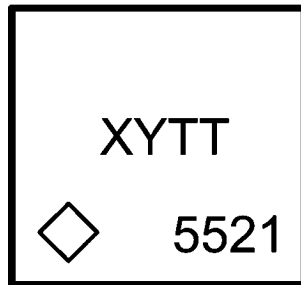
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Bottom View

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## Package Mark



XY = 2 Digit Date Code

TT = Die Traceability

5521 = Product Identification

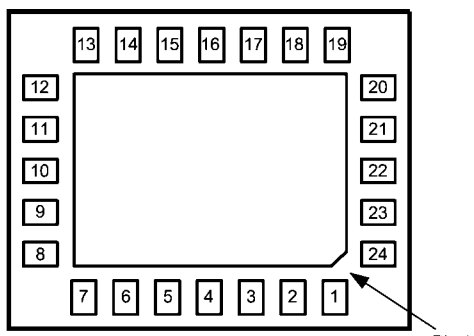
= Pin 1A

Package Mark - Top View

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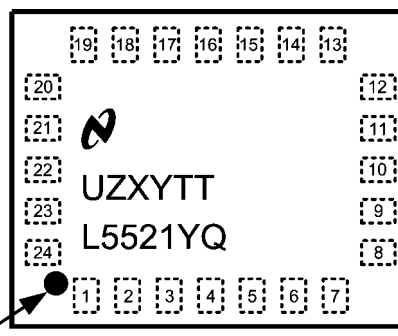
# Connection Diagrams and Package Mark Information

Bumped LLP-24 Package (5 x 4 x 0.8 mm, 0.5 mm pitch)  
 NS Package Number YQA24A



Bottom View

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Package Mark - Top View

20186201

**U = Fab**  
**Z = Assembly**  
**XY = 2 Digit Date Code**  
**TT = Die Traceability**  
**L5521YQ = Product Identification**

## Ordering Information

| Order Number | Package    | Package Marking | Supplied As               | Spec/Flow |
|--------------|------------|-----------------|---------------------------|-----------|
| LP5521TM     | μSMD       | 5521            | 250 units, Tape-and-Reel  | NoPb      |
| LP5521TM X   | μSMD       | 5521            | 3000 units, Tape-and-Reel | NoPb      |
| LP5521YQ     | bumped LLP | L5521YQ         | 1000 units, Tape-and-Reel | NoPb      |
| LP5521YQ X   | bumped LLP | L5521YQ         | 4500 units, Tape-and-Reel | NoPb      |

## Pin Descriptions LP5521TM

| Pin # | Name      | Type | Description   |
|-------|-----------|------|---|
| 1A    | B         | A    | Current source output                               |
| 1B    | G         | A    | Current source output                               |
| 1C    | R         | A    | Current source output                               |
| 1D    | SCL       | I    | I <sup>2</sup> C Serial interface clock input       |
| 1E    | SDA       | I/OD | I <sup>2</sup> C Serial interface data input/output |
| 2A    | VOUT      | A    | Charge pump output                                  |
| 2B    | ADDR_SEL1 | I    | I <sup>2</sup> C address select input               |
| 2C    | ADDR_SEL0 | I    | I <sup>2</sup> C address select input               |
| 2D    | GPO       | O    | General purpose output                              |
| 2E    | EN        | I    | Chip enable   |
| 3A    | CFLY2N    | A    | Negative terminal of charge pump fly capacitor 2    |
| 3B    | CFLY1N    | A    | Negative terminal of charge pump fly capacitor 1    |
| 3C    | GND       | G    | Ground  |
| 3D    | CLK_32K   | I    | 32 kHz clock input                                  |
| 3E    | INT       | OD/O | Interrupt output / General Purpose Output           |
| 4A    | CFLY2P    | A    | Positive terminal of charge pump fly capacitor 2    |
| 4B    | CFLY1P    | A    | Positive terminal of charge pump fly capacitor 1    |
| 4C    | VDD       | P    | Power supply pin                                    |
| 4D    | GND       | G    | Ground  |
| 4E    | TRIG      | I/OD | Trigger input/output                                |

**A: Analog Pin, G: Ground Pin, P: Power Pin, I: Input Pin, I/O: Input/Output Pin, O: Output Pin, OD: Open Drain Pin**

## Pin Descriptions LP5521YQ

| Pin # | Name      | Type | Description   |
|-------|-----------|------|---|
| 1     | CFLY2P    | A    | Positive terminal of charge pump fly capacitor 2    |
| 2     | CFLY1P    | A    | Positive terminal of charge pump fly capacitor 1    |
| 3     | VDD       | P    | Power supply pin                                    |
| 4     | GND       | G    | Ground  |
| 5     | CLK_32K   | I    | 32 kHz clock input                                  |
| 6     | INT       | OD/O | Interrupt output / General purpose output           |
| 7     | TRIG      | I/OD | Trigger input/output                                |
| 8     |           | N/C  |   |
| 9     |           | N/C  |   |
| 10    |           | N/C  |   |
| 11    |           | N/C  |   |
| 12    |           | N/C  |   |
| 13    | SDA       | I/OD | I <sup>2</sup> C Serial interface data input/output |
| 14    | EN        | I    | Chip enable   |
| 15    | SCL       | I    | I <sup>2</sup> C Serial interface clock input       |
| 16    | GPO       | O    | General purpose output                              |
| 17    | R         | A    | Current source output                               |
| 18    | G         | A    | Current source output                               |
| 19    | B         | A    | Current source output                               |
| 20    | ADDR_SEL0 | I    | I <sup>2</sup> C address select input               |
| 21    | ADDR_SEL1 | I    | I <sup>2</sup> C address select input               |
| 22    | VOUT      | A    | Charge pump output                                  |
| 23    | CFLY2N    | A    | Negative terminal of charge pump fly capacitor 2    |
| 24    | CFLY1N    | A    | Negative terminal of charge pump fly capacitor 1    |

**A: Analog Pin, G: Ground Pin, P: Power Pin, I: Input Pin, I/O: Input/Output Pin, O: Output Pin, OD: Open Drain Pin, N/C: Not Connected**

## Absolute Maximum Ratings (Note 1, Note 2)

If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

|  |  |
|--|--|
| V <sub>DD</sub> , V <sub>OUT</sub> , R, G, B         | -0.3V to +6.0V                               |
| Voltage on Logic Pins                                | -0.3V to V <sub>DD</sub> +0.3V with 6.0V max |
| Continuous Power Dissipation <small>(Note 3)</small> | Internally Limited                           |
| Junction Temperature (T <sub>J-MAX</sub> )           | 125°C  |
| Storage Temperature Range                            | -65°C to +150°C                              |
| Maximum Lead Temperature (Soldering)                 | <small>(Note 4)</small>                      |
| ESD Rating <small>(Note 5)</small>                   |  |
| Human Body Model:                                    | 2 kV   |
| Machine Model:                                       | 200V   |

## Operating Ratings (Note 1, Note 2)

|   |                 |
|---|-----------------|
| V <sub>DD</sub>   | 2.7 to 5.5V     |
| Recommended Charge Pump   |                 |
| Load Current I <sub>OUT</sub>                                       | 0 to 100 mA     |
| Junction Temperature (T <sub>J</sub> ) Range                        | -30°C to +125°C |
| Ambient Temperature (T <sub>A</sub> ) Range <small>(Note 6)</small> | -30°C to +85°C  |

## Thermal Properties

|   |             |
|---|-------------|
| Junction-to-Ambient Thermal Resistance (θ <sub>JA</sub> ), TMD20 Package <small>(Note 7)</small>  | 50 - 90°C/W |
| Junction-to-Ambient Thermal Resistance (θ <sub>JA</sub> ), YQA24A Package <small>(Note 7)</small> | 37 - 90°C/W |

## Electrical Characteristics (Note 2, Note 8)

Limits in standard typeface are for T<sub>J</sub> = 25°C. Limits in **boldface** type apply over the operating ambient temperature range (-30°C < T<sub>A</sub> < +85°C). Unless otherwise noted, specifications apply to the LP5521 Block Diagram with: 2.7V ≤ V<sub>DD</sub> ≤ 5.5V, C<sub>OUT</sub> = C<sub>IN</sub> = 1 μF, C<sub>FLY1</sub> = C<sub>FLY2</sub> = 0.47 μF. (Note 9).

| Symbol                        | Parameter                              | Condition   | Min             | Typ  | Max           | Units |    |
|-------------------------------|--|---|-----------------|------|---------------|-------|----|
| I <sub>VDD</sub>              | Standby supply current                 | EN = 0 (pin), CHIP_EN = 0 (bit), external 32 kHz clock running or not running |                 | 0.2  | <b>2</b>      | μA    |    |
|                               |  | EN = 1 (pin), CHIP_EN = 0 (bit), external 32 kHz clock not running            |                 | 1.0  |               | μA    |    |
|                               |  | EN = 1 (pin), CHIP_EN = 0 (bit), external 32 kHz clock running                |                 | 1.4  |               | μA    |    |
|                               | Normal mode supply current             | Charge pump and LED drivers disabled  |                 |      | 0.25          |       | mA |
|                               |  | Charge pump in 1x mode, no load, LED drivers disabled                         |                 |      | 0.70          |       | mA |
|                               |  | Charge pump in 1.5x mode, no load, LED drivers disabled                       |                 |      | 1.5           |       | mA |
|                               |  | Charge pump in 1x mode, no load, LED drivers enabled                          |                 |      | 1.2           |       | mA |
| Powersave mode supply current | External 32 kHz clock running          |   |                 | 10   |               | μA    |    |
|                               | Internal oscillator running            |   |                 | 0.25 |               | mA    |    |
| f <sub>OSC</sub>              | Internal oscillator frequency accuracy |   | -4<br><b>-7</b> |      | 4<br><b>7</b> | %     |    |

## Charge Pump Electrical Characteristics (Note 10)

| Symbol           | Parameter   | Condition   | Min       | Typ  | Max      | Units    |
|------------------|---|---|-----------|------|----------|----------|
| R <sub>OUT</sub> | Charge pump output resistance                                   | Gain = 1.5x   |           | 3.5  |          | Ω        |
|                  |   | Gain = 1x   |           | 1    |          | Ω        |
| f <sub>SW</sub>  | Switching frequency   |   | <b>-7</b> | 1.25 | <b>7</b> | MHz<br>% |
| I <sub>GND</sub> | Ground current  | Gain = 1.5x   |           | 1.2  |          | mA       |
|                  |   | Gain = 1x   |           | 0.5  |          | mA       |
| t <sub>ON</sub>  | V <sub>OUT</sub> turn-on time from charge pump off to 1.5x mode | V <sub>DD</sub> = 3.6V, CHIP_EN = H<br>I <sub>OUT</sub> = 60 mA |           | 100  |          | μs       |
| V <sub>OUT</sub> | Charge pump output voltage                                      | V <sub>DD</sub> = 3.6V, no load, Gain = 1.5x                    |           | 4.55 |          | V        |

## LED Driver Electrical Characteristics (R, G, B Outputs)

| Symbol        | Parameter                             | Condition  | Min      | Typ  | Max    | Units   |
|---------------|---------------------------------------|--|----------|------|--------|---------|
| $I_{LEAKAGE}$ | R, G, B pin leakage current           |  |          | 0.1  | 1      | $\mu A$ |
| $I_{MAX}$     | Maximum Source Current                | Outputs R, G, B  |          | 25.5 |        | mA      |
| $I_{OUT}$     | Accuracy of output current            | Output current set to 17.5 mA, $V_{DD} = 3.6V$                         | -4<br>-5 |      | 4<br>5 | %       |
| $I_{MATCH}$   | Matching ( <i>Note 11</i> )           | $I_{OUT} = 17.5 mA, V_{DD} = 3.6V$                                     |          | 1    | 2      | %       |
| $f_{LED}$     | LED PWM switching frequency           | PWM_HF = 1<br>Frequency defined by internal oscillator                 |          | 558  |        | Hz      |
|               |                                       | PWM_HF = 0<br>Frequency defined by 32 kHz clock (internal or external) |          | 256  |        | Hz      |
| $V_{SAT}$     | Saturation voltage ( <i>Note 12</i> ) | $I_{OUT}$ set to 17.5 mA   |          | 50   | 100    | mV      |

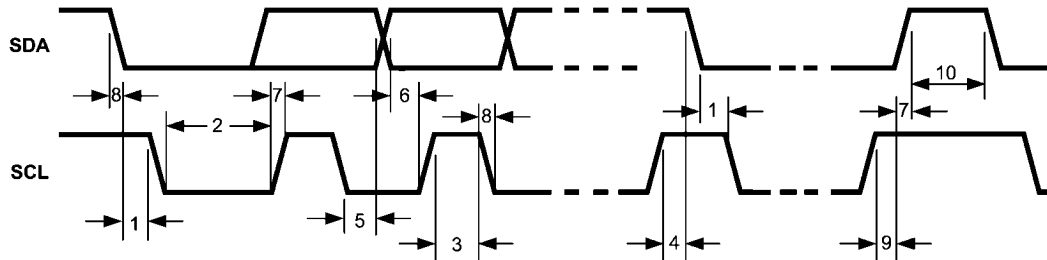
## Logic Interface Characteristics

(V(EN) = 1.65V... $V_{DD}$  unless otherwise noted)

| Symbol                                      | Parameter              | Conditions                         | Min            | Typ            | Max           | Units   |
|---|------------------------|------------------------------------|----------------|----------------|---------------|---------|
| <b>LOGIC INPUT EN</b>                       |                        |                                    |                |                |               |         |
| $V_{IL}$                                    | Input Low Level        |                                    |                |                | 0.5           | V       |
| $V_{IH}$                                    | Input High Level       |                                    | 1.2            |                |               | V       |
| $I_I$                                       | Logic Input Current    |                                    | -1.0           |                | 1.0           | $\mu A$ |
| $t_{DELAY}$                                 | Input delay            |                                    |                | 2              |               | $\mu s$ |
| <b>LOGIC INPUT SCL, SDA, TRIG, CLK_32K</b>  |                        |                                    |                |                |               |         |
| $V_{IL}$                                    | Input Low Level        |                                    |                |                | 0.2xV(EN)     | V       |
| $V_{IH}$                                    | Input High Level       |                                    | 0.8xV(EN)      |                |               | V       |
| $I_I$                                       | Input Current          |                                    | -1.0           |                | 1.0           | $\mu A$ |
| $f_{CLK\_32K}$                              | Clock frequency        |                                    |                | 32             |               | kHz     |
| $f_{SCL}$                                   | Clock frequency        |                                    |                |                | 400           | kHz     |
| <b>LOGIC OUTPUT SDA, TRIG, INT</b>          |                        |                                    |                |                |               |         |
| $V_{OL}$                                    | Output Low Level       | $I_{OUT} = 3 mA$ (pull-up current) |                | 0.3            | 0.5           | V       |
| $I_L$                                       | Output Leakage Current |                                    |                |                | 1.0           | $\mu A$ |
| <b>LOGIC INPUT ADDR_SEL0, ADDR_SEL1</b>     |                        |                                    |                |                |               |         |
| $V_{IL}$                                    | Input Low Level        |                                    |                |                | 0.2x $V_{DD}$ | V       |
| $V_{IH}$                                    | Input High Level       |                                    | 0.8x $V_{DD}$  |                |               | V       |
| $I_I$                                       | Input Current          |                                    | -1.0           |                | 1.0           | $\mu A$ |
| <b>LOGIC OUTPUT GPO, INT (in GPO state)</b> |                        |                                    |                |                |               |         |
| $V_{OL}$                                    | Output Low Level       | $I_{OUT} = 3 mA$                   |                | 0.3            | 0.5           | V       |
| $V_{OH}$                                    | Output High Level      | $I_{OUT} = -2 mA$                  | $V_{DD} - 0.5$ | $V_{DD} - 0.3$ |               | V       |
| $I_L$                                       | Output leakage current |                                    |                |                | 1.0           | $\mu A$ |

## I<sup>2</sup>C Timing Parameters (SDA, SCL) *(Note 13)*

| Symbol    | Parameter  | Limit       |     | Units   |
|-----------|--|-------------|-----|---------|
|           |  | Min         | Max |         |
| $f_{SCL}$ | Clock Frequency                                    |             | 400 | kHz     |
| 1         | Hold Time (repeated) START Condition               | 0.6         |     | $\mu$ s |
| 2         | Clock Low Time                                     | 1.3         |     | $\mu$ s |
| 3         | Clock High Time                                    | 600         |     | ns      |
| 4         | Setup Time for a Repeated START Condition          | 600         |     | ns      |
| 5         | Data Hold Time                                     | 50          |     | ns      |
| 6         | Data Setup Time                                    | 100         |     | ns      |
| 7         | Rise Time of SDA and SCL                           | $20+0.1C_b$ | 300 | ns      |
| 8         | Fall Time of SDA and SCL                           | $15+0.1C_b$ | 300 | ns      |
| 9         | Set-up Time for STOP condition                     | 600         |     | ns      |
| 10        | Bus Free Time between a STOP and a START Condition | 1.3         |     | $\mu$ s |
| $C_b$     | Capacitive Load for Each Bus Line                  | 10          | 200 | pF      |



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**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

**Note 2:** All voltages are with respect to the potential at the GND pins.

**Note 3:** Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at  $T_J = 150^\circ\text{C}$  (typ.) and disengages at  $T_J = 130^\circ\text{C}$  (typ.).

**Note 4:** For detailed soldering specifications and information, please refer to National Semiconductor Application Note AN1112 : Micro SMD Wafer Level Chip Scale Package or AN1187 : Leadless Leadframe Package (LLP).

**Note 5:** The Human body model is a 100 pF capacitor discharged through a 1.5 k $\Omega$  resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin. MIL-STD-883 3015.7

**Note 6:** In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ( $T_{A-MAX}$ ) is dependent on the maximum operating junction temperature ( $T_{J-MAX-OP} = 125^\circ\text{C}$ ), the maximum power dissipation of the device in the application ( $P_{D-MAX}$ ), and the junction-to ambient thermal resistance of the part/package in the application ( $\theta_{JA}$ ), as given by the following equation:  $T_{A-MAX} = T_{J-MAX-OP} - (\theta_{JA} \times P_{D-MAX})$ .

**Note 7:** Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

**Note 8:** Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.

**Note 9:** Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.

**Note 10:** Input, output, and fly capacitors should be of the type X5R or X7R low ESR ceramic capacitor.

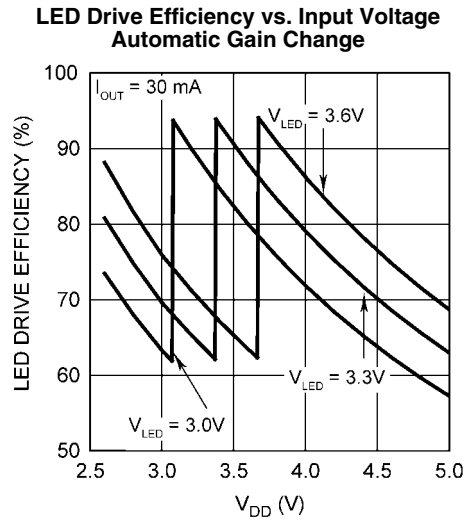
**Note 11:** Matching is the maximum difference from the average of the three output's currents.

**Note 12:** Saturation voltage is defined as the voltage when the LED current has dropped 10% from the value measured at  $V_{OUT} - 1V$ .

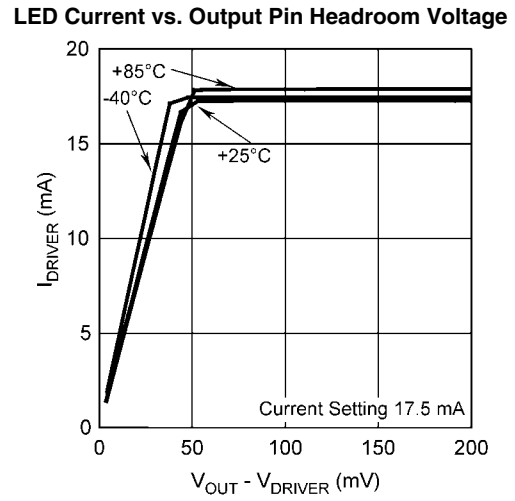
**Note 13:** Guaranteed by design.

# Typical Performance Characteristics

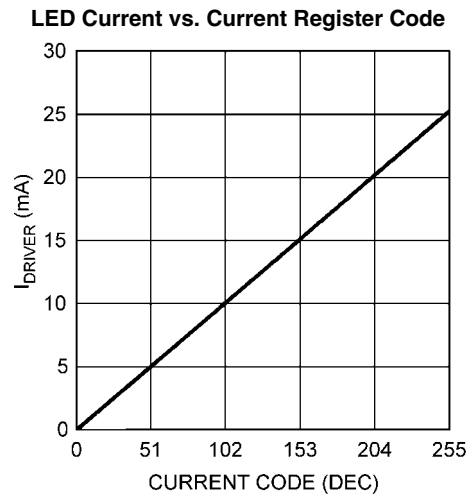
Unless otherwise specified:  $V_{DD} = 3.6V$



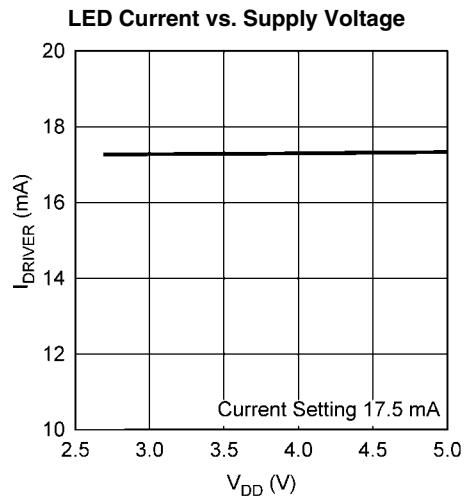
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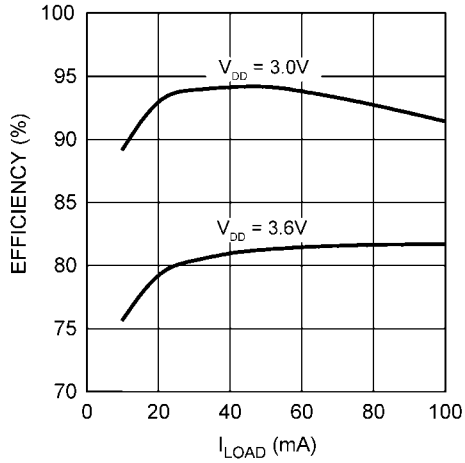


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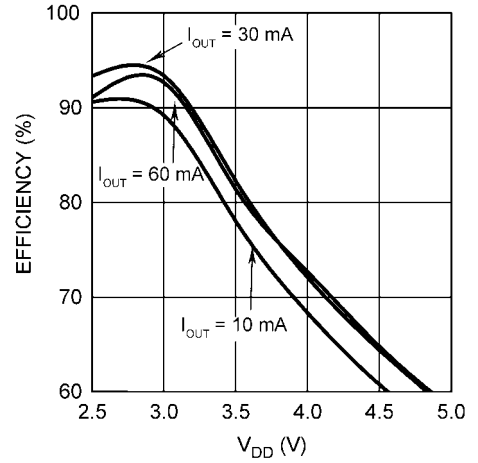
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Charge Pump Efficiency vs. Load Current



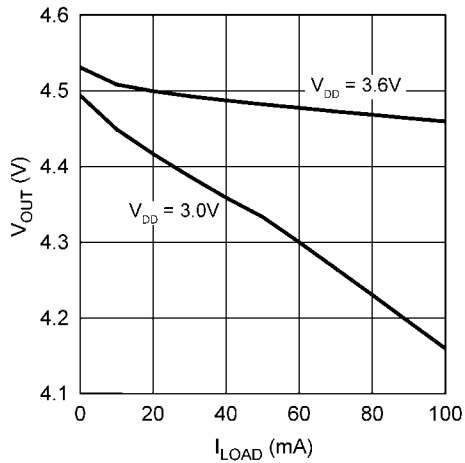
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Charge Pump Efficiency vs. Input Voltage  
1.5x Mode



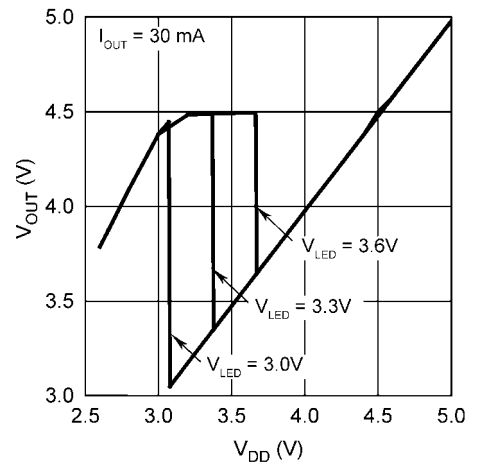
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Charge Pump Output Voltage vs. Load Current



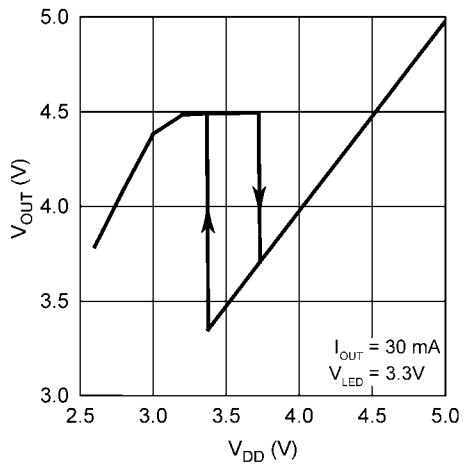
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Charge Pump Output Voltage vs. Input Voltage  
Automatic Gain Change from 1x to 1.5x



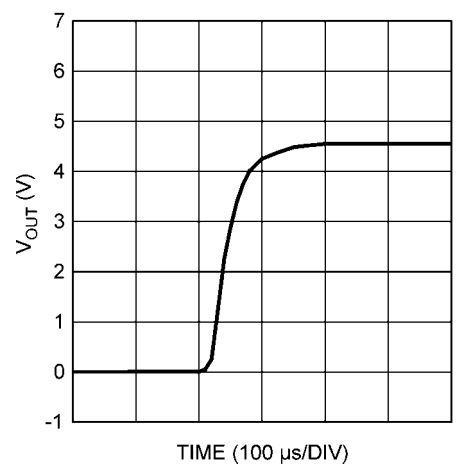
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Charge Pump Automatic Gain Change Hysteresis



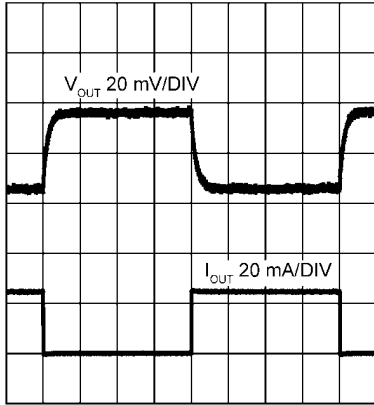
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Charge Pump Startup in 1.5x Mode  
No Load



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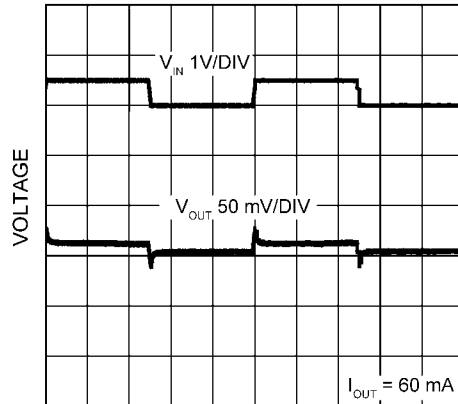
**Charge Pump Load Transient Response in 1.5x Mode (0 to 25.5 mA)**



TIME (500  $\mu$ s/DIV)

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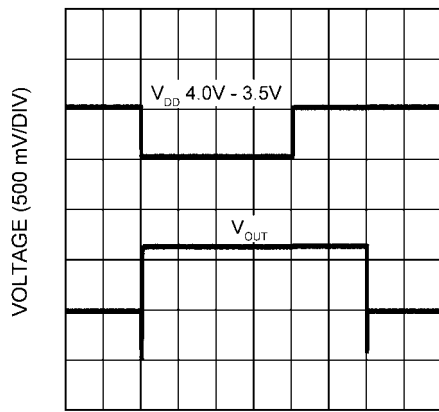
**Charge Pump Line Transient Response 1.5x Mode ( $V_{IN}$  3.5V to 4.0V)**



TIME (200  $\mu$ s/DIV)

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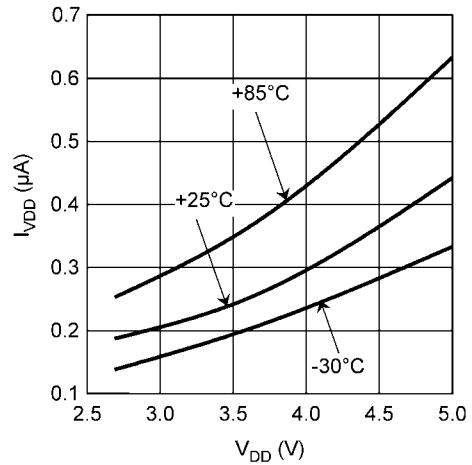
**Charge Pump Automatic Gain Change (LED  $V_F = 3.6$ V)**



TIME (5 ms/DIV)

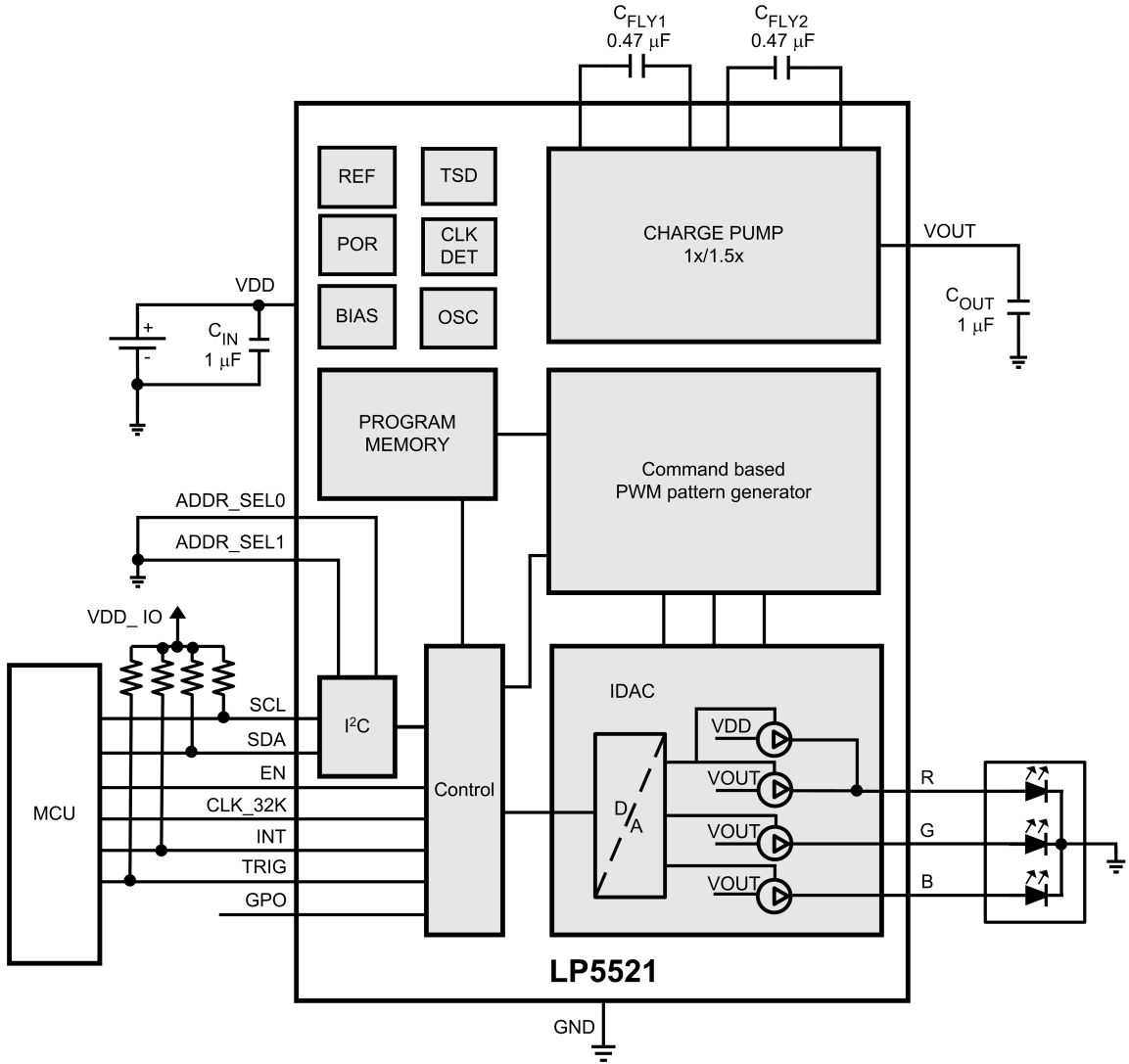
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**Standby Current vs. Input Voltage**



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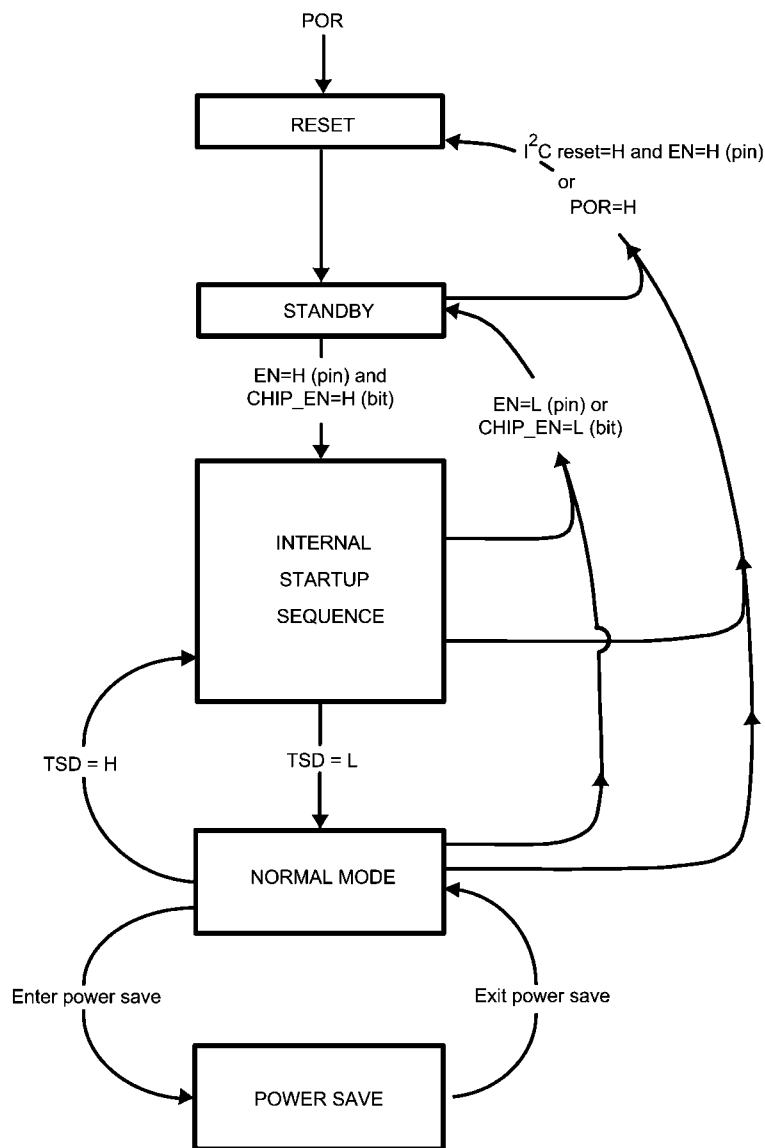
# Block Diagram



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## Modes of Operation

- RESET:** In the RESET mode all the internal registers are reset to the default values. Reset is done always if Reset Register (0DH) is written FFH or internal Power On Reset (POR) will activate when supply voltage is connected or when the supply voltage  $V_{DD}$  falls below 1.5V typ (0.8V min). Once  $V_{DD}$  rises above 1.5V, POR will inactivate and the chip will continue to the STANDBY mode. CHIP\_EN control bit is low after POR by default.
- STANDBY:** The STANDBY mode is entered if the register bit CHIP\_EN or EN pin is LOW and Reset is not active. This is the low power consumption mode, when all circuit functions are disabled. Registers can be written in this mode if EN pin is high. Control bits are effective after start up.
- STARTUP:** When CHIP\_EN bit is written high and EN pin is high, the INTERNAL STARTUP SEQUENCE powers up all the needed internal blocks ( $V_{REF}$ , Bias, Oscillator etc.). Startup delay is 500  $\mu$ s. If the chip temperature rises too high, the Thermal Shutdown (TSD) disables the chip operation and the chip state is in STARTUP mode, until no thermal shutdown event is present. (*Note 3*)
- NORMAL:** During NORMAL mode the user controls the chip using the Control Registers. If EN pin is set low, the CHIP\_EN bit is reset to 0.
- POWER SAVE:** In POWER SAVE mode analog blocks are disabled to minimize power consumption. See chapter Power Save Mode for further information.



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# Charge Pump Operational Description

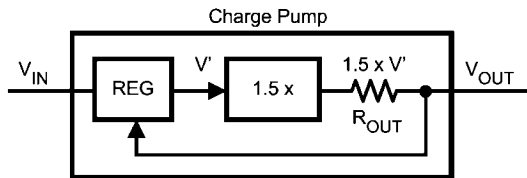
## OVERVIEW

The LP5521 includes a pre-regulated switched-capacitor charge pump with a programmable voltage multiplication of 1 and 1.5x.

On 1.5x mode by combining the principles of a switched-capacitor charge pump and a linear regulator, it generates a regulated 4.5V output from Li-Ion input voltage range. A two-phase non-overlapping clock generated internally controls the operation of the charge pump. During the charge phase, both flying capacitors ( $C_{FLY1}$  and  $C_{FLY2}$ ) are charged from input voltage. In the pump phase that follows, the flying capacitors are discharged to output. A traditional switched capacitor charge pump operating in this manner will use switches with very low on-resistance, ideally  $0\Omega$ , to generate an output voltage that is 1.5x the input voltage. The LP5521 regulates the output voltage by controlling the resistance of the input-connected pass-transistor switches in the charge pump.

## OUTPUT RESISTANCE

At lower input voltages, the charge pump output voltage may degrade due to effective output resistance ( $R_{OUT}$ ) of the charge pump. The expected voltage drop can be calculated by using a simple model for the charge pump illustrated in following figure.



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The model shows a linear pre-regulation block (REG), a voltage multiplier (1.5x), and an output resistance ( $R_{OUT}$ ). Output resistance models the output voltage drop that is inherent to switched capacitor converters. The output resistance is  $3.5\Omega$  (typ), and is function of switching frequency, input voltage, flying capacitors' capacitance value, internal resistances of switches and ESR of flying capacitors. When the output voltage is in regulation, the regulator in the model controls the voltage  $V'$  to keep the output voltage equal to 4.5V (typ). With increased output current, the voltage drop across  $R_{OUT}$  increases. To prevent drop in output voltage, the voltage drop across the regulator is reduced,  $V'$  increases, and  $V_{OUT}$  remains at 4.5V. When the output current increases to the point that there is zero voltage drop across the regulator,  $V'$  equals the input voltage, and the output voltage is "on the edge" of regulation. Additional output current causes the output voltage to fall out of regulation, so that the operation is similar to a basic open-loop 1.5x charge pump. In this mode, output current results in output voltage drop proportional to the output resistance of the charge pump. The out-of-regulation output voltage can be approximated by:  $V_{OUT} = 1.5 \times V_{IN} - I_{OUT} \times R_{OUT}$ .

## CONTROLLING CHARGE PUMP

Charge pump is controlled with two CP\_MODE bits in register 08H. When both bits are low, charge pump is disabled and output voltage is pulled down with  $300\text{ k}\Omega$ . Charge pump can be forced to bypass mode, so battery voltage is going directly to RGB outputs. In 1.5x mode output voltage is boosted to 4.5V. In automatic mode, charge pump operation mode is defined by LED outputs saturation like described in LED Forward Voltage Monitoring. In following table are listed operation modes and selection bits.

CONFIG register (08H):

| Name    | Bit | Description  |
|---------|-----|--|
| CP_MODE | 4:3 | Charge Pump Operation Mode<br>00b = OFF<br>01b = Forced to bypass mode (1x)<br>10b = Forced to 1.5x mode<br>11b = Automatic mode selection |

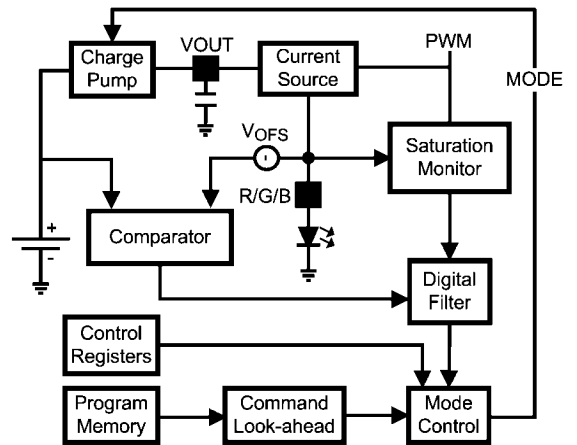
## LED FORWARD VOLTAGE MONITORING

When charge pump automatic mode selection is enabled, voltages over LED drivers are monitored. If drivers do not have enough headroom, charge pump gain is set to 1.5x. Driver saturation monitor does not have a fixed voltage limit, since saturation voltage is a function of temperature and current. Charge pump gain is set to 1x, when battery voltage is high enough to supply all LEDs.

In automatic gain change mode, charge pump is switched to bypass mode (1x), when LEDs are inactive for over 50 ms.

Charge pump gain control utilizes digital filtering to prevent supply voltage disturbances from triggering gain changes. If R driver current source is connected to battery (address 08H, bit R\_TO\_BATT = 1) voltage monitoring is disabled in R output, but still functional in B and G output.

LED forward voltage monitoring and gain control block diagram is shown below.



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Voltage monitoring block diagram for one output

## LED Driver Operational Description

The LP5521 LED drivers are constant current sources with 8-bit PWM control. Output current can be programmed with I<sup>2</sup>C register up to 25.5 mA. Current setting resolution is 100  $\mu$ A (8-bit control).

R driver has two modes: current source can be connected to battery ( $V_{DD}$ ) or to charge pump output. If current source is connected to battery, automatic charge pump gain control is not used for this output. This approach provides better efficiency when LED with low  $V_F$  is connected to R driver, and battery voltage is high enough to drive this LED in all conditions. R driver mode can be selected with I<sup>2</sup>C register bit. When address 08H, bit R\_TO\_BATT = 1, R current source is connected to battery. When it is 0 (default), R current source is connected to charge pump same way as in G and B drivers. G and B drivers are always connected to charge pump output.

Some LED configuration examples are given in table below. When LEDs with low  $V_F$  are used, charge pump can be operating in bypass mode (1x). This eliminates the need of having double drivers for all outputs; one connected to battery and another connected to charge pump output. When LP5521 is driving a RGB LED, R channel can be configured to use battery power. This configuration increases power efficiency by minimizing the voltage drop across the LED driver.

### LED configuration examples

| Configuration                | R output to BATT | R output to CP | CP Mode           |
|------------------------------|------------------|----------------|-------------------|
| RGB LED with low $V_F$ red   | X                |                | Auto (1x or 1.5x) |
| 3 x low $V_F$ LED            |                  | X              | 1x                |
| 3 x white LED                |                  | X              | Auto (1x or 1.5x) |
| 1 x low $V_F$ LED (R output) | X                |                | Disabled          |

PWM frequency is either 256 Hz or 558 Hz, frequency is set with PWM\_HF bit in register 08H. When PWM\_HF is 0, then the frequency is 256 Hz, and when bit is 1 then the PWM frequency is 558 Hz. Brightness adjustment is either linear or logarithmic. This can be set with register 00H LOG\_EN bit. When LOG\_EN = 0 linear adjustment scale is used, and when LOG\_EN = 1 logarithmic scale is used. By using logarithmic scale the visual effect seems linear to the eye. Register control bits are presented in following tables:

### R\_CURRENT register (05H), G\_CURRENT register (06H), B\_CURRENT register (07H):

| Name      | Bit | Description      |           |            |                   |
|-----------|-----|------------------|-----------|------------|-------------------|
| CURRENT   | 7:0 | Current setting  |           |            |                   |
|           |     | bin              | hex       | dec        | mA                |
|           |     | 0000 0000        | 00        | 0          | 0.0               |
|           |     | 0000 0001        | 01        | 1          | 0.1               |
|           |     | 0000 0010        | 02        | 2          | 0.2               |
|           |     | 0000 0011        | 03        | 3          | 0.3               |
|           |     | 0000 0100        | 04        | 4          | 0.4               |
|           |     | 0000 0101        | 05        | 5          | 0.5               |
|           |     | 0000 0110        | 06        | 6          | 0.6               |
|           |     | ...              | ...       | ...        | ...               |
|           |     | <b>1010 1111</b> | <b>AF</b> | <b>175</b> | <b>17.5 (def)</b> |
|           |     | ...              | ...       | ...        | ...               |
|           |     | 1111 1011        | FB        | 251        | 25.1              |
| 1111 1100 | FC  | 252              | 25.2      |            |                   |
| 1111 1101 | FD  | 253              | 25.3      |            |                   |
| 1111 1110 | FE  | 254              | 25.4      |            |                   |
| 1111 1111 | FF  | 255              | 25.5      |            |                   |

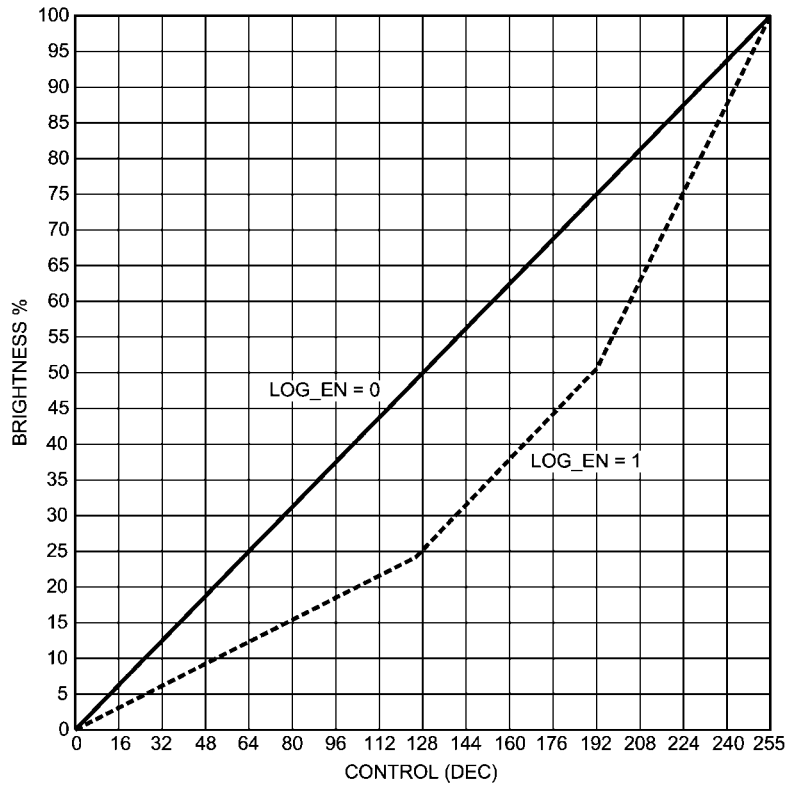
### ENABLE register (00H):

| Name   | Bit | Description  |
|--------|-----|--|
| LOG_EN | 7   | Logarithmic PWM adjustment enable bit<br>0 = Linear adjustment<br>1 = Logarithmic adjustment |

### CONFIG register (08H):

| Name   | Bit | Description   |
|--------|-----|---|
| PWM_HF | 6   | PWM clock frequency<br>0 = 256 Hz, frequency defined by 32 kHz clock (internal or external)<br>1 = 558 Hz, frequency defined by internal oscillator |

Logarithmic and Linear PWM Adjustment Curves



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### LED Controller Operation Modes

Operation modes are defined in register address 01H. Each output channel (R, G, B) operation mode can be configured

separately. MODE registers are synchronized to 32 kHz clock. Delay between consecutive I<sup>2</sup>C writes to OP\_MODE register (01H) need to be longer than 153 μs (typ).

OP\_MODE register (01H):

| Name   | Bit | Description   |
|--------|-----|---|
| R_MODE | 5:4 | R channel operation mode<br><b>00b</b> = Disabled, reset R channel PC<br><b>01b</b> = Load program to SRAM, reset R channel PC<br><b>10b</b> = Run program defined by R_EXEC<br><b>11b</b> = Direct control, reset R channel PC |
| G_MODE | 3:2 | G channel operation mode<br><b>00b</b> = Disabled, reset G channel PC<br><b>01b</b> = Load program to SRAM, reset G channel PC<br><b>10b</b> = Run program defined by G_EXEC<br><b>11b</b> = Direct control, reset G channel PC |
| B_MODE | 1:0 | B channel operation mode<br><b>00b</b> = Disabled, reset B channel PC<br><b>01b</b> = Load program to SRAM, reset B channel PC<br><b>10b</b> = Run program defined by B_EXEC<br><b>11b</b> = Direct control, reset B channel PC |

**DISABLED**

Each channel can be configured to disabled mode. LED output current will be 0 during this mode. Disabled mode resets respective channel's PC.

**LOAD Program**

LP5521 can store 16 commands for each channel (R, G, B). Each command consists of 16 bits. Because one register has only 8 bits, one command requires two I<sup>2</sup>C register addresses. In order to reduce program load time LP5521 supports address auto incrementation. Register address is incremented after each 8 data bits. Whole program memory can be written in one I<sup>2</sup>C write sequence.

Program memory is defined in the LP5521 register table, 10H to 2FH for R channel, 30H to 4FH for G channel and 50H to 6FH for B channel. In order to be able to access program memory at least one channel operation mode needs to be LOAD Program.

Memory writes are allowed only to the channel in LOAD mode. All channels are in hold while one or several channels are in LOAD program mode, and PWM values are frozen for the channels which are not in LOAD mode. Program execu-

tion continues when all channels are out of LOAD program mode. LOAD Program mode resets respective channel's PC.

**RUN PROGRAM**

RUN Program mode executes the commands defined in program memory for respective channel (R, G, B). Execution register bits in ENABLE register define how program is executed. Program start position can be programmed to Program Counter register (see the following tables). By manually selecting the PC start value, user can write different lighting sequences to the memory, and select appropriate sequence with the PC register. If program counter runs to end (15) the next command will be executed from program location 0.

If internal clock is used in the RUN program mode, operation mode needs to be written disabled (00b) before disabling the chip (with CHIP\_EN bit or EN pin) to ensure that the sequence starts from the correct program counter (PC) value when restarting the sequence.

PC registers are synchronized to 32 kHz clock. Delay between consecutive I<sup>2</sup>C writes to PC registers (09H, 0AH, 0BH) need to be longer than 153  $\mu$ s (typ.).

**R Channel PC register (09H), G CHANNEL PC register (0AH), B CHANNEL PC register (0BH)**

| Name | Bit | Description                         |
|------|-----|-------------------------------------|
| PC   | 3:0 | Program counter value from 0 to 15d |

**ENABLE register (00H)**

| Name   | Bit | Description  |
|--------|-----|--|
| R_EXEC | 5:4 | R channel program execution<br><b>00b</b> = Hold: Wait until current command is finished then stop while EXEC mode is hold. PC can be read or written only in this mode.<br><b>01b</b> = Step: Execute instruction defined by current R channel PC value, increment PC and change R_EXEC to 00b (Hold)<br><b>10b</b> = Run: Start at program counter value defined by current R channel PC value<br><b>11b</b> = Execute instruction defined by current R channel PC value and change R_EXEC to 00b (Hold) |
| G_EXEC | 3:2 | G channel program execution<br><b>00b</b> = Hold: Wait until current command is finished then stop while EXEC mode is hold. PC can be read or written only in this mode.<br><b>01b</b> = Step: Execute instruction defined by current G channel PC value, increment PC and change G_EXEC to 00b (Hold)<br><b>10b</b> = Run: Start at program counter value defined by current G channel PC value<br><b>11b</b> = Execute instruction defined by current G channel PC value and change G_EXEC to 00b (Hold) |
| B_EXEC | 1:0 | B channel program execution<br><b>00b</b> = Hold: Wait until current command is finished then stop while EXEC mode is hold. PC can be read or written only in this mode.<br><b>01b</b> = Step: Execute instruction defined by current B channel PC value, increment PC and change B_EXEC to 00b (Hold)<br><b>10b</b> = Run: Start at program counter value defined by current B channel PC value<br><b>11b</b> = Execute instruction defined by current B channel PC value and change B_EXEC to 00b (Hold) |

EXEC registers are synchronized to 32 kHz clock. Delay between consecutive I<sup>2</sup>C writes to ENABLE register (00H) need to be longer than 488  $\mu$ s (typ.).

**DIRECT Control**

When R, G or B channel mode is set to 00b, the LP5521 drivers work in direct control mode. LP5521 LED channels can be controlled independently through I<sup>2</sup>C. For each channel there is a PWM control register and a output current

control register. With output current control register is set what is the maximum output current with 8-bit resolution, step size is 100 μA. Duty cycle can be set with 8-bit resolution. Direct control mode resets respective channel's PC. PWM control bits are presented in following table:

**R\_PWM register (02H), G\_PWM register (03H), B\_PWM register (04H):**

| Name | Bit | Description  |
|------|-----|--|
| PWM  | 7:0 | LED PWM value during direct control operation mode<br>0000 0000b = 0%<br>1111 1111b = 100% |

If charge pump automatic gain change is used in this mode, then PWM values need to be written 0 before changing the

drivers' operation mode to disabled (00b) to ensure proper automatic gain change operation.

## LED Controller Programming Commands

LP5521 has three independent programmable channels (R, G, B). Trigger connections between channels are common for all channels. All channels have own program memories for storing complex patterns. Brightness control and patterns are done with 8-bit PWM control (256 steps) to get accurate and smooth color control.

Program execution is timed with 32 768 Hz clock. This clock can be generated internally or external 32 kHz clock can be connected to CLK\_32K pin. Using external clock enables synchronization of LED timing to this clock rather than internal

clock. Selection of the clock is made with address 08H bits INT\_CLK\_EN and CLK\_DET\_EN. See External Clock Detection for details.

Supported commands are listed in the table below. **Command compiler is available for easy sequence programming. With Command compiler it is possible to write sequences with simple ASCII commands, which are then converted to binary or hex format. See application note "LP5521 Programming Considerations" for examples of Command compiler usage.**

| Command            | 15 | 14        | 13        | 12                               | 11    | 10 | 9 | 8         | 7                            | 6                     | 5 | 4 | 3 | 2 | 1 | 0 |   |
|--------------------|----|-----------|-----------|----------------------------------|-------|----|---|-----------|------------------------------|-----------------------|---|---|---|---|---|---|---|
| <b>Ramp Wait</b>   | 0  | Pre-scale | Step time |                                  |       |    |   | Sign      | Increment (number of steps)  |                       |   |   |   |   |   |   |   |
| <b>Set PWM</b>     | 0  | 1         | 0         |                                  |       |    |   | PWM Value |                              |                       |   |   |   |   |   |   |   |
| <b>Go to Start</b> | 0  | 0         | 0         |                                  |       |    |   | 0         | 0                            | 0                     | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| <b>Branch</b>      | 1  | 0         | 1         | Loop count                       |       |    |   |           | x                            | Step / command number |   |   |   |   |   |   |   |
| <b>End</b>         | 1  | 1         | 0         | Int                              | Reset | X  |   |           |                              |                       |   |   |   |   |   |   |   |
| <b>Trigger</b>     | 1  | 1         | 1         | Wait for trigger on channels 5-0 |       |    |   |           | Send trigger on channels 5-0 |                       |   |   |   | X |   |   |   |

X means do not care whether 1 or 0.

### Ramp/Wait

Ramp command generates a PWM ramp starting from current value. At each ramp step the output is incremented by one. Time for one step is defined with Prescale and Step time bits. Minimum time for one step is 0.49 ms and maximum time is 63 x 15.6 ms = 1 second/step, so it is possible to program very fast and also very slow ramps. Increment value defines how many steps are taken in one command. Number of actual steps is Increment + 1. Maximum value is 127d, which corresponds to half of full scale (128 steps). If during ramp command PWM reaches minimum/maximum (0/255) ramp command will be executed to the end and PWM will stay at

minimum/maximum. This enables ramp command to be used as combined ramp and wait command in a single instruction. Ramp command can be used as wait instruction when increment is zero.

Setting register 00H bit LOG\_EN sets the scale from linear to logarithmic. When LOG\_EN = 0 linear scale is used, and when LOG\_EN = 1 logarithmic scale is used. By using logarithmic scale the visual effect of the ramp command seems linear to the eye.

| Ramp/Wait command |           |           |    |    |    |   |      |           |   |   |   |   |   |   |   |
|-------------------|-----------|-----------|----|----|----|---|------|-----------|---|---|---|---|---|---|---|
| 15                | 14        | 13        | 12 | 11 | 10 | 9 | 8    | 7         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0                 | Pre-scale | Step time |    |    |    |   | Sign | Increment |   |   |   |   |   |   |   |

| Name      | Value(d) | Description  |
|-----------|----------|--|
| Prescale  | 0        | Divides master clock (32 768Hz) by 16 = 2048 Hz, 0.49 ms cycle time                            |
|           | 1        | Divides master clock (32 768Hz) by 512 = 64 Hz, 15.6 ms cycle time                             |
| Step time | 1-63     | One ramp increment done in (step time) x (clock after prescale) Note: 0 means Set PMW command. |
| Sign      | 0        | Increase PWM output  |
|           | 1        | Decrease PWM output  |
| Increment | 0-127    | The number of steps is Increment + 1. Note: 0 is a wait instruction.                           |

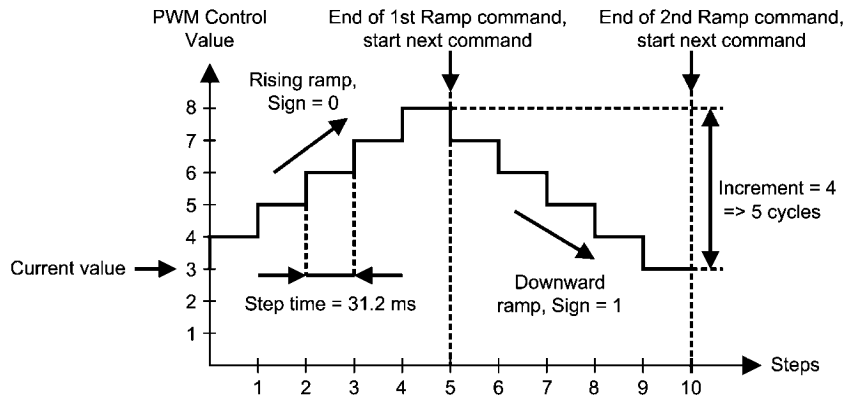
**Application example:**

For example if following parameters are used for ramp:

- Prescale = 1 => cycle time = 15.6 ms
- Step time = 2 => time = 15.6 ms x 2 = 31.2 ms
- Sign = 0 => rising ramp
- Increment = 4 => 5 cycles

Ramp command will be: 0100 0010 0000 0100b = 4204H

If current PWM value is 3, and the first command is as described above and next command is a ramp with otherwise same parameters, but with Sign = 1 (Command = 4284H), the result will be like in the following figure:



**Example of 2 sequential ramp commands.**

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**Set PWM**

Set PWM output value from 0 to 255. Command takes sixteen 32 kHz clock cycles (= 488 μs). Setting register 00H bit LOG\_EN sets the scale from linear to logarithmic.

| Set PWM command |    |    |    |    |    |   |   |           |   |   |   |   |   |   |   |
|-----------------|----|----|----|----|----|---|---|-----------|---|---|---|---|---|---|---|
| 15              | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0               | 1  | 0  | 0  | 0  | 0  | 0 | 0 | PWM value |   |   |   |   |   |   |   |

**Go to start**

Go to start command resets Program Counter register and continues executing program from the 00H location. Com-

mand takes sixteen 32 kHz clock cycles. Note that default value for all program memory registers is 0000H, which is Go to start command.

| Go to start command |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15                  | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0                   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Branch**

When branch command is executed, the 'step number' value is loaded to PC and program execution continues from this location. Looping is done by the number defined in loop count

parameter. Nested looping is supported (loop inside loop). The number of nested loops is not limited. Command takes sixteen 32kHz clock cycles.

| Branch command |    |    |            |    |    |   |   |   |   |   |   |             |   |   |   |  |
|----------------|----|----|------------|----|----|---|---|---|---|---|---|-------------|---|---|---|--|
| 15             | 14 | 13 | 12         | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3           | 2 | 1 | 0 |  |
| 1              | 0  | 1  | Loop count |    |    |   |   |   | X | X | X | Step number |   |   |   |  |

| Name        | Value(d) | Description  |
|-------------|----------|--|
| loop count  | 0-63     | The number of loops to be done. 0 means infinite loop. |
| step number | 0-15     | The step number to be loaded to program counter.       |

**End**

End program execution, resets the program counter and sets the corresponding EXEC register to 00b (hold). Command takes sixteen 32 kHz clock cycles.

| End command |    |    |     |       |    |   |   |   |   |   |   |   |   |   |   |
|-------------|----|----|-----|-------|----|---|---|---|---|---|---|---|---|---|---|
| 15          | 14 | 13 | 12  | 11    | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 1           | 1  | 0  | int | reset | X  | X | X | X | X | X | X | X | X | X | X |

| Name  | Value | Description  |
|-------|-------|--|
| int   | 0     | No interrupt will be sent.   |
|       | 1     | Send interrupt to processor by pulling the INT pin down and setting corresponding status register bit high to notify that program has ended. Interrupt can only be cleared by reading interrupt status register 0CH. |
| reset | 0     | Keep the current PWM value.  |
|       | 1     | Set PWM value to 0.  |

X means do not care whether 1 or 0.

### Trigger

Wait or send triggers can be used to e.g. synchronize operation between different channels. Send trigger command takes sixteen 32 kHz clock cycles and wait for trigger takes at least sixteen 32 kHz clock cycles. The receiving channel stores sent triggers. Received triggers are cleared by wait for trigger command if received triggers match to channels defined in the command. Channel waits for until all defined triggers have been received.

External trigger input signal must be at least two 32 kHz clock cycles (= 61  $\mu$ s typ.) long to be recognized. Trigger output

signal is three 32 kHz clock cycles (92  $\mu$ s typ.) long. External trigger signal is active low, i.e. when trigger is sent/received the pin is pulled to GND. Sent external trigger is masked, i.e. the device which has sent the trigger will not recognize it. If send and wait external trigger are used on the same command, the send external trigger is executed first, then the wait external trigger.

### Trigger command

| 15 | 14 | 13 | 12                 | 11 | 10 | 9 | 8 | 7                  | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|--------------------|----|----|---|---|--------------------|---|---|---|---|---|---|---|
| 1  | 1  | 1  | wait trigger <5:0> |    |    |   |   | send trigger <5:0> |   |   |   |   | X |   |   |
|    |    |    | EXT                | X  | B  | G | R | EXT                | X | B | G | R |   |   |   |

| Name              | Value(d) | Description  |
|-------------------|----------|--|
| wait trigger<5:0> | 0-31     | Wait for trigger for the channel(s) defined. Several triggers can be defined in the same command. Bit 0 is R, bit 1 is G, bit 2 is B and bit 5 is external trigger I/O. Bits 3 and 4 are not in use. |
| send trigger<5:0> | 0-31     | Send trigger for the channel(s) defined. Several triggers can be defined in the same command. Bit 0 is R, bit 1 is G, bit 2 is B and bit 5 is external trigger I/O. Bits 3 and 4 are not in use.     |

X means do not care whether 1 or 0.

## Power Save Mode

Automatic power save mode is enabled when PWRSAVE\_EN bit in register address 08H is 1. Almost all analog blocks are powered down in power save, if external clock is used. Only charge pump protection circuits remain active. However if internal clock has been selected only charge pump and led drivers are disabled during power save since digital part of the LED controller need to remain active. In both cases charge pump enters 'weak 1x' mode. In this mode charge pump utilizes a passive current limited keep-alive switch, which keeps the output voltage at battery level.

During program execution LP5521 can enter power save if there is no PWM activity in R, G and B outputs. To prevent short power save sequences during program execution, LP5521 has command look-ahead filter. In every instruction cycle R, G, B commands are analyzed, and if there is sufficient time left with no PWM activity, device will enter power save. In power save program execution continues uninterrupted. When a command that requires PWM activity is executed, fast internal start-up sequence will be started automatically. Following tables describe commands and conditions that can activate power save. All channels (R,G,B) need to meet power save condition in order to enable power save.

| LED controller operation mode (R,G,B_MODE) | Power save condition   |
|--|--|
| 00b  | Disabled mode enables power save   |
| 01b  | Load program to SRAM mode prevents power save  |
| 10b  | Run program mode enables power save if there is no PWM activity and command look-ahead filter condition is met |
| 11b  | Direct control mode enables power save if there is no PWM activity   |

| Command        | Power save condition  |
|----------------|---|
| Wait           | No PWM activity and current command wait time longer than 50 ms. If prescale = 1 then wait time needs to be longer than 80 ms.                                |
| Ramp           | Ramp Command PWM value reaches minimum 0 and current command execution time left more than 50 ms. If prescale = 1 then time left needs to be more than 80 ms. |
| Trigger        | No PWM activity during wait for trigger command execution.  |
| End            | No PWM activity or Reset bit = 1  |
| Set PWM        | Enables power save if PWM set to 0 and next command generates at least 50 ms wait   |
| Other commands | No effect to power save   |

See application note "LP5521 Power Efficiency Considerations" for more information.

## External Clock Detection

The presence of external clock can be detected by the LP5521. Program execution is clocked with internal 32 kHz clock or with external clock. Clocking is controlled with register address 08H bits, INT\_CLK\_EN and CLK\_DET\_EN as seen on the following table.

External clock can be used if clock is present at CLK\_32K pin. External clock frequency must be 32 kHz for the program execution / PWM timing to be like specified. If higher or lower frequency is used, it will affect the program engine execution speed. If other than 32kHz clock frequency is used, the program execution timings must be scaled accordingly. The external clock detector block only detects too low clock frequency (<15 kHz). If external clock frequency is higher than

specified, the external clock detector notifies that external clock is present. External clock status can be checked with read only bit EXT\_CLK\_USED in register address 0CH, when the external clock detection is enabled (CLK\_DET\_EN bit = high). If EXT\_CLK\_USED = 1, then the external clock is detected and it is used for timing, if automatic clock selection is enabled (see table below).

If external clock is stuck-at-zero or stuck-at-one, or the clock frequency is too low, the clock detector indicates that external clock is not present.

If external clock is not used on the application, CLK\_32K pin should be connected to GND to prevent floating of this pin and extra current consumption.

### CONFIG register (08H):

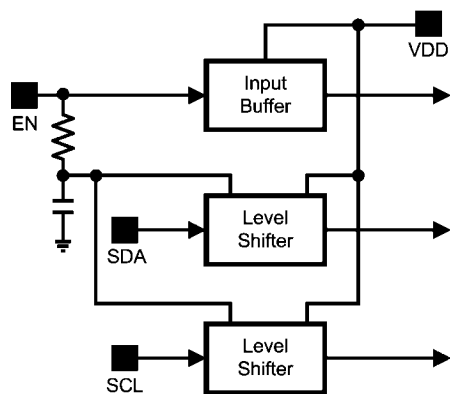
| Name                      | Bit | Description   |
|---------------------------|-----|---|
| CLK_DET_EN,<br>INT_CLK_EN | 1:0 | LED Controller clock source<br>00b = External clock source (CLK_32K)<br>01b = Internal clock<br>10b = Automatic selection<br>11b = Internal clock |

## Logic Interface Operational Description

LP5521 features a flexible logic interface for connecting to processor and peripheral devices. Communication is done with I<sup>2</sup>C compatible interface and different logic input/output pins makes it possible to synchronize operation of several devices.

### IO Levels

I<sup>2</sup>C interface, CLK\_32K and TRIG pins input levels are defined by EN pin. Using EN pin as voltage reference for logic inputs simplifies PWB routing and eliminates the need for dedicated V<sub>IO</sub> pin. In the following block diagram is described EN pin connections.



Using EN pin as digital IO voltage reference 20186254

ADDR\_SEL0/1 are referenced to V<sub>DD</sub> voltage. GPO pin level is defined by V<sub>DD</sub> voltage.

### GPO/INT pins

LP5521 has one General Purpose Output pin (GPO) and also INT pin can be configured as a GPO pin. When INT is configured as GPO output, it's level is defined by the V<sub>DD</sub> voltage. State of the pins can be controlled with GPO register (0EH). GPO pins are digital CMOS outputs and no pull-up/down resistors are needed.

When INT pin GPO function is disabled, it operates as an open drain pin. INT signal is active low, i.e. when interrupt signal is sent, the pin is pulled to GND. External pull-up resistor is needed for proper functionality.

GPO register (0EH)

| Name       | Bit | Description   |
|------------|-----|---|
| INT_AS_GPO | 2   | Enable INT pin GPO function<br>0 = INT pin functions as a INT pin<br>1 = INT pin functions as a GPO pin |
| GPO        | 1   | 0 = GPO pin state is low<br>1 = GPO pin state is high   |
| INT        | 0   | 0 = INT pin state is low<br>(INT_AS_GPO=1)<br>1 = INT pin state is high<br>(INT_AS_GPO=1)               |

### TRIG pin

TRIG pin can function as an external trigger input or output. External trigger signal is active low, i.e. when trigger is sent/received the pin is pulled to GND. TRIG is an open drain pin and external pull-up resistor is needed for trigger line. External trigger input signal must be at least two 32 kHz clock cycles long to be recognized. Trigger output signal is three 32 kHz clock cycles long. If TRIG pin is not used on application, it should be connected to GND to prevent floating of this pin and extra current consumption.

### ADDR\_SEL0,1 pins

ADDR\_SEL0,1 pins define the chip I<sup>2</sup>C address. Pins are referenced to V<sub>DD</sub> signal level. See I<sup>2</sup>C Compatible Serial Bus Interface chapter for I<sup>2</sup>C address definitions.

### CLK\_32K pin

CLK\_32K pin is used for connecting external 32 kHz clock to LP5521. External clock can be used to synchronize the sequence engines of several LP5521. Using external clock can also improve automatic power save mode efficiency, because internal clock can be switched off automatically when device has entered power save mode, and external clock is present. See application note "LP5521 Power Efficiency Considerations" for more information.

Device can be used without the external clock. If external clock is not used on the application, CLK\_32K pin should be connected to GND to prevent floating of this pin and extra current consumption.

# I<sup>2</sup>C Compatible Serial Bus Interface

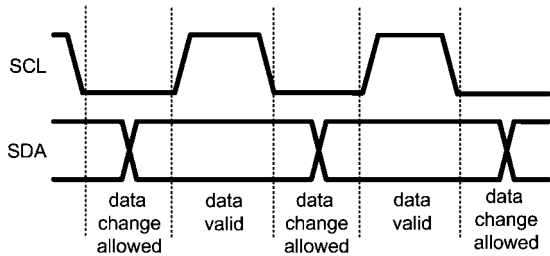
## Interface Bus Overview

The I<sup>2</sup>C compatible synchronous serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the IC's connected to the bus. The two interface lines are the Serial Data Line (SDA), and the Serial Clock Line (SCL). These lines should be connected to a positive supply, via a pull-up resistor and remain HIGH even when the bus is idle.

Every device on the bus is assigned a unique address and acts as either a Master or a Slave depending on whether it generates or receives the serial clock (SCL).

## Data Transactions

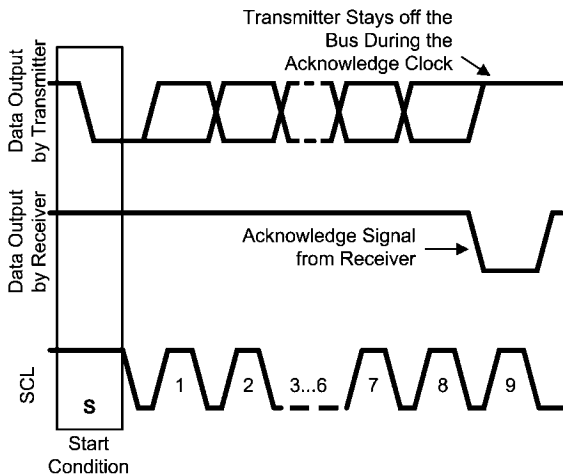
One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol permits a single data line to transfer both command/control information and data using the synchronous serial clock.



Data Validity

20186249

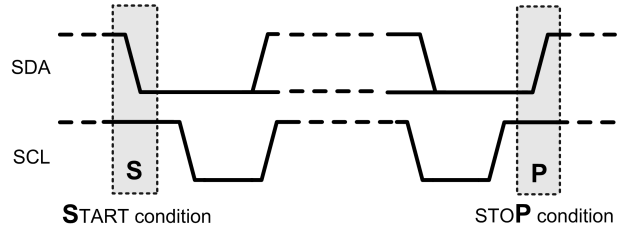
Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow. The following sections provide further details of this process.



Acknowledge Signal

20186220

The Master device on the bus always generates the Start and Stop Conditions (control codes). After a Start Condition is generated, the bus is considered busy and it retains this status until a certain time after a Stop Condition is generated. A high-to-low transition of the data line (SDA) while the clock (SCL) is high indicates a Start Condition. A low-to-high transition of the SDA line while the SCL is high indicates a Stop Condition.



Start and Stop Conditions

20186250

In addition to the first Start Condition, a repeated Start Condition can be generated in the middle of a transaction. This allows another device to be accessed, or a register read cycle.

## Acknowledge Cycle

The Acknowledge Cycle consists of two signals: the acknowledge clock pulse the master sends with each byte transferred, and the acknowledge signal sent by the receiving device.

The master generates the acknowledge clock pulse on the ninth clock pulse of the byte transfer. The transmitter releases the SDA line (permits it to go high) to allow the receiver to send the acknowledge signal. The receiver must pull down the SDA line during the acknowledge clock pulse and ensure that SDA remains low during the high period of the clock pulse, thus signaling the correct reception of the last data byte and its readiness to receive the next byte.

## "ACKNOWLEDGE AFTER EVERY BYTE" RULE

The master generates an acknowledge clock pulse after each byte transfer. The receiver sends an acknowledge signal after every byte received.

There is one exception to the "acknowledge after every byte" rule. When the master is the receiver, it must indicate to the transmitter an end of data by not-acknowledging ("negative acknowledge") the last byte clocked out of the slave. This "negative acknowledge" still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

## ADDRESSING TRANSFER FORMATS

Each device on the bus has a unique slave address. The LP5521 operates as a slave device with the 7-bit address. LP5521 I<sup>2</sup>C address is pin selectable from four different choices. If 8-bit address is used for programming, the 8th bit is 1 for read and 0 for write. In the following table is represented the 8-bit I<sup>2</sup>C addresses.

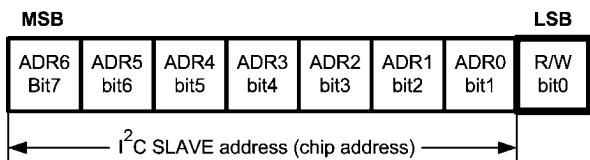
| ADDR_SEL [1:0] | I <sup>2</sup> C address write (8 bits) | I <sup>2</sup> C address read (8 bits) |
|----------------|---|--|
| 00             | 0110 0100 = 64H                         | 0110 0101 = 65H                        |
| 01             | 0110 0110 = 66H                         | 0110 0111 = 67H                        |
| 10             | 0110 1000 = 68H                         | 0110 1001 = 69H                        |
| 11             | 0110 1010 = 6AH                         | 0110 1011 = 6BH                        |

Before any data is transmitted, the master transmits the address of the slave being addressed. The slave device should send an acknowledge signal on the SDA line, once it recognizes its address.

The slave address is the first seven bits after a Start Condition. The direction of the data transfer (R/W) depends on the bit sent after the slave address — the eighth bit.

When the slave address is sent, each device in the system compares this slave address with its own. If there is a match, the device considers itself addressed and sends an acknowledge signal. Depending upon the state of the R/W bit (1:read, 0:write), the device acts as a transmitter or a receiver.

I<sup>2</sup>C chip address



20186251

**Control Register Write Cycle**

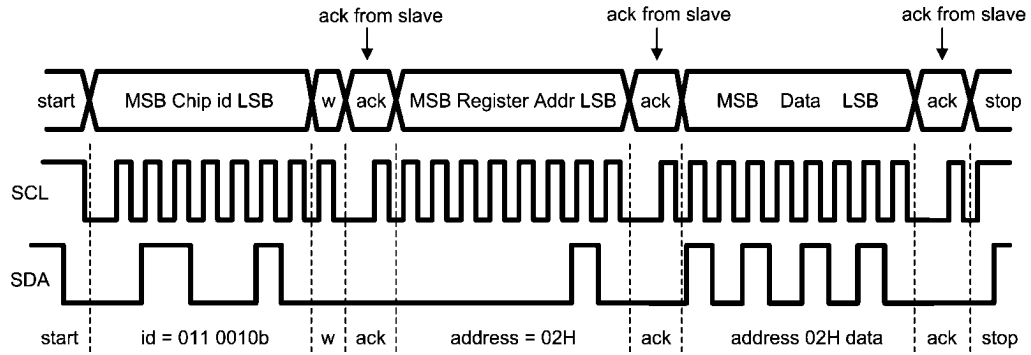
- Master device generates start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w = 0).
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master sends data byte to be written to the addressed register.
- Slave sends acknowledge signal.
- If master will send further data bytes the control register address will be incremented by one after acknowledge signal.
- Write cycle ends when the master creates stop condition.

**Control Register Read Cycle**

- Master device generates a start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w = 0).
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master device generates repeated start condition.
- Master sends the slave address (7 bits) and the data direction bit (r/w = 1).
- Slave sends acknowledge signal if the slave address is correct.
- Slave sends data byte from addressed register.
- If the master device sends acknowledge signal, the control register address will be incremented by one. Slave device sends data byte from addressed register.
- Read cycle ends when the master does not generate acknowledge signal after data byte and generates stop condition.

|            | Address Mode   |
|------------|--|
| Data Read  | <Start Condition><br><Slave Address><r/w = 0>[Ack]<br><Register Addr.>[Ack]<br><Repeated Start Condition><br><Slave Address><r/w = 1>[Ack]<br>[Register Data]<Ack or NAck><br>... additional reads from subsequent register address possible<br><Stop Condition> |
| Data Write | <Start Condition><br><Slave Address><r/w='0'>[Ack]<br><Register Addr.>[Ack]<br><Register Data>[Ack]<br>... additional writes to subsequent register address possible<br><Stop Condition>   |

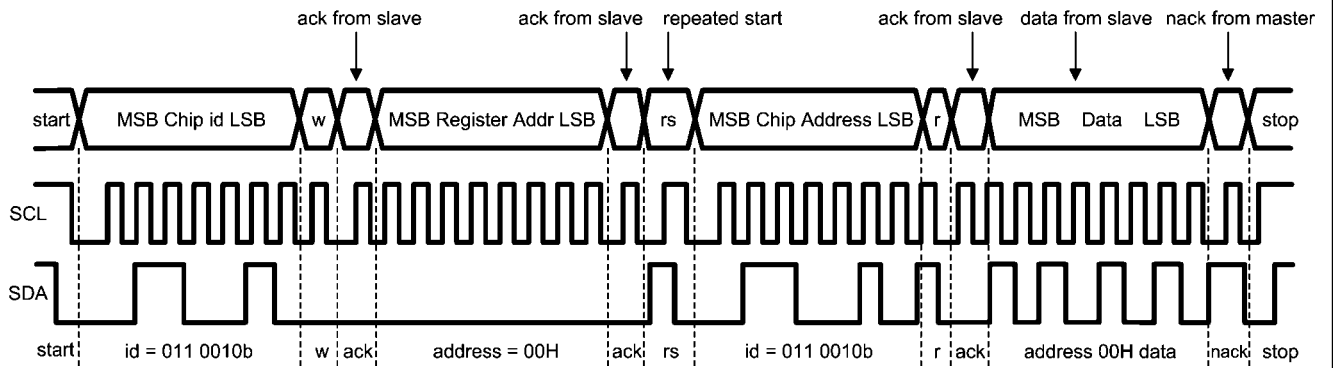
<>Data from master [ ] Data from slave



**Register Write Format**

20186293

When a READ function is to be accomplished, a WRITE function must precede the READ function, as show in the Read Cycle waveform



**Register Read Format**

20186294

w = write (SDA = 0)

r = read (SDA = 1)

ack = acknowledge (SDA pulled down by either master or slave)

rs = repeated start

id = 7-bit chip address

## Recommended External Components

### CAPACITOR SELECTION

The LP5521 requires 4 external capacitors for proper operation ( $C_{IN} = C_{OUT} = 1 \mu\text{F}$ ,  $C_{FLY1} = C_{FLY2} = 470 \text{ nF}$ ). Surface-mount multi-layer ceramic capacitors are recommended. These capacitors are small, inexpensive and have very low equivalent series resistance ( $\text{ESR} < 20 \text{ m}\Omega$  typ.). Tantalum capacitors, OS-CON capacitors, and aluminum electrolytic capacitors are not recommended for use with the LP5521 due to their high ESR, as compared to ceramic capacitors.

For most applications, ceramic capacitors with X7R or X5R temperature characteristic are preferred for use with the LP5521. These capacitors have tight capacitance tolerance (as good as  $\pm 10\%$ ) and hold their value over temperature (X7R:  $\pm 15\%$  over  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ ; X5R:  $\pm 15\%$  over  $-55^\circ\text{C}$  to  $85^\circ\text{C}$ ).

Capacitors with Y5V or Z5U temperature characteristic are generally not recommended for use with the LP5521. Capacitors with these temperature characteristics typically have

wide capacitance tolerance ( $+80\%$ ,  $-20\%$ ) and vary significantly over temperature (Y5V:  $+22\%$ ,  $-82\%$  over  $-30^\circ\text{C}$  to  $+85^\circ\text{C}$  range; Z5U:  $+22\%$ ,  $-56\%$  over  $+10^\circ\text{C}$  to  $+85^\circ\text{C}$  range). Under some conditions, a nominal  $1 \mu\text{F}$  Y5V or Z5U capacitor could have a capacitance of only  $0.1 \mu\text{F}$ . Such detrimental deviation is likely to cause Y5V and Z5U capacitors to fail to meet the minimum capacitance requirements of the LP5521.

The minimum voltage rating acceptable for all capacitors is 6.3V. The recommended voltage rating of the output capacitor is 10V to account for DC bias capacitance losses.

**Some ceramic capacitors, especially those in small packages, exhibit a strong capacitance reduction with the increased applied voltage (DC bias effect). The capacitance value can fall below half of the nominal capacitance. Choose output and input capacitor with DC bias voltage effect better than  $-50\%$  at 5V voltage ( $0.5 \mu\text{F}$  at 5V).**

### List of Recommended External Components

| Model  | Type                      | Vendor    | Voltage Rating | Size inch (mm) |
|--|---------------------------|-----------|----------------|----------------|
| <b>1 <math>\mu\text{F}</math> for <math>C_{OUT}</math> and <math>C_{IN}</math></b> |                           |           |                |                |
| C1005X5R1A105K   | Ceramic X5R               | TDK       | 10 V           | 0402 (1005)    |
| ECJ0EB1A105M   | Ceramic X5R               | Panasonic | 10 V           | 0402 (1005)    |
| ECJUVBPA105M   | Ceramic X5R, array of two | Panasonic | 10 V           | 0504           |
| <b>470 nF for <math>C_{FLY1-2}</math></b>  |                           |           |                |                |
| C1005X5R1A474K   | Ceramic X5R               | TDK       | 10 V           | 0402 (1005)    |
| ECJ0EB0J474K   | Ceramic X5R               | Panasonic | 10 V           | 0402 (1005)    |
| <b>LEDs</b>  | User Defined              |           |                |                |

## Program Load and Execution Example

### Startup Device and Configure Device to SRAM Write Mode:

- Supply e.g. 3.6V to VDD
- Supply e.g. 1.8V to EN
- Generate 32 kHz clock to CLK\_32K pin
- Write to address 00H 0100 0000b (enable LP5521)
- Wait 500  $\mu$ s (start-up delay)
- Write to address 01H 0001 0000b (Configure R channel into "Load program to SRAM" mode)

### Program Load to SRAM (see figure below):

- Write to address 10H 0000 0011b (1st ramp command 8 MSB)
- Write to address 11H 0111 1111b (1st ramp command 8 LSB)
- Write to address 12H 0100 1101b (1st wait command 8 MSB)
- Write to address 13H 0000 0000b (1st wait command 8 LSB)
- Write to address 14H 0000 0011b (2nd ramp command 8 MSB)
- Write to address 15H 1111 1111b (2nd ramp command 8 LSB)
- Write to address 16H 0110 0000b (2nd wait command 8 MSB)
- Write to address 17H 0000 0000b (2nd wait command 8 LSB)

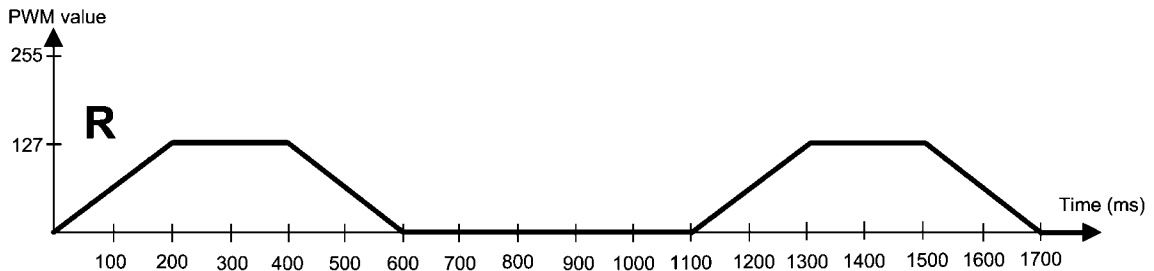
### Enable Powersave, charge pump automatic mode (1x / 1.5x) and use external 32 kHz clock:

- Write to address 08H 0011 1000b

### Run program:

- Write to address 01H 0010 0000b (Configure LED controller operation mode to "Run program" in R channel)
- Write to address 00H 0110 0000b (Configure program execution mode from "Hold" to "Run" in R channel)

LP5521 will generate 1100 ms long LED pattern which will be repeated infinitely. LED pattern is illustrated on the figure below.



**R program:**  
 ramp up to PWM value 128 in 200 ms  
 wait 200 ms  
 ramp down to PWM value 0 in 200 ms  
 wait 500 ms

**R program as binary code:**  
 0000001101111111  
 0100110100000000  
 0000001111111111  
 0110000000000000

Sequence diagram

20186224

## Direct PWM Control Example

### Startup device:

- Supply e.g. 3.6V to VDD
- Supply e.g. 1.8V to EN
- Write to address 00H 0100 0000b (enable LP5521)
- Wait 500  $\mu$ s (start-up delay)

### Enable charge pump 1.5x mode and use internal clock:

- Write to address 08H 0001 0001b

### Direct PWM control:

- Write to address 01H 0011 1111b (Configure R, G and B channels into "Direct PWM control mode")

### Write PWM values:

- Write to address 02H 1000 0000b (R driver PWM 50% duty cycle)
- Write to address 03H 1100 0000b (G driver PWM 75% duty cycle)
- Write to address 04H 1111 1111b (B driver PWM 100% duty cycle)

LEDs are turned on after the PWM values are written. Changes to the PWM value registers are reflected immediately to the LED brightness. Default LED current (17.5 mA) is used for LED outputs, if no other values are written.

**See application note "LP5521 Programming Considerations" for more information.**

## LP5521 Control Register Names and Default Values

| ADDR (HEX) | REGISTER   | D7     | D6      | D5            | D4             | D3           | D2          | D1          | D0          | DEFAULT   |
|------------|------------|--------|---------|---------------|----------------|--------------|-------------|-------------|-------------|-----------|
| 00         | ENABLE     | LOG_EN | CHIP_EN | R_EXEC[1:0]   | R_EXEC[1:0]    | G_EXEC[1:0]  | G_EXEC[1:0] | B_EXEC[1:0] | B_EXEC[1:0] | 0000 0000 |
| 01         | OP MODE    |        |         | R_MODE[1:0]   | R_MODE[1:0]    | G_MODE[1:0]  | G_MODE[1:0] | B_MODE[1:0] | B_MODE[1:0] | 0000 0000 |
| 02         | R PWM      |        |         |               | R_PWM[7:0]     |              |             |             |             | 0000 0000 |
| 03         | G PWM      |        |         |               | G_PWM[7:0]     |              |             |             |             | 0000 0000 |
| 04         | B PWM      |        |         |               | B_PWM[7:0]     |              |             |             |             | 0000 0000 |
| 05         | R CURRENT  |        |         |               | R_CURRENT[7:0] |              |             |             |             | 1010 1111 |
| 06         | G CURRENT  |        |         |               | G_CURRENT[7:0] |              |             |             |             | 1010 1111 |
| 07         | B CURRENT  |        |         |               | B_CURRENT[7:0] |              |             |             |             | 1010 1111 |
| 08         | CONFIG     |        | PWM_HF  | PWRSV_SAVE_EN |                | CP_MODE[1:0] | R_TO_BATT   | CLK_DET_EN  | INT_CLK_EN  | 0000 0000 |
| 09         | R PC       |        |         |               |                |              | R_PC[3:0]   |             |             | 0000 0000 |
| 0A         | G PC       |        |         |               |                |              | G_PC[3:0]   |             |             | 0000 0000 |
| 0B         | B PC       |        |         |               |                |              | B_PC[3:0]   |             |             | 0000 0000 |
| 0C         | STATUS     |        |         |               |                | EXT_CLK_USED | R_INT       | G_INT       | B_INT       | 0000 0000 |
| 0D         | RESET      |        |         |               |                | RESET[7:0]   |             |             |             | 0000 0000 |
| 0E         | GPO        |        |         |               |                |              | INT_AS_GPO  | GPO         | INT         | 0000 0000 |
| 10         | PROG MEM R |        |         |               | CMD_R1[15:8]   |              |             |             |             | 0000 0000 |
| 11         | PROG MEM R |        |         |               | CMD_R1[7:0]    |              |             |             |             | 0000 0000 |
|            |            |        |         |               | ...            |              |             |             |             |           |
| 2E         | PROG MEM R |        |         |               | CMD_R16[15:8]  |              |             |             |             | 0000 0000 |
| 2F         | PROG MEM R |        |         |               | CMD_R16[7:0]   |              |             |             |             | 0000 0000 |
| 30         | PROG MEM G |        |         |               | CMD_G1[15:8]   |              |             |             |             | 0000 0000 |
| 31         | PROG MEM G |        |         |               | CMD_G1[7:0]    |              |             |             |             | 0000 0000 |
|            |            |        |         |               | ...            |              |             |             |             |           |
| 4E         | PROG MEM G |        |         |               | CMD_G16[15:8]  |              |             |             |             | 0000 0000 |
| 4F         | PROG MEM G |        |         |               | CMD_G16[7:0]   |              |             |             |             | 0000 0000 |
| 50         | PROG MEM B |        |         |               | CMD_B1[15:8]   |              |             |             |             | 0000 0000 |
| 51         | PROG MEM B |        |         |               | CMD_B1[7:0]    |              |             |             |             | 0000 0000 |
|            |            |        |         |               | ...            |              |             |             |             |           |
| 6E         | PROG MEM B |        |         |               | CMD_B16[15:8]  |              |             |             |             | 0000 0000 |
| 6F         | PROG MEM B |        |         |               | CMD_B16[7:0]   |              |             |             |             | 0000 0000 |

## Enable Register (ENABLE)

Address 00H

Reset value 00H

Enable Register

| 7      | 6       | 5         | 4         | 3         | 2         | 1         | 0         |
|--------|---------|-----------|-----------|-----------|-----------|-----------|-----------|
| LOG_EN | CHIP_EN | R_EXEC[1] | R_EXEC[0] | G_EXEC[1] | G_EXEC[0] | B_EXEC[1] | B_EXEC[0] |

| Name    | Bit | Access | Active | Description   |
|---------|-----|--------|--------|---|
| LOG_EN  | 7   | R/W    | High   | Logarithmic PWM adjustment generation enable  |
| CHIP_EN | 6   | R/W    | High   | Master chip enable. Enables device internal start-up sequence. See Modes of Operation for further information. Setting EN pin low resets the CHIP_EN state to 0.  |
| R_EXEC  | 5:4 | R/W    |        | R channel program execution.<br><b>00b</b> = Hold: Wait until current command is finished then stop while EXEC mode is hold. PC can be read or written only in this mode.<br><b>01b</b> = Step: Execute instruction defined by current R channel PC value, increment PC and change R_EXEC to 00b (Hold)<br><b>10b</b> = Run: Start at program counter value defined by current R Channel PC value<br><b>11b</b> = Execute instruction defined by current R channel PC value and change R_EXEC to 00b (Hold) |
| G_EXEC  | 3:2 | R/W    |        | G channel program execution<br><b>00b</b> = Hold: Wait until current command is finished then stop while EXEC mode is hold. PC can be read or written only in this mode.<br><b>01b</b> = Step: Execute instruction defined by current G channel PC value, increment PC and change G_EXEC to 00b (Hold)<br><b>10b</b> = Run: Start at program counter value defined by current G Channel PC value<br><b>11b</b> = Execute instruction defined by current G channel PC value and change G_EXEC to 00b (Hold)  |
| B_EXEC  | 1:0 | R/W    |        | B channel program execution<br><b>00b</b> = Hold: Wait until current command is finished then stop while EXEC mode is hold. PC can be read or written only in this mode.<br><b>01b</b> = Step: Execute instruction defined by current B channel PC value, increment PC and change B_EXEC to 00b (Hold)<br><b>10b</b> = Run: Start at program counter value defined by current B Channel PC value<br><b>11b</b> = Execute instruction defined by current B channel PC value and change B_EXEC to 00b (Hold)  |

EXEC registers are synchronized to 32 kHz clock. Delay between consecutive I<sup>2</sup>C writes to ENABLE register (00H) need to be longer than 488  $\mu$ s (typ).

## Operation Mode Register (OP MODE)

Address 01H

Reset value 00H

OP Mode Register

|   |   |           |           |           |           |           |           |
|---|---|-----------|-----------|-----------|-----------|-----------|-----------|
| 7 | 6 | 5         | 4         | 3         | 2         | 1         | 0         |
|   |   | R_MODE[1] | R_MODE[0] | G_MODE[1] | G_MODE[0] | B_MODE[1] | B_MODE[0] |

| Name   | Bit | Access | Active | Description   |
|--------|-----|--------|--------|---|
| R_MODE | 5:4 | R/W    |        | R channel operation mode<br>00b = Disabled<br>01b = Load program to SRAM, reset R channel PC<br>10b = Run program defined by R_EXEC<br>11b = Direct control |
| G_MODE | 3:2 | R/W    |        | G channel operation mode<br>00b = Disabled<br>01b = Load program to SRAM, reset G channel PC<br>10b = Run program defined by G_EXEC<br>11b = Direct control |
| B_MODE | 1:0 | R/W    |        | B channel operation mode<br>00b = Disabled<br>01b = Load program to SRAM, reset B channel PC<br>10b = Run program defined by B_EXEC<br>11b = Direct control |

MODE registers are synchronized to 32 kHz clock. Delay between consecutive I<sup>2</sup>C writes to OP\_MODE register (01H) need to be longer than 153  $\mu$ s (typ).

## R channel PWM control (R\_PWM)

Address 02H

Reset value 00H

R PWM Register

|            |   |   |   |   |   |   |   |
|------------|---|---|---|---|---|---|---|
| 7          | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R_PWM[7:0] |   |   |   |   |   |   |   |

| Name  | Bit | Access | Active | Description  |
|-------|-----|--------|--------|--|
| R_PWM | 7:0 | R/W    |        | R Channel PWM value during direct control operation mode |

## G Channel PWM Control (G\_PWM)

Address 03H

Reset value 00H

G PWM Register

|            |   |   |   |   |   |   |   |
|------------|---|---|---|---|---|---|---|
| 7          | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| G_PWM[7:0] |   |   |   |   |   |   |   |

| Name  | Bit | Access | Active | Description  |
|-------|-----|--------|--------|--|
| G_PWM | 7:0 | R/W    |        | G Channel PWM value during direct control operation mode |

## B Channel PWM Control (B\_PWM)

Address 04H

Reset value 00H

B PWM Register

|            |   |   |   |   |   |   |   |
|------------|---|---|---|---|---|---|---|
| 7          | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| B_PWM[7:0] |   |   |   |   |   |   |   |

| Name  | Bit | Access | Active | Description  |
|-------|-----|--------|--------|--|
| B_PWM | 7:0 | R/W    |        | B Channel PWM value during direct control operation mode |

## R Channel Current (R\_CURRENT)

Address 05H

Reset Value AFH

R CURRENT Register

|                |   |   |   |   |   |   |   |
|----------------|---|---|---|---|---|---|---|
| 7              | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R_CURRENT[7:0] |   |   |   |   |   |   |   |

| Name      | Bit | Access | Active | Description   |
|-----------|-----|--------|--------|---|
| R_CURRENT | 7:0 | R/W    |        | Current setting<br>0000 0000b = 0.0 mA<br>0000 0001b = 0.1 mA<br>0000 0010b = 0.2 mA<br>0000 0011b = 0.3 mA<br>0000 0100b = 0.4 mA<br>0000 0101b = 0.5 mA<br>0000 0110b = 0.6 mA<br>...<br><b>1010 1111b = 17.5 mA (default)</b><br>...<br>1111 1011b = 25.1 mA<br>1111 1100b = 25.2 mA<br>1111 1101b = 25.3 mA<br>1111 1110b = 25.4 mA<br>1111 1111b = 25.5 mA |

## G Channel Current (G\_CURRENT)

Address 06H

Reset Value AFH

**G CURRENT Register**

|                |   |   |   |   |   |   |   |
|----------------|---|---|---|---|---|---|---|
| 7              | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| G_CURRENT[7:0] |   |   |   |   |   |   |   |

| Name      | Bit | Access | Active | Description   |
|-----------|-----|--------|--------|---|
| G_CURRENT | 7:0 | R/W    |        | Current setting<br>0000 0000b = 0.0 mA<br>0000 0001b = 0.1 mA<br>0000 0010b = 0.2 mA<br>0000 0011b = 0.3 mA<br>0000 0100b = 0.4 mA<br>0000 0101b = 0.5 mA<br>0000 0110b = 0.6 mA<br>...<br><b>1010 1111b = 17.5 mA (default)</b><br>...<br>1111 1011b = 25.1 mA<br>1111 1100b = 25.2 mA<br>1111 1101b = 25.3 mA<br>1111 1110b = 25.4 mA<br>1111 1111b = 25.5 mA |

## B Channel Current (B\_CURRENT)

Address 07H

Reset value AFH

**B CURRENT Register**

|                |   |   |   |   |   |   |   |
|----------------|---|---|---|---|---|---|---|
| 7              | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| B_CURRENT[7:0] |   |   |   |   |   |   |   |

| Name      | Bit | Access | Active | Description   |
|-----------|-----|--------|--------|---|
| B_CURRENT | 7:0 | R/W    |        | Current setting<br>0000 0000b = 0.0 mA<br>0000 0001b = 0.1 mA<br>0000 0010b = 0.2 mA<br>0000 0011b = 0.3 mA<br>0000 0100b = 0.4 mA<br>0000 0101b = 0.5 mA<br>0000 0110b = 0.6 mA<br>...<br><b>1010 1111b = 17.5 mA (default)</b><br>...<br>1111 1011b = 25.1 mA<br>1111 1100b = 25.2 mA<br>1111 1101b = 25.3 mA<br>1111 1110b = 25.4 mA<br>1111 1111b = 25.5 mA |

## Configuration Control (CONFIG)

Address 08H

Reset value 00H

CONFIG Register

| 7 | 6      | 5          | 4            | 3 | 2         | 1          | 0          |
|---|--------|------------|--------------|---|-----------|------------|------------|
|   | PWM_HF | PWRSAVE_EN | CP_MODE[1:0] |   | R_TO_BATT | CLK_DET_EN | INT_CLK_EN |

| Name                      | Bit | Access | Active | Description   |
|---------------------------|-----|--------|--------|---|
| PWM_HF                    | 6   | R/W    | High   | PWM clock<br>0 = 256 Hz PWM clock used (CLK_32K)<br>1 = 558 Hz PWM clock used (internal oscillator)   |
| PWRSAVE_EN                | 5   | R/W    | High   | Power save mode enable  |
| CP_MODE                   | 4:3 | R/W    |        | Charge pump operation mode<br>00b = OFF<br>01b = Forced to bypass mode (1x)<br>10b = Forced to 1.5x mode<br>11b = Automatic mode selection        |
| R_TO_BATT                 | 2   | R/W    | High   | R channel supply connection<br>0 = R output connected to charge pump<br>1 = R output connected to battery   |
| CLK_DET_EN,<br>INT_CLK_EN | 1:0 | R/W    |        | LED Controller clock source<br>00b = External clock source (CLK_32K)<br>01b = Internal clock<br>10b = Automatic selection<br>11b = Internal clock |

## R Channel Program Counter Value (R channel PC)

Address 09H

Reset value 00H

R Channel PC Register

| 7 | 6 | 5 | 4 | 3       | 2       | 1       | 0       |
|---|---|---|---|---------|---------|---------|---------|
|   |   |   |   | R_PC[3] | R_PC[2] | R_PC[1] | R_PC[0] |

| Name | Bit | Access | Active | Description                     |
|------|-----|--------|--------|---------------------------------|
| R_PC | 3:0 | R/W    |        | R channel program counter value |

PC registers are synchronized to 32 kHz clock. Delay between consecutive I<sup>2</sup>C writes to PC registers needs to be longer than 153  $\mu$ s (typ.). PC register can be read or written only when EXEC mode is 'hold'.

## G Channel Program Counter Value (G channel PC)

Address 0AH

Reset value 00H

G Channel PC Register

|   |   |   |   |         |         |         |         |
|---|---|---|---|---------|---------|---------|---------|
| 7 | 6 | 5 | 4 | 3       | 2       | 1       | 0       |
|   |   |   |   | G_PC[3] | G_PC[2] | G_PC[1] | G_PC[0] |

| Name | Bit | Access | Active | Description                     |
|------|-----|--------|--------|---------------------------------|
| G_PC | 3:0 | R/W    |        | G channel program counter value |

PC registers are synchronized to 32 kHz clock. Delay between consecutive I<sup>2</sup>C writes to PC registers needs to be longer than 153  $\mu$ s (typ.). PC register can be read or written only when EXEC mode is 'hold'.

## B Channel Program Counter Value (B channel PC)

Address 0BH

Reset value 00H

B Channel PC Register

|   |   |   |   |         |         |         |         |
|---|---|---|---|---------|---------|---------|---------|
| 7 | 6 | 5 | 4 | 3       | 2       | 1       | 0       |
|   |   |   |   | B_PC[3] | B_PC[2] | B_PC[1] | B_PC[0] |

| Name | Bit | Access | Active | Description                     |
|------|-----|--------|--------|---------------------------------|
| B_PC | 3:0 | R/W    |        | B channel program counter value |

PC registers are synchronized to 32 kHz clock. Delay between consecutive I<sup>2</sup>C writes to PC registers needs to be longer than 153  $\mu$ s (typ.). PC register can be read or written only when EXEC mode is 'hold'.

## STATUS/INTERRUPT Register

Address 0CH

Reset value 00H

STATUS/INTERRUPT Register

|   |   |   |   |                 |       |       |       |
|---|---|---|---|-----------------|-------|-------|-------|
| 7 | 6 | 5 | 4 | 3               | 2     | 1     | 0     |
|   |   |   |   | EXT_CLK<br>USED | R_INT | G_INT | B_INT |

| Name            | Bit | Access | Active | Description  |
|-----------------|-----|--------|--------|--|
| EXT_CLK<br>USED | 3   | R      |        | External clock state<br>0 = Internal 32kHz clock used<br>1 = External 32kHz clock used |
| R_INT           | 2   | R      | High   | Interrupt from R channel   |
| G_INT           | 1   | R      | High   | Interrupt from G channel   |
| B_INT           | 0   | R      | High   | Interrupt from B channel   |

Note: Register INT bits will be cleared when read operation to Status/Interrupt register occurs. INT output pin (active low) will go high after read operation.

## RESET Register

Address 0DH

Reset value 00H

RESET Register

| 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
|-------|-------|-------|-------|-------|-------|-------|-------|
| RESET | RESET | RESET | RESET | RESET | RESET | RESET | RESET |

| Name  | Bit | Access | Active | Description  |
|-------|-----|--------|--------|--|
| RESET | 7:0 | W      |        | Reset all register values when FFH is written. No acknowledge from LP5521 after write. |

## GPO Register

Address 0EH

Reset value 00H

GPO Register

| 7 | 6 | 5 | 4 | 3 | 2          | 1   | 0   |
|---|---|---|---|---|------------|-----|-----|
|   |   |   |   |   | INT_AS_GPO | GPO | INT |

| Name       | Bit | Access | Active | Description   |
|------------|-----|--------|--------|---|
| INT_AS_GPO | 2   | R/W    | High   | Enable INT pin GPO function                               |
| GPO        | 1   | R/W    | High   | GPO pin state:<br>0 = LOW<br>1 = HIGH                     |
| INT        | 0   | R/W    | High   | INT pin state (when INT_AS_GPO=1):<br>0 = LOW<br>1 = HIGH |

## PROGRAM MEMORY

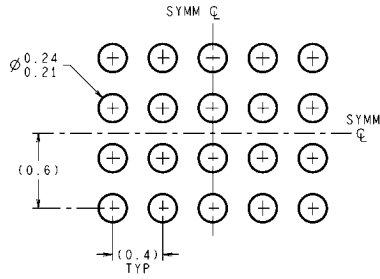
Address 10H – 6FH

Reset values 00H

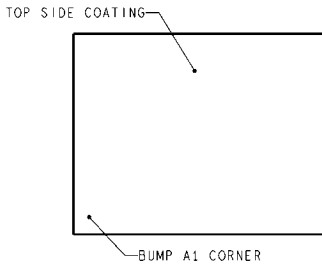
Please see chapter LED Controller Programming Commands for further information.

| Command           | 15 | 14        | 13        | 12                               | 11    | 10 | 9 | 8         | 7                            | 6           | 5 | 4 | 3 | 2 | 1 | 0 |   |
|-------------------|----|-----------|-----------|----------------------------------|-------|----|---|-----------|------------------------------|-------------|---|---|---|---|---|---|---|
| <b>Ramp Wait</b>  | 0  | Pre-scale | Step time |                                  |       |    |   | Sign      | Increment                    |             |   |   |   |   |   |   |   |
| <b>Set PWM</b>    | 0  | 1         | 0         |                                  |       |    |   | PWM Value |                              |             |   |   |   |   |   |   |   |
| <b>Go toStart</b> | 0  | 0         | 0         |                                  |       |    |   | 0         | 0                            | 0           | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| <b>Branch</b>     | 1  | 0         | 1         | Loop Count                       |       |    |   |           | X                            | Step number |   |   |   |   |   |   |   |
| <b>End</b>        | 1  | 1         | 0         | Int                              | Reset | X  |   |           |                              |             |   |   |   |   |   |   |   |
| <b>Trigger</b>    | 1  | 1         | 1         | Wait for trigger on channels 5-0 |       |    |   |           | Send trigger on channels 5-0 |             |   |   |   | X |   |   |   |

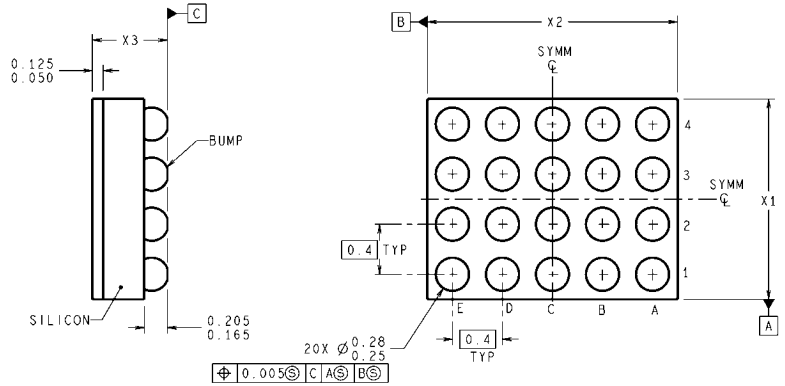
# Physical Dimensions inches (millimeters) unless otherwise noted



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS  
DIMENSIONS IN ( ) FOR REFERENCE ONLY

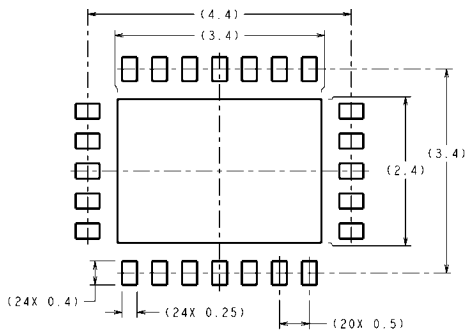


TMD20XXX (Rev D)

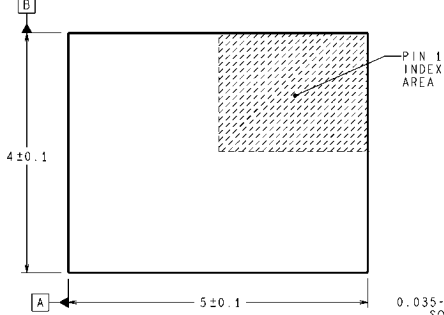
The dimension for X1 ,X2 and X3 are as given:

- X1=1.717 mm ± 0.03 mm
- X2=2.066 mm ± 0.03 mm
- X3=0.600 mm ± 0.075 mm

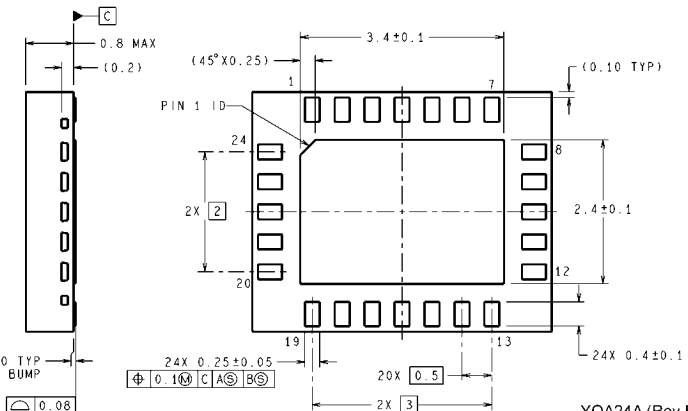
## TMD20ECA: Thin microSMD-20, Small Bump



RECOMMENDED LAND PATTERN  
1:1 RATIO WITH PKG SOLDER PADS



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## YQA24A: Bumped LLP-24

YQA24A (Rev B)

# Notes

**Notes**

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