LMH6401 DC to 4.5 GHz, Fully-Differential, Digital Variable-Gain Amplifier

1 Features

- 3-dB Bandwidth: 4.5 GHz at 26-dB Gain
- Maximum Voltage Gain: 26 dB
- Gain Range: 32 dB with 1-dB Step Control
- Differential Input Impedance: 100 Ω
- Fully-Differential Output
- Distortion at Max Gain (V_O= 2 V_{PP}, R_L= 200 Ω):
  - 200 MHz: HD2 at –73 dBc, HD3 at –80 dBc
  - 500 MHz: HD2 at –68 dBc, HD3 at –72 dBc
  - 1 GHz: HD2 at –63 dBc, HD3 at –63 dBc
  - 2 GHz: HD2 at –58 dBc, HD3 at –54 dBc
- Output IP3:
  - 43 dBm at 200 MHz
  - 33 dBm at 1 GHz
  - 27 dBm at 2 GHz
- Output IP2:
  - 60 dBm at 1 GHz
  - 52 dBm at 2 GHz
- Supply Operation: 5.0 V with 71-mA Current
- Supports Single- and Split-Supply Operation:
  - DC- and AC-Coupled Applications
- Fabricated on Advanced Complementary BiCMOS Process
- 3-mm × 3-mm UQFN-16 Package

2 Applications

- Test and Measurement
- Ultra-Wideband ADC Drivers
- Communications Receivers
- RF Sampling Subsystems
- SAW Filter Buffers and Drivers
- Defense and Radar

3 Description

The LMH6401 is a high-performance, digitally-controlled, variable-gain-amplifier (DVGA) designed for radio frequency (RF) or intermediate frequency (IF) as well as high-speed, time-domain applications. The device is an ideal analog-to-digital converter (ADC) driver for dc- or ac-coupled applications that require an automatic gain control (AGC).

Noise and distortion performance is optimized to drive GSPS ADCs. The amplifier has an 8-dB noise figure at maximum gain and a –63-dBc harmonic distortion at 1 GHz for full-scale signal levels. Single- and split-supply operation is supported for applications requiring a dc-coupled drive to the ADC. A common-mode reference input pin is provided to align the amplifier output common-mode with the ADC input requirements.

Gain control is performed via an SPI™ interface, allowing a 32-dB range with a 1-dB step. A power-down feature is also available through the PD pin.

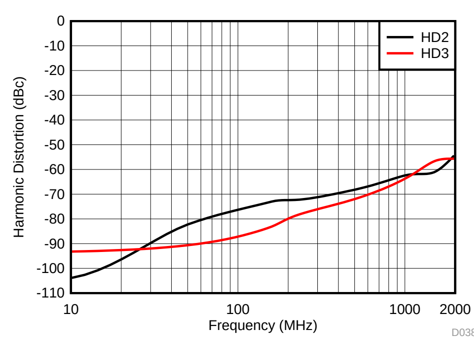
This level of performance is achieved at a low power level of 355 mW. The operating ambient temperature range is –40°C to 85°C.

Device Information(1)

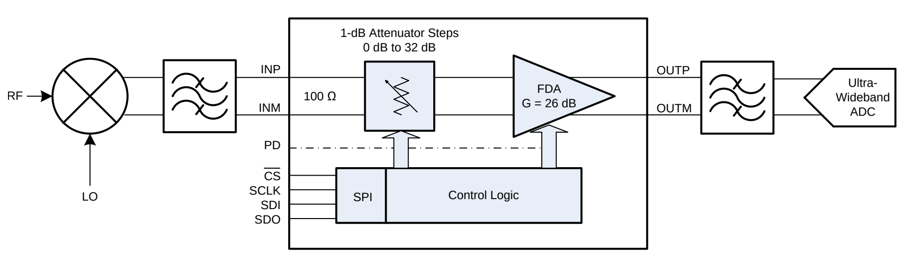
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMH6401	UQFN (16)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Harmonic Distortion versus Frequency



Down-Converted IF Sampling Application



PRODUCT PREVIEW

Table of Contents

4 Revision History

DATE	REVISION	NOTES
April 2015	*	Initial release.

PRODUCT PREVIEW

5 Device Options

Table 1. Device Companion

DEVICE	BW (A_V = 12 dB)	DISTORTION	NOISE
LMH5401	6.2 GHz	–75-dBc HD2, –75-dBc HD3 at 500 MHz	1.25 nV/√Hz
LMH3401	7 GHz, G = 16 dB	–79-dBc HD2, –77-dBc HD3 at 500 MHz	1.4 nV/√Hz
LMH6554	1.6 GHz	–79-dBc HD2, –70-dBc HD3 at 250 MHz	0.9 nV/√Hz

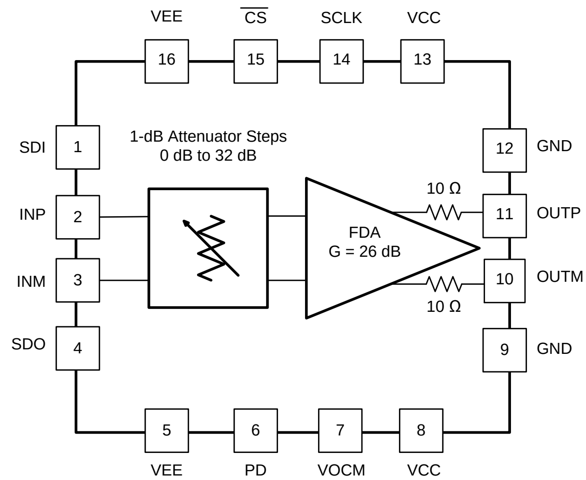
Table 2. Device Comparison

DEVICE	MAX GAIN, BW	DISTORTION	NOISE FIGURE
LMH6517	22 dB, 1.2 GHz	43-dBm OIP3 at 200 MHz, –74-dBc HD3 at 200 MHz	5.5 dB
LMH6881	26 dB, 2.4 GHz	42-dBm OIP3 at 200 MHz, –76-dBc HD3 at 200 MHz	9.7 dB
LMH6882	26 dB, 2.4 GHz	42-dBm OIP3 at 200 MHz, –76-dBc HD3 at 200 MHz	9.7 dB

PRODUCT PREVIEW

6 Pin Configuration and Functions

RMZ Package
UQFN-16
Top View



Pin Functions

PIN		FUNCTION	DESCRIPTION
NO.	NAME		
1	SDI	Input	Serial interface input data
2	INP	Input	Positive input pin
3	INM	Input	Negative input pin
4	SDO	Output	Serial interface output data
5	VEE	Power	Negative supply voltage
6	PD	Input	Power-down pin. 0 = amplifier enabled, 1 = amplifier disabled
7	VOCM	Input	Input pin to set amplifier output common-mode voltage
8	VCC	Power	Positive supply voltage
9	GND	Power	Ground
10	OUTM	Output	Negative output pin
11	OUTP	Output	Positive output pin
12	GND	Power	Ground
13	VCC	Input	Positive supply voltage
14	SCLK	Input	Serial interface clock
15	$\overline{CS}$	Input	Chip select
16	VEE	Power	Negative supply voltage

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage (V = VCC – VEE)		5.5	V
Digital input pins	From –0.5 + VEE to VCC		V
Maximum input differential voltage		1.2	V
Maximum input voltage	From VEE to VCC		V
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±TBD	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±TBD	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Operating temperature range	–40		85	°C
Supply voltage	4.0		5.25	V

7.4 Thermal Information

THERMAL METRIC(1)		RMZ (UQFN)	UNIT
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	77.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	24.0	
ψ_{JT}	Junction-to-top characterization parameter	2.3	
ψ_{JB}	Junction-to-board characterization parameter	24.0	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

PRODUCT PREVIEW

PRODUCT PREVIEW

7.5 Electrical Characteristics

At T_A = 25°C, V_{EE} = –2.5 V, V_{CC} = 2.5 V, VOCM = 0 V, R_{LOAD} = 200-Ω differential ($R_{s(internal,\ diff)}$ = 20 Ω), $V_{OUT(PP)D}$ = 2 V, and A_V = 26 dB, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
GAIN PARAMETERS							
MVG	Maximum voltage gain			26.0		dB	C
	Gain accuracy	At all gain steps		±0.5		dB	C
GR	Gain range			32.0		dB	C
GS	Gain step			1.0		dB	C
DYNAMIC PERFORMANCE							
SSBW	Small-signal, –3-dB bandwidth	A_V = 26 dB, V_O = 200 mV_{PPD}		4.5		GHz	C
LSBW	Large-signal, –3-dB bandwidth	A_V = 26 dB, V_O = 2.0 V_{PPD}		4.5		GHz	C
SR	Slew rate			TBD		V/µs	C
t_s	Settling time to 1%	V_O = 2-V step		TBD		ns	C
HD2	Second-order harmonic distortion	f = 200 MHz, V_O = 2.0 V_{PPD}		–73		dBc	C
		f = 500 MHz, V_O = 2.0 V_{PPD}		–68		dBc	C
		f = 1 GHz, V_O = 2.0 V_{PPD}		–63		dBc	C
		f = 2 GHz, V_O = 2.0 V_{PPD}		–58		dBc	C
HD3	Third-order harmonic distortion	f = 200 MHz, V_O = 2.0 V_{PPD}		–80		dBc	C
		f = 500 MHz, V_O = 2.0 V_{PPD}		–72		dBc	C
		f = 1 GHz, V_O = 2.0 V_{PPD}		–63		dBc	C
		f = 2 GHz, V_O = 2.0 V_{PPD}		–54		dBc	C
OIP2	Output second-order intercept point	f = 200 MHz, P_O = –2 dBm per tone		67		dBm	C
		f = 500 MHz, P_O = –2 dBm per tone		65		dBm	C
		f = 1 GHz, P_O = –2 dBm per tone		60		dBm	C
		f = 2 GHz, P_O = –2 dBm per tone		52		dBm	C
OIP3	Output third-order intercept point	f = 200 MHz, P_O = –2 dBm per tone		43		dBm	C
		f = 500 MHz, P_O = –2 dBm per tone		40		dBm	C
		f = 1 GHz, P_O = –2 dBm per tone		33		dBm	C
		f = 2 GHz, P_O = –2 dBm per tone		27		dBm	C
P1dB	1-dB compression point	f = 500 MHz, power measured at amplifier output		TBD		dBm	C
NF	Noise figure	50-Ω, single-ended source, f = 200 MHz		7.7		dB	C
		50-Ω, single-ended source, f = 1 GHz		8		dB	C
S12	Reverse transmission (S12)			–70		dB	C
S11	Input return loss (S11)	100-Ω system, f = 2 GHz		–15		dB	C
ANALOG INPUT, OUTPUT CHARACTERISTICS							
V_{ILR}	Low-level input voltage range			V_{EE} + 1.5		V	C
V_{IHR}	High-level input voltage range			V_{CC} – 1.5		V	C
V_{OLR}	Low-level output voltage range			V_{CC} + 1	V_{CC} + 1.2	V	C
V_{OHR}	High-level output voltage range		V_{CC} – 1.2	V_{CC} – 1		V	C
V_{OM}	Maximum output voltage swing	Differential		6.0		V_{PPD}	C
	Maximum output voltage	Each output		TBD		V	C
	Minimum output voltage	Each output		TBD		V	C
CMRR	Common-mode rejection ratio			TBD		dB	C
r_i	Input resistance	Differential		100		Ω	A
r_o	Output resistance	Differential		20		Ω	A
POWER SUPPLY							
I_Q	Quiescent current	PD = 0		71		mA	A
	Supply voltage		4		5.25	V	A

(1) Test levels: (A) 100% tested at 25°C. Overtemperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

Electrical Characteristics (continued)

At T_A = 25°C, V_{EE} = –2.5 V, V_{CC} = 2.5 V, VOCM = 0 V, R_{LOAD} = 200-Ω differential ($R_{s(internal,\ diff)}$ = 20 Ω), $V_{OUT(PP)D}$ = 2 V, and A_V = 26 dB, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
POWER DOWN							
	Power-down quiescent current		TBD		TBD	mA	A
	PD bias current	PD = 2.5 V		10	±100	µA	C
	Turn-on time delay	Time to V_O = 90% of final value		70		ns	C
	Turn-off time delay	Time to V_O = 10% of original value		10		ns	C
DIGITAL INPUT/OUTPUT							
V_{IH}	High-level input voltage	Referred to GND	1.2		VCC	V	A
V_{IL}	Low-level input voltage	Referred to GND	–0.3		0.8	V	A
V_{OH}	High-level output voltage	I_{OH} = 100 µA (source)	1.8			V	A
		I_{OH} = 2 mA (source)	1.55			V	A
V_{OL}	Low-level output voltage	I_{OL} = 100 µA (sink)			0.2	V	A
		I_{OL} = 2 mA (sink)			0.45	V	A

7.6 SPI Timing Requirements(1)

		MIN	NOM	MAX	UNIT
f_{s_c}	SCLK frequency			50	MHz
t_{PH}	SCLK pulse duration, high	10			ns
t_{PL}	SCLK pulse duration, low	10			ns
t_{SU}	SDI setup	3			ns
t_H	SDO hold	3			ns
t_{IZ}	SDO tri-state			3	ns
t_{ODZ}	SDO driven to tri-state(2)			5	ns
t_{OZD}	SDO tri-state to driven			3	ns
t_{OD}	SDO output delay(2)			3	ns
t_{CSS}	$\overline{CS}$ setup(3)	3			ns
t_{CSH}	$\overline{CS}$ hold	3			ns
t_{IAG}	Inter-access gap	20			ns

(1) Ensured by design.
(2) Reference to negative edge of SCLK.
(3) Reference to positive edge of SCLK.

PRODUCT PREVIEW

PRODUCT PREVIEW

8 Detailed Description

8.1 Register Maps

Table 3 lists the SPI register map.

Table 3. SPI Register Map

ADDRESS (A[6:0])	R/W	REGISTER	DEFAULT (Hex)
0	R	Revision ID	03h
1	R	Product ID	00h
2	R/W	Gain Control	20h (minimum gain)
3	R/W	Reserved	8Ch
4	R/W	Thermal feedback gain control	27h
5	R/W	Thermal feedback frequency control	45h
6-127	R	Reserved	00h

8.1.1 Revision ID (address = 0h, Read-Only) [default = 03h]

Figure 1. Revision ID

7	6	5	4	3	2	1	0
Revision ID							
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-1b	R-1b

LEGEND: R = Read only; -n = value after reset

Table 4. Revision ID Field Descriptions

Bit	Field	Type	Default	Description
7-0	Revision ID	R	00000011	Revision identification bits.

8.1.2 Product ID (address = 1h, Read-Only) [default = 00h]

Figure 2. Product ID

7	6	5	4	3	2	1	0
Product ID							
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

LEGEND: R = Read only; -n = value after reset

Table 5. Product ID Field Descriptions

Bit	Field	Type	Default	Description
7-0	Product ID	R	00000000	Product identification bits.

8.1.3 Gain Control (address = 2h) [default = 20h]

Figure 3. Gain Control

7	6	5	4	3	2	1	0
Reserved	Power Down	Gain Control					
R/W-0b	R/W-0b	R/W-1b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6. Gain Control Field Description

Bit	Field	Type	Default	Description
7	Reserved	R/W	0	Reserved, always program to 0
6	Power Down	R/W	0	0 = Active 1 = Power down
5-0	Gain Control	R/W	100000	Gain control (see Table 10 for gain settings)

8.1.4 Reserved (address = 3h) [default = 8Ch]

Figure 4. Reserved

7	6	5	4	3	2	1	0
Reserved							
R/W-1b	R/W-0b	R/W-0b	R/W-0b	R/W-1b	R/W-1b	R/W-0b	R/W-0b

LEGEND: R/W = Read/Write; -n = value after reset

Table 7. Reserved Field Descriptions

Bit	Field	Type	Default	Description
7-0	Reserved	R/W	10001100	Reserved

8.1.5 Thermal Feedback Gain Control (address = 4h) [default = 27h]

Figure 5. Thermal Feedback Gain Control

7	6	5	4	3	2	1	0
Reserved	Reserved	Thermal SD	Thermal Feedback Gain Control				
R/W-0b	R/W-0b	R/W-1b	R/W-0b	R/W-0b	R/W-1b	R/W-1b	R/W-1b

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 8. Thermal Feedback Gain Control Field Descriptions

Bit	Field	Type	Default	Description
7-6	Reserved	R/W	00	Reserved, always program to 00
5	Thermal SD	R/W	1	0 = Thermal feedback control enabled 1 = Thermal feedback control disabled
4-0	Thermal feedback gain control	R/W	00111	TBD

PRODUCT PREVIEW

8.1.6 Thermal Feedback Frequency Control (address = 5h) [default = 45h]

Figure 6. Thermal Feedback Frequency Control

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Thermal Feedback Frequency Control				
R/W-0b	R/W-1b	R/W-0b	R/W-0b	R/W-0b	R/W-1b	R/W-0b	R/W-1b

LEGEND: R/W = Read/Write; -n = value after reset

Table 9. Thermal Feedback Frequency Control Field Descriptions

Bit	Field	Type	Default	Description
7-5	Reserved	R/W	010	Reserved, always program to 010
4-0	Thermal feedback frequency control	R/W	00101	TBD

Table 10. Gain Control Register Controls

ATTENUATION (dB)	GAIN (dB)	REGISTER SETTING (Address = 02h)
0	26	00h
1	25	01h
2	24	02h
3	23	03h
4	22	04h
5	21	05h
6	20	06h
7	19	07h
8	18	08h
9	17	09h
10	16	0Ah
11	15	0Bh
12	14	0Ch
13	13	0Dh
14	12	0Eh
15	11	0Fh
16	10	10h
17	9	11h
18	8	12h
19	7	13h
20	6	14h
21	5	15h
22	4	16h
23	3	17h
24	2	18h
25	1	19h
26	0	1Ah
27	–1	1Bh
28	–2	1Ch
29	–3	1Dh
30	–4	1Eh
31	–5	1Fh
32	–6	20h-3Fh

PRODUCT PREVIEW

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- ADS12D1800RF Data Sheet, SNAS518
- ADC12J1600, ADC12J2700 Data Sheet, SLAS969
- ADC12J4000 Data Sheet, SLAS989
- ADS54J60 Data Sheet, SBAS706
- ADS5424 Data Sheet, SLWS157
- ADS5485 Data Sheet, SLAS610
- ADS4149 Data Sheet, SBAS483
- ADS6149 Data Sheet, SLWS211
- LMH3401 Data Sheet, SBOS695
- LMH5401 Data Sheet, SBOS710
- LMH6517 Data Sheet, SNOSB19
- *AN-2188 Between the Amplifier and the ADC: Managing Filter Loss in Communications Systems*, SNOA567
- *AN-2235 Circuit Board Design for LMH6517/21/22 and Other High-Speed IF/RF Feedback Amplifiers*, SNOA869
- *LMH6401EVM Evaluation Module*, SLOU406

9.2 Trademarks

SPI is a trademark of Motorola.
All other trademarks are the property of their respective owners.

9.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6401IRMZR	PREVIEW	UQFN	RMZ	16	3000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	MH6401	
LMH6401IRMZT	PREVIEW	UQFN	RMZ	16	250	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	MH6401	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

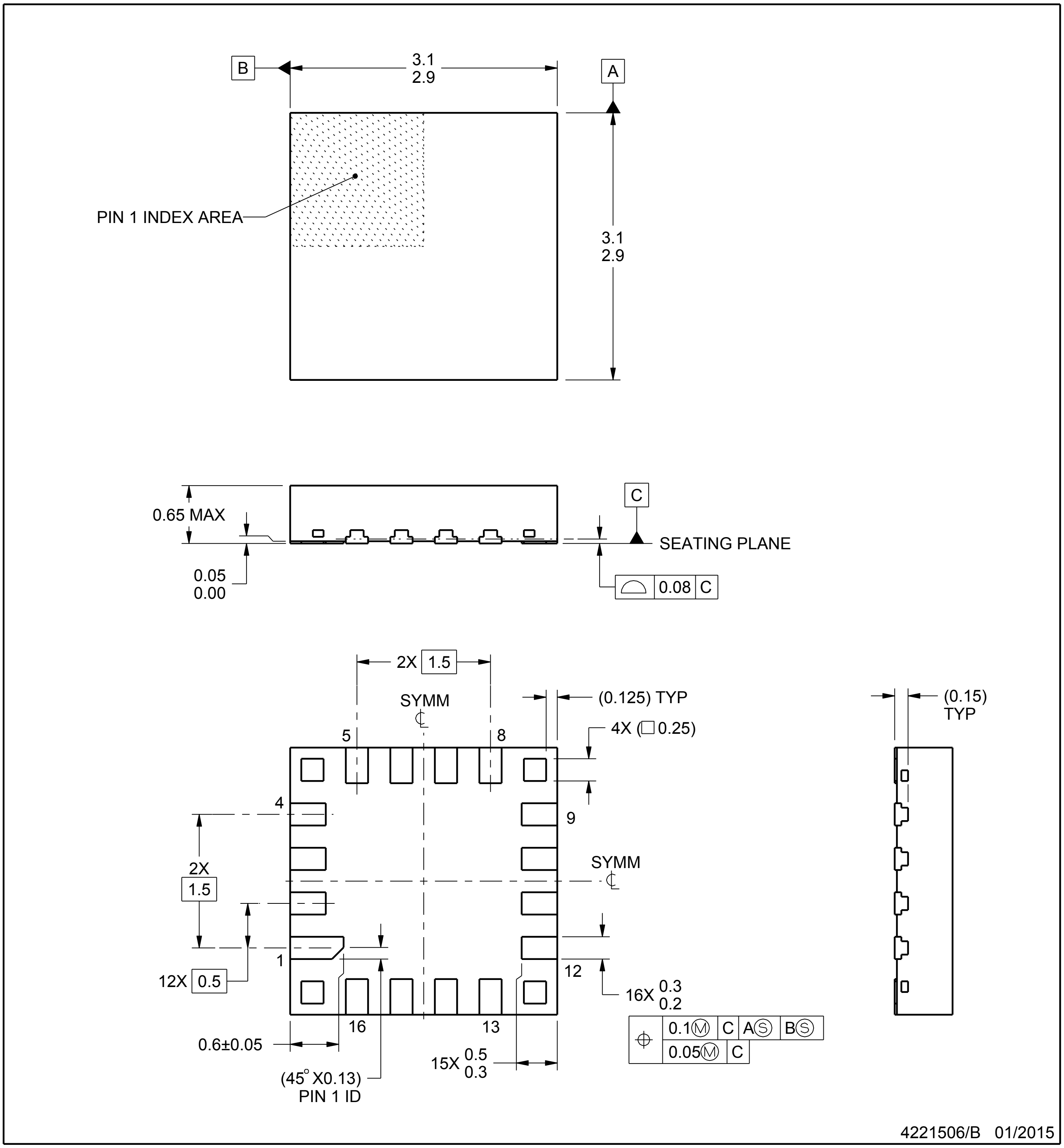
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

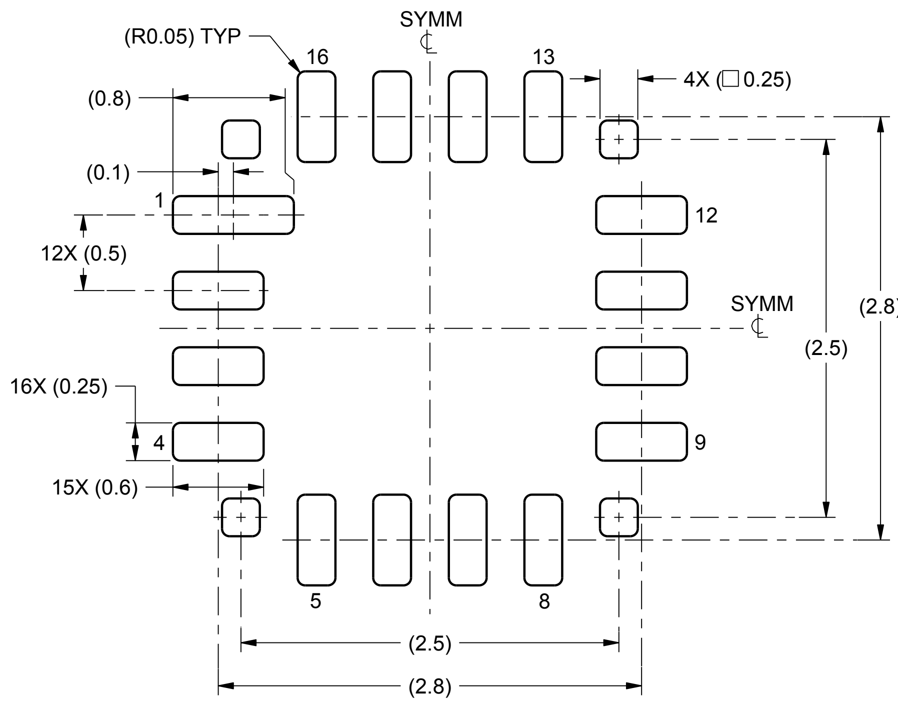
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

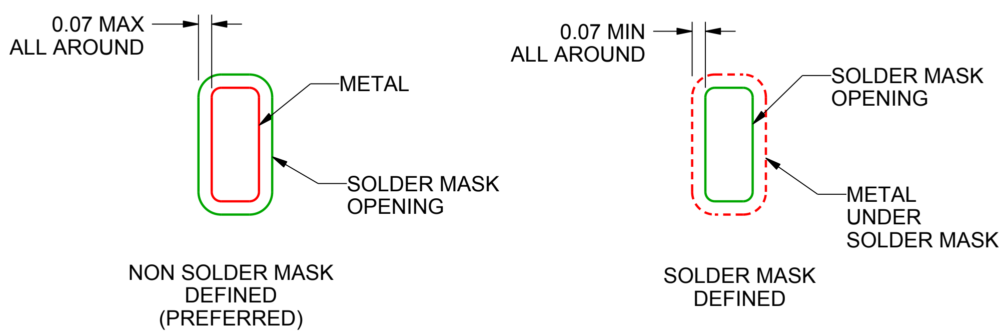


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



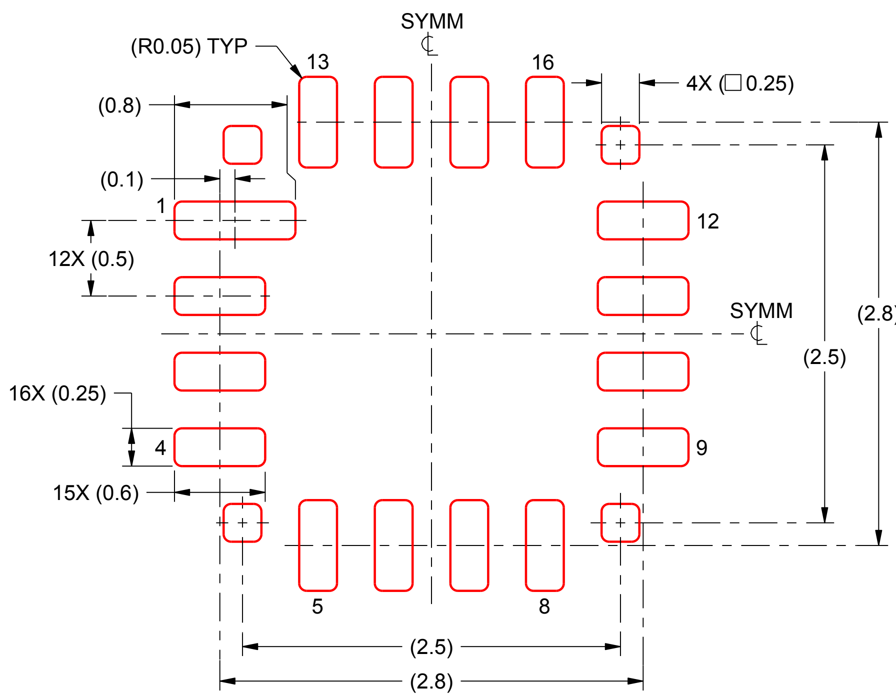
LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS
NOT TO SCALE

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICKNESS
SCALE:20X

4221506/B 01/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE

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