LDC1000 Inductance-to-Digital Converter

1 Features

- Magnet-Free Operation
- Sub-Micron Precision
- Adjustable Sensing Range (Through Coil Design)
- Lower System Cost
- Remote Sensor Placement (Decoupling the LDC From Harsh Environments)
- High Durability (by Virtue of Contact-Less Operation)
- Insensitivity to Environmental Interference (Such as Dirt, Dust, Water, Oil)
- Supply Voltage, Analog: 4.75 V to 5.25 V
- Supply Voltage, I/O: 1.8 V to 5.25 V
- Supply Current (Without LC Tank): 1.7 mA
- Rp Resolution: 16-Bit
- L Resolution: 24-Bit
- LC Frequency Range: 5 kHz to 5 MHz

2 Applications

- Drive-by-Wire Systems
- Gear-Tooth Counting
- Flow Meters
- Push-Button Switches
- Notebook Computers
- Game Controllers
- Multi-Function Printers
- Digital Cameras
- Medical Devices

3 Description

Inductive Sensing is a contact-less, short-range sensing technology that enables low-cost, high-resolution sensing of conductive targets in the presence of dust, dirt, oil, and moisture, making it extremely reliable in hostile environments. Using a coil which can be created on a PCB as a sensing element, the LDC1000 enables ultra-low cost system solutions.

Inductive sensing technology enables precise measurement of linear and angular position, displacement, motion, compression, vibration, metal composition, and serval other applications in markets including automotive, consumer, computer, industrial, medical, and communications. Inductive sensing offers better performance and reliability at lower cost than other competitive solutions.

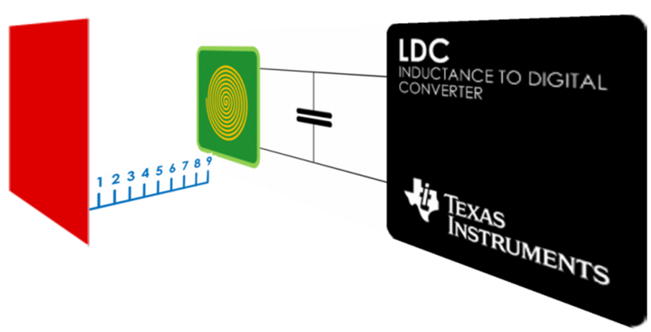
The LDC1000 is the world's first inductance-to-digital converter, offering the benefits of inductive sensing in a low-power, small-footprint solution. The product is available in a SON-16 package and offers several modes of operation. A serial peripheral interface (SPI) simplifies connection to an MCU.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LDC1000	WSON (16)	5.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Axial Distance Sensing Application



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4 Revision History

Changes from Revision A (December 2013) to Revision B — **Page**

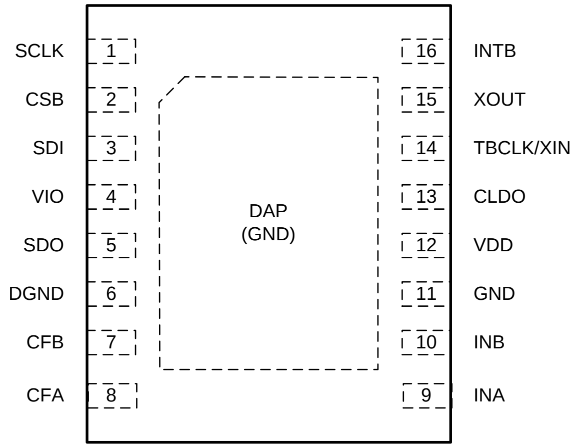
- Added *ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device* and *Documentation Support section,* and *Mechanical, Packaging, and Orderable Information section* 1
- Changed SCLK Pin type from DO to DI 3
- Added L Res value to *Electrical Characteristics* 5
- Added *Measuring Inductance With LDC1000* subsection to *Feature Description* 11
- Changed Frequency Counter Data values in Register Description table 16

Changes from Original (September 2013) to Revision A — **Page**

- Changed SCLK to CSB 6

5 Pin Configuration and Functions

NHR Package
16-Pin WSON
Top View



Pin Functions

PIN		TYPE (1)	DESCRIPTION
NAME	NO.		
SCLK	1	DI	SPI clock input. SCLK is used to clock-out/clock-in the data from/into the chip
CSB	2	DI	SPI CSB. Multiple devices can be connected on the same SPI bus and CSB can be used to select the device to be communicated with
SDI	3	DI	SPI Slave Data In (Master Out Slave In). This should be connected to the Master Out Slave In of the master
VIO	4	P	Digital IO Supply
DGND	6	P	Digital ground
SDO	5	DO	SPI Slave Data Out (Master In Slave Out).It is Hi-z when CSB is high
CFB	7	A	LDC filter capacitor
CFA	8	A	LDC filter capacitor
INA	9	A	External LC Tank. Connected to external LC tank
INB	10	A	External LC Tank. Connected to external LC tank
GND	11	P	Analog ground
VDD	12	P	Analog supply
CLDO	13	A	LDO bypass capacitor. A 56-nF capacitor should be connected from this pin to GND
TBCLK/XIN	14	DI/A	External time-base clock/XTAL. Either an external clock or crystal can be connected
XOUT	15	A	XTAL. Crystal out. Recommended to connect 8-Mhz crystal between XIN and XOUT with 20-pF cap from each pin-to-ground. Should be floating when external clock is used
INTB	16	DO	Configurable interrupt. This pin can be configured to behave in 3 different ways by programing the INT pin mode register. Either threshold detect, wake-up, or DRDYB
DAP	17	P	Connect to GND

(1) DO: Digital Output, DI: Digital Input, P: Power, A: Analog

6 Specifications

6.1 Absolute Maximum Ratings[1]

	MIN	MAX	UNIT
Analog Supply Voltage (VDD – GND)		6	V
IO Supply Voltage (VIO – GND)		6	V
Voltage on any Analog Pin	–0.3	VDD + 0.3	V
Voltage on any Digital Pin	–0.3	VIO + 0.3	V
Input Current on INA and INB		8	mA
Junction Temperature, T_J[2]		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{θJA}$, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is $P_{DMAX} = (T_{J(MAX)} - T_A)/ R_{θJA}$. All numbers apply for packages soldered directly onto a PC board. The package thermal impedance is calculated in accordance with JESD 51-7.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Condition[1]

	MIN	MAX	UNIT
Analog Supply Voltage (VDD – GND)	4.75	5.25	V
IO Supply Voltage (VIO – GND)	1.8	5.25	V
VDD-VIO	≥0		V
Operating Temperature, T_A	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.4 Thermal Information

THERMAL METRIC[1]		LDC1000	UNIT
		NHR (WSON)	
		16-PINS	
$R_{θJA}$	Junction-to-ambient thermal resistance[2]	28	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{θJA}$, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is $P_{DMAX} = (T_{J(MAX)} - T_A)/ R_{θJA}$. All numbers apply for packages soldered directly onto a PC board. The package thermal impedance is calculated in accordance with JESD 51-7.

6.5 Electrical Characteristics

Unless otherwise specified, all limits ensured for TA = TJ = 25°C, VDD = 5.0 V, VIO = 3.3 V[(1)(2)]

PARAMETER		TEST CONDITIONS	MIN[(3)]	TYP[(4)]	MAX[(3)]	UNIT
POWER						
V_{DD}	Analog Supply Voltage		4.75	5	5.25	V
V_{IO}	IO Supply Voltage	VIO≤VDD	1.8	3.3	5.25	V
I_{DD}	Supply Current, VDD	Does not include LC tank current		1.7	2.3	mA
I_{VIO}	IO Supply Current	Static current			14	uA
I_{DD_LP}	Low-Power Mode Supply Current	With out LC Tank		250		uA
t_{START}	Start-Up Time	From POR to ready-to-convert. Crystal not used for frequency counter		2		ms
LDC						
f_{sensor_MIN}	Minimum sensor frequency			5		kHz
f_{sensor_MAX}	Maximum sensor frequency			5		MHz
A_{sensor_MIN}	Minimum sensor amplitude			1		VPP
A_{sensor_MAX}	Maximum sensor amplitude			4		VPP
t_{REC}	Recovery time	Oscillation start-up time after RP under-range condition		10		$1/f_{sensor}$
R_{p_MIN}	Minimum Sensor Rp Range			798		Ω
R_{p_MAX}	Maximum Sensor Rp Range			3.93		MΩ
R_{p_RES}	Rp Measurement Resolution			16		Bits
L Res	Inductance measurement resolution			24		Bits
t_{S_MIN}	Minimum Response Time	Minimum programmable settling time of digital filter		$192 \times 1/f_{sensor}$		s
t_{S_MAX}	Maximum Response Time	Maximum programmable settling time of digital filter		$6144 \times 1/f_{sensor}$		s
EXTERNAL CLOCK/CRYSTAL FOR FREQUENCY COUNTER						
Crystal	Frequency			8		MHz
	Startup time			30		ms
External Clock	Frequency				8	MHz
	Clock Input High Voltage				V_{IO}	V
DIGITAL I/O CHARACTERISTICS						
V_{IH}	Logic 1 Input Voltage		$0.8 \times V_{IO}$			V
V_{IL}	Logic 0 Input Voltage				$0.2 \times V_{IO}$	V
V_{OH}	Logic 1 Output Voltage	ISOURCE=400 uA		$V_{IO}-0.3$		V
V_{OL}	Logic 0 Output Voltage	ISINK=400 uA			0.3	V
I_{IOHL}	Digital IO Leakage Current		–500		500	nA

(1) *Electrical Characteristics* table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. *Absolute Maximum Ratings* indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is $P_{DMAX} = (T_{J(MAX)} - T_A)/ R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC board. The package thermal impedance is calculated in accordance with JESD 51-7.
(3) Limits are specified by testing, design, or statistical analysis at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
(4) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.

6.6 Timing Requirements

Unless otherwise noted, all limits specified at TA = 25°C, VDD=5.0, VIO=3.3, 10 pF capacitive load in parallel with a 10 kΩ load on SDO. Specified by design; not production tested.

			MIN	TYP	MAX	UNIT
f_{SCLK}	Serial Clock Frequency				4	MHz
t_{PH}	SCLK Pulse Width High	f_{SCLK} = 4 MHz	0.4 / f_{SCLK}			s
t_{PL}	SCLK Pulse Width Low	f_{SCLK} = 4 MHz	0.4 / f_{SCLK}			s
t_{SU}	SDI Setup Time		10			ns
t_{H}	SDI Hold Time		10			ns
t_{ODZ}	SDO Driven-to-Tristate Time	Measured at 10% / 90% point			20	ns
t_{OZD}	SDO Tristate-to-Driven Time	Measured at 10% / 90% point			20	ns
t_{OD}	SDO Output Delay Time				20	ns
t_{CSS}	CSB Setup Time		20			ns
t_{CSH}	CSB Hold Time		20			ns
t_{IAG}	Inter-Access Gap		100			ns
t_{DRDYB}	Data ready pulse width	Data ready pulse at every 1 / ODR if no data is read		1 / f_{sensor}		s

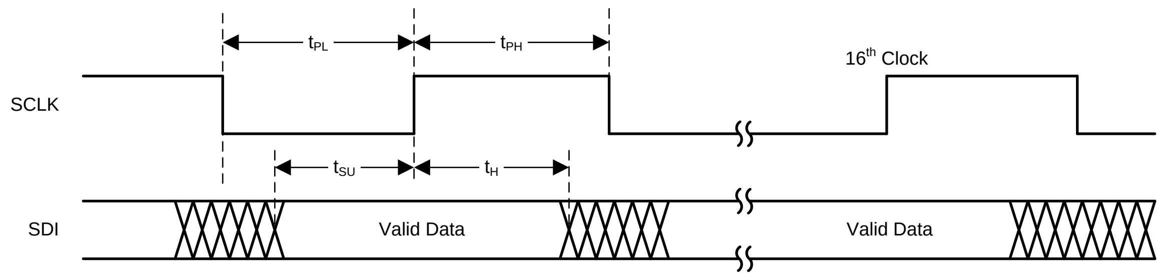


Figure 1. Write Timing Diagram

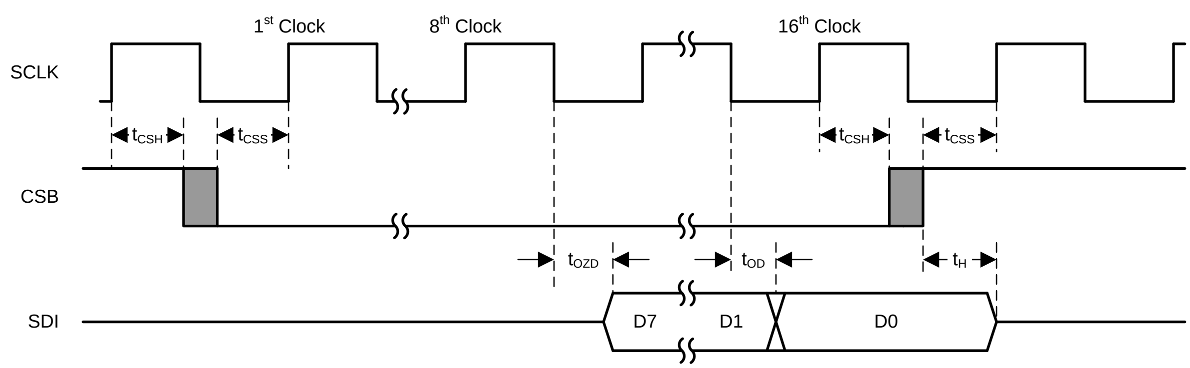
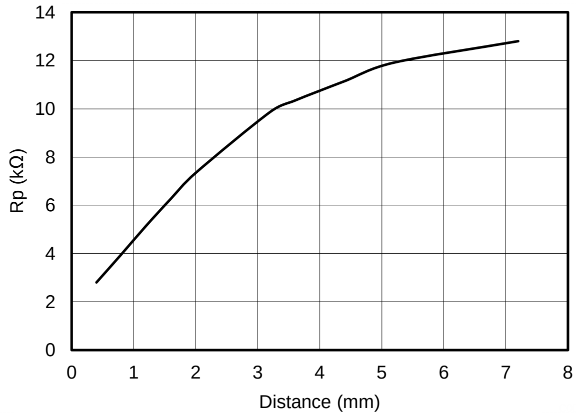


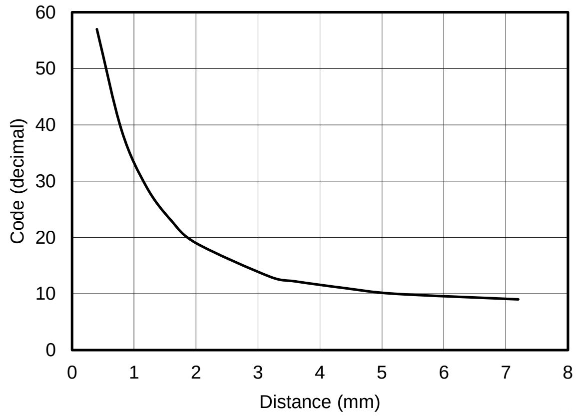
Figure 2. Read Timing Diagram

6.7 Typical Characteristics



Sensor Details:	Table 20	Rp_MIN:	1.347 kΩ
Target Material:	Stainless Steel	Rp_MAX:	38.785 kΩ

Figure 3. Rp vs Distance



Sensor Details:	Table 20	Rp_MIN:	1.347 kΩ
Target Material:	Stainless Steel	Rp_MAX:	38.785 kΩ

Figure 4. Proximity Data vs Distance

7 Detailed Description

7.1 Overview

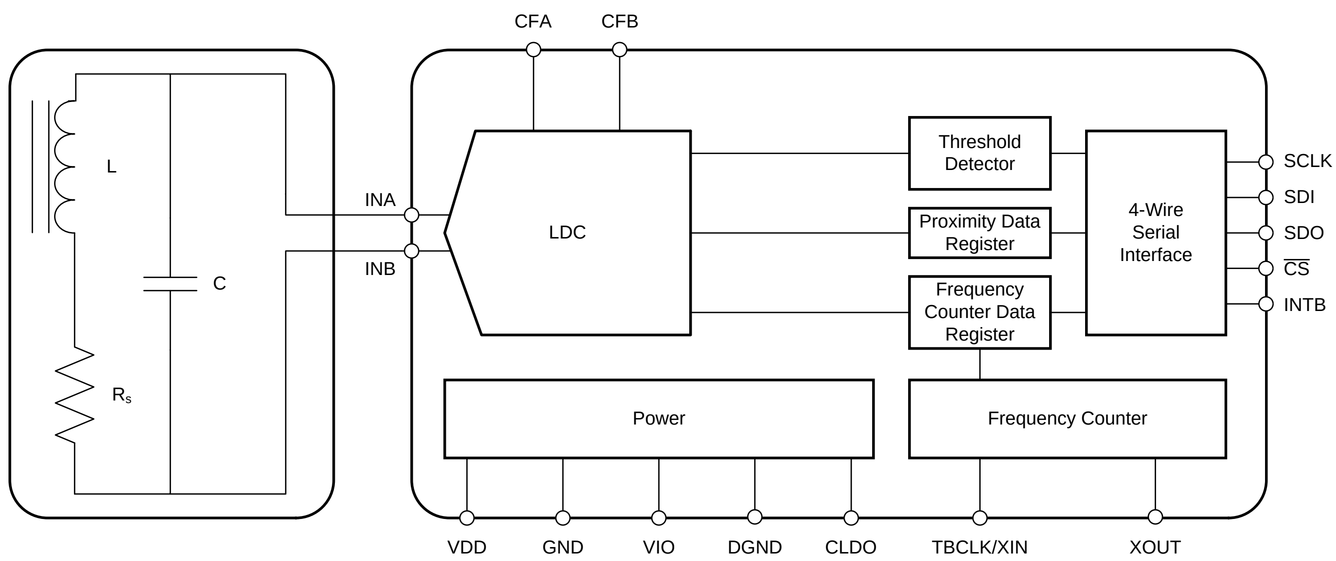
The LDC1000 is an Inductance-to-Digital Converter that measures the parallel impedance of an LC resonator. It accomplishes this task by regulating the oscillation amplitude in a closed-loop configuration to a constant level, while monitoring the energy dissipated by the resonator. By monitoring the amount of power injected into the resonator, the LDC1000 can determine the value of Rp; it returns this as a digital value which is inversely proportional to Rp.

The threshold detector block provides a comparator with hysteresis. With the threshold registers programed and comparator enabled, proximity data register is compared with threshold registers and INTB terminal indicates the output.

The device has a simple 4-wire SPI interface. The INTB terminal provides multiple functions which are programmable with SPI.

The device has separate supplies for Analog and I/O, with analog operating at 5 V and I/O at 1.8-5 V. The integrated LDO needs a 56 nF capacitor connected from CLDO terminal to GND.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Inductive Sensing

An AC current flowing through a coil will generate an AC magnetic field. If a conductive material, such as a metal target, is brought into the vicinity of the coil, this magnetic field will induce circulating currents (eddy currents) on the surface of the target. These eddy currents are a function of the distance, size, and composition of the target. The eddy currents then generate their own magnetic field, which opposes the original field generated by the coil. This mechanism is best compared to a transformer, where the coil is the primary core and the eddy current is the secondary core. The inductive coupling between both cores depends on distance and shape. Hence the resistance and inductance of the secondary core (eddy current), shows up as a distant dependent resistive and inductive component on the primary side (coil). The figures (Figure 5 to Figure 8) below show a simplified circuit model.

Feature Description (continued)

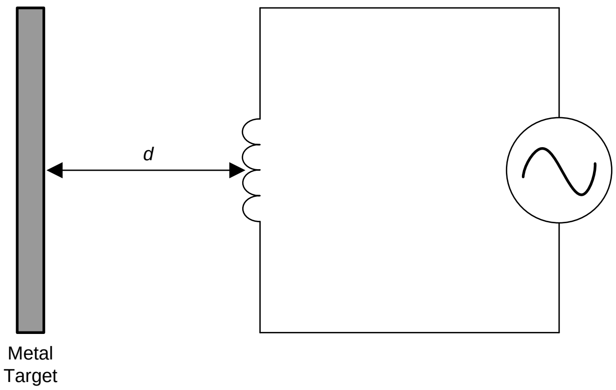


Figure 5. Inductor With a Metal Target

Eddy currents generated on the surface of the target can be modeled as a transformer as shown in Figure 6. The coupling between the primary and secondary coils is a function of the distance and the conductor's characteristics. In Figure 6, the inductance Ls is the coil's inductance, and Rs is the coil's parasitic series resistance. The inductance L(d), which is a function of distance, d, is the coupled inductance of the metal target. Likewise, R(d) is the parasitic resistance of the eddy currents and is also a function of distance.

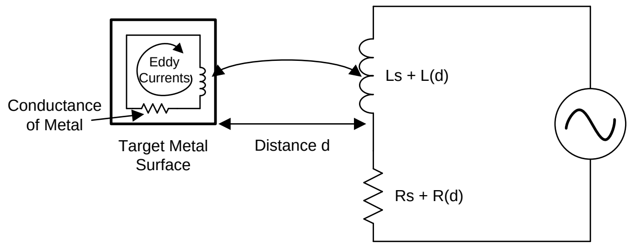


Figure 6. Metal Target Modeled as L and R With Circulating Eddy Currents

Generating an alternating magnetic field with just an inductor will consume a large amount of power. This power consumption can be reduced by adding a parallel capacitor, turning it into a resonator as shown in Figure 7. In this manner the power consumption is reduced to the eddy and inductor losses Rs+R(d) only.

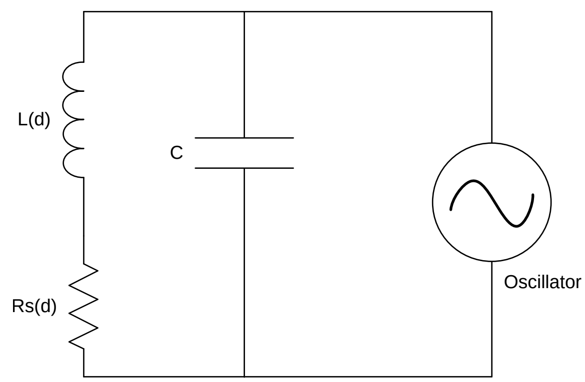


Figure 7. LC Tank Connected to Oscillator

The LDC1000 doesn't measure the series resistance directly; instead it measures the equivalent parallel resonance impedance Rp (see Figure 8). This representation is equivalent to the one shown in Figure 8, where the parallel resonance impedance Rp(d) is given by:

Feature Description (continued)

$$Rp(d) = \frac{Ls + L(d)}{[Rs + R(d)] \times C} \quad (1)$$

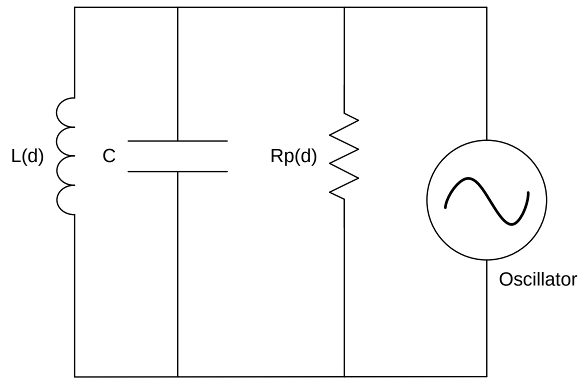


Figure 8. Equivalent Resistance of Rs in Parallel With LC Tank

Figure 9 below shows the variation in Rp as a function of distance for a 14 mm diameter PCB coil (Sensor Details: Table 20). The target in this example is a section of a 2 mm thick stainless steel disk.

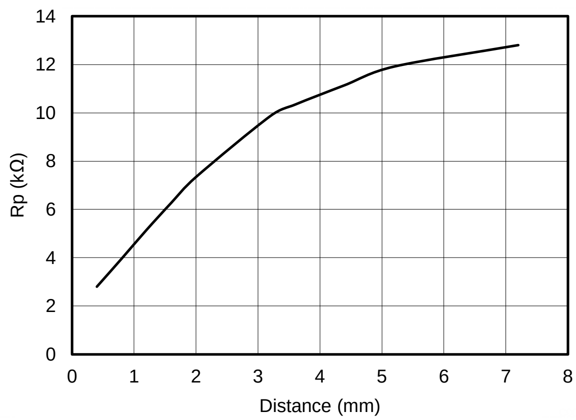


Figure 9. Typical Rp vs Distance With 14-mm PCB Coil

7.3.2 Measuring Rp With LDC1000

The LDC1000 supports a wide range of LC combinations, with oscillation frequencies ranging from 5 kHz to 5 MHz and Rp ranging from 798 Ω to 3.93 MΩ. This range of Rp can be viewed as the maximum input range of an ADC. As illustrated in Figure 9, the range of Rp is typically much smaller than the maximum input range supported by the LDC1000. To get better resolution in the desired sensing range, the LDC1000 offers a programmable input range through the Rp_MIN and Rp_MAX registers. Refer to *Calculation of Rp_MIN and Rp_MAX* for information on setting these registers.

When the resonance impedance Rp of the sensor drops below the programed Rp_MIN, the Rp output of the LDC will clip at its full scale output. This situation could, for example, happen when a target comes too close to the coil.

Feature Description (continued)

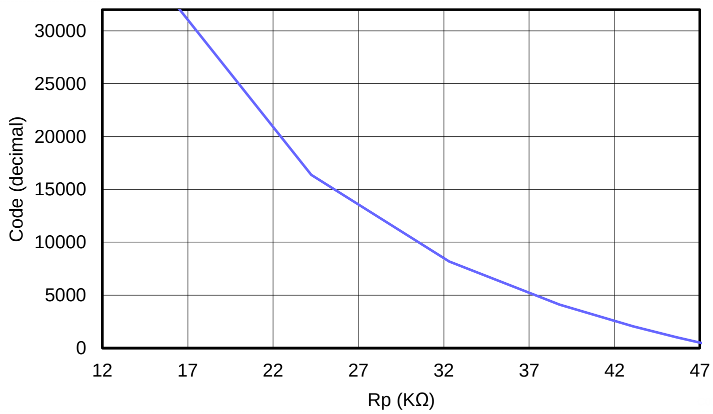


Figure 10. Transfer Characteristics of LDC1000 With Rp_MIN = 16.160 kΩ and Rp_MAX = 48.481 kΩ

The resonance impedance can be calculated from the digital output code as follows:

$R_P = (R_PMAX \times R_PMIN) / (R_PMIN \times (1-Y) + R_PMAX \times Y)$, in Ω.

Where:

- $Y = \text{Proximity Data}/2^{15}$
- Proximity data is the LDC output, register address 0x21 and 0x22. (2)

Example: If Proximity data (address 0x22:0x21) is 5000, Rp_MIN is 2.394 kΩ, and Rp_MAX is 38.785 kΩ ,the resonance impedance is given by:

$Y = 5000/2^{15} = 0.1526$

RP = (38785 × 2394) ÷ (2394 × (1 – 0.1526) + 38785 × 0.1526) = (92851290 ÷ (2028.675 + 5918.591))

RP = 11.683 kΩ

7.3.3 Measuring Inductance With LDC1000

LDC1000 measures the sensor's frequency of oscillation using a frequency counter. The frequency counter timing is set by an external clock applied on TBCLK terminal. The sensor frequency can be calculated from the frequency counter register value (see registers 0x23 through 0x25) as follows:

$$\text{Sensor frequency, } f_{sensor} = \frac{1}{3} \times \frac{Fext}{Fcount} \times \text{Response time}$$

where

- Fext is the frequency of the external clock.
- Fcount is the value obtained from the Frequency Counter Data register (address 0x23,0x24,0x25).
- Response Time is the programmed response time (see LDC configuration register, address 0x04). (3)

The sensor inductance can be determined by:

$$L = \frac{1}{C \times (2\pi \times f_{sensor})^2}$$

where

- C is the parallel capacitance of the resonator (4)

Example: If Fext = 6MHz, Response time = 6144, C = 100 pF and measured Fcount = 3000 (dec) (address 0x23 through 0x25)

f_{sensor}=(1/3) × (6000000/3000) × (6144)= 4.096 MHz

Now using, $L = \frac{1}{C \times (2\pi \times f_{sensor})^2}$

Feature Description (continued)

Inductance, L = 15.098 µH

The accuracy of measurement largely depends upon the choice of the external time-base clock (TBCLK). A higher frequency will provide better measurement accuracy.

7.4 Device Functional Modes

7.4.1 Power Modes

The LDC1000 has two power modes:

- Active Mode : In this mode the Proximity data conversion is enabled.
- Standby Mode: This is the default mode on device power-up. In this mode conversion is disabled.

7.4.2 INTB Pin Modes

The INTB pin is a configurable output pin which can be used to drive an interrupt on an MCU. The LDC1000 provides three different modes on INTB pin:

1. Comparator Mode
2. Wake-Up Mode
3. DRDY Mode

LDC1000 has a built-in High and Low trigger threshold which registers as a comparator with programmable hysteresis or a special mode which can be used to wake up an MCU. These modes are explained in detail below.

7.4.2.1 Comparator Mode

In the Comparator mode, the INTB pin is asserted or deasserted when the proximity register value increases above Threshold High or decreases below Threshold Low registers respectively. In this mode, the LDC1000 essentially behaves as a proximity switch with programmable hysteresis.

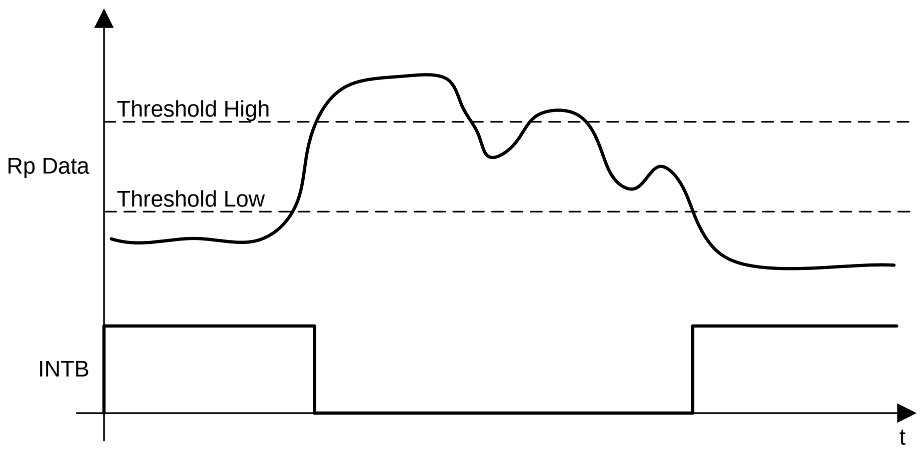


Figure 11. Behavior of INTB Pin in Comparator Mode

Device Functional Modes (continued)

7.4.2.2 Wake-Up Mode

In Wake-up mode, the INTB pin is asserted when proximity register value increases above Threshold High and deasserted when wake-up mode is disabled in INTB pin mode register.

This mode can be used to wake up an MCU which is asleep, to conserve power.

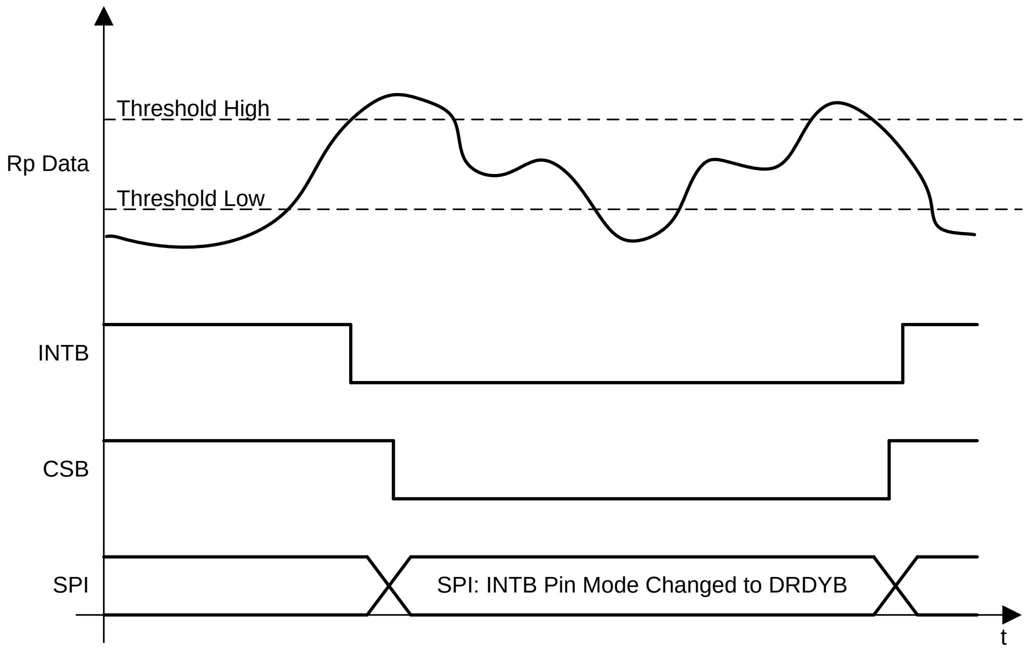


Figure 12. Behavior of INTB Pin in Wake-Up Mode

7.4.2.3 DRDYB Mode

In DRDY mode (default), the INTB pin is asserted every time the conversion data is available and deasserted once the read command on register 0x21 is registered internally; if the read is in progress, the pin is pulsed instead.

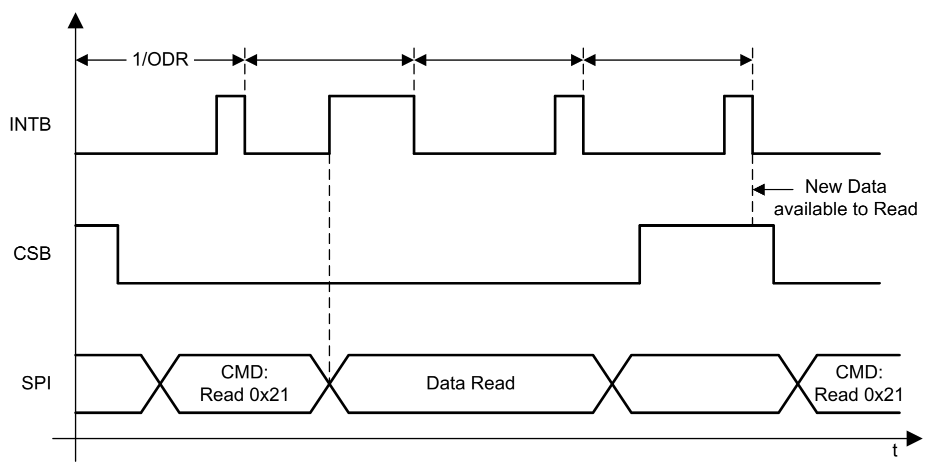


Figure 13. Behavior of INTB Terminal in DRDYB Mode With SPI Extending Beyond Subsequent Conversions

Device Functional Modes (continued)

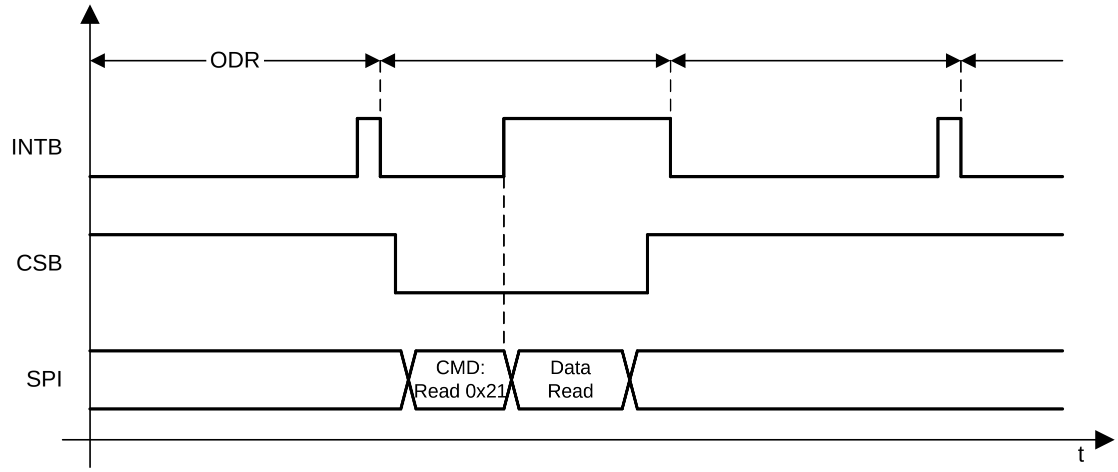


Figure 14. Behavior of INTB Pin in DRDYB Mode With SPI Reading the Data Within Subsequent Conversion

7.5 Programming

The LDC1000 uses a 4-wire SPI to access control and data registers. The LDC1051 is an SPI slave device and does not initiate any transactions.

7.5.1 SPI Description

A typical serial interface transaction begins with an 8-bit instruction, which is comprised of a read/write bit (MSB, R=1) and a 7-bit address of the register, followed by a Data field which is typically 8 bits. However, the data field can be extended to a multiple of 8 bits by providing sufficient SPI clocks. Refer to the *Extended SPI Transactions* section below.

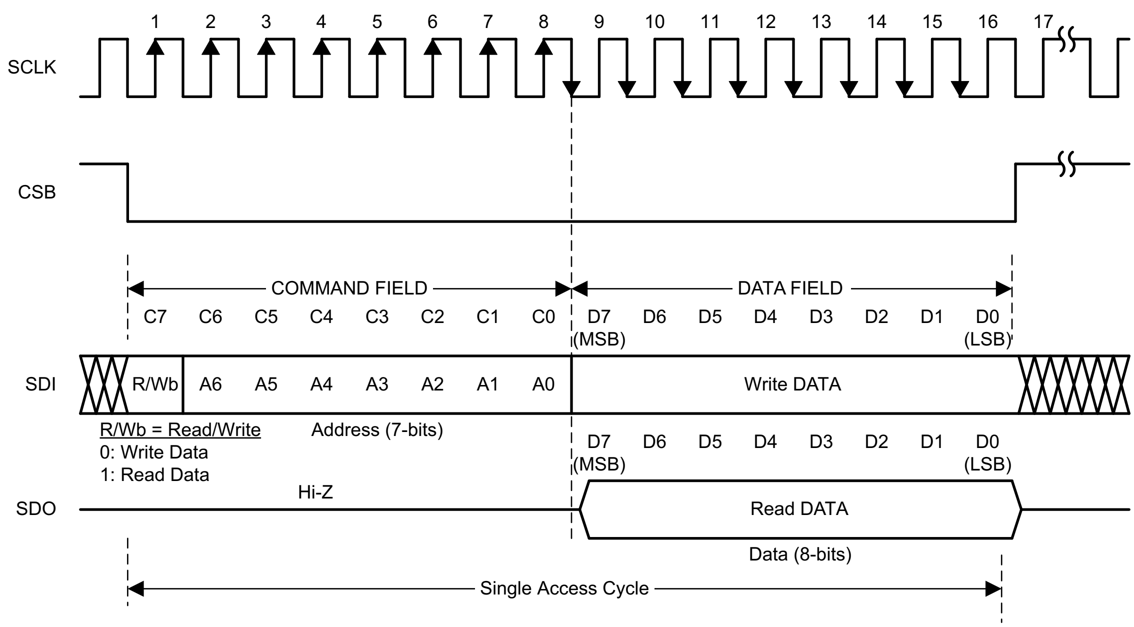


Figure 15. Serial Interface Protocol

Programming (continued)

Each assertion of chip select bar (CSB) starts a new register access. The R/Wb bit in the command field configures the direction of the access; a value of 0 indicates a write operation and a value of 1 indicates a read operation. All output data is driven on the falling edge of the serial clock (SCLK), and all input data is sampled on the rising edge of the serial clock (SCLK). Data is written into the register on the rising edge of the 16th clock. It is required to deassert CSB after the 16th clock; if CSB is deasserted before the 16th clock, no data write will occur.

The LDC1000 utilizes a 4-wire SPI interface to access control and data registers. The LDC1000 is an SPI slave device and does not initiate any transactions.

7.5.1.1 Extended SPI Transactions

A transaction may be extended to multiple registers by keeping the CSB asserted beyond the stated 16 clocks. In this mode, the register addresses increment automatically. CSB must be asserted during 8*(1+N) clock cycles of SCLK, where N is the amount of bytes to write or read during the transaction.

During an extended read access, SDO outputs the register contents every 8 clock cycles after the initial 8 clocks of the command field. During an extended write access, the data is written to the registers every 8 clock cycles after the initial 8 clocks of the command field.

Extended transactions can be used to read 16 bits of Proximity data and 24 bits of frequency data all in one SPI transaction by initiating a read from register 0x21.

7.6 Register Maps

Table 1. Register Description(1)(2)(3)

Register Name	Address	Direction	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Device ID	0x00	RO	0x84	Device ID							
Rp_MAX	0x01	R/W	0x0E	Rp Maximum							
Rp_MIN	0x02	R/W	0x14	Rp Minimum							
Watchdog Timer Frequency	0x03	R/W	0x45	Min Sensor Frequency							
LDC Configuration	0x04	R/W	0x1B	Reserved (000)			Amplitude		Response Time		
Reserved	0x05	RO	0x01	Reserved(00000001)							
Reserved	0x06	R/W	0xFF ??	Reserved							
Comparator Threshold High MSB	0x07	R/W	0xFF	Threshold High MSB							
Reserved	0x08	R/W	0x00 ??	Reserved							
Comparator Threshold Low MSB	0x09	R/W	0x00	Threshold Low MSB							
INTB Terminal Configuration	0x0A	R/W	0x00	Reserved (00000)					INTB_MODE		
Power Configuration	0x0B	R/W	0x00	Reserved (0000000)							PWR_MODE
Status	0x20	RO		OSC Dead	DRDYB	Wake-up	Comparator	Don't Care			
Proximity	0x21	RO		Proximity Data[7:0] Data LSB							
Proximity	0x22	RO		Proximity Data [15:8] Data MSB							

(1) Values of register fields which are unused should be set to default values only.
(2) Registers 0x01 through 0x05 are Read Only when the part is awake (PWR_MODE bit is SET)
(3) R/W: Read/Write. RO: Read Only. WO: Write Only.

Register Maps (continued)

Table 1. Register Description[(1)(2)(3)] (continued)

Register Name	Address	Direction	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Frequency Counter Data LSB	0x23	RO		FCOUNT LSB							
Frequency Counter Data Mid-Byte	0x24	RO		FCOUNT Mid Byte							
Frequency Counter Data MSB	0x25	RO		FCOUNT MSB							

Table 2. Revision ID

Address = 0x00, Default=0x80, Direction=RO		
Bit Field	**Field Name**	**Description**
7:0	Revision ID	Revision ID of Silicon.

Table 3. Rp_MAX

Address = 0x01, Default=0x0E, Direction=R/W		
Bit Field	**Field Name**	**Description**
7:0	Rp Maximum	Maximum Rp that LDC1000 needs to measure. Configures the input dynamic range of LDC1000. See Table 4 for register settings.

Table 4. Register Settings for Rp_MAX

Register setting	Rp (kΩ)
0x00	3926.991
0x01	3141.593
0x02	2243.995
0x03	1745.329
0x04	1308.997
0x05	981.748
0x06	747.998
0x07	581.776
0x08	436.332
0x09	349.066
0x0A	249.333
0x0B	193.926
0x0C	145.444
0x0D	109.083
0x0E	83.111
0x0F	64.642
0x10	48.481
0x11	38.785
0x12	27.704
0x13	21.547
0x14	16.160
0x15	12.120
0x16	9.235

Table 4. Register Settings for Rp_MAX (continued)

Register setting	Rp (kΩ)
0x17	7.182
0x18	5.387
0x19	4.309
0x1A	3.078
0x1B	2.394
0x1C	1.796
0x1D	1.347
0x1E	1.026
0x1F	0.798

Table 5. Rp_MIN

Address = 0x02, Default=0x14, Direction=R/W		
Bit Field	Field Name	Description
7:0	Rp Minimum	Minimum Rp that LDC1000 needs to measure. Configures the input dynamic range of LDC1000. See Table 6 for register settings.(1)

(1) This register needs a mandatory write as it defaults to 0x14.

Table 6. Register Settings for Rp_MIN

Register setting	Rp (kΩ)
0x20	3926.991
0x21	3141.593
0x22	2243.995
0x23	1745.329
0x24	1308.997
0x25	981.748
0x26	747.998
0x27	581.776
0x28	436.332
0x29	349.066
0x2A	249.333
0x2B	193.926
0x2C	145.444
0x2D	109.083
0x2E	83.111
0x2F	64.642
0x30	48.481
0x31	38.785
0x32	27.704
0x33	21.547
0x34	16.160
0x35	12.120
0x36	9.235
0x37	7.182
0x38	5.387
0x39	4.309
0x3A	3.078
0x3B	2.394

Table 6. Register Settings for Rp_MIN (continued)

Register setting	Rp (kΩ)
0x3C	1.796
0x3D	1.347
0x3E	1.026
0x3F	0.798

Table 7. Watchdog Timer Frequency

Address = 0x03, Default=0x45, Direction=R/W		
Bit Field	**Field Name**	**Description**
7:0	Min Sensor Frequency	Sets the watchdog timer. The Watchdog timer is set based on the lowest sensor frequency. $N = 68.94 \times \log_{10}\left(\frac{F}{2500}\right)$ where • F is the sensor frequency (5) Example: If Sensor frequency is 1Mhz Min Sensor Frequency=68.94*log10(1M/2500)=Round to nearest integer(179.38)=179

Table 8. LDC Configuration

Address = 0x04, Default=0x1B, Direction=R/W		
Bit Field	**Field Name**	**Description**
7:5	Reserved	Reserved to 0
4:3	Amplitude	Sets the oscillation amplitude 00:1V 01:2V 10:4V **11:Reserved**
2:0	Response Time	000: Reserved 001: Reserved 010: 192 **011: 384** 100: 768 101: 1536 110: 3072 111: 6144

Table 9. Comparator Threshold High MSB

Address = 0x07, Default=0xFF, Direction=R/W		
Bit Field	**Field Name**	**Description**
7:0	Threshold High	Threshold High Register.

Table 10. Comparator Threshold Low MSB

Address = 0x09, Default=0x00, Direction=R/W		
Bit Field	**Field Name**	**Description**
7:0	Threshold Low	Threshold Low Register.

Table 11. INTB Terminal Configuration

Address = 0x0A, Default=0x00, Direction=R/W		
Bit Field	**Field Name**	**Description**
7:3	Reserved	Reserved to 0
2:0	Mode	**000: All modes disabled** 001: Wake-up Enabled on INTB terminal 010: INTB terminal indicates the status of Comparator output 100: DRDYB Enabled on INTB terminal All other combinations are Reserved

Table 12. Power Configuration

Address = 0x0B, Default=0x00, Direction=R/W		
Bit Field	**Field Name**	**Description**
7:1	Reserved	Reserved to 0
0	PWR_MODE	**0:Standby mode** 1:Active Mode. Conversion is Enabled Refer to *Power Modes* for more details.

Table 13. Status

Address = 0x20, Default=NA, Direction=RO		
Bit Field	**Field Name**	**Description**
7	OSC status	1:Indicates oscillator overloaded and stopped 0:Oscillator working
6	Data Ready	1:No new data available 0:Data is ready to be read
5	Wake-up	1:Wake-up disabled 0:Wake-up triggered. Proximity data is more than Threshold High value.
4	Comparator	1:Proximity data is less than Threshold Low value 0:Proximity data is more than Threshold High value
3:0	Don't Care	

Table 14. Proximity Data LSB

Address = 0x21, Default=NA, Direction=RO		
Bit Field	**Field Name**	**Description**
7:0	Proximity Data[7:0]	Least Significant Byte of Proximity Data

Conversion data is updated to the proximity register only when a read is initiated on 0x21 register. If the read is delayed between subsequent conversions, these registers are not updated until another read is initiated on 0x21.

Table 15. Proximity Data MSB

Address = 0x22, Default=NA, Direction=RO		
Bit Field	**Field Name**	**Description**
7:0	Proximity data [15:8]	Most Significant Byte of Proximity data

Table 16. Frequency Counter LSB

Address = 0x23, Default=NA, Direction=RO		
Bit Field	**Field Name**	**Description**
7:0	FCOUNT LSB (FCOUNT[7:0])	LSB of Frequency Counter. Sensor frequency can be calculated using the output data rate. Please refer to the Measuring Inductance With LDC1000.

Table 17. Frequency Counter Mid-Byte

Address = 0x24, Default=NA, Direction=RO		
Bit Field	**Field Name**	**Description**
7:0	FCOUNT Mid byte (FCOUNT[15:8])	Middle Byte of Output data rate

Table 18. Frequency Counter MSB

Address = 0x25, Default=NA, Direction=RO		
Bit Field	**Field Name**	**Description**
7:0	FCOUNT MSB (FCOUNT[23:16])	MSB of Output data rate

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Calculation of Rp_MIN and Rp_MAX

Different sensing applications may have a different range of the resonance impedance Rp to measure. The LDC1000 measurement range of Rp is controlled by setting 2 registers – Rp_MIN and Rp_MAX. For a given application, Rp must never be outside the range set by these register values, otherwise the measured value will be clipped. For optimal sensor resolution, the range of Rp_MIN to Rp_MAX should not be unnecessarily large. The following procedure is recommended to determine the Rp_MIN and Rp_MAX register values.

8.1.1.1 Rp_MAX

Rp_MAX sets the upper limit of the LDC1000 resonant impedance input range.

- Configure the sensor such that the eddy current losses are minimized. As an example, for a proximity sensing application, set the distance between the sensor and the target to the maximum sensing distance.
- Measure the resonant impedance Rp using an impedance analyzer.
- Multiply Rp by 2 and use the next higher value from Table 7.

Note that setting Rp_MAX to a value not listed in Table 7 can result in indeterminate behavior.

8.1.1.2 Rp_MIN

Rp_MIN sets the lower limit of the LDC1051 resonant impedance input range.

- Configure the sensor such that the eddy current losses are maximized. As an example, for a proximity sensing application, set the distance between the sensor and the metal target to the minimum sensing distance.
- Measure the resonant impedance Rp using an impedance analyzer.
- Divide the Rp value by 2 and then select the next lower Rp value from Table 9.

Note that setting Rp_MIN to a value not listed on Table 9 can result in indeterminate behavior. In addition, Rp_MIN powers on with a default value of 0x14 which must be set to a value from Table 9 prior to powering on the LDC.

8.1.2 Output Data Rate

Output data rate of LDC1000 depends on the sensor frequency, f_{sensor} and 'Response Time' field in LDC Configuration register(Address:0x04).

$$\text{Output Data Rate} = \frac{f_{sensor}}{\left(\frac{\text{Response time}}{3}\right)} \tag{6}$$

8.1.3 Choosing Filter Capacitor (CFA and CFB Pins)

The filter capacitor is critical to the operation of the LDC1000. The capacitor should be low leakage, temperature stable, and it must not generate any piezoelectric noise (the dielectrics of many capacitors exhibit piezoelectric characteristics and any such noise is coupled directly through Rp into the converter). The optimal capacitance values range from 20 pF to 100 nF. The value of the capacitor is based on the time constant and resonating frequency of the LC tank.

Application Information (continued)

If a ceramic capacitor is used, then a C0G (or NP0) grade dielectric is recommended; the voltage rating should be ≥10 V. The traces connecting CFA and CFB to the capacitor should be as short as possible to minimize any parasitics.

For optimal performance, the chosen filter capacitor, connected between pinsCFA and CFB, needs to be as small as possible, but large enough such that the active filter does not saturate. The size of this capacitor depends on the time constant of the sense coil, which is given by L/Rs, (L=inductance, Rs=series resistance of the inductor at oscillation frequency). The larger this time constant, the larger filter capacitor is required. Hence, this time constant reaches its maximum when there is no target present in front of the sensing coil.

The following procedure can be used to find the optimal filter capacitance:

1. Start with a large filter capacitor. For a ferrite core coil, 10 nF is usually large enough. For an air coil or PCB coil, 100 pF is usually large enough.
2. Power on the LDC and set the desired register values. Minimize the eddy currents losses. This is done by minimizing the amount of conductive target covering the sensor. For an axial sensing application, the target should be at farthest distance from coil. For a lateral or angular position sensing application, the target coverage of the coil should be minimized.
3. Observe the signal on the CFB terminal using a scope. Because this node is very sensitive to capacitive loading, it is recommended to use an active probe. As an alternative, a passive probe with a 1 kΩ series resistance between the tip and the CFB terminal can be used.
4. Vary the values of the filter capacitor until that the signal observed on the CFB terminal has an amplitude of approximate 1 V peak-to-peak. This signal scales linearly with the reciprocal of the filter capacitance. For example, if a 100 pF filter capacitor is applied and the signal observed on the CFB terminal has a peak-to-peak value of 200 mV, the desired 1 V peak-to-peak value is obtained using a 200 mV / 1 V * 100 pF = 20 pF filter capacitor.

8.2 Typical Application

8.2.1 Axial Distance Sensing Using a PCB Sensor With LDC1000

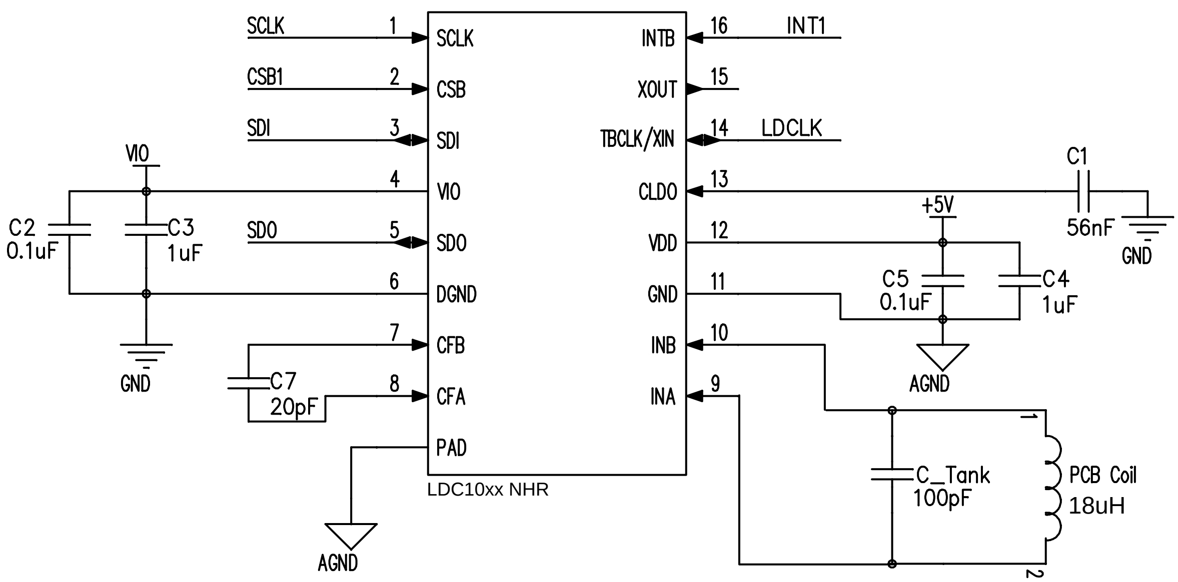


Figure 16. Typical Application Schematic, LDC10xx

Typical Application (continued)

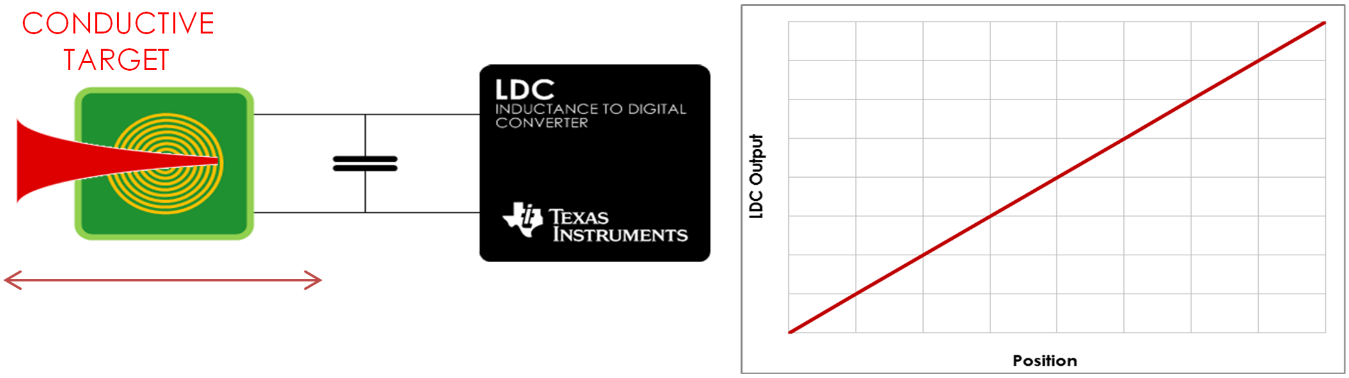


Figure 17. Linear Position Sensing

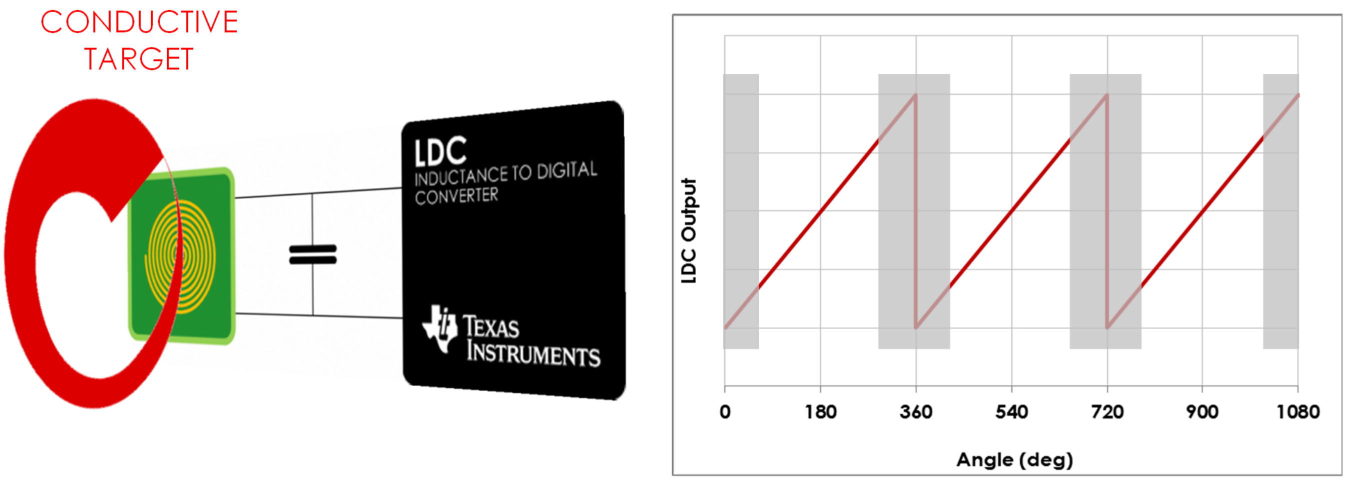


Figure 18. Angular Position Sensing

8.2.1.1 Design Requirements

For this design example, use the following as the input parameters.

Table 19. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Minimum sensing distance	1 mm
Maximum sensing distance	8 mm
Output data rate	78 KSPS (Max data rate with LDC10xx series)
Number of PCB layers for sensor	2 layers

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Sensor and Target

In this example, consider a sensor with the below characteristics.

Table 20. Sensor Characteristics

PARAMETER	VALUE
Layers	2

Table 20. Sensor Characteristics (continued)

PARAMETER	VALUE
Thickness of copper	1 Oz
Coil shape	Circular
Number of turns	23
Trace thickness	4 mil
Trace spacing	4 mil
PCB core material	FR4
Rp @ 1 mm	5 kΩ
Rp @ 8 mm	12.5 kΩ
Nominal Inductance	18 µH

Target material used is stainless steel

8.2.1.2.2 Calculating Sensor Capacitor

Sensor frequency depends on various factors in the application. In this example because one of the design parameter is to achieve output data rate of 78 KSPS, sensor frequency can be calculated as below.

$$\text{Output Data Rate} = \frac{f_{sensor}}{\left(\frac{\text{Response time}}{3}\right)} \tag{7}$$

With the lowest response time of 192 and output data rate of 78 KSPS, sensor frequency calculated using the above formula is 4.99 MHz.

Now, using the below formula sensor capacitor is calculated to be 55 pF with a sensor inductance of 18 µH

$$L = \frac{1}{C \times (2\pi \times f_{sensor})^2} \tag{8}$$

8.2.1.2.3 Choosing Filter Capacitor

Using the steps given in *Choosing Filter Capacitor (CFA and CFB Pins)* filter capacitor for the example sensor is 20 pF. Below waveform shows the pattern on CFB terminal with 100 pF and 20 pF filter capacitor.

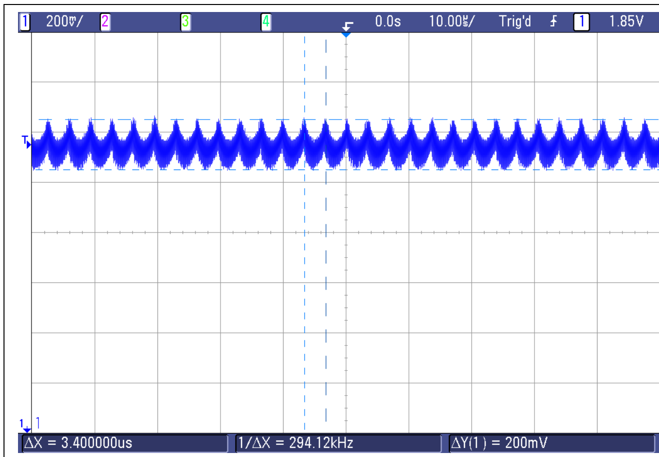


Figure 19. Waveform on CFB With 100 pF

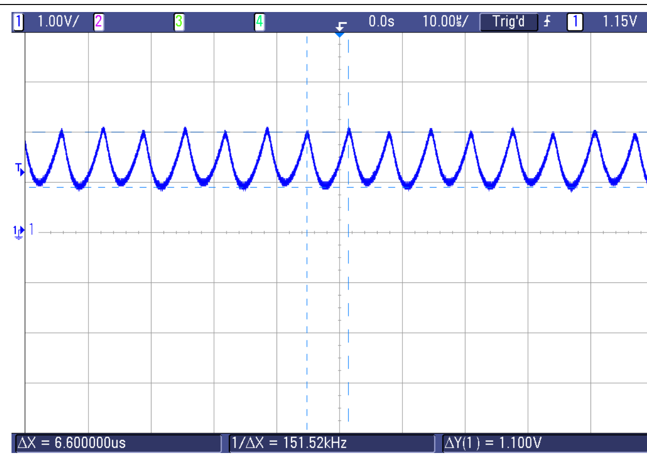


Figure 20. Waveform on CFB With 20 pF

8.2.1.2.4 Setting Rp_MIN and Rp_MAX

Calculating value for Rp_MAX Register : Rp at 8 mm is 12.5 kΩ, 12500×2 = 25000. In Table 7, then 27.704 kΩ is the nearest value larger than 25 kΩ; this corresponds to Rp_MAX value of 0x12.

Calculating value for Rp_MIN Register : Rp at 1mm is 5 kΩ, 5000/2 = 2500. In Table 6, 2.394 kΩ is the nearest value lower than 2.5 kΩ; this corresponds to Rp_MIN value of 0x3B.

8.2.1.2.5 Calculating Minimum Sensor Frequency

Using,

$$N = 68.94 \times \log_{10}\left(\frac{F}{2500}\right) \tag{9}$$

N is 227.51, round off to 228 decimal. This value has to be written into Watchdog Timer Register, which is used to wake up the internal circuit when the sensor is saturated.

8.2.1.3 Application Curve

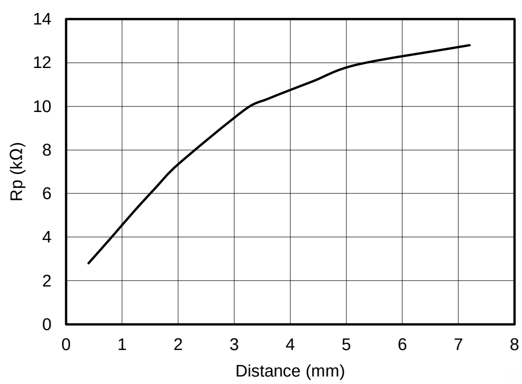


Figure 21. Rp vs Distance

9 Power Supply Recommendations

The LDC1000 is designed to operate from an analog supply range of 4.75 V to 5.25 V and digital I/O supply range of 1.8 V to 5.25 V. The analog supply voltage should be greater than or equal to the digital supply voltage for proper operation of the device. The supply voltage should be well regulated. If the supply is located more than a few inches from the LDC1000, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 10 uF is a typical choice.

10 Layout

10.1 Layout Guidelines

- The VDD and VIO terminal should be bypassed to ground with a low ESR ceramic bypass capacitor. The typical recommended bypass capacitance is 0.1 uF ceramic with a X5R or X7R dielectric.
- The optimum placement is closest to the VDD/VIO and GND/DGND pins of the device. Take care to minimize the loop area formed by the bypass capacitor connection, the VDD/VIO terminal, and the GND/DGND terminal of the IC. See Figure 22 for a PCB layout example.
- The CLDO terminal should be bypassed to digital ground (DGND) with a 56-nF ceramic bypass capacitor.
- The filter capacitor selected for the application using the procedure described in section *Choosing Filter Capacitor (CFA and CFB Pins)* is connected between CFA and CFB terminals. Place the filter capacitor close to the CFA and CFB terminals. Do not use any ground or power plane below the capacitor and the trace connecting the capacitor and the CFA /CFB terminals.
- Use of two separate ground plane for GND and DGND is recommended with a start connection. See Figure 22 for a PCB layout example.

10.2 Layout Example

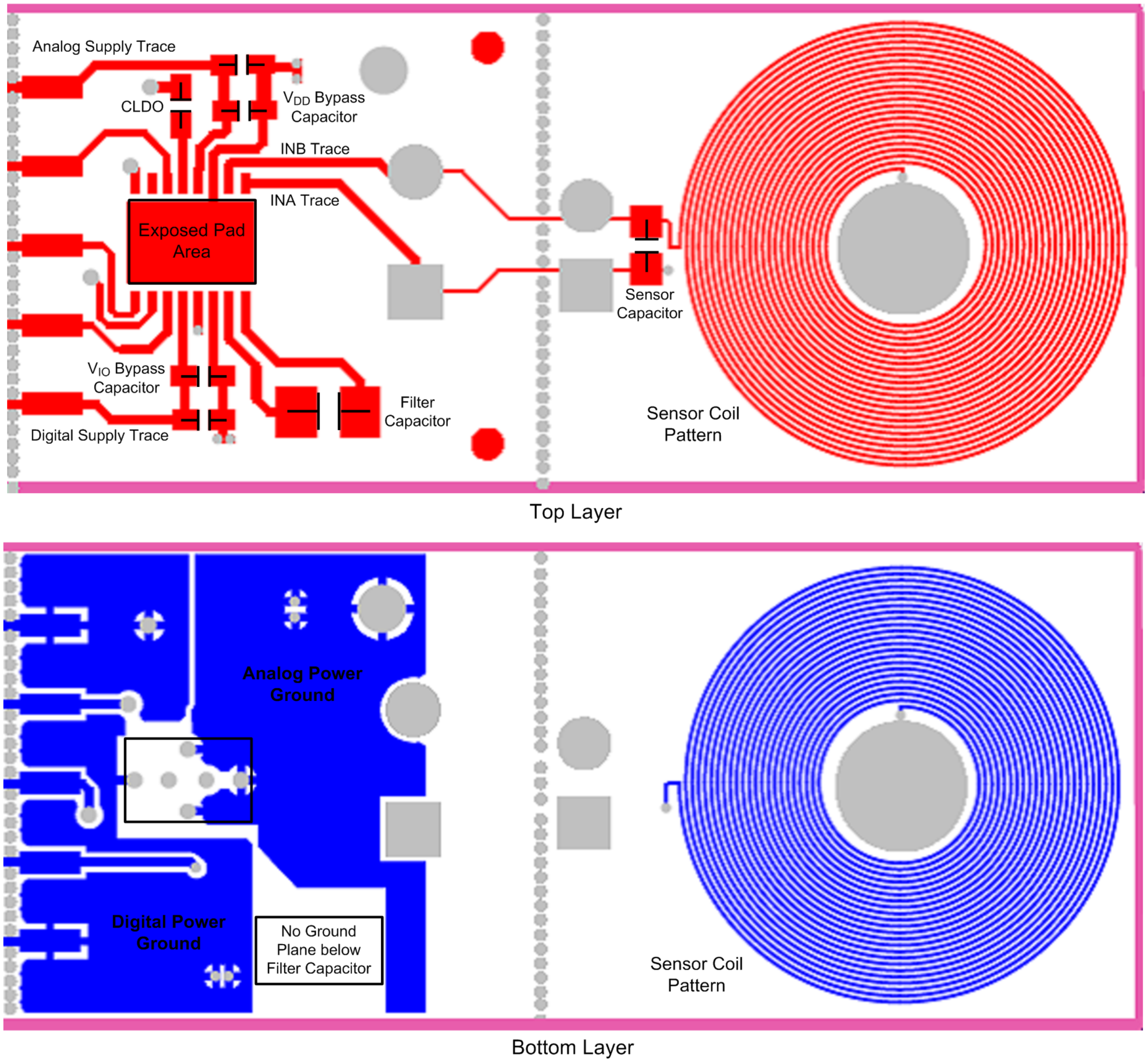


Figure 22. LDC10xx Board Layout

11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LDC1000NHRJ	ACTIVE	WSON	NHR	16	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LDC1000	Samples
LDC1000NHRR	ACTIVE	WSON	NHR	16	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LDC1000	Samples
LDC1000NHRT	ACTIVE	WSON	NHR	16	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LDC1000	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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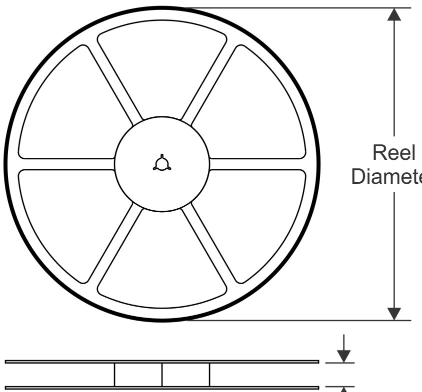
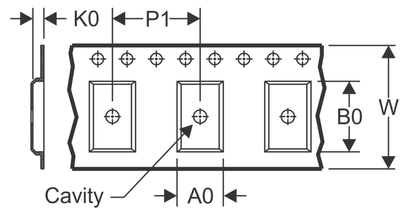
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

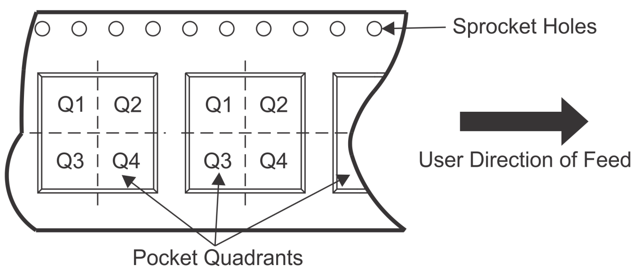


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

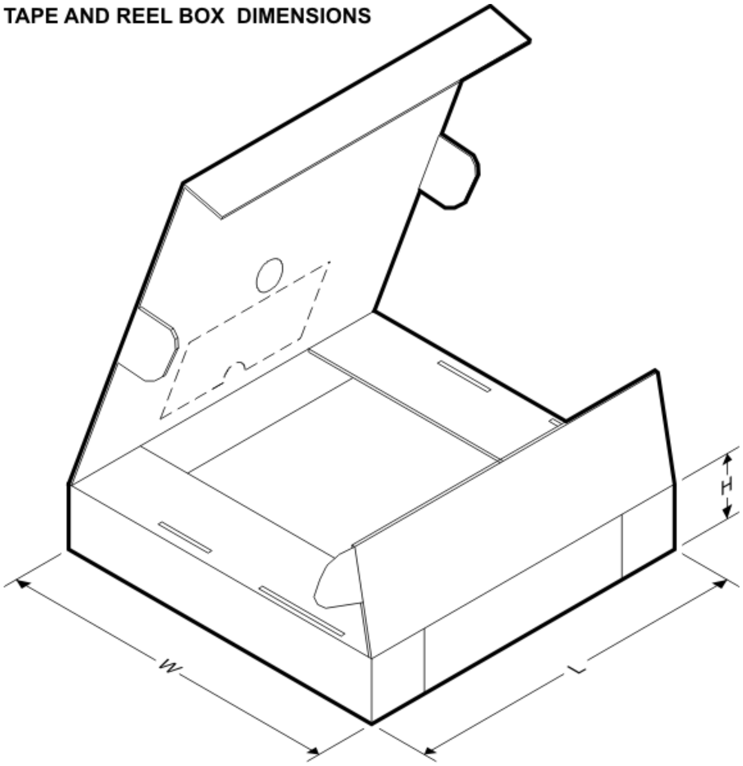
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LDC1000NHRJ	WSON	NHR	16	4500	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LDC1000NHRR	WSON	NHR	16	1000	178.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LDC1000NHRT	WSON	NHR	16	250	178.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1

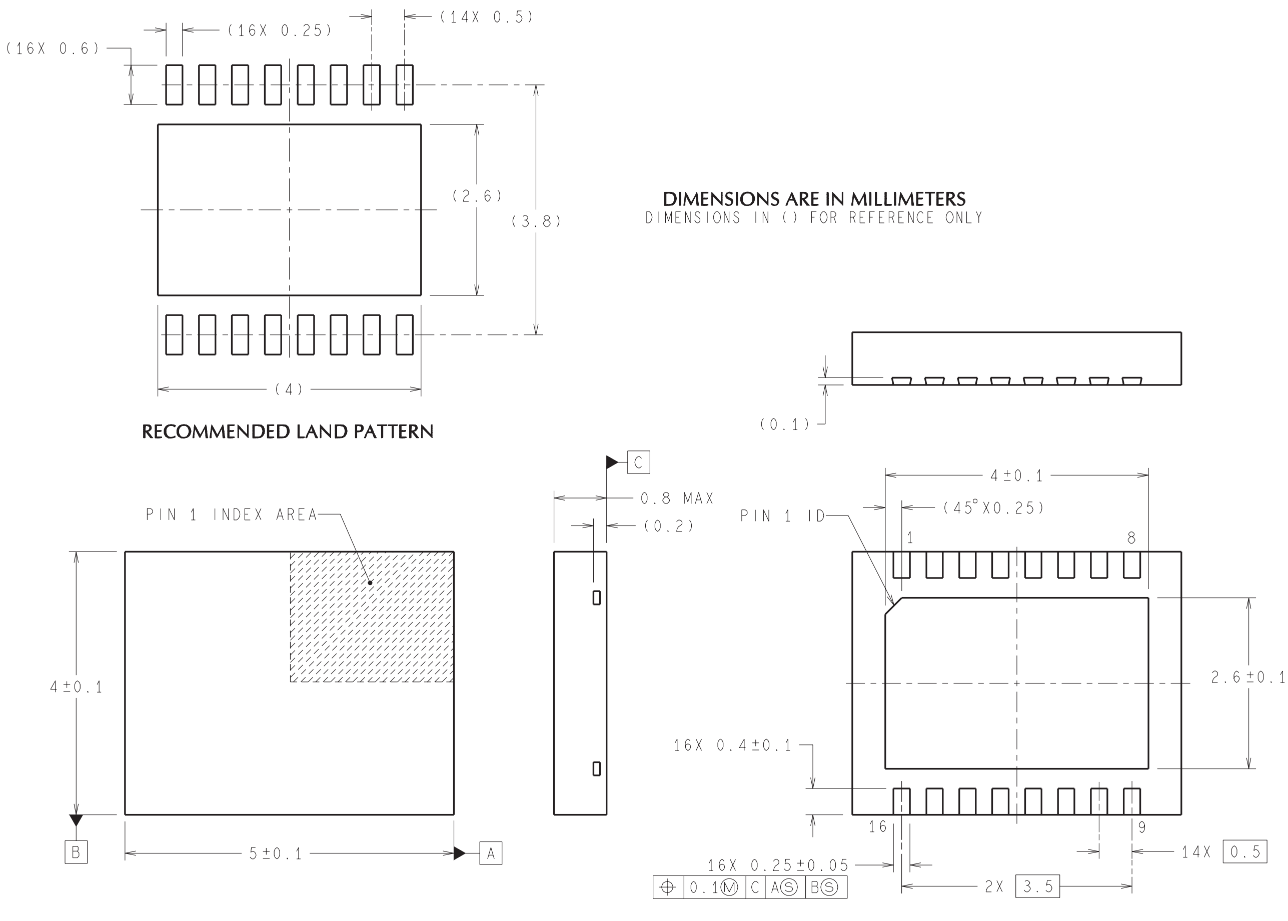
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LDC1000NHRJ	WSON	NHR	16	4500	367.0	367.0	35.0
LDC1000NHRR	WSON	NHR	16	1000	210.0	185.0	35.0
LDC1000NHRT	WSON	NHR	16	250	210.0	185.0	35.0

NHR0016B



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