

LC898150XH

Advance Information

Summary of Specification for SMA & Open-AF Control LSI

Overview

LC898150XH is a system LSI integrating a EEPROM and peripherals including analog circuits for SMA-OIS (Optical Image Stabilization) / AF (Open-Auto Focus) control and PWM / constant current drivers.

Features

- Hard wired digital signal processing
 - ◆ SMA-OIS Control I/F
 - ◆ FST(Fast Settling Time) Function for AF
- Memory
 - ◆ 64byte EEPROM
- Peripherals
 - ◆ AD Converter 12 bit Input 2ch
 - ◆ DA Converter 8 bit Output 1ch for Offset Adjust to OpAmp
 - ◆ Sensor Hub I/F (4/3-wire Serial I/F)
 - ◆ ISP I/F (2-wire Serial I/F Circuit)
 - ◆ OpAmp (Settling time: < 1 μ s R2/R1=15)
 $V_{adc} = V_w * (R2/R1 + 1) - V_{dac} * R2/R1$
(R1, R2, V_{adc}, V_w, V_{dac} → refer to Block Diagram)
 - ◆ OSC (Oscillator) typ. 48 MHz (with Frequency Adjustment Function)
 - ◆ LDO (Low Drop-Out Regulator)
 - ◆ PLL (Input: 6-48 MHz Output: 192 MHz)
 - ◆ HSYNC/Interrupt I/F
- Driver
 - ◆ OIS PWM Sink Driver (x4ch)
 - ◆ OP-AF (bi-direction)
Constant Current Linear Driver (x1ch, I_{full} = 130 mA)
- Power supply voltage
 - ◆ LDO/OSC/PLL DVDD = 2.6 V to 3.3 V
 - ◆ Driver/AD/DA/OpAmp VM = 2.6 V to 3.3 V
 - ◆ 1.8 V I/O IOVDD = 1.7 V to 3.3 V
 - ◆ Core Logic generated by on-chip LDO
- Gnd
 - ◆ LDO/OSC/PLL/AD/DA/OpAmp/1.8V IO/Core logic VSS
Driver PGND
- Package
 - ◆ WLCSP21 (1.17 mm x 2.77 mm) Pitch: 0.4 mm
Thickness: Max. 0.33 mm with Back Coat
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

This document contains information on a new product. Specifications and information herein are subject to change without notice.



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WLCSP21 1.17x2.77x0.30
CASE 567UJ

LC898150XH

ORDERING INFORMATION

Part Number	Package	Shipping†
LC898150XH-MH	WLCSP21 (Pb-Free, Halogen-Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

BLOCK DIAGRAM

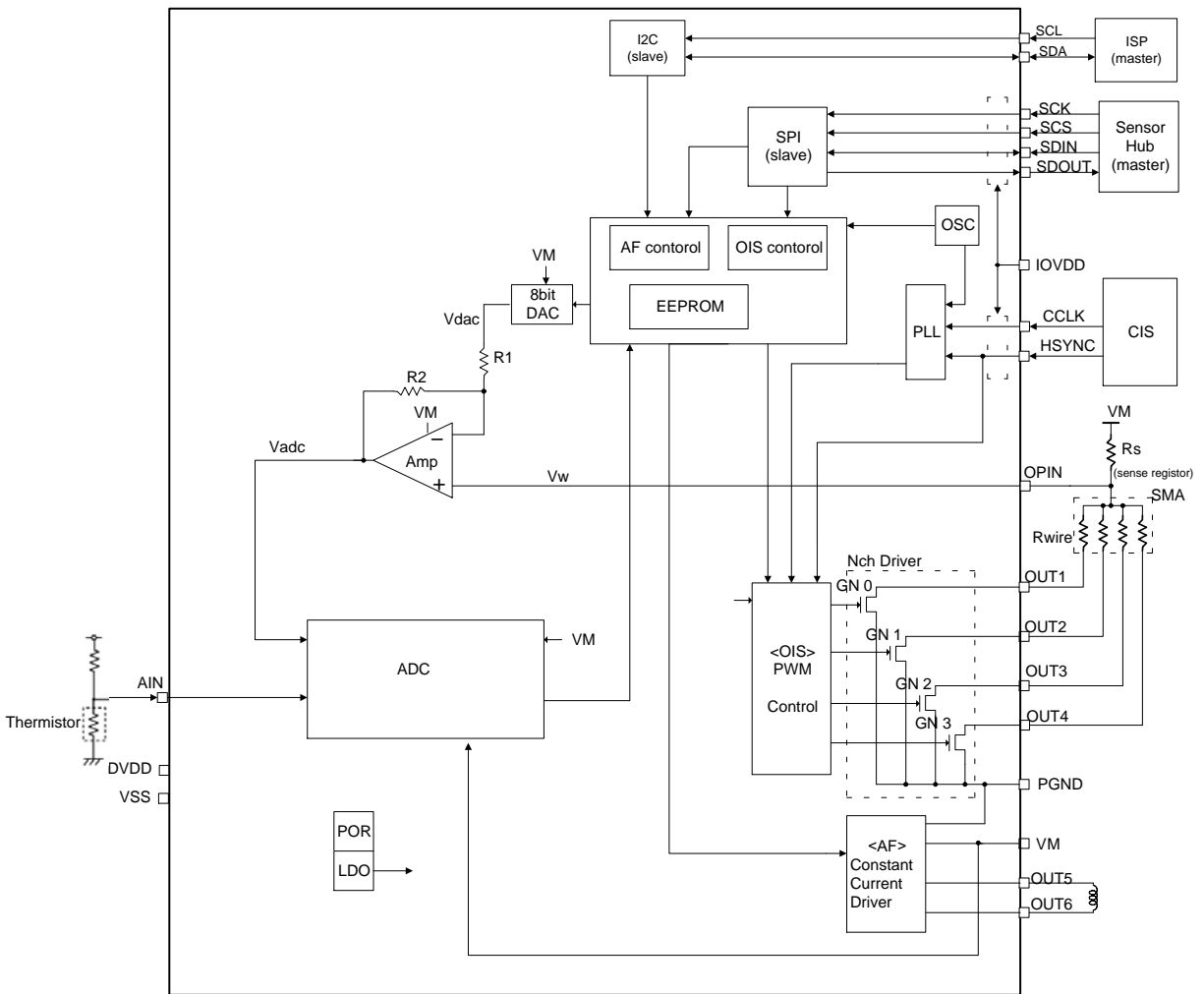


Figure 1. Block Diagram

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PIN ASSIGN

bottom view

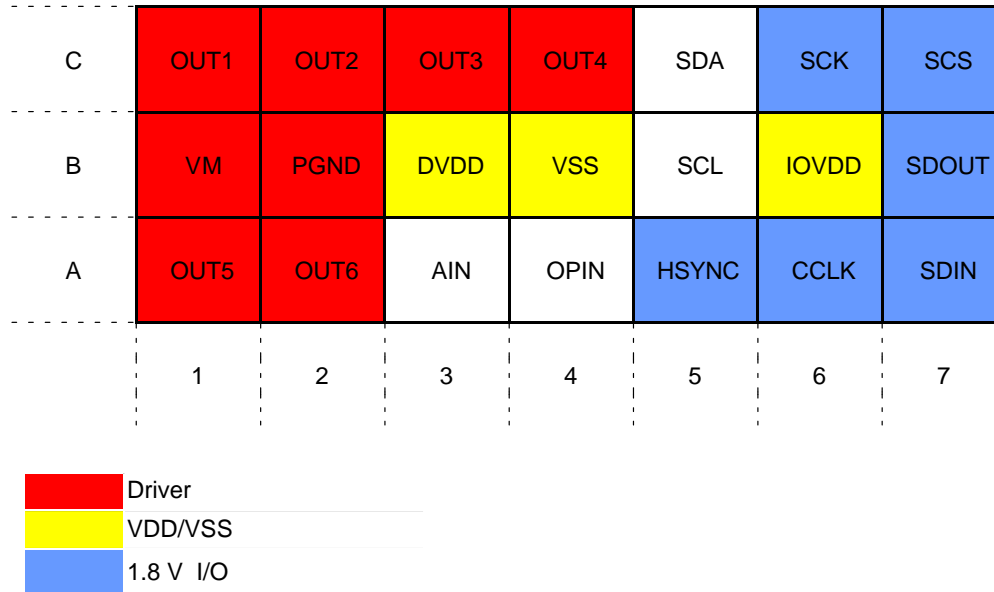


Figure 2. Pin Assign

Table 1. PIN DESCRIPTION

No.	Pin	I/O	I/O Spec	Primary Function	Sub Functions	Init
1	SCS	I	*2	Sensor Hub I/F Chip Select Input (4/3-wire slave)		Z
2	SCK	I	*2	Sensor Hub I/F Clock Input (4/3-wire slave)		Z
3	SDIN	B	*2	Sensor Hub I/F Data Input (4-wire slave)	Sensor Hub I/F Data (3-wire slave)	Z
4	SDOUT	B	*2	Sensor Hub I/F Data Output (4-wire slave)	Interrupt out	Z
5	SCL	B	OD*1	ISP I/F Clock (2-wire slave)		Z
6	SDA	B	OD*1	ISP I/F Data (2-wire slave)		Z
7	CCLK	I	*2	Clock Input for PLL		Z
8	HSYNC	B	OD*2	Hsync or OIS pulse from CIS	Interrupt input Interrupt output	Z
9	OPIN	I	Analog	Analog Input for Opamp		-
10	AIN	I	Analog	Analog Input		-
11	OUT1	O		SMA Driver	Output for Test	Z
12	OUT2	O		SMA Driver	Output for Test	Z
13	OUT3	O		SMA Driver	Output for Test	Z
14	OUT4	O		SMA Driver	Output for Test	Z
15	OUT5	O		Open-AF Driver+		Z
16	OUT6	O		Open-AF Driver-		Z
17	DVDD	P		Power		-
18	VSS	P		GND		-
19	IOVDD	P		I/O Power		-
20	VM	P		Driver Power		-
21	PGND	P		Driver GND		-

NOTES:*1: SCL SDA tolerate 3.0 V input at the time of power off.

*2: SCK, SCS, SDIN, SDOUT, CCLK, HSYNC tolerate 1.8 V input at the time of power off.

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ELECTRICAL CHARACTERISTICS

Table 2. ABSOLUTE MAXIMUM RATINGS at VSS = 0 V, PGND = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V _{DD30} max	Ta ≤ 25°C	-0.3 ~ 4.6	V
	V _M max	Ta ≤ 25°C	-0.3 ~ 4.6	
	V _{IO} max	Ta ≤ 25°C	-0.3 ~ 4.6	
Input/Output voltage	V _{AI30} , V _{AO30}	Ta ≤ 25°C	-0.3 ~ V _{DD30} +0.3	V
	V _{MI30} , V _{MO30}	Ta ≤ 25°C	-0.3 ~ V _{M30} +0.3	
	V _{II} , V _{IOO}	Ta ≤ 25°C	-0.3 ~ V _{IO} 18+0.3	V
Output Peak current (Note 1)	I _{opeak}	OUT1-OUT4 t ≤ 1 mS ON-duty ≤ 25%	300	mA
Storage temperature	T _{stg}		-55 ~ 125	°C
Operating temperature	Topr1	Read for EEPROM	-30 ~ 85	°C
	Topr2	Program&Erase for EEPROM	-30 ~ 70	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. OUT1-4 Only 1 output is "ON".

Table 3. ALLOWABLE OPERATING RATINGS at Ta = -30 ~ 85°C, VSS = 0 V, PGND = 0 V

Parameter	Symbol	Min	Typ	Max	Unit
3.0 V Power Supply (AVDD)					
Power supply voltage	V _{DD30}	2.6	2.8	3.3	V
Input voltage range	V _{INA}	0	-	V _{DD30}	V
3.0 V Power Supply (VM)					
Power supply voltage	V _{M30}	2.6	2.8	the lower of 3.3 and AVDD+0.5 (TBD)	V
Input voltage range	V _{INM}	0	-	V _{M30}	V
1.8 V Power Supply (IOVDD)					
Power supply voltage	V _{IO}	1.7	1.8	3.3	V
Input voltage range	V _{INI}	0	-	V _{IO}	V

Table 4. D.C. CHARACTERISTICS: INPUT/OUTPUT

at Ta = -30 ~ 85°C, VSS = 0 V, PGND = 0 V, DVDD = 2.6 ~ 3.3 V, IOVDD = 1.7 ~ 3.3 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Applicable Pins
High-level input voltage	V _{IH}	CMOS Schmitt	0.75 IOVDD			V	SCK, SCS, SDIN, SDOUT, CCLK, HSYNC
Low-level input voltage	V _{IL}					0.25 IOVDD	
High-level input voltage	V _{IH}	CMOS Schmitt	1.4			V	SCL, SDA
Low-level input voltage	V _{IL}					0.4	
High-level output voltage	V _{OH}	IOH = -2 mA	IOVDD - 0.2			V	SDOUT, SDIN
Low-level output voltage	V _{OL}	IOL = 2 mA			0.2	V	SDOUT, HSYNC, SDIN, SCL, SDA
Pull Down resistor	R _{dn}		20		250	kΩ	SCK, SCS, SDIN, SDOUT, CCLK, HSYNC

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Table 5. DRIVER OUTPUT (OUT1–OUT6) at Ta = 25°C, VSS = 0 V, PGND = 0 V, DVDD = VM = 2.8 V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Output Current OUT5, OUT6	I _{full}	Full Code OP–AF (bidirection)	–	130	–	mA
Output ON resistance OUT1–OUT4	R _{on}	Nch resistance	–	1.0	–	Ω
Output ON resistance OUT5, OUT6		Full code Total On resistance	–	2.2	–	Ω

Calculation method of max. current (I_{max})

R_{coil}*1 : Coil resistance of actuator R_b*1: Wiring resistance of the board

$$VM / (R_{coil} + R_b + R_{on}) \geq I_{full}$$

$$I_{max} = I_{full}$$

$$VM / (R_{coil} + R_b + R_{on}) < I_{full}$$

$$I_{max} = VM / (R_{coil} + R_b + R_{on})$$

*1: These parameters do not depending on this LSI. Please use the appropriate value.

Table 6. NON-VOLATILE MEMORY CHARACTERISTICS

Item	Symbol	Condition	Min	Typ	Max	Unit	Applicable Circuit
Endurance	EN				1000	Cycles	EEPROM
Data retention	RT		10			Years	
Write time	t _{WT}				20	ms	

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AC CHARACTERISTICS

Power Sequence

- Power ON → OFF → ON sequence

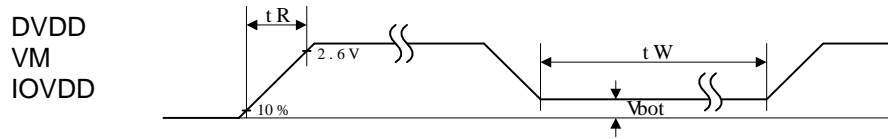


Figure 3. Power ON → OFF → ON Sequence

Table 7.

Item	Symbol	Min	Typ	Max	Units
Rise time	tR			3	ms
Wait time	tW	100			ms
Bottom Voltage	Vbot			0.2	V

- Injection order and limitation of DVDD, VM, IOVDD is below

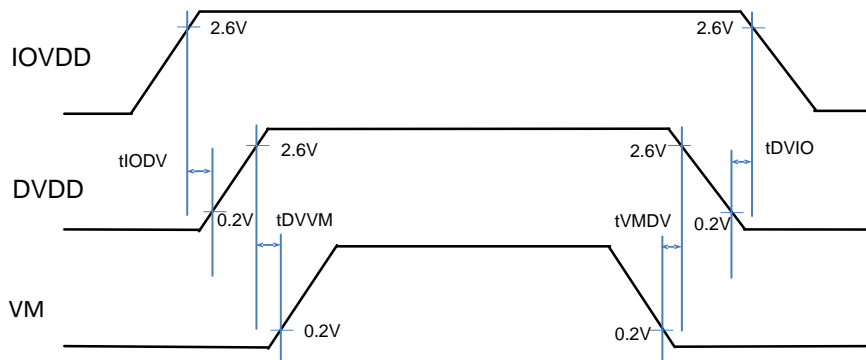


Figure 4.

Table 8.

Item	Symbol	Min	Typ	Max	Units
IOVDD ON to DVDD ON	tIODV	0			ms
DVDD ON to VM ON	tDVVM	0			ms
VM OFF to DVDD OFF	tVMDV	0			ms
DVDD OFF to IOVDD OFF	tDVIO	0		*	ms

* Please make IOPRSTB (303Eh, bit0 or 331Ch, bit0) = 0 before turning OFF DVDD, when DVDD is turned off with keeping IOVDD on.

- $VM \leq DVDD + 0.5 \text{ V}$ (TBD)
- SDA, SCL tolerate 3 V input at the time of power off.
- The data in the EEPROM may be rewritten unintentionally if you do not keep specifications. And it

- is forbidden to power off during EEPROM access. The data in EEPROM may be rewritten unintentionally.
- OIS driver and AF driver are recommended to set standby before VM power off.

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2-wire Serial Interface Timing

The communication protocol is compatible with I2C (Fast mode Plus).

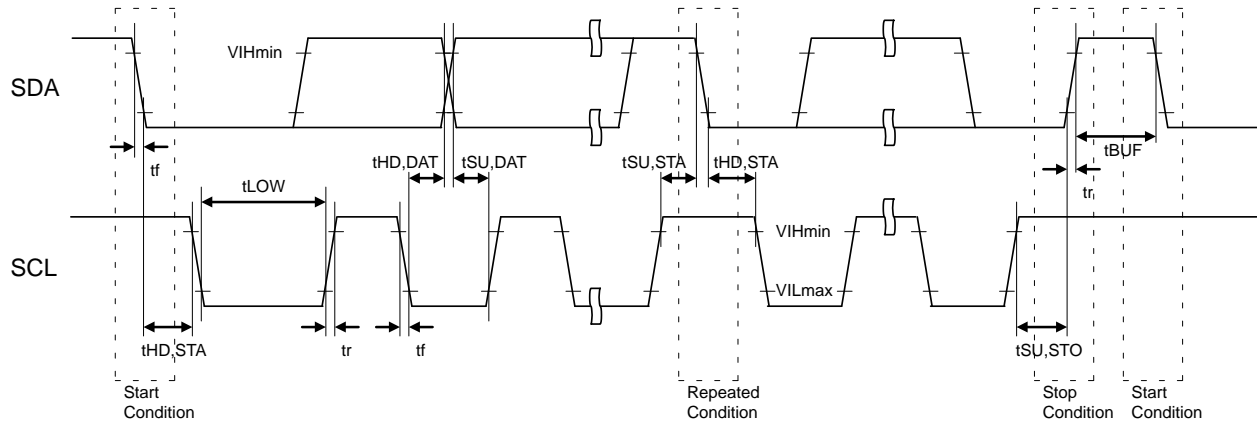


Figure 5.

Table 9.

Item	Symbol	Pin Name	Min	Typ	Max	Units
SCL clock frequency	Fscl	SCL			1000	KHz
START condition hold time	tHD,STA	SCL SDA	0.26			us
SCL clock Low period	tLOW	SCL	0.5			us
SCL clock High period	tHIGH	SCL	0.26			us
Setup time for repetition START condition	tSU,STA	SCL SDA	0.26			us
Data hold time	tHD,DAT	SCL SDA	0 (Note 1)		0.9	us
Data setup time	tSU,DAT	SCL SDA	50			ns
SDA, SCL rising time	tr	SCL SDA			120	ns
SDA, SCL falling time	tf	SCL SDA			120	ns
STOP condition setup time	tSU,STO	SCL SDA	0.26			us
Bus free time between STOP and START	tBUF	SCL SDA	0.5			us

1. Although the I2C specification defines a condition that 300 ns of hold time is required internally, This LSI is designed for a condition with typ. 40 ns of hold time. If SDA signal is unstable around falling point of SCL signal, please implement an appropriate treatment on board, such as inserting a resistor.

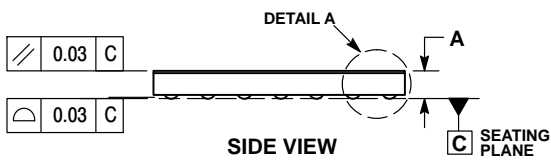
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PACKAGE DIMENSIONS

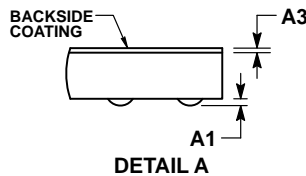
WLCSP21 1.17x2.77x0.30
CASE 567UJ
ISSUE O



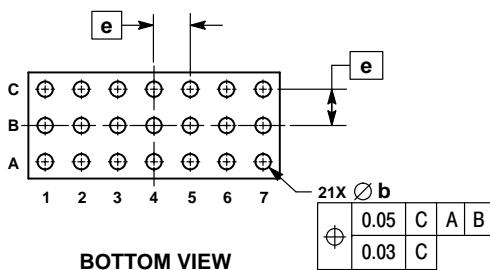
TOP VIEW



SIDE VIEW



DETAIL A



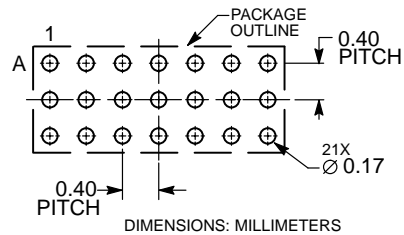
BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF CONTACT BALLS.
4. COPLANARITY APPLIES TO SPHERICAL CROWNS OF CONTACT BALLS.
5. DIMENSION b IS MEASURED AT THE MAXIMUM CONTACT BALL DIAMETER PARALLEL TO DATUM C.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.27	0.30	0.33
A1	0.04 REF		
A3	0.025 REF		
b	0.12	0.17	0.22
D	1.12	1.17	1.22
E	2.72	2.77	2.82
e	0.40 BSC		

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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