

**UNIDIRECTIONAL ESD PROTECTION DIODE**

STAND-OFF VOLTAGE - **5.0 Volts**  
POWER DISSIPATION - **25 WATTS**

**GENERAL DESCRIPTION**

- The L02ESD5V0D6-5 is a low capacitance 5-fold ESD protection diode array in SOT363 package.

**FEATURES**

- Uni-directional ESD protection of five lines.
- Bi-directional ESD protection of up four lines.
- Max.peak pulse power : Ppp = 25W at tp = 8/20 us
- ESD protection > 20 KV
- IEC 61000-4-2, level 4 ( ESD ), > 15KV ( air ) ; > 8KV ( contact ).
- IEC 61000-4-5 ( surge ); Ipp = 2.5A at tp = 8/20 us.
- Low clamping voltage; Vcl < 12V at Ipp = 2.5A
- Low capacitance device.

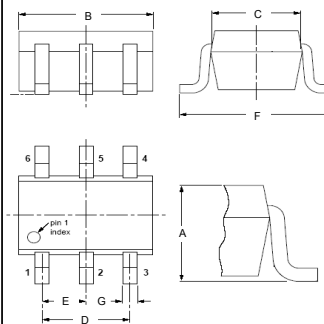
**APPLICATION**

- Computers and peripherals.
- Communication system.
- Cellular handsets and accessories.
- Audio & video equipment.

**MECHANICAL DATA**

- Case Material: "Green" molding compound UL flammability classification 94V-0 (No Br.Sb, Cl)
- Terminals: Lead Free Plating (Matte Tin Finish)
- Component in accordance to RoHs 2002/95/EC

**SOT363**

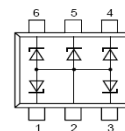
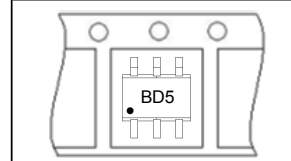


SOT363		
DIM.	MIN.	MAX.
A	0.80	1.10
B	1.80	2.20
C	1.15	1.40
D	1.30 (Typ.)	
E	0.65 (Typ.)	
F	2.00	2.45
G	0.15	0.35

All Dimensions in millimeter

PIN ASSIGNMENT	
1	Cathode 1
2	Common Anode
3	Cathode 2
4	Cathode 3
5	Cathode 4
6	Cathode 5

**Marking & Orientation**



**MAXIMUM RATINGS (Tj= 25°C unless otherwise noticed)**

Rating	Symbol	Value	Unit
Peak pulse Power ( 8/20us Waveform ) , Notes (1,2)	PPPM	25	W
Operating Junction Temperature Range	TJ	-55 to + 150	°C
Storage Temperature Range	Tstg	-55 to + 150	°C
Soldering Temperature, t max = 10s	TL	260	°C

**ELECTRICAL CHARACTERISTICS (Tj= 25°C unless otherwise noticed)**

Parameter	Symbol	Conditions	Min	Max	Unit
Reverse standoff voltage	VDRM	---	---	5.0	V
Reverse leakage current	IRM	VDRM = 5 V	---	25	nA
Breakdown voltage	VBR	IR = 1 mA	6.4	7.2	V
Diode capacitance	CJ	VR = 0 V , f = 1MHz	---	19	pF
Clamping voltage	VCL	Ipp = 1A	---	10	V
Clamping voltage	VCL	Ipp = 2.5A	---	12	V

- NOTE:**1. Non-repetitive current pulse 8/20 us exponentially decaying waveform.  
2. Measured from any of pins 1,3,4,5 or 6 to pin2.

REV. 3, Oct-2010, KSIR11

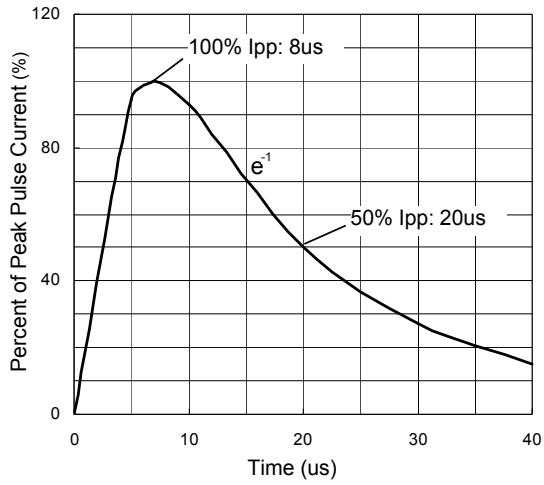


Figure 1. 8/20 us pulse waveform according to IEC 61000-4-5

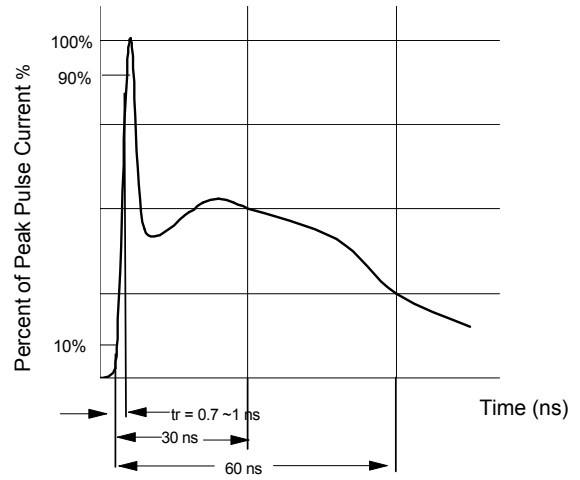


Figure 2. ESD pulse waveform according to IEC 61000-4-2

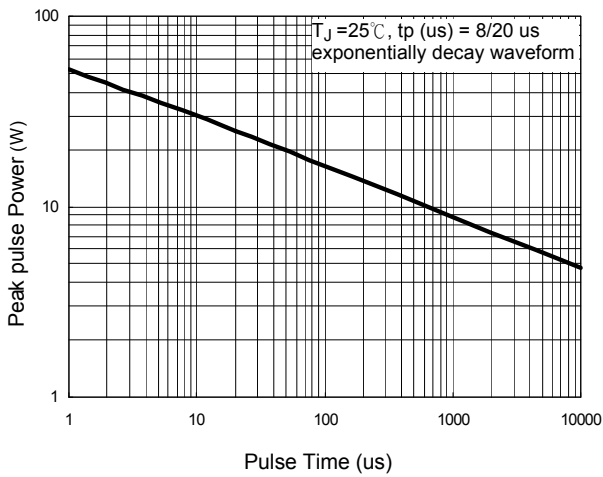


Figure 3. Power Dissipation versus Pulse Time

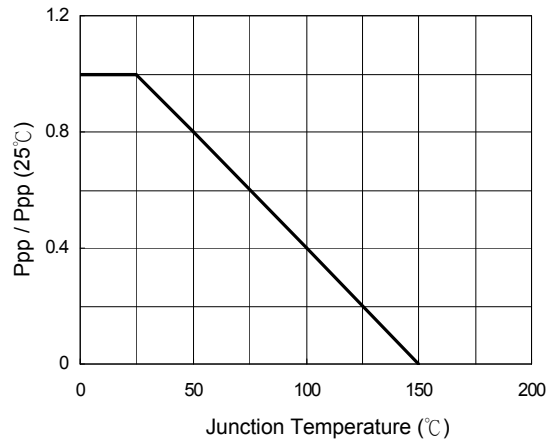


Figure 4. Peak pulse power versus  $T_J$

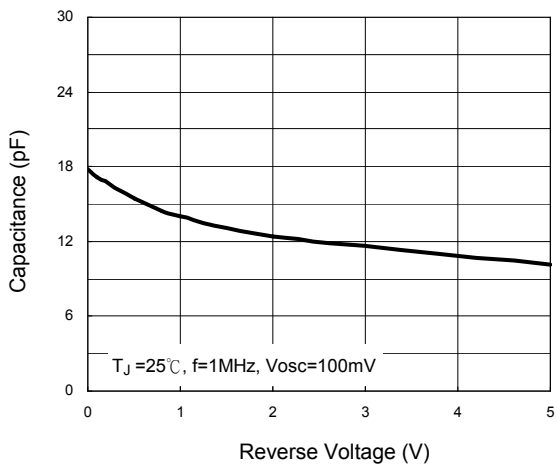


Figure 5. Typical Junction Capacitance

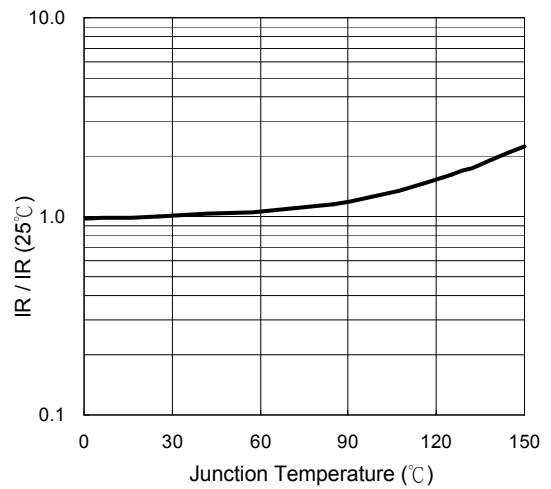


Figure 6. Reverse Leakage Current versus  $T_J$

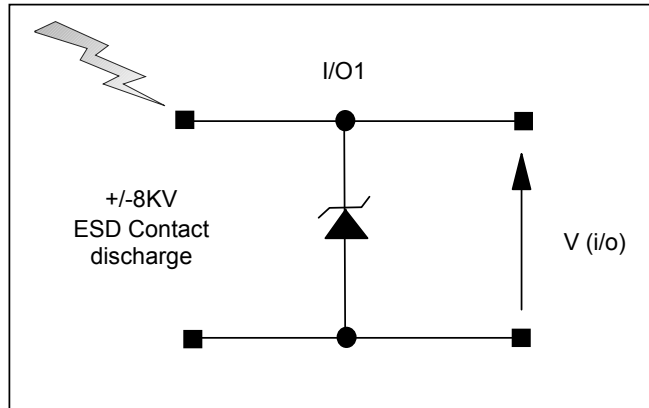


Figure 7. ESD Test Configuration

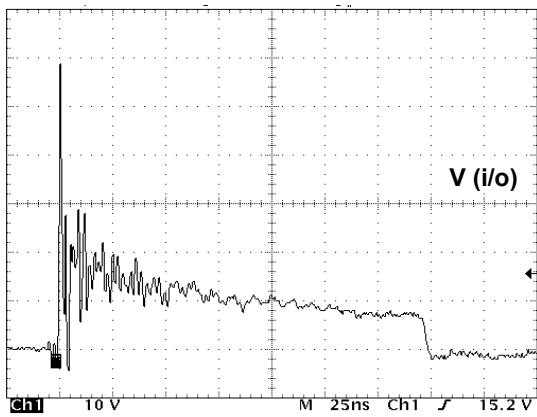


Figure 8. Clamped +8 kV ESD voltage waveform

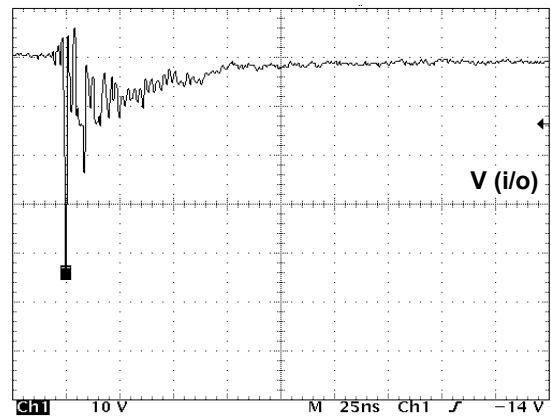


Figure 9. Clamped -8 kV ESD voltage waveform

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