

Integrated 5-Port 10/100 Managed Switch

Description

The KSZ8895MLU is a highly-integrated Layer 2-managed 5-port switch with an optimized design and plentiful features. It is designed for cost-sensitive 10/100Mbps 5-port switch systems with on-chip termination, lowest power consumption and internal core power controller. These features will save more system cost. It has 1.4Gbps high-performance memory bandwidth, shared memory based switch fabric with full non-blocking configuration. It also provides an extensive feature set such as power management, programmable rate limit and priority ratio, tag/port-based VLAN, packets filtering, quality of service (QoS) four-queues prioritization, management interface, and MIB counters. The SW5-MII interface can be connected to a processor with a MAC MII interface or external PHY with a PHY MII Interface.

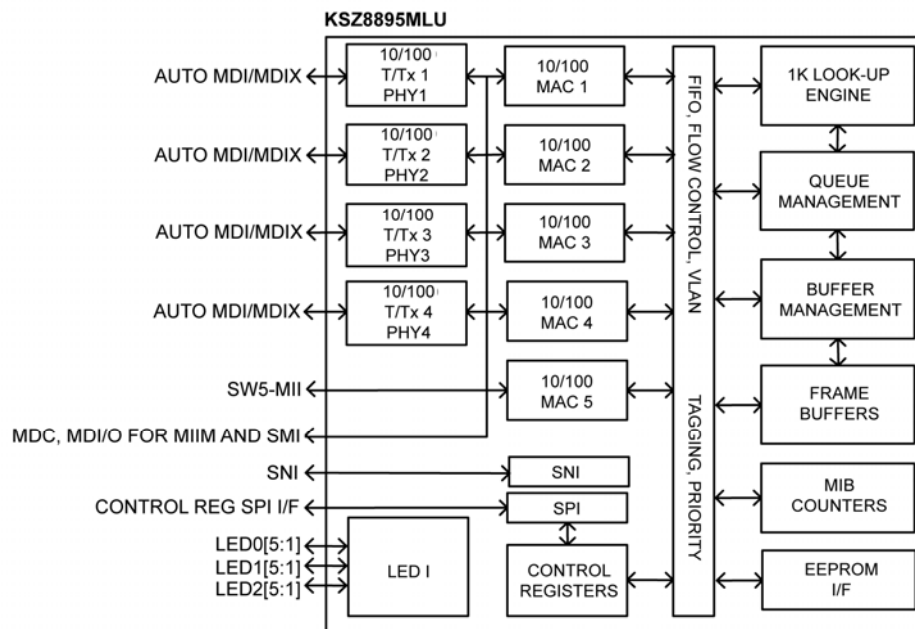
The KSZ8895MLU provides multiple CPU control/data interfaces to effectively address both current and emerging fast Ethernet applications.

The KSZ8895MLU consists of 10/100 PHYs with patented and enhanced mixed-signal technology, media access control (MAC) units, a high-speed non-blocking switch fabric, a dedicated address lookup engine, and an on-chip frame buffer memory. The KSZ8895MLU contains five MACs and four integrated PHYs. All PHYs support 10/100Base-T/TX.

All registers of MACs and PHYs units can be managed by the SPI interface or the SMI interface. MIIM registers of the PHYs can be accessed through the MDC/MDIO interface. EEPROM can set all control registers for the unmanaged mode.

Datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Functional Diagram



Features	Benefits
AEC-Q100 qualified.	Enables low power and power efficient design for next generation automotive multi-media networks.
Fully-compliant to IEEE 802.3/802.3u Standard.	Standard compliance ensures to work with other standard compliant, already deployed devices.
Single 3.3V supply with internal 1.2V LDO controller, and optional 3.3V, 2.5V or 1.8V VDDIO.	Enables low-power design and offers flexibility in design.
Integration of termination resistors on the chip.	On-chip termination (eliminating 4 external resistors/transceiver) not only simplifies PCB design and reduces system BOM, but also improves overall signal integrity and EMI emission.
Energy Detect Power Down when the cable is not plugged; and power down/ slow oscillator mode when the device is not in use.	Power consumption is optimized based on the status of the link or the device.
Rapid spanning tree (RSTP) support.	Provides faster spanning tree convergence after network topology change (< 6 sec vs. 30 – 50 sec for STP).
2K Byte maximum packet size.	Improves the efficiency of bulk data transfer, and system performance.
HP Auto MDI/MDIX crossover support.	Auto-MDI/MDIX eliminates the need for cross-over cable, thus reduces installation costs. Easy to use.

Applications

- Automotive Head Unit
- In Vehicle Gateway

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