128Kx8 Bit Low Voltage Operating Static RAM

FEATURES

- Fast Access Time : 70,100ns(max.)
- Low Power Dissipation
  Standby(CMOS) : 132μW(max.)L-Version
  : 33μW(max.)LL-Version
  Operating : 132mW(max.)
- Single 2.7V ~ 3.3V Power Supply
- TTL compatible inputs and outputs
- Fully Static Operation
  -No clock or refresh required
- Three State Output
- Battery Back-up Operation
  -2V(min.) Data Retention
- Standard Pin Configuration
  KM68U1000BLG/BLG-L: 32 pin-SOP (525mil)
  KM68U1000BLT/BLT-L : 32 pin-TSOP (Standard Type)
  KM68U1000BLR/BLR-L: 32 pin-TSOP (Reverse Type)

GENERAL DESCRIPTION

The KM68U1000BL/BL-L is a 1,048,576-bit high speed Static Random Access Memory organized as 131,072 words by 8 bits.
The device is fabricated using Samsung's advanced CMOS process.
The KM68U1000BL/BL-L has an output enable input for precise control of the data outputs.
It also has chip enable inputs for the minimum current power down mode.
The KM68U1000BL/BL-L has been designed for high speed and low power applications.
It is particularly well suited for low voltage(2.7 ~ 3.3V) operation and battery back-up application.

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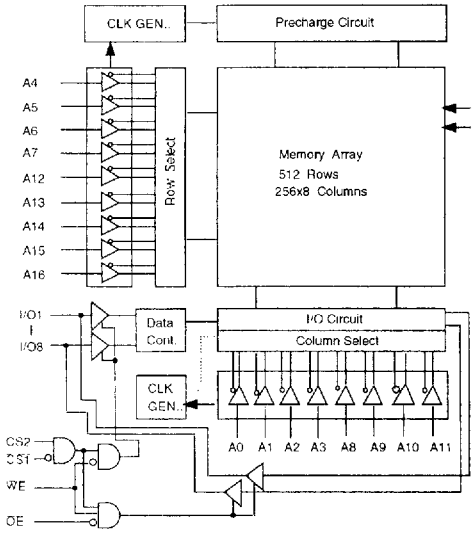
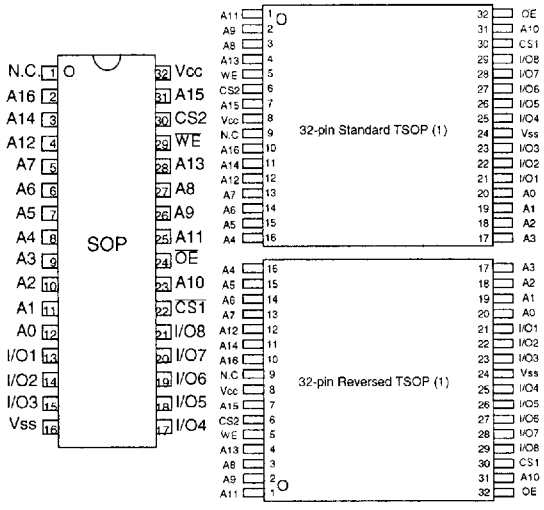
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(TOP VIEW)*



Pin Name	Pin Function
A_0-A_{16}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS1}$, CS2	Chip Select Input
$\overline{OE}$	Output Enable Input
I/O_1~I/O_8	Data Inputs/Outputs
V_{CC}	Power(2.7 ~ 3.3V)
V_{SS}	Ground
N.C	No Connection

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5 to Vcc+0.5	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 4.6	V
Power Dissipation	P_D	0.7	W
Storage Temperature	Tstg	-55 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A= 0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	2.7	3.0	3.3	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	Vcc+0.3	V
Input Low Voltage	V_{IL}	-0.3*	-	0.4	V

* V_{IL}(Min.)= -3.0V for ≤50 ns Pulse

DC AND OPERATING CHARACTERISTICS

(T_A= 0 to 70°C, Vcc=2.7 ~ 3.3V, unless otherwise specified)

Item	Symbol	Test Condition		Min.	* Typ	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc		-1	-	1	μA
Output Leakage Current	I_{LO}	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{WE}$=V_{IL}, $V_{I/O}$=Vss to Vcc		-1	-	1	μA
Operating Power Supply Current	I_{CC}	$\overline{CS1}$=V_{IL}, CS2= V_{IH} V_{IN}=V_{IL} or V_{IH}, $I_{I/O}$=0mA		-	2	5	mA
Average Operating Current	I_{CC1}	Cycle Time=1μs, 100% Duty, $\overline{CS1}$≤0.2V, CS2≥Vcc-0.2V, $I_{I/O}$=0mA		-	3	5	mA
	I_{CC2}	Min. Cycle, 100% Duty $\overline{CS1}$=V_{IL}, CS2=V_{IH}, $I_{I/O}$=0mA		-	30	40	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1}$=V_{IH} or CS2=V_{IL}		-	-	0.3	mA
	I_{SB1}	$\overline{CS1}$≥Vcc-0.2V	L	-	1	50	μA
		CS2≥Vcc-0.2V or CS2≤0.2V	L - L	-	0.5	15	μA
Output Low Voltage	V_{OL}	Iol=2.1 mA		-	-	0.4	V
Output High Voltage	V_{OH}	Ioh=-1.0 mA		2.2	-	-	V

* Typ; Vcc=3.0V, Ta=25°C

CAPACITANCE * (f=1MHz, T_A=25 °C)

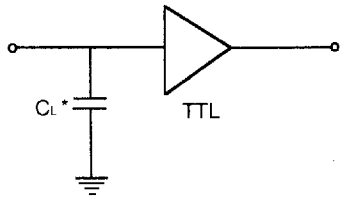
Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

* Note: Capacitance is sampled and not 100% tested.

TEST CONDITIONS

(T_A= 0 to 70°C, V_{CC}=2.7 ~ 3.3V, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0.4 to2.2V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L=100pF+1TTL Load



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM68U1000BL-7 KM68U1000BL-7L		KM68U1000BL-10 KM68U1000BL-10L		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	70		100	-	ns
Address Access Time	t_{AA}	-	70	-	100	ns
Chip Select to Output	t_{CO1}, t_{CO2}	-	70	-	100	ns
Output Enable to Valid Output	t_{OE}	-	35	-	50	ns
Chip Select to Low-Z Output	t_{LZ1}, t_{LZ2}	10	-	10	-	ns
Output Enable to Low-Z Output	t_{OLZ}	5	-	5	-	ns
Chip Disable to High-Z Output	t_{HZ1}, t_{HZ2}	0	25	0	30	ns
Output Disable to High-Z Output	t_{OHZ}	0	25	0	30	ns
Output Hold from Address Change	t_{OH}	10	-	15	-	ns

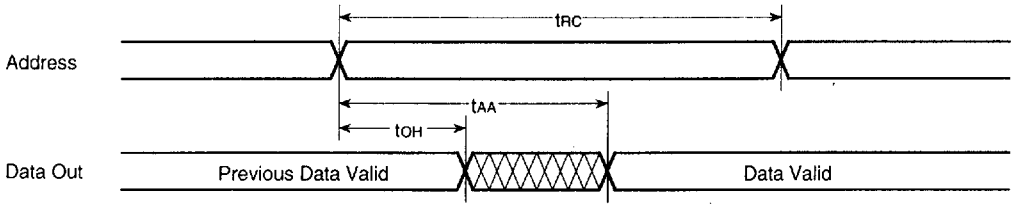
WRITE CYCLE

Farameter	Symbol	KM68U1000BL-7 KM68U1000BL-7L		KM68U1000BL-10 KM68U1000BL-10L		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	tWC	70	-	100	-	ns
Chip Select to End of Write	tCW	60	-	80	-	ns
Address Set-up Time	tAS	0	-	0	-	ns
Address Valid to End of Write	tAW	60	-	80	-	ns
Write Pulse Width	tWP	55	-	70	-	ns
Write Recovery Time	tWR	0		0	-	ns
Write to Output High-Z	tWHZ	0	25	0	30	ns
Data to Write Time Overlap	tDW	30	-	40	-	ns
Data Hold from Write Time	tDH	0	-	0	-	ns
End Write to Output Low-Z	tOW	5	-	5	-	ns

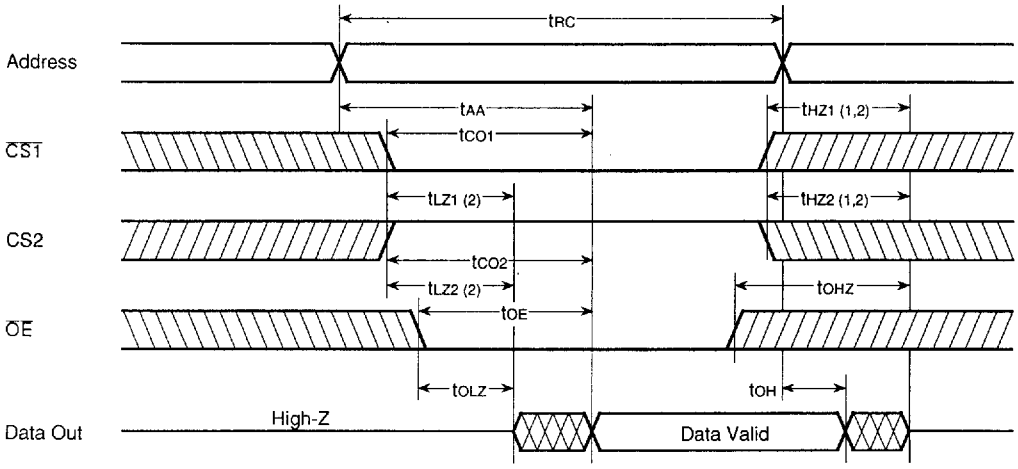
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

($\overline{CS1}$=$\overline{OE}$=VIL, CS2=$\overline{WE}$=VIH)



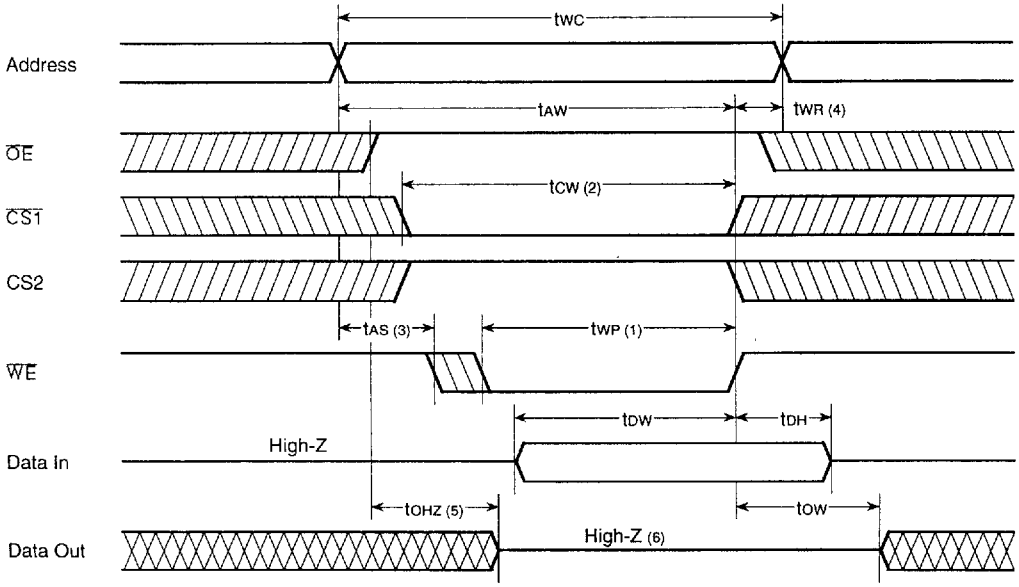
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



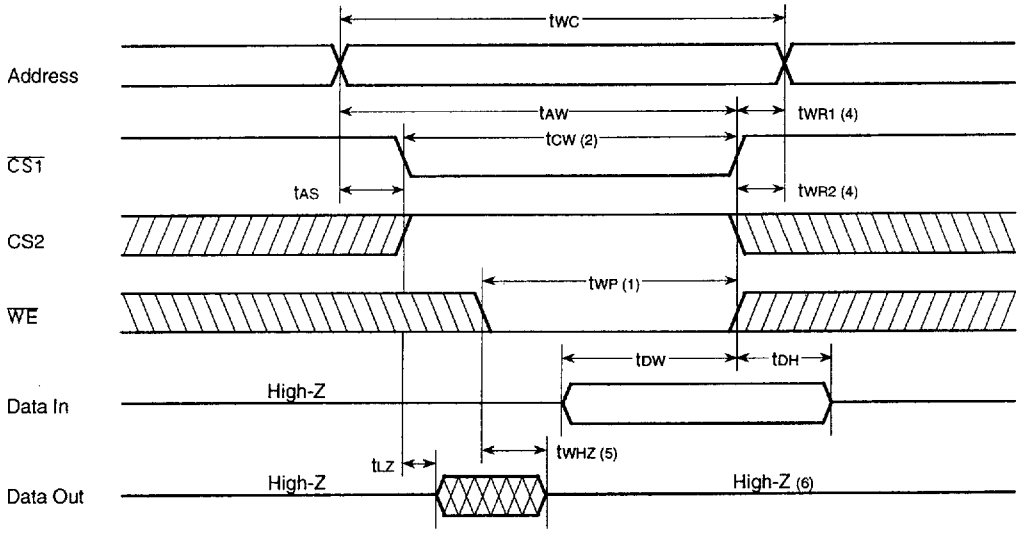
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are referenced to the V_{OH} or V_{OL}.
2. At any given temperature and voltage condition t_{HZ}(max) is less than t_{LZ}(min) both for a given device and from device to device.
3. $\overline{WE}$ is high for read cycle.

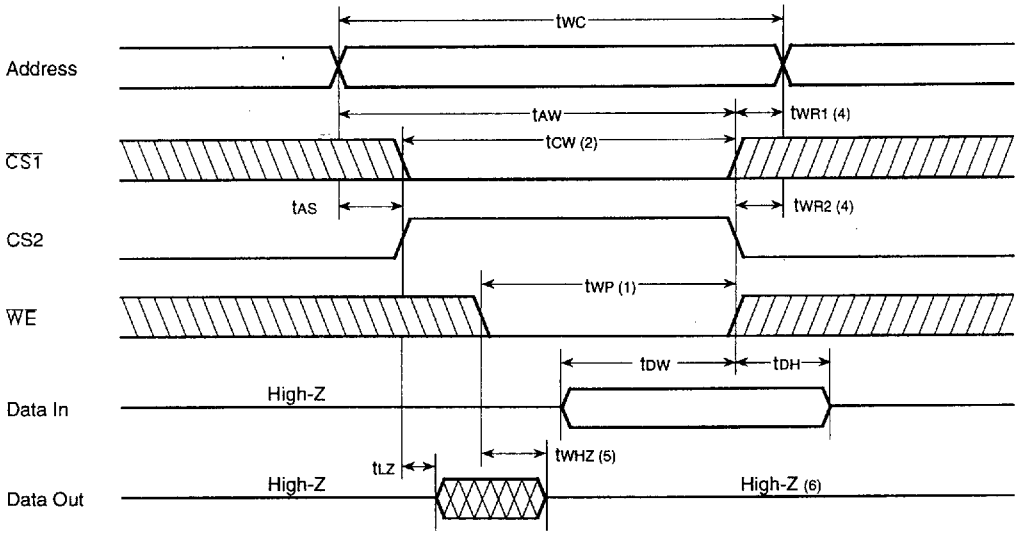
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS2 Controlled)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured form the end of write to the address change. t_{WR1} applied in case a write ends at $\overline{CS1}$, or $\overline{WE}$ going high, t_{WR2} applied in case a write ends at CS2 going to low.
5. If $\overline{OE}$, CS2 and $\overline{WE}$ are in the read mode during in this period, the I/O pins are in the Low-Z state, inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.

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FUNCTIONAL DESCRIPTION

$\overline{CS}$	CS2	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Vcc Current
H	X	X	X	Power down	High-Z	I_{SB}, I_{SB1}
X	L	X	X	Power down	High-Z	I_{SB},I_{SB1}
L	H	H	H	Output Disable	High-Z	I_{CC}
L	H	H	L	Read	D_{OUT}	I_{CC}
L	H	L	X	Write	D_{IN}	I_{CC}

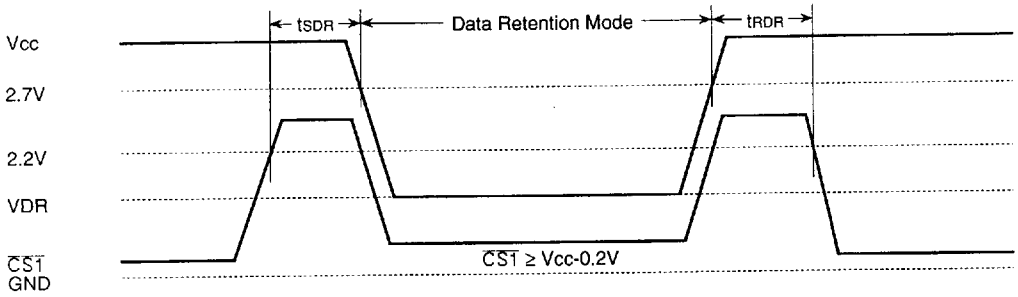
Note : X means Don't Care.

DATA RETENTION CHARACTERISTICS (Ta= 0 to 70°C)

PARAMETER	SYMBOL	TEST CONDITION		MIN	Typ	MAX	UNIT
Vcc for Data Retention	Vdr	(1)$\overline{CS1}$≥Vcc-0.2V		2.0		3.3	V
Data Retention Current	Idr	Vcc=3.0V	L		1.0	40(2)	µA
		$\overline{CS1}$≥VCC-0.2V	LL		0.5	10(3)	µA
Data Retention Set-up Time	tSDR	See Data Retention		0			ns
Recovery Time	tRDR	Waveforms (below)		5			ms

(1) $\overline{CS1}$≥Vcc-0.2,CS2≥VCC-0.2($\overline{CS1}$ Controlled) or CS2≤0.2(CS2 Controlled)
(2) 20 µA (max.) at 0 °C to 40 °C
(3) 3 µA (max.) at 0 °C to 40 °C

DATA RETENTION WAVEFORM 1 ($\overline{CS1}$ Controlled)



DATA RETENTION WAVEFORM 2 (CS2 Controlled)