

Document Title

**256Kx16 Bit High Speed Static RAM(3.3V Operating).
Operated at Commercial and Industrial Temperature Ranges.**

Revision History

<u>Rev No.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>
Rev. 0.0	Initial release with Preliminary.	Aug. 20. 2001	Preliminary
Rev. 0.1	Add Low Ver.	Sep. 19. 2001	Preliminary
Rev. 0.2	Package dimensions modify on page 11.	Sep. 28. 2001	Preliminary
Rev. 0.3	Change ICC , ISB, ISB1	Oct. 09. 2001	Preliminary

Item		Previous	Current
ICC(Commercial)	8ns	110mA	80mA
	10ns	90mA	65mA
	12ns	80mA	55mA
	15ns	70mA	45mA
ICC(Industrial)	8ns	130mA	100mA
	10ns	115mA	85mA
	12ns	100mA	75mA
	15ns	85mA	65mA
ISB		30mA	20mA
ISB1(L-ver.)		0.5mA	1.2mA

Rev. 0.4	1. Correct AC parameters : Read & Write Cycle 2. Change Data Retention Current : from 0.45mA to 1.1mA when Vcc=3.0V from 0.35mA to 0.9mA when Vcc=2.0V 3. Limit L-Ver. to 48 TBGA Package	Nov.23. 2001	Preliminary
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Rev. 1.0	1. Delete 12ns,15ns speed bin. 2. Change Icc for Industrial mode.	Dec.18. 2001	Final
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Item		Previous	Current
ICC(Industrial)	8ns	100mA	90mA
	10ns	85mA	75mA

Rev. 2.0	1. Add tBA,tBLZ,tBHZ,tBW AC parematers.	Feb. 14. 2002	Final
Rev. 2.1	1. Correct the Package dimensions(48-TBGA)	Oct. 23. 2002	Final
Rev. 2.2	1. Add the tPU and tPD into the waveform.	Mar. 10, 2003	Final

The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.

4Mb Async. Fast SRAM Ordering Information

Org.	Part Number	VDD(V)	Speed (ns)	PKG	Temp. & Power
1M x4	K6R4004C1D-JC(I) 10	5	10	J : 32-SOJ	C : Commercial Temperature ,Normal Power Range I : Industrial Temperature ,Normal Power Range L : Commercial Temperature ,Low Power Range P : Industrial Temperature ,Low Power Range
	K6R4004V1D-JC(I) 08/10	3.3	8/10		
512K x8	K6R4008C1D-J(T)C(I) 10	5	10	J : 36-SOJ	
	K6R4008V1D-J(T)C(I) 08/10	3.3	8/10	T : 44-TSOP2	
256K x16	K6R4016C1D-J(T,E)C(I) 10	5	10	J : 44-SOJ	
	K6R4016V1D-J(T,E)C(I,L,P) 08/10	3.3	8/10	T : 44-TSOP2 E : 48-TBGA	

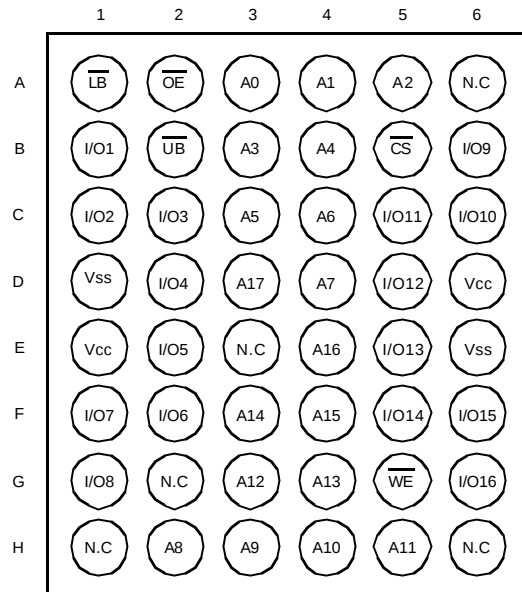
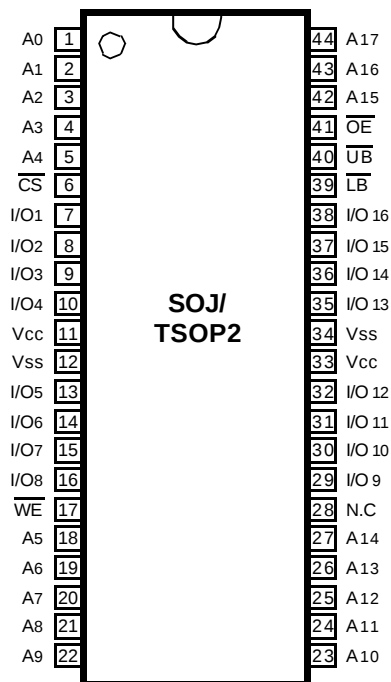
FEATURES

- ## GENERAL DESCRIPTION

The K6R4016V1D is a 4,194,304-bit high-speed Static Random Access Memory organized as 262,144 words by 16 bits. The K6R4016V1D uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control (UB, LB). The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The K6R4016V1D is packaged in a 400mil 44-pin plastic SOJ or TSOP(II) forward or 48 TBGA.

The block diagram illustrates the architecture of the 1024 Rows 256 x 16 Columns Memory Array. The central component is the **Memory Array**, which is 1024 Rows by 256 x 16 Columns. It is connected to a **Pre-Charge Circuit** and a **Row Select** circuit. The **Row Select** circuit is driven by address lines A_0 through A_9 . The **Memory Array** is also connected to a **Data Cont.** (Data Controller) and a **Gen. CLK** (General Clock) circuit. The **Data Cont.** is connected to the **I/O Circuit & Column Select** circuit, which is driven by address lines A_{10} through A_{17} . The **I/O Circuit & Column Select** circuit is connected to the **I/O₁~I/O₈** and **I/O₉~I/O₁₆** ports. The **Gen. CLK** circuit is connected to the **I/O Circuit & Column Select** circuit. The **WE** (Write Enable) and **OE** (Output Enable) signals are connected to the **I/O Circuit & Column Select** circuit. The **UB** (Upper Bank) and **LB** (Lower Bank) signals are connected to the **I/O Circuit & Column Select** circuit. The **CS** (Chip Select) signal is connected to the **I/O Circuit & Column Select** circuit.

PIN CONFIGURATION (Top View)



48-TBGA

PIN FUNCTION

Pin Name	Pin Function
A0 - A17	Address Inputs
WE	Write Enable
CS	Chip Select
OE	Output Enable
LB	Lower-byte Control(I/O1~I/O8)
UB	Upper-byte Control(I/O9~I/O16)
I/O1 ~ I/O16	Data Inputs/Outputs
Vcc	Power(+3.3V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		V _{IN} , V _{OUT}	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss		V _{CC}	-0.5 to 4.6	V
Power Dissipation		P _D	1.0	W
Storage Temperature		T _{STG}	-65 to 150	°C
Operating Temperature	Commercial	T _A	0 to 70	°C
	Industrial	T _A	-40 to 85	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*(T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	3.0	3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.0	-	V _{CC} +0.3***	V
Input Low Voltage	V _{IL}	-0.3**	-	0.8	V

* The above parameters are also guaranteed at industrial temperature range.

** V_{IL}(Min) = -2.0V a.c(Pulse Width ≤ 8ns) for I ≤ 20mA

*** V_{IH}(Max) = V_{CC} + 2.0V a.c (Pulse Width ≤ 8ns) for I ≤ 20mA.

DC AND OPERATING CHARACTERISTICS*(T_A=0 to 70°C, V_{CC}=3.3±0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions			Min	Max	Unit
Input Leakage Current	I _{LI}	V _{IN} =V _{SS} to V _{CC}			-2	2	μA
Output Leakage Current	I _{LO}	CS=V _{IH} or OE=V _{IH} or WE=V _{IL} V _{OUT} =V _{SS} to V _{CC}			-2	2	μA
Operating Current	I _{CC}	Min. Cycle, 100% Duty CS=V _{IL} , V _{IN} =V _{IH} or V _{IL} , I _{OUT} =0mA	Com.	8ns	-	80	mA
				10ns	-	65	
			Ind.	8ns	-	90	
				10ns	-	75	
Standby Current	ISB	Min. Cycle, CS=V _{IH}			-	20	mA
	ISB1	f=0MHz, CS≥V _{CC} -0.2V, V _{IN} ≥V _{CC} -0.2V or V _{IN} ≤0.2V	Normal		-	5	
			L-ver.		-	1.2	
Output Low Voltage Level	V _{OL}	I _{OL} =8mA			-	0.4	V
Output High Voltage Level	V _{OH}	I _{OH} =-4mA			2.4	-	V

* The above parameters are also guaranteed at industrial temperature range.

CAPACITANCE*(T_A=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	TYP	Max	Unit
Input/Output Capacitance	C _{I/O}	V _{I/O} =0V	-	8	pF
Input Capacitance	C _{IN}	V _{IN} =0V	-	6	pF

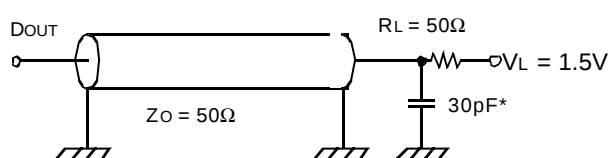
* Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS ($T_A=0$ to 70°C , $V_{CC}=3.3\pm0.3\text{V}$, unless otherwise noted.)**TEST CONDITIONS***

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

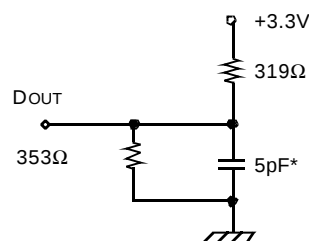
* The above test conditions are also applied at industrial temperature range.

Output Loads(A)



Output Loads(B)

for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Capacitive Load consists of all components of the test environment.

* Including Scope and Jig Capacitance

READ CYCLE*

Parameter	Symbol	K6R4016V1D-08		K6R4016V1D-10		Unit
		Min	Max	Min	Max	
Read Cycle Time	t _{RC}	8	-	10	-	ns
Address Access Time	t _{AA}	-	8	-	10	ns
Chip Select to Output	t _{CO}	-	8	-	10	ns
Output Enable to Valid Output	t _{OE}	-	4	-	5	ns
$\overline{\text{UB}}$, $\overline{\text{LB}}$ Access Time	t _{BA}	-	4	-	5	ns
Chip Enable to Low-Z Output	t _{LZ}	3	-	3	-	ns
Output Enable to Low-Z Output	t _{OLZ}	0	-	0	-	ns
$\overline{\text{UB}}$, $\overline{\text{LB}}$ Enable to Low-Z Output	t _{BLZ}	0	-	0	-	ns
Chip Disable to High-Z Output	t _{HZ}	0	4	0	5	ns
Output Disable to High-Z Output	t _{OHZ}	0	4	0	5	ns
$\overline{\text{UB}}$, $\overline{\text{LB}}$ Disable to High-Z Output	t _{BHZ}	0	4	0	5	ns
Output Hold from Address Change	t _{OH}	3	-	3	-	ns
Chip Selection to Power Up Time	t _{PU}	0	-	0	-	ns
Chip Selection to Power Down Time	t _{PD}	-	8	-	10	ns

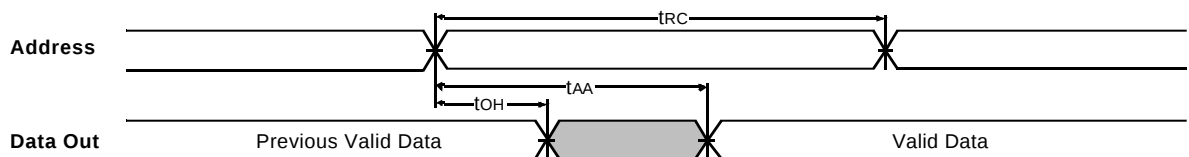
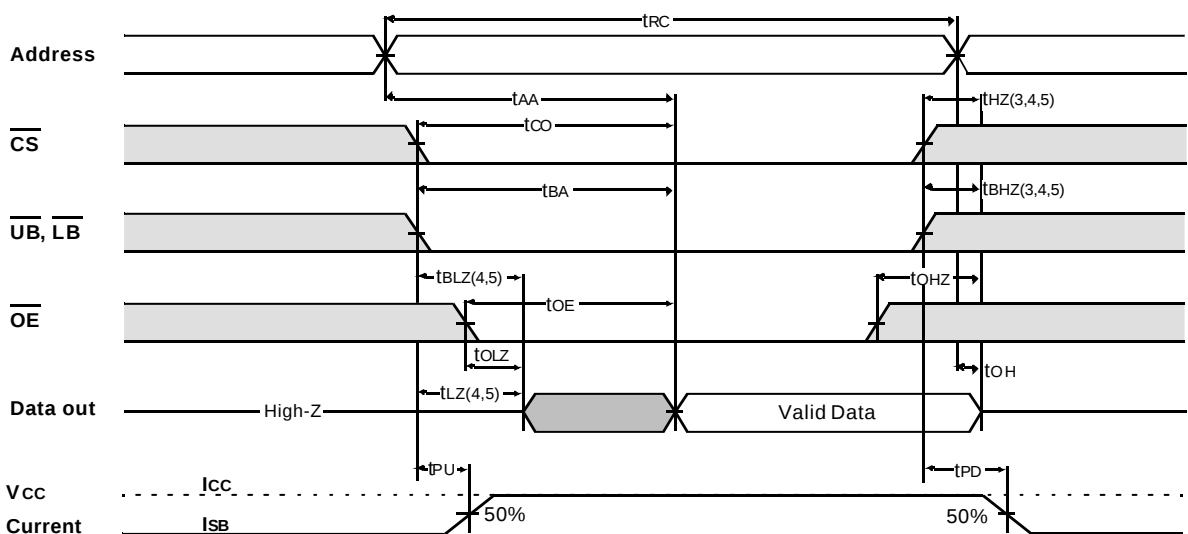
* The above parameters are also guaranteed at industrial temperature range.

WRITE CYCLE*

Parameter	Symbol	K6R4016V1D-08		K6R4016V1D-10		Unit
		Min	Max	Min	Max	
Write Cycle Time	t _{WC}	8	-	10	-	ns
Chip Select to End of Write	t _{CW}	6	-	7	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	ns
Address Valid to End of Write	t _{AW}	6	-	7	-	ns
Write Pulse Width($\overline{\text{OE}}$ High)	t _{WP}	6	-	7	-	ns
Write Pulse Width($\overline{\text{OE}}$ Low)	t _{WP1}	8	-	10	-	ns
$\overline{\text{UB}}$, $\overline{\text{LB}}$ Valid to End of Write	t _{BW}	6	-	7	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	ns
Write to Output High-Z	t _{WHZ}	0	4	0	5	ns
Data to Write Time Overlap	t _{DW}	4	-	5	-	ns
Data Hold from Write Time	t _{DH}	0	-	0	-	ns
End of Write to Output Low-Z	t _{OW}	3	-	3	-	ns

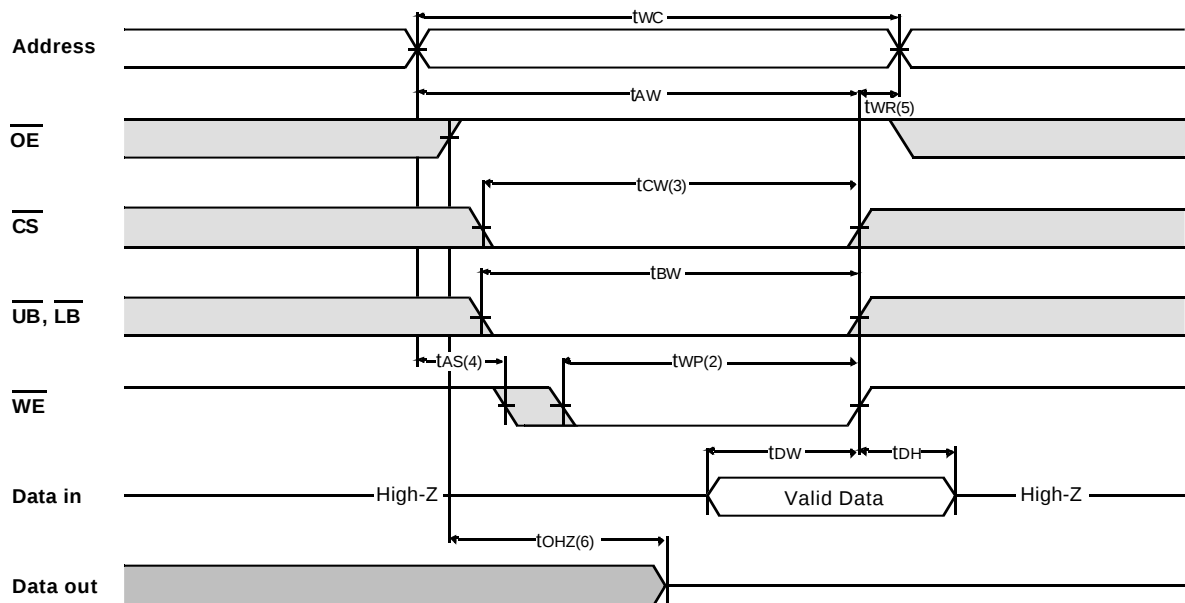
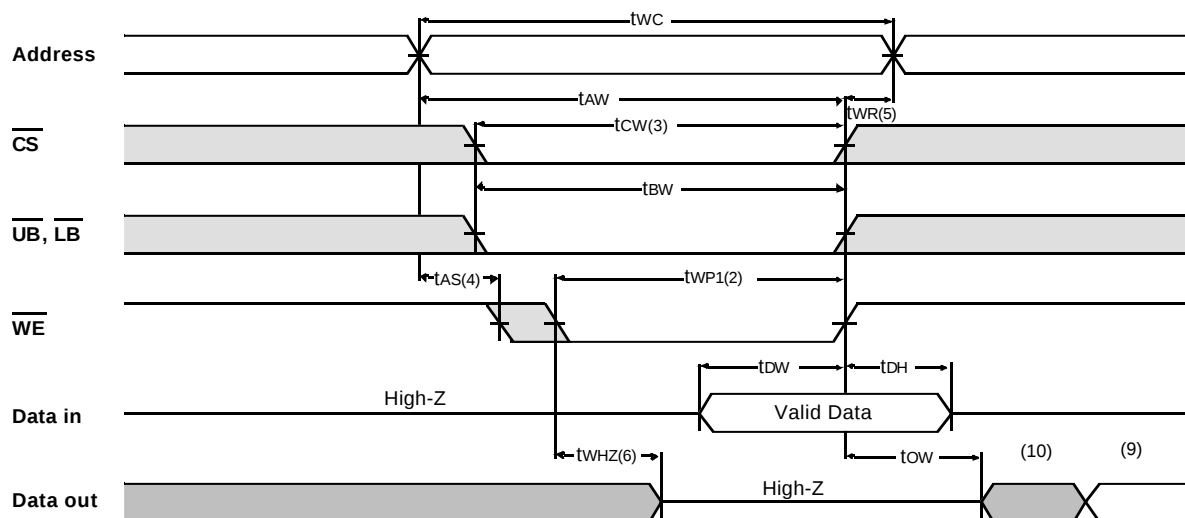
* The above parameters are also guaranteed at industrial temperature range.

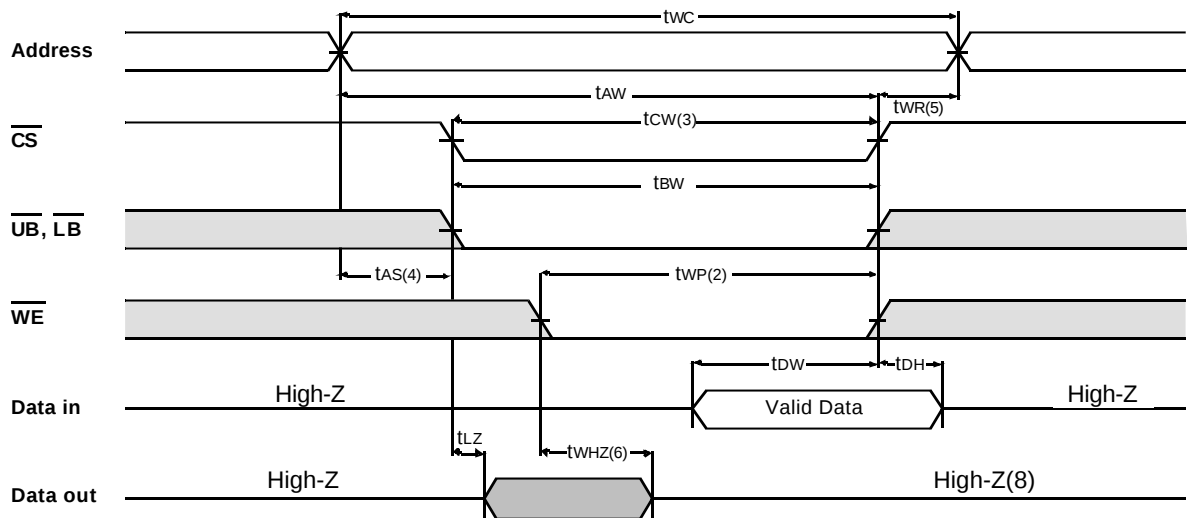
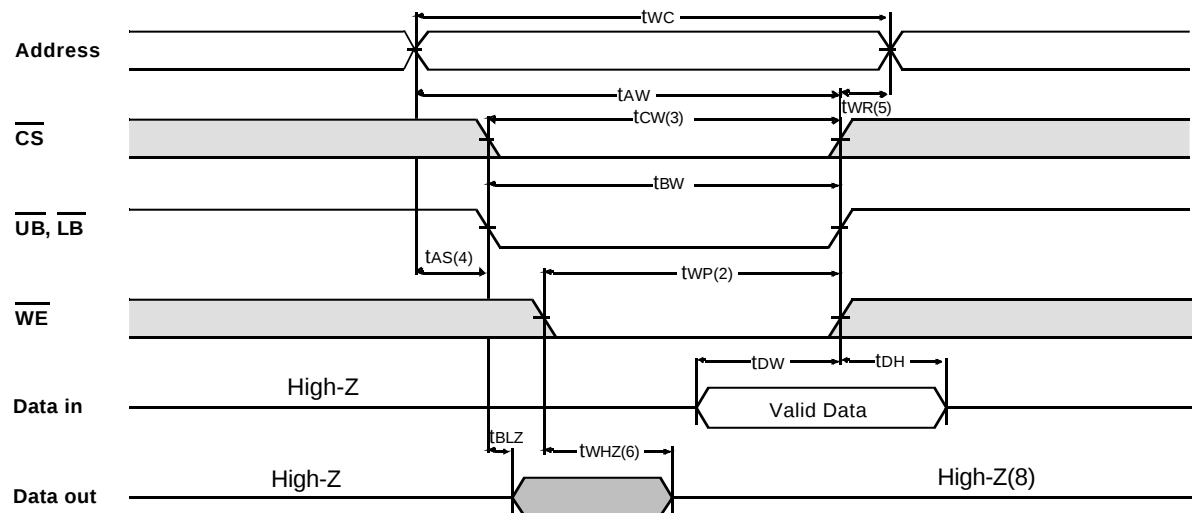
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{\text{CS}}=\overline{\text{OE}}=\text{V}_{\text{IL}}$, $\overline{\text{WE}}=\text{V}_{\text{IH}}$, $\overline{\text{UB}}$, $\overline{\text{LB}}=\text{V}_{\text{IL}}$)TIMING WAVEFORM OF READ CYCLE(2) ($\overline{\text{WE}}=\text{V}_{\text{IH}}$)

NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device.
5. Transition is measured $\pm 200\text{mV}$ from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS} = V_{IL}$.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}$ =Low fixed)

TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{CS}$ =Controlled)TIMING WAVEFORM OF WRITE CYCLE(4) ($\overline{UB}$, $\overline{LB}$ Controlled)

NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$, $\overline{WE}$, $\overline{LB}$ and $\overline{UB}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{\text{CS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{LB}}$	$\overline{\text{UB}}$	Mode	I/O Pin		Supply Current
						I/O1~I/O8	I/O9~I/O16	
H	X	X*	X	X	Not Select	High-Z	High-Z	ISB, ISB1
L	H	H	X	X	Output Disable	High-Z	High-Z	ICC
L	X	X	H	H		High-Z	High-Z	
L	H	L	L	H	Read	DOUT	High-Z	ICC
			H	L		High-Z	DOUT	
			L	L		DOUT	DOUT	
L	L	X	L	H	Write	DIN	High-Z	ICC
			H	L		High-Z	DIN	
			L	L		DIN	DIN	

* X means Don't Care.

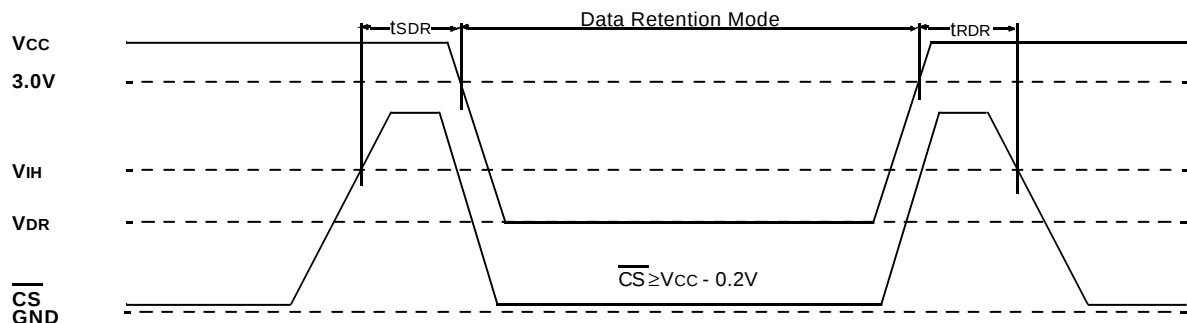
DATA RETENTION CHARACTERISTICS*(TA=0 to 70°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Vcc for Data Retention	VDR	$\overline{\text{CS}} \geq V_{\text{CC}} - 0.2\text{V}$	2.0	-	3.6	V
Data Retention Current	IDR	$V_{\text{CC}}=3.0\text{V}$, $\overline{\text{CS}} \geq V_{\text{CC}} - 0.2\text{V}$ $V_{\text{IN}} \geq V_{\text{CC}} - 0.2\text{V}$ or $V_{\text{IN}} \leq 0.2\text{V}$	-	-	1.1	mA
		$V_{\text{CC}}=2.0\text{V}$, $\overline{\text{CS}} \geq V_{\text{CC}} - 0.2\text{V}$ $V_{\text{IN}} \geq V_{\text{CC}} - 0.2\text{V}$ or $V_{\text{IN}} \leq 0.2\text{V}$	-	-	0.9	
Data Retention Set-Up Time	tSDR	See Data Retention Wave form(below)	0	-	-	ns
Recovery Time	tRDR		5	-	-	ms

* The above parameters are also guaranteed at industrial temperature range.
Data Retention Characteristic is for L-ver only.

DATA RETENTION WAVE FORM

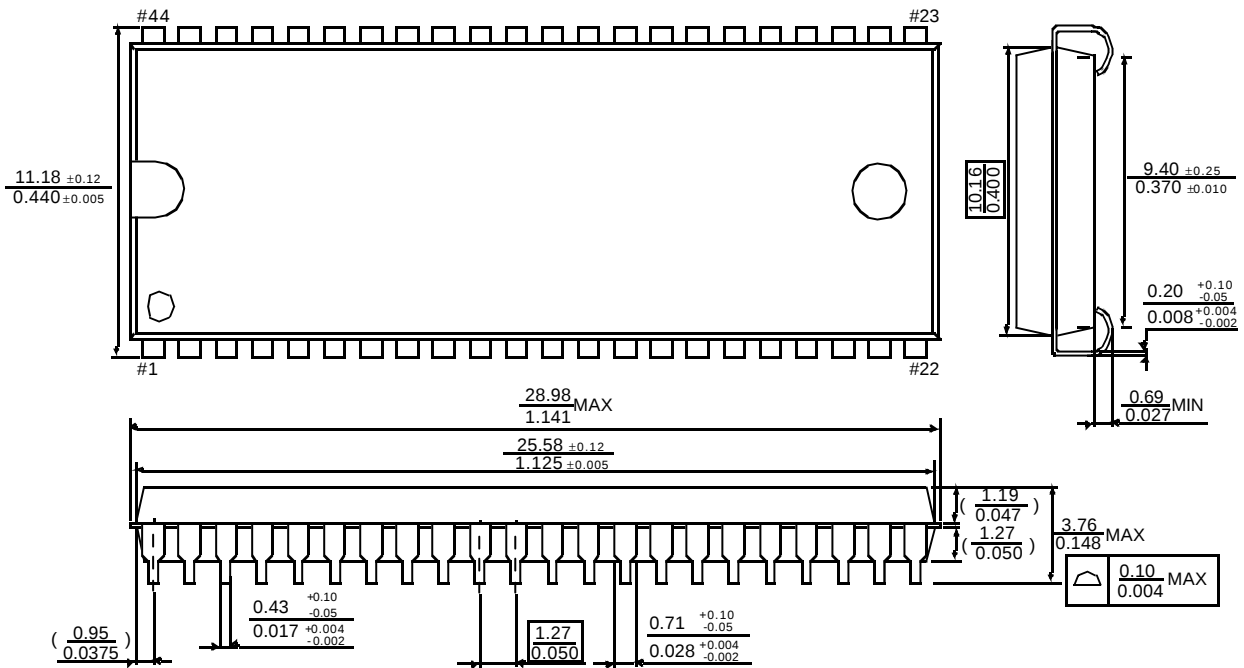
$\overline{\text{CS}}$ controlled



PACKAGE DIMENSIONS

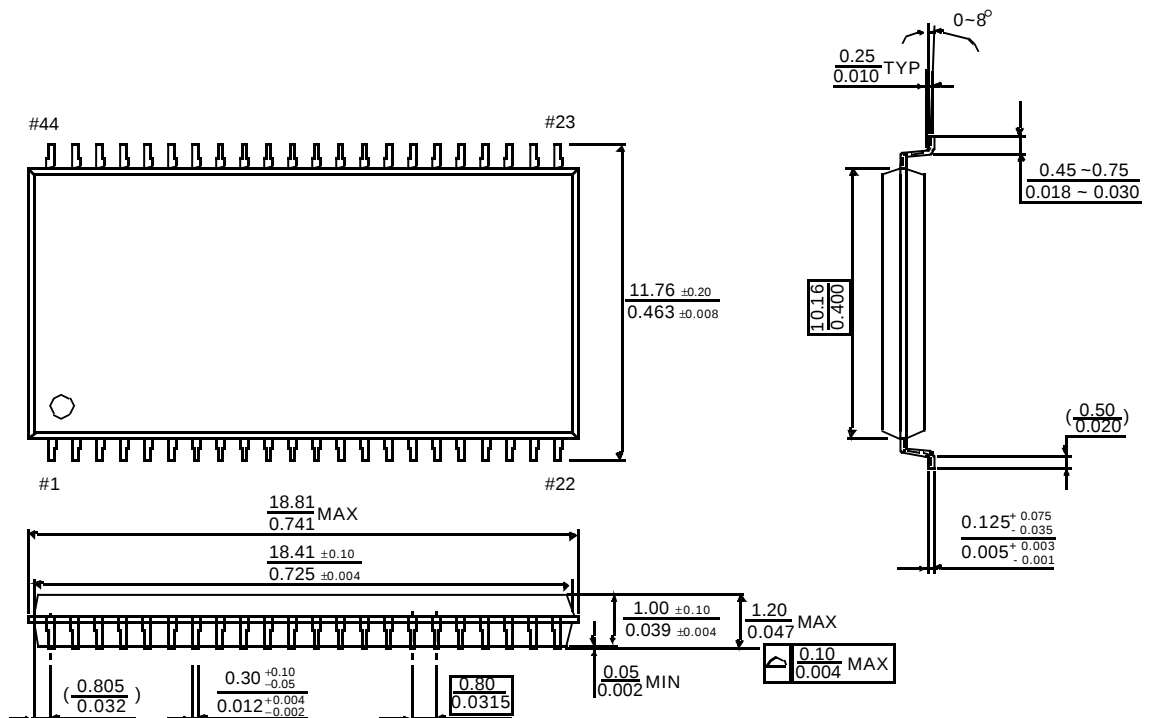
Units: millimeters/Inches

44-SOJ-400



44-TSOP2-400BF

Units: millimeters/Inches



PACKAGE DIMENSIONS

Units : millimeter.

