

## Low-Power Dual Channel Digital Isolator

Check for Samples: [ISO7420FCC](#)

### FEATURES

- Signaling Rate: 50 Mbps (5V Supplies)
- Output is Low in Default Mode
- Integrated Noise Filter on the Input pins
- Low Power Consumption: Typical  $I_{CC}$  per Channel
  - 1.8 mA at 1 Mbps, 3.9 mA at 25 Mbps (5V Supplies)
  - 1.4 mA at 1 Mbps, 2.6 mA at 25 Mbps (3.3V Supplies)
- Low Propagation Delay: 20 ns Typical (5V Supplies)
- Channel-to-Channel Output Skew: 2ns Maximum
- 3.3 V / 5 V Level Translation
- Wide  $T_A$  Range Specified:  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
- 60 KV/ $\mu\text{s}$  Transient Immunity, Typical (5V Supplies)
- Low Emissions
- Isolation Barrier Life: > 25 Years
- Operates from 2.7V to 5.5V Supply Levels
- Narrow Body SOIC-8 Package

### APPLICATIONS

- Opto-Coupler Replacement in:
  - Industrial FieldBus
    - ProfiBus
    - ModBus
    - DeviceNet™ Data Buses
  - Servo Control Interface
  - Motor Control
  - Power Supplies
  - Battery Packs

### SAFETY AND REGULATORY APPROVALS

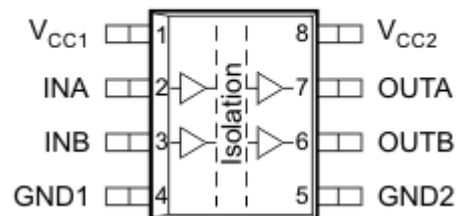
- 3 KV<sub>RMS</sub> / 4242 V<sub>PK</sub> Isolation per DIN EN 60747-5-5 (VDE 0884-5)
- 2.5 KV<sub>RMS</sub> Isolation for 1 minute per UL 1577
- CSA Component Acceptance Notice #5A
- IEC 60950-1 and IEC 61010-1 End Equipment Standards Approval
- GB4943.1-2011 CQC Certification (Approval Pending)

### DESCRIPTION

ISO7420FCC provides galvanic isolation up to 2500 V<sub>RMS</sub> for 1 minute per UL and 4242 V<sub>PK</sub> per VDE. This device has two isolated channels. Each channel has a logic input and output buffer separated by a silicon dioxide (SiO<sub>2</sub>) insulation barrier. Used in conjunction with isolated power supplies, this device prevents noise currents on a data bus or other circuit from entering the local ground and interfering with or damaging sensitive circuitry. The suffix F indicates low-output option in fail-safe conditions (see [Table 1](#)). This device has integrated noise filter for harsh environments where short noise pulses may be present at the device input pins.

These devices have TTL input thresholds and operate from 2.7V to 5.5V supplies. All inputs are 5V tolerant when supplied from a 2.7V or 3.3V supply.

**ISO7420  
D Package  
(Top View)**



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## PIN DESCRIPTIONS

| PIN       |            | I/O | DESCRIPTION                     |
|-----------|------------|-----|---------------------------------|
| NAME      | ISO7420FCC |     |                                 |
| INA       | 2          | I   | Input, channel A                |
| INB       | 3          | I   | Input, channel B                |
| GND1      | 4          | –   | Ground connection for $V_{CC1}$ |
| GND2      | 5          | –   | Ground connection for $V_{CC2}$ |
| OUTA      | 7          | O   | Output, channel A               |
| OUTB      | 6          | O   | Output, channel B               |
| $V_{CC1}$ | 1          | –   | Power supply, $V_{CC1}$         |
| $V_{CC2}$ | 8          | –   | Power supply, $V_{CC2}$         |

**Table 1. FUNCTION TABLE**

| INPUT SIDE<br>$V_{CC}$ | OUTPUT SIDE<br>$V_{CC}$ | INPUT<br>INA, INB | OUTPUT<br>OUTA, OUTB |
|------------------------|-------------------------|-------------------|----------------------|
| PU                     | PU                      | H                 | H                    |
|                        |                         | L                 | L                    |
|                        |                         | Open              | L <sup>(1)</sup>     |
| PD                     | PU                      | X                 | L <sup>(1)</sup>     |
| X                      | PD                      | X                 | Undetermined         |

(1) In fail-safe condition, output defaults to low level

## AVAILABLE OPTIONS

| PRODUCT    | DATA RATE | DEFAULT OUTPUT | INTEGRATED NOISE FILTER | RATED $T_A$    | CHANNEL DIRECTION | MARKED AS | ORDERING NUMBER     |
|------------|-----------|----------------|-------------------------|----------------|-------------------|-----------|---------------------|
| ISO7420FCC | 50 Mbps   | Low            | Yes                     | –40°C to 125°C | Same              | 7420FC    | ISO7420FCCD (rail)  |
|            |           |                |                         |                |                   |           | ISO7420FCCDR (reel) |

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

|                       |                               | VALUE                              |  |          |         |
|-----------------------|-------------------------------|------------------------------------|--|----------|---------|
| $V_{CC1}$ , $V_{CC2}$ | Supply voltage <sup>(2)</sup> | –0.5 V to 6 V                      |  |          |         |
| $V_I$                 | Voltage at INA, INB           | –0.5 V to 6 V                      |  |          |         |
| $V_O$                 | Voltage at OUTA, OUTB         | –0.5 V to $V_{CC} + 0.5$ V         |  |          |         |
| $I_O$                 | Output current                | ±15 mA                             |  |          |         |
| ESD                   | Electrostatic discharge       | Human-body model                   | JEDEC Standard 22, Test Method A114-C.01 | All pins | ±4 kV   |
|                       |                               | Field-induced charged-device model | JEDEC Standard 22, Test Method C101      |          | ±1.5 kV |
| $T_{J(Max)}$          | Maximum junction temperature  | 150°C                              |  |          |         |
| $T_{stg}$             | Storage temperature           | –65°C to 150°C                     |  |          |         |

- Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- All voltage values except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values.

**RECOMMENDED OPERATING CONDITIONS**

|                    |  | MIN                    | TYP | MAX | UNIT |
|--------------------|--|------------------------|-----|-----|------|
| $V_{CC1}, V_{CC2}$ | Supply voltage                                 | 2.7                    |     | 5.5 | V    |
| $I_{OH}$           | High-level output current ( $V_{CC} \geq 3V$ ) | -4                     |     |     | mA   |
|                    | High-level output current ( $V_{CC} < 3V$ )    | -2                     |     |     | mA   |
| $I_{OL}$           | Low-level output current                       |                        |     | 4   | mA   |
| $V_{IH}$           | High-level input voltage                       | 2                      |     | 5.5 | V    |
| $V_{IL}$           | Low-level input voltage                        | 0                      |     | 0.8 | V    |
| $t_{ui}$           | Input pulse duration                           | $\geq 4.5V$ -Operation | 20  |     | ns   |
|                    |  | $< 4.5V$ -Operation    | 25  |     |      |
| $1 / t_{ui}$       | Signaling rate                                 | $\geq 4.5V$ -Operation | 0   | 50  | Mbps |
|                    |  | $< 4.5V$ -Operation    | 0   | 40  |      |
| $T_J^{(1)}$        | Junction temperature                           | -40                    |     | 136 | °C   |
| $T_A$              | Ambient temperature                            | -40                    | 25  | 125 | °C   |

(1) To maintain the recommended operating conditions for  $T_J$ , see the [Package Thermal Characteristics](#) table.

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## ELECTRICAL CHARACTERISTICS

 $V_{CC1}$  and  $V_{CC2} = 5V \pm 10\%$ ,  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ 

| PARAMETER  |  | TEST CONDITIONS  | MIN  | TYP | MAX | UNIT              |    |
|--|--|--|--|-----|-----|-------------------|----|
| $V_{OH}$   | High-level output voltage                  | $I_{OH} = -4 \text{ mA}$ ; see <a href="#">Figure 1</a> .        | $V_{CC2} - 0.5$  | 4.8 |     | V                 |    |
|  |  | $I_{OH} = -20 \mu\text{A}$ ; see <a href="#">Figure 1</a> .      | $V_{CC2} - 0.1$  | 5   |     |                   |    |
| $V_{OL}$   | Low-level output voltage                   | $I_{OL} = 4 \text{ mA}$ ; see <a href="#">Figure 1</a> .         |  | 0.2 | 0.4 | V                 |    |
|  |  | $I_{OL} = 20 \mu\text{A}$ ; see <a href="#">Figure 1</a> .       |  | 0   | 0.1 |                   |    |
| $V_{I(HYS)}$   | Input threshold voltage hysteresis         |  |  | 450 |     | mV                |    |
| $I_{IH}$   | High-level input current                   | $INx = V_{CC}$   |  |     | 10  | $\mu\text{A}$     |    |
| $I_{IL}$   | Low-level input current                    | $INx = 0 \text{ V}$  | -10  |     |     | $\mu\text{A}$     |    |
| CMTI   | Common-mode transient immunity             | $V_I = V_{CC}$ or $0 \text{ V}$ ; see <a href="#">Figure 3</a> . | 25   | 60  |     | kV/ $\mu\text{s}$ |    |
| <b>SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic <math>I_{CC}</math> measurement)</b> |  |  |  |     |     |                   |    |
| $I_{CC1}$  | Supply current for $V_{CC1}$ and $V_{CC2}$ | DC to 1 Mbps   | DC Input: $V_I = V_{CC}$ or $0 \text{ V}$ ,<br>AC Input: $C_L = 15\text{pF}$ |     | 0.5 | 1.1               | mA |
| $I_{CC2}$  |  |  |  |     | 3   | 4.6               |    |
| $I_{CC1}$  |  | 10 Mbps  | $C_L = 15\text{pF}$  |     | 1   | 1.5               |    |
| $I_{CC2}$  |  |  |  |     | 4   | 6                 |    |
| $I_{CC1}$  |  | 25 Mbps  | $C_L = 15\text{pF}$  |     | 1.7 | 2.5               |    |
| $I_{CC2}$  |  |  |  |     | 6   | 8.5               |    |
| $I_{CC1}$  |  | 50 Mbps  | $C_L = 15\text{pF}$  |     | 2.7 | 4                 |    |
| $I_{CC2}$  |  |  |  |     | 8.5 | 12                |    |

## SWITCHING CHARACTERISTICS

 $V_{CC1}$  and  $V_{CC2} = 5V \pm 10\%$ ,  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ 

| PARAMETER                   |   | TEST CONDITIONS                | MIN | TYP | MAX | UNIT          |
|-----------------------------|---|--------------------------------|-----|-----|-----|---------------|
| $t_{PLH}$ , $t_{PHL}$       | Propagation delay time                                    | See <a href="#">Figure 1</a> . | 10  | 20  | 37  | ns            |
| PWD <sup>(1)</sup>          | Pulse width distortion $ t_{PHL} - t_{PLH} $              |                                |     |     | 2.5 | 5             |
| $t_{sk(o)}$ <sup>(2)</sup>  | Channel-to-channel output skew time                       |                                |     |     | 2   | ns            |
| $t_{sk(pp)}$ <sup>(3)</sup> | Part-to-part skew time                                    |                                |     |     | 12  | ns            |
| $t_r$                       | Output signal rise time                                   | See <a href="#">Figure 1</a> . |     | 2.5 |     | ns            |
| $t_f$                       | Output signal fall time                                   |                                |     | 2.5 |     | ns            |
| $t_{GS}$                    | Pulse width of glitches suppressed by the input filter    |                                |     | 12  |     | ns            |
| $t_{fs}$                    | Fail-safe output delay time from input data or power loss | See <a href="#">Figure 2</a> . |     | 8   |     | $\mu\text{s}$ |

- (1) Also known as pulse skew.
- (2)  $t_{sk(o)}$  is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
- (3)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

## ELECTRICAL CHARACTERISTICS

 $V_{CC1}$  and  $V_{CC2} = 3.3\text{ V} \pm 10\%$ ,  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ 

| PARAMETER  |  | TEST CONDITIONS  |  | MIN             | TYP | MAX | UNIT              |
|--|--|--|--|-----------------|-----|-----|-------------------|
| $V_{OH}$   | High-level output voltage                  | $I_{OH} = -4\text{ mA}$ ; see <a href="#">Figure 1</a> .           |  | $V_{CC2} - 0.5$ | 3   |     | V                 |
|  |  | $I_{OH} = -20\text{ }\mu\text{A}$ ; see <a href="#">Figure 1</a> . |  | $V_{CC2} - 0.1$ | 3.3 |     |                   |
| $V_{OL}$   | Low-level output voltage                   | $I_{OL} = 4\text{ mA}$ ; see <a href="#">Figure 1</a> .            |  |                 | 0.2 | 0.4 | V                 |
|  |  | $I_{OL} = 20\text{ }\mu\text{A}$ ; see <a href="#">Figure 1</a> .  |  |                 | 0   | 0.1 |                   |
| $V_{I(HYS)}$   | Input threshold voltage hysteresis         |  |  |                 | 425 |     | mV                |
| $I_{IH}$   | High-level input current                   | $I_{Nx} = V_{CC}$  |  |                 |     | 10  | $\mu\text{A}$     |
| $I_{IL}$   | Low-level input current                    | $I_{Nx} = 0\text{ V}$  |  | -10             |     |     | $\mu\text{A}$     |
| CMTI   | Common-mode transient immunity             | $V_I = V_{CC}$ or $0\text{ V}$ ; see <a href="#">Figure 3</a> .    |  | 25              | 40  |     | kV/ $\mu\text{s}$ |
| <b>SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic <math>I_{CC}</math> measurement)</b> |  |  |  |                 |     |     |                   |
| $I_{CC1}$  | Supply current for $V_{CC1}$ and $V_{CC2}$ | DC to 1 Mbps   | DC Input: $V_I = V_{CC}$ or $0\text{ V}$ ,<br>AC Input: $C_L = 15\text{ pF}$ |                 | 0.3 | 0.8 | mA                |
| $I_{CC2}$  |  |  |  |                 | 2.4 | 3.3 |                   |
| $I_{CC1}$  |  | 10 Mbps  | $C_L = 15\text{ pF}$   |                 | 0.6 | 1.2 |                   |
| $I_{CC2}$  |  |  |  |                 | 3.1 | 4.5 |                   |
| $I_{CC1}$  |  | 25 Mbps  | $C_L = 15\text{ pF}$   |                 | 1   | 2   |                   |
| $I_{CC2}$  |  |  |  |                 | 4.2 | 6.1 |                   |
| $I_{CC1}$  |  | 40 Mbps  | $C_L = 15\text{ pF}$   |                 | 1.3 | 2.3 |                   |
| $I_{CC2}$  |  |  |  |                 | 5.3 | 7.5 |                   |

## SWITCHING CHARACTERISTICS

 $V_{CC1}$  and  $V_{CC2} = 3.3\text{ V} \pm 10\%$ ,  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ 

| PARAMETER                   |  | TEST CONDITIONS                | MIN | TYP  | MAX | UNIT          |
|-----------------------------|--|--------------------------------|-----|------|-----|---------------|
| $t_{PLH}$ , $t_{PHL}$       | Propagation delay time                                 | See <a href="#">Figure 1</a> . | 10  | 22   | 40  | ns            |
| PWD <sup>(1)</sup>          | Pulse width distortion $ t_{PHL} - t_{PLH} $           |                                |     |      | 3   | ns            |
| $t_{sk(o)}$ <sup>(2)</sup>  | Channel-to-channel output skew time                    |                                |     | 2    | ns  |               |
| $t_{sk(pp)}$ <sup>(3)</sup> | Part-to-part skew time                                 |                                |     | 19   | ns  |               |
| $t_r$                       | Output signal rise time                                | See <a href="#">Figure 1</a> . |     | 3    |     | ns            |
| $t_f$                       | Output signal fall time                                |                                |     | 3    |     | ns            |
| $t_{GS}$                    | Pulse width of glitches suppressed by the input filter |                                |     | 12.5 |     | ns            |
| $t_{fs}$                    | Fail-safe output delay time from input power loss      | See <a href="#">Figure 2</a> . |     | 8    |     | $\mu\text{s}$ |

- (1) Also known as pulse skew.
- (2)  $t_{sk(o)}$  is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
- (3)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

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## ELECTRICAL CHARACTERISTICS

$V_{CC1}$  and  $V_{CC2} = 2.7\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$

| PARAMETER  |  | TEST CONDITIONS   |  | MIN             | TYP  | MAX | UNIT              |
|--|--|---|--|-----------------|------|-----|-------------------|
| $V_{OH}$   | High-level output voltage                  | $I_{OH} = -2\text{ mA}$ ; see <a href="#">Figure 1</a> .        |  | $V_{CC2} - 0.3$ | 2.5  |     | V                 |
|  |  | $I_{OH} = -20\ \mu\text{A}$ ; see <a href="#">Figure 1</a> .    |  | $V_{CC2} - 0.1$ | 2.7  |     |                   |
| $V_{OL}$   | Low-level output voltage                   | $I_{OL} = 4\text{ mA}$ ; see <a href="#">Figure 1</a> .         |  |                 | 0.2  | 0.4 | V                 |
|  |  | $I_{OL} = 20\ \mu\text{A}$ ; see <a href="#">Figure 1</a> .     |  |                 | 0    | 0.1 |                   |
| $V_{I(HYS)}$   | Input threshold voltage hysteresis         |   |  |                 | 350  |     | mV                |
| $I_{IH}$   | High-level input current                   | $I_{Nx} = V_{CC}$   |  |                 |      | 10  | $\mu\text{A}$     |
| $I_{IL}$   | Low-level input current                    | $I_{Nx} = 0\text{ V}$   |  | -10             |      |     | $\mu\text{A}$     |
| CMTI   | Common-mode transient immunity             | $V_I = V_{CC}$ or $0\text{ V}$ ; see <a href="#">Figure 3</a> . |  | 25              | 35   |     | kV/ $\mu\text{s}$ |
| <b>SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic <math>I_{CC}</math> measurement)</b> |  |   |  |                 |      |     |                   |
| $I_{CC1}$  | Supply current for $V_{CC1}$ and $V_{CC2}$ | DC to 1 Mbps  | DC Input: $V_I = V_{CC}$ or $0\text{ V}$ ,<br>AC Input: $C_L = 15\text{ pF}$ |                 | 0.15 | 0.4 | mA                |
| $I_{CC2}$  |  |   |  |                 | 2.1  | 3.1 |                   |
| $I_{CC1}$  |  | 10 Mbps   | $C_L = 15\text{ pF}$   |                 | 0.4  | 0.7 |                   |
| $I_{CC2}$  |  |   |  |                 | 2.7  | 4   |                   |
| $I_{CC1}$  |  | 25 Mbps   | $C_L = 15\text{ pF}$   |                 | 0.7  | 1.2 |                   |
| $I_{CC2}$  |  |   |  |                 | 3.6  | 5   |                   |
| $I_{CC1}$  |  | 40 Mbps   | $C_L = 15\text{ pF}$   |                 | 1    | 1.7 |                   |
| $I_{CC2}$  |  |   |  |                 | 4.4  | 6.3 |                   |

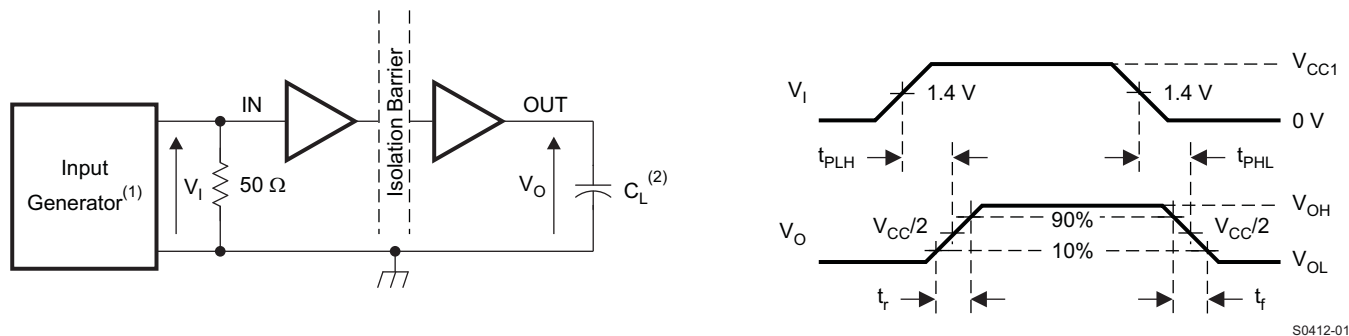
## SWITCHING CHARACTERISTICS

$V_{CC1}$  and  $V_{CC2} = 2.7\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$

| PARAMETER                   |  | TEST CONDITIONS                | MIN | TYP  | MAX | UNIT          |
|-----------------------------|--|--------------------------------|-----|------|-----|---------------|
| $t_{PLH}$ , $t_{PHL}$       | Propagation delay time                                 | See <a href="#">Figure 1</a> . | 15  | 26   | 45  | ns            |
| PWD <sup>(1)</sup>          | Pulse width distortion $ t_{PHL} - t_{PLH} $           |                                |     |      | 3   | ns            |
| $t_{sk(o)}$ <sup>(2)</sup>  | Channel-to-channel output skew time                    |                                |     | 2    | ns  |               |
| $t_{sk(pp)}$ <sup>(3)</sup> | Part-to-part skew time                                 |                                |     | 22   | ns  |               |
| $t_r$                       | Output signal rise time                                | See <a href="#">Figure 1</a> . |     | 3    |     | ns            |
| $t_f$                       | Output signal fall time                                |                                |     | 3    |     | ns            |
| $t_{GS}$                    | Pulse width of glitches suppressed by the input filter |                                |     | 13.5 |     | ns            |
| $t_{fs}$                    | Fail-safe output delay time from input power loss      | See <a href="#">Figure 2</a> . |     | 8    |     | $\mu\text{s}$ |

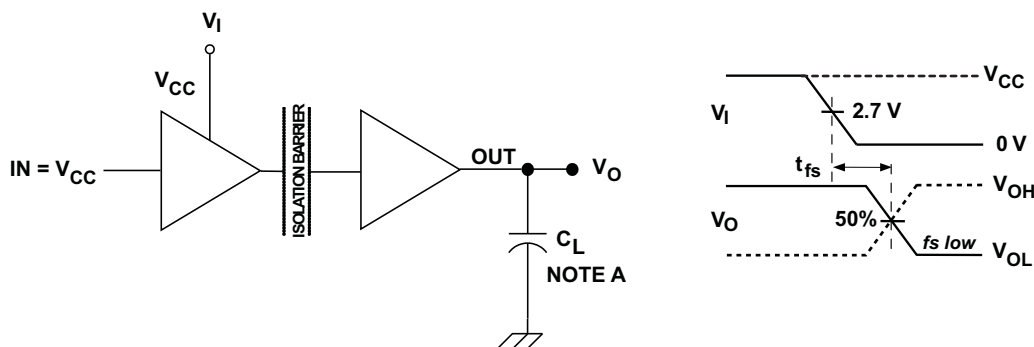
- (1) Also known as pulse skew.
- (2)  $t_{sk(o)}$  is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
- (3)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

PARAMETER MEASUREMENT INFORMATION



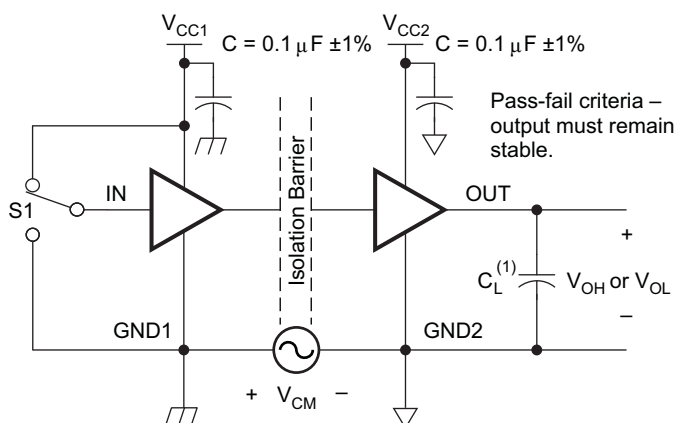
- (1) The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns,  $Z_O = 50 \Omega$ . At the input, a 50-Ω resistor is required to terminate the Input Generator signal. It is not needed in actual application.
- (2)  $C_L = 15$  pF and includes instrumentation and fixture capacitance within ±20%.

Figure 1. Switching Characteristic Test Circuit and Voltage Waveforms



- A.  $C_L = 15$  pF and includes instrumentation and fixture capacitance within ±20%.

Figure 2. Fail-Safe Output Delay-Time Test Circuit and Voltage Waveforms



- (1)  $C_L = 15$  pF and includes instrumentation and fixture capacitance within ±20%.

Figure 3. Common-Mode Transient Immunity Test Circuit

## DEVICE INFORMATION

### IEC Insulation and Safety-Related Specifications for D-8 Package

over recommended operating conditions (unless otherwise noted)

| PARAMETER       |  | TEST CONDITIONS  | MIN               | TYP | MAX | UNIT |
|-----------------|--|--|-------------------|-----|-----|------|
| L(I01)          | Minimum air gap (clearance)                          | Shortest terminal-to-terminal distance through air                                     | 4                 |     |     | mm   |
| L(I02)          | Minimum external tracking (creepage)                 | Shortest terminal-to-terminal distance across the package surface                      | 4                 |     |     | mm   |
| CTI             | Tracking resistance (comparative tracking index)     | DIN IEC 60112 / VDE 0303 Part 1  | >400              |     |     | V    |
|                 | Minimum internal gap (internal clearance)            | Distance through the insulation  | 0.014             |     |     | mm   |
| R <sub>IO</sub> | Isolation resistance, input to output <sup>(1)</sup> | V <sub>IO</sub> = 500 V, T <sub>A</sub> < 100°C  | >10 <sup>12</sup> |     |     | Ω    |
|                 |  | V <sub>IO</sub> = 500 V, 100°C ≤ T <sub>A</sub> ≤ max                                  | >10 <sup>11</sup> |     |     | Ω    |
| C <sub>IO</sub> | Barrier capacitance, input to output <sup>(1)</sup>  | V <sub>IO</sub> = 0.4 sin (2πft), f = 1 MHz  |                   | 1   |     | pF   |
| C <sub>I</sub>  | Input capacitance <sup>(2)</sup>                     | V <sub>I</sub> = V <sub>CC</sub> /2 + 0.4 sin (2πft), f = 1 MHz, V <sub>CC</sub> = 5 V |                   | 1   |     | pF   |

(1) All pins on each side of the barrier tied together creating a two-terminal device.

(2) Measured from input pin to ground.

#### NOTE

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

### INSULATION CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER <sup>(1)</sup> |   | TEST CONDITIONS   | SPECIFICATION    | UNIT              |
|--------------------------|---|---|------------------|-------------------|
| V <sub>IORM</sub>        | Maximum working insulation voltage                |   | 566              | V <sub>PEAK</sub> |
| V <sub>PR</sub>          | Input-to-output test voltage per DIN EN 60747-5-5 | Method a, After environmental tests subgroup 1, V <sub>PR</sub> = V <sub>IORM</sub> × 1.6, t = 10 s, Partial Discharge < 5 pC | 906              | V <sub>PEAK</sub> |
|                          |   | Method b1, V <sub>PR</sub> = V <sub>IORM</sub> × 1.875, t = 1 s (100% Production test) Partial discharge < 5 pC               | 1062             |                   |
|                          |   | After Input/Output safety test subgroup 2/3, V <sub>PR</sub> = V <sub>IORM</sub> × 1.2, t = 10 s, Partial discharge < 5 pC    | 680              |                   |
| V <sub>IOTM</sub>        | Transient overvoltage per DIN EN 60747-5-5        | V <sub>TEST</sub> = V <sub>IOTM</sub><br>t = 60 sec (qualification)<br>t = 1 sec (100% production)                            | 4242             | V <sub>PEAK</sub> |
| V <sub>ISO</sub>         | Isolation voltage per UL 1577                     | V <sub>TEST</sub> = V <sub>ISO</sub> , t = 60 sec (qualification)   | 2500             | V <sub>RMS</sub>  |
|                          |   | V <sub>TEST</sub> = 1.2 × V <sub>ISO</sub> , t = 1 sec (100% production)  | 3000             |                   |
| R <sub>S</sub>           | Insulation resistance                             | V <sub>IO</sub> = 500 V at T <sub>S</sub>   | >10 <sup>9</sup> | Ω                 |
|                          | Pollution degree                                  |   | 2                |                   |

(1) Climatic Classification 40/125/21

**Table 2. IEC 60664-1 RATINGS TABLE**

| PARAMETER                   | TEST CONDITIONS                        | SPECIFICATION |
|-----------------------------|--|---------------|
| Basic isolation group       | Material group                         | II            |
| Installation classification | Rated mains voltage $\leq 150 V_{RMS}$ | I–IV          |
|                             | Rated mains voltage $\leq 300 V_{RMS}$ | I–III         |
|                             | Rated mains voltage $\leq 400 V_{RMS}$ | I–II          |

**REGULATORY INFORMATION**

| VDE   | CSA  | UL  | CQC   |
|---|--|---|---|
| Certified according to DIN EN 60747-5-5 (VDE 0884-5)  | Approved under CSA Component Acceptance Notice #5A   | Recognized under UL 1577 Component Recognition Program          | Certified according to GB 4943.1-2011   |
| Basic Insulation<br>Maximum Transient Overvoltage, 4242 $V_{PK}$<br>Maximum Working Voltage, 566 $V_{PK}$ | 400 $V_{RMS}$ Basic and 200 $V_{RMS}$ Reinforced Insulation per CSA 60950-1-07 and IEC 60950-1 (2nd Ed)<br>300 $V_{RMS}$ Basic and 150 $V_{RMS}$ Reinforced Insulation per CSA 61010-1-12 and IEC 61010-1 (3rd Ed) | Single / Basic Isolation Voltage, 2500 $V_{RMS}$ <sup>(1)</sup> | Basic Insulation, Altitude $\leq 5000m$ , Tropical Climate, 250 $V_{RMS}$ maximum working voltage |
| Certificate number: 40016131  | Master contract number: 220991   | File number: E181974  | File number: Pending  |

(1) Production tested  $\geq 3000 V_{RMS}$  for 1 second in accordance with UL 1577.

### IEC SAFETY LIMITING VALUES

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

| PARAMETER  | TEST CONDITIONS   | MIN | TYP | MAX | UNIT |
|--|---|-----|-----|-----|------|
| I <sub>S</sub> Safety input, output, or supply current | $\theta_{JA} = 115.1^{\circ}\text{C/W}$ , $V_I = 5.5\text{ V}$ , $T_J = 150^{\circ}\text{C}$ , $T_A = 25^{\circ}\text{C}$ |     |     | 197 | mA   |
|  | $\theta_{JA} = 115.1^{\circ}\text{C/W}$ , $V_I = 3.6\text{ V}$ , $T_J = 150^{\circ}\text{C}$ , $T_A = 25^{\circ}\text{C}$ |     |     | 302 |      |
|  | $\theta_{JA} = 115.1^{\circ}\text{C/W}$ , $V_I = 2.7\text{ V}$ , $T_J = 150^{\circ}\text{C}$ , $T_A = 25^{\circ}\text{C}$ |     |     | 402 |      |
| T <sub>S</sub> Maximum case temperature                |   |     |     | 150 | °C   |

The safety-limiting constraint is the absolute-maximum junction temperature specified in the *Absolute Maximum Ratings* table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed on a High-K Test Board for Leaded Surface-Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

### PACKAGE THERMAL CHARACTERISTICS

(over recommended operating conditions unless otherwise noted)

| THERMAL METRIC <sup>(1)</sup>                                 |   | ISO7420               | UNITS |
|---|---|-----------------------|-------|
|   |   | D PACKAGE<br>(8) PINS |       |
| $\theta_{JA}$ Junction-to-ambient thermal resistance          |   | 115.1                 | °C/W  |
| $\theta_{JCtop}$ Junction-to-case (top) thermal resistance    |   | 60.1                  |       |
| $\theta_{JB}$ Junction-to-board thermal resistance            |   | 56.4                  |       |
| $\psi_{JT}$ Junction-to-top characterization parameter        |   | 17.2                  |       |
| $\psi_{JB}$ Junction-to-board characterization parameter      |   | 55.8                  |       |
| $\theta_{JCbot}$ Junction-to-case (bottom) thermal resistance |   | N/A                   |       |
| P <sub>D</sub> Device power dissipation                       | $V_{CC1} = V_{CC2} = 5.5\text{ V}$ , $T_J = 150^{\circ}\text{C}$ , $C_L = 15\text{ pF}$ ,<br>Input a 50-Mbps 50% duty-cycle square wave | 120                   | mW    |

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, [SPRA953](#).

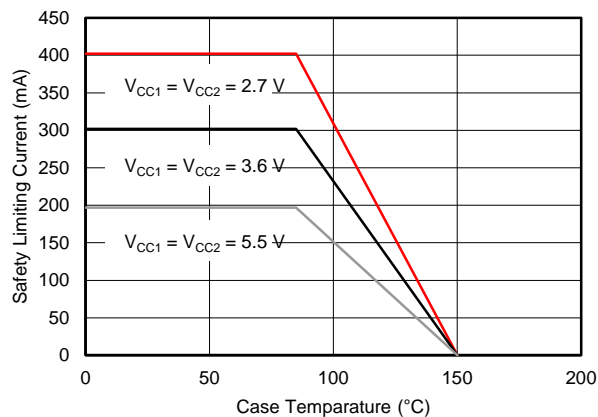


Figure 4.  $\theta_{JC}$  Thermal Derating Curve per DIN EN 60747-5-5

APPLICATION INFORMATION

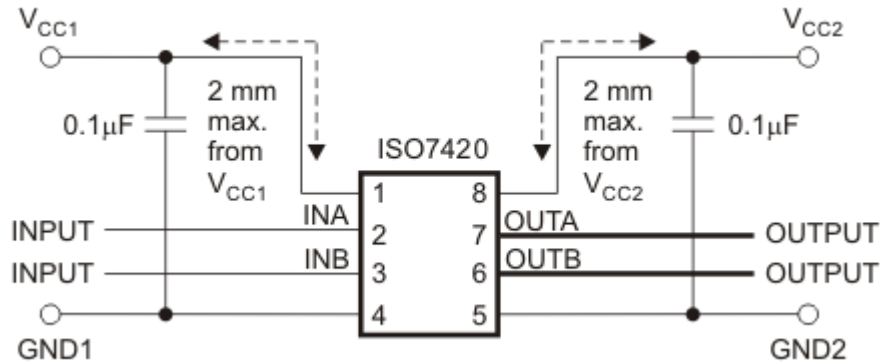


Figure 5. Typical ISO7420FCC Application Circuit

Note: For detailed layout recommendations, see Application Note [SLLA284](#), *Digital Isolator Design Guide*.

SUPPLY CURRENT EQUATIONS

Maximum Supply Current Equations

(Calculated over recommended operating temperature range and Silicon process variation)

At  $V_{CC1} = V_{CC2} = 5V \pm 10\%$

$$I_{CC1(max)} = 1.1 + 5.80E-02 \times f$$

$$I_{CC2(max)} = 4.6 + 6.55E-02 \times f + 5.5E-03 \times f \times C_L$$

At  $V_{CC1} = V_{CC2} = 3.3V \pm 10\%$

$$I_{CC1(max)} = 0.8 + 3.40E-02 \times f$$

$$I_{CC2(max)} = 3.3 + 4.60E-02 \times f + 3.6E-03 \times f \times C_L$$

At  $V_{CC1} = V_{CC2} = 2.7V$

$$I_{CC1(max)} = 0.4 + 3.20E-02 \times f$$

$$I_{CC2(max)} = 3.1 + 3.75E-02 \times f + 2.7E-03 \times f \times C_L$$

f is data rate of each channel measured in Mbps;  $C_L$  is the capacitive load of each channel measured in pF;  $I_{CC1(max)}$  and  $I_{CC2(max)}$  are measured in mA.

Typical Supply Current Equations

(Calculated for  $T_A = 25^\circ C$  and nominal Silicon process material)

At  $V_{CC1} = V_{CC2} = 5V$

$$I_{CC1(typ)} = 0.5 + 4.40E-02 \times f$$

$$I_{CC2(typ)} = 3 + 3.50E-02 \times f + 5.0E-03 \times f \times C_L$$

At  $V_{CC1} = V_{CC2} = 3.3V$

$$I_{CC1(typ)} = 0.3 + 2.60E-02 \times f$$

$$I_{CC2(typ)} = 2.4 + 2.25E-02 \times f + 3.3E-03 \times f \times C_L$$

At  $V_{CC1} = V_{CC2} = 2.7V$

$$I_{CC1(typ)} = 0.15 + 2.10E-02 \times f$$

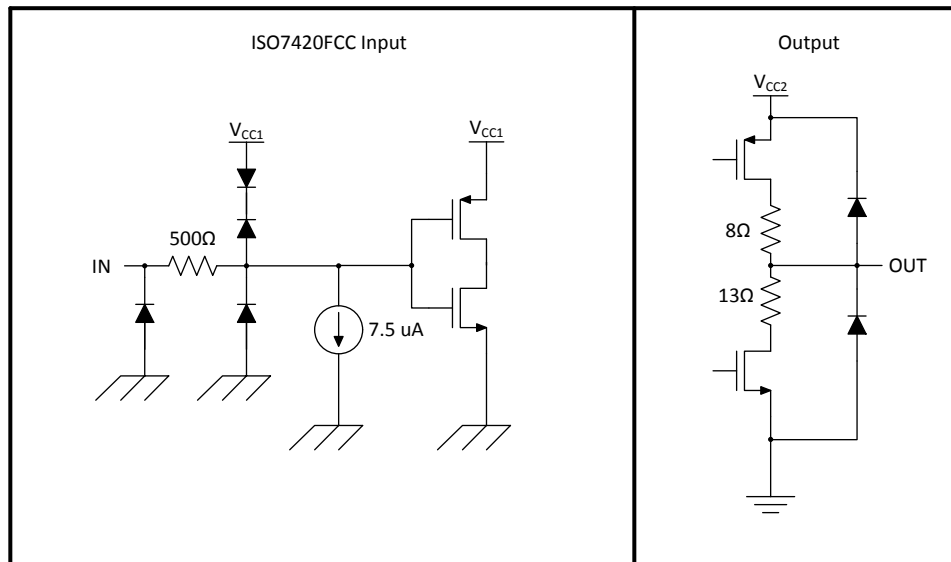
$$I_{CC2(typ)} = 2.1 + 1.75E-02 \times f + 2.7E-03 \times f \times C_L$$

f is Data Rate of each channel measured in Mbps;  $C_L$  is the Capacitive Load of each channel measured in pF;  $I_{CC1(typ)}$  and  $I_{CC2(typ)}$  are measured in mA.

# ISO7420FCC

SLLSED3B – JUNE 2013 – REVISED JANUARY 2014

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**Figure 6. Device I/O Schematics**

TYPICAL CHARACTERISTICS

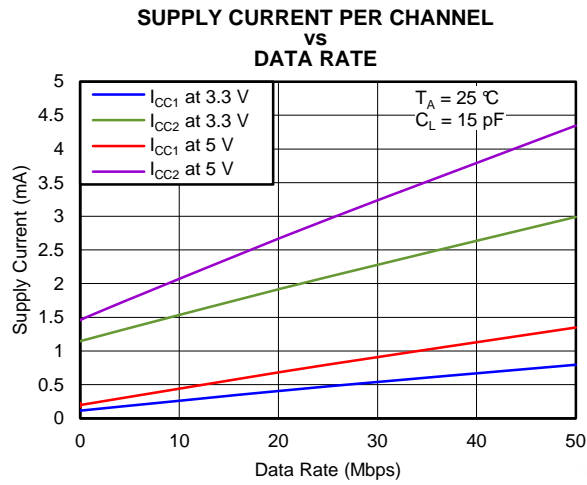


Figure 7.

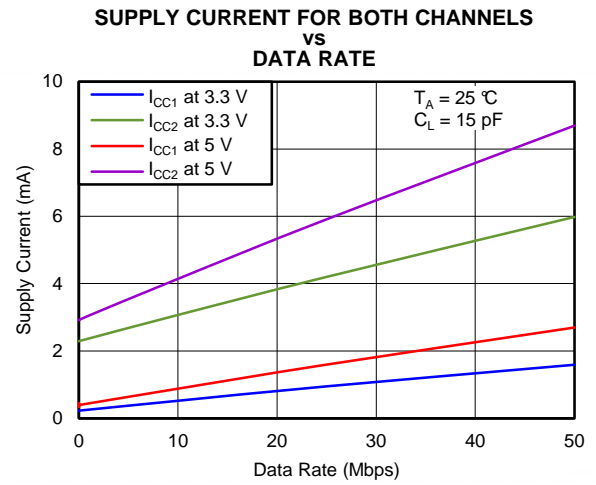


Figure 8.

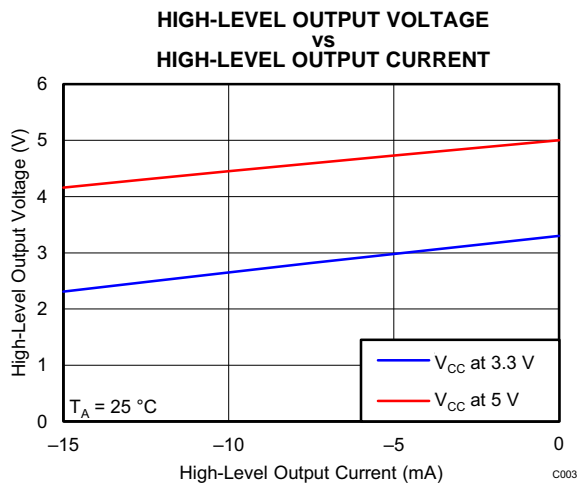


Figure 9.

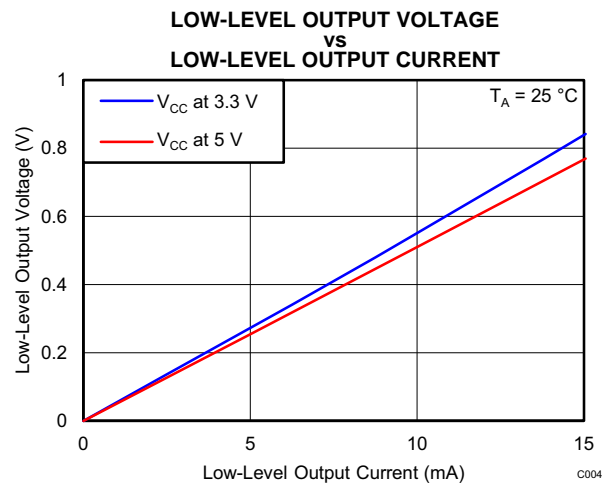


Figure 10.

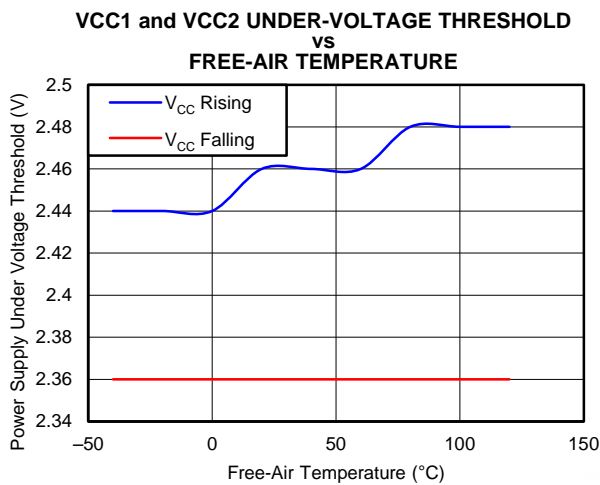


Figure 11.

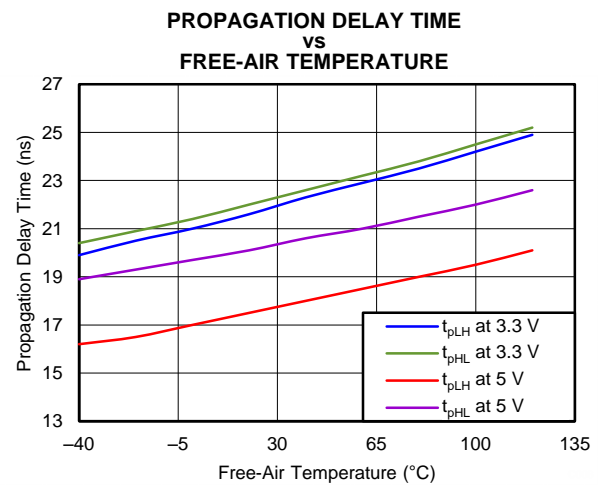


Figure 12.

TYPICAL CHARACTERISTICS (continued)

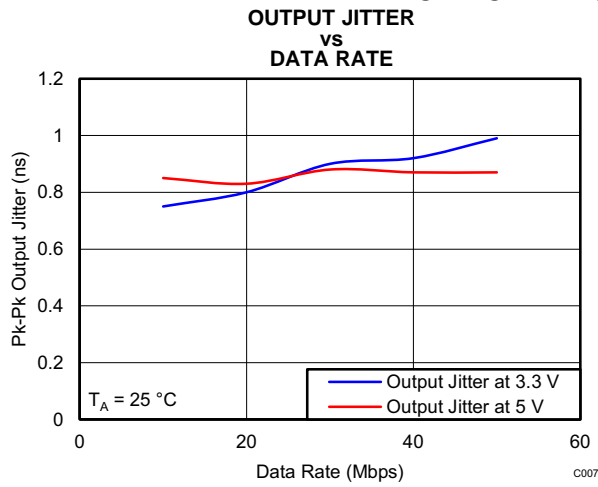


Figure 13.

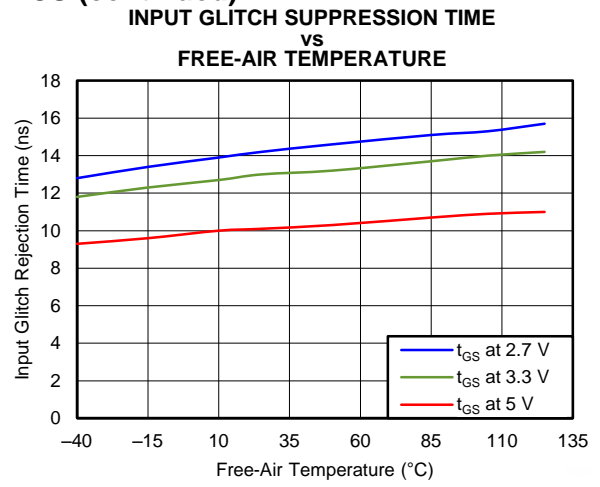


Figure 14.

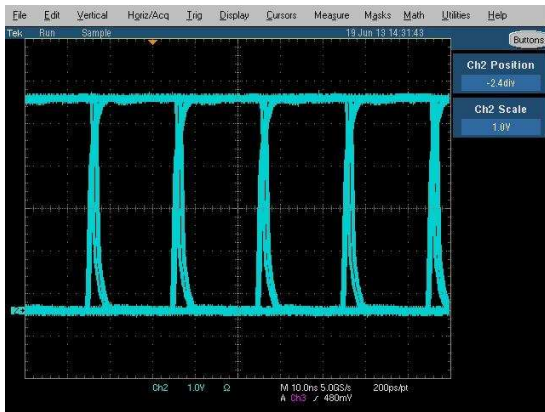


Figure 15. Eye Diagram at 50 Mbps, 5V at 25°C

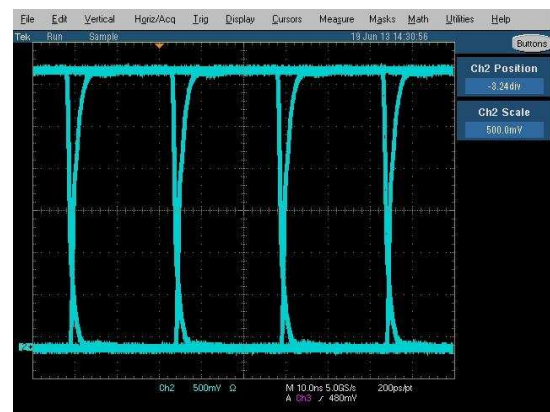


Figure 16. Eye Diagram at 40 Mbps, 3.3V at 25°C



Figure 17. Eye Diagram at 40 Mbps, 2.7V at 25°C

## REVISION HISTORY

| <b>Changes from Original (June 2013) to Revision A</b>   | <b>Page</b> |
|--|-------------|
| • Changed High-level output voltage MIN Value From: $V_{CCx}$ To: $V_{CC2}$ .....                    | 4           |
| • Changed High-level output voltage MIN Value From: $V_{CCx}$ To: $V_{CC2}$ and removed Note 1 ..... | 5           |
| • Changed High-level output voltage MIN Value From: $V_{CCx}$ To: $V_{CC2}$ and removed Note 1 ..... | 6           |
| • Changed <a href="#">Figure 9</a> X axis values .....   | 13          |

| <b>Changes from Revision A (July 2013) to Revision B</b>  | <b>Page</b> |
|---|-------------|
| • Changed the SAFETY AND REGULATORY APPROVALS list .....  | 1           |
| • Changed the $V_{IH}$ MAX value From: $V_{CC}$ To: 5.5V in the RECOMMENDED OPERATING CONDITIONS table .....  | 3           |
| • Changed the $V_{PR}$ and $V_{IOTM}$ parameter From: DIN EN 60747-5-2 To: DIN EN 60747-5-5 in the INSULATION CHARACTERISTICS table .....   | 8           |
| • Changed the REGULATORY INFORMATION table .....  | 9           |
| • Changed the title of <a href="#">Figure 4</a> From: $\theta_{JC}$ Thermal Derating Curve per DIN EN 60747-5-2 To: $\theta_{JC}$ Thermal Derating Curve per DIN EN 60747-5-5 ..... | 10          |

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| ISO7420FCCD      | ACTIVE        | SOIC         | D               | 8    | 75          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | -40 to 125   | 7420FC                  | <a href="#">Samples</a> |
| ISO7420FCCDR     | ACTIVE        | SOIC         | D               | 8    | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | -40 to 125   | 7420FC                  | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ISO7420FCCDR | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**

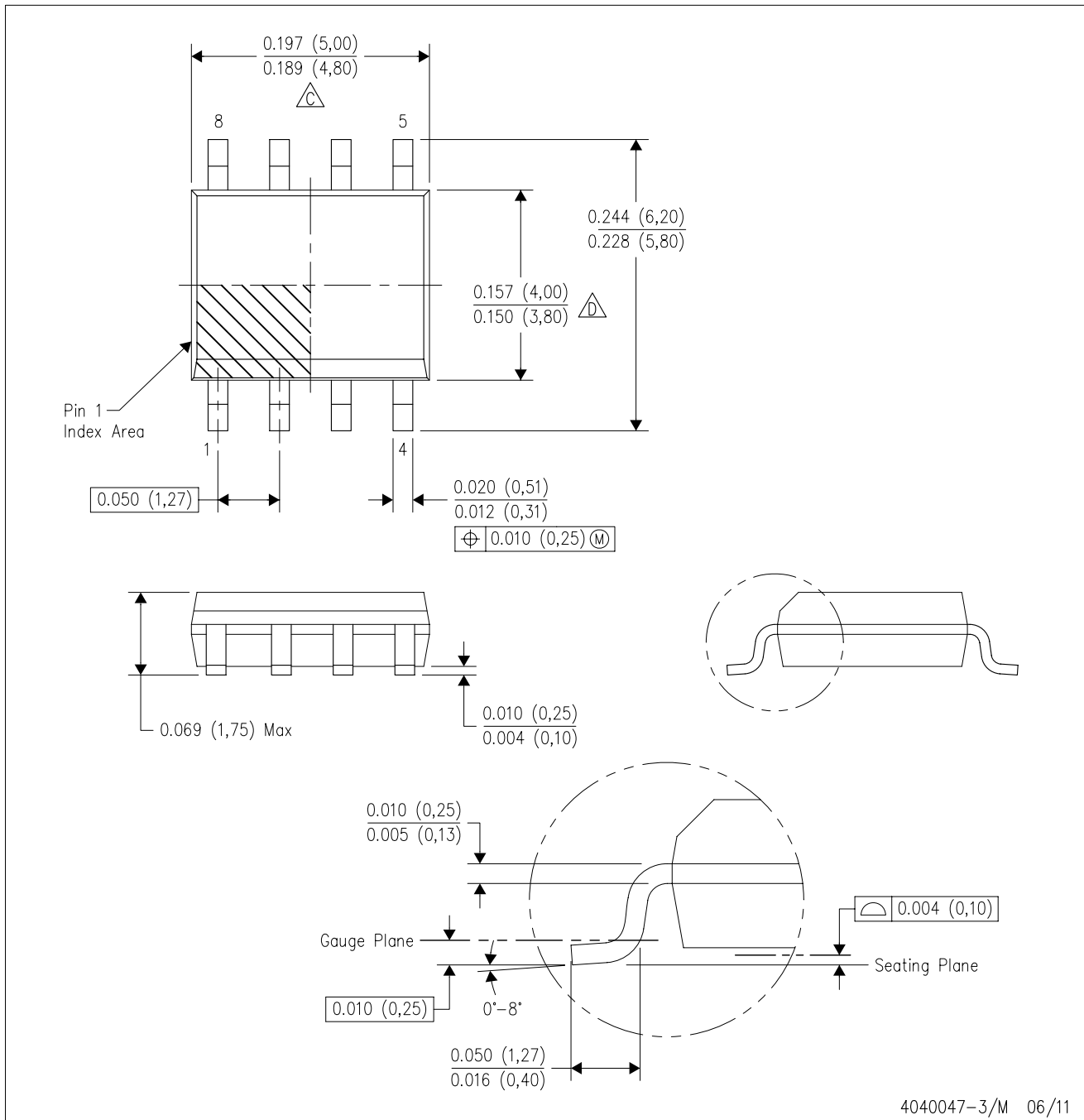


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ISO7420FCCDR | SOIC         | D               | 8    | 2500 | 367.0       | 367.0      | 35.0        |

D (R-PDSO-G8)

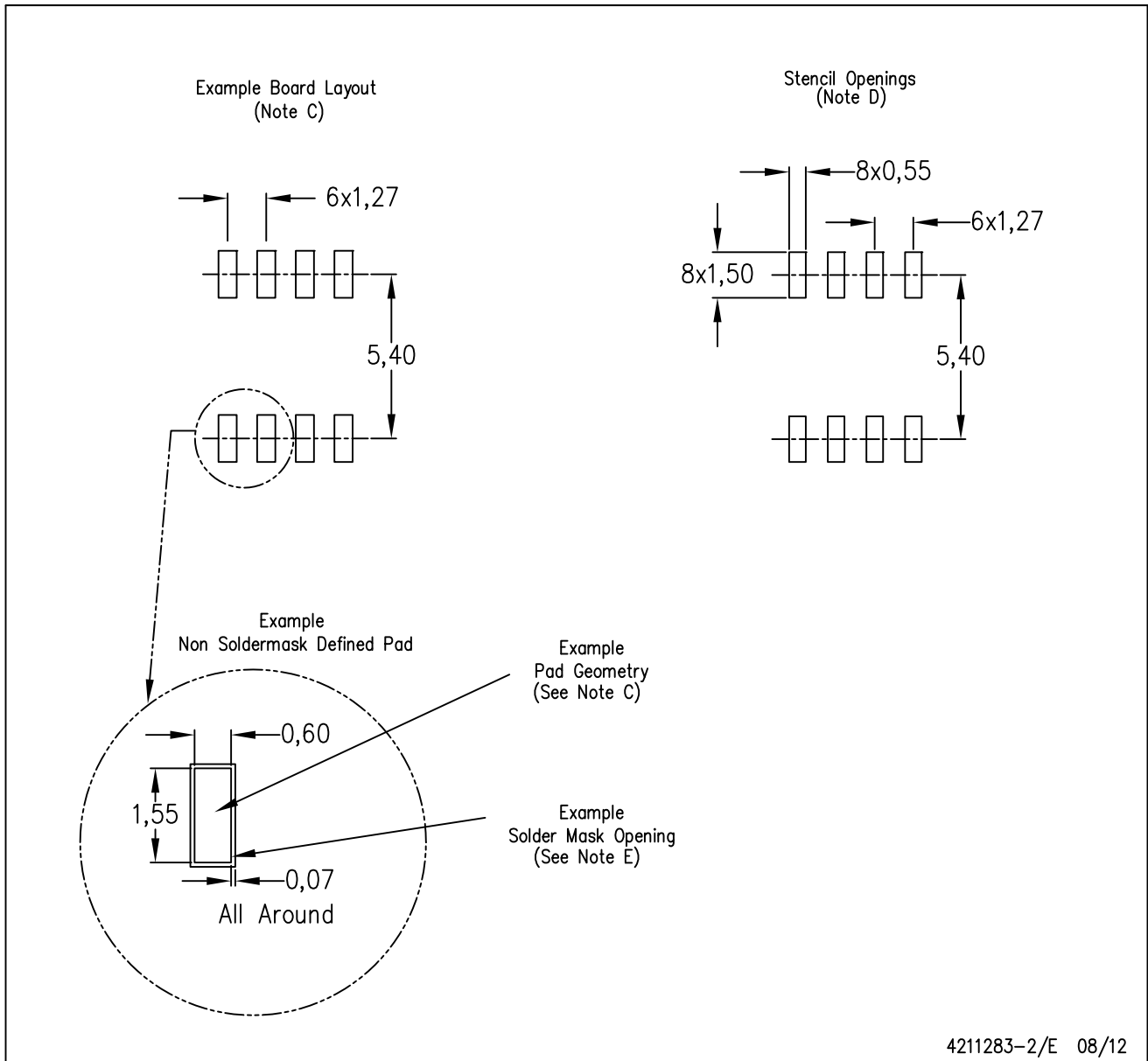
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - △ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - △ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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| Energy and Lighting           | <a href="http://www.ti.com/energy">www.ti.com/energy</a>                                 |
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