512Kx8 LOW VOLTAGE, SERIAL SRAM with SPI, SDI and SQI INTERFACE

OCTOBER 2020

KEY FEATURES

- SPI-Compatible Bus Interface:
  - 16/20 MHz Clock rate
  - SPI/SDI/SQI mode
- Low-Power CMOS Technology:
  - Read Current: 16 mA(max) at 3.6V, 20 MHz, 85°C
  - CMOS Standby Current: 8 μA(typ)
- 512K x 8-bit Organization:
  - 32-byte page
- Byte, Page and Sequential mode for Reads and Writes
- Temperature Ranges Supported:
  - Industrial (I): -40°C to +85°C
  - Automotive (A3): -40°C to +125°C
- RoHS Compliant
  - 8-pin SOIC, 8-pin TSSOP, and 24-ball TFBGA packages

DESCRIPTION

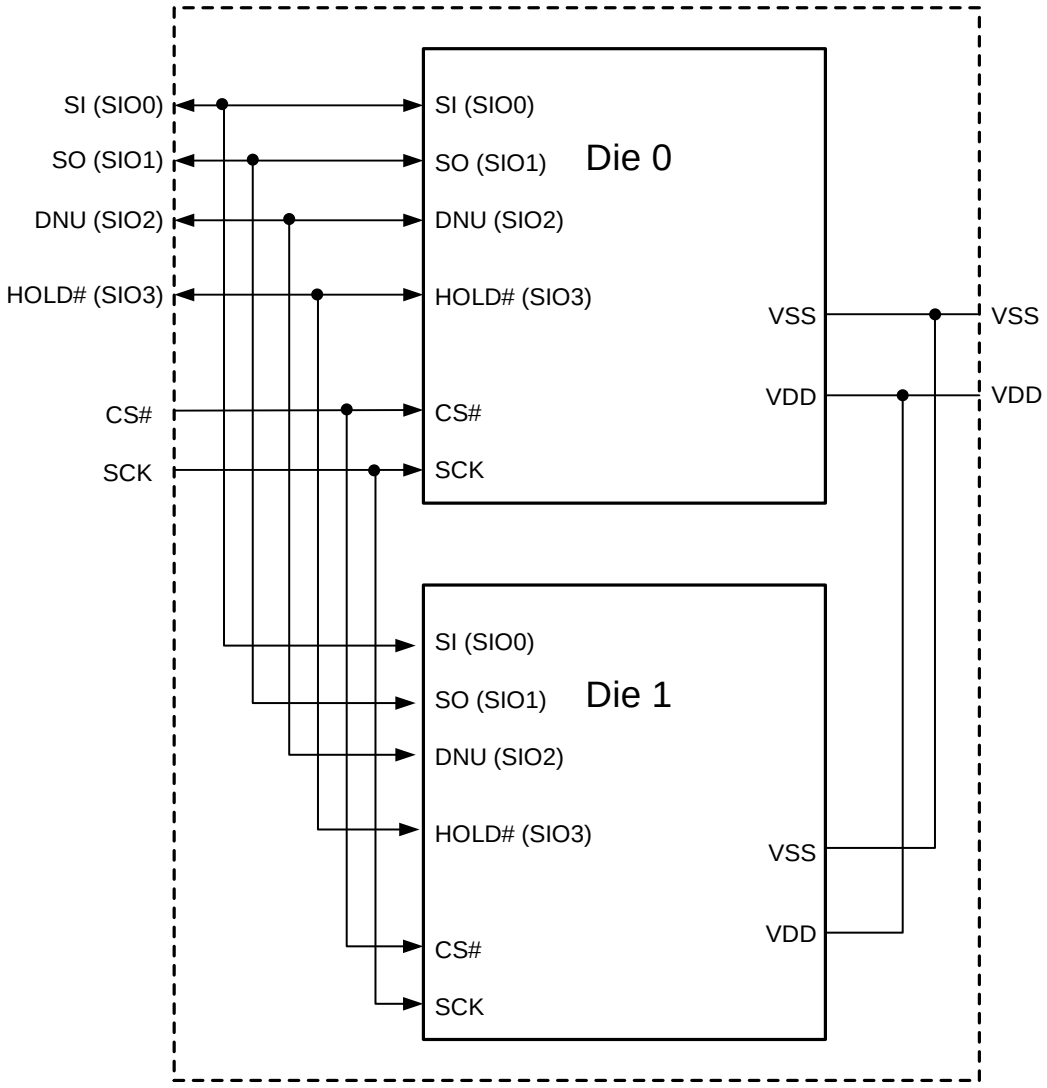
The *ISSI* IS62/65WVS5128FALL/FBLL are 4M bit Serial static RAMs organized as 512K bytes by 8 bits. It is a dual die stack of two 2Mb Serial SRAMs.

The device is accessed via a simple Serial Peripheral Interface (SPI) compatible serial bus. The bus signals required are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access the device is controlled through a Chip Select (CS#) input. Additionally, SDI (Serial Dual Interface) and SQI (Serial Quad Interface) is supported if your application needs faster data rates.

This device also supports unlimited reads and writes to the memory array.

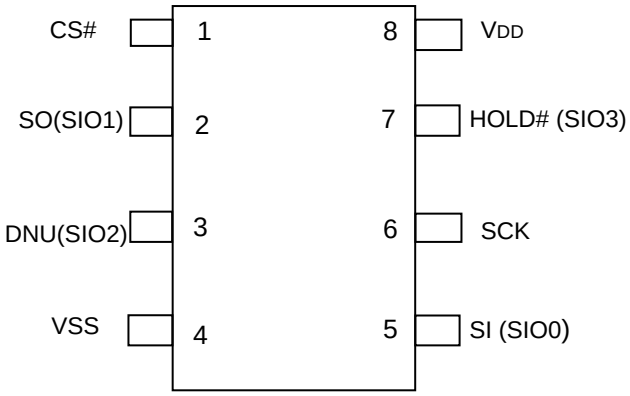
The IS62/65WVS5128FALL/FBLL are available in the standard packages including 8-pin SOIC, 8-pin TSSOP and 24-ball TFBGA (6mm x 8mm).

BLOCK DIAGRAM



PIN CONFIGURATIONS

8-pin SOIC/TSSOP

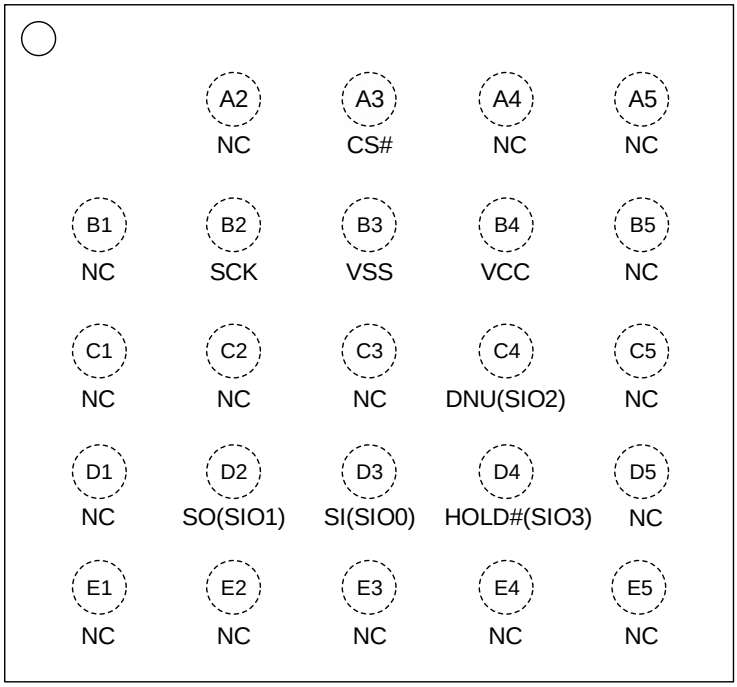


PIN DESCRIPTIONS

CS#	Chip Enable Input
SO/SIO1	Serial Output/SIO1
DNU/SIO2	Do Not Use/SIO2
VSS	Ground
SI/SIO0	Serial Input/SIO0
SCK	Serial Clock
HOLD#/SIO3	HOLD#/SIO3
VDD	Power

24-ball TFBGA

Top View, Balls Facing Down



Chip Select (CS#)

A low level on this pin selects the device. A high level deselects the device and forces it into Standby mode. When the device is deselected, SO goes to the high- impedance state, allowing multiple parts to share the same SPI bus. After power-up, a low level on CS# is required, prior to any sequence being initiated.

Serial Clock (SCK)

The SCK is used to synchronize the communication between a master and Serial SRAM. Instructions, addresses or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

Serial Output (SO: SPI mode)

The SO pin is used to transfer data out of the device. During a read cycle, data is shifted out on this pin after the falling edge of the serial clock.

Serial Input (SI: SPI mode)

The SI pin is used to transfer data into the device. It receives instructions, addresses, and data. Data is latched on the rising edge of the serial clock.

HOLD Function (HOLD#: SPI Mode, and SDI Mode)

The HOLD# pin is used to suspend transmission to Serial SRAM while in the middle of a serial sequence without having to re-transmit the entire sequence over again. It must be held high any time this function is not being used. Once the device is selected and a serial sequence is underway, the HOLD# pin may be pulled low to pause further serial communication without resetting the serial sequence.

The HOLD# pin should be brought low while SCK is low, otherwise the HOLD function will not be invoked until the next SCK high-to-low transition. The device must remain selected during this sequence. The SI and SCK levels are “don’t cares” during the time the device is paused and any transitions on these pins will be ignored. To resume serial communication, HOLD# should be brought high while the SCK pin is low, otherwise serial communication will not be resumed until the next SCK high-to-low transition.

The SO line will tri-state immediately upon a high-to low transition of the HOLD# pin, and will begin outputting again Immediately upon a subsequent low- to-high transition of the HOLD pin, independent of the state of SCK.

Hold functionality is not available when operating in Quad SPI mode

Serial Input / Output Pins (SIO0, SIO1: SDI Mode)

The SIO0 and SIO1 pins are used for Dual SPI mode of operation (SI→SIO0, SO-->SIO1). Functionality of these I/O pins is shared with SO and SI.

Serial Input / Output Pins (SIO0, SIO1, SIO2, SIO3: SQI Mode)

The SIO0 through SIO3 pins are used for Quad SPI mode of operation. Because of the shared functionality of these pins the HOLD# feature is not available when using Quad SPI mode (Hold# →SIO3 in Quad SPI mode)

DNU/SIO2 (Do Not Use or SIO2)

Pin 3 is DNU (Do No Use) in SPI mode and SDI mode. SIO3 in SQI mode.

FUNCTION DESCRIPTION

Serial SRAM is designed to interface directly with the Serial Peripheral Interface (SPI). It can also interface with Multi-IO SPI interface (Dual SPI and Quad SPI).

The device contains an 8-bit instruction register. The device is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The CS# pin must be low for the entire operation.

All instructions, addresses and data are transferred MSB first, LSB last.

OPERATION MODE

The device has three modes of operation that are selected by setting bits 7 and 6 in the MODE register. The modes of operation are Byte, Page and Sequential.

Byte Operation

Byte Operation is selected when bits 7 and 6 in the MODE register are set to 00. In this mode, the read/ write operations are limited to only one byte. The Command followed by the 24-bit address is clocked into the device and the data to/from the device is transferred on the next eight clocks.

Page Operation

Page Operation is selected when bits 7 and 6 in the MODE register are set to 10. The device has 16,384 pages of 32 bytes. In this mode, the read and write operations are limited to within the addressed page (the address is automatically incremented internally). If the data being read or written reaches the page boundary, then the internal address counter will increment to the start of the page.

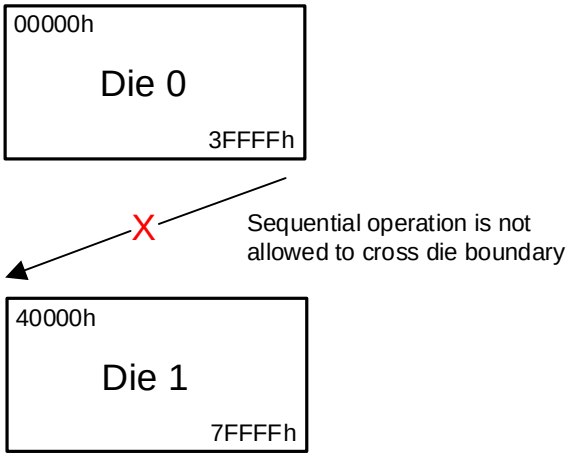
Sequential Operation

Sequential Operation is selected when bits 7 and 6 in the MODE register are set to 01. Sequential operation allows the entire array to be written to and read from. The internal address counter is automatically incremented until reaches the end of die boundary.

The device is stacked with 2-die, so it has a restriction in sequential operation: The address counter cannot cross the die boundary.

When the Address Pointer reaches the highest address of first die (3FFFFh), the address counter cannot cross to first address of 2nd die (40000h). Instead, it rolls over to (00000h). So the sequential operation must be terminated at the last address of first die (Die 0) by CS# HIGH, and begin new sequential operation from first address (40000h) of second die (Die 1) by CS# LOW.

MEMORY ARRAY SEGMENTS



WRITE MODE

Prior to any attempt to write data to the device, the device must be selected by bringing CS# low. Once the device is selected, the Write command can be started by issuing a WRITE instruction, followed by the 24-bit address, with the first five MSB's of the address being a "don't care" bit, and then the data to be written. A write is terminated by the CS# being brought high.

If operating in Page mode, after the initial data byte is shifted in, additional bytes can be shifted into the device. The Address Pointer is automatically incremented. This operation can continue for the entire page (32 bytes) before data will start to be overwritten.

If operating in Sequential mode, after the initial data byte is shifted in, additional bytes can be clocked into the Device. The internal Address Pointer is automatically incremented until reaches to die boundary address.

READ MODE

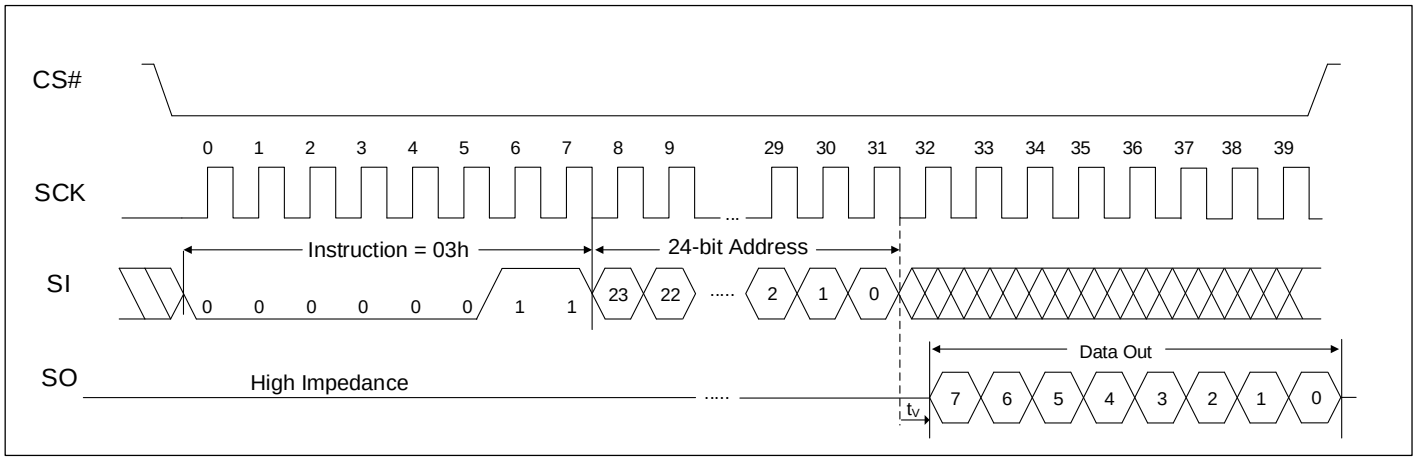
The device is selected by pulling CS# Low. Then 8 bit instruction is transmitted to the device followed by the 24 bit address, with the first five MSB's of the address being a "don't care" bit.

After the correct READ instruction and address are sent, the data stored in the memory at the selected address is shifted out on the SO pin. If operating in Sequential mode, the data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses until reaches to die boundary address.

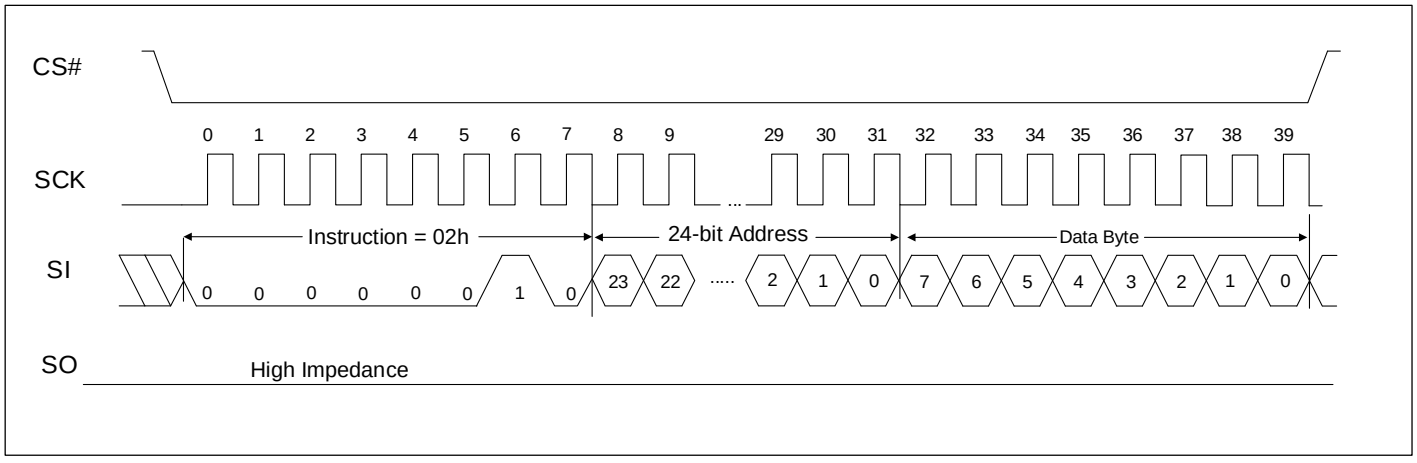
INSTRUCTION SET

Instruction Name	Instruction Format	Hex Code	Description
READ	0000 0011	0x03	Read data from memory array beginning at selected address
WRITE	0000 0010	0x02	Write data to memory array beginning at selected address
ESDI	0011 1011	0x3B	Enter SDI mode
ESQI	0011 1000	0x38	Enter SQI mode
RSTDQI	1111 1111	0xFF	Reset SDI/SQI mode
RDMR	0000 0101	0x05	Read Mode Register
WRMR	0000 0001	0x01	Write Mode Register

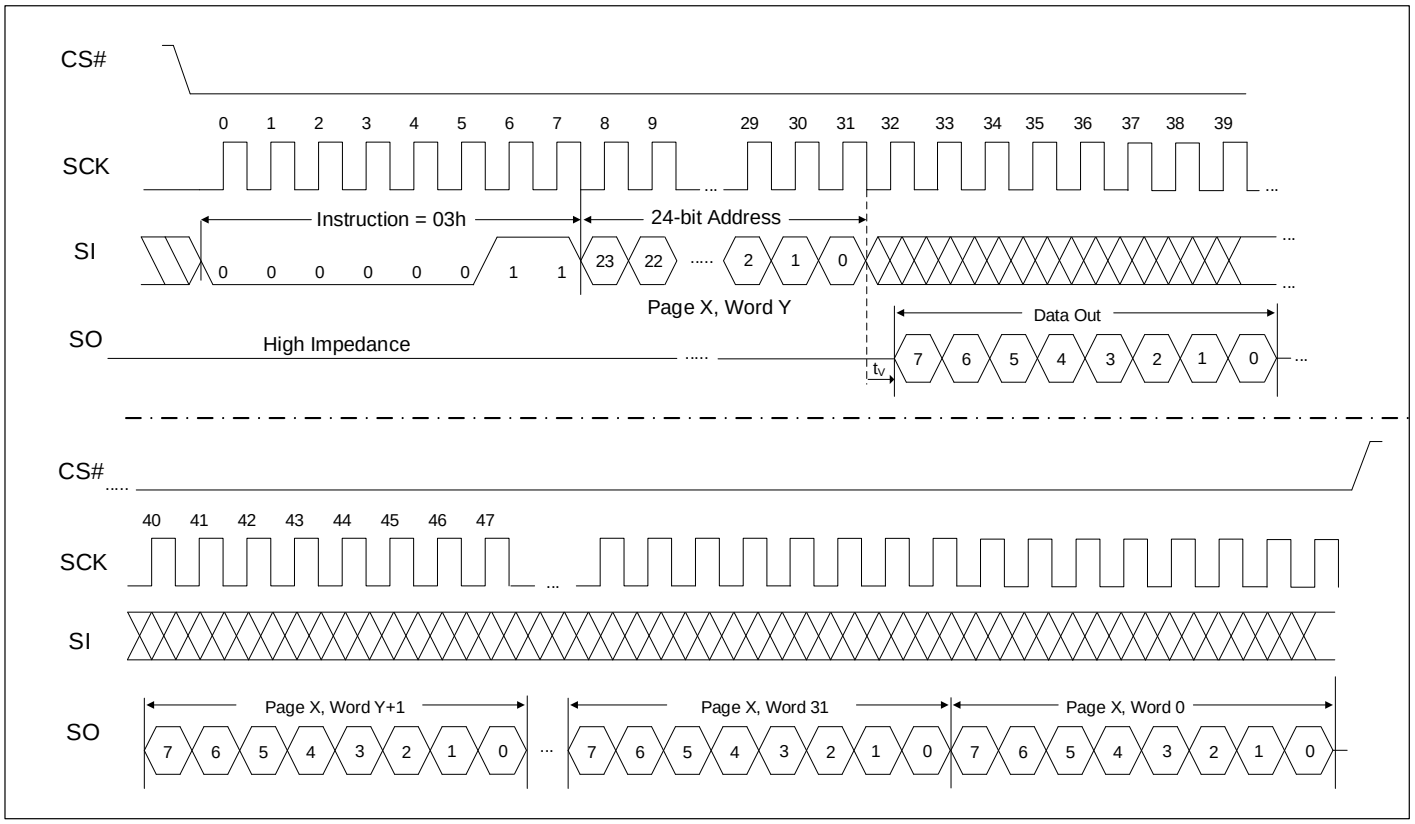
BYTE READ OPERATION (SPI MODE)



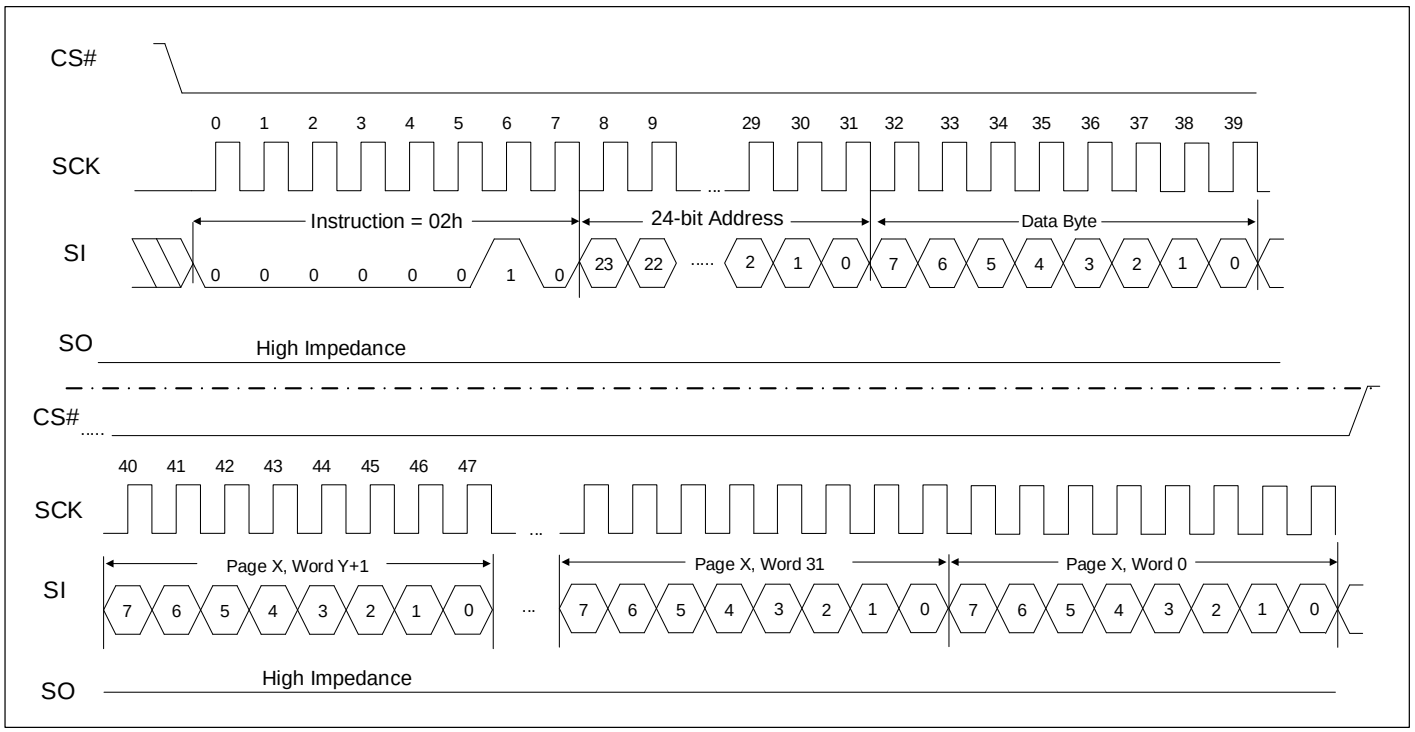
BYTE WRITE OPERATION (SPI MODE)



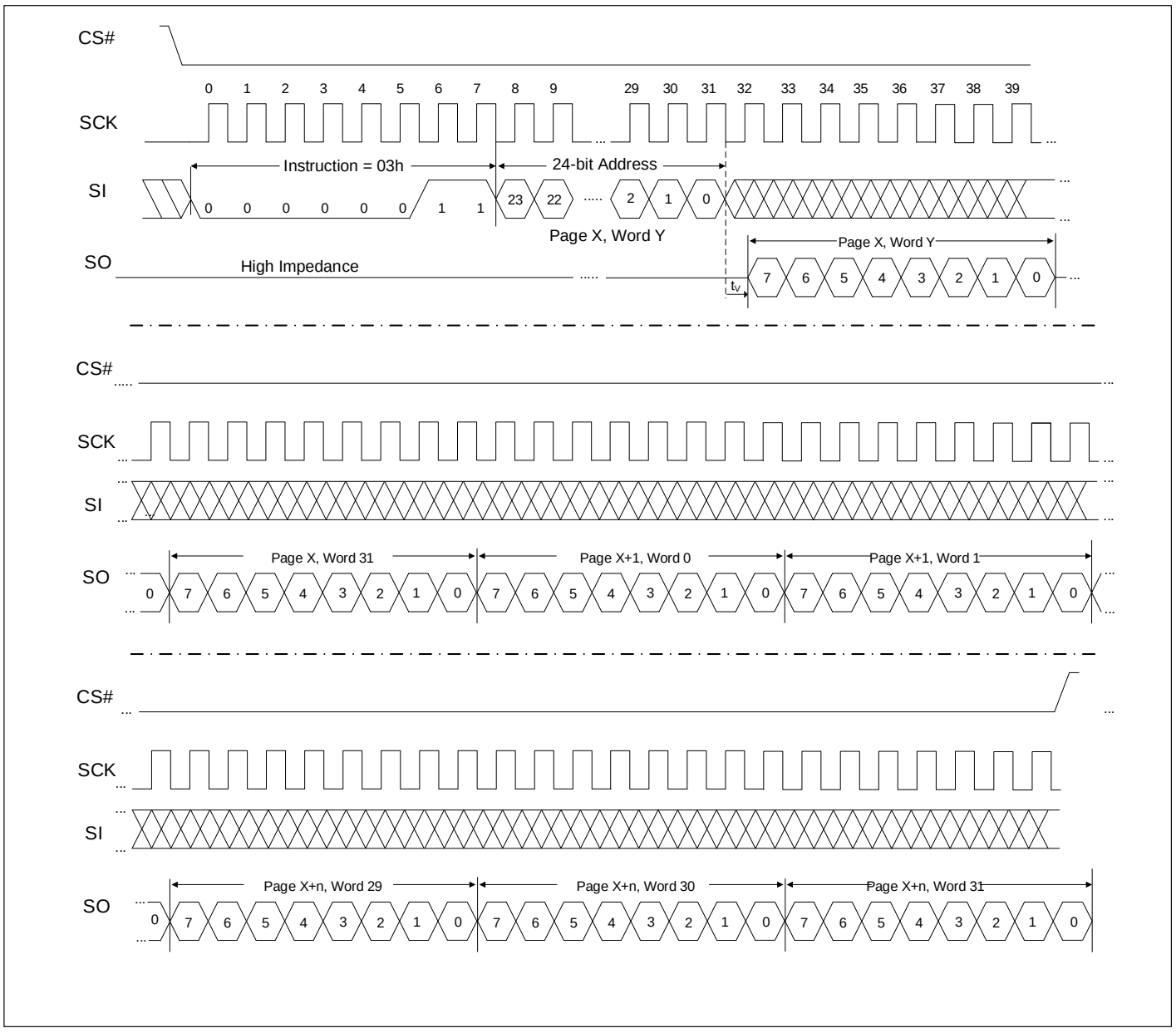
PAGE READ OPERATION (SPI MODE)



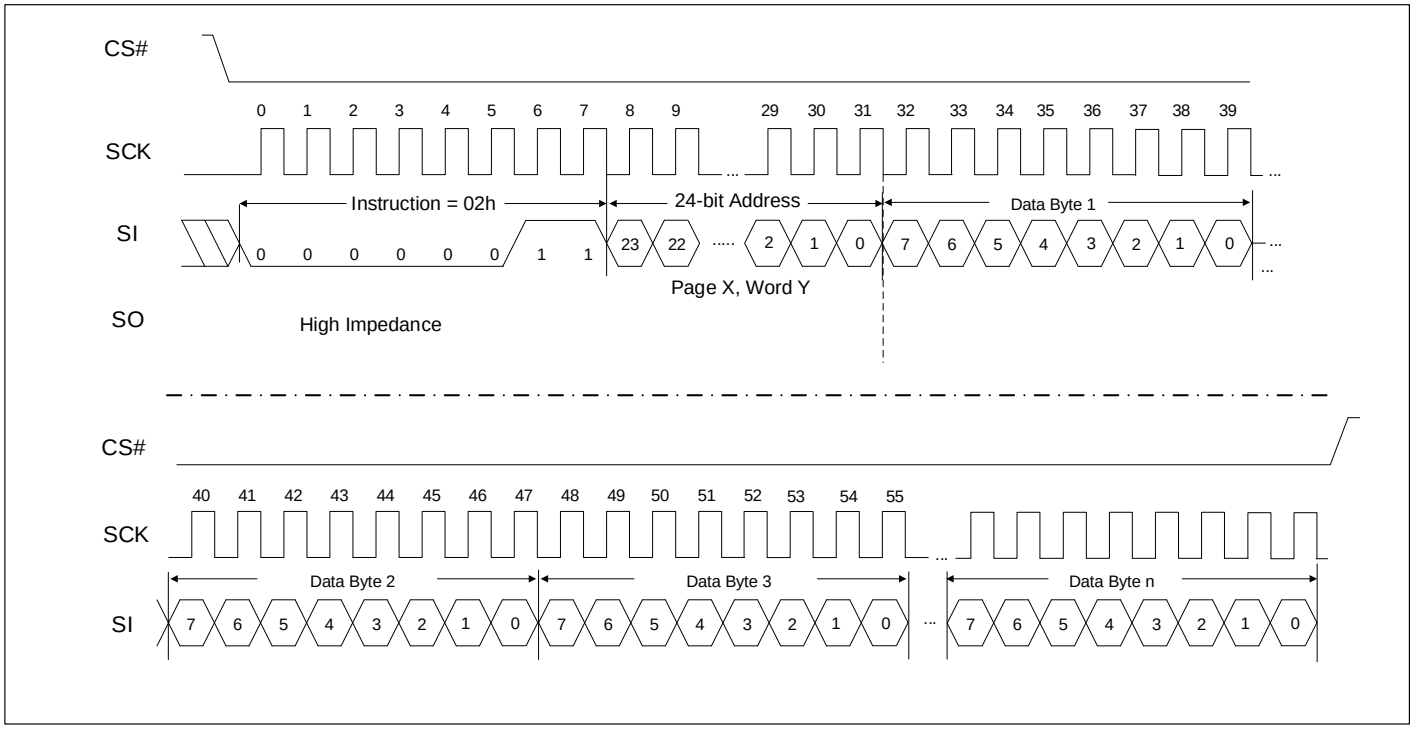
PAGE WRITE OPERATION (SPI MODE)



SEQUENTIAL READ OPERATION (SPI MODE)



SEQUENTIAL WRITE OPERATION (SPI MODE)



READ MODE REGISTER INSTRUCTION (RDMR)

The Read Mode Register instruction (RDMR: 05h) provides access to the MODE register. The MODE register may be read at any time. The MODE register is formatted as follows:

.

7	6	5	4	3	2	1	0
W/R		–	–	–	–	–	–
MODE		Reserved					
W/R = writable/readable							

The mode bits (7:6) indicate the operating mode of the SRAM. The possible modes of operation are:

0 0= Byte mode

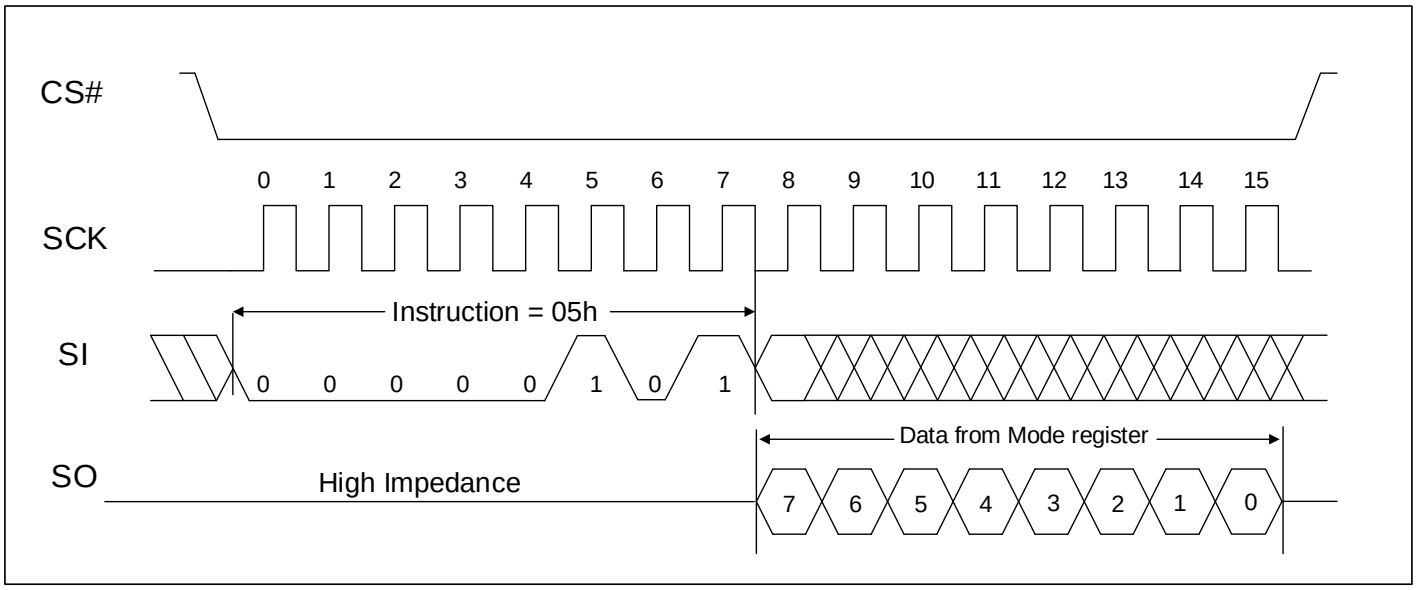
1 0= Page mode

0 1= Sequential mode (default operation)

1 1= Reserved

Bits 0 through 5 are reserved and should always be set to '0'.

READ MODE REGISTER OPERATION TIMING (RDMR)

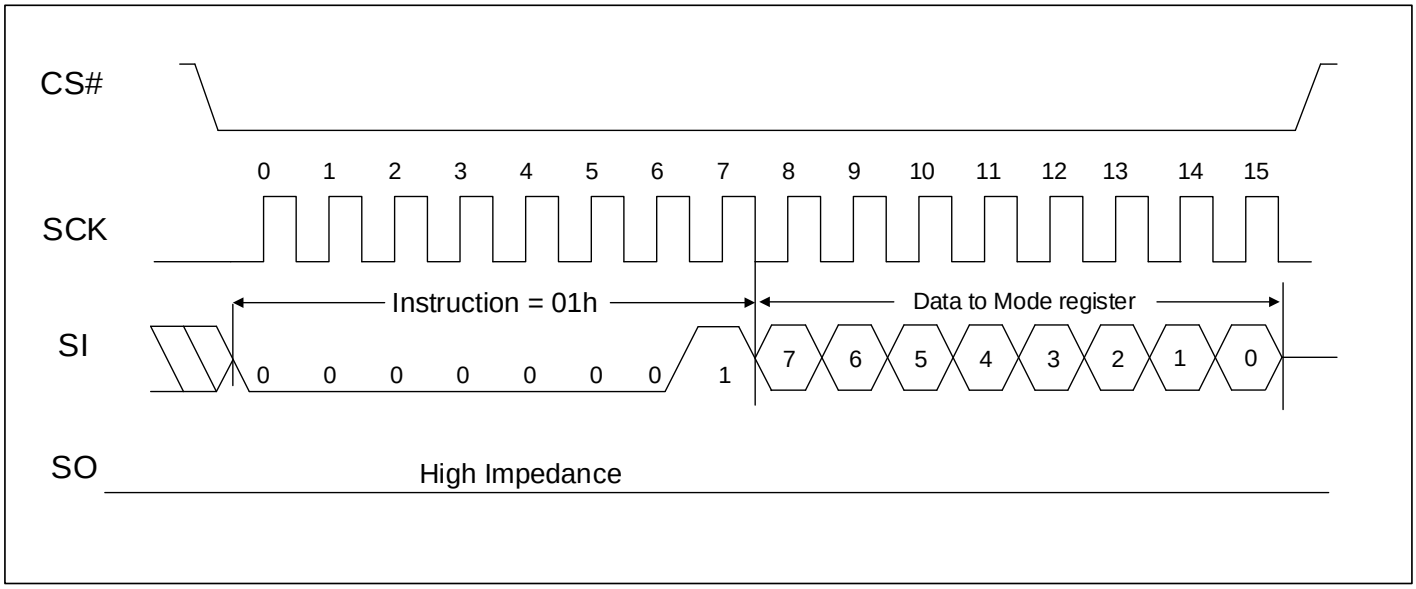


WRITE MODE REGISTER INSTRUCTION (WRMR)

The Write Mode Register instruction (WRMR: 01h) allows the user to write to the bits in the MODE register.

This allows for setting of the Device operating mode. Several of the bits in the MODE register must be cleared to '0'.

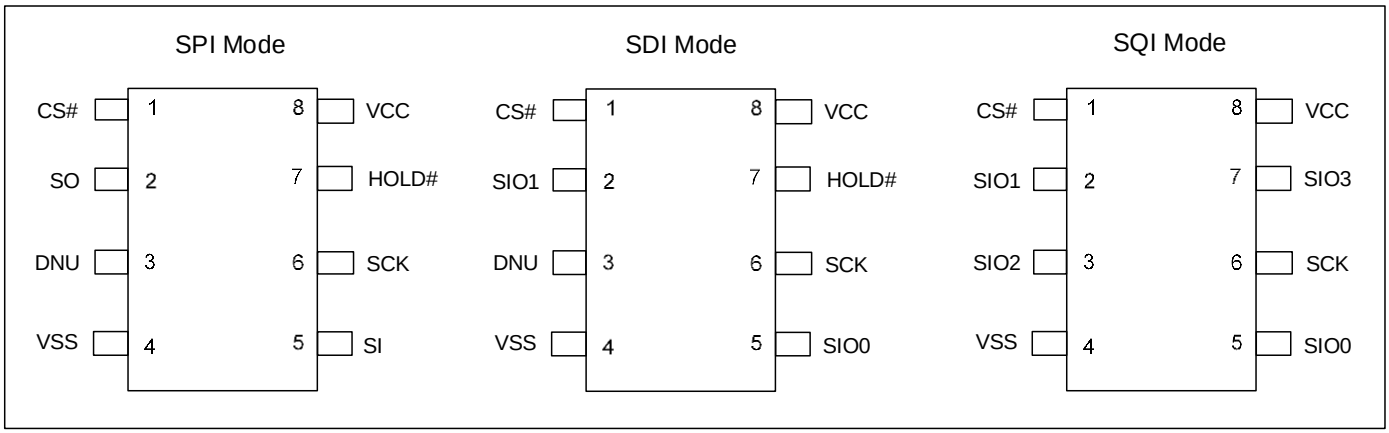
WRITE MODE REGISTER OPERATION TIMING (WRMR)



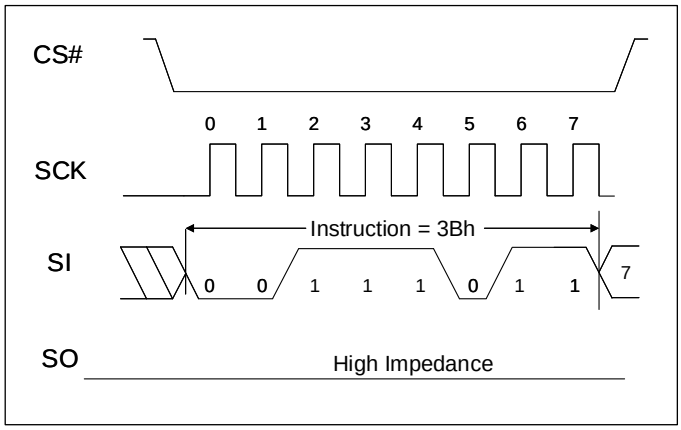
SDI MODE AND SQI MODE OPERATION

The device also supports SDI (Serial Dual Interface) and SQI (Serial Quad Interface) mode of operation when used with compatible master devices. To enter SDI mode, the ESDI command (3Bh) must be clocked in. As a convention for SDI mode of operation, two bits are entered per clock using the SIO0 and SIO1 pins. Bits are clocked MSB first.

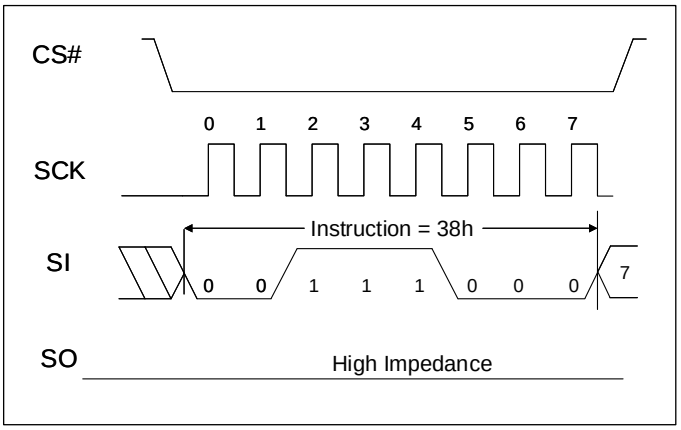
To enter SQI mode, the ESQI command (38h) must be clocked in. For SQI mode of operation, four bits of data are entered per clock, or one nibble per clock. The nibbles are clocked MSB first.



Enter SDI Mode

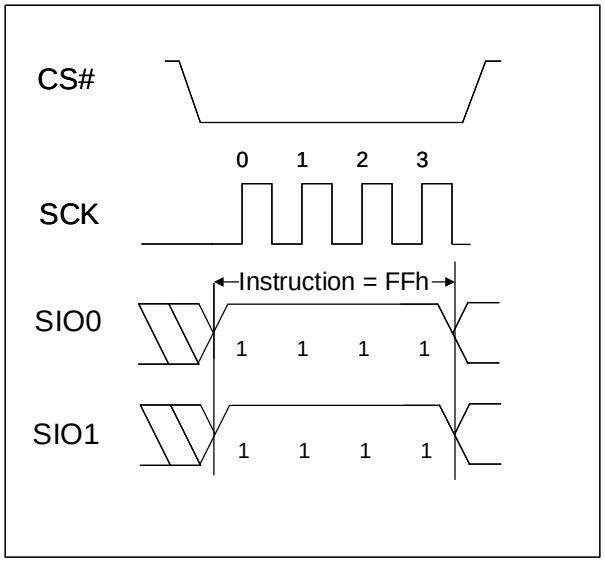


Enter SQI Mode

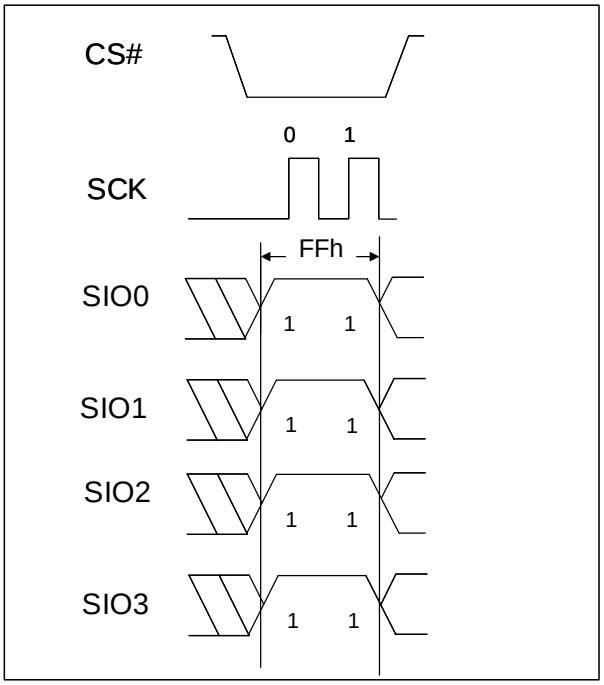


To exit from SDI mode, the RSTDQI command (FFh) must be issued. The command must be entered in the current device configuration, either SDI mode or SQI mode.

Reset SDI Mode



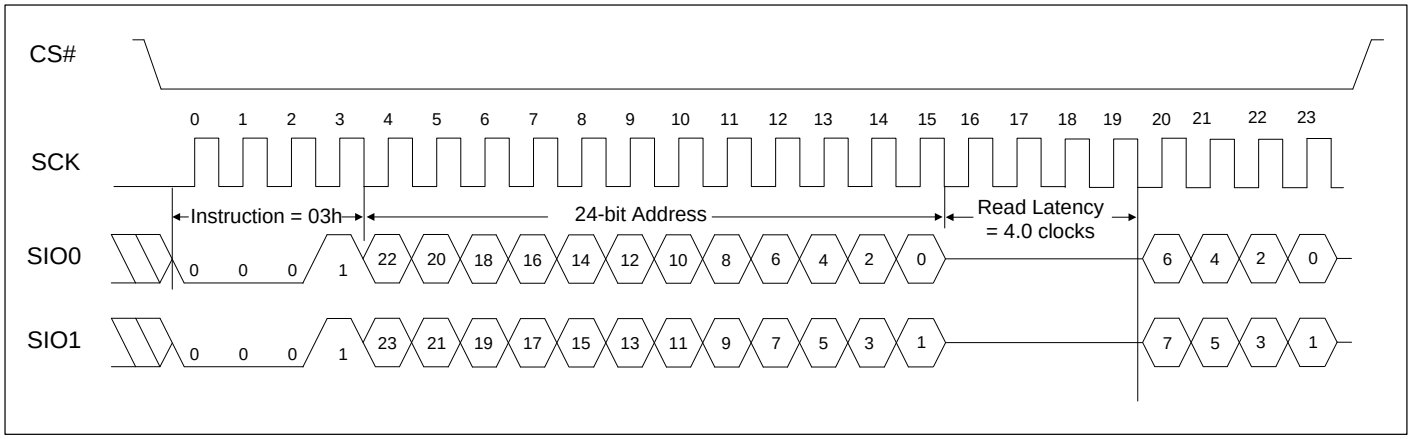
Reset SQI Mode



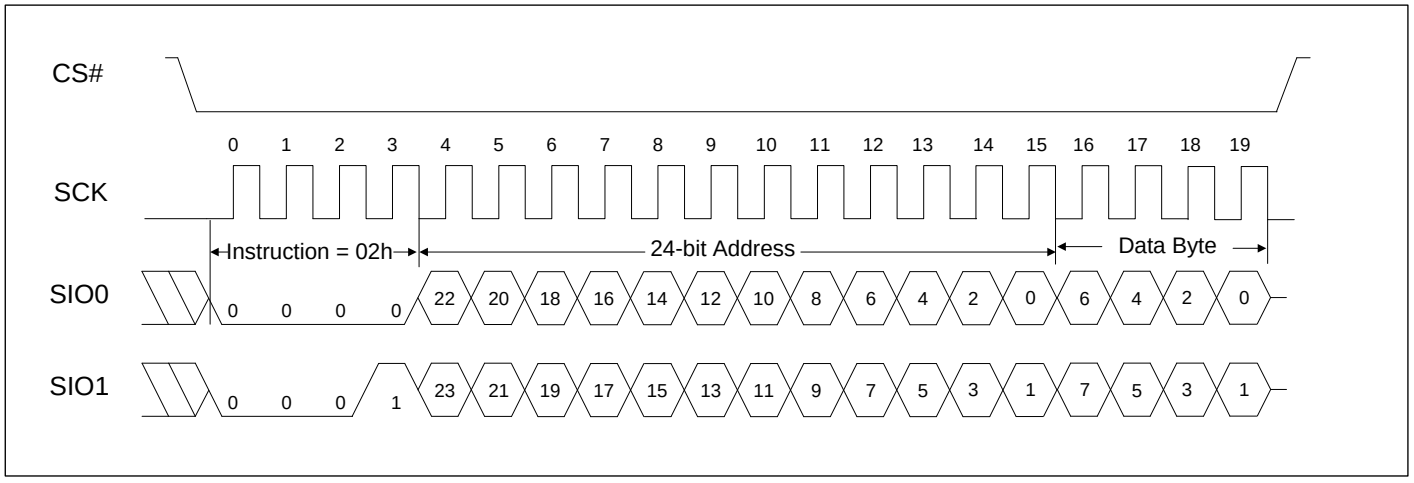
SDI (SERIAL DUAL INTERFACE) MODE OPERATION

The device supports Serial Dual Interface (SDI) mode of operation. There are 4.0 clock cycles (Dummy Byte) of Read Latency in SDI mode Byte Read Operation. No Write Latency in SDI Write Operation. It should be noted that if the MCU resets before the SRAM, the user will need to determine the serial mode of operation of the SRAM and reset it accordingly.

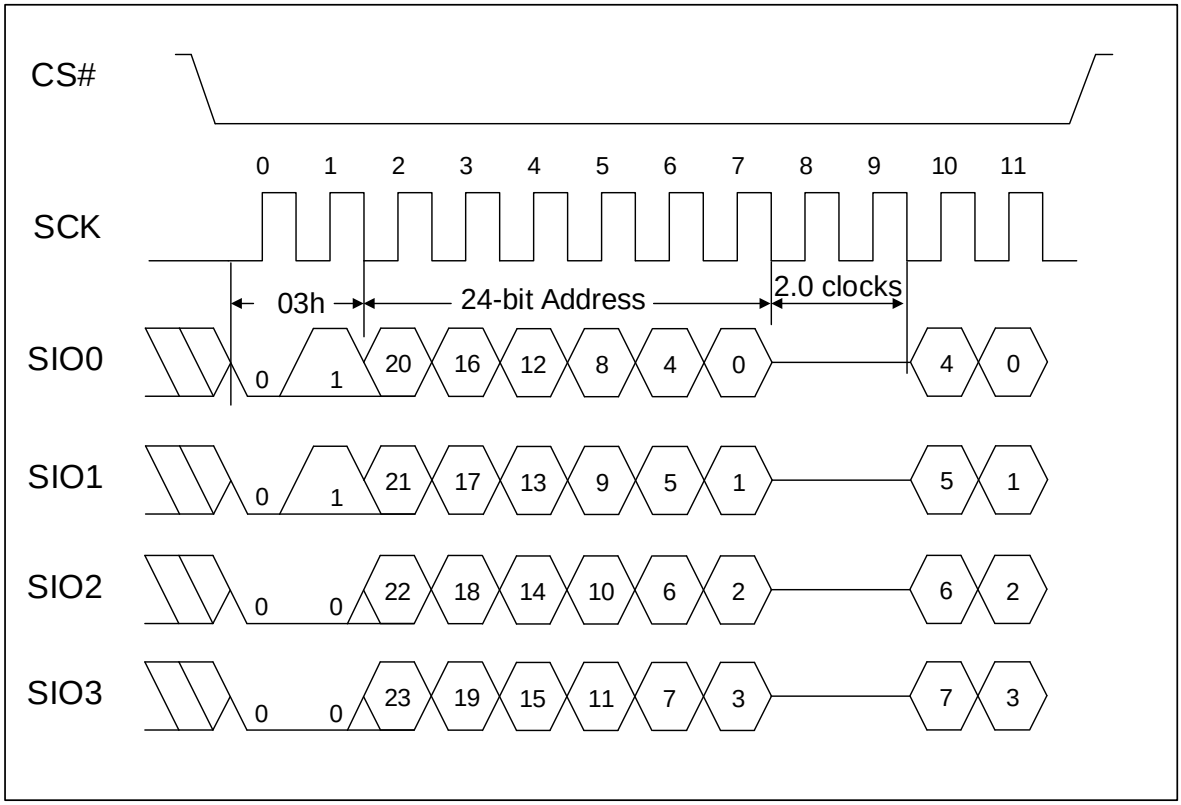
Byte Read Operation in SDI Mode



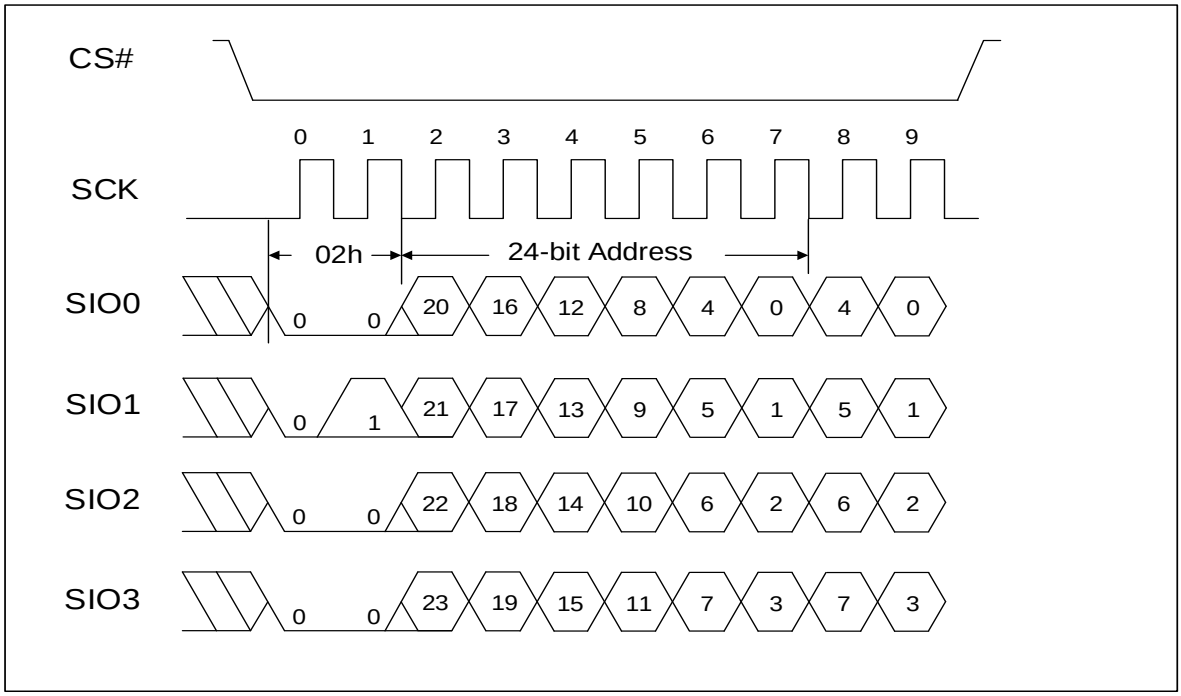
Byte Write Operation in SDI Mode



Byte Read Operation in SQI Mode



Byte Write Operation in SQI Mode



ABSOLUTE MAXIMUM RATINGS AND OPERATING RANGE

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter	Value	Unit
Vterm	Terminal Voltage with Respect to GND	–0.2 to +3.9(V_{DD}+0.3V)	V
tBIAS	Temperature Under Bias	–55 to +125	°C
V_{DD}	V_{DD} Related to GND	–0.2 to +3.9(V_{DD}+0.3V)	V
tStg	Storage Temperature	–65 to +150	°C

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE (1)

Range	Device Marking	Ambient Temperature	V_{DD}
Industrial	IS62WVS5128FALL	-40°C to +85°C	1.65V-2.2V
Industrial	IS62WVS5128FBLL	-40°C to +85°C	2.2V-3.6V
Automotive	IS65WVS5128FBLL	-40°C to +125°C	2.2V-3.6V

Note:

1. Full device AC operation assumes a 100 µs ramp time from 0 to Vcc(min) and 200 µs wait time after Vcc stabilization.

PIN CAPACITANCE (1)

Parameter	Symbol	Test Condition	Max	Units
Input capacitance (CS#, SCK)	C_{IN}	T_A = 25°C, f = 1 MHz, V_{DD} = V_{DD}(typ)	12	pF
Input/Output capacitance (other pins)	$C_{I/O}$		16	pF

Note:

1. These parameters are guaranteed by design and tested by a sample basis only.

AC TEST CONDITIONS (OVER THE OPERATING RANGE)

Parameter	Unit (1.65V~2.2V)	Unit (2.2V~2.7V)	Unit (2.7V~3.6V)
Input Pulse Level	0V to V_{DD}	0V to V_{DD}	0V to V_{DD}
Input Rise and Fall Time	1V/ns	1V/ns	1V/ns
Output Timing Reference Level	0.9V	½ V_{DD}	½ V_{DD}
R1	13500	16667	1103
R2	10800	15385	1554
V_{TM}	1.8V	V_{DD}	V_{DD}
Output Load Conditions		Refer to Figure 1 and 2	

OUTPUT LOAD CONDITIONS FIGURES

Figure1

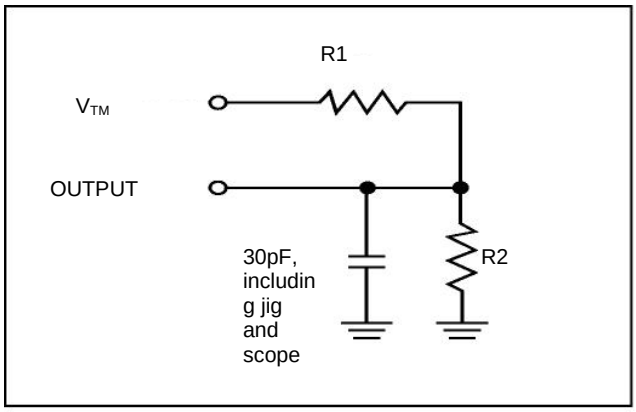
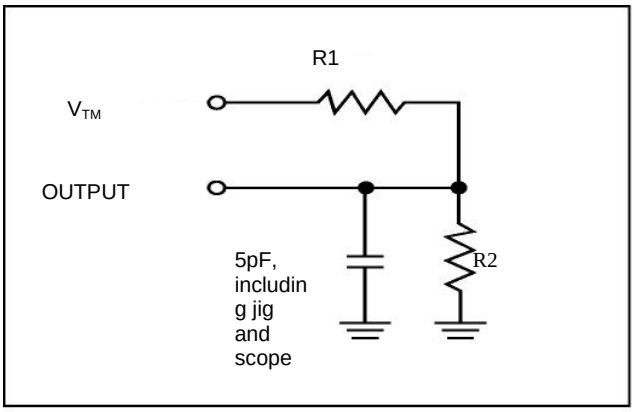


Figure2



ELECTRICAL CHARACTERISTICS

IS62WVS2568FALL DC ELECTRICAL CHARACTERISTICS-I (OVER THE OPERATING RANGE) VDD=1.65V~2.2V

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -0.1 mA	1.4	-	-	V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	-	-	0.2	V
V_{IH}(1)	Input HIGH Voltage		1.4	-	V_{DD} + 0.2	V
V_{IL}(1)	Input LOW Voltage		–0.2	-	0.4	V
V_{DR}(2)	Data Retention Voltage		-	1.0	-	V
I_{LI}	Input Leakage	GND < V_{IN} < V_{DD}	–1	-	1	µA
I_{LO}	Output Leakage	GND < V_{IN} < V_{DD}, Output Disabled	–1	-	1	µA

Notes:
1. VILL (min) = -1.0V AC (pulse width < 10ns). Not 100% tested.
   VIHH (max) = VDD + 1.0V AC (pulse width < 10ns). Not 100% tested.
2. This is the limit to which VDD can be lowered without losing RAM data at TA = 25°C. This parameter is periodically sampled and not 100% tested.

IS62 (5) WVS2568FBLL DC ELECTRICAL CHARACTERISTICS-I (OVER THE OPERATING RANGE) VDD=2.2V~3.6V

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	2.2 ≤ V_{DD} < 2.7, I_{OH} = -0.1 mA	2.0	-	-	V
		2.7 ≤ V_{DD} ≤ 3.6, I_{OH} = -1.0 mA	2.4	-	-	V
V_{OL}	Output LOW Voltage	2.2 ≤ V_{DD} < 2.7, I_{OL} = 0.1 mA	-	-	0.4	V
		2.7 ≤ V_{DD} ≤ 3.6, I_{OL} = 2.1 mA	-	-	0.4	V
V_{IH}(1)	Input HIGH Voltage	2.2 ≤ V_{DD} < 2.7	1.8	-	V_{DD} + 0.3	V
		2.7 ≤ V_{DD} ≤ 3.6	2.2	-	V_{DD} + 0.3	V
V_{IL}(1)	Input LOW Voltage	2.2 ≤ V_{DD} < 2.7	–0.3	-	0.6	V
		2.7 ≤ V_{DD} ≤ 3.6	–0.3	-	0.8	V
V_{DR}(2)	Data Retention Voltage		-	1.0	-	V
I_{LI}	Input Leakage	GND < V_{IN} < V_{DD}	–1	-	1	µA
I_{LO}	Output Leakage	GND < V_{IN} < V_{DD}, Output Disabled	–1	-	1	µA

Notes:
1. VILL (min) = -2.0V AC (pulse width < 10ns). Not 100% tested.
   VIHH (max) = VDD + 2.0V AC (pulse width < 10ns). Not 100% tested.
2. This is the limit to which VDD can be lowered without losing RAM data at TA = 25°C. This parameter is periodically sampled and not 100% tested.

IS62WVS5128FALL DC ELECTRICAL CHARACTERISTICS-II FOR POWER (OVER THE OPERATING RANGE)

Symbol	Parameter	Test Conditions	Grade	-16		Unit
				Typ.	Max.	
ICC	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max , f = f_{MAX} , CS# = V_{IL} I_{OUT} = 0 mA	Com.	-	14	mA
			Ind.		16	
ISB2	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max, f = 0, CS# ≥ V_{DD} - 0.2V VIN ≤ 0.2V or VIN ≥ V_{DD} - 0.2V	Com.	8	20	µA
			Ind.		40	µA

Note:
1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at TA = 25°C

IS62(5)WVS5128FBLL DC ELECTRICAL CHARACTERISTICS-II FOR POWER (OVER THE OPERATING RANGE)

Symbol	Parameter	Test Conditions	Grade	-20		-16		Unit
				Typ.	Max.	Typ.	Max.	
ICC	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max , f = f_{MAX} , CS# = V_{IL} I_{OUT} = 0 mA	Com.	-	14	-	14	mA
			Ind.		16		16	
			Auto.		26		26	
ISB2	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max, f = 0 CS# ≥ V_{DD} - 0.2V VIN ≤ 0.2V or VIN ≥ V_{DD} - 0.2V	Com.	8	20	-	20	µA
			Ind.		40		40	µA
			Auto.		72		72	µA

Note:
1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at TA = 25°C

AC CHARACTERISTICS (1) (OVER OPERATING RANGE)

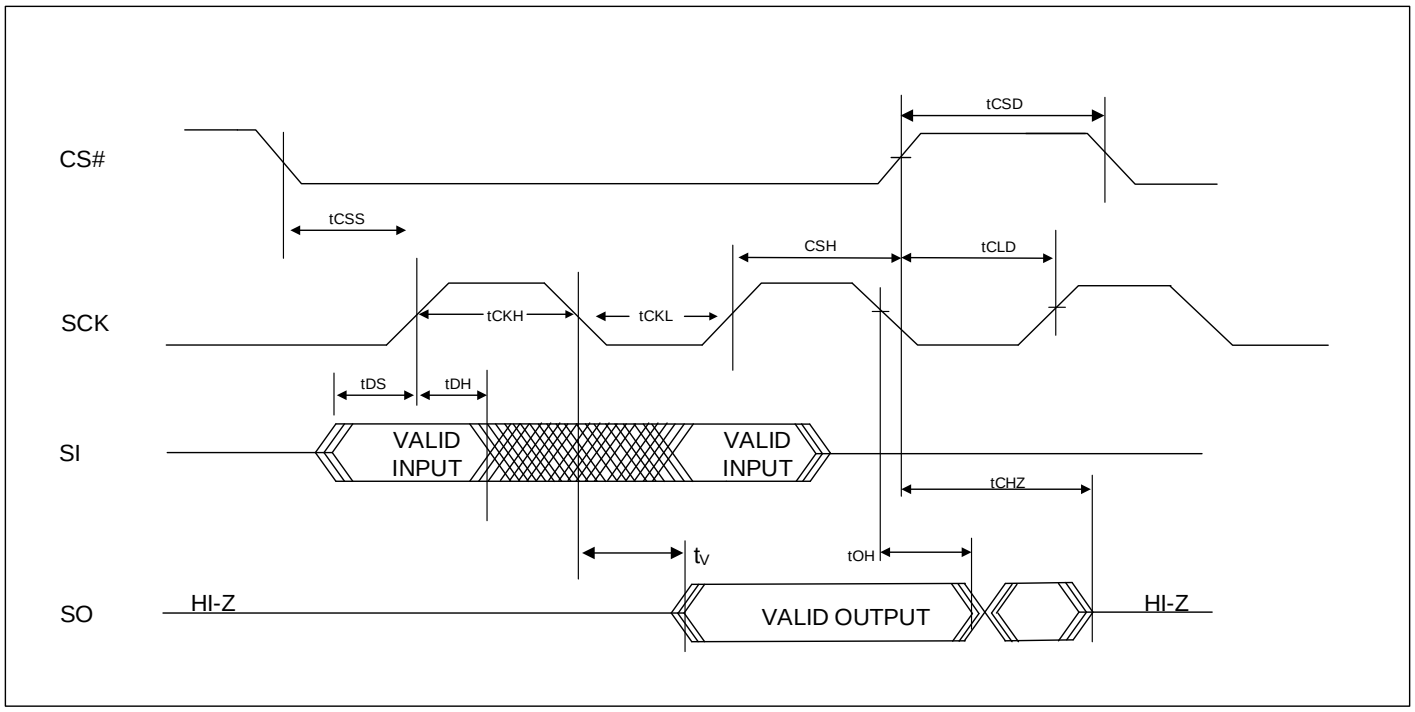
READ/WRITE CYCLE AC CHARACTERISTICS

Parameter	Symbol	-20		-16		unit	notes
		Min	Max	Min	Max		
Clock Frequency	FCLK	-	20	-	16	MHz	
CS# Setup Time	tCSS	25	-	32	-	ns	
CS# Hold Time	tCSH	50	-	50	-	ns	
CS# Disable Time	tCSD	25	-	32	-	ns	
Data Setup Time	tDS	10	-	10	-	ns	
Data Hold Time	tDH	10	-	10	-	ns	
Clock High Time	tCKH	23	-	32	-	ns	
Clock Low Time	tCKL	23	-	32	-	ns	
Clock Delay Time	tCLD	25	-	32	-	ns	
Output Valid from Clock Low	tV	-	25	-	36	ns	
Output Hold Time	tOH	0	-	0	-	ns	1
CS# High to Output High-Z	tCHZ	-	20	-	20	ns	1
HOLD# Setup Time	tHS	10	-	10	-	ns	
HOLD# Hold Time	tHH	10	-	10	-	ns	
HOLD# Low to Output High-Z	tHZ	-	20	-	20	ns	1
HOLD# High to Output Valid	tHV	-	50	-	50	ns	

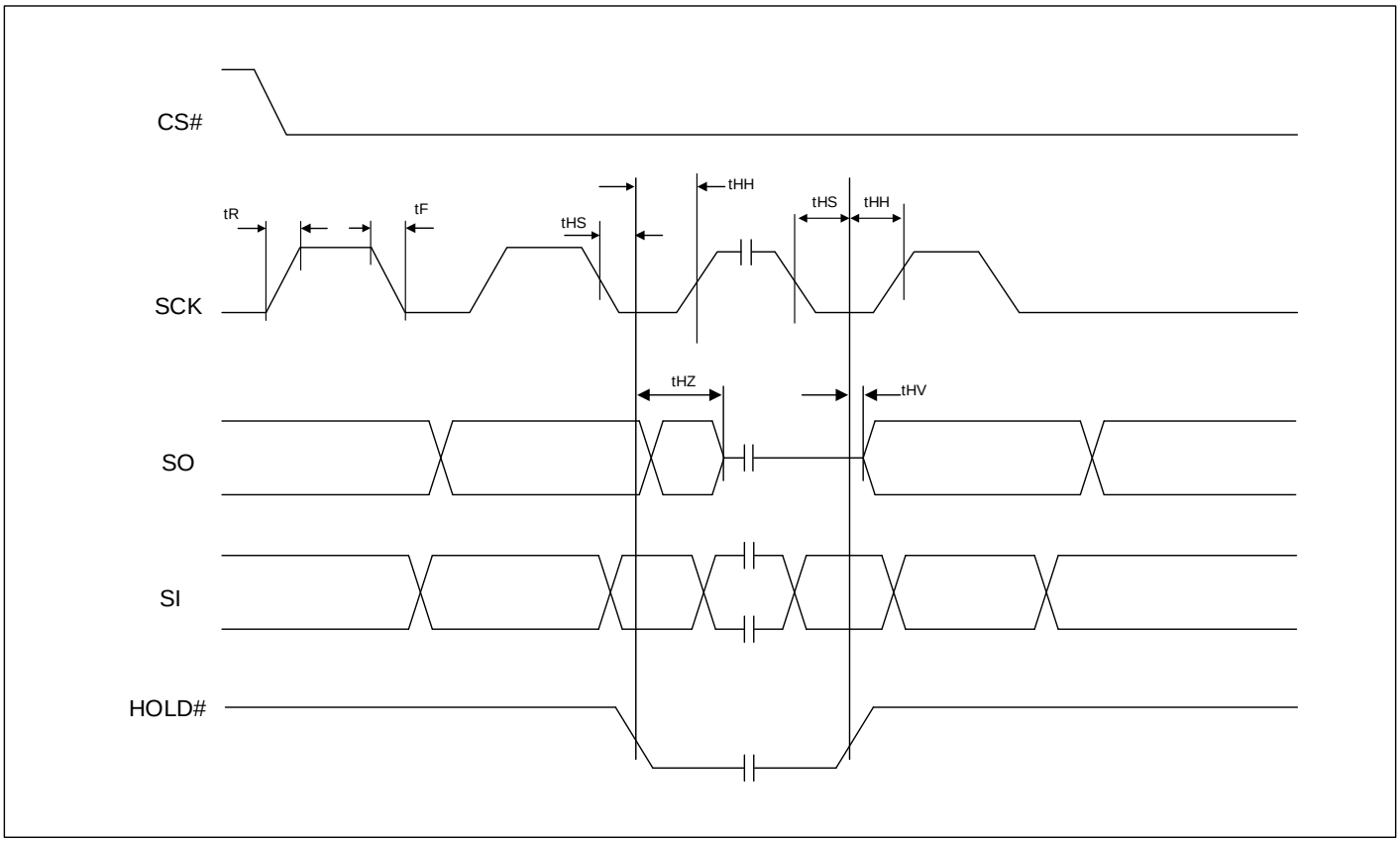
Note:
1. Not 100% tested.

TIMING DIAGRAM

Serial Input/Output Timing (SPI Mode)



HOLD Timing (SPI Mode)



ORDERING INFORMATION

IS62WVS5128FALL (1.65V - 2.2V)

Industrial Range: –40°C to +85°C

Speed (MHz)	Order Part No.	Package
16	IS62WVS5128FALL-16NLI	8-pin SOIC 150mil, Lead-free
16	IS62WVS5128FALL-16DLI	8-pin TSSOP, Lead-free
16	IS62WVS5128FALL-16BLI	24-ball TFBGA (6mm x 8mm), Lead-free

IS62WV5128FBLL (2.2V - 3.6V)

Industrial Range: –40°C to +85°C

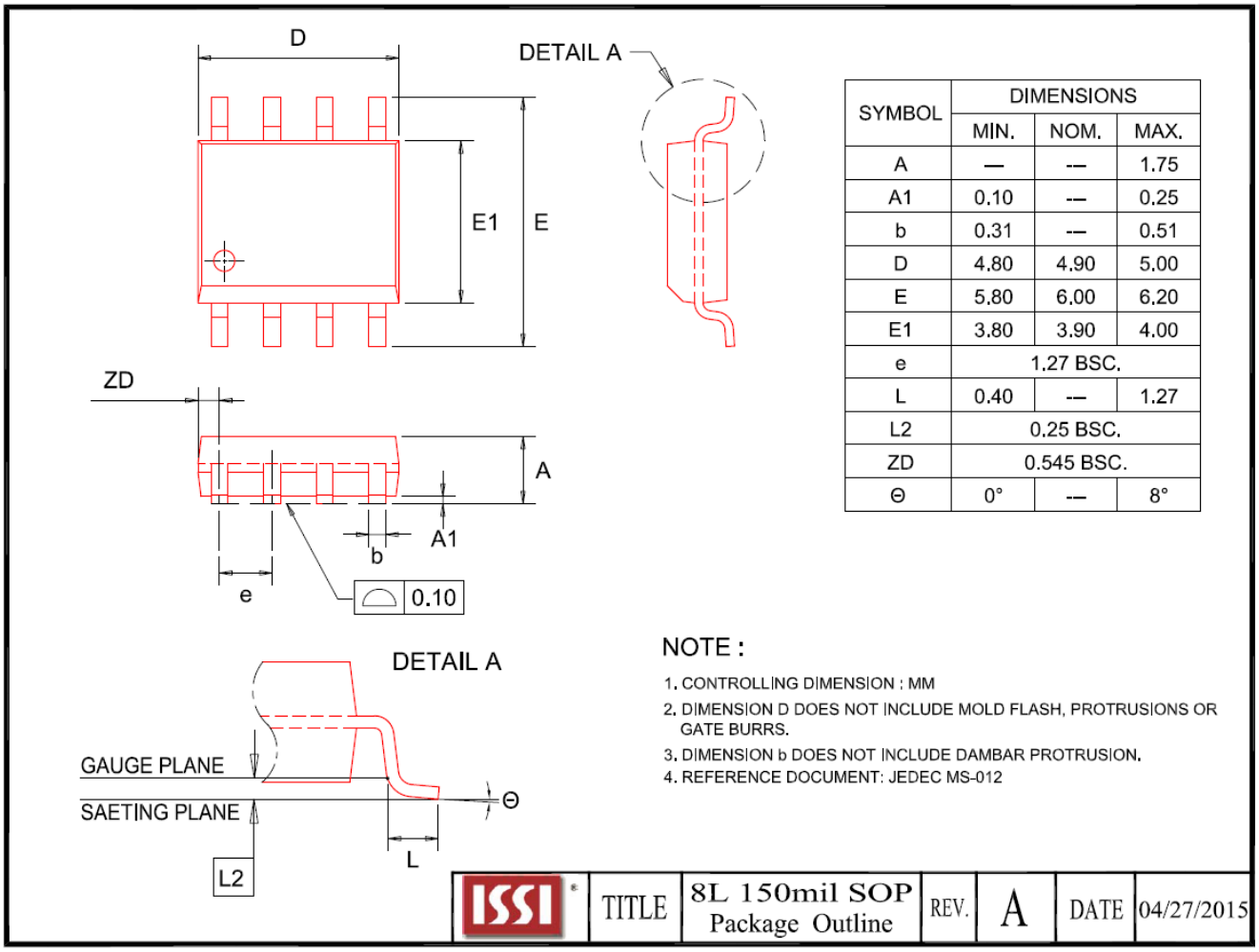
Speed (MHz)	Order Part No.	Package
20	IS62WVS5128FBLL-20NLI	8-pin SOIC 150mil, Lead-free
20	IS62WVS5128FBLL-20DLI	8-pin TSSOP, Lead-free
20	IS62WVS5128FBLL-20BLI	24-ball TFBGA (6mm x 8mm), Lead-free
16	IS62WVS5128FBLL-16NLI	8-pin SOIC 150mil, Lead-free
16	IS62WVS5128FBLL-16DLI	8-pin TSSOP, Lead-free
16	IS62WVS5128FBLL-16BLI	24-ball TFBGA (6mm x 8mm), Lead-free

Automotive Range (A3): –40°C to +125°C

Speed (MHz)	Order Part No.	Package
16	IS65WVS5128FBLL-16NLA3	8-pin SOIC 150mil, Lead-free
16	IS65WVS5128FBLL-16DLA3	8-pin TSSOP, Lead-free
16	IS65WVS5128FBLL-16BLA3	24-ball TFBGA (6mm x 8mm), Lead-free

PACKAGE INFORMATION

8-Pin SOIC 150MIL Package (N)



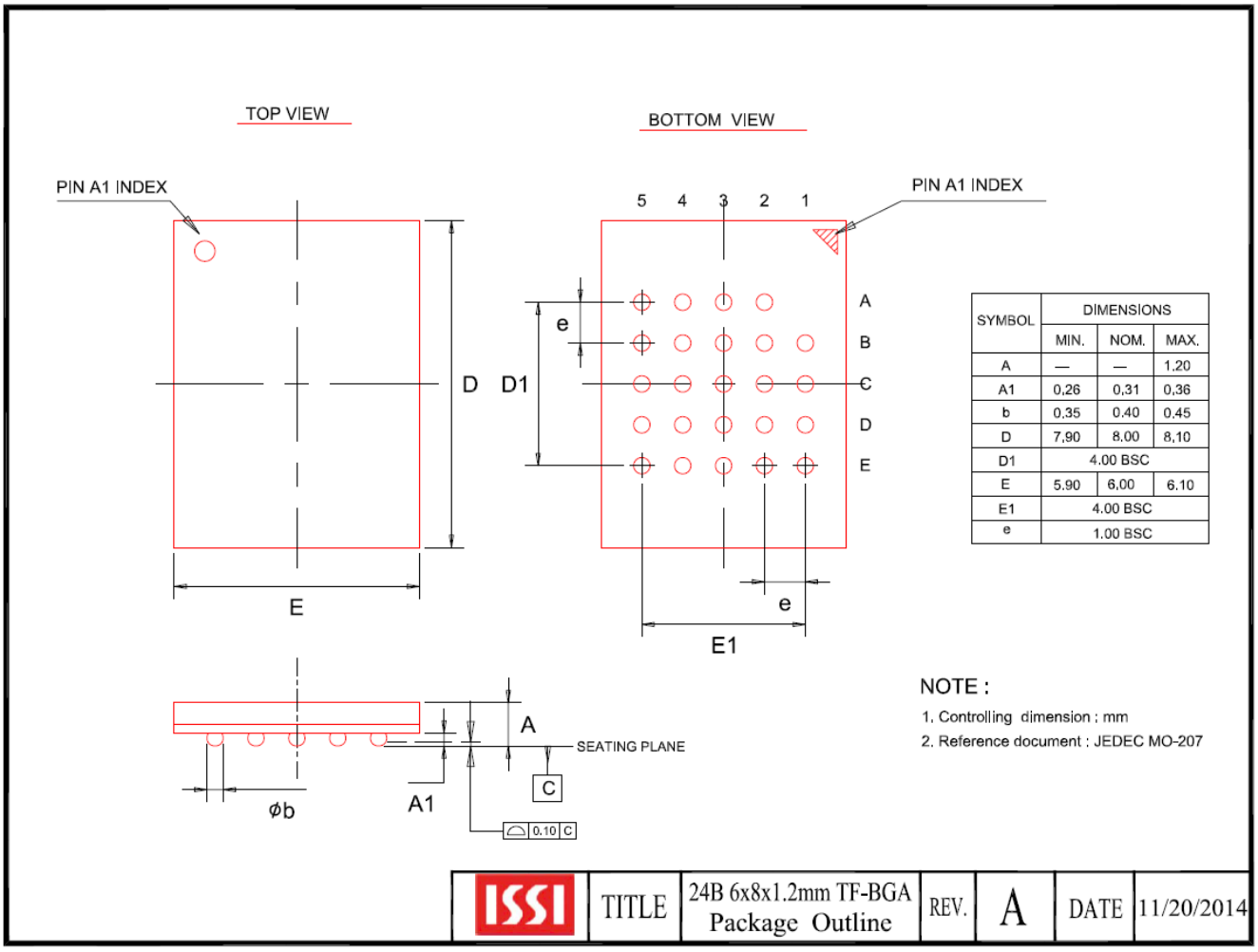
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	---	1.75
A1	0.10	---	0.25
b	0.31	---	0.51
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC.		
L	0.40	---	1.27
L2	0.25 BSC.		
ZD	0.545 BSC.		
Θ	0°	---	8°

NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
4. REFERENCE DOCUMENT: JEDEC MS-012

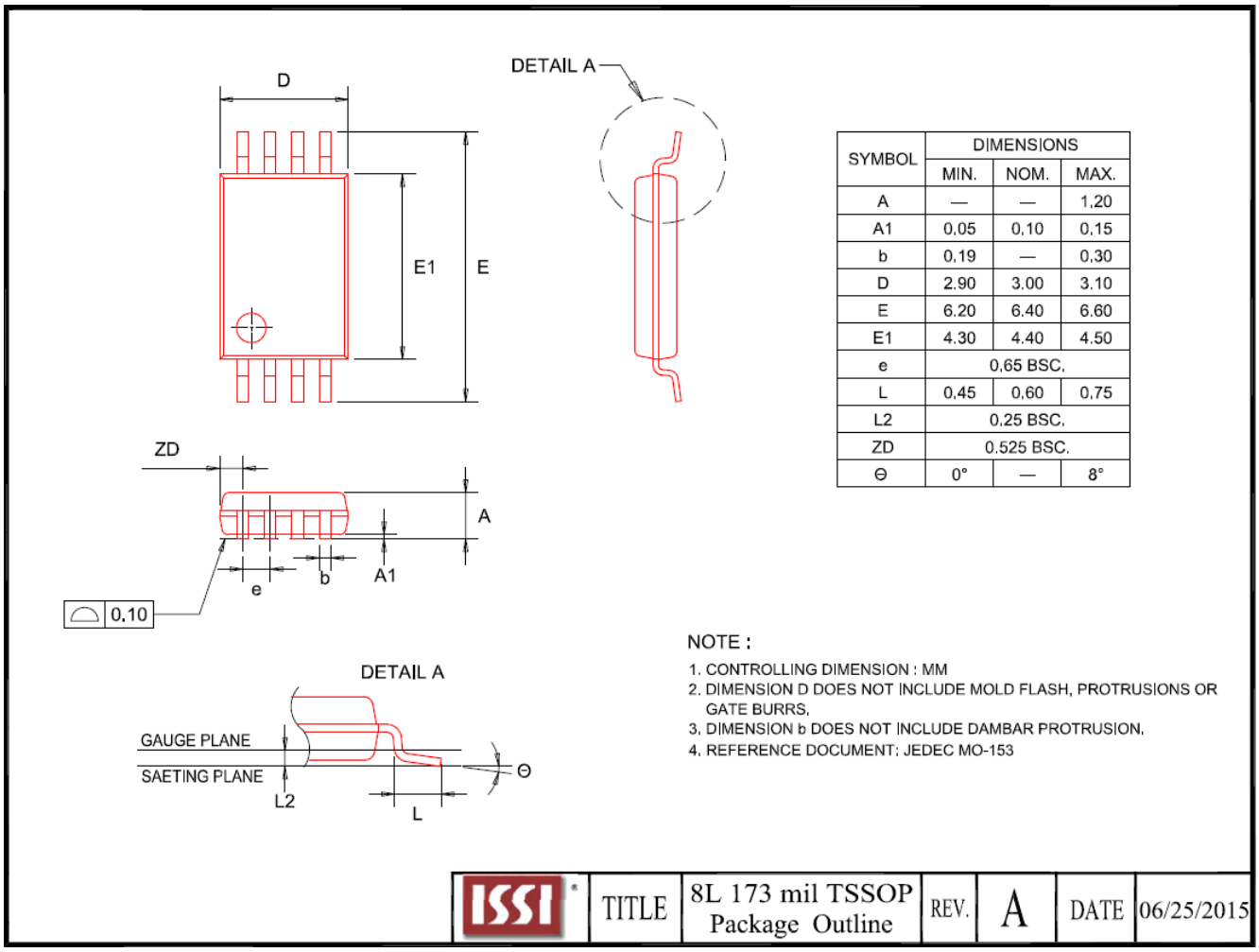
	TITLE	8L 150mil SOP Package Outline	REV.	A	DATE	04/27/2015

24-Ball TFBGA 6x8mm, 5x5 Ball Array (B)



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.26	0.31	0.36
b	0.35	0.40	0.45
D	7.90	8.00	8.10
D1		4.00 BSC	
E	5.90	6.00	6.10
E1		4.00 BSC	
e		1.00 BSC	

8-Pin TSSOP Package (D)



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.05	0.10	0.15
b	0.19	—	0.30
D	2.90	3.00	3.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65 BSC.		
L	0.45	0.60	0.75
L2	0.25 BSC.		
ZD	0.525 BSC.		
Θ	0°	—	8°

NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
4. REFERENCE DOCUMENT: JEDEC MO-153

	TITLE	8L 173 mil TSSOP Package Outline	REV.	A	DATE	06/25/2015