International Rectifier

PD-97268A

2N7632UC
IRHLUC7670Z4

RADIATION HARDENED LOGIC LEVEL POWER MOSFET SURFACE MOUNT (LCC-6)

60V, Combination 1N-1P-CHANNEL

R7™ TECHNOLOGY

Product Summary

Part Number	Radiation Level	$R_{DS(on)}$	I_D	CHANNEL
IRHLUC7670Z4	100K Rads (Si)	0.75Ω	0.89A	N
		1.60Ω	-0.65A	P
IRHLUC7630Z4	300K Rads (Si)	0.75Ω	0.89A	N
		1.60Ω	-0.65A	P

LCC-6

International Rectifier's R7™ Logic Level Power MOSFETs provide simple solution to interfacing CMOS and TTL control circuits to power devices in space and other radiation environments.The threshold voltage remains within acceptable operating limits over the full operating temperature and post radiation.This is achieved while maintaining single event gate rupture and single event burnout immunity.

The device is ideal when used to interface directly with most logic gates, linear IC's, micro-controllers, and other device types that operate from a 3.3-5V source. It may also be used to increase the output current of a PWM, voltage comparator or an operational amplifier where the logic level drive signal is available.

Features:

- 5V CMOS and TTL Compatible
- Low $R_{DS(on)}$
- Fast Switching
- Single Event Effect (SEE) Hardened
- Low Total Gate Charge
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Light Weight

Absolute Maximum Ratings (Per Die)

Pre-Irradiation

	Parameter	N-Channel	P-Channel	Units
I_D @ V_{GS} = ±4.5V, T_C= 25°C	Continuous Drain Current	0.89	-0.65	A
I_D @ V_{GS} = ±4.5V, T_C=100°C	Continuous Drain Current	0.56	-0.41	
I_{DM}	Pulsed Drain Current ①	3.56	-2.6	
P_D @ T_C = 25°C	Max. Power Dissipation	1.0	1.0	W
	Linear Derating Factor	0.01	0.01	W/°C
V_{GS}	Gate-to-Source Voltage	±10	±10	V
E_{AS}	Single Pulse Avalanche Energy	20 ②	34 ⑦	mJ
I_{AR}	Avalanche Current ①	0.89	-0.65	A
E_{AR}	Repetitive Avalanche Energy ①	0.1	0.1	mJ
dv/dt	Peak Diode Recovery dv/dt	4.7 ③	-5.6 ⑧	V/ns
T_J T_{STG}	Operating Junction Storage Temperature Range	-55 to 150		°C
	Pckg. Mounting Surface Temp.	300 (for 5s)		
	Weight	0.2 (Typical)		g

For footnotes refer to the last page

Electrical Characteristics For N-Channel Die @Tj = 25°C (Unless Otherwise specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	60	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta BV_{DSS}/\Delta T_J$	Temperature Coefficient of Breakdown Voltage	—	0.07	—	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.75	Ω	V_{GS} = 4.5V, I_D = 0.56A ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	V_{DS} = V_{GS}, I_D = 250µA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-4.5	—	mV/°C	
g_{fs}	Forward Transconductance	0.25	—	—	S	V_{DS} = 10V, I_{DS} = 0.56A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	1.0	µA	V_{DS}= 48V ,V_{GS}= 0V
		—	—	10		V_{DS} = 48V, V_{GS} = 0V, T_J =125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 10V
I_{GSS}	Gate-to-Source Leakage Reverse	—	—	-100		V_{GS} = -10V
Q_g	Total Gate Charge	—	—	3.6	nC	V_{GS} = 4.5V, I_D = 0.89A
Q_{gs}	Gate-to-Source Charge	—	—	1.5		V_{DS} = 30V
Q_{gd}	Gate-to-Drain ('Miller') Charge	—	—	1.8		
$t_{d(on)}$	Turn-On Delay Time	—	—	8.0	ns	V_{DD} = 30V, I_D = 0.89A,
t_r	Rise Time	—	—	15		V_{GS} = 5.0V, R_G = 24Ω
$t_{d(off)}$	Turn-Off Delay Time	—	—	30		
t_f	Fall Time	—	—	12		
$L_S + L_D$	Total Inductance	—	33	—	nH	Measured from the center of drain pad to center of source pad
C_{iss}	Input Capacitance	—	145	—	pF	V_{GS} = 0V, V_{DS} = 25V
C_{oss}	Output Capacitance	—	43	—		f = 1.0MHz
C_{rss}	Reverse Transfer Capacitance	—	2.5	—		
R_g	Gate Resistance	—	8.2	—	Ω	f = 1.0MHz, open drain

Source-Drain Diode Ratings and Characteristics (Per N Channel Die)

	Parameter	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	0.89	A	
I_{SM}	Pulse Source Current (Body Diode) ①	—	—	3.56		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	T_j = 25°C, I_S = 0.89A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	—	65	ns	T_j = 25°C, I_F = 0.89A, di/dt ≤ 100A/µs
Q_{RR}	Reverse Recovery Charge	—	—	67	nC	V_{DD} ≤ 25V ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

Thermal Resistance (Per N Channel Die)

	Parameter	Min	Typ	Max	Units	Test Conditions
R_{thJA}	Junction-to-Ambient	—	—	125	°C/W	Typical socket mount

Note: Corresponding Spice and Saber models are available on International Rectifier Website.
For footnotes refer to the last page

Electrical Characteristics For P-Channel Die @Tj = 25°C (Unless Otherwise specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-60	—	—	V	V_{GS} = 0V, I_D = -250μA
$\Delta BV_{DSS}/\Delta T_J$	Temperature Coefficient of Breakdown Voltage	—	-0.06	—	V/°C	Reference to 25°C, I_D = -1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	1.60	Ω	V_{GS} = -4.5V, I_D = -0.41A ④
$V_{GS(th)}$	Gate Threshold Voltage	-1.0	—	-2.0	V	V_{DS} = V_{GS}, I_D = -250μA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	3.6	—	mV/°C	
g_{fs}	Forward Transconductance	0.5	—	—	S	V_{DS} = -10V, I_{DS} = -0.41A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	-1.0	μA	V_{DS}= -48V ,V_{GS}= 0V
		—	—	-10		V_{DS} = -48V, V_{GS} = 0V, T_J =125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	V_{GS} = -10V
I_{GSS}	Gate-to-Source Leakage Reverse	—	—	100		V_{GS} = 10V
Q_g	Total Gate Charge	—	—	3.6	nC	V_{GS} = -4.5V, I_D = -0.65A V_{DS} = -30V
Q_{gs}	Gate-to-Source Charge	—	—	1.5		
Q_{gd}	Gate-to-Drain ('Miller') Charge	—	—	1.8		
$t_{d(on)}$	Turn-On Delay Time	—	—	23	ns	V_{DD} = -30V, I_D = -0.65A, V_{GS} = -5.0V, R_G = 24Ω
t_r	Rise Time	—	—	22		
$t_{d(off)}$	Turn-Off Delay Time	—	—	32		
t_f	Fall Time	—	—	26		
$L_S + L_D$	Total Inductance	—	33	—	nH	Measured from the center of drain pad to center of source pad
C_{iss}	Input Capacitance	—	147	—	pF	V_{GS} = 0V, V_{DS} = -25V f = 1.0MHz
C_{oss}	Output Capacitance	—	46	—		
C_{rss}	Reverse Transfer Capacitance	—	8.1	—		
R_g	Gate Resistance	—	52	—	Ω	f = 1.0MHz, open drain

Source-Drain Diode Ratings and Characteristics (Per P Channel Die)

	Parameter	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-0.65	A	
I_{SM}	Pulse Source Current (Body Diode) ①	—	—	-2.6		
V_{SD}	Diode Forward Voltage	—	—	-5.0	V	T_j = 25°C, I_S = -0.65A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	—	35	ns	T_j = 25°C, I_F = -0.65A, di/dt ≤ -100A/μs V_{DD} ≤ -25V ④
Q_{RR}	Reverse Recovery Charge	—	—	9.8	nC	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

Thermal Resistance (Per P Channel Die)

	Parameter	Min	Typ	Max	Units	Test Conditions
R_{thJA}	Junction-to-Ambient	—	—	125	°C/W	Typical socket mount

Note: Corresponding Spice and Saber models are available on International Rectifier Website.

For footnotes refer to the last page

Radiation Characteristics

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-39 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table 1. Electrical Characteristics For N-Channel Device @Tj = 25°C, Post Total Dose Irradiation ⑤⑥

	Parameter	Upto 300K Rads (Si)[1] Min	Max	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	60	—	V	$V_{GS} = 0V$, $I_D = 250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	1.0	2.0		$V_{GS} = V_{DS}$, $I_D = 250\mu A$
I_{GSS}	Gate-to-Source Leakage Forward	—	100	nA	$V_{GS} = 10V$
I_{GSS}	Gate-to-Source Leakage Reverse	—	-100		$V_{GS} = -10V$
I_{DSS}	Zero Gate Voltage Drain Current	—	1.0	µA	$V_{DS}= 48V$, $V_{GS}= 0V$
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-39)	—	0.60	Ω	$V_{GS} = 4.5V$, $I_D = 0.56A$
$R_{DS(on)}$	Static Drain-to-Source On-state ④ Resistance (LCC-6)	—	0.75	Ω	$V_{GS} = 4.5V$, $I_D = 0.56A$
V_{SD}	Diode Forward Voltage ④	—	1.2	V	$V_{GS} = 0V$, $I_D = 0.89A$

1. Part numbers IRHLUC7670Z4, IRHLUC7630Z4

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

LET (MeV/(mg/cm^2))	Energy (MeV)	Range (µm)	VDS (V) @VGS= 0V	@VGS= -2V	@VGS= -4V	@VGS= -5V	@VGS= -6V	@VGS= -7V
38 ± 5%	300 ± 7.5%	38 ± 7.5%	60	60	60	60	60	35
62 ± 5%	355 ± 7.5%	33 ± 7.5%	60	60	60	60	30	-
85 ± 5%	380 ± 7.5%	29 ± 7.5%	60	60	60	40	-	-

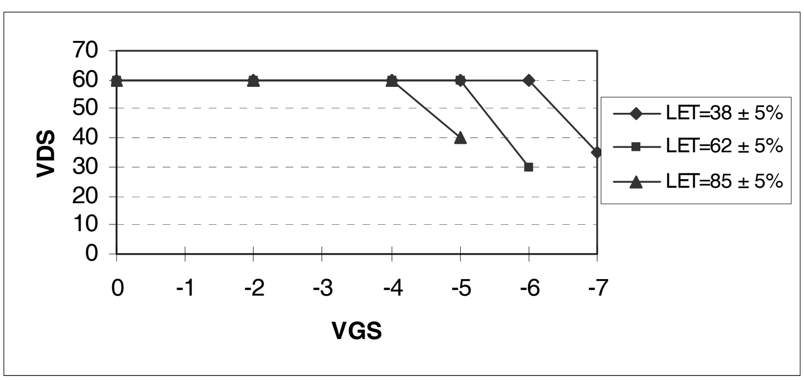


Fig a. Typical Single Event Effect, Safe Operating Area

For footnotes refer to the last page

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-39 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table 1. Electrical Characteristics For P-Channel Device @Tj = 25°C, Post Total Dose Irradiation ⑤⑥

	Parameter	Upto 300K Rads (Si)[1] Min	Max	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-60	—	V	V_{GS} = 0V, I_D = -250µA
$V_{GS(th)}$	Gate Threshold Voltage	-1.0	-2.0		$V_{GS} = V_{DS}$, I_D = -250µA
I_{GSS}	Gate-to-Source Leakage Forward	—	-100	nA	V_{GS} = -10V
I_{GSS}	Gate-to-Source Leakage Reverse	—	100		V_{GS} = 10V
I_{DSS}	Zero Gate Voltage Drain Current	—	-1.0	µA	V_{DS}= -48V, V_{GS}= 0V
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-39)	—	1.40	Ω	V_{GS} = -4.5V, I_D = -0.41A
$R_{DS(on)}$	Static Drain-to-Source On-state ④ Resistance (LCC-6)	—	1.60	Ω	V_{GS} = -4.5V, I_D = -0.41A
V_{SD}	Diode Forward Voltage ④	—	-5.0	V	V_{GS} = 0V, I_D = -0.65A

1. Part numbers IRHLUC7670Z4, IRHLUC7630Z4

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

LET (MeV/(mg/cm^2))	Energy (MeV)	Range (µm)	VDS (V) @VGS= 0V	@VGS= 2V	@VGS= 4V	@VGS= 5V	@VGS= 6V	@VGS= 7V
38 ± 5%	300 ± 7.5%	38 ± 7.5%	-60	-60	-60	-60	-60	-50
62 ± 5%	355 ± 7.5%	33 ± 7.5%	-60	-60	-60	-60	-60	-
85 ± 5%	380 ± 7.5%	29 ± 7.5%	-60	-60	-60	-60	-	-

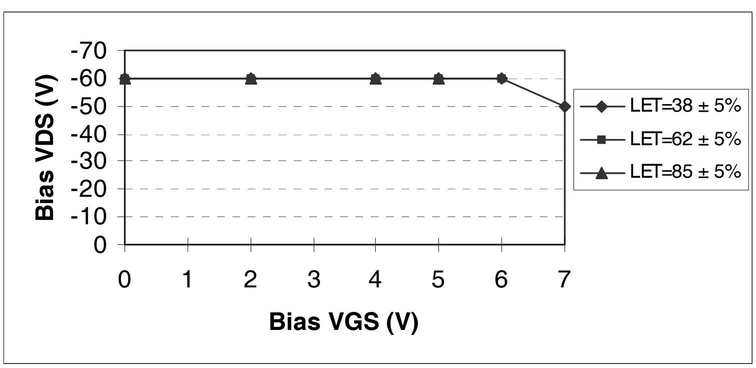


Fig a. Typical Single Event Effect, Safe Operating Area

For footnotes refer to the last page

N-Channel
Die 1

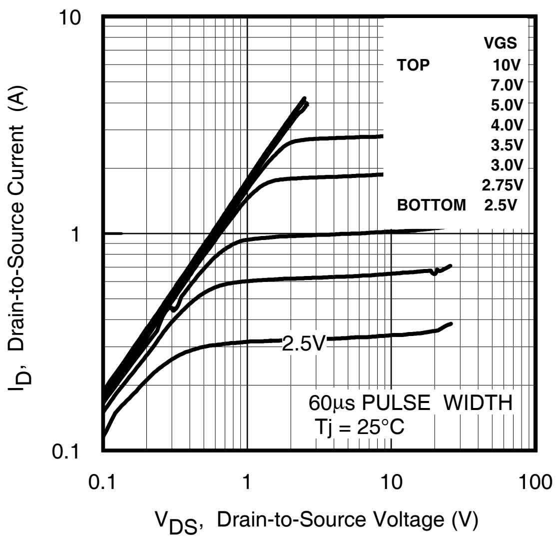


Fig 1. Typical Output Characteristics

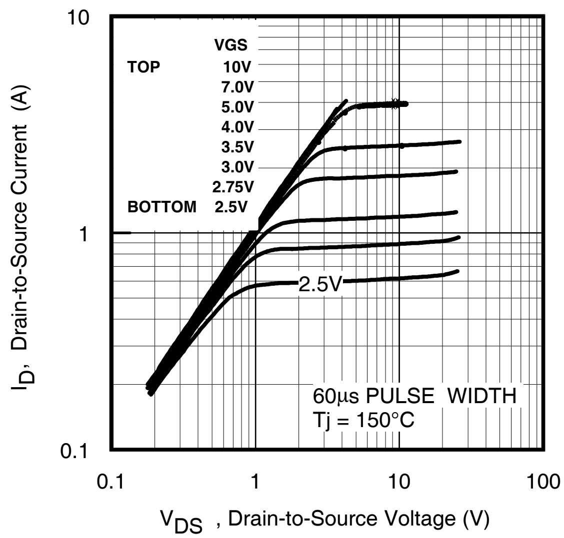


Fig 2. Typical Output Characteristics

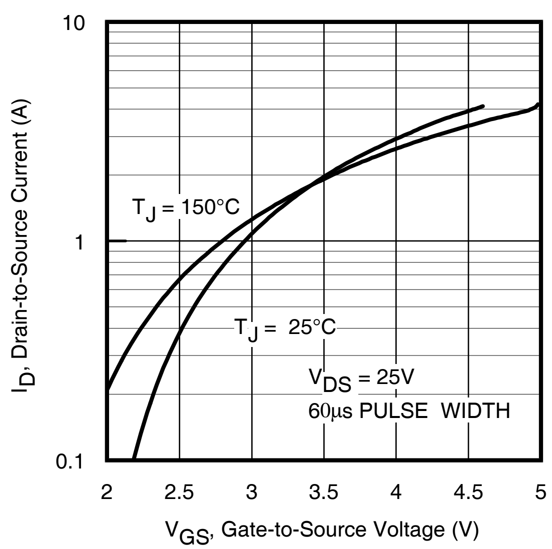


Fig 3. Typical Transfer Characteristics

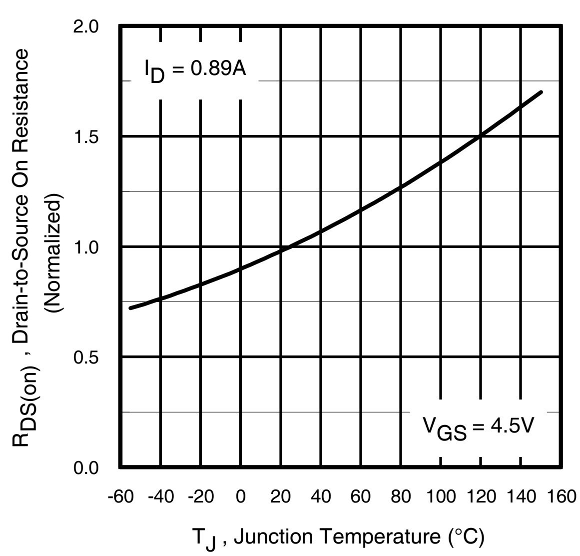


Fig 4. Normalized On-Resistance Vs. Temperature

N-Channel
Die 1

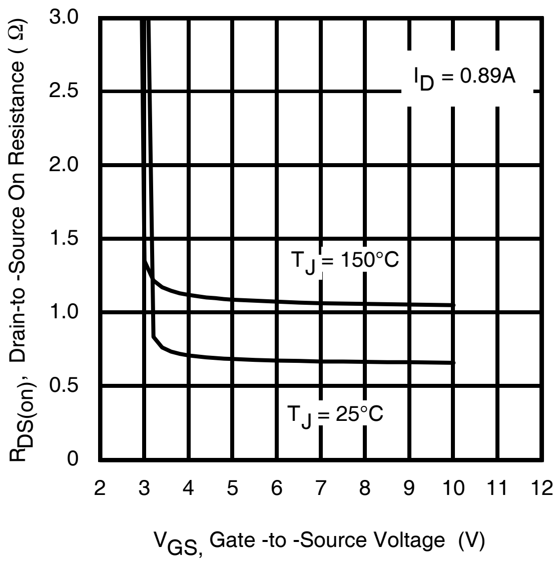


Fig 5. Typical On-Resistance Vs Gate Voltage

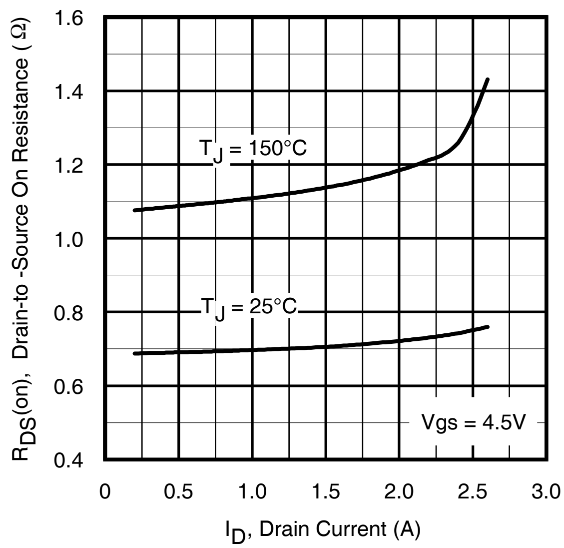


Fig 6. Typical On-Resistance Vs Drain Current

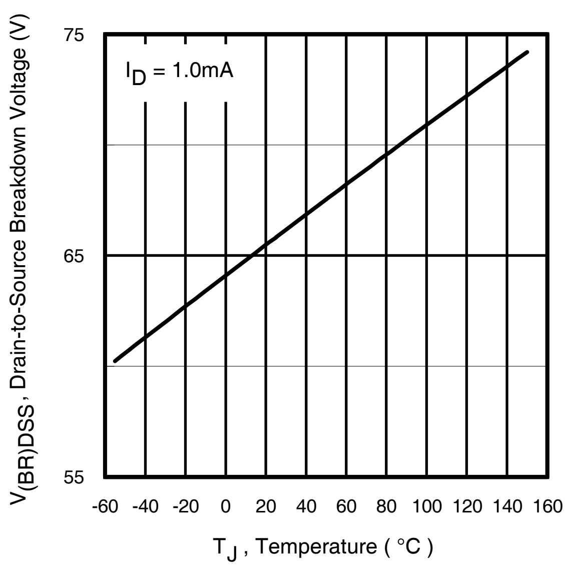


Fig 7. Typical Drain-to-Source Breakdown Voltage Vs Temperature

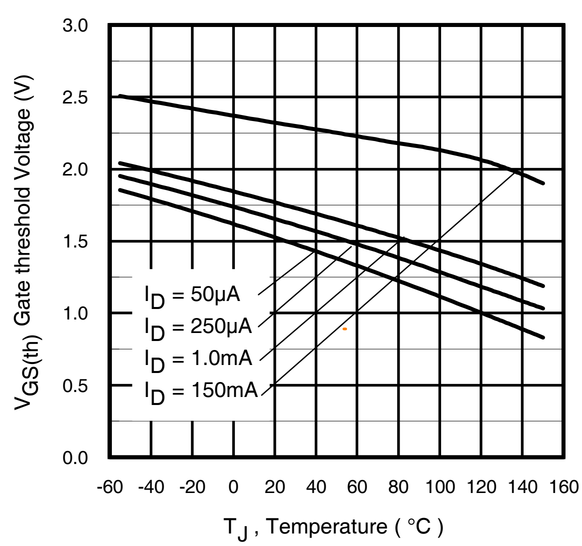


Fig 8. Typical Threshold Voltage Vs Temperature

N-Channel
Die 1

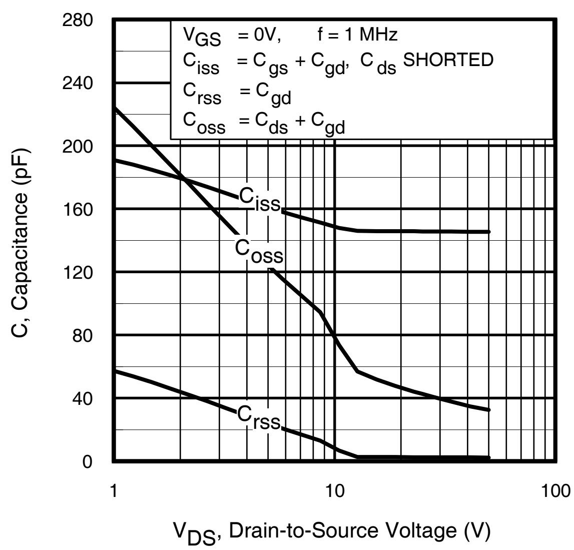


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

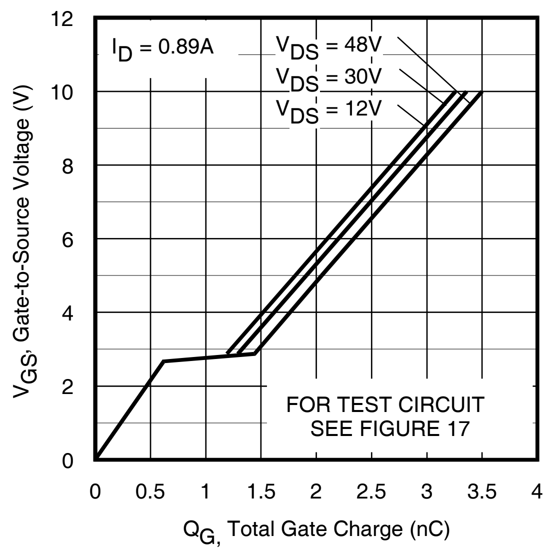


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

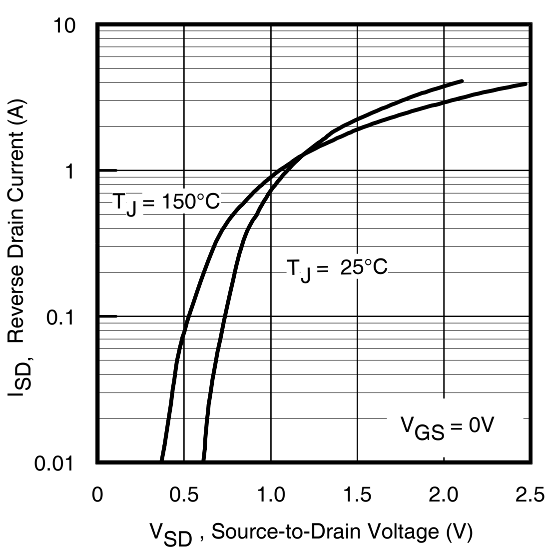


Fig 11. Typical Source-to-Drain Diode Forward Voltage

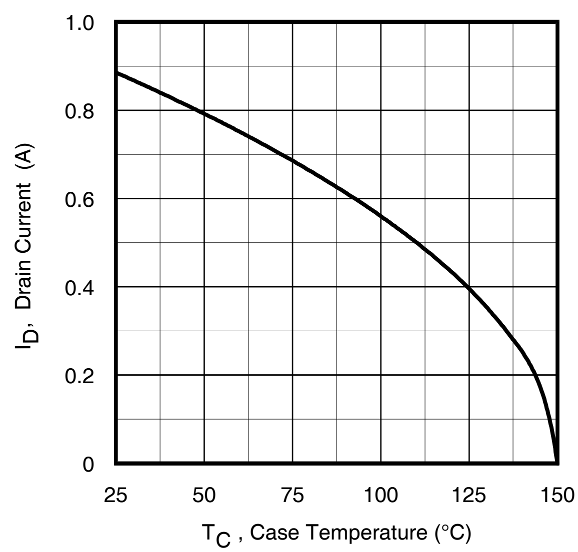


Fig 12. Maximum Drain Current Vs. Case Temperature

N-Channel
Die 1

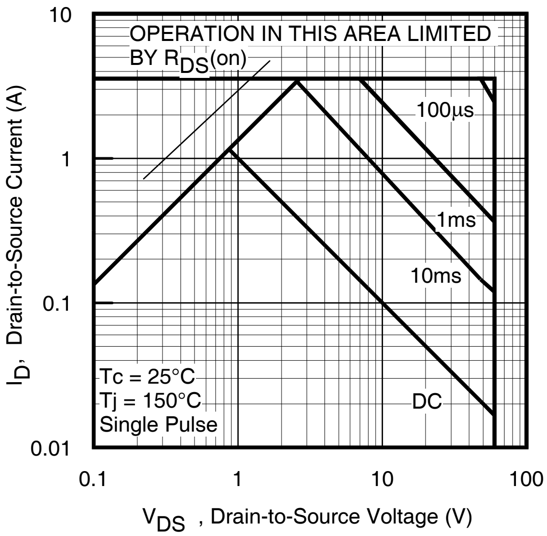


Fig 13. Maximum Safe Operating Area

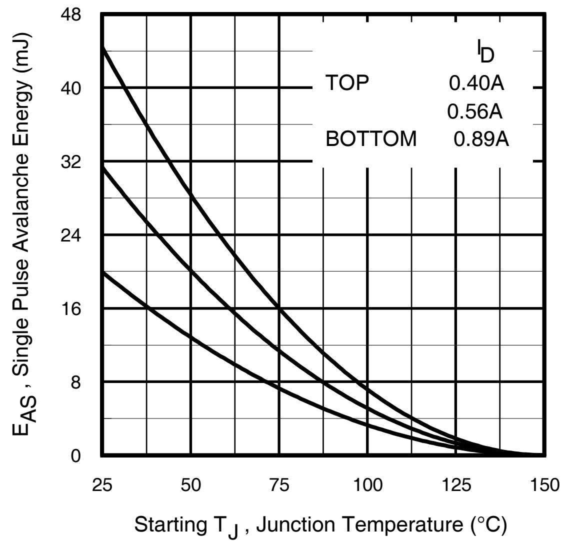


Fig 14. Maximum Avalanche Energy Vs. Drain Current

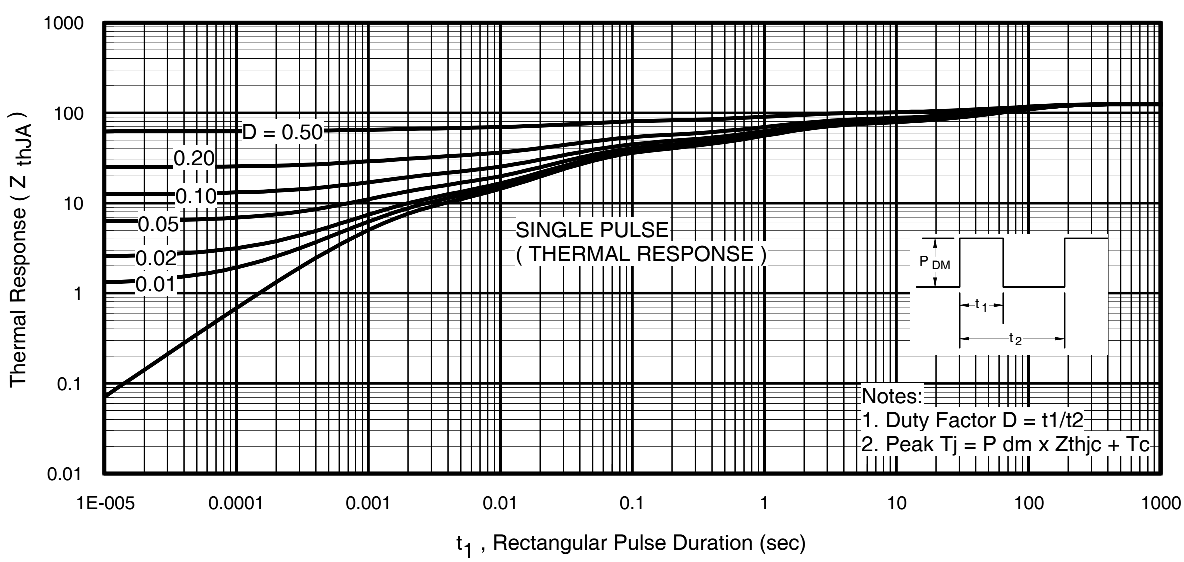


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

N-Channel
Die 1

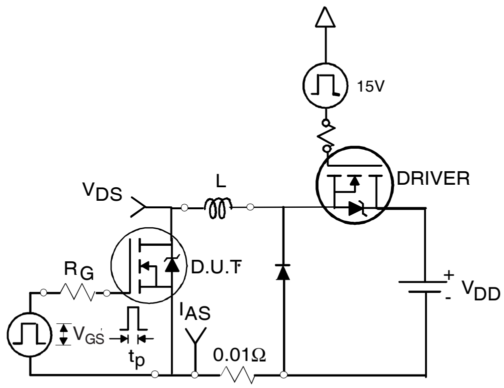


Fig 16a. Unclamped Inductive Test Circuit

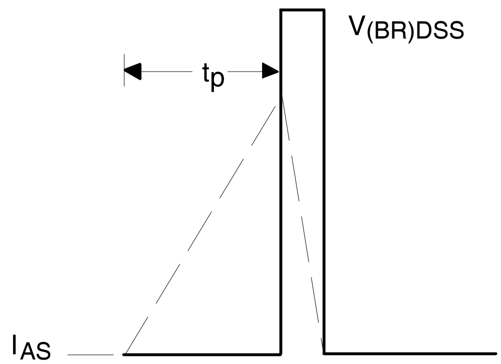


Fig 16b. Unclamped Inductive Waveforms

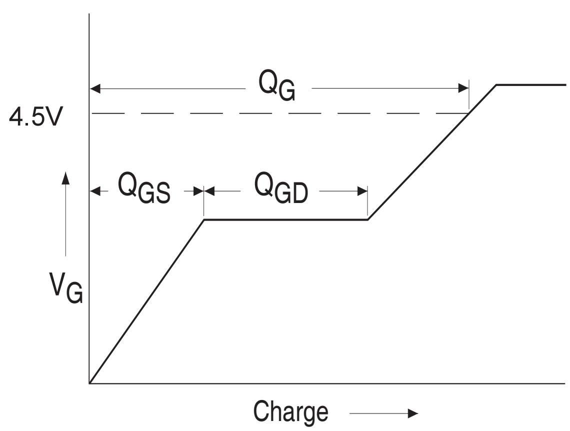


Fig 17a. Basic Gate Charge Waveform

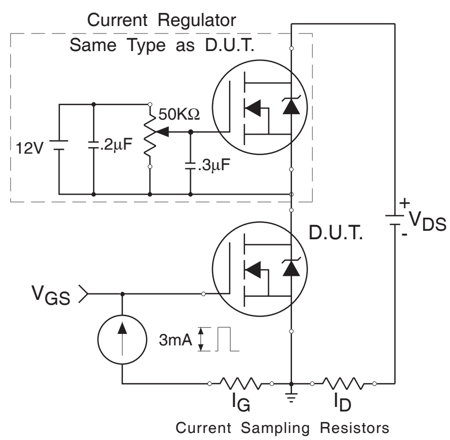


Fig 17b. Gate Charge Test Circuit

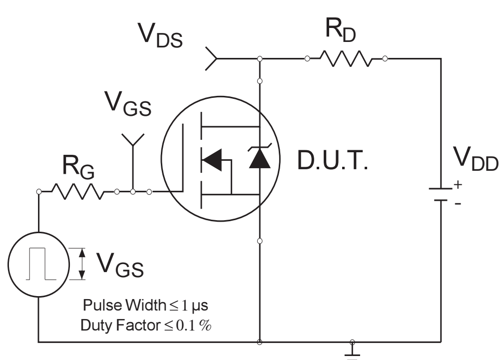


Fig 18a. Switching Time Test Circuit

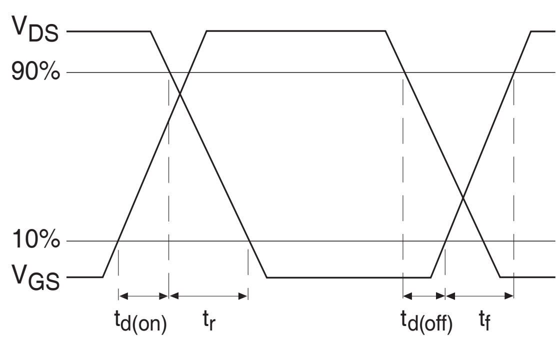


Fig 18b. Switching Time Waveforms

P-Channel
Die 2

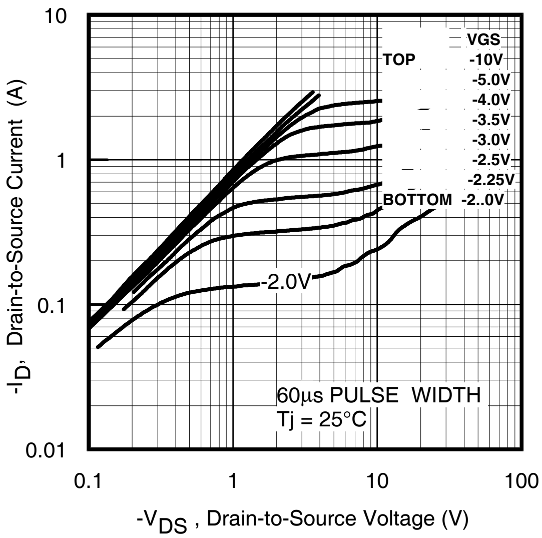


Fig 19. Typical Output Characteristics

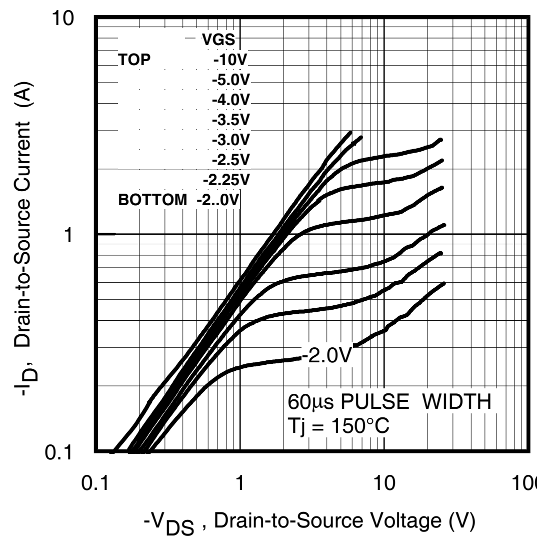


Fig 20. Typical Output Characteristics

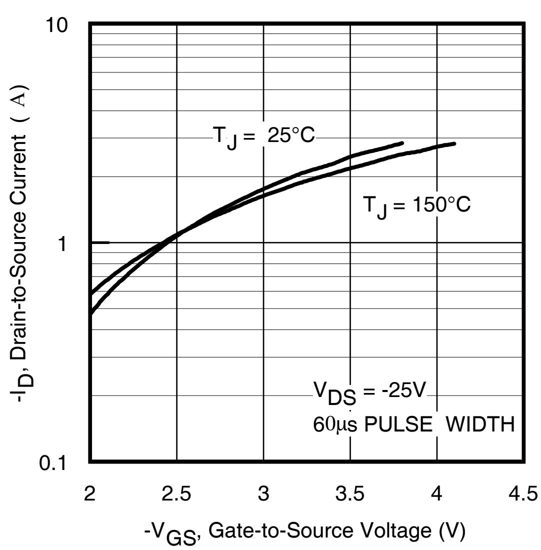


Fig 21. Typical Transfer Characteristics

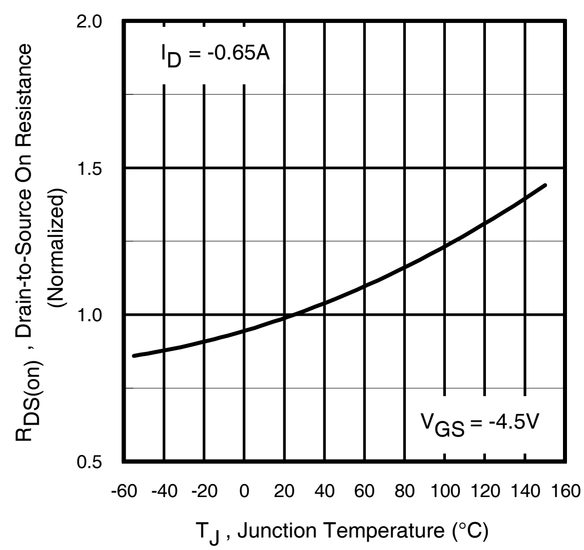


Fig 22. Normalized On-Resistance Vs. Temperature

P-Channel
Die 2

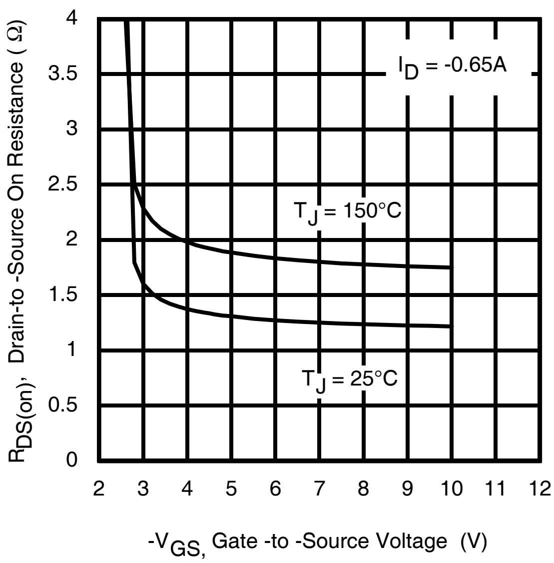


Fig 23. Typical On-Resistance Vs Gate Voltage

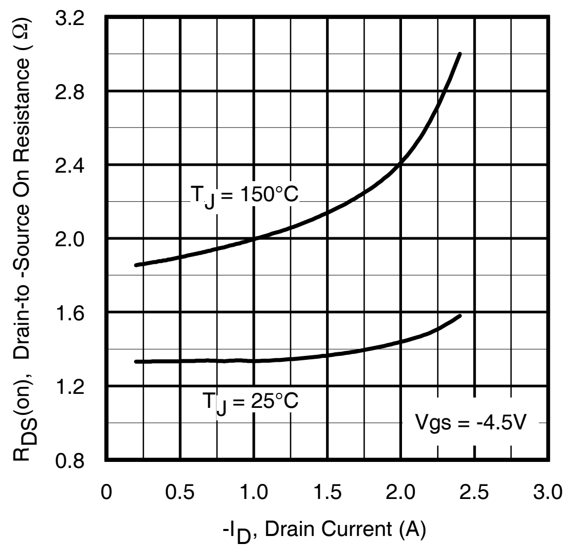


Fig 24. Typical On-Resistance Vs Drain Current

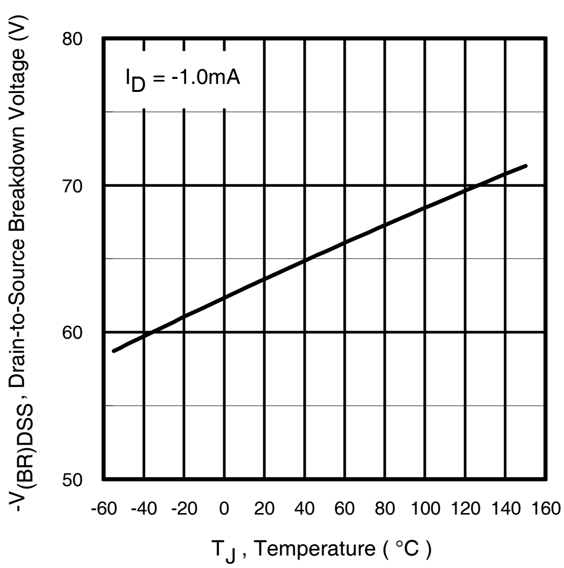


Fig 25. Typical Drain-to-Source Breakdown Voltage Vs Temperature

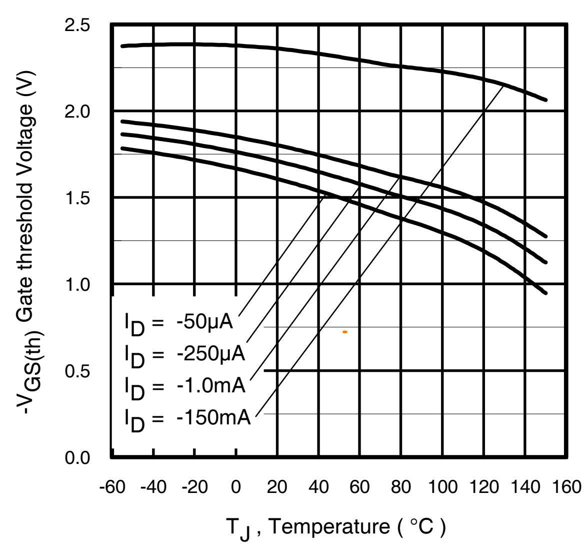


Fig 26. Typical Threshold Voltage Vs Temperature

P-Channel
Die 2

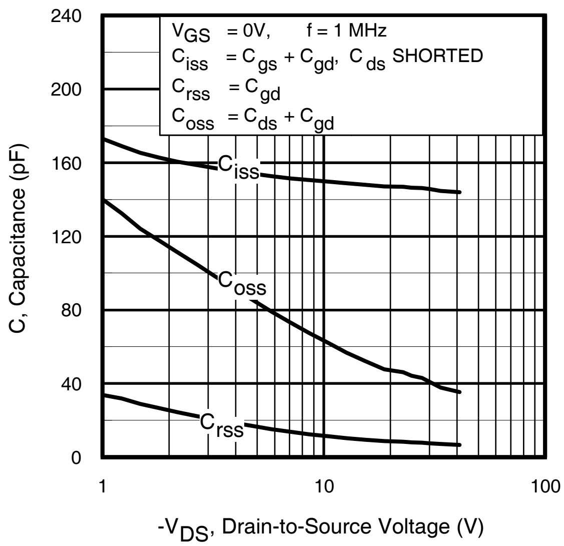


Fig 27. Typical Capacitance Vs. Drain-to-Source Voltage

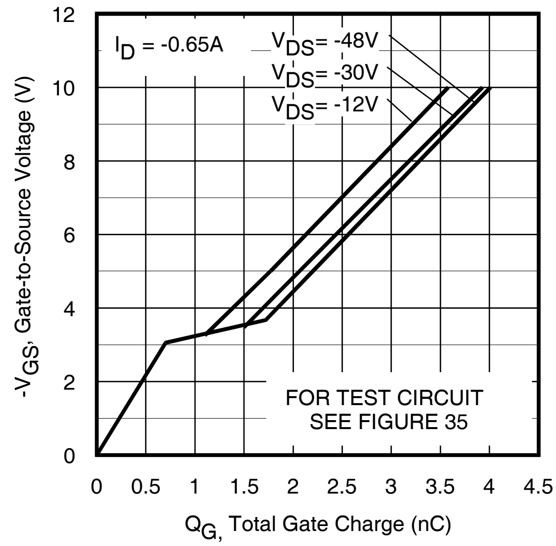


Fig 28. Typical Gate Charge Vs. Gate-to-Source Voltage

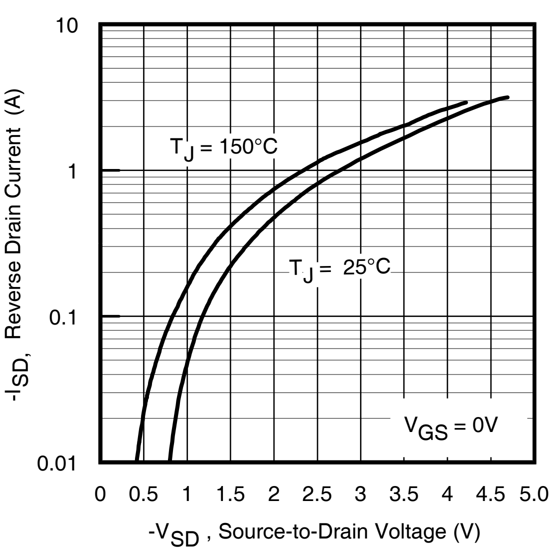


Fig 29. Typical Source-Drain Diode Forward Voltage

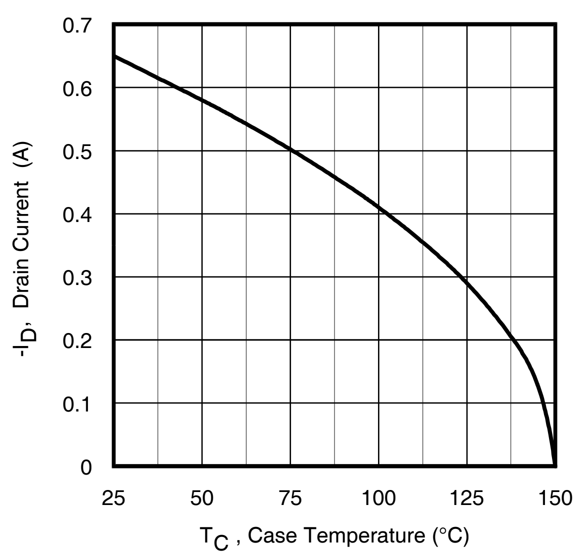


Fig 30. Maximum Drain Current Vs. Case Temperature

P-Channel
Die 2

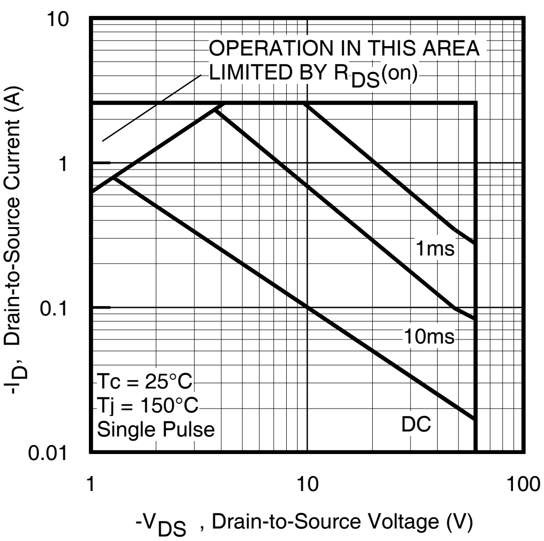


Fig 31. Maximum Safe Operating Area

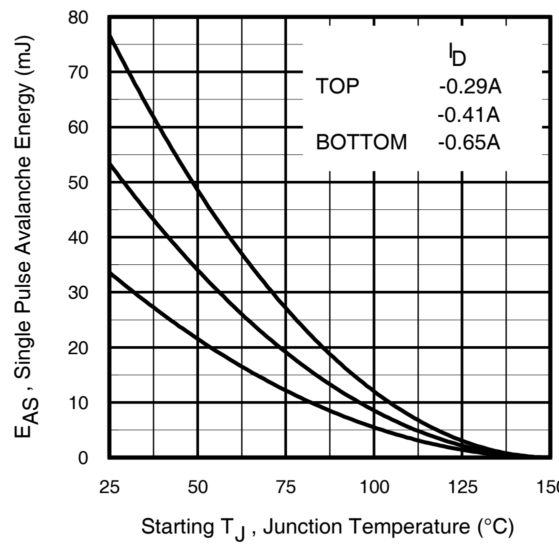


Fig 32. Maximum Avalanche Energy Vs. Drain Current

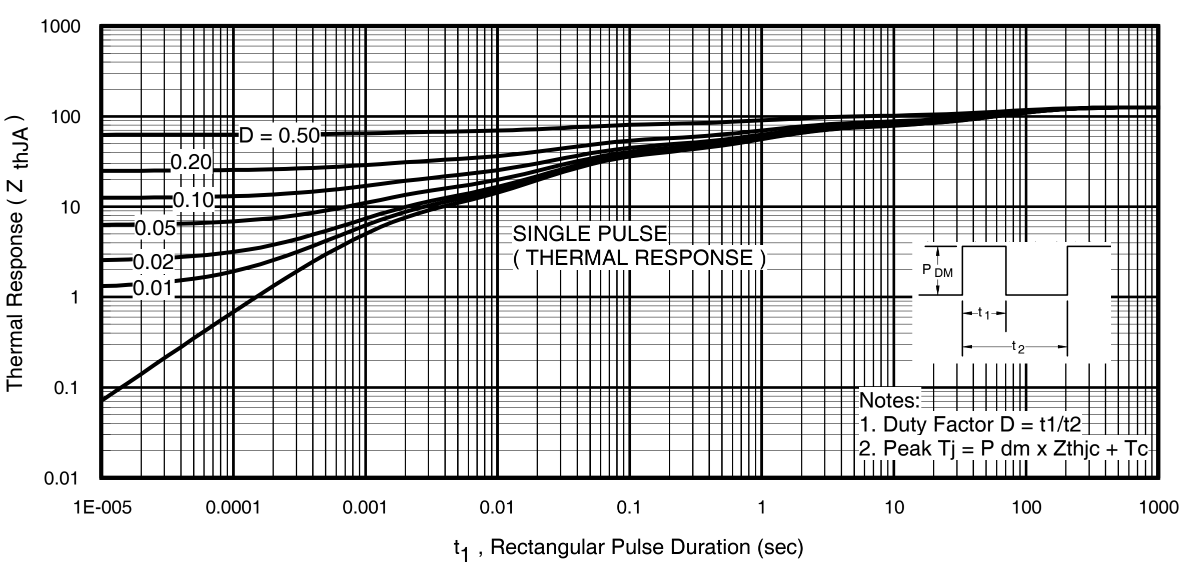


Fig 33. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

P-Channel
Die 2

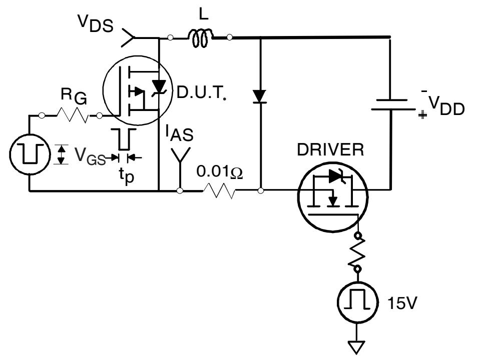


Fig 34a. Unclamped Inductive Test Circuit

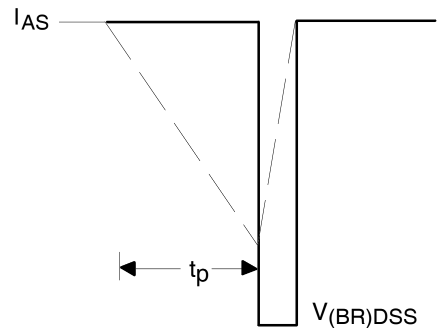


Fig 34b. Unclamped Inductive Waveforms

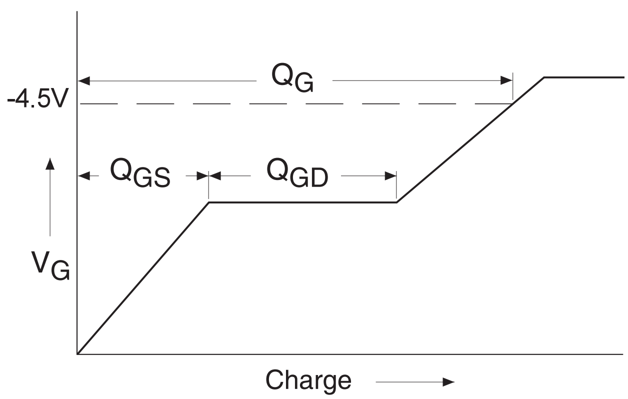


Fig 35a. Basic Gate Charge Waveform

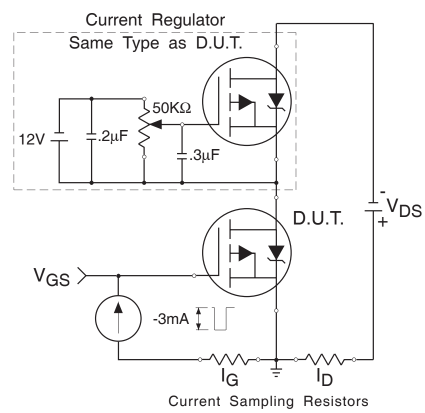


Fig 35b. Gate Charge Test Circuit

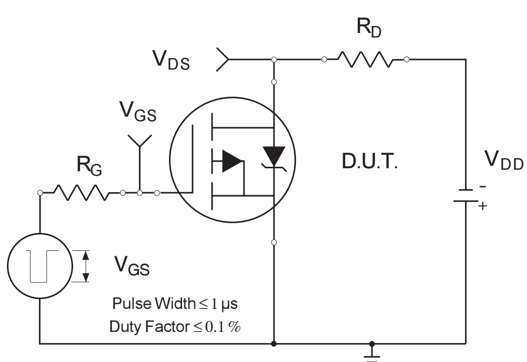


Fig 36a. Switching Time Test Circuit

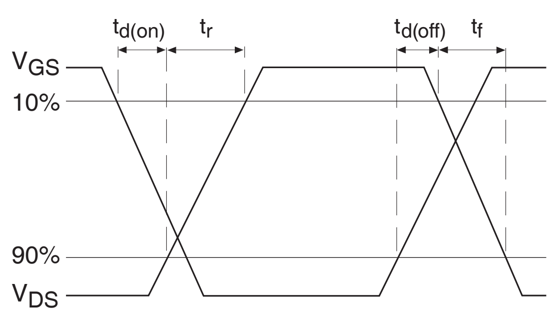


Fig 36b. Switching Time Waveforms

Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.

② V_{DD} = 25V, starting T_J = 25°C, L= 50.4mH, Peak I_L = 0.89A, V_{GS} = 10V

③ $I_{SD} \leq$ 0.89A, di/dt $\leq$ 200A/µs, $V_{DD} \leq$ 60V, $T_J \leq$ 150°C

④ Pulse width $\leq$ 300 µs; Duty Cycle $\leq$ 2%

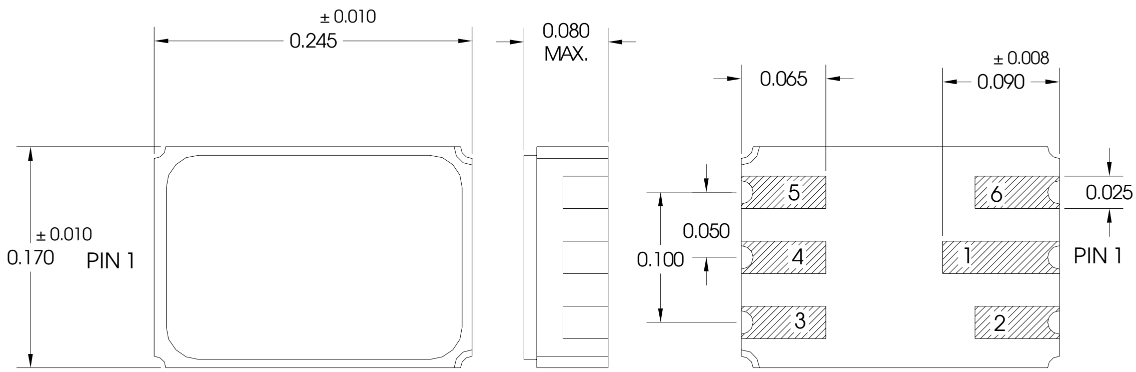
⑤ **Total Dose Irradiation with V_{GS} Bias.** ±10 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, method 1019, condition A

⑥ **Total Dose Irradiation with V_{DS} Bias.** ±48 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, method 1019, condition A

⑦ V_{DD} = -25V, starting T_J = 25°C, L= 161mH, Peak I_L = -0.65A, V_{GS} = -10V

⑧ $I_{SD} \leq$ -0.65A, di/dt $\leq$ -150A/µs, $V_{DD} \leq$ -60V, $T_J \leq$ 150°C

Case Outline and Dimensions — LCC-6



NOTES:

1. OUTLINE CONFORMS TO MIL-PRF-19500/255L
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. CONTROLLING DIMENSION: INCH.

DIE 1 (N Ch)		DIE 2 (P Ch)	
PIN NAME	PIN #	PIN NAME	PIN #
DRAIN	- 1	DRAIN	- 4
GATE	- 2	GATE	- 5
SOURCE	- 6	SOURCE	- 3

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Data and specifications subject to change without notice. 10/2010