

PRELIMINARY

PD-97174A

International
IR Rectifier

**RADIATION HARDENED
 LOGIC LEVEL POWER MOSFET
 SURFACE MOUNT (SMD-2)**

**2N7622U2
 IRHLNA797064
 60V, P-CHANNEL
 TECHNOLOGY**

Product Summary

Part Number	Radiation Level	R _{DS(on)}	I _D
IRHLNA797064	100K Rads (Si)	0.015Ω	-56A*
IRHLNA793064	300K Rads (Si)	0.015Ω	-56A*



International Rectifier's R7TM Logic Level Power MOSFETs provide simple solution to interfacing CMOS and TTL control circuits to power devices in space and other radiation environments. The threshold voltage remains within acceptable operating limits over the full operating temperature and post radiation. This is achieved while maintaining single event gate rupture and single event burnout immunity.

These devices are used in applications such as current boost low signal source in PWM, voltage comparator and operational amplifiers.

Features:

- 5V CMOS and TTL Compatible
- Fast Switching
- Single Event Effect (SEE) Hardened
- Low Total Gate Charge
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Ceramic Package
- Surface Mount
- Light Weight

Absolute Maximum Ratings

Pre-Irradiation

	Parameter		Units
I _D @ V _{GS} = -4.5V, T _C = 25°C	Continuous Drain Current	-56*	A
I _D @ V _{GS} = -4.5V, T _C = 100°C	Continuous Drain Current	-56*	
I _{DM}	Pulsed Drain Current ①	-224	
P _D @ T _C = 25°C	Max. Power Dissipation	250	W
	Linear Derating Factor	2.0	W/°C
V _{GS}	Gate-to-Source Voltage	±10	V
EAS	Single Pulse Avalanche Energy ②	1060	mJ
I _{AR}	Avalanche Current ①	-56	A
E _{AR}	Repetitive Avalanche Energy ①	25	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-3.7	V/ns
T _J	Operating Junction	-55 to 150	°C
T _{STG}	Storage Temperature Range		
	Pckg. Mounting Surface Temp.	300 (for 5s)	
	Weight	3.3 (Typical)	g

* Current is limited by package

For footnotes refer to the last page

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Pre-Irradiation

Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BVDSS	Drain-to-Source Breakdown Voltage	-60	—	—	V	V _{GS} = 0V, I _D = -250μA
ΔBVDSS/ΔT _J	Temperature Coefficient of Breakdown Voltage	—	-0.06	—	V/°C	Reference to 25°C, I _D = -1.0mA
RDS(on)	Static Drain-to-Source On-State Resistance	—	—	0.015	Ω	V _{GS} = -4.5V, I _D = -56A ④
VGS(th)	Gate Threshold Voltage	-1.0	—	-2.0	V	V _{DS} = V _{GS} , I _D = -250μA
ΔVGS(th)/ΔT _J	Gate Threshold Voltage Coefficient	—	4.1	—	mV/°C	
gfs	Forward Transconductance	82	—	—	S	V _{DS} = -15V, I _{DS} = -56A ④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	-1.0	μA	V _{DS} = -48V, V _{GS} = 0V
		—	—	-10		V _{DS} = -48V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	V _{GS} = -10V
I _{GSS}	Gate-to-Source Leakage Reverse	—	—	100		V _{GS} = 10V
Q _g	Total Gate Charge	—	—	190	nC	V _{GS} = -4.5V, I _D = -56A
Q _{gs}	Gate-to-Source Charge	—	—	53		V _{DS} = -30V
Q _{gd}	Gate-to-Drain ('Miller') Charge	—	—	56		
t _{d(on)}	Turn-On Delay Time	—	—	38	ns	V _{DD} = -30V, I _D = -56A, V _{GS} = -6.0V, R _G = 2.35Ω
t _r	Rise Time	—	—	265		
t _{d(off)}	Turn-Off Delay Time	—	—	210		
t _f	Fall Time	—	—	70		
L _S + L _D	Total Inductance	—	4.0	—	nH	Measured from the center of drain pad to center of source pad
C _{iss}	Input Capacitance	—	10520	—	pF	V _{GS} = 0V, V _{DS} = -25V f = 1.0MHz
C _{oss}	Output Capacitance	—	2780	—		
C _{rss}	Reverse Transfer Capacitance	—	310	—		
R _g	Gate Resistance	—	2.3	—		

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	-56*	A	T _j = 25°C, I _S = -56A, V _{GS} = 0V ④
I _{SM}	Pulse Source Current (Body Diode) ①	—	—	-224		
V _{SD}	Diode Forward Voltage	—	—	-5.0	V	T _j = 25°C, I _F = -56A, di/dt ≤ -100A/μs
t _{rr}	Reverse Recovery Time	—	—	159	ns	V _{DD} ≤ -25V ④
Q _{RR}	Reverse Recovery Charge	—	—	430	nC	
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

* Current is limited by package

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R _{thJC}	Junction-to-Case	—	—	0.5	°C/W	soldered to a 2" square copper-cladboard
R _{thJ-PCB}	Junction-to-PC board	—	1.6	—		

Note: Corresponding Spice and Saber models are available on International Rectifier Web site.

For footnotes refer to the last page

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Radiation Characteristics

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International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table 1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

	Parameter	Upto 300K Rads (Si) ¹		Units	Test Conditions
		Min	Max		
BV _{DSS}	Drain-to-Source Breakdown Voltage	-60	—	V	V _{GS} = 0V, I _D = -250μA
V _{GS(th)}	Gate Threshold Voltage	-1.0	-2.0		V _{GS} = V _{DS} , I _D = -250μA
I _{GSS}	Gate-to-Source Leakage Forward	—	-100	nA	V _{GS} = -10V
I _{GSS}	Gate-to-Source Leakage Reverse	—	100		V _{GS} = 10V
I _{DSS}	Zero Gate Voltage Drain Current	—	-10	μA	V _{DS} = -48V, V _{GS} = 0V
R _{DS(on)}	Static Drain-to-Source On-State Resistance (TO-3) ④	—	0.015	Ω	V _{GS} = -4.5V, I _D = -56A
R _{DS(on)}	Static Drain-to-Source On-state Resistance (SMD-2) ④	—	0.015	Ω	V _{GS} = -4.5V, I _D = -56A
V _{SD}	Diode Forward Voltage④	—	-5.0	V	V _{GS} = 0V, I _D = -56A

1. Part numbers IRHLNA797064, IRHLNA793064

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Single Event Effect Safe Operating Area

Ion	LET (MeV/(mg/cm ²))	Energy (MeV)	Range (μm)	V _{DS} (V)							
				@V _{GS} = 0V	@V _{GS} = 2V	@V _{GS} = 4V	@V _{GS} = 5V	@V _{GS} = 6V	@V _{GS} = 7V	@V _{GS} = 8V	@V _{GS} = 10V
Br	37	305	39	-60	-60	-60	-60	-40	-30	-25	-20
I	60	370	34	-60	-60	-60	-40	-20	-	-	-
Au	82	390	30	-60	-60	-60	-	-	-	-	-

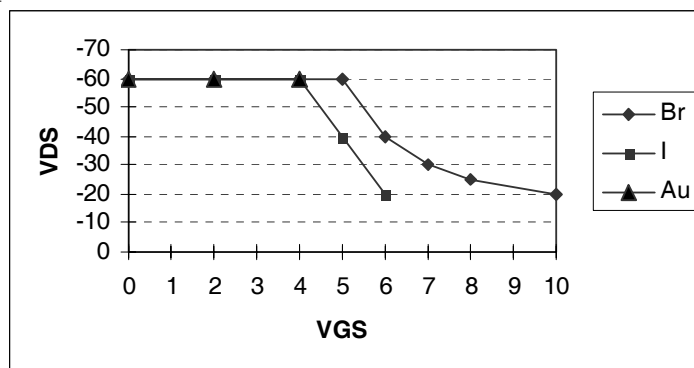
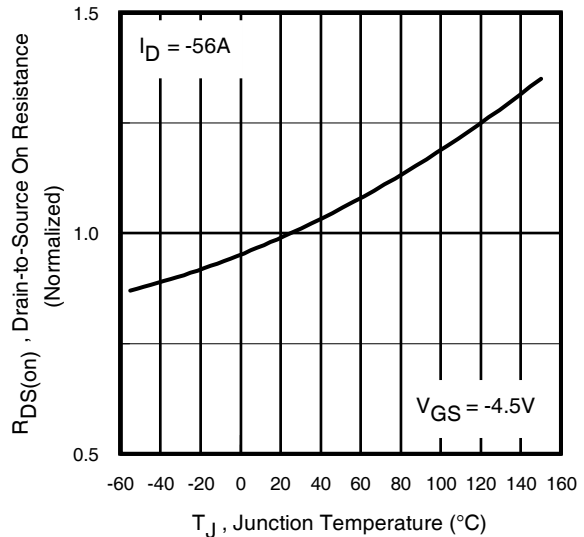
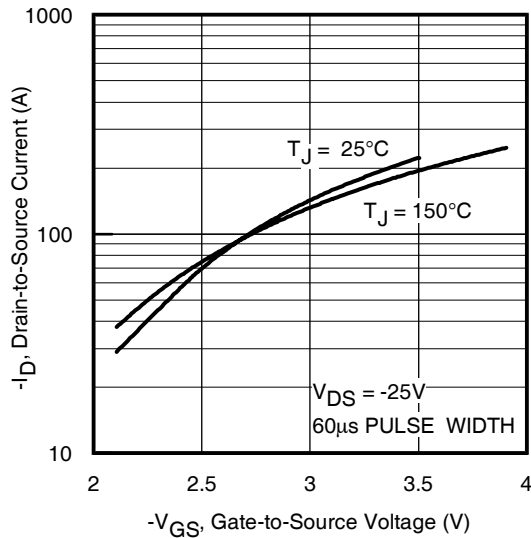
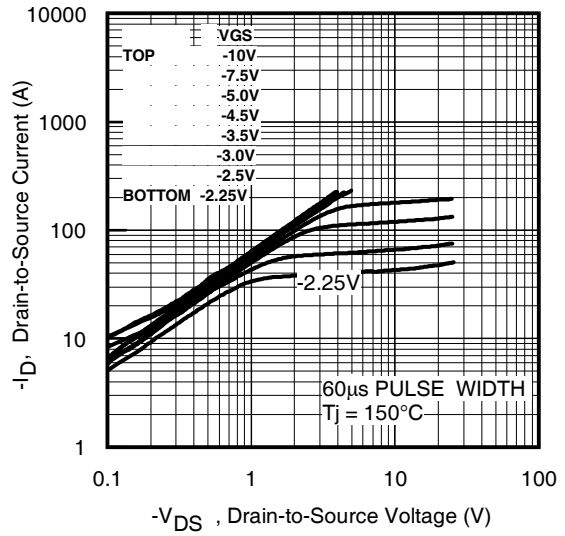
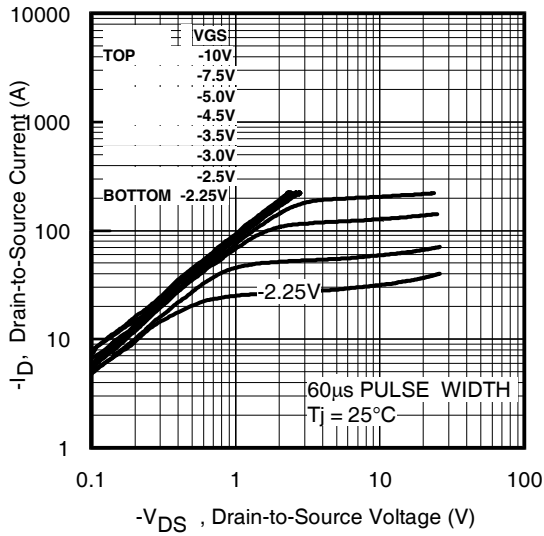


Fig a. Single Event Effect, Safe Operating Area

For footnotes refer to the last page



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Pre-Irradiation

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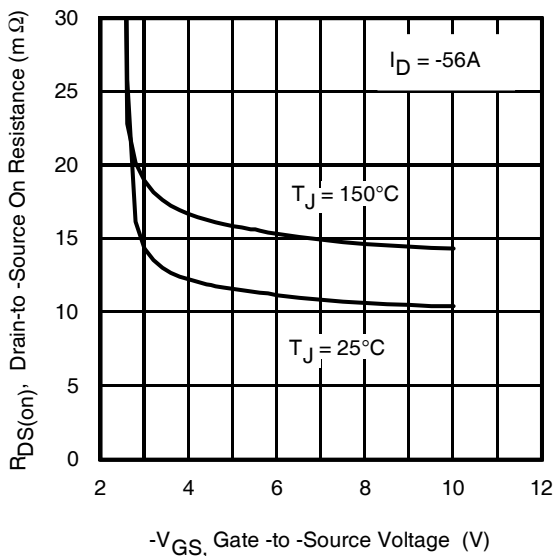


Fig 5. Typical On-Resistance Vs Gate Voltage

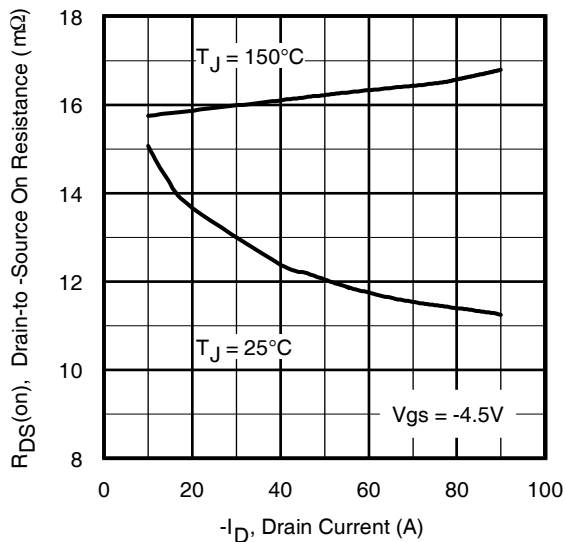


Fig 6. Typical On-Resistance Vs Drain Current

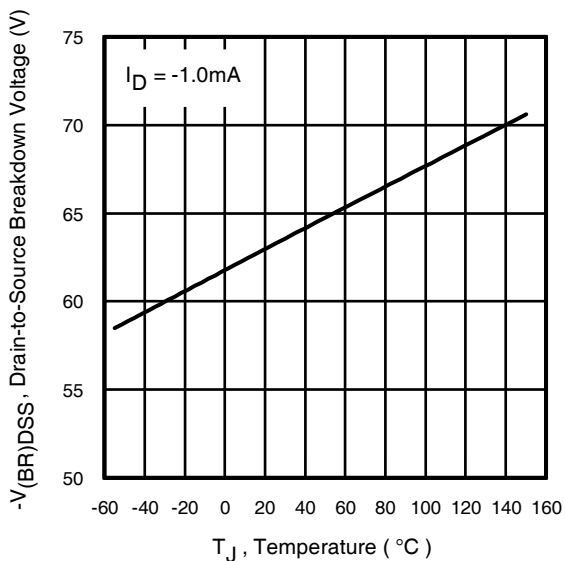


Fig 7. Typical Drain-to-Source Breakdown Voltage Vs Temperature

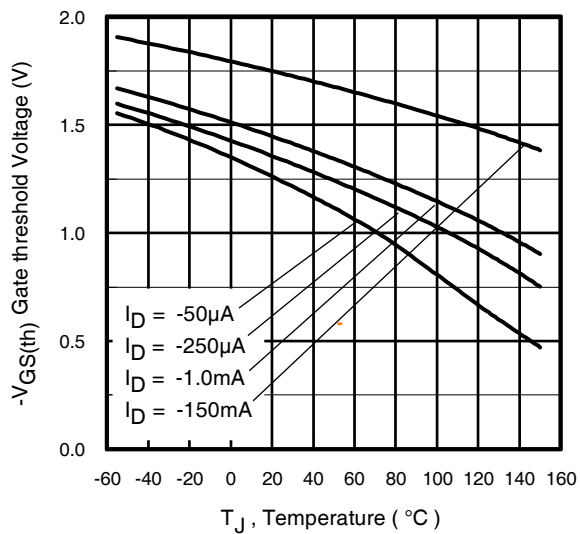


Fig 8. Typical Threshold Voltage Vs Temperature

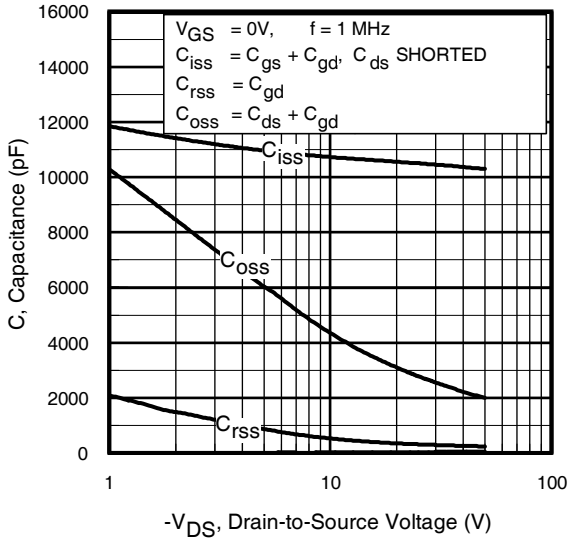


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

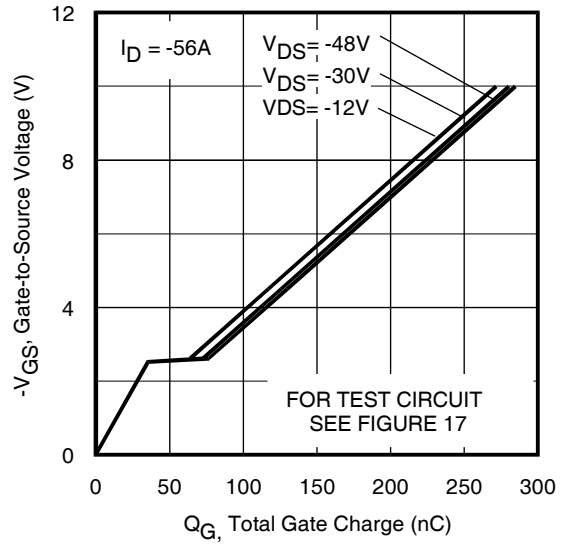


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

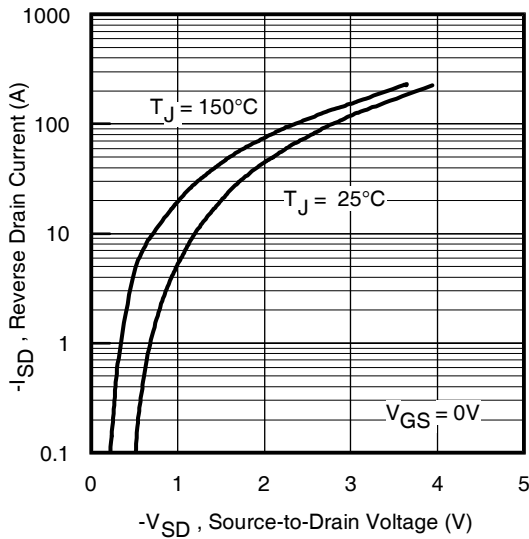


Fig 11. Typical Source-to-Drain Diode Forward Voltage

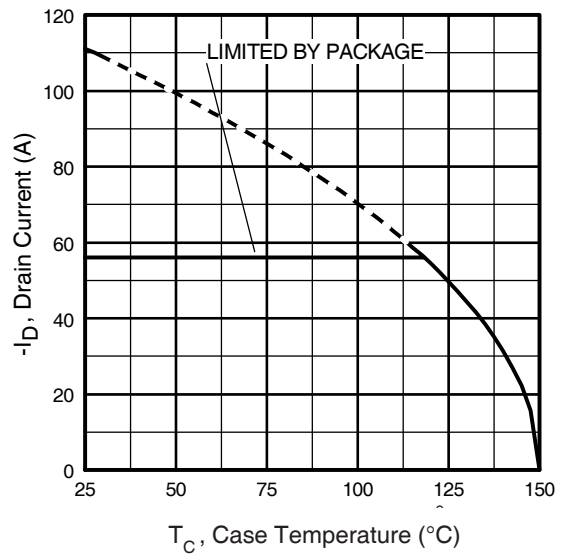


Fig12. Maximum Drain Current Vs. Case Temperature

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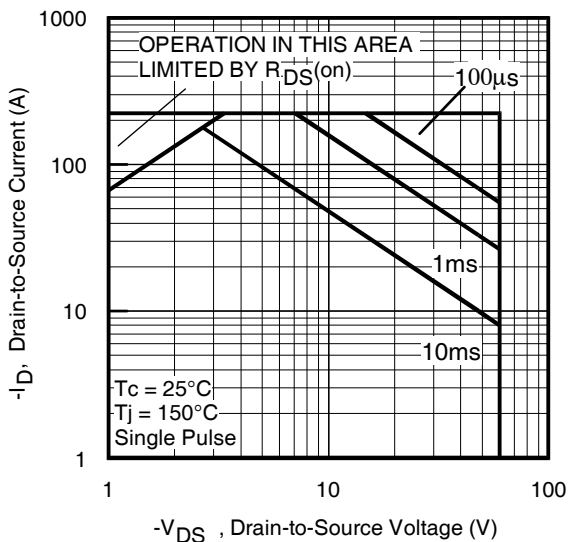


Fig 13. Maximum Safe Operating Area

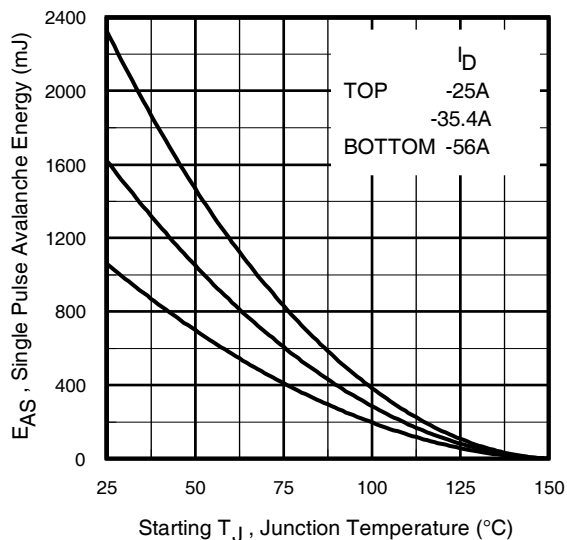


Fig 14. Maximum Avalanche Energy Vs. Drain Current

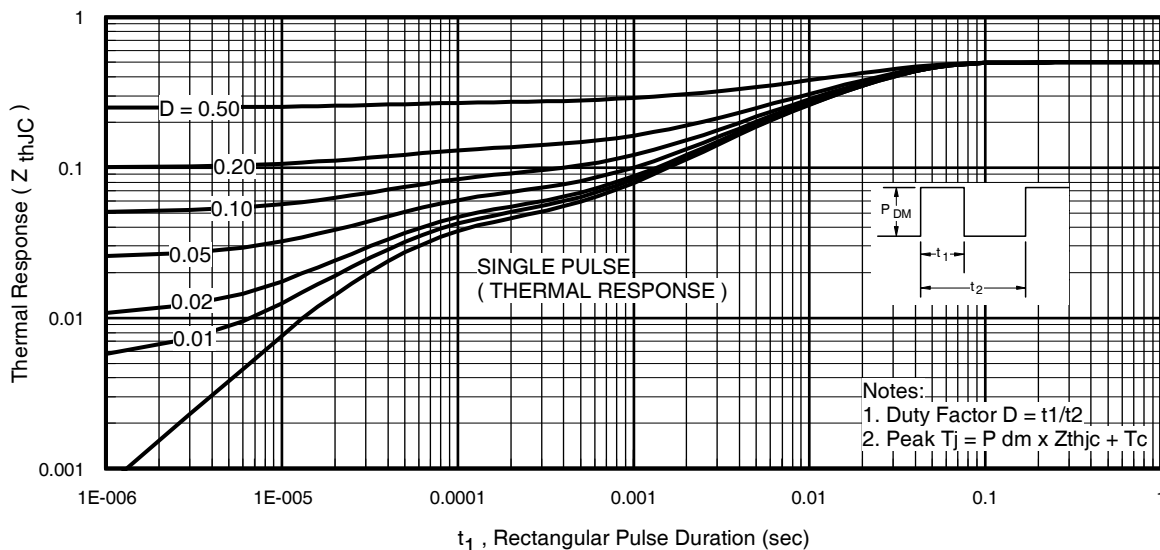


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Case

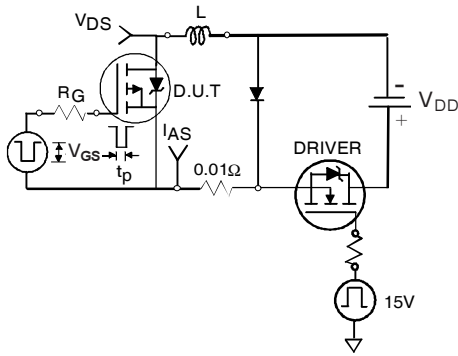


Fig 16a. Unclamped Inductive Test Circuit

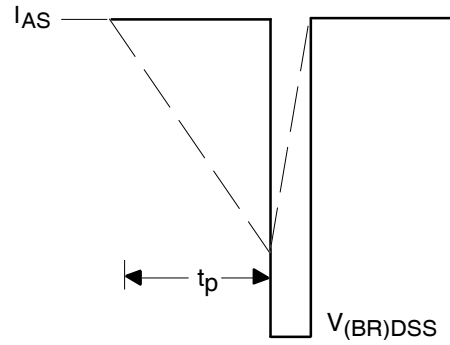


Fig 16b. Unclamped Inductive Waveforms

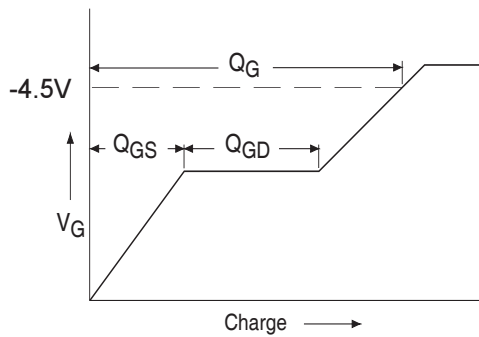


Fig 17a. Basic Gate Charge Waveform

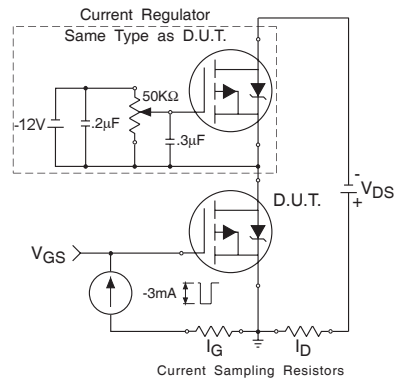


Fig 17b. Gate Charge Test Circuit

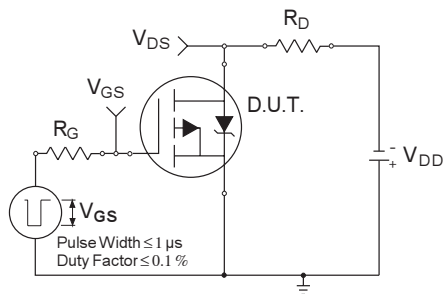


Fig 18a. Switching Time Test Circuit

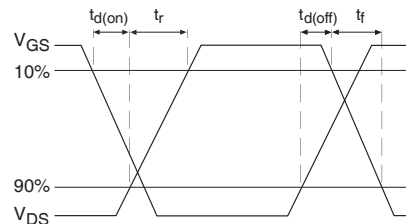


Fig 18b. Switching Time Waveforms

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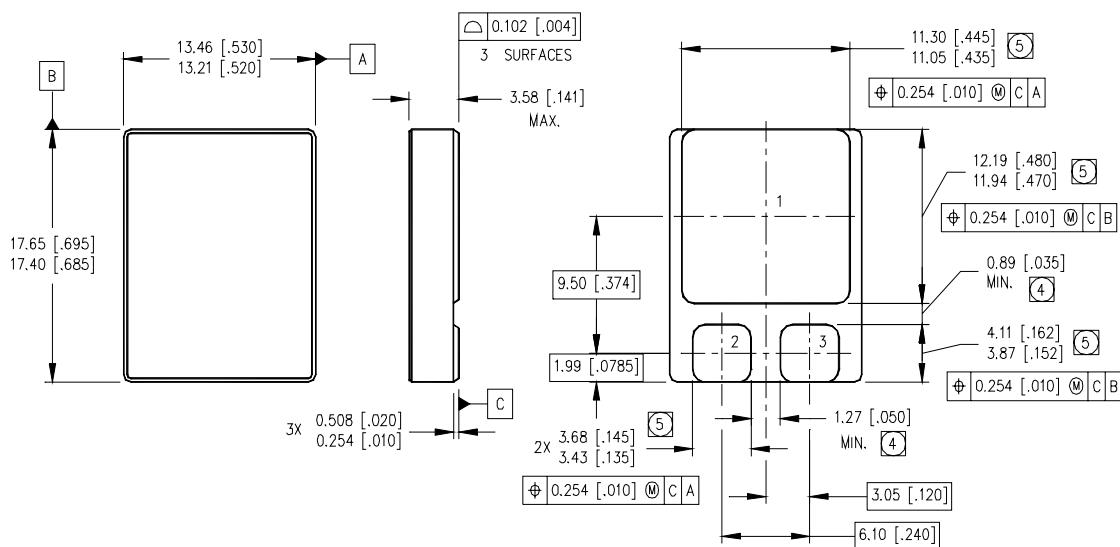
Pre-Irradiation

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Footnotes:

- | | |
|--|--|
| <p>① Repetitive Rating; Pulse width limited by maximum junction temperature.</p> <p>② $V_{DD} = -25V$, starting $T_J = 25^\circ C$, $L = 0.67mH$
Peak $I_L = -56A$, $V_{GS} = -10V$</p> <p>③ $I_{SD} \leq -56A$, $di/dt \leq -380A/\mu s$,
$V_{DD} \leq -60V$, $T_J \leq 150^\circ C$</p> | <p>④ Pulse width $\leq 300 \mu s$; Duty Cycle $\leq 2\%$</p> <p>⑤ Total Dose Irradiation with V_{GS} Bias.
-10 volt V_{GS} applied and $V_{DS} = 0$ during irradiation per MIL-STD-750, method 1019, condition A.</p> <p>⑥ Total Dose Irradiation with V_{DS} Bias.
-48 volt V_{DS} applied and $V_{GS} = 0$ during irradiation per MIL-STD-750, method 1019, condition A.</p> |
|--|--|

Case Outline and Dimensions — SMD-2



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

- ④ DIMENSION INCLUDES METALLIZATION FLASH.
- ⑤ DIMENSION DOES NOT INCLUDE METALLIZATION FLASH.

PAD ASSIGNMENTS

- 1 = DRAIN
2 = GATE
3 = SOURCE

International
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Data and specifications subject to change without notice. 03/2011