

Control Integrated Power System (CIPOS™)

IKCM15R60GD

Datasheet



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CIPOS™

Control Integrated **P**ower **S**ystem

Dual In-Line Intelligent Power Module

Two Phase Switched Reluctance Drives 600V / 15A

Features

Dual In-Line molded module

- TrenchStop® IGBTs
- Rugged SOI gate driver technology with stability against transient and negative voltage
- Allowable negative VS potential up to -11V for signal transmission at VBS=15V
- Integrated bootstrap functionality
- Over current shutdown
- Under-voltage lockout at all channels
- All of 4 switches turn off during protection
- Lead-free terminal plating; RoHS compliant
- Very low thermal resistance due to DCB
- Temperature monitor

Target Applications

- Two Phase Switched Reluctance Drive

Description

The CIPOS™ module family offers the chance for integrating various power and control components to increase reliability, optimize PCB size and system costs.

It is designed to control two phase switched reluctance motors in variable speed drives for applications like a vacuum cleaner. The package concept is specially adapted to power applications, which need good thermal conduction and electrical isolation, but also EMI-save control and overload protection.

TrenchStop® IGBTs and anti parallel diodes are combined with an optimized SOI gate driver for excellent electrical performance.

System Configuration

- Two phase switched reluctance drive with TrenchStop® IGBTs
- SOI gate driver
- Thermistor
- Pin-to- heatsink creepage distance typ. 1.6mm

Pin Configuration

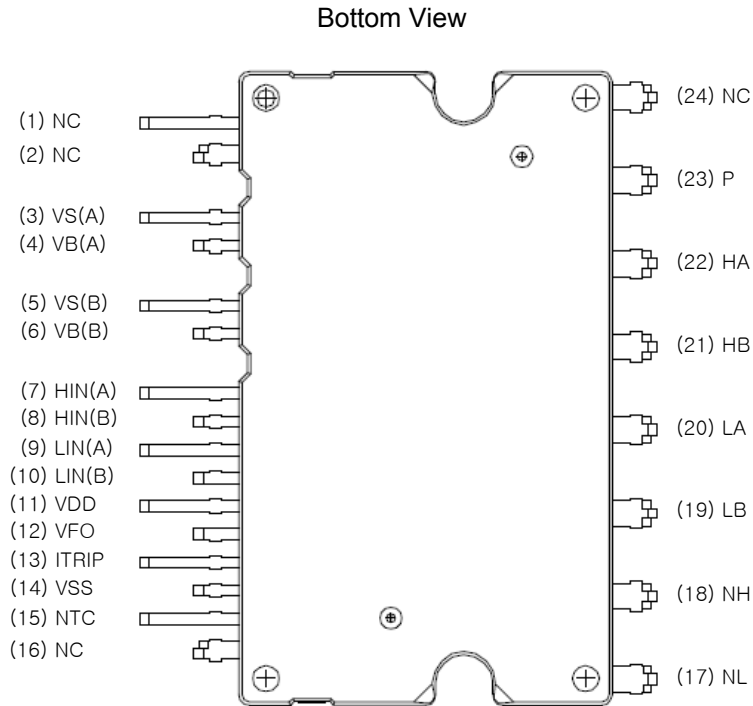


Figure 1: Pin configuration

Internal Electrical Schematic

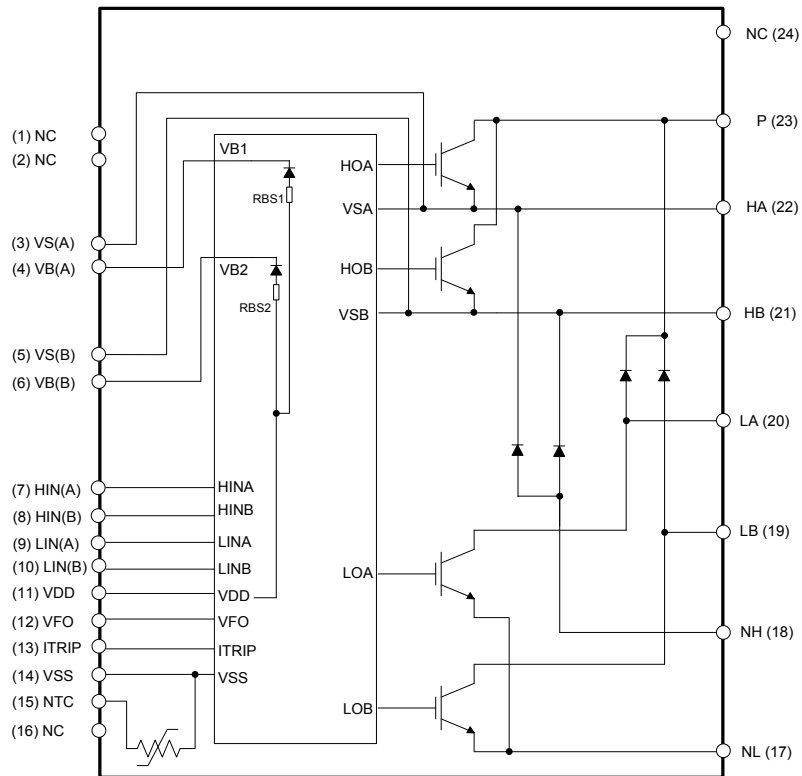


Figure 2: Internal schematic

Pin Assignment

Pin Number	Pin Name	Pin Description
1	NC	No Connection
2	NC	No Connection
3	VS(A)	A-phase high side floating IC supply offset voltage
4	VB(A)	A-phase high side floating IC supply voltage
5	VS(B)	B-phase high side floating IC supply offset voltage
6	VB(B)	B-phase high side floating IC supply voltage
7	HIN(A)	A phase high side gate driver input
8	HIN(B)	B phase high side gate driver input
9	LIN(A)	A phase low side gate driver input
10	LIN(B)	B phase low side gate driver input
11	VDD	Low side control supply
12	VFO	Fault output
13	ITRIP	Over current shutdown input
14	VSS	Low side control negative supply
15	NTC	Temperature monitor
16	NC	No Connection
17	NL	LA, LB IGBT emitter
18	NH	HA, HB diode anode
19	LB	LB phase output
20	LA	LA phase output
21	HB	HB phase output
22	HA	HA phase output
23	P	Positive bus input voltage
24	NC	No Connection

Pin Description

HIN(A, B) and LIN(A, B) (IGBT control pins, Pin 7 - 10)

These pins are positive logic and they are responsible for the control of the integrated IGBT. The Schmitt-trigger input thresholds of them are such to guarantee LSTTL and CMOS compatibility down to 3.3V controller outputs. Pull-down resistor of about 5kΩ is internally provided to pre-bias inputs during supply start-up and a zener clamp is provided for pin protection purposes. Input Schmitt-trigger and noise filter provide beneficial noise rejection to short input pulses.

The noise filter suppresses control pulses which are below the filter time t_{FILIN} . The filter acts according to Figure 4.

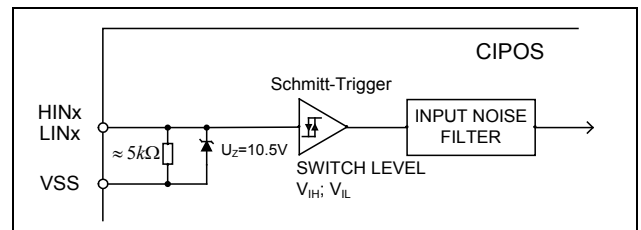


Figure 3: Input pin structure

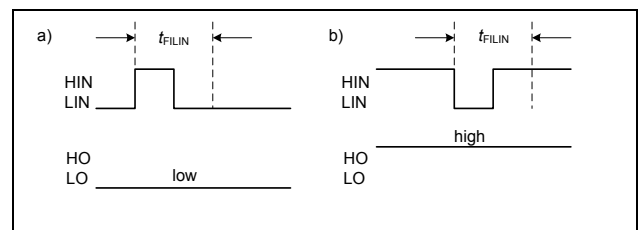


Figure 4: Input filter timing diagram

It is recommended for proper work of CIPOS™ not to provide input pulse-width lower than 1 μ s.

VFO (Fault-output, Pin 12)

The VFO pin indicates a module failure in case of under voltage at pin VDD or in case of triggered over current detection at ITRIP.

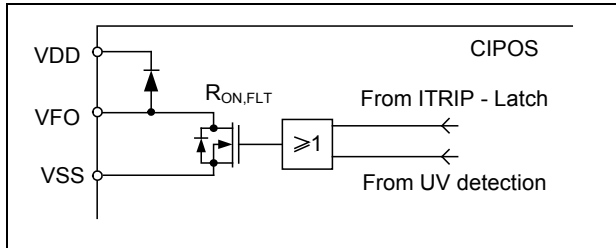


Figure 5: Internal circuit at pin VFO

ITRIP (Over current detection function, Pin 13)

CIPOS™ provides an over current detection function by connecting the ITRIP input with the motor current feedback. The ITRIP comparator threshold (typ. 0.47V) is referenced to VSS ground. A input noise filter (typ: $t_{ITRIPMIN} = 530ns$) prevents the driver to detect false over-current events.

Over current detection generates a shut down of all outputs of the gate driver after the shutdown propagation delay of typically 1000ns.

The fault-clear time is set to typical 65 μ s.

VDD, VSS (Low side control supply and reference, Pin 11, 14)

VDD is the low side supply and it provides power both to input logic and to low side output power stage. Input logic is referenced to VSS ground.

The under-voltage circuit enables the device to operate at power on when a supply voltage of at least a typical voltage of $V_{DDUV+} = 12.1V$ is present.

The IC shuts down all the gate drivers' power outputs, when the VDD supply voltage is below $V_{DDUV-} = 10.4V$. This prevents the external power switches from critically low gate voltage levels during on-state and therefore from excessive power dissipation.

VB(A, B) and VS(A, B) (High side supplies, Pin 3 - 6)

VB to VS is the high side supply voltage. The high side circuit can float with respect to VSS following the external high side power device emitter voltage.

Due to the low power consumption, the floating driver stage is supplied by integrated bootstrap circuit.

The under-voltage detection operates with a rising supply threshold of typical $V_{BSUV+} = 12.1V$ and a falling threshold of $V_{BSUV-} = 10.4V$.

VS(A, B) provide a high robustness against negative voltage in respect of VSS of -50V transiently. This ensures very stable designs even under rough conditions.

NL (IGBT emitter, Pin 17)

The low side IGBT emitters are available for current measurements. It is recommended to keep the connection to pin VSS as short as possible in order to avoid unnecessary inductive voltage drops.

NH (Diode anode, Pin 18)

The low side anodes of the integrated diodes are connected.

P (Positive bus input voltage, Pin 23)

The high sides of IGBT are connected to the bus voltage. It is noted that the bus voltage does not exceed 450 V.

Absolute Maximum Ratings

($V_{DD} = 15V$ and $T_J = 25^\circ C$, if not stated otherwise)

Module Section

Description	Condition	Symbol	Value		Unit
			min	max	
Storage temperature range		T_{stg}	-40	125	$^\circ C$
Insulation test voltage	RMS, $f = 60Hz$, $t = 1min$	V_{ISOL}	2000	-	V
Operating case temperature range	Refer to Figure 6	T_C	-40	100	$^\circ C$

Inverter Section

Description	Condition	Symbol	Value		Unit
			min	max	
Max. blocking voltage	$I_C = 250\mu A$	V_{CES}	600	-	V
DC link supply voltage of P-N	Applied between P-N	V_{PN}	-	450	V
DC link supply voltage (surge) of P-N	Applied between P-N	$V_{PN(surge)}$	-	500	V
Output current	$T_C = 25^\circ C$, $T_J \leq 150^\circ C$	I_C	-15	15	A
Maximum peak output current	$T_C = 25^\circ C$, less than 1ms	I_C	-30	30	A
Short circuit withstand time ¹	$V_{DC} \leq 400V$, $T_J \leq 150^\circ C$	t_{SC}	-	5	μs
Power dissipation per IGBT		P_{tot}	-	65.7	W
Operating junction temperature range		T_J	-40	150	$^\circ C$
Single IGBT thermal resistance, junction-case		R_{thJC}	-	1.90	K/W
Single diode thermal resistance, junction-case		R_{thJCD}	-	3.48	K/W

Control Section

Description	Condition	Symbol	Value		Unit
			min	max	
Module supply voltage		V_{DD}	-1	20	V
High side floating supply voltage (VB vs. VS)		V_{BS}	-1	20	V
Input voltage	LIN, HIN, ITRIP	V_{IN} , V_{ITRIP}	-1	10	V
Switching frequency		f_{PWM}	-	20	kHz

¹ Allowed number of short circuits: <1000; time between short circuits: >1s.

Recommended Operation Conditions

All voltages are absolute voltages referenced to V_{SS} -potential unless otherwise specified.

Description	Symbol	Value			Unit
		min	typ	max	
DC link supply voltage of P-N	V_{PN}	0	-	400	V
High side floating supply voltage (V_B vs. V_S)	V_{BS}	13.5	-	18.5	V
Low side supply voltage	V_{DD}	14.5	16	18.5	V
Control supply variation	ΔV_{BS}	-1	-	1	V/ μ s
	ΔV_{DD}	-1	-	1	
Logic input voltages LIN,HIN,ITRIP	V_{IN}	0	-	5	V
	V_{ITRIP}	0	-	5	
Between V_{SS} - N (including surge)	V_{SS}	-5	-	5	V

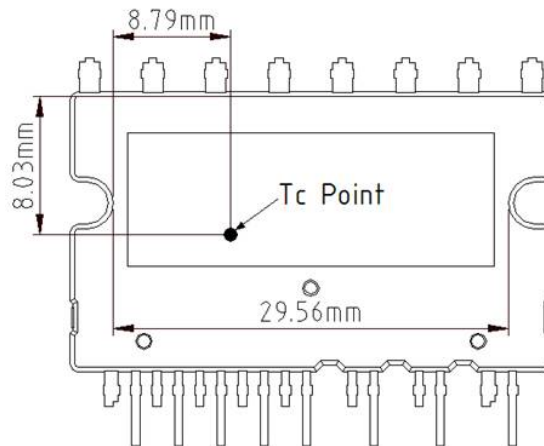


Figure 6: T_c measurement point¹

¹Any measurement except for the specified point in figure 6 is not relevant for the temperature verification and brings wrong or different information.

Static Parameters

(V_{DD} = 15V and T_J = 25°C, if not stated otherwise)

Description	Condition	Symbol	Value			Unit
			min	typ	max	
Collector-Emitter saturation voltage	I _C =10A, T _J = 25°C 150°C	V _{CE(sat)}	- -	1.55 1.85	2.1 -	V
Emitter-Collector forward voltage	I _C =-10A, T _J = 25°C 150°C	V _F	- -	1.75 1.8	2.45 -	V
Collector-Emitter leakage current	V _{CE} = 600V	I _{CES}	-	-	1	mA
Logic "1" input voltage (LIN,HIN)		V _{IH}	-	2.1	2.5	V
Logic "0" input voltage (LIN,HIN)		V _{IL}	0.7	0.9	-	V
ITRIP positive going threshold		V _{IT,TH+}	400	470	540	mV
ITRIP input hysteresis		V _{IT,HYS}	40	70	-	mV
VDD and VBS supply under voltage positive going threshold		V _{DDUV+} V _{BSUV+}	10.8	12.1	13.0	V
VDD and VBS supply under voltage negative going threshold		V _{DDUV-} V _{BSUV-}	9.5	10.4	11.2	V
VDD and VBS supply under voltage lockout hysteresis		V _{DDUVH} V _{BSUVH}	1.0	1.7	-	V
Input clamp voltage (HIN, LIN, ITRIP)	I _{in} = 4mA	V _{INCLAMP}	9.0	10.1	12.5	V
Quiescent VBx supply current (VBx only)	H _{IN} = 0V	I _{QBS}	-	300	500	μA
Quiescent VDD supply current (VDD only)	L _{IN} = 0V, H _{INX} = 5V	I _{QDD}	-	370	900	μA
Input bias current	V _{IN} = 5V	I _{IN+}	-	1	1.5	mA
Input bias current	V _{IN} = 0V	I _{IN-}	-	2	-	μA
ITRIP input bias current	V _{ITRIP} = 5V	I _{ITRIP+}	-	65	150	μA
VFO input bias current	V _{FO} = 5V, V _{ITRIP} = 0V	I _{FO}	-	2	-	nA
VFO output voltage	I _{FO} = 10mA, V _{ITRIP} = 1V	V _{FO}	-	0.5	-	V

Dynamic Parameters

($V_{DD} = 15V$ and $T_J = 25^\circ C$, if not stated otherwise)

Description	Condition	Symbol	Value			Unit
			min	typ	max	
Turn-on propagation delay time	$V_{LIN,HIN} = 5V,$ $I_{out} = 10A,$ $V_{DC} = 300V$	t_{on}	-	680	-	ns
Turn-on rise time		t_r	-	30	-	ns
Turn-on switching time		$t_{c(on)}$	-	220	-	ns
Reverse recovery time		t_{rr}	-	60	-	ns
Turn-off propagation delay time	$V_{LIN,HIN} = 0V,$ $I_{out} = 10A,$ $V_{DC} = 300V$	t_{off}	-	950	-	ns
Turn-off fall time		t_f	-	55	-	ns
Turn-off switching time		$t_{c(off)}$	-	120	-	ns
Short circuit propagation delay time	From $V_{IT,TH+}$ to 10% I_{SC}	t_{SCP}	-	1250	-	ns
Input filter time ITRIP	$V_{ITRIP} = 1V$	$t_{ITRIPmin}$	-	530	-	ns
Input filter time at LIN, HIN for turn on and off	$V_{LIN,HIN} = 0V \& 5V$	t_{FILIN}	-	290	-	ns
Fault clear time after ITRIP-fault	$V_{ITRIP} = 1V$	t_{FLTCLR}	40	-	-	μs
IGBT turn-on energy (includes reverse recovery of diode)	$V_{DC} = 300V,$ $T_J = 25^\circ C$ $I_C = 15A$ $150^\circ C$	E_{on}	-	400	-	μJ
			-	490	-	
IGBT turn-off energy	$V_{DC} = 300V,$ $T_J = 25^\circ C$ $I_C = 15A$ $150^\circ C$	E_{off}	-	190	-	μJ
			-	290	-	
Diode recovery energy	$V_{DC} = 300V,$ $T_J = 25^\circ C$ $I_C = 15A$ $150^\circ C$	E_{rec}	-	55	-	μJ
			-	70	-	

Bootstrap Parameters

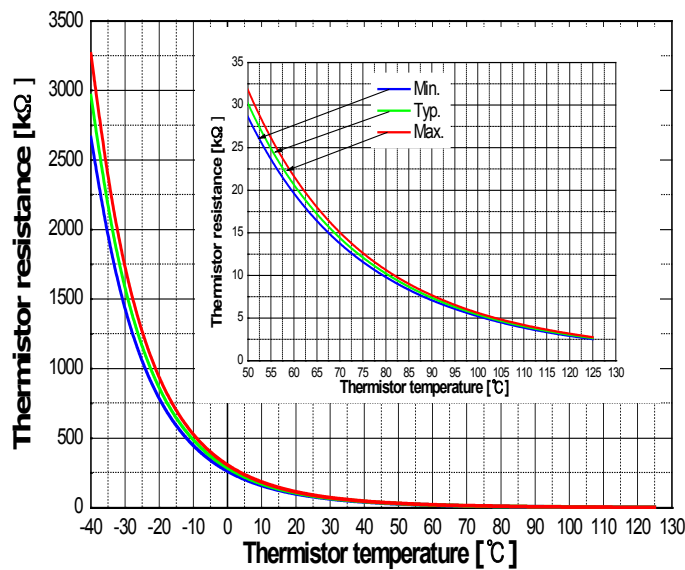
($T_J = 25^\circ C$, if not stated otherwise)

Description	Condition	Symbol	Value			Unit
			min	typ	max	
Repetitive peak reverse voltage		VRRM	600			V
Bootstrap resistance of U-phase ¹	$VS2$ or $VS3 = 300V,$ $T_J = 25^\circ C$	RBS1	-	35	-	Ω
	$VS2$ and $VS3 = 0V,$ $T_J = 25^\circ C$		-	40	-	
	$VS2$ or $VS3 = 300V,$ $T_J = 125^\circ C$		-	50	-	
	$VS2$ and $VS3 = 0V,$ $T_J = 125^\circ C$		-	65	-	
Reverse recovery time	$I_F = 0.6A,$ $di/dt = 80A/\mu s$	trr_BS		50	-	ns
Forward voltage drop	$I_F = 20mA,$ $VS2$ and $VS3 = 0V$	VF_BS		2.6	-	V

¹ R_{BS2} and R_{BS3} have same values to R_{BS1} .

Thermistor

Description	Condition	Symbol	Value			Unit
			min	typ	max	
Resistor	$T_{NTC} = 25^{\circ}\text{C}$	R_{NTC}	-	85	-	$k\Omega$
B-constant of NTC (Negative temperature coefficient)		B(25/100)	-	4092	-	K



T [°C]	Rmin. [kΩ]	Rtyp. [kΩ]	Rmax. [kΩ]
50	28.400	29.972	31.545
60	19.517	20.515	21.514
70	13.670	14.315	14.960
80	9.745	10.169	10.593
90	7.062	7.345	7.628
100	5.199	5.388	5.576
110	3.856	4.009	4.163
120	2.900	3.024	3.149
125	2.527	2.639	2.751

Figure 7: Thermistor resistance – temperature curve and table
(For more information, please refer to the application note ‘AN CIPOS mini-1 Technical Description’)

Mechanical Characteristics and Ratings

Description	Condition	Value			Unit
		min	typ	max	
Mounting torque	M3 screw and washer	0.49	-	0.78	Nm
Flatness	Refer to Figure 8	-50	-	100	μm
Weight		-	6.84	-	g

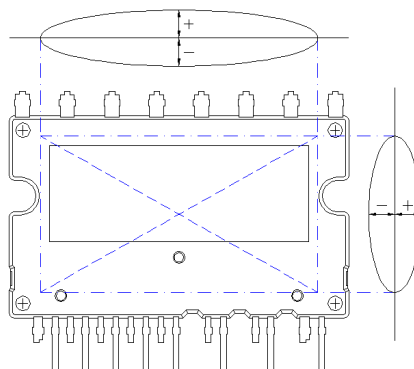


Figure 8: Flatness measurement position

Circuit of a Typical Application

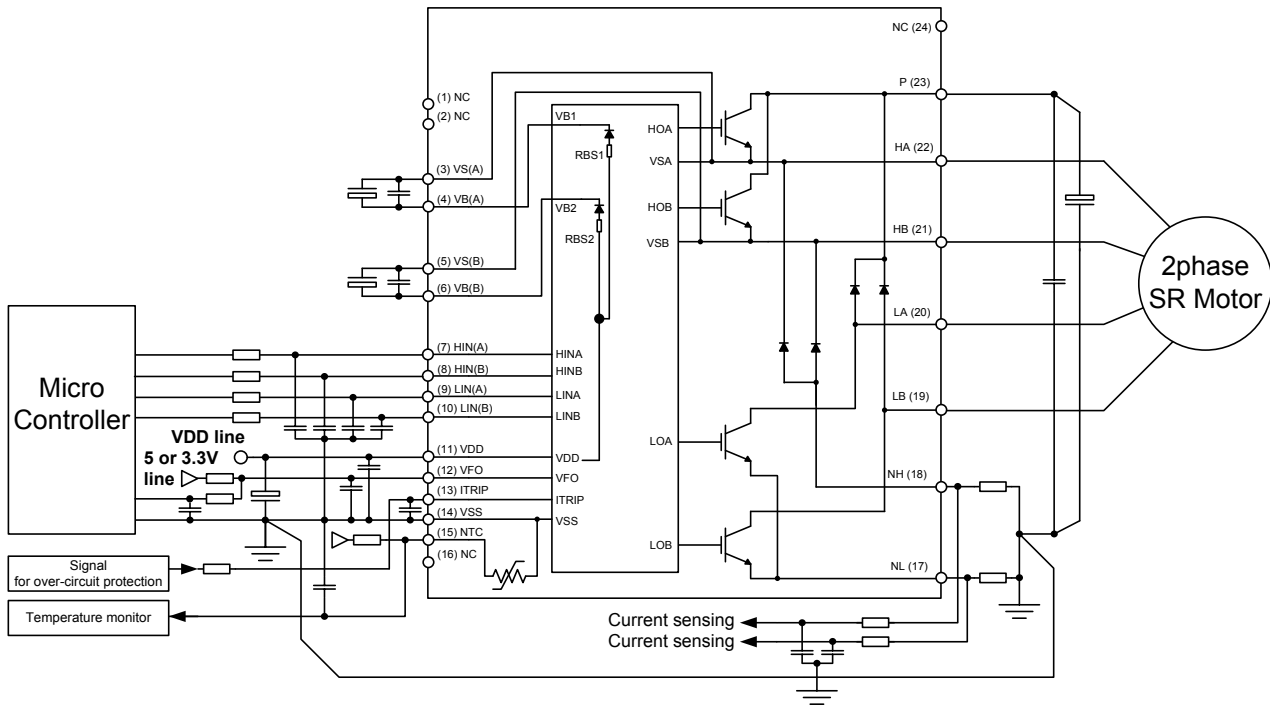


Figure 9: Application circuit

Switching Times Definition

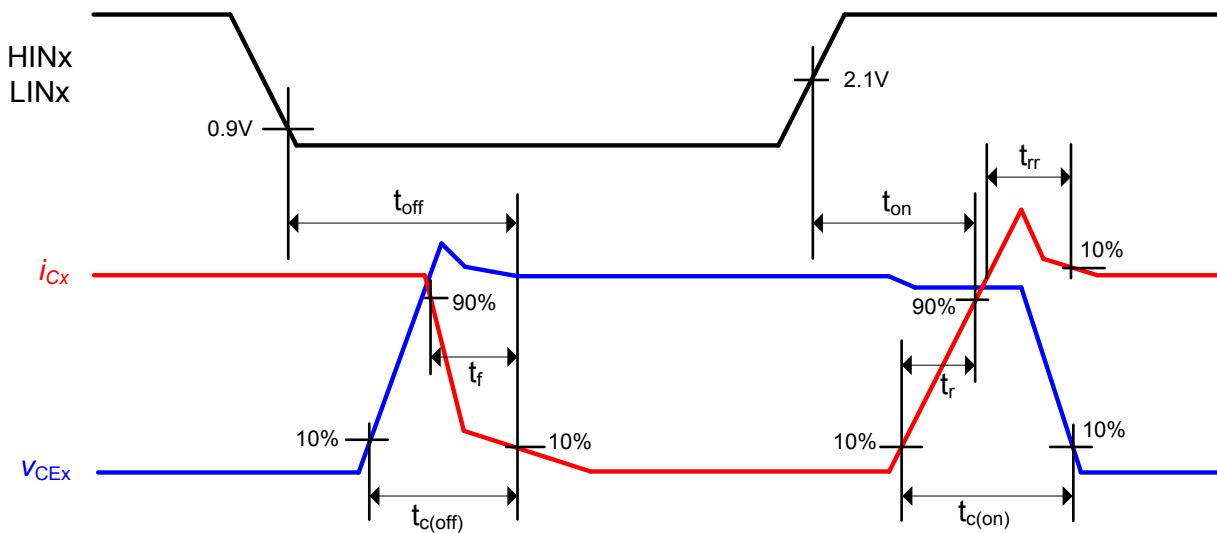
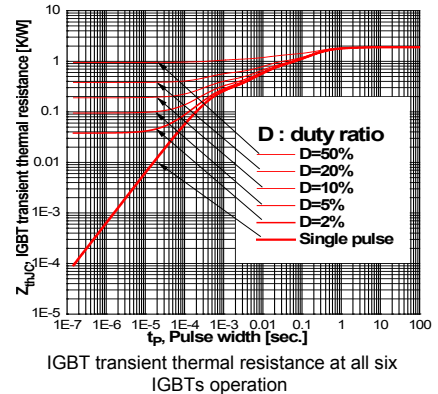
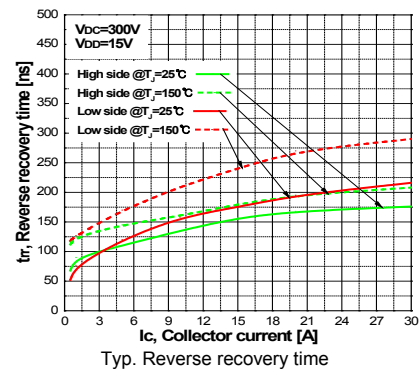
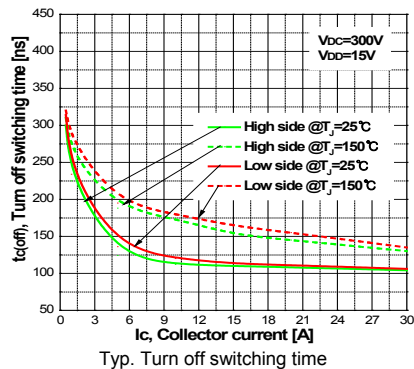
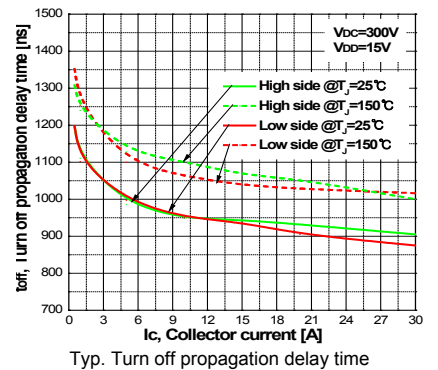
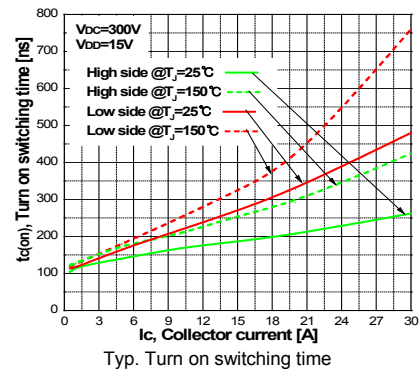
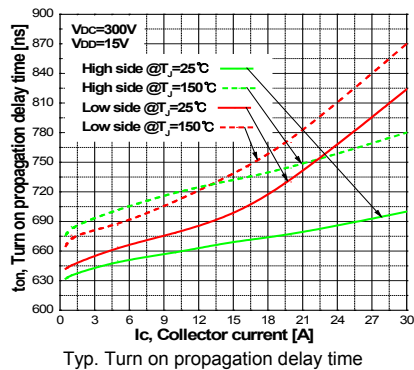
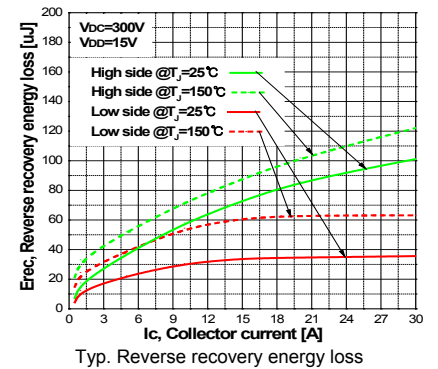
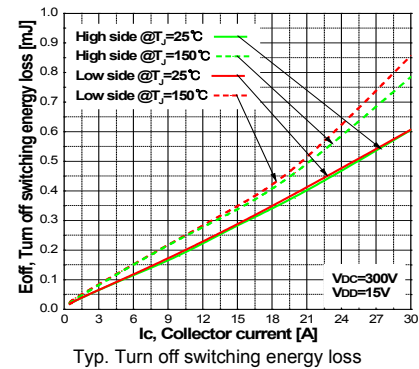
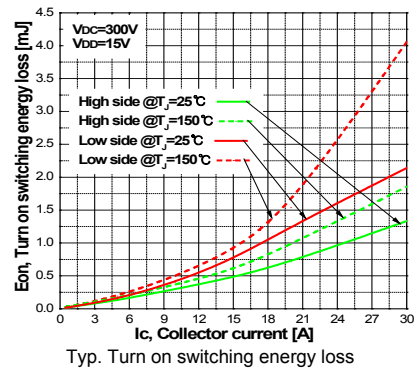
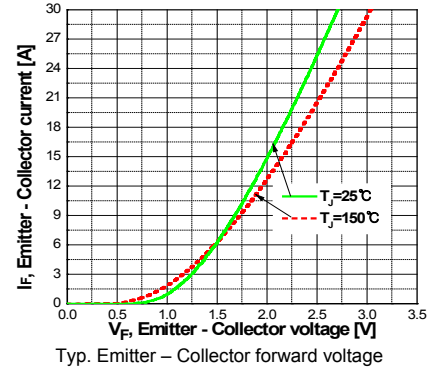
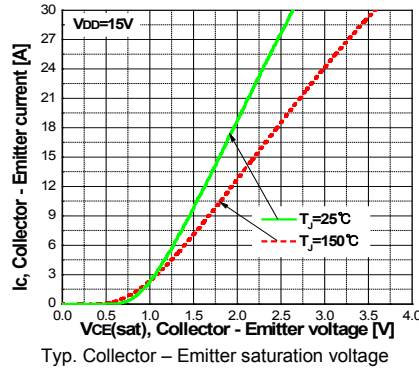
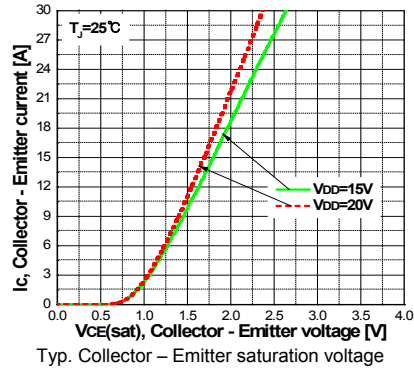
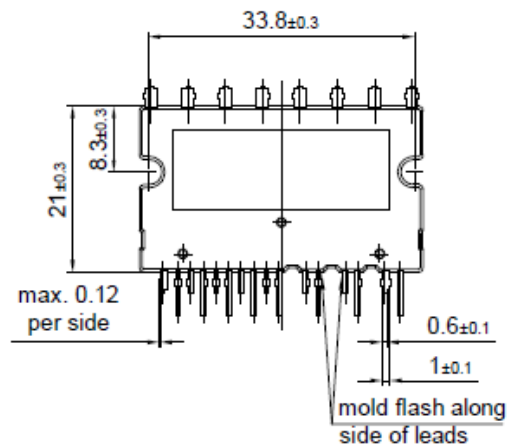
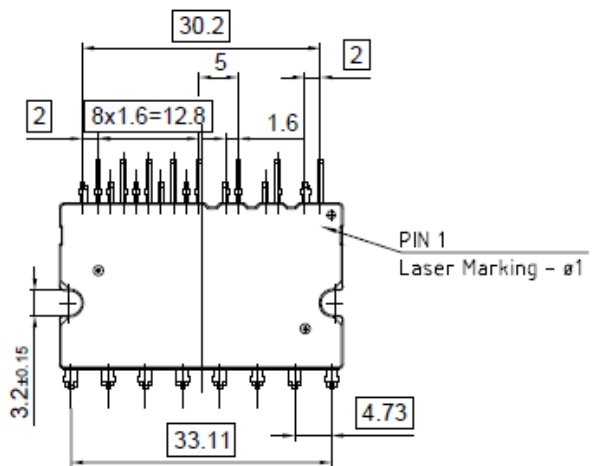
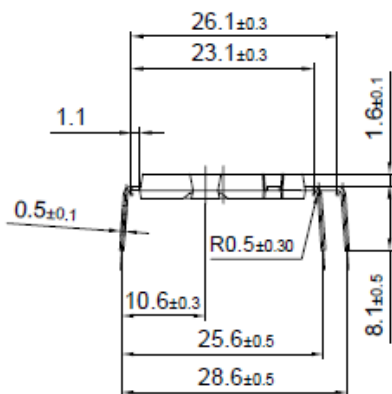
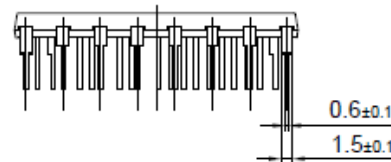
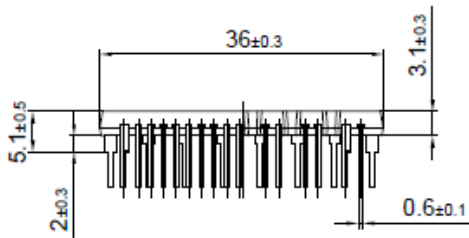


Figure 10: Switching times definition

Electrical characteristic



Package Outline



Revision History

Major changes since the last revision

Page or Reference	Description of change

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