

# ICL8105 - Digital Flyback Controller IC

.dp digital power 2.0

Datasheet

## About this document

### Scope and purpose

This document contains information about Infineon high-performance single-stage digital flyback controller ICL8105 for LED lighting applications. Features and electrical characteristics are listed and explained.

### Intended audience

This document is intended for customers wishing to design high-performance single-stage digital flyback AC-DC converters for LED lighting based on the ICL8105 controller.



## Revision History

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### Revision History

Page or Item	Subjects (major changes since previous revision)
Rev. 1.0, 2015-09-18	

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## Overview

### Product highlights

- Highly accurate primary side controlled output current (Line/load regulation typical within +/- 3%)
- High power quality (Typical PF up to 0.99 and THD < 10%)
- High Efficiency (up to 91%)
- Configurable output current with no BOM change
- Supports universal input voltage (85 – 305 V AC)
- Supports wide output voltage (up to 4 times of minimum output voltage)
- Supports fully isolated 0 – 10 V dimming. No extra ICs required.
- Supports low output current dimming.
- Low standby power

### Features

- Single stage QR Flyback with PFC and high precision primary side controlled constant current output
- Excellent line and load regulation
- Supports AC input (45 ~ 65 Hz) and/or DC input voltage operation
- Integrated 600 V startup cell
- Low Bill Of Material (BOM)
- Configurable parameters, e.g. adjustable voltage and current ranges, protection modes
- Supports Non-Dimmed and/or Dimmed applications.
- Intelligent thermal management with adaptive thermal protection

### Applications

- Electronic Control Gear for LED luminaires (5 W to 80 W)

### Description

The ICL8105 is a high performance microcontroller-based digital single-stage flyback controller with power factor correction (PFC) for constant output current applications. The IC is available in a DSO-8 package and supports a wide feature set, requiring a minimum of external components. The digital engine offers the possibility to configure operational parameters and protection modes, which helps to ease the design phase and allows a reduced number of Hardware variants in production. Accurate primary side output current control is implemented to eliminate the need for secondary side feedback circuitry.

**Table 1**

Product Type	Package
ICL8105	PG-DSO-8

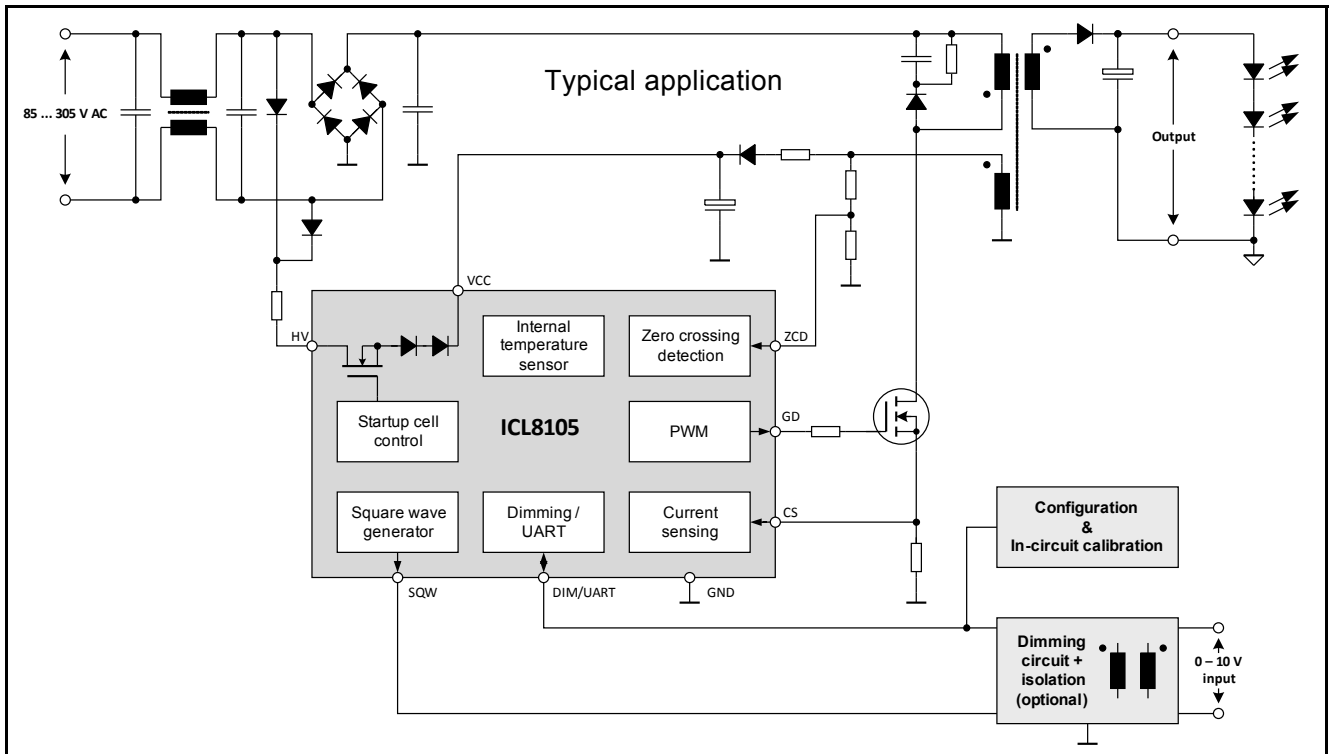
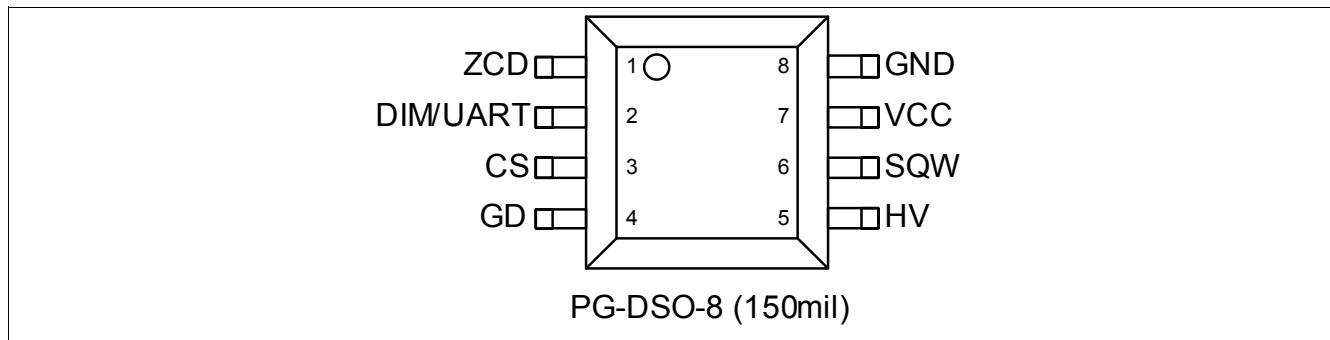


Figure 1 Typical application

Pin configuration and description

## 1 Pin configuration and description

The pin configuration is shown in [Figure 2](#). The pin functions are listed and described in [Table 2](#).



**Figure 2** Pin configuration

**Table 2** Pin definitions and functions

Symbol	Pin	Type	Function
ZCD	1	I	<b>Zero crossing detection</b> Pin ZCD is connected to an auxiliary winding for zero crossing detection. Output & input voltage are measured via this pin with sampled positive & negative voltage sensing
DIM/UART	2	I/O	<b>Dimming / UART</b> Shared functioning pin with either as Dimming Input or UART configuration. Based on the IC condition, it will select to enter which function.
CS	3	I	<b>Current sense</b> Pin CS is connected to an external shunt resistor and the source of the power MOSFET.
GD	4	O	<b>Gate driver</b> Output signal to drive an external power mosfet.
HV	5	I	<b>High voltage</b> Pin HV is connected to the rectified input voltage via external resistor. An internal 600 V HV startup-cell is used to pre-charge VCC for IC startup once the mains input voltage is applied. Furthermore sampled high voltage sensing is used for synchronization with the input voltage frequency.
SQW	6	O	<b>Square wave generator</b> PIN SQW provides a square wave signal for driving the isolated dimming transformer circuit. The signal can be turned off for non-dimmed or non-isolated dimming applications.
VCC	7	I	<b>Voltage supply</b> IC power supply
GND	8	—	<b>Power and signal ground</b>

## Functional description

## 2 Functional description

The functional description provides an overview about the integrated functions and features as well as their relationship. The mentioned parameters and equations are based on typical values at  $T_A = 25^\circ\text{C}$ . The corresponding min. and max. values are shown in the electrical characteristics.

### 2.1 Introduction

The ICL8105 is a digital AC/DC flyback controller with Power Factor Correction (PFC). The PFC function enables a rectified sinusoidal input current waveform with a power factor typically up to 0.99 and THD < 10% for a wide range of operating conditions. ICL8105 provides primary side constant output current control that avoids the secondary side control feedback loop circuitry usually needed in isolated power converters. This approach supports a low part count that is necessary to build up the application. ICL8105 uses multi-mode operations to select the best mode of operation based on operation conditions. The multi-mode operation will automatically switch between quasi-resonant mode (QRM) and discontinuous mode (DCM) and active burst mode (ABM). In addition, ICL8105 supports 0 - 10 V dimming functionality with no additional microcontroller. Digital and RF interfaces can be supported by a microcontroller using a digital-to-analog converter.

The ICL8105 provides a high flexibility in the design-in of the application. A graphic user interface (GUI) tool supports users to tune a set of configurable parameters. The configuration can be done via a single pin UART interface at pin DIM/UART.

### 2.2 Controller features

**Table 3** gives an overview about the controller features that are described in the mentioned chapters.

**Table 3** Controller features

Primary side voltage and current sensing	Chapter 2.2.1
Primary side control scheme for output current control	Chapter 2.2.2
Power factor correction (PFC)	Chapter 2.2.3
Dimming via pin DIM/UART	Chapter 2.2.4
Wide output voltage range circuit (optional)	Chapter 2.2.6
Automatic output discharge circuit (optional)	Chapter 2.2.7
VCC startup function combined with direct input monitoring	Chapter 2.2.8
Configurable soft start	Chapter 2.2.9
Configurable gate voltage rising slope at pin GD (Lower EMI)	Chapter 2.2.10

Functional description

2.2.1 Primary side voltage and current sensing

The ICL8105 provides a primary side control of the output current by means of measuring the input peak current and measuring the period of conduction of the output diode. Input and output voltages are measured at pin ZCD using an external resistor divider and an auxiliary winding of the transformer. The voltage signal  $V_{AUX}$  contains the information of the rectified input voltage  $V_{in}$  and the output voltage  $V_{out}$  at the secondary side. **Figure 3** shows typical current and voltage waveforms of the Quasi-Resonant flyback application.

The following topics are described:

- Input current sensing via pin CS and output current calculation (**Chapter 2.2.1.1**)
- Input voltage sensing via pin ZCD (**Chapter 2.2.1.2**)
- Output voltage sensing via pin ZCD (**Chapter 2.2.1.3**)

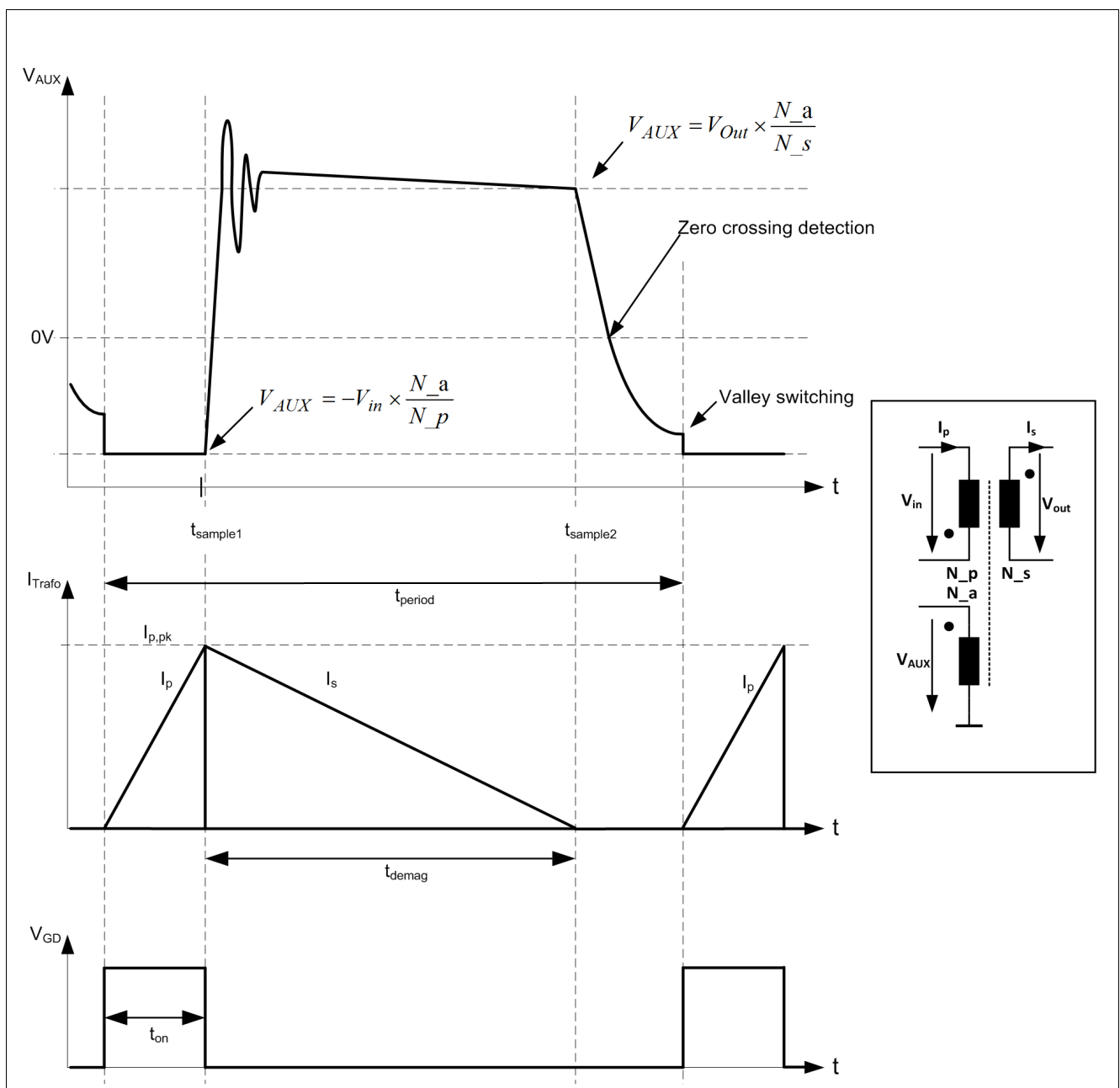


Figure 3 Typical waveforms (Example with QRM valley switching)

Functional description

2.2.1.1 Input current sensing via pin CS and output current calculation

The output current  $I_{out}$  is determined by the primary input peak current  $I_{p,pk}$  which is sensed at pin CS at time  $t_{sample1}$ , by the duration of conduction of the output diode ( $t_{sample2} - t_{sample1}$ ) and by the switching period  $t_{period}$ . The result is used for the control loop and for output overcurrent protections (Chapter 2.3.7).

2.2.1.2 Input voltage sensing via pin ZCD

The input voltage is measured using current  $I_{IV}$  at pin ZCD at time  $t_{sample1}$ . As the voltage  $V_{AUX}$  is a negative voltage, pin ZCD is clamped to a fixed negative voltage  $V_{INPCLN}$  (Figure 4). The negative current  $I_{IV}$  (flowing out of pin ZCD) is proportional to the input voltage. The monitored input voltage is used for input over- and undervoltage protection (Chapter 2.3.4).

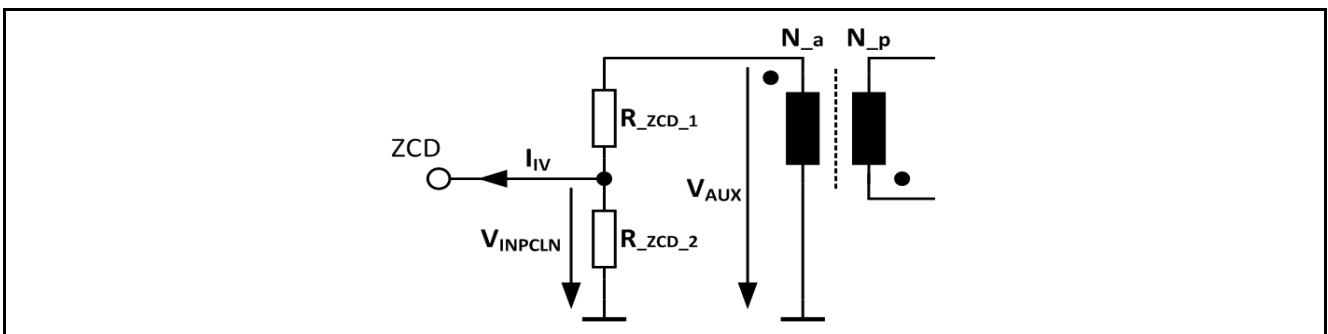


Figure 4 Input voltage sensing via pin ZCD

2.2.1.3 Output voltage sensing via pin ZCD

The output voltage is measured using voltage  $V_{ZCD SH}$  at pin ZCD at time  $t_{sample2}$  (Figure 5). The measured voltage at pin ZCD and the dimensioning of the resistor divider are used to calculate the reflected output voltage  $V_{out,aux}$  at the auxiliary winding.  $V_{out,aux}$  is used for output over- and undervoltage protection (Chapter 2.3.3). The relation between VCC and ZCD can be decoupled by adding a regulator for VCC (Chapter 2.2.6).

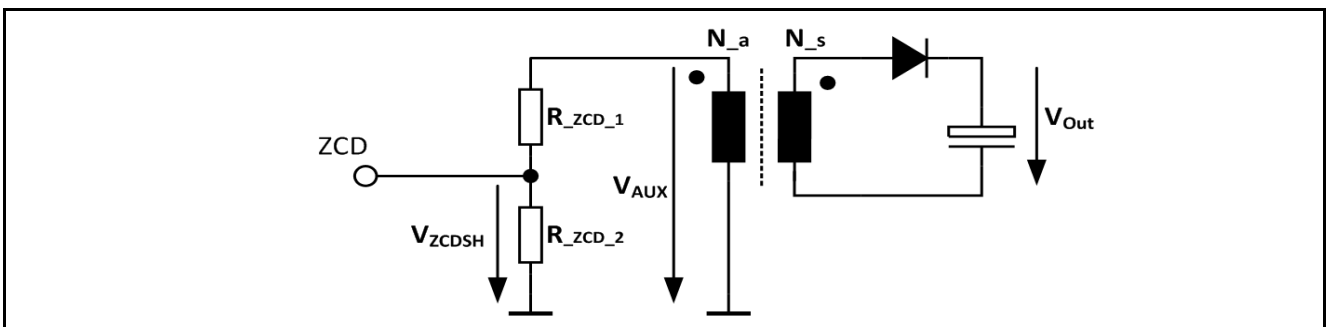


Figure 5 Output voltage sensing via pin ZCD

Note: Please note that the time ( $t_{sample2} - t_{sample1}$ ) has to be longer than 2.0  $\mu s$  to ensure that the reflected output voltage can correctly be sensed at pin ZCD!

Functional description

2.2.2 Primary side control scheme for output current control

The basic control scheme for the primary side constant current control is shown in Figure 6.

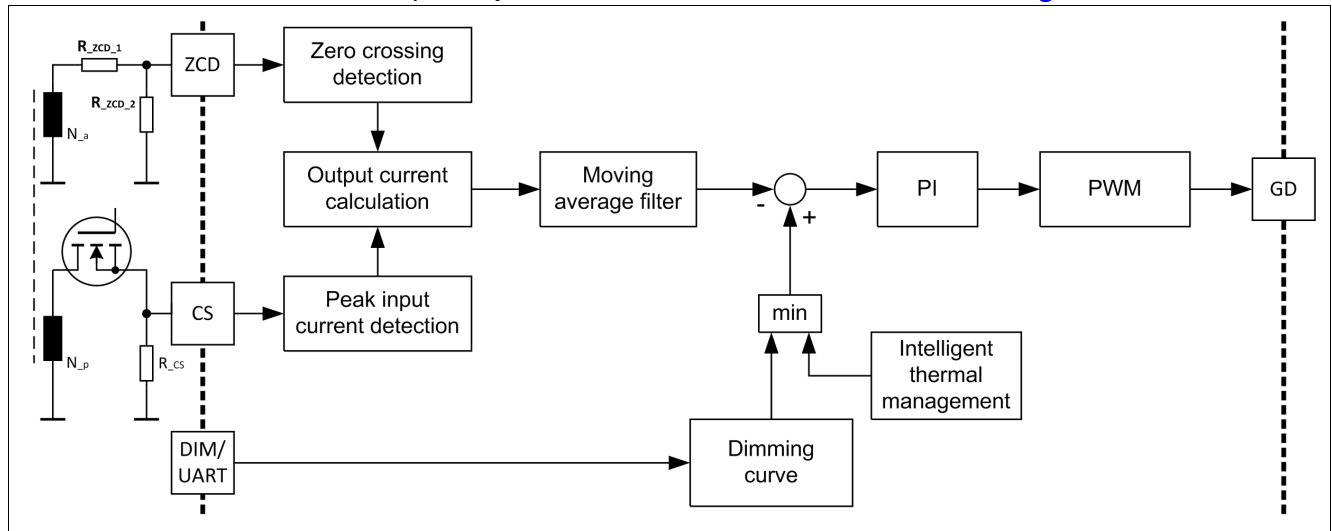


Figure 6 Integrated PI control scheme for output current control

The sampled signal  $V_{CS}$  at pin CS is used to estimate the output current  $I_{out}$  as described in Chapter 2.2.1.1. The internal reference current  $I_{out\_set}$  is weighted according to thermal management and dimming curve. The average estimated output current is compared with the weighted reference current to generate an error signal. The error signal is fed into a PI regulator to control the PWM at pin GD for the power MOSFET. The coefficients of the PI regulator are configurable.

The PI regulator allows different modes of operation as shown in Figure 7:

- Quasi-resonant mode (QRM)  
 This mode maximizes the efficiency by switching on at the 1st valley of the  $V_{AUX}$  signal. This ensures zero-current switching with a minimum of switching losses.
- Discontinuous mode (DCM)  
 This mode is used if the on-time cannot be reduced further. The controller will extend the switching period later than the 1st valley to control the output power.
- Active-Burst mode (ABM)  
 To extend the dimming range even further, ICL8105 features an ABM which is automatically aligned with the input frequency to avoid any undesired effects like flicker or shimmer as well as to reduce any audible noise.

The controller will autonomously select the best mode of operation based on operation conditions like input voltage, input frequency and dimming input voltage which defines the output power.

Functional description

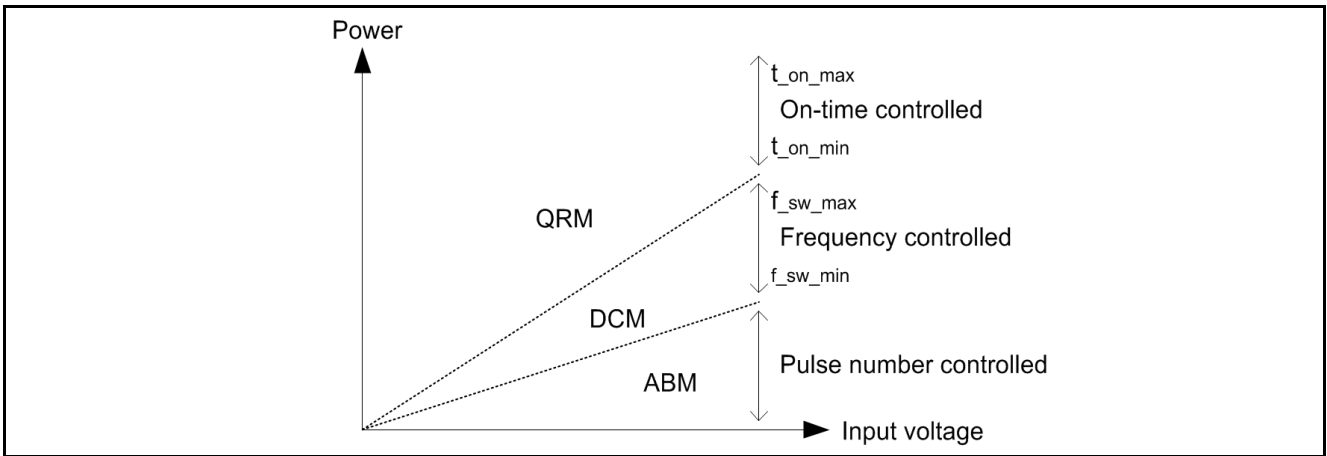


Figure 7 Overview of operation modes

### 2.2.3 Power factor correction (PFC)

The gate driver GD is used for driving the power MOSFET of the flyback. Constant output current regulation and a sinusoidally shaped input current are achieved by on-time control. The quasi-constant on-time  $t_{on}$  ensures high PF and low THD performance. The internal control signal  $t_{on}$  is calculated by the digital engine so that the output current is close to the target current (Chapter 2.2.2).

Optionally, an enhanced PFC (EPFC) scheme can be enabled to compensate the input current distortion caused by the EMI filter<sup>1)</sup>. In this scheme, the on-time is a function of the internal controller signal  $t_{on}$ , the input voltage  $V_{in}$ , output voltage  $V_{out}$ , output current  $I_{out}$ , phase angle and a configurable gain parameter ( $C_{EMI}$ ) optimizing the input current waveform (Chapter 2.4).

### 2.2.4 Dimming via pin DIM/UART

The voltage sensed at pin DIM/UART is used to determine the output current level. Figure 8 shows the relation of DIM/UART voltage to the output current target value. Levels of  $V_{DIM\_min}$  and  $V_{DIM\_max}$  ensure that minimum current  $I_{out\_min}$  and maximum current  $I_{out\_set}$  can always be achieved, making the application robust against dimmer and other component tolerances. The sampled voltage  $V_{DIM}$  at pin DIM/UART is digitally filtered to stabilize light output. The ICL8105 can be configured to use a linear or a quadratic dimming curve.

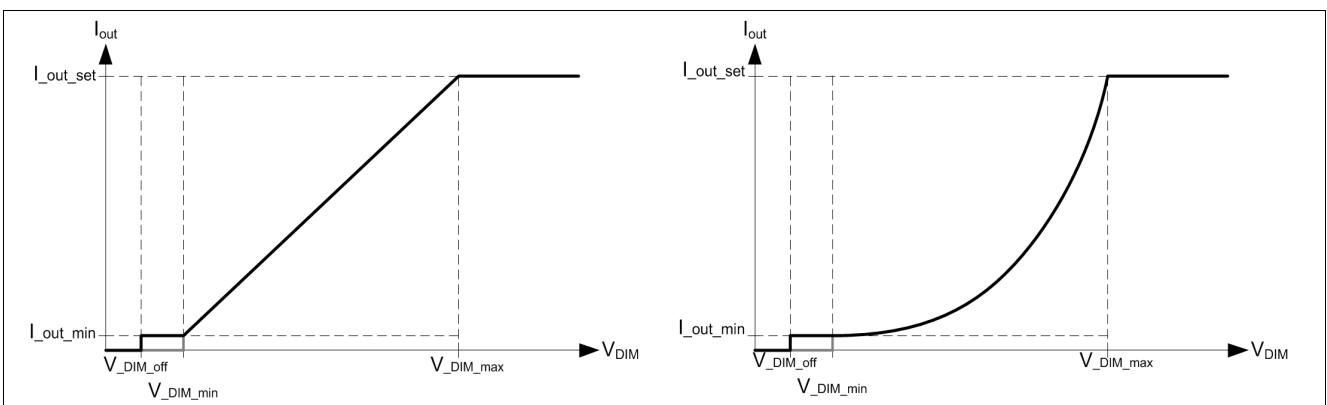


Figure 8 Dimming curves for pin DIM/UART

1) Patent pending

Functional description

Optionally, The output current can be turned off completely below a DIM/UART voltage of  $V_{DIM\_off}$ .

*Note: The dim-to-off feature requires an active voltage source to exit the dim-to-off state.*

In some cases where the dimming control circuitry is on the primary side and it is using PWM control, please refer ICL8105 design guide for the circuit which will convert the PWM dimming signal to an analog dimming voltage that is used by the DIM/UART pin for the required dimming.

2.2.5 Isolated dimming interface via pin SQW (optional)

Figure 9 shows an exemplary schematic of a 0 - 10 V dimming interface for low BOM cost. The interface is optimized to consume only a minimum of power. Pin SQW can generate a square wave signal with a 50% duty cycle. This allows the dimming circuitry to transfer the isolated dimming voltage level to primary side.

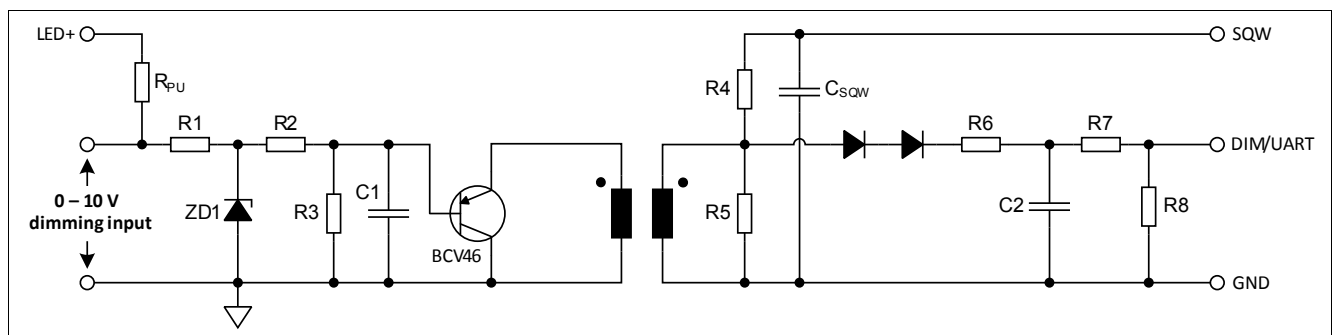
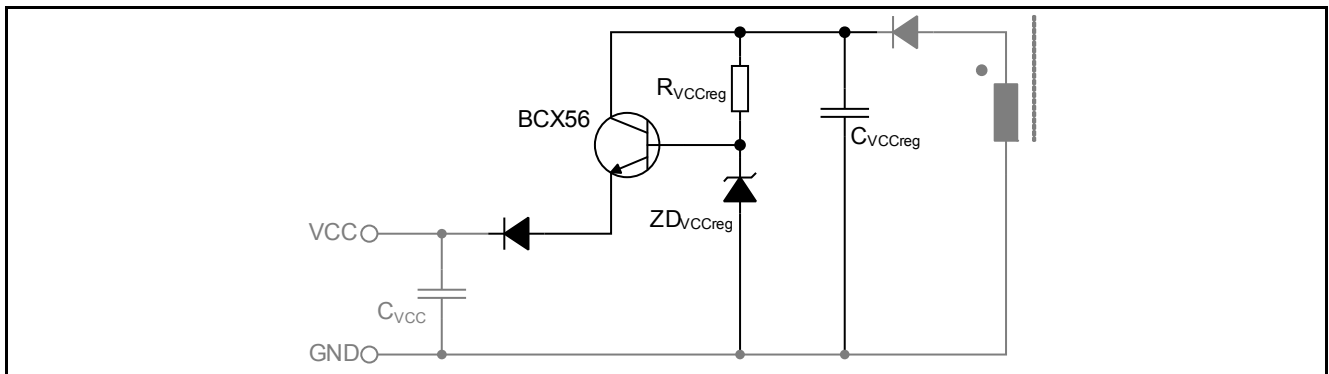


Figure 9 Optional circuit for isolated dimming

Functional description

### 2.2.6 Wide output voltage range circuit (optional)

To achieve a wide range of output voltage a regulator for VCC is required. This regulator limits the maximum voltage at pin VCC during steady state operation. **Figure 10** shows an exemplary schematic for the optional wide output voltage range support. A wide output voltage range impacts efficiency due to the necessary voltage regulator for VCC.



**Figure 10** Optional wide output voltage range circuit

### 2.2.7 Automatic output discharge circuit (optional)

In case of a fault (e.g. Open Load) the output capacitors stay charged and may keep a high voltage. It is therefore recommended to add an automatic output discharge circuit. This circuit discharges the output capacitors if the main switch stops switching. More details can be found in the ICL8105 application note.

### 2.2.8 VCC startup function combined with direct input monitoring

There are two main functions supported at pin HV which needs to be connected to the input voltage via resistor and two diodes.

The integrated HV startup-cell is switched on during the VCC startup phase before the IC is activated. Current flows from pin HV to pin VCC via an internal diode, which charges the capacitor at pin VCC. Once the voltage at pin VCC exceeds the  $V_{VCCon}$  threshold, the IC enables the active operating phase and switches off the HV startup-cell.

Furthermore, a direct input monitoring is supported that is controlled by an internal timer. The timer switches on the HV startup cell for a very short time after a defined period. During this short on-time the current is sensed at pin HV by a comparator to synchronize to frequency and phase of the input voltage.

### 2.2.9 Configurable soft start

After startup, the IC initiates a soft-start. During soft-start, the switching stress for the power MOSFET, diode and transformer is minimized. The cycle-by-cycle current limit is increased in steps with a configurable time  $t_{ss}$  for each step. The number of soft start steps is defined by parameter  $n_{ss}$ . After the final CS limit level has been reached, the output will be charged up with maximum on-time and maximum CS limitation level to the minimum output voltage that ensures self-supply. After the minimum output voltage has been reached, the current control loop (**Chapter 2.2.2**) takes over and output undervoltage protection is activated (if enabled by configuration).

Functional description

### 2.2.10 Configurable gate voltage rising slope at pin GD (Lower EMI)

The gate driver output signal can be configured with respect to the rising slope for switching on the power MOSFET. This feature can save BOM components (1 diode & 1 resistor) which are conventionally added to achieve the same purpose for EMI improvement. The maximum gate drive current  $I_{GD\_pk}$  for the gate driver slope can be set between 30 mA and 118 mA (Chapter 2.4). Figure 11 shows the gate driver output signal.

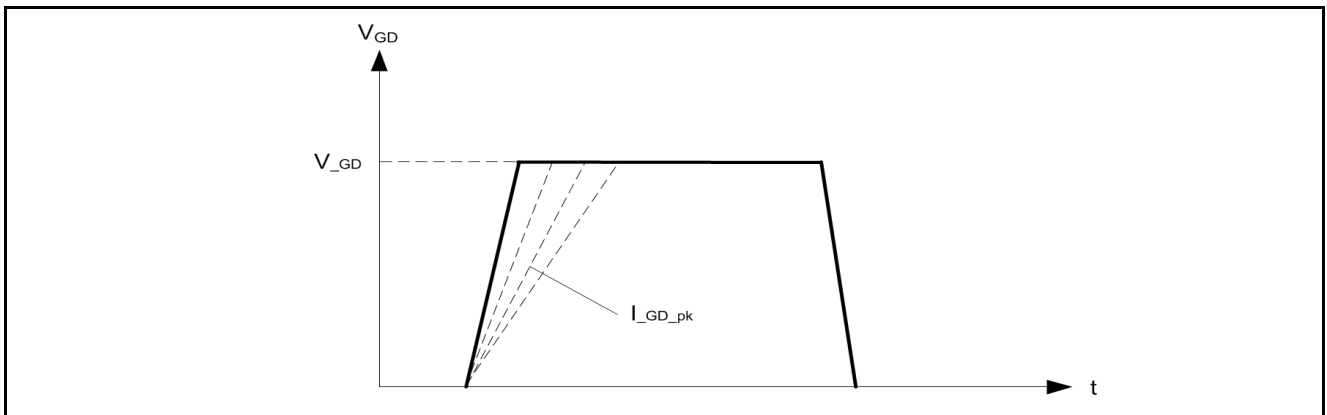


Figure 11 Configurable gate voltage rising slope for lower EMI

Functional description

## 2.3 Protection features

**Table 4** gives an overview about the available protection features and corresponding default actions in case a protection feature is triggered. Two protection reactions (auto restart mode and latch mode) are implemented.

### Auto restart mode

Once the auto restart mode is activated, the IC stops the power MOSFET switching at pin GD and reduces the current consumption to a minimum. After the configurable auto restart time  $t_{\text{auto\_restart}}$  the IC initiates a new start-up<sup>1)</sup>. During this auto restart the HV startup-cell is switched on and off in order to keep the VCC between  $V_{\text{UVLO}}$  and  $V_{\text{OVLO}}$  thresholds<sup>2)</sup>. The auto restart cycle starts first with charging the VCC capacitor by means of switching on the HV startup cell until the  $V_{\text{VCCon}}$  threshold is exceeded. A regular startup procedure with soft start is initiated afterwards.

### Latch mode

When latch mode is activated the power MOSFET switching at pin GD is immediately stopped. The HV startup-cell is switched on and off in order to keep the VCC between  $V_{\text{UVLO}}$  and  $V_{\text{OVLO}}$  thresholds. The device stays in this state until input voltage is completely removed and the VCC voltage drops below the  $V_{\text{UVLO}}$  threshold. The IC can then be re-started by applying input voltage.

**Table 4 Protection Features**

Protection Feature	Active	Predefined Reaction	Description
Undervoltage lockout for VCC	Always on	Auto restart	<a href="#">Chapter 2.3.1</a>
Overvoltage protection for VCC	Always on	Latch mode	<a href="#">Chapter 2.3.2</a>
Overvoltage protection for $V_{\text{out}}$	Always on	Auto restart <sup>1)</sup>	<a href="#">Chapter 2.3.3</a>
Undervoltage protection for $V_{\text{out}}$	Activated after startup <sup>1)</sup>	Auto restart	<a href="#">Chapter 2.3.3</a>
Overvoltage protection for $V_{\text{in}}$	Always on <sup>1)</sup>	Latch mode	<a href="#">Chapter 2.3.4</a>
Undervoltage protection for $V_{\text{in}}$	Always on <sup>1)</sup>	Auto restart	<a href="#">Chapter 2.3.4</a>
Input overcurrent detection level 1	Always on	Current limiting	<a href="#">Chapter 2.3.5</a>
Input overcurrent protection level 2	Always on	Latch mode	<a href="#">Chapter 2.3.6</a>
Output current protection (average)	Activated after startup <sup>1)</sup>	Auto restart	<a href="#">Chapter 2.3.7</a>
Output current protection (peak)	Activated after startup <sup>1)</sup>	Auto restart	<a href="#">Chapter 2.3.7</a>
Overtemperature protection	Always on	Latch mode	<a href="#">Chapter 2.3.8</a>
Firmware protections (1st Watchdog & RAM Parity)	Always on	Auto restart	<a href="#">Chapter 2.3.9</a>

1) Configurable

1) After  $t_{\text{auto\_restart}}$  the VCC will be charged to  $V_{\text{VCCon}}$  again. Therefore, the effective auto-restart time is longer than  $t_{\text{auto\_restart}}$  (see [Chapter 2.2.8](#))

2) This feature can be disabled for applications with externally supplied VCC.

Functional description

### 2.3.1 Undervoltage lockout for VCC

An undervoltage lockout unit (UVLO) is implemented which ensures a defined enabling and disabling of the IC operation depending on the supply voltage at pin VCC. The UVLO contains a hysteresis with the voltage thresholds  $V_{VCCon}$  for enabling the IC and  $V_{UVOFF}$  for disabling the IC. Once the mains input voltage is applied, current flows through an external resistor into pin HV via the integrated diode to pin VCC. The IC is enabled once VCC exceeds the threshold  $V_{VCCon}$  and enters normal operation if no fault condition is detected. In this phase VCC will drop until the self supply via the auxiliary winding takes over the supply at pin VCC. In case of output short, the auxiliary winding cannot provide power to VCC. A timeout of  $t_{start\_max}$  is available to capture this failure condition. The self supply via the auxiliary winding must be in place before the output short timeout occurs or before VCC falls below the  $V_{UVOFF}$  threshold. Otherwise, the system will do a fast restart.

### 2.3.2 Overvoltage protection for VCC

Overvoltage detection at pin VCC is implemented via a threshold  $V_{VCC\_max}$ .

### 2.3.3 Over / undervoltage protection for output voltage

Overvoltage (e.g. Open Load) or undervoltage (e.g. Output short) detection of the output voltage  $V_{out}$  is provided by the measurement and calculation as described in [Chapter 2.2.1.3](#). Over / undervoltage detection thresholds  $V_{outOV}$  and  $V_{outUV}$  can be configured ([Chapter 2.4](#)). Output undervoltage protection is disabled during startup. For output overvoltage protection in auto-restart reaction, either slow auto-restart or fast auto-restart can be selected. The startup threshold  $V_{out\_start}$  has to be configured above the undervoltage threshold to allow for undershoots (especially for resistive loads).

*Note: Please note that there are possibilities where critical protection like output over-voltage not working properly (example: wrong parameter configurations loaded). Thus, please consider adding zener diode or any voltage suppressor device/circuit on output for reinforced safety purpose.*

*Note: It is mandatory to have output discharge resistor/circuit which discharges the output capacitor after triggering open load protection at  $V_{outOV}$ . Latch reaction is recommended for open load protection as it can shut down the unit to prevent output overcharged if the discharge resistor ohmic value is too high.*

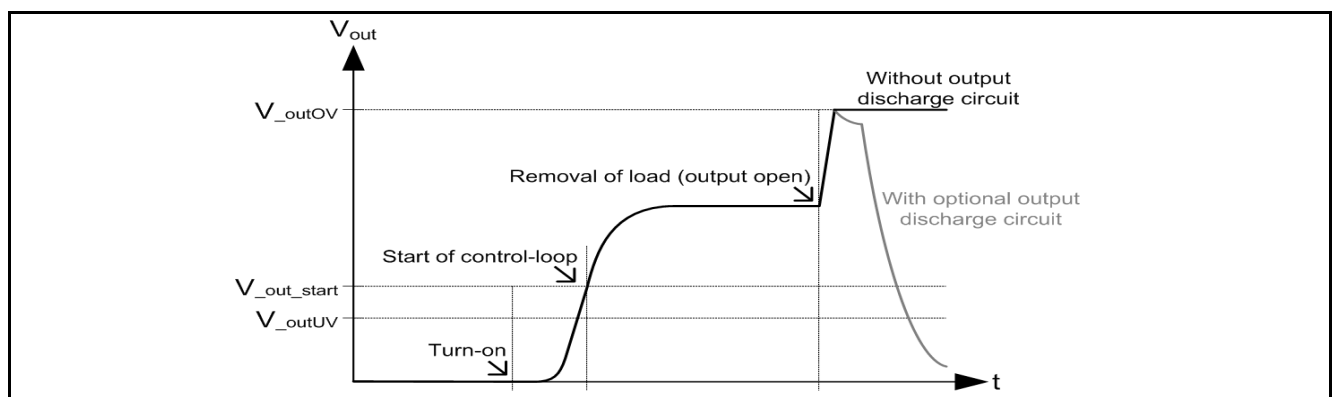


Figure 12 Voltage threshold for output over / undervoltage protection

### 2.3.4 Over / undervoltage protection for input voltage

An over / undervoltage detection of the input voltage  $V_{in}$  is provided by the measurement and calculation as described in [Chapter 2.2.1.2](#). Peak values of  $V_{in}$  are compared to the configurable internal input over / undervoltage protection thresholds  $V_{inOV}$  and  $V_{inUV}$  ([Chapter 2.4](#)).

Functional description

Figure 13 shows an exemplary setting of both over- and undervoltage thresholds together with configurable startup thresholds  $V_{in\_start\_min}$  and  $V_{in\_start\_max}$  to create hysteresis for flicker-free operation at auto-restart.

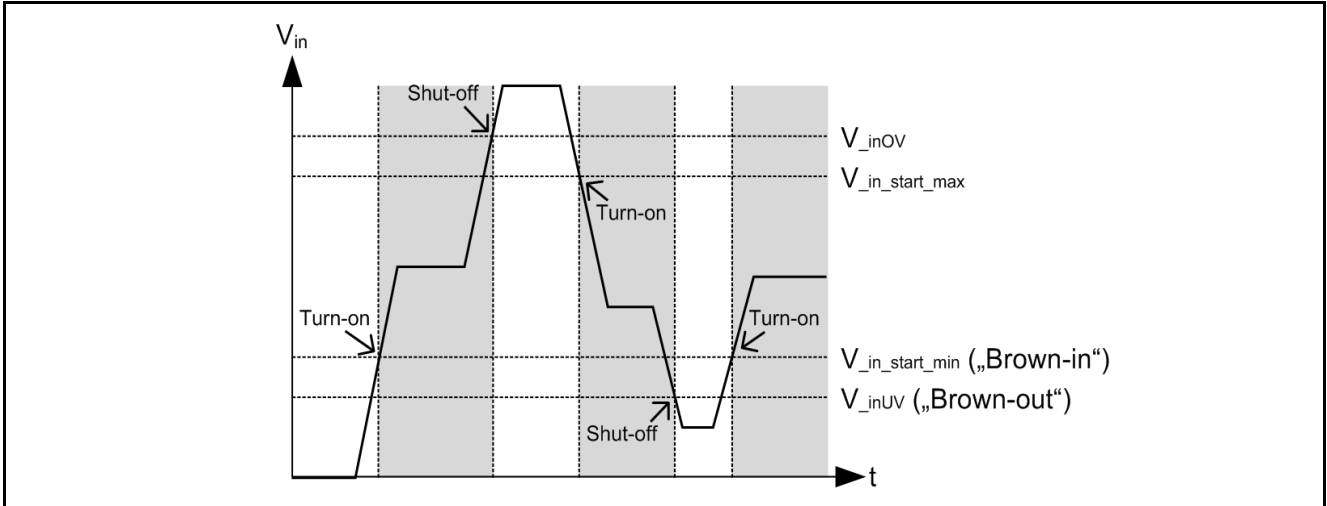


Figure 13 Voltage threshold for input over / undervoltage protection

### 2.3.5 Input overcurrent detection level 1 (OCP1)

The input overcurrent protection level 1 is performed by means of the cycle-by-cycle peak current limitation to  $V_{ocp1}$ . A leading edge blanking,  $t_{CSLEB}$  prevents the IC from falsely switching off the power MOSFET due to a leading edge spike.

### 2.3.6 Input overcurrent protection level 2 (OCP2)

The input overcurrent protection level 2 is meant for covering fault conditions like a short in the transformer primary winding. In this case overcurrent protection level 1 will not limit properly the peak current due to the very steep slope of the peak current. Once the threshold  $V_{ocp2}$  is exceeded for longer than  $t_{CSOCP2}$ , the protection is triggered.

### 2.3.7 Output overcurrent protections

The ICL8105 includes protections against exceeding an average and peak current limit. The average output current is calculated over one half cycle of the input frequency to remove the output current ripple. With auto-restart reaction, either slow auto-restart or fast auto-restart can be selected.

### 2.3.8 Overtemperature protection

ICL8105 offers a conventional as well as an adaptive overtemperature protection scheme using an internal temperature sensor.

*Note: Please note that the internal temperature sensor may not be able to sense and protect the temperature of external components (e.g. power MOSFET, VCC regulator) without sufficient thermal coupling.*

#### Conventional overtemperature protection

The overtemperature protection initiates a thermal shutdown once the internal temperature detection level  $T_{critical}$  is reached. With latch mode protection, IC will turn off and only restart after recycling of input power. At startup, junction temperature has to be below  $T_{start}$ .

Functional description

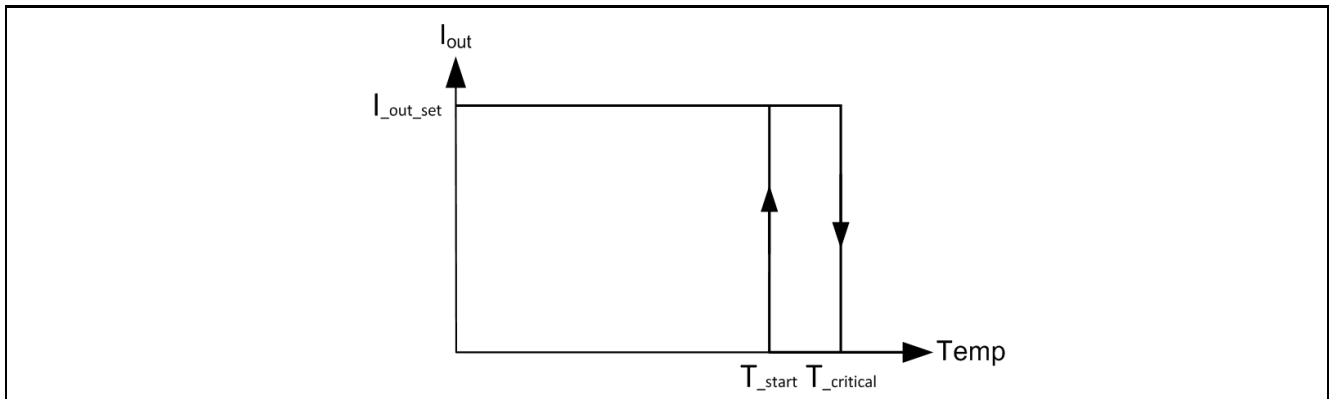


Figure 14 Conventional temperature protection

Adaptive temperature protection

To protect load and driver against overtemperature, ICL8105 features a reduction of output current below maximum current  $I_{out\_set}$ . As long as temperature  $T_{hot}$  is exceeded, the current is gradually reduced as shown in Figure 15. If a reduction down to a minimum current  $I_{out\_red}$  is not able to compensate the increase of temperature, IC will turn off at temperature  $T_{critical}$ .

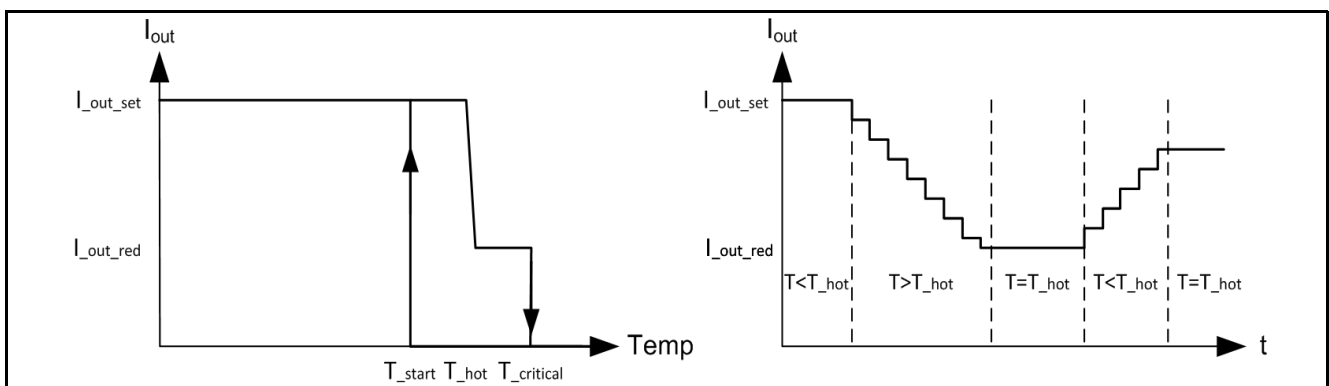


Figure 15 Adaptive temperature protection

2.3.9 Firmware protections

ICL8105 includes several protections to ensure the integrity and flow of the firmware:

- A hardware watchdog triggers a protection in case the firmware does not service the watchdog within a defined time period.
- A RAM parity check triggers a protection in case a bit in the memory flips.
- A cyclic redundancy check (CRC) at each startup verifies the integrity of firmware and parameters.
- A first firmware watchdog triggers a protection if the ADC hardware cannot provide all necessary information within a defined time period. This may occur if timing requirements for the ADC are exceeded.
- A second firmware watchdog triggers a protection if the execution of protection checks and the control loop are not matching a defined time period. This may occur if timing requirements are exceeded (e.g. operation beyond frequency limits).

Functional description

## 2.4 Configuration and support

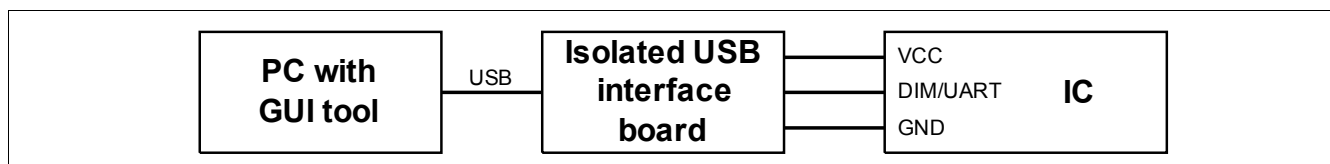
The configuration of ICL8105 is supported by the GUI tool .dp vision provided by Infineon. This chapter describes the configuration procedure via the UART interface. Furthermore, it contains an overview about the parameters and functions that can be configured.

### 2.4.1 Configuration procedure and design-in support

**Figure 16** shows the setup for the configuration of ICL8105. The Infineon graphic user interface (GUI) .dpVision connects via the isolated .dp Interface Board Gen2 to ICL8105. The isolated USB interface board provides power via VCC to ICL8105 and connects via UART interface at pin DIM/UART.

The common UART interface enables communication with the IC even without the interactive GUI tool. This allows easy configuration during mass production.

When VCC exceeds the  $V_{VCCon}$  threshold, ICL8105 will sense pin DIM/UART for a UART connection. If power is provided by VCC and no input voltage is applied at startup, ICL8105 will enter configuration mode. Also, ICL8105 will enter configuration mode if no parameters have been programmed so far, regardless of input voltage being applied or not.



**Figure 16** Setup for configuration of the IC

A graphic user interface guides the user through the configuration of parameters. Further information on the GUI can be found in the GUI User Manual provided by Infineon.

The process of dimensioning of the application (e.g. layout, transformer construction and component selection) is covered in the ICL8105 Design Guide.

An ICL8105 form factor board is available from Infineon to demonstrate the ICL8105 features and performance. The ICL8105 design guide & application note present the reference implementation and the achieved performance.

### 2.4.2 Overview configurable parameters and functions

The ICL8105 provides a generic firmware version that includes all configurable parameters set to zero. The parameter values need to be specified by the user according to the target application. **Table 5** lists the configurable parameters. **Table 6** lists parameters with fixed value which are not configurable.

**Table 5** List of configurable parameters

Description	Parameter	Example	Configuration Range
<b>Hardware configuration</b>			
$I_{out}$ set point (non-dimmed)	$I_{out\_set}$	1600 mA	Calculated by GUI
Primary winding turns	$N_p$	54	> 0
Secondary winding turns	$N_s$	14	> 0
Auxiliary winding turns	$N_a$	23	> 0
Transformer Primary Inductance	$L_p$	0.31 mH	> 0

Functional description

**Table 5 List of configurable parameters (cont'd)**

Description	Parameter	Example	Configuration Range
Current sense resistor	R_CS	0.205 ohm	Calculated by GUI
Primary OCP1 limitation threshold	V_OCP1	1.07 V	Calculated by GUI
ZCD series resistor	R_ZCD_1	76.8 kohm	Calculated by GUI
ZCD shunt resistor	R_ZCD_2	2.20 kohm	Calculated by GUI
Vcc Voltage Supply Type	VCC_SUPPLY	Wide	[External, Narrow, Wide]
Vcc capacitor total capacitance	C_Vcc	14.8 uF	Calculated by GUI
Output capacitor maximum Voltage Rating	V_out_cap_rating	63 V	$\geq V_{outOV}$
HV pin resistor	R_HV	68 kohm	Calculated by GUI
Gate driver peak source current	I_GD_pk	118mA	30 mA to 118 mA
<b>Protections</b>			
Auto restart time	t_auto_restart	1 s	0.1 s to 25.5 s <sup>1)</sup>
Fast auto restart time	t_auto_restart_fast	0.4 s	0.1 s to 25.5 s <sup>1)</sup>
Output OVP / Open Reaction	Reaction_OVP_Vout	Auto restart	[Auto restart, Latch mode]
Auto restart speed for output OVP	Speed_OVP_Vout	Slow	[Slow, Fast]
Output OVP threshold	V_outOV	54 V	Calculated by GUI
Enable output UVP / Short Protection	EN_UVP_Vout	Enabled	[Enabled, Disabled]
Timeout for short detection at startup	t_start_max	15 ms	0 ms to 100 ms <sup>2)</sup>
Output UVP threshold (at steady state)	V_outUV	5 V	0 V to V_out_start
Enable Maximum Average output OCP	EN_lout_max_avg	Enabled	[Enabled, Disabled]
Enable Maximum Peak output OCP	EN_lout_max_peak	Enabled	[Enabled, Disabled]
Maximum peak Output OCP threshold	I_out_max_peak	5000 mA	Calculated by GUI
Auto restart speed for output OCP	Speed_OCP_lout	Slow	[Slow, Fast]
Enable Input OVP	EN_OVP_In	Enabled	[Enabled, Disabled]
Enable Input UVP	EN_UVP_In	Enabled	[Enabled, Disabled]
Input OVP threshold	V_inOV	305 V <sub>rms</sub> <sup>3)</sup>	Calculated by GUI
Maximum startup input voltage	V_in_start_max	277 V <sub>rms</sub> <sup>3)</sup>	V_in_start_min to V_inOV
Minimum startup input voltage	V_in_start_min	72 V <sub>rms</sub> <sup>3)</sup>	V_inUV to V_in_start_max
Input UVP threshold	V_inUV	65 V <sub>rms</sub> <sup>3)</sup>	Calculated by GUI
Stop instead of Latch	EN_STOP	Latch mode	[Stop, Latch mode]
<b>Temperature guard</b>			
Overtemperature detection threshold	T_critical	119 °C	T_start to (T <sub>J(max)</sub> - 6°C)
Enable Adaptive temperature protection	EN_ITP	Enabled	[Enabled, Disabled]
Temperature to start derating of I <sub>out</sub>	T_hot	110 °C	0 °C to T_critical
Minimum I <sub>out</sub> for Adaptive temperature derating	I_out_red	200 mA	0 mA to I_out_set
Time step for each I <sub>out</sub> derating	t_step	10 s	2 s to 20 s

Functional description

**Table 5 List of configurable parameters (cont'd)**

Description	Parameter	Example	Configuration Range
<b>Startup &amp; shutdown</b>			
Soft start timestep	t <sub>ss</sub>	0.5 ms	Calculated by GUI
Minimum V <sub>out</sub> when fully dimmed	V <sub>out_dim_min</sub>	11 V	V <sub>out_start</sub> to V <sub>outOV</sub>
V <sub>out</sub> to start constant current control loop	V <sub>out_start</sub>	8 V	V <sub>outUV</sub> to V <sub>out_dim_min</sub>
Initial mode of operation	control_loop_init	ABM	[ABM, DCM, QRM]
Initial number of ABM pulses at startup	N <sub>ABM_init</sub>	50	Calculated by GUI
<b>Control loop</b>			
QRM PI regulator proportional coefficient	PI_KP_QRM	512	10 to 3000
QRM PI regulator integral coefficient	PI_KI_QRM	8	1 to 1000
DCM PI regulator proportional coefficient	PI_KP_DCM	16384	100 to 30000
DCM PI regulator integral coefficient	PI_KI_DCM	192	10 to 10000
ABM PI regulator proportional coefficient	PI_KP_ABM	64	1 to 600
ABM PI regulator proportional coefficient	PI_KI_ABM	32	1 to 200
<b>Dimming</b>			
Enable Dimming	EN_DIM	Enabled	[Enabled, Disabled]
Minimum I <sub>out</sub> when fully dimmed	I <sub>out_dim_min</sub>	20 mA	Calculated by GUI
Dimming curve shape	C_DIM	Quadratic	[Linear, Quadratic]
Enable dim-to-off	EN_DIM_TO_OFF	Disabled	[Enabled, Disabled]
Enable Square Wave Output for SQW pin	EN_SQW	Enabled	[Enabled, Disabled]
<b>Multimode</b>			
Maximum switching frequency	f <sub>sw_max</sub>	158 kHz	f <sub>sw_min_QRM</sub> to 180.8kHz
Maximum on-time	t <sub>on_max</sub>	11.5 us	Calculated by GUI
Minimum on-time	t <sub>on_min</sub>	1.1us	1 us to t <sub>on_max</sub>
Minimum switching frequency in DCM	f <sub>sw_min_DCM</sub>	20 kHz	3 kHz to 20kHz
Enable Active Burst Mode	EN_ABM	Enabled	[Enabled, Disabled]
DCM switching period modulation gain	N <sub>DCM_mod_gain</sub>	32	[0, 8, 16, 32]
<b>Enhanced PFC</b>			
Enable Enhanced PFC	EN_EPFC	Enabled	[Enabled, Disabled]
Capacitance compensation factor	C <sub>EMI</sub>	0.15 uF	≥ 0
<b>Fine tuning</b>			
Minimum demagnetization time	t <sub>min_demag</sub>	3.0 us	2 us to 10 us
CS Propagation delay compensation	t <sub>PDC</sub>	250 ns	0 ns to 1000 ns
ZCD propagation delay compensation	t <sub>ZCDPD</sub>	395 ns	0 ns to 1000 ns
Transformer coupling	T <sub>coupling</sub>	1.040	0.000 to 2.000
Input voltage drop compensation	R <sub>in</sub>	5 ohm	≥ 0

Functional description

- 1) The auto-restart time has to be chosen sufficiently large enough to avoid a stepping up of the output voltage which would exceed the output overvoltage level.
- 2) VCC capacitance has to be dimensioned large enough to provide power for the maximum startup time
- 3) The input voltage levels refer to AC RMS voltage. If a programmed ICL8105 is operated with both AC or DC, the threshold for DC input voltage is 1.41 times the threshold for AC RMS input voltage.

**Table 6 List of non-configurable parameters**

Description	Parameter	Fixed Value	Notes
<b>Hardware configuration</b>			
Transformer primary leakage inductance	L <sub>p_lk</sub>	L <sub>p</sub> * 1% uH	
Output diode voltage drop	V <sub>out_diode_drop</sub>	0.7 V	
Gate driver high voltage	V <sub>GD</sub>	9 V	
<b>Protections</b>			
Output UVP / Short Reaction	Reaction_UVP_Vout	Auto restart	
Steady state Output UVP blanking time	t <sub>Vout_blank</sub>	1 ms	
Maximum Average output OCP Reaction	Reaction_lout_max_avg	Auto restart	
Maximum Average Output OCP threshold	I <sub>out_max_avg</sub>	I <sub>out_set</sub> * 150% mA	
Maximum Peak output OCP Reaction	Reaction_lout_max_peak	Auto restart	
Input OVP Reaction	Reaction_OVP_Vin	Latch mode	
Input UVP Reaction	Reaction_UVP_Vin	Auto restart	
Input OCP2 / Short Winding Reaction	Reaction_OCP2	Latch mode	
Vcc OVP Reaction	Reaction_VCCP	Latch mode	
Vcc OVP Threshold	V <sub>VCC_max</sub>	24 V	
Hardware reaction for Firmware Protection (Watchdog, RAM parity)	Reaction_HW	Auto restart	
<b>Temperature guard</b>			
Overtemperature Reaction	Reaction_TP	Latch mode	
Maximum startup temperature	T <sub>start</sub>	T <sub>hot</sub> or T <sub>critical</sub>	T <sub>hot</sub> if EN_ITP = enabled T <sub>critical</sub> if EN_ITP = disabled
I <sub>out</sub> reduction in each derating step	I <sub>out_step</sub>	I <sub>out_set</sub> /80	
<b>Startup &amp; shutdown</b>			
Number of soft start steps	n <sub>ss</sub>	3	
<b>Dimming</b>			
DIM/UART pin voltage for maximum I <sub>out</sub>	V <sub>DIM_max</sub>	1.72 V	
DIM/UART pin voltage for minimum I <sub>out</sub>	V <sub>DIM_min</sub>	0.45 V	
DIM/UART pin voltage for dim-to-off	V <sub>DIM_off</sub>	0.4 V	
Square-wave frequency for SQW pin	f <sub>SQW</sub>	160 kHz	

Functional description

**Table 6** List of non-configurable parameters (cont'd)

Description	Parameter	Fixed Value	Notes
Square-wave voltage for SQW pin	V_SQW	7.5 V	
<b>Multimode</b>			
Minimum switching frequency in QRM	f_sw_min_QRM	20 kHz	
Enable DCM	EN_DCM	Enabled	
<b>Fine tuning</b>			
Spike blanking time for OCP2 trigger	t_CSOP2	240 ns	
Leading edge blanking time	t_CSLEB	480 ns	
ZCD ringing suppression time	t_ZCDring	1200 ns	
Blanking time for CCM protection	t_CCM	10 ms	
Temperature compensation for V_DIM	a_DIM	-0.729 mV/K	
Number of digital filter stages for V_DIM	N_DIM_Filter	6	

Electrical Characteristics

### 3 Electrical Characteristics

All signals are measured with respect to ground (pin 8). The voltage levels are valid if other ratings are not violated.

#### 3.1 Package Characteristics

**Table 7** Package Characteristics

Parameter	Symbol	Limit Values		Unit	Remarks
		min	max		
Thermal resistance from junction to ambient	$R_{thJA}$	—	178	K/W	PG-DSO-8 <sup>1)</sup>

1) JEDEC 1s0p at  $P_v = 140$  mW

#### 3.2 Absolute Maximum Ratings

Absolute maximum ratings ([Table 8](#)) are defined as ratings which when being exceeded may lead to destruction of the integrated circuit. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. These values are not tested during production test.

**Table 8** Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min	max		
Voltage externally supplied at pin VCC	$V_{CC}$	-0.5	26	V	
Voltage at pin GD	$V_{GD}$	-0.5	$V_{CC} + 0.3$	V	
Voltage at pin SQW	$V_{SQW}$	-0.5	$V_{CC} + 0.3$	V	
Ambient temperature	$T_A$	-40	85	°C	
Junction temperature	$T_J$	-40	125	°C	
Storage temperature	$T_S$	-55	150	°C	
Soldering temperature	$T_{Sold}$	—	260	°C	Wave soldering <sup>1)</sup>
ESD capability HBM	$V_{HBM}$	—	2000	V	Excluding pin HV <sup>2)</sup>
ESD capability HBM	$V_{HBM}$	—	1500	V	Pin HV <sup>2)</sup>
Voltage at pin ZCD	$V_{ZCD}$	-0.5	3.6	V	
Voltage at pin CS	$V_{CS}$	-0.5	3.6	V	
Voltage at pin DIM/UART	$V_{DIM/UART}$	-0.5	3.6	V	
Maximum transient input clamping for pins ZCD and CS	$-I_{CLN\_TR}$	—	10	mA	<sup>3)</sup>
Maximum permanent input clamping current for pins ZCD and CS	$-I_{CLN\_DC}$	—	5	mA	Permanently applied as DC value

Electrical Characteristics

**Table 8 Absolute Maximum Ratings (cont'd)**

Parameter	Symbol	Limit Values		Unit	Remarks
		min	max		
Maximum negative transient input voltage at pin ZCD	$-V_{IN\_ZCD}$	—	1.5	V	<sup>3)</sup>
Maximum negative transient input voltage at pin CS	$-V_{IN\_CS}$	—	3.0	V	<sup>3)</sup>
Maximum current into pin HV	$I_{HV}$	—	10	mA	
Voltage at pin HV	$V_{HV}$	—	600	V	

1) According to JESD22A111 Rev A

2) ESD-HBM according to ANSI/ESDA/JEDEC JS-001-2012.

3) Only valid during transitions, allowed for maximum 2  $\mu$ s and with a duty cycle of maximum 10%. Values for DC operation, see absolute maximum table.

### 3.3 Operating Conditions

**Table 9** shows the recommended operating range where the electrical characteristics shown in [Chapter 3.4](#) are valid for.

**Table 9 Operating Range**

Parameter	Symbol	Limit Values		Unit	Remarks
		min	max		
Lower VCC limit	$V_{CC}$	$V_{UVOFF}$	—	V	Device is held in reset when $V_{CC} < V_{UVOFF}$
Voltage externally supplied to VCC pin	$V_{CCext}$	—	24	V	Maximum voltage that can be applied to pin VCC by an external voltage source
Voltage at pin GD	$V_{GD}$	-0.3	$V_{CC} + 0.3$	V	
Voltage at pin SQW	$V_{SQW}$	-0.3	$V_{CC} + 0.3$	V	

Electrical Characteristics

3.4 DC Electrical Characteristics

The electrical characteristics involve the spread of values given within the specified supply voltage and junction temperature range,  $T_j$  from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$ . Typical values represent the median values related to  $T_A = 25\text{ }^{\circ}\text{C}$ . All voltages refer to GND, and the assumed supply voltage is  $V_{CC} = 18\text{ V}$ , if not specified otherwise.

The following characteristics are specified

- Power supply (Table 10)
- Clock Oscillators (Table 11)
- Internal temperature sensor (Table 12)
- Pin ZCD (Table 13)
- Pin DIM/UART (Table 14)
- Pin CS (Table 15)
- Pin GD (Table 16)
- Pin HV (Table 17)
- Pin SQW (Table 18)

Table 10 Electrical Characteristics of the Power Supply

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
VCC turn-on threshold	$V_{VCCon}$	19	20.5	22	V	$dV_{CC}/dt = 0.2\text{ V/ms}$
VCC turn-off threshold	$V_{UVOFF}$	-5%	6	+5%	V	
VCC UVOFF current	$I_{VCCUVOFF}$	5	20	40	$\mu\text{A}$	$V_{CC} < V_{VCCon}(\text{min}) - 0.3\text{ V}$
VCC threshold for turning on HV startup cell in auto restart and latch mode	$V_{UVLO}$	-5%	7.5	+5%	V	
VCC threshold for turning off HV startup cell in auto restart	$V_{OVLO}$	—	20.5	—	V	
VCC average quiescent current in latched mode	$I_{VCCqu,latch}$	—	0.3	0.48	mA	$T_j \leq 85\text{ }^{\circ}\text{C}$ , Latch mode
		—	—	1.2	mA	$T_j \leq 125\text{ }^{\circ}\text{C}$ , Latch mode
VCC average quiescent current in auto restart mode	$I_{VCCqu,restart}$	—	0.3	0.48	mA	$T_j \leq 85\text{ }^{\circ}\text{C}$ , Off phase in auto restart mode
		—	—	1.2	mA	$T_j \leq 125\text{ }^{\circ}\text{C}$ , Off phase in auto restart mode
VCC voltage for OTP programming	$V_{PP}$	7.35	7.5	7.65	V	Operational values, not tested in production test

Electrical Characteristics

**Table 11 Electrical Characteristics of the Clock Oscillators**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Main clock oscillator period	$t_{MCLK}$	15.0	15.8	16.6	ns	
DCM Minimum switching frequency	$f_{sw\_min\_DCM}$	-5.1%	20 <sup>1)</sup>	+5.3%	kHz	
Maximum switching frequency	$f_{sw\_max}$	-5.1%	1)	+5.3%	kHz	

1) See configuration chapter

**Table 12 Electrical Characteristics of the Internal Temperature Sensor**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Internal Temperature sensing	$T_{critical},$ $T_{start},$ $T_{hot}$	-6	1)	+6	°C	3 sigma deviation by lab characterization, not tested in production

1) See configuration chapter

**Table 13 Electrical Characteristics of pin ZCD**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
ZCD clamping of negative voltages	$-V_{INPCLN}$	150	180	220	mV	analog clamp activated
ZCD threshold	$V_{ZCDdet}$	5	20	35	mV	
ZCD clamping current	$-I_{IV}$	0.021	—	3.14	mA	
ZCD voltage sensing	$V_{ZCDSH}$	0.067	—	2.61	V	
ZCD S&H delay of input buffer referring to positive jump of ZCD voltage	$t_{ZSHST}$	—	—	2.0	μs	not tested in production

**Table 14 Electrical Characteristics of pin DIM/UART**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Dimming mode voltage	$V_{DIM}$	0.1	—	2.0	V	

Electrical Characteristics

Table 14 Electrical Characteristics of pin DIM/UART (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
UART mode output low voltage	$V_{\text{UARTLow}}$	—	—	0.8	V	$I_{\text{OL}} = 2 \text{ mA}$
UART mode output high voltage	$V_{\text{UARTHigh}}$	2.2	—	—	V	$I_{\text{OH}} = -2 \text{ mA}$

Table 15 Electrical Characteristics of pin CS

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
CS voltage threshold for 1st level overcurrent protection	$V_{\text{OCP1}}$	-5%	<sup>1)</sup>	+5%	V	
CS voltage threshold for 2nd level overcurrent protection	$V_{\text{OCP2}}$	-5%	1.6	+5%	V	$0.806\text{V} < V_{\text{OCP1}} \leq 1.2\text{V}$
		-5%	1.2	+5%	V	$0.605\text{V} < V_{\text{OCP1}} \leq 0.806\text{V}$
		-5%	0.8	+5%	V	$0.403\text{V} < V_{\text{OCP1}} \leq 0.605\text{V}$

1) see configuration chapter

Table 16 Electrical Characteristics of pin GD

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Output voltage at low state	$V_{\text{GDlow}}$	—	—	1.6	V	$I_{\text{GD}} = 5 \text{ mA}^1$
Output voltage at high state	$V_{\text{GD}}$	—	9	—	V	
Tolerance of output voltage at high state	$\Delta V_{\text{GD}}$	-0.5V	—	+0.5V		
Output high current	$I_{\text{GD\_pk}}$	-20%	<sup>2)</sup>	+20%	mA	$C_{\text{LOAD}} = 2 \text{ nF}$
Discharge current	$I_{\text{GDDIS}}$	500	—	—	mA	$V_{\text{GD}} = 4\text{V}$ and driver at low state

1) Not tested in production test

2) See configuration chapter

Table 17 Electrical Characteristics of pin HV

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Leakage current at pin HV	$I_{\text{HVleak}}$	—	—	10	$\mu\text{A}$	$V_{\text{HV}} = 600 \text{ V}$ , HV startup cell disabled
Current for VCC cap charging	$I_{\text{LD}}$	3.2	5	7.5	mA	$V_{\text{HV}} = 30 \text{ V}$ ; $V_{\text{VCC}} < V_{\text{VCCcon}} - 0.3 \text{ V}$
Current into pin HV	$I_{\text{HV,max}}$	—	—	9.6	mA	

Electrical Characteristics

Table 18 Electrical Characteristics of pin SQW

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Squarewave frequency	f <sub>SQW</sub>	-5.1%	160	+5.3%	kHz	
Output voltage at low state	V <sub>SQWlow</sub>	—	—	1.6	V	I <sub>SQW</sub> = 5 mA <sup>1)</sup>
Output voltage at high state	V <sub>SQW</sub>	—V	7.5	—	V	
Tolerance of output voltage at high state	Δ V <sub>SQW</sub>	-0.5V	—	+0.5V		
Output high current	-I <sub>SQWH</sub>	-20%	30	+20%	mA	C <sub>LOAD</sub> = 2 nF
Discharge current	I <sub>SQWDIS</sub>	500	—	—	mA	V <sub>SQW</sub> = 4V and pin at low state

1) Not tested in production test.

Outline dimensions

## 4 Outline dimensions

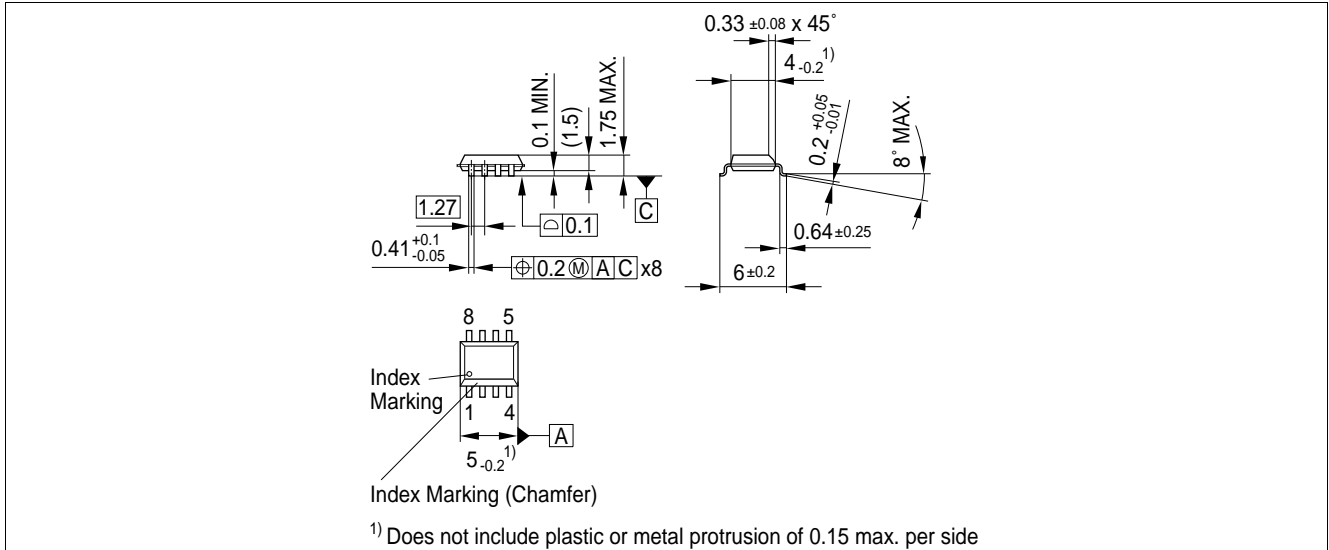


Figure 17 PG-DSO-8

### Notes

1. You can find all of our packages, sorts of packing and others in our Infineon Internet Page "Products":  
<http://www.infineon.com/products>.
2. Dimensions in mm

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