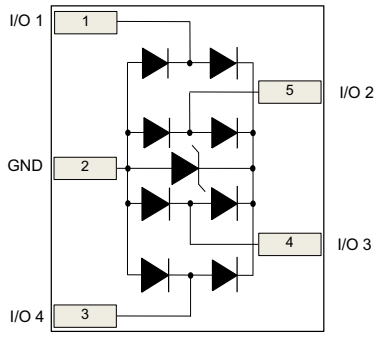
HSP051-4M5

4-line ESD protection for high speed lines

Datasheet – production data

µQFN-5L package
1.3 mm x 0.8 mm

Figure 1. Functional schematic (top view)



Features

- Very compact 500 µm pitch package for easy PCB layout.
- Ultra large bandwidth: 12 GHz
- Ultra low capacitance:
  - 0.2 pF (I/O to I/O)
  - 0.35 pF (I/O to GND)
- Very low dynamic resistance: 0.45 Ω
- Low leakage current: 100 nA at 25 °C
- Extended operating junction temperature range: -40 °C to 150 °C
- Thin package: 0.4 mm max.
- RoHS compliant

Benefits

- High ESD protection level
- High integration
- Suitable for high density boards

Complies with following standards

- MIL-STD 883G Method 3015-7 Class 3B:
  - 8 kV
- Exceeds IEC 61000-4-2 level 4:
  - 15 kV (contact discharge)
  - 30 kV (air discharge)

Applications

The HSP051-4M5 is designed to protect against electrostatic discharge on sub micron technology circuits driving:

- HDMI 1.4 and 2.0
- Digital video Interface
- Display port
- USB 3.1 Gen 1 and Gen 2
- Serial ATA

The ultra-low variation of the capacitance ensures very low influence on signal-skew. The large bandwidth makes it compatible with HDMI 2.0 4K/2K (= 5.94 Gbps) and USB 3.1 Gen 2 (= 10 Gbps).

Description

The device is a 4-channel ESD array with a rail to rail architecture designed specifically for the protection of high speed differential lines.

Packaged in µQFN 1.3 mm x 0.8 mm with a 500µm pitch.

1 Characteristics

Table 1. Absolute maximum ratings T_{amb} = 25 °C

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse voltage	IEC 61000-4-2 contact discharge IEC 61000-4-2 air discharge	15 30	kV
T_j	Operating junction temperature range		-40 to +150	°C
T_{stg}	Storage temperature range		-65 to +150	°C
T_L	Maximum lead temperature for soldering during 10 s		260	°C

Table 2. Electrical characteristics T_{amb} = 25 °C

Symbol	Test conditions		Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA		4.5	5.8		V
I_{RM}	V_{RM} = 3.6 V			10	100	nA
V_{CL}	I_{PP} = 1.5 A, 8/20 µs				10	V
V_{CL}	IEC 61000-4-2, +8 kV contact measured at 30 ns			13		V
Rd	Dynamic resistance, pulse duration 100 ns	I/O to GND		0.55		Ω
		GND to I/O		0.75		
$C_{I/O - I/O}$	$V_{I/O}$ = 0 V, F = 2.5 GHz to 9 GHz, V_{OSC} = 30 mV			0.2	0.3	pF
$C_{I/O - GND}$	$V_{I/O}$ = 0 V	F = 200 MHz to 2.5 GHz		0.4	0.55	pF
		F = 2.5 GHz to 9 GHz		0.35	0.45	pF
f_C	-3dB			12		GHz

Figure 2. Leakage current versus junction temperature (typical values)

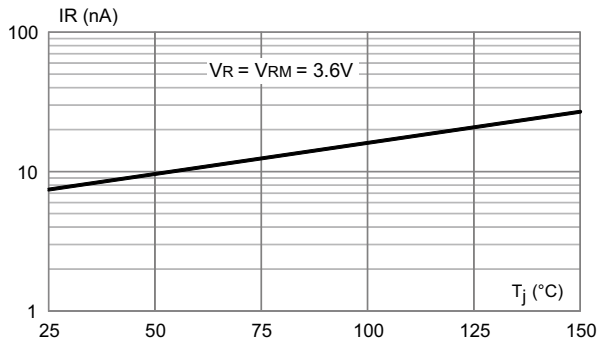


Figure 3. S21 attenuation measurement

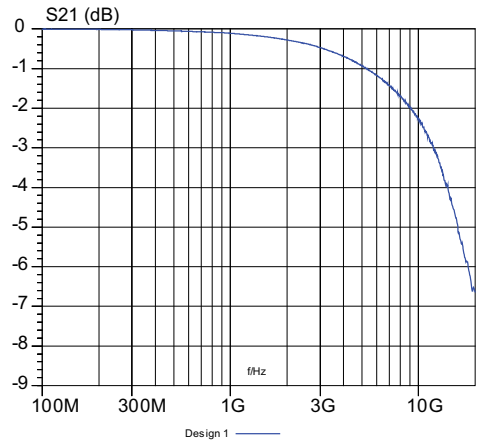


Figure 4. Eye diagram - HDMI 1.4 mask at 3.35 Gbps per channel (without HSP051-4M5)

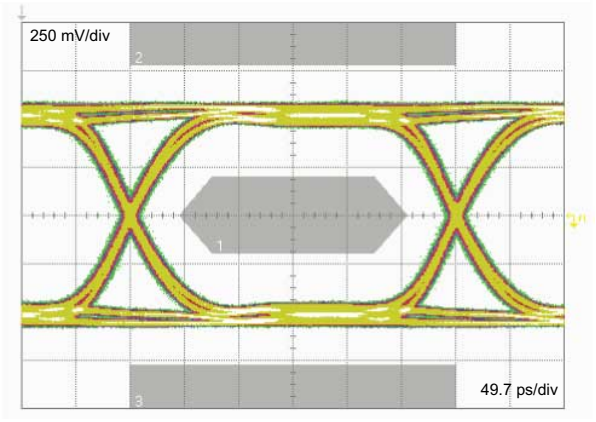


Figure 5. Eye diagram - HDMI mask at 3.35 Gbps per channel (with HSP051-4M5)

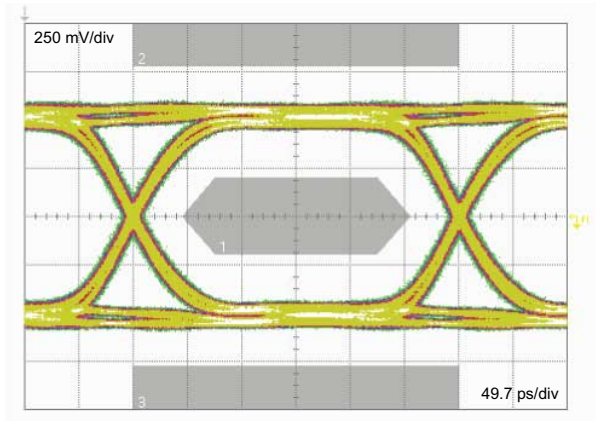


Figure 6. Eye diagram - HDMI 2.0 mask at 5.94 Gbps per channel without HSP051-4M5 (without cable and EQ)

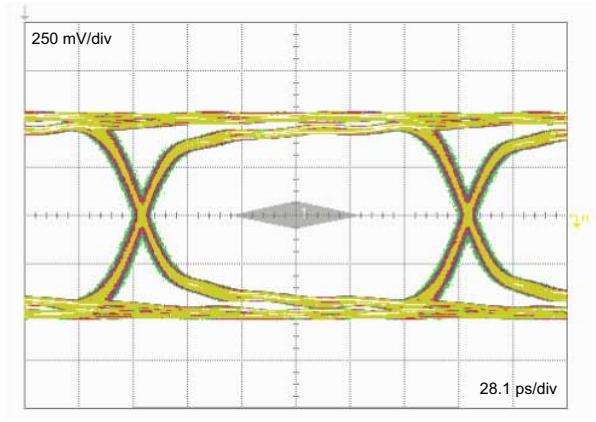


Figure 7. Eye diagram - HDMI 2.0 mask at 5.94 Gbps per channel with HSP051-4M5 (without cable and EQ)

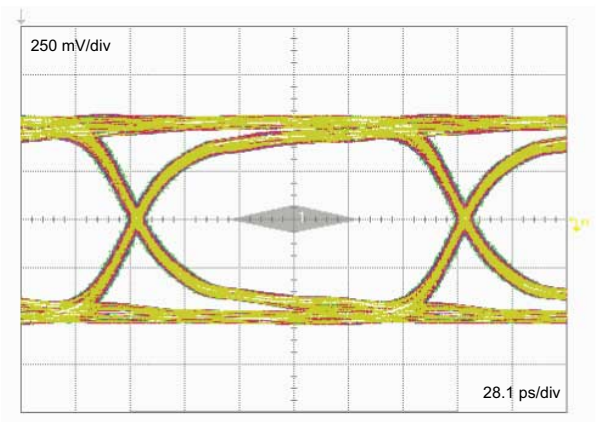


Figure 8. Eye diagram - USB 3.1 Gen mask at 5.0 Gbps per channel without HSP051-4M5 (without cable and EQ)

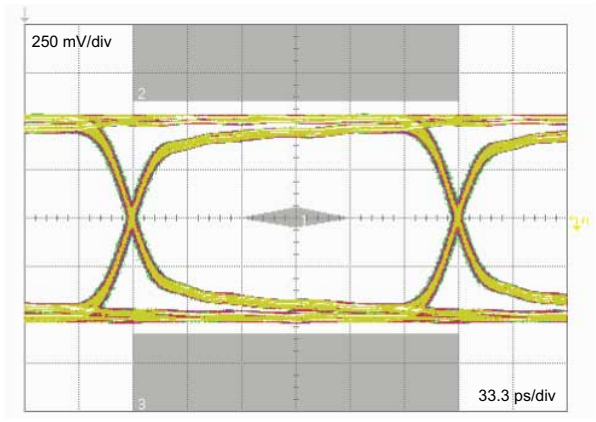


Figure 9. Eye diagram - USB 3.1 mask at 5.0 Gbps per channel with HSP051-4M5(without cable and EQ)

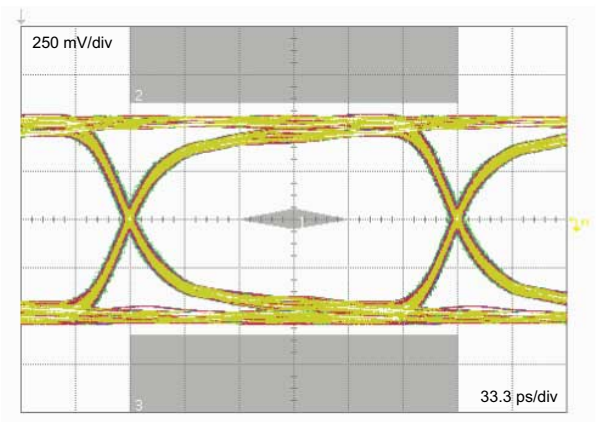


Figure 10. Eye diagram - USB 3.1 Gen 2 mask at 10.0 Gbps per channel without HSP051-4M5 (without cable and EQ)

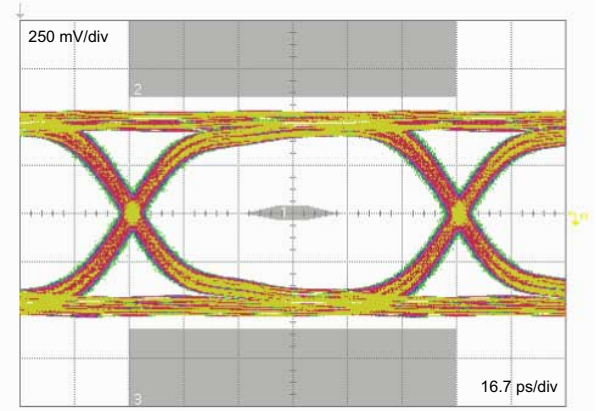


Figure 11. Eye diagram - USB 3.1 Gen 2 mask at 10.0 Gbps per channel with HSP051-4M5 (without cable and EQ)

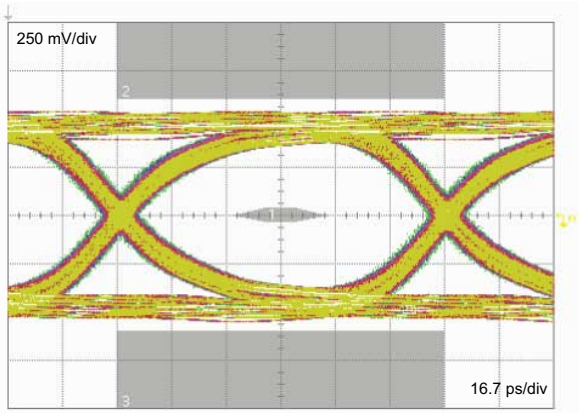
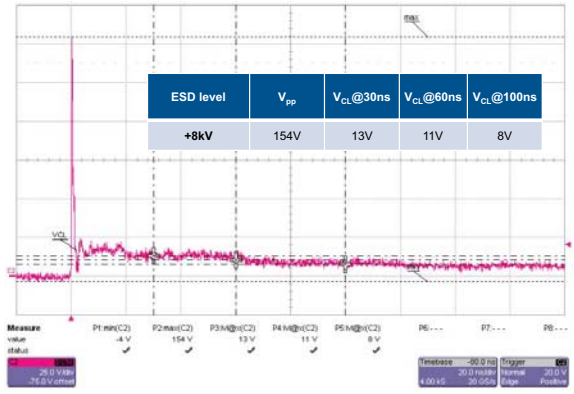
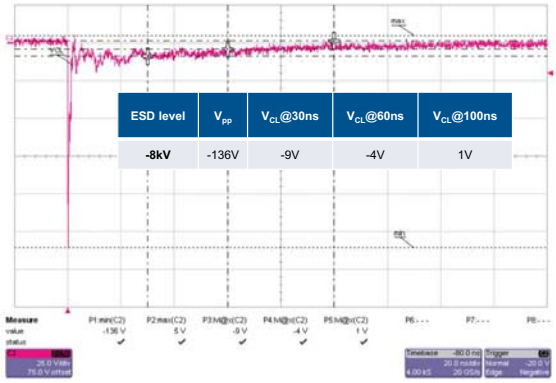


Figure 12. ESD response to IEC 61000-4-2 (+8 kV contact discharge)



ESD level	V_{PP}	V_{CL}@30ns	V_{CL}@60ns	V_{CL}@100ns
+8kV	154V	13V	11V	8V

Figure 13. ESD response to IEC 61000-4-2 (-8 kV contact discharge)



ESD level	V_{PP}	V_{CL}@30ns	V_{CL}@60ns	V_{CL}@100ns
-8kV	-136V	-9V	-4V	1V

Figure 14. TLP characteristic

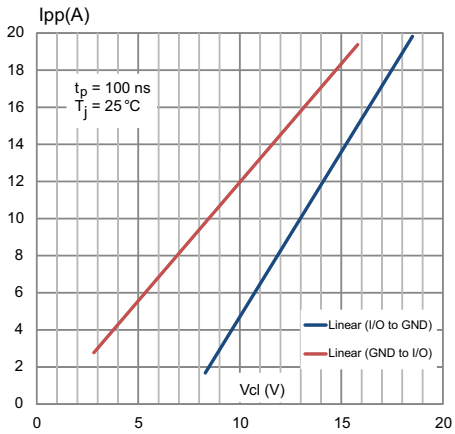
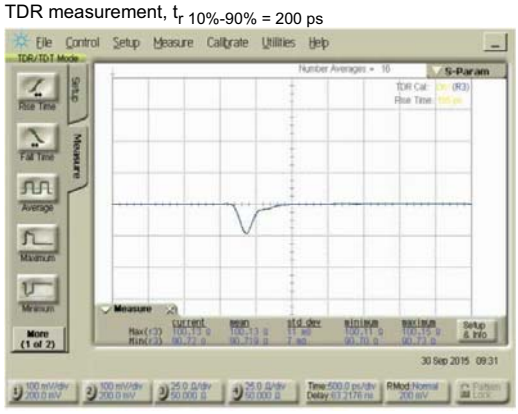


Figure 15. TDR measurement



2 Package information

- Epoxy meets UL94, V0
- Lead-free packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com.* ECOPACK® is an ST trademark.

2.1 µQFN 5L package information

Figure 16. µQFN 5L package outline

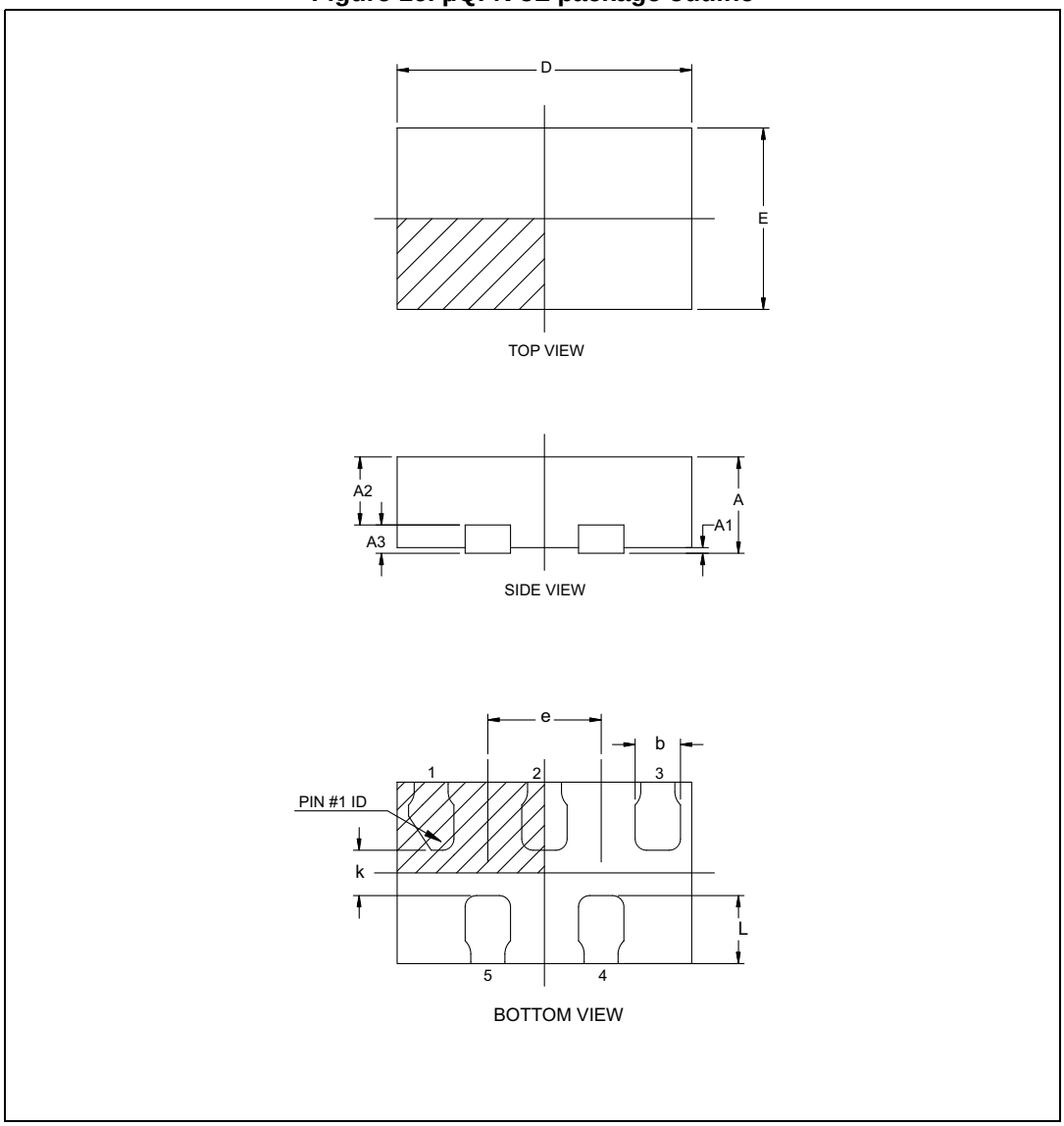


Table 3. µQFN 5L mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A	0.36	0.38	0.40
A1	0.00		0.05
A2	0.15	0.25	0.35
A3		0.125	
b	0.16	0.20	0.24
D	1.20	1.30	1.40
e		0.50	
E	0.70	0.80	0.90
L	0.20	0.30	0.40
k		0.20	

Figure 17. Footprint recommendations (dimensions in mm)

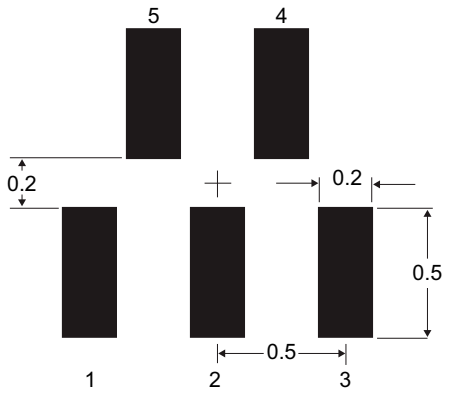


Figure 18. Marking

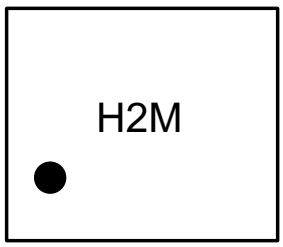
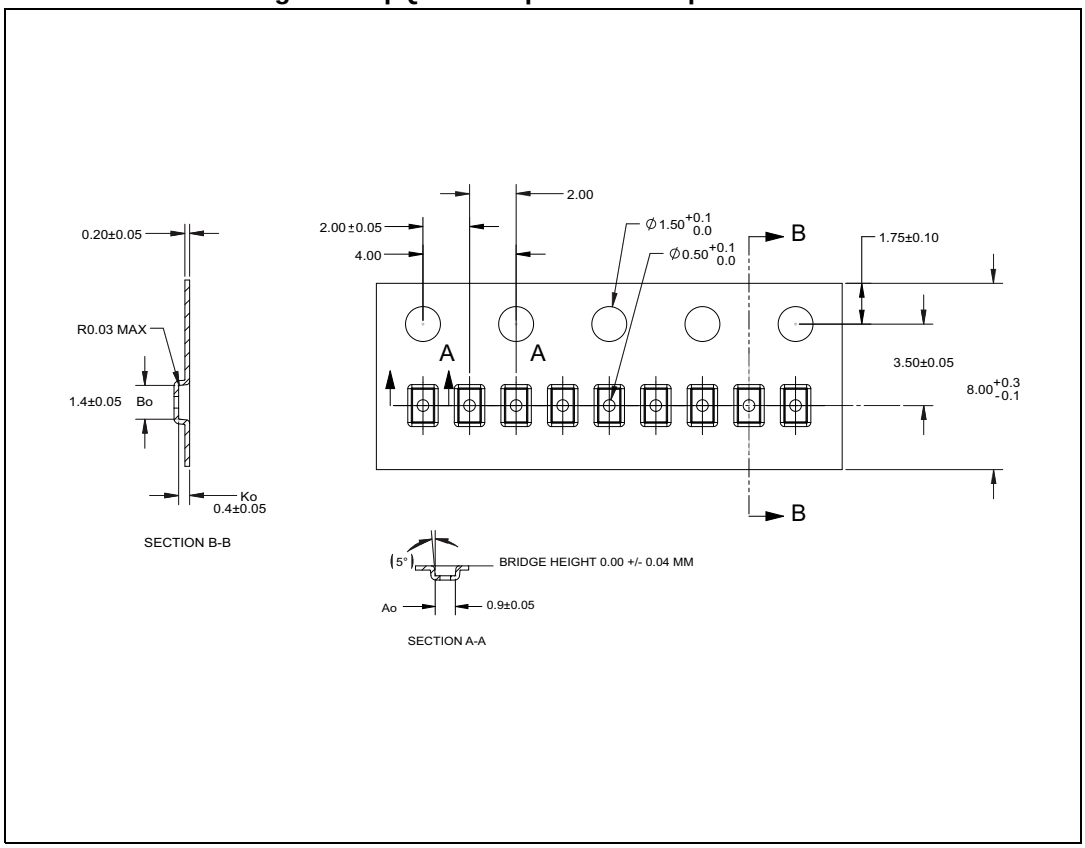


Figure 19. µQFN 5L tape and reel specification



3 Recommendation on PCB assembly

3.1 Solder paste

1. Use halide-free flux, qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste recommended.
3. Offers a high tack force to resist component displacement during high speed.
4. Use solder paste with fine particles: powder particle size 20-45 µm.

3.2 Placement

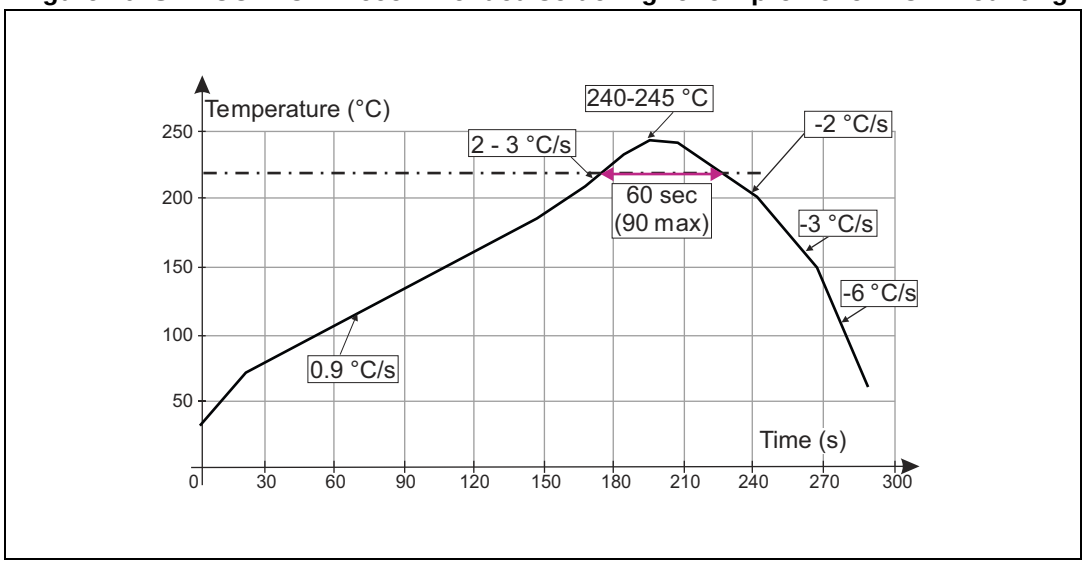
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.3 PCB design

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

3.4 Reflow profile

Figure 20. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

3.4.1 General advice about reflow conditions:

For each individual board, the appropriate heat profile has to be adjusted experimentally. The proposed profiles are just starting points. In every case, the following precautions have to be considered:

- Always preheat the device. The purpose of this step is to minimize the rate of temperature rise to less than 2 °C per second in order to minimize thermal shock on the component.

- Dry out sections ensure that the solder paste is fully dried before starting reflow step. Also, this step allows the temperature gradient on the board to be evened out.

- Peak temperature should be at least 30 °C higher than the melting point of the chosen solder alloy to ensure the reflow quality. In any case the peak temperature should not exceed 260 °C.

4 Ordering information

Figure 21. Ordering information scheme

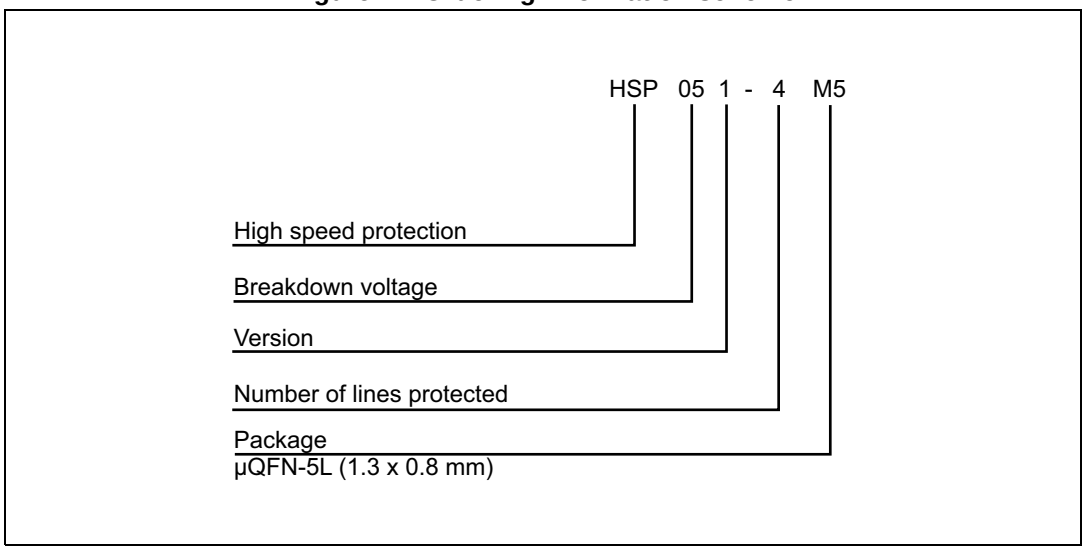


Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
HSP051-4M5	H2M	µQFN-5L	4.24 mg	10000	Tape and reel

5 Revision history

Table 5. Document revision history

Date	Revision	Changes
04-Feb-2016	1	Initial release.