HMC7911LP5E

v00.0815

GaAs MMIC I/Q UPCONVERTER 17.5 - 19.7 GHz

Typical Applications

The HMC7911LP5E is ideal for:

- Point-to-Point and Point-to-Multi-Point Radios
- Military Radar, EW & ELINT
- Satellite Communications
- Sensors

Features

Conversion Gain: 14 dB

Sideband Rejection: 25 dBc

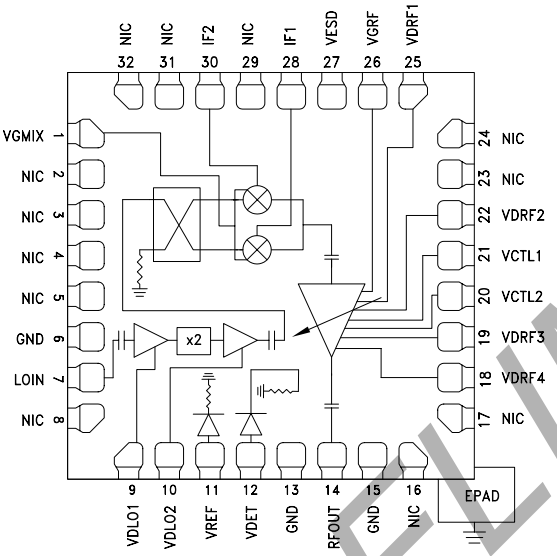
Dynamic Range: 30 dB

Output Third-Order Intercept (OIP3): 32 dBm

x2 LO to RF Leakage: -35 dBm

32 Lead 5 x 5 mm SMT Package

Functional Diagram



General Description

The HMC7911LP5E is a compact GaAs MMIC I/Q upconverter in a RoHS compliant Low Stress Injection Molded Plastic SMT package. This device provides a small signal conversion gain of 14 dB with 25 dBc of sideband rejection. The HMC7911LP5E utilizes a RF amplifier preceded by an I/Q mixer where the LO is driven by a driver amplifier. IF1 and IF2 mixer inputs are provided and an external 90° hybrid is needed to select the required sideband. The I/Q mixer topology reduces the need for filtering of the unwanted sideband. The HMC7911LP5E is a much smaller alternative to hybrid style single sideband upconverter assemblies and it eliminates the need for wire bonding by allowing the use of surface mount manufacturing techniques.

Electrical Specifications, T_A = +25°C, IF = 1000 MHz, LO = 4 dBm, VGMIX= -1.4 V, VDRF = 5 V, VDLO = 3.3 V, VCTL = -6 V, VESD = -5 V, LSB [1]

Parameter	Min.	Typ.	Max.	Units
RF Frequency Range	17.5		19.7	GHz
LO Frequency Range	7.1		11.6	GHz
IF Frequency Range	DC		3.5	GHz
LO Power	0		6	dBm
Conversion Gain	11	14		dB
Dynamic Range		30		dB
Sideband Rejection	15	25		dBc
Noise Figure at Maximum Gain		10		dB
Noise Figure at 20 dB Attenuation		22		dB
Output Third-Order Intercept (OIP3) at Max Gain	28	31		dBm
x2 LO to RF Leakage			-20	dBm
Total Supply Current (IDLO1 + IDLO2)		110		mA
Total Supply Current (IDRF1 + IDRF2 + IDRF3 + IDRF4)		225		mA

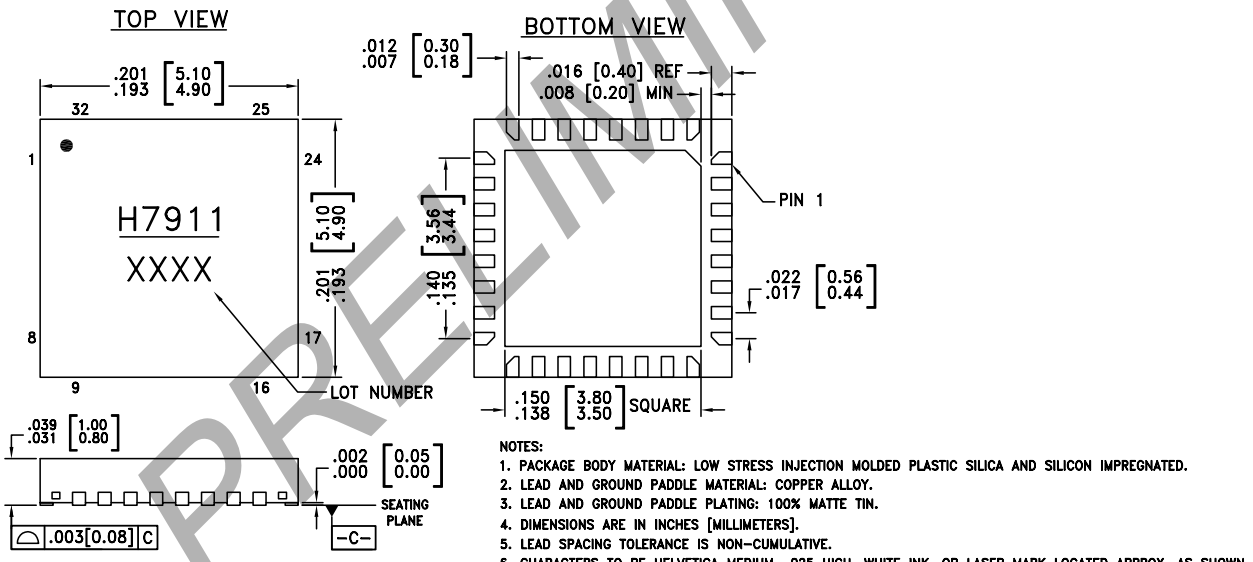
[1] Unless otherwise noted all measurements performed with upper sideband selected and external 90° hybrid at the IF ports.
[2] Adjust VGRF between -2 V and 0 V to achieve total RF drain current = 225 mA.

Absolute Maximum Ratings

Drain Bias Voltage (VDRF)	5.5 V
Drain Bias Voltage (VDLO)	5.5 V
Gate Bias Voltage (VGRF)	-3 V to 0 V
Gain Control Voltage (VCTL)	TBD
Maximum Junction Temperature (to maintain 1 Million hours MTTF)	175 °C
Continuous Pdiss @ Maximum Junction Temperature = 175 °C (T = 85 °C) (derate= 125 mW/ °C above 85 °C)	1.7 W
Thermal Resistance (R_{TH}) (channel to die bottom)	47 °C/W
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to 125°C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



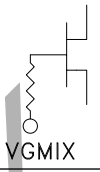
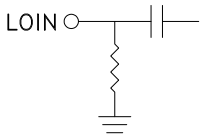
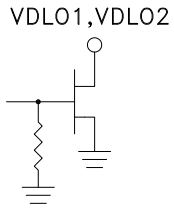
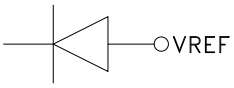
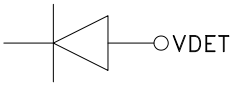
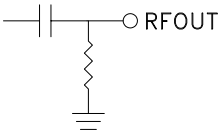
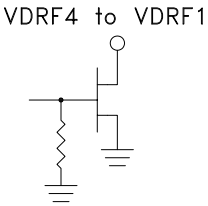
NOTES:
1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
3. LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN.
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
6. CHARACTERS TO BE HELVETICA MEDIUM, .025 HIGH, WHITE INK, OR LASER MARK LOCATED APPROX. AS SHOWN.
7. PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.25mm MAX.
8. PACKAGE WARP SHALL NOT EXCEED 0.05mm
9. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
10. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

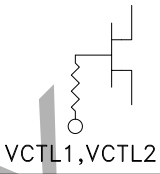
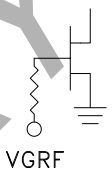
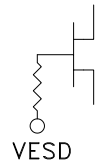
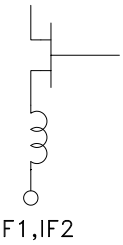
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [2]
HMC7911LP5E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL3 [1]	H7911 XXXX

[1] Max peak reflow temperature of 260 °C
[2] 4-Digit lot number XXXX

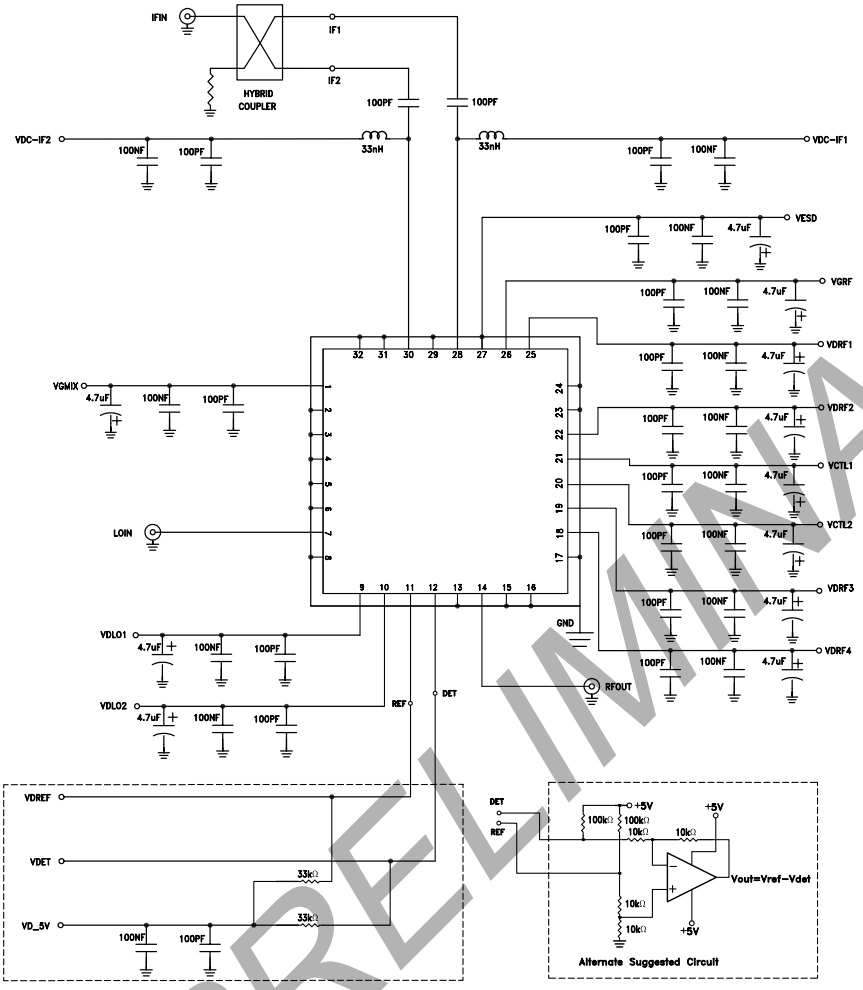
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1	VGMIX	Gate voltage for FET mixer. External bypass capacitors of 100 pF, 0.1 µF and 4.7 µF are recommended.	
2, 3, 4, 5, 8, 16, 17, 23, 24, 29, 31, 32	NIC	No Internal Connection. The pins are not connected internally. However, all data shown herein was measured with these pins connected to RF/DC ground externally.	
6, 13, 15	GND	Ground Connect. These pins and package bottom must be connected to RF/DC ground.	
7	LOIN	Local Oscillator Input. This pin is dc coupled and matched to 50 Ohms.	
9	VDLO1	First and second power supply voltage for the LO amplifier. External bypass capacitors of 100 pF, 0.1µF and 4.7 µF are recommended.	
10	VDLO2		
11	VREF	Reference Voltage for the detector. Dc bias of diode biased through external resistor used for temperature compensation of VDET. See application circuit for required external components.	
12	VDET	Detector Voltage for the detector. Dc voltage representing RF output power rectified by diode which is biased through an external resistor. See application circuit for required external components.	
14	RFOUT	Radio Frequency Output. This pin is dc coupled and matched to 50 Ohms.	
18	VDRF4	Power supply voltage for the RF amplifier. External bypass capacitors of 100 pF, 0.1µF and 4.7 µF are recommended.	
19	VDRF3		
22	VDRF2		
25	VDRF1		

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
20	VCTL2	Gain control voltage for the RF amplifier. External bypass capacitors of 100 pF, 0.1µF and 4.7 µF are recommended.	
21	VCTL1		
26	VGRF	Gate Bias Voltage for the RF amplifier. External bypass capacitors of 100 pF, 0.1µF and 4.7 µF are recommended.	
27	VESD	Dc voltage for ESD protection. External bypass capacitors of 100 pF, 0.01µF and 4.7 µF are recommended.	
28	IF1	First and Second Quadrature Intermediate Frequency input pins. For applications not requiring operation to dc, an off chip dc blocking capacitor should be used. For operation to dc this pin must not source/sink more than 3 mA of current or part non function and possible part failure will result.	
30	IF2		
	EPAD	Exposed Pad. Connect the exposed pad to a low impedance thermal and electrical ground plane.	

Typical Application Circuit



A typical single-sideband upconversion circuit is shown in the application circuit above. For single-sideband upconversion, an external 90° hybrid splits the IF signal into I and Q inputs. The LO to RF leakage can be improved by applying a small dc offsets to the I/Q mixer cores via the IF-VI and IF-VQ inputs. However, it is important to limit the applied dc bias to avoid sourcing or sinking more than ±3 mA of bias current. Depending on the bias sources used, it may be prudent to add series resistance to ensure the applied bias current does not exceed ±3 mA.

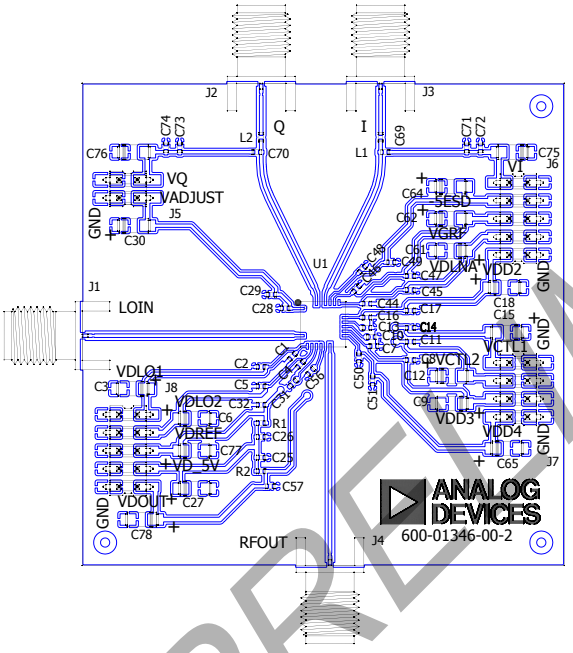
The HMC7911LP5E uses amplifiers in the LO and RF paths. These active stages use depletion mode pseudomorphic high electron mobility transistors (pHEMTs).

To ensure transistor damage does not occur, use the following power-up bias sequence:

1. Apply a –5 V bias to pin 27 (VESD).
2. Apply a –2.0 V bias to pin 26 (VGRF) (Pinched off State).
3. Apply a –1.4 V bias to pin 1 (VGMIX).
4. Apply 2.4 V to 3.6 V to pin 9 (VDLO1) and pin 10 (VDLO2).
5. Apply -6 V to pin 20 and pin 21 (VCTL2, VCTL1). Adjust from -6 V to 0 V depending on amount of attenuation required.
6. Apply 5 V to pin 18, pin 19, pin 22, pin 25 (VDRF4 to VDRF1)
7. Adjust VGRF between –2 V and 0 V to achieve total amplifier drain current of 225 mA.

8. Adjust VDC-IF1 between -0.2 V to 0.2 V and monitor the LO leakage on the RF port. Once desired or maximum level of suppression is achieved, move to step 9.
9. Adjust VDC-IF2 between -0.2 V to 0.2 V and monitor the LO leakage on the RF port until either desired or maximum level of suppression is achieved.
10. If desired level of the LO signal on the RF port has still not been achieved, further tune each VDC-IF1, VDC-IF2 independently in order to achieve desired LO leakage. The resolution of the voltage changed on the voltage of the VDC-IF pins should be in the mV range.

Evaluation PCB



The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

List of Materials for Evaluation PCB [1]

Item	Description
J1 - J4	K CONNECTOR, SRI
J5	CONNECTOR HEADER 4 POS SMT
J7	CONNECTOR HEADER 8 POS SMT
J6, J8	CONNECTOR HEADER 10 POS SMT
C1, C4, C7, C10, C13, C16, C25, C28, C31, C44, C46, C48, C50, C56, C69-C71, C73	100 PF CAPACITOR, 5% 50V COG, 0402
C2, C5, C8, C11, C14, C17, C26, C29, C32, C45, C47, C49, C51, C57, C72, C74	0.1 µF CAPACITOR, 25V 10% X5R, 0402.
C3, C6, C9, C12, C15, C18, C27, C30, C61-C62, C64-C65, C75-C78	4.7 µF CAPACITOR, 16V 20% SMD 3216
L1-L2	INDUCTOR, 33nH, 0402, 5%, 200nA
R1-R2	RESISTOR 33K OHM 1/10W 5% 0402 SMD
U1	HMC7911LP5E Upconverter
PCB [2]	600-01346-00 Evaluation Board

[1] EV1HMC7911LP5, reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR, FR4 or Rogers 4350