

HD44780U (LCD-II)

(Dot Matrix Liquid Crystal Display Controller/Driver)

Description

The HD44780U dot-matrix liquid crystal display controller and driver LSI displays alphanumerics, Japanese kana characters, and symbols. It can be configured to drive a dot-matrix liquid crystal display under the control of a 4- or 8-bit microprocessor. Since all the functions such as display RAM, character generator, and liquid crystal driver, required for driving a dot-matrix liquid crystal display are internally provided on one chip, a minimal system can be interfaced with this controller/driver.

A single HD44780U can display up to one 8-character line or two 8-character lines.

The HD44780U has pin function compatibility with the HD44780S which allows the user to easily replace an LCD-II with an HD44780U. The HD44780U character generator ROM is extended to generate 208 5 × 8 dot character fonts and 32 5 × 10 dot character fonts for a total of 240 different character fonts.

The low power supply (2.7 V to 5.5 V) of the HD44780U is suitable for any portable battery-driven product requiring low power dissipation.

Features

- 5 × 8 and 5 × 10 dot matrix possible
- Low power operation support:
 - 2.7 to 5.5 V
- Wide range of liquid crystal display driver power
 - 3.0 to 11 V
- Liquid crystal drive waveform
 - A (One line frequency AC waveform)
- Correspond to high speed MPU bus interface
 - 2 MHz (when $V_{CC} = 5\text{ V}$)
- 4-bit or 8-bit MPU interface enabled

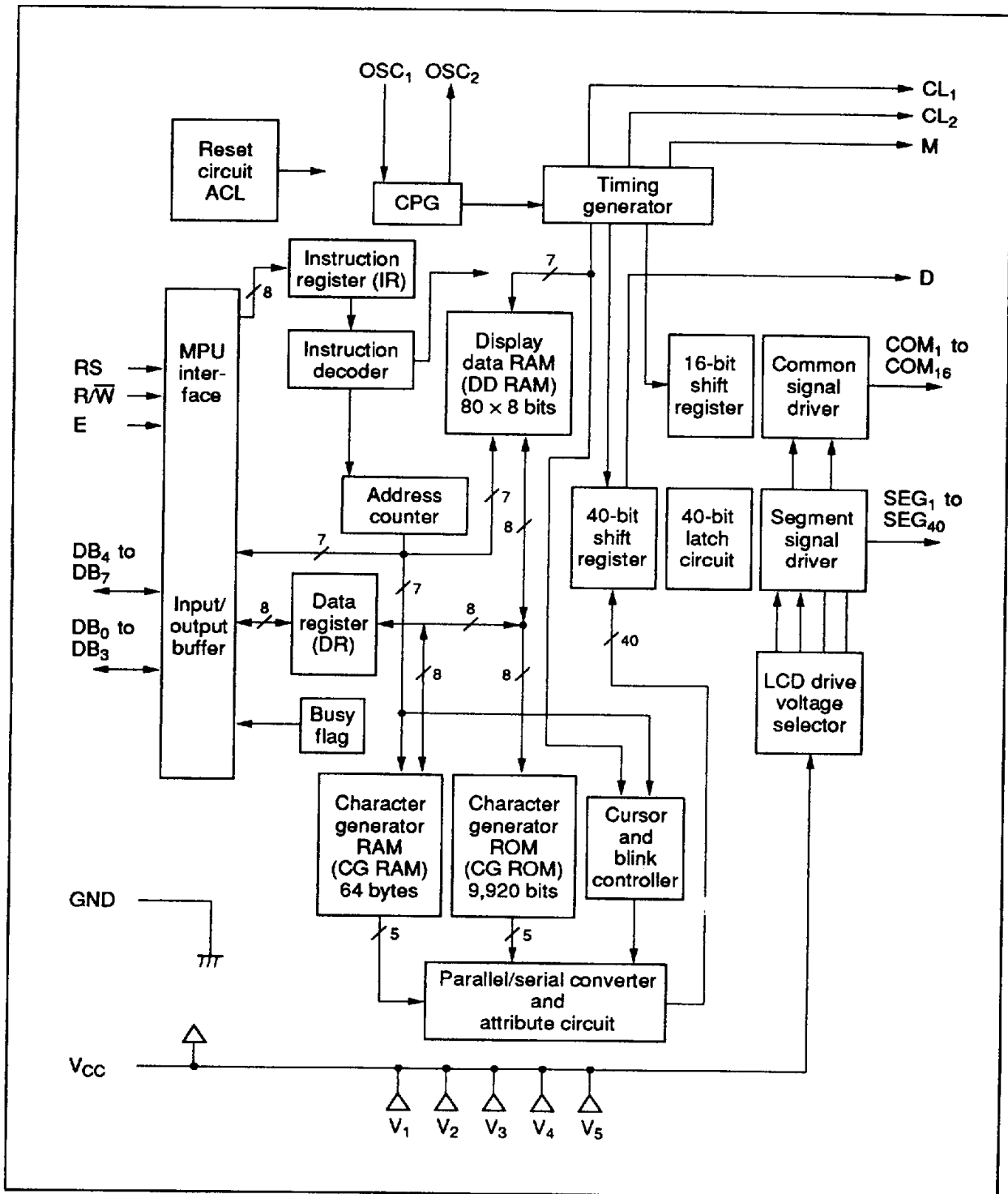
- 80 × 8-bit display RAM (80 characters max.)
- 9,920-bit character generator ROM for a total of 240 character fonts
 - 208 character fonts (5 × 8 dot)
 - 32 character fonts (5 × 10 dot)
- 64 × 8-bit character generator RAM
 - 8 character fonts (5 × 8 dot)
 - 4 character fonts (5 × 10 dot)
- 16-common × 40-segment liquid crystal display driver
- Programmable duty cycles
 - 1/8 for one line of 5 × 8 dots with cursor
 - 1/11 for one line of 5 × 10 dots with cursor
 - 1/16 for two lines of 5 × 8 dots with cursor
- Wide range of instruction functions:
 - Display clear, cursor home, display on/off, cursor on/off, display character blink, cursor shift, display shift
- Pin function compatibility with HD44780S
- Automatic reset circuit that initializes the controller/driver after power on
- Internal oscillator with external resistors
- Low power consumption

Ordering Information

Type No.	Package	CG ROM
HD44780UA00FS	FP-80B	Japanese standard font
HCD44780UA00	Chip	
HD44780UA00TF*	TFP-80	Standard font for communication, European standard font
HD44780UA01FS*	FP-80B	
HD44780UA02FS*	FP-80B	
HD44780UBxxFS	FP-80B	Custom font
HCD44780UBxx	Chip	
HD44780UBxxTF	TFP-80	

Note: * Under development xx: ROM code No.

HD44780U Block Diagram



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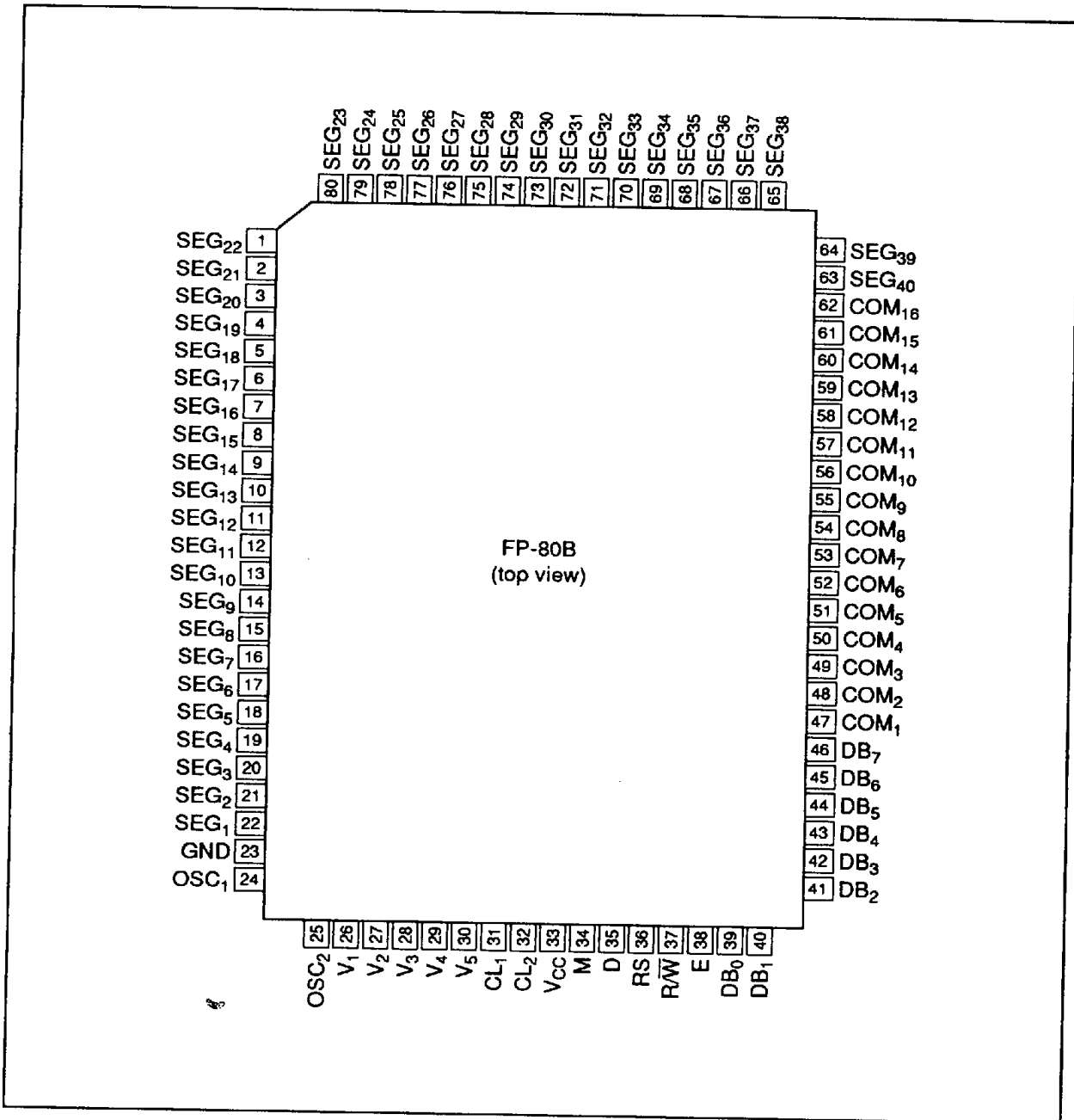
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HD44780U

LCD-II Family Comparison

Item		HD44780S	HD66780 (LCD-II/A)	HD44780U
Power supply voltage		5 V \pm 10%	5 V \pm 10%	2.7 to 5.5 V
Liquid crystal drive voltage V_{LCD}	1/4 bias	3.0 to 11.0 V	3.0 V to V_{CC}	3.0 to 11.0 V
	1/5 bias	4.6 to 11.0 V	3.0 V to V_{CC}	3.0 to 11.0 V
Maximum display digits per chip		16 digits (8 digits \times 2 lines)	16 digits (8 digits \times 2 lines)	16 digits (8 digits \times 2 lines)
Display duty cycle		1/8, 1/11, and 1/16	1/8, 1/11, and 1/16	1/8, 1/11, and 1/16
CGROM		7,200 bits (160 character fonts for 5 \times 7 dot and 32 character fonts for 5 \times 10 dot)	12,000 bits (240 character fonts for 5 \times 10 dot)	9,920 bits (208 character fonts for 5 \times 8 dot and 32 character fonts for 5 \times 10 dot)
CGRAM		64 bytes	64 bytes	64 bytes
DDRAM		80 bytes	80 bytes	80 bytes
Segment signals		40	40	40
Common signals		16	16	16
Liquid crystal drive waveform		A	B	A
Oscillator	Clock source	External resistor, external ceramic filter, or external clock	External resistor, external ceramic filter, or external clock	External resistor or external clock
	R_f oscillation frequency (frame frequency)	270 kHz \pm 30% (59 to 110 Hz for 1/8 and 1/16 duty cycles; 43 to 80 Hz for 1/11 duty cycle)	270 kHz \pm 30% (59 to 110 Hz for 1/8 and 1/16 duty cycles; 43 to 80 Hz for 1/11 duty cycle)	270 kHz \pm 30% (59 to 110 Hz for 1/8 and 1/16 duty cycles; 43 to 80 Hz for 1/11 duty cycle)
	R_f resistance	91 k Ω \pm 2%	82 k Ω \pm 2%	91 k Ω \pm 2% (when $V_{CC} = 5$ V) 75 k Ω \pm 2% (when $V_{CC} = 3$ V)
Instructions		Fully compatible within the HD44780S		
CPU bus timing		1 MHz	2 MHz	1 MHz (when $V_{CC} = 3$ V) 2 MHz (when $V_{CC} = 5$ V)
Package		FP-80	FP-80B	FP-80B

HD44780U Pin Arrangement

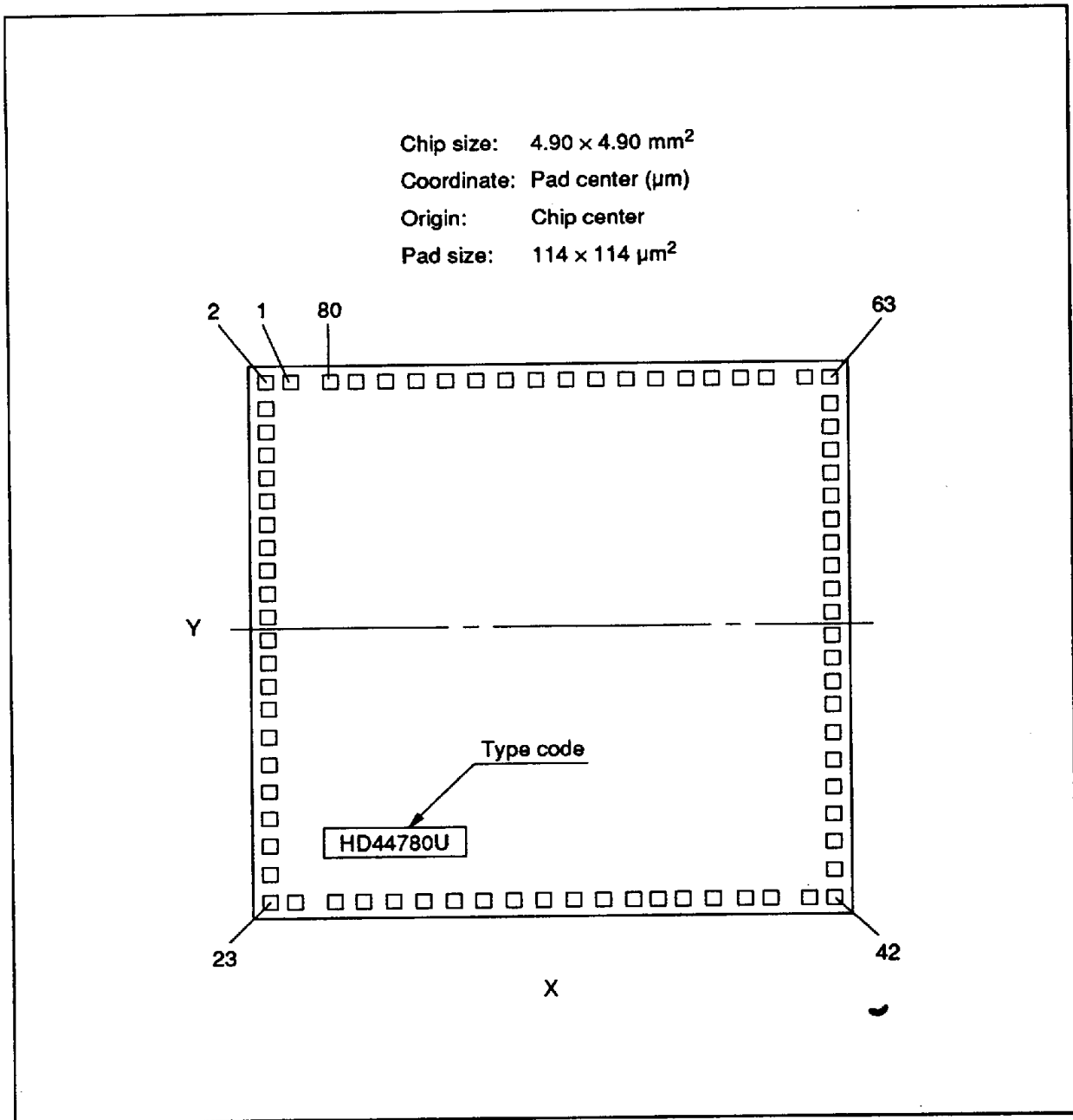


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HD44780U Pad Arrangement



HCD44780U Pad Location Coordinates

Pad No.	Function	Coordinate	
		X (um)	Y (um)
1	SEG ₂₂	-2100	2313
2	SEG ₂₁	-2280	2313
3	SEG ₂₀	-2313	2089
4	SEG ₁₉	-2313	1833
5	SEG ₁₈	-2313	1617
6	SEG ₁₇	-2313	1401
7	SEG ₁₆	-2313	1186
8	SEG ₁₅	-2313	970
9	SEG ₁₄	-2313	755
10	SEG ₁₃	-2313	539
11	SEG ₁₂	-2313	323
12	SEG ₁₁	-2313	108
13	SEG ₁₀	-2313	-108
14	SEG ₉	-2313	-323
15	SEG ₈	-2313	-539
16	SEG ₇	-2313	-755
17	SEG ₆	-2313	-970
18	SEG ₅	-2313	-1186
19	SEG ₄	-2313	-1401
20	SEG ₃	-2313	-1617
21	SEG ₂	-2313	-1833
22	SEG ₁	-2313	-2073
23	GND	-2280	-2290
24	OSC ₁	-2080	-2290
25	OSC ₂	-1749	-2290
26	V ₁	-1550	-2290
27	V ₂	-1268	-2290
28	V ₃	-941	-2290
29	V ₄	-623	-2290
30	V ₅	-304	-2290
31	CL ₁	-48	-2290
32	CL ₂	142	-2290
33	V _{CC}	309	-2290
34	M	475	-2290
35	D	665	-2290
36	RS	832	-2290
37	R/W	1022	-2290
38	E	1204	-2290
39	DB ₀	1454	-2290
40	DB ₁	1684	-2290

Pad No.	Function	Coordinate	
		X (um)	Y (um)
41	DB ₂	2070	-2290
42	DB ₃	2260	-2290
43	DB ₄	2290	-2099
44	DB ₅	2290	-1883
45	DB ₆	2290	-1667
46	DB ₇	2290	-1452
47	COM ₁	2313	-1186
48	COM ₂	2313	-970
49	COM ₃	2313	-755
50	COM ₄	2313	-539
51	COM ₅	2313	-323
52	COM ₆	2313	-108
53	COM ₇	2313	108
54	COM ₈	2313	323
55	COM ₉	2313	539
56	COM ₁₀	2313	755
57	COM ₁₁	2313	970
58	COM ₁₂	2313	1186
59	COM ₁₃	2313	1401
60	COM ₁₄	2313	1617
61	COM ₁₅	2313	1833
62	COM ₁₆	2313	2095
63	SEG ₄₀	2296	2313
64	SEG ₃₉	2100	2313
65	SEG ₃₈	1617	2313
66	SEG ₃₇	1401	2313
67	SEG ₃₆	1186	2313
68	SEG ₃₅	970	2313
69	SEG ₃₄	755	2313
70	SEG ₃₃	539	2313
71	SEG ₃₂	323	2313
72	SEG ₃₁	108	2313
73	SEG ₃₀	-108	2313
74	SEG ₂₉	-323	2313
75	SEG ₂₈	-539	2313
76	SEG ₂₇	-755	2313
77	SEG ₂₆	-970	2313
78	SEG ₂₅	-1186	2313
79	SEG ₂₄	-1401	2313
80	SEG ₂₃	-1617	2313

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Pin Functions

Signal	No. of Lines	I/O	Device Interfaced with	Function
RS	1	I	MPU	Selects registers. 0: Instruction register (for write) Busy flag: address counter (for read) 1: Data register (for write and read)
$\overline{R/W}$	1	I	MPU	Selects read or write. 0: Write 1: Read
E	1	I	MPU	Starts data read/write
DB ₄ to DB ₇	4	I/O	MPU	Four high order bidirectional tristate data bus pins. Used for data transfer and receive between the MPU and the HD44780U. DB ₇ can be used as a busy flag.
DB ₀ to DB ₃	4	I/O	MPU	Four low order bidirectional tristate data bus pins. Used for data transfer and receive between the MPU and the HD44780U. These pins are not used during 4-bit operation.
CL ₁	1	O	HD44100	Clock to latch serial data D sent to the HD44100 driver
CL ₂	1	O	HD44100	Clock to shift serial data D
M	1	O	HD44100	Switch signal for converting the liquid crystal drive waveform to AC
D	1	O	HD44100	Character pattern data corresponding to each segment signal
COM ₁ to COM ₁₆	16	O	LCD	Common signals that are not used are changed to non-selection waveforms. COM ₉ to COM ₁₆ are non-selection waveforms at 1/8 duty factor and COM ₁₂ to COM ₁₆ are non-selection waveforms at 1/11 duty factor.
SEG ₁ to SEG ₄₀	40	O	LCD	Segment signals
V ₁ to V ₅	5	—	Power supply	Power supply for LCD drive V _{CC} - V ₅ = 11 V (max)
V _{CC} , GND	2	—	Power supply	V _{CC} : 2.7 V to 5.5 V, GND: 0 V
OSC ₁ , OSC ₂	2	—	Oscillation resistor clock	When crystal oscillation is performed, a resistor must be connected externally. When the pin input is an external clock, it must be input to OSC ₁ .

Function Description

Registers

The HD44780U has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as display clear and cursor shift, and address information for display data RAM (DD RAM) and character generator RAM (CG RAM). The IR can only be written from the MPU.

The DR temporarily stores data to be written into DD RAM or CG RAM and temporarily stores data to be read from DD RAM or CG RAM. Data written into the DR from the MPU is automatically written into DD RAM or CG RAM by an internal operation. The DR is also used for data storage when reading data from DD RAM or CG RAM. When address information is written into the IR, data is read and then stored into the DR from DD RAM or CG RAM by an internal operation. Data transfer between the MPU is then completed when the MPU reads the DR. After the read, data in DD RAM or CG RAM at the next address is sent to the DR for the next read from the MPU. By the register selector (RS) signal, these two registers can be selected (table 1).

Busy Flag (BF)

When the busy flag is 1, the HD44780U is in the internal operation mode, and the next instruction will not be accepted. When RS = 0 and R/W = 1 (table 1), the busy flag is output to DB₇. The next instruction must be written after ensuring that the busy flag is 0.

Address Counter (AC)

The address counter (AC) assigns addresses to both DD RAM and CG RAM. When an address of an instruction is written into the IR, the address information is sent from the IR to the AC. Selection of either DD RAM or CG RAM is also determined concurrently by the instruction.

After writing into (reading from) DD RAM or CG RAM, the AC is automatically incremented by 1 (decremented by 1). The AC contents are then output to DB₀ to DB₆ when RS = 0 and R/W = 1 (table 1).

Table 1 Register Selection

RS	R/W	Operation
0	0	IR write as an internal operation (display clear, etc.)
0	1	Read busy flag (DB ₇) and address counter (DB ₀ to DB ₆)
1	0	DR write as an internal operation (DR to DD RAM or CG RAM)
1	1	DR read as an internal operation (DD RAM or CG RAM to DR)

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Display Data RAM (DD RAM)

Display data RAM (DD RAM) stores display data represented in 8-bit character codes. Its extended capacity is 80×8 bits, or 80 characters. The area in display data RAM (DD RAM) that is not used for display can be used as general data RAM. See figure 1 for the relationships between DD RAM addresses and positions on the liquid crystal display.

The DD RAM address (A_{DD}) is set in the address counter (AC) as hexadecimal.

- 1-line display ($N = 0$) (figure 2)
 - Case 1: When there are fewer than 80 display characters, the display begins at the head position. For example, if using only the HD44780, 8 characters are displayed. See figure 3.

When the display shift operation is performed, the DD RAM address shifts. See figure 3.

- Case 2: For a 16-character display, the HD44780 can be extended using one HD44100 and displayed. See figure 4.

When the display shift operation is performed, the DD RAM address shifts. See figure 4.

- Case 3: The relationship between the display position and DD RAM address when the number of display digits is increased through the use of two or more HD44100s can be considered as an extension of case #2.

Since the increase can be eight digits per additional HD44100, up to 80 digits can be displayed by externally connecting nine HD44100s. See figure 5.

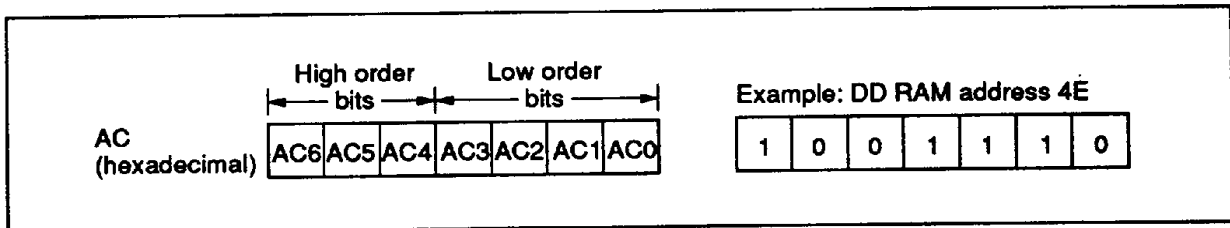


Figure 1 DD RAM Address

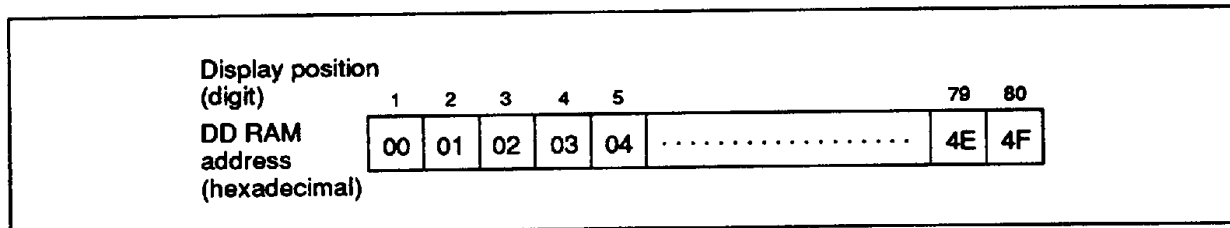


Figure 2 1-Line Display

Timing Generation Circuit

The timing generation circuit generates timing signals for the operation of internal circuits such as DD RAM, CG ROM and CG RAM. RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interfering with each other. Therefore, when writing data to DD RAM, for example, there will be no undesirable interferences, such as flickering, in areas other than the display area. This circuit also generates timing signals for the operation of the externally connected HD44100 driver.

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 16 common signal drivers and 40 segment signal drivers. When the character font and number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, while the other common signal drivers continue to output non-selection waveforms.

The segment signal driver has essentially the same configuration as the HD44100 driver. Character pattern data is sent serially through a 40-bit shift register and latched when all needed data has

arrived. The latched data then enables the driver to generate drive waveform outputs. The serial data can be sent to externally cascaded HD44100s used for displaying extended digit numbers.

Sending serial data always starts at the display data character pattern corresponding to the last address of the display data RAM (DD RAM).

Since serial data is latched when the display data character pattern corresponding to the starting address enters the internal shift register, the HD44780U drives from the head display. The rest of the display, corresponding to latter addresses, are added with each additional HD44100.

Cursor/Blink Control Circuit

The cursor/blink control circuit generates the cursor or character blinking. The cursor or the blinking will appear with the digit located at the display data RAM (DD RAM) address set in the address counter (AC).

For example (figure 11), when the address counter is 08H, the cursor position is displayed at DD RAM address 08H.

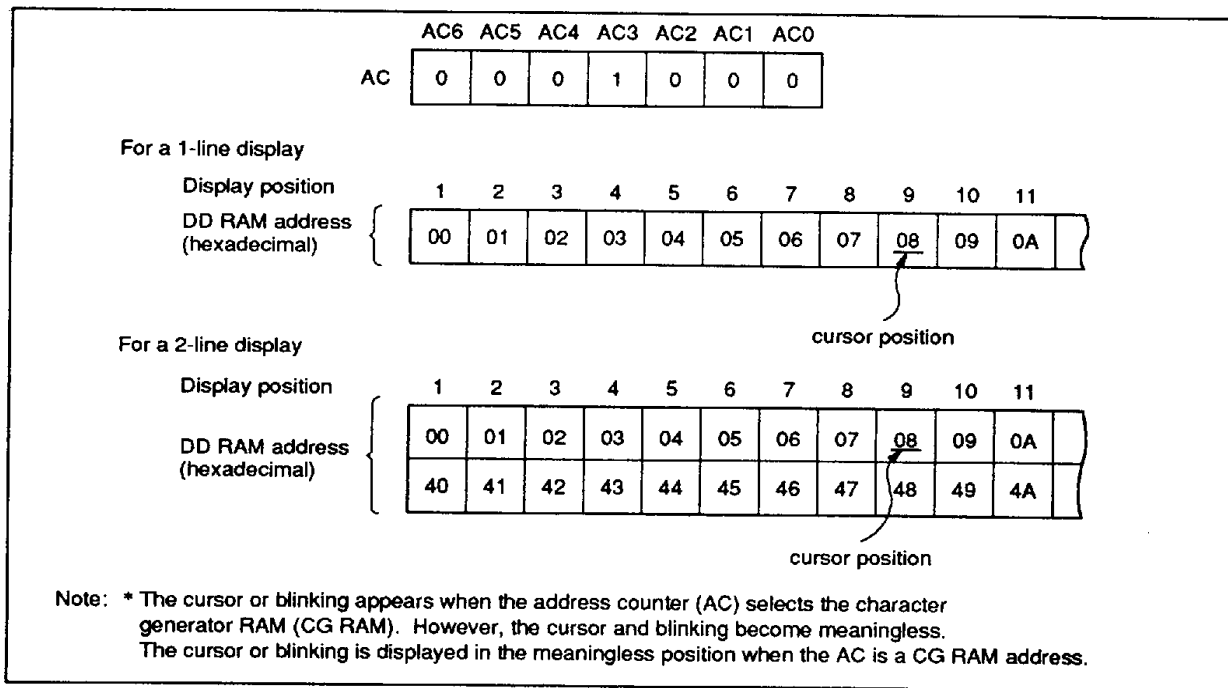


Figure 11 Cursor/Blink Display Example

Interfacing to the MPU

The HD44780U can send data in either two 4-bit operations or one 8-bit operation, thus allowing interfacing with 4- or 8-bit MPUs.

- For 4-bit interface data, only four bus lines (DB₄ to DB₇) are used for transfer. Bus lines DB₀ to DB₃ are disabled. The data transfer between the HD44780U and the MPU is completed after the 4-bit data has been transferred twice. As for the order of data transfer, the four high order bits (for 8-bit operation, DB₄ to DB₇) are transferred before the four low order bits (for 8-bit operation, DB₀ to DB₃).

The busy flag must be checked (one instruction) after the 4-bit data has been transferred twice. Two more 4-bit operations then transfer the busy flag and address counter data.

- For 8-bit interface data, all eight bus lines (DB₀ to DB₇) are used.

Reset Function

Initializing by Internal Reset Circuit

An internal reset circuit automatically initializes the HD44780U when the power is turned on. The following instructions are executed during the initialization. The busy flag (BF) is kept in the busy state until the initialization ends (BF = 1). The busy state lasts for 10 ms after V_{CC} rises to 4.5 V.

- Display clear
- Function set:
DL = 1; 8-bit interface data
N = 0; 1-line display
F = 0; 5 × 8 dot character font
- Display on/off control:
D = 0; Display off
C = 0; Cursor off
B = 0; Blinking off
- Entry mode set:
I/D = 1; Increment by 1
S = 0; No shift

Note: If the electrical characteristics conditions listed under the table Power Supply Conditions Using Internal Reset Circuit are not met, the internal reset circuit will not operate normally and will fail to initialize the HD44780U. For such a case, initialization must be performed by the MPU as explained in the section, Initializing by Instruction.

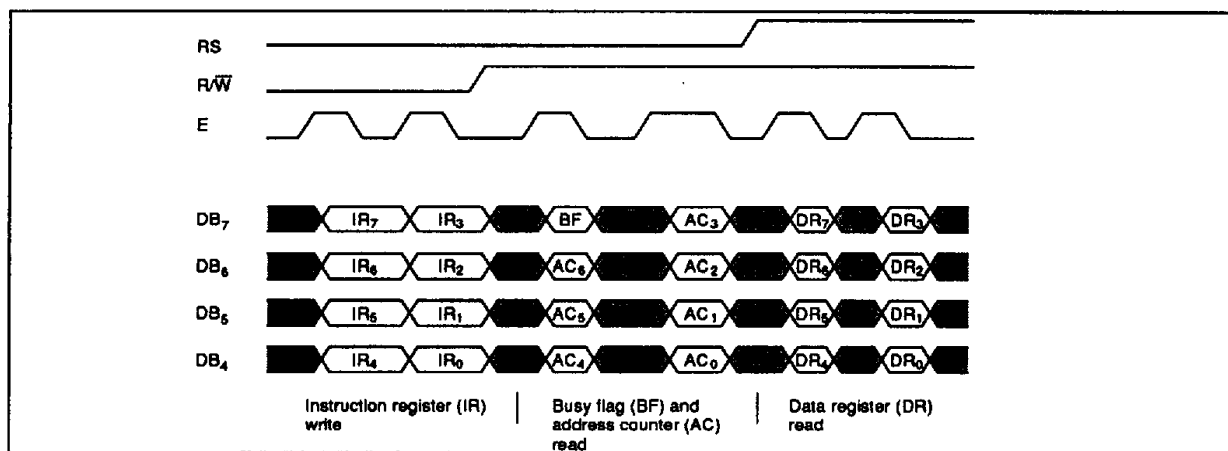


Figure 12 4-Bit Transfer Example

Timing Characteristics

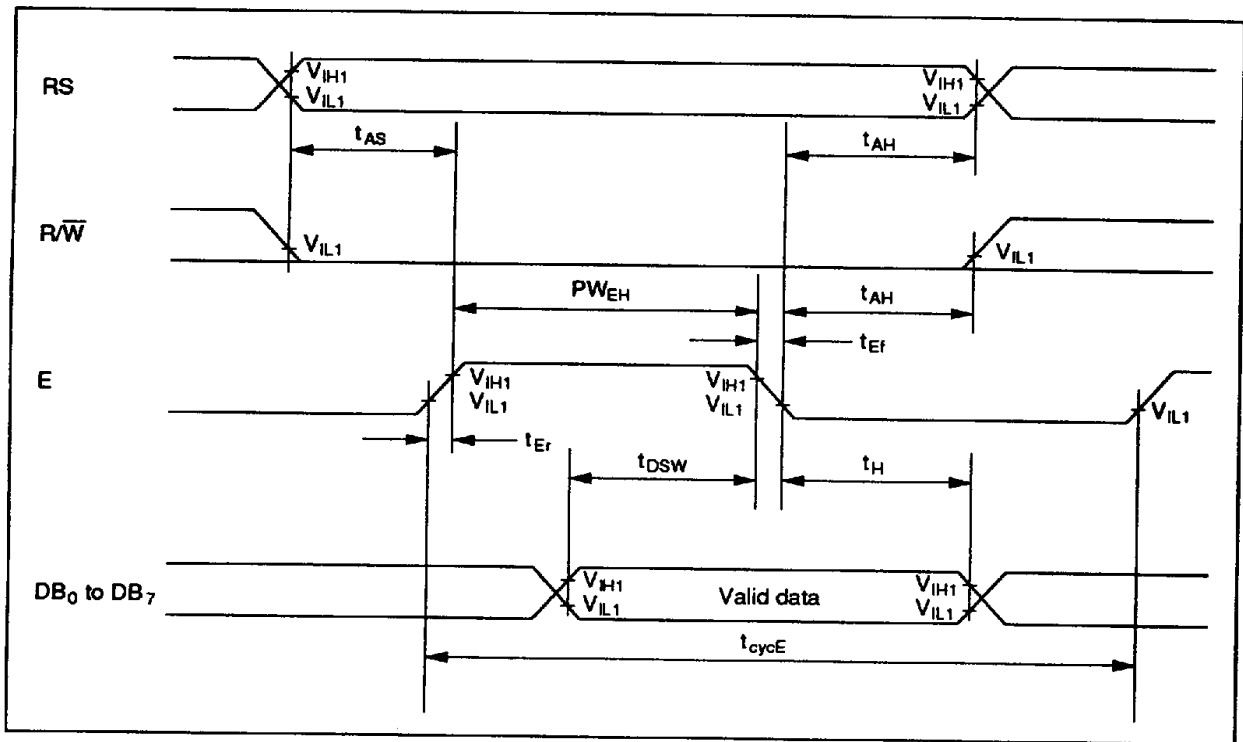
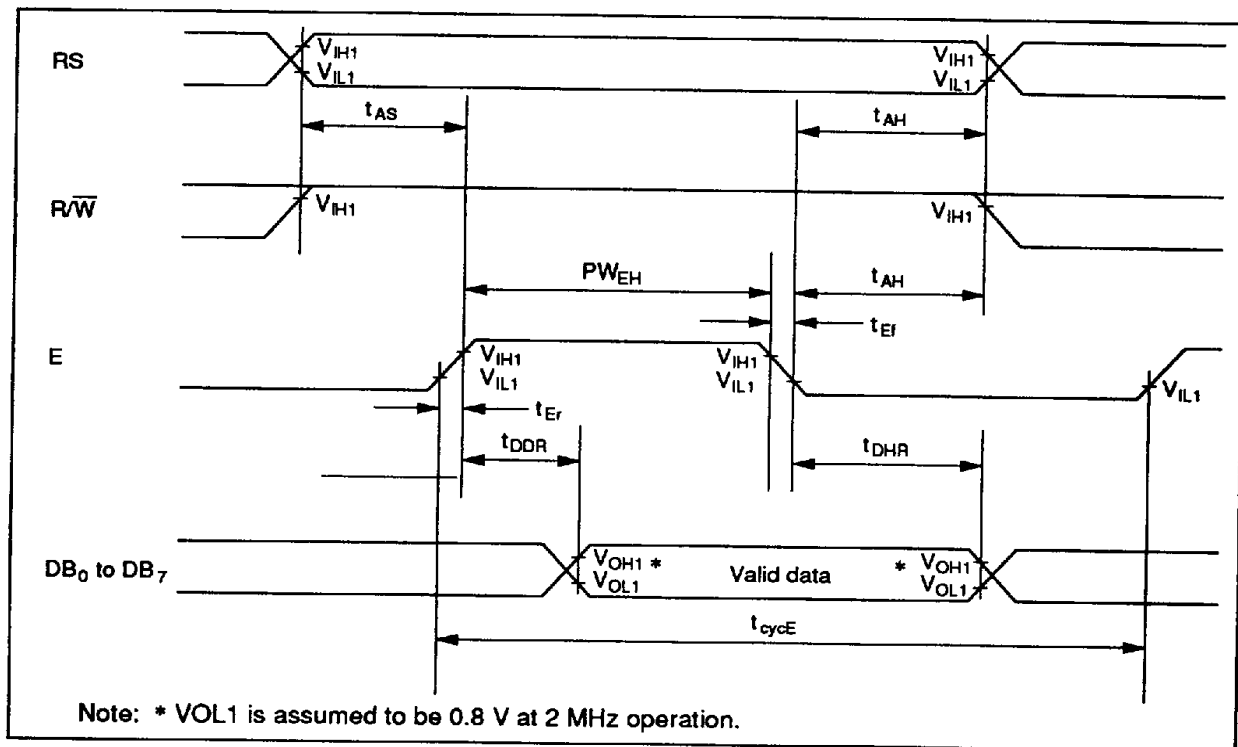


Figure 34 Write Operation



Note: * VOL1 is assumed to be 0.8 V at 2 MHz operation.

Figure 35 Read Operation

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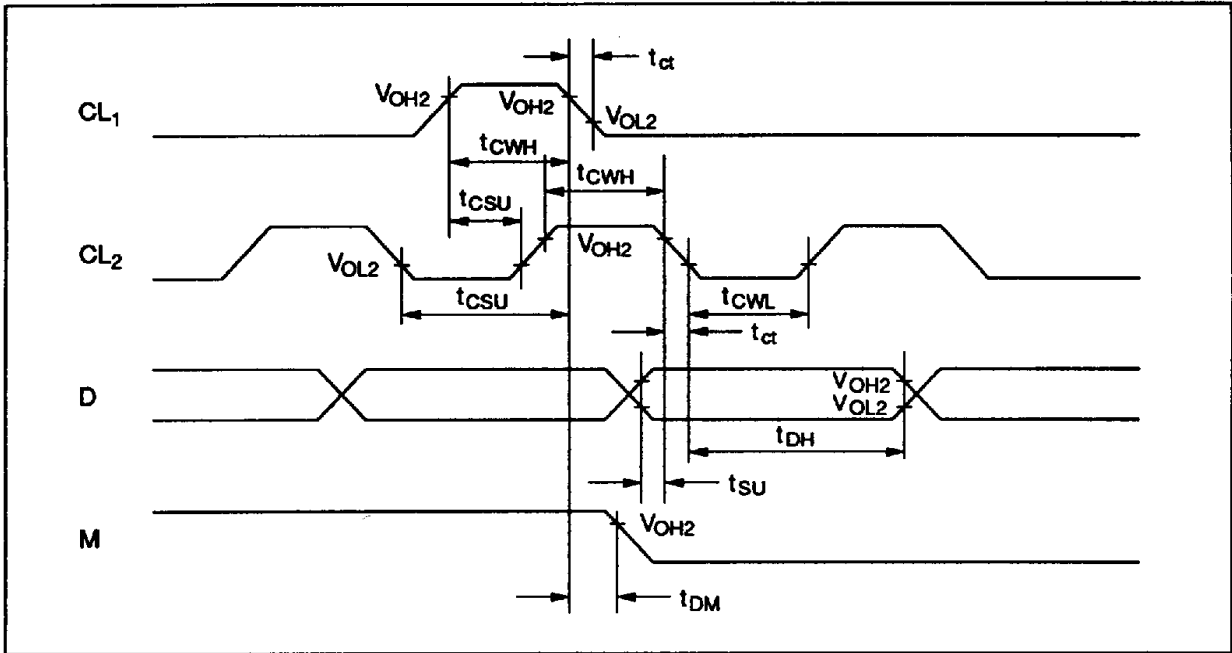


Figure 36 Interface Timing with External Driver

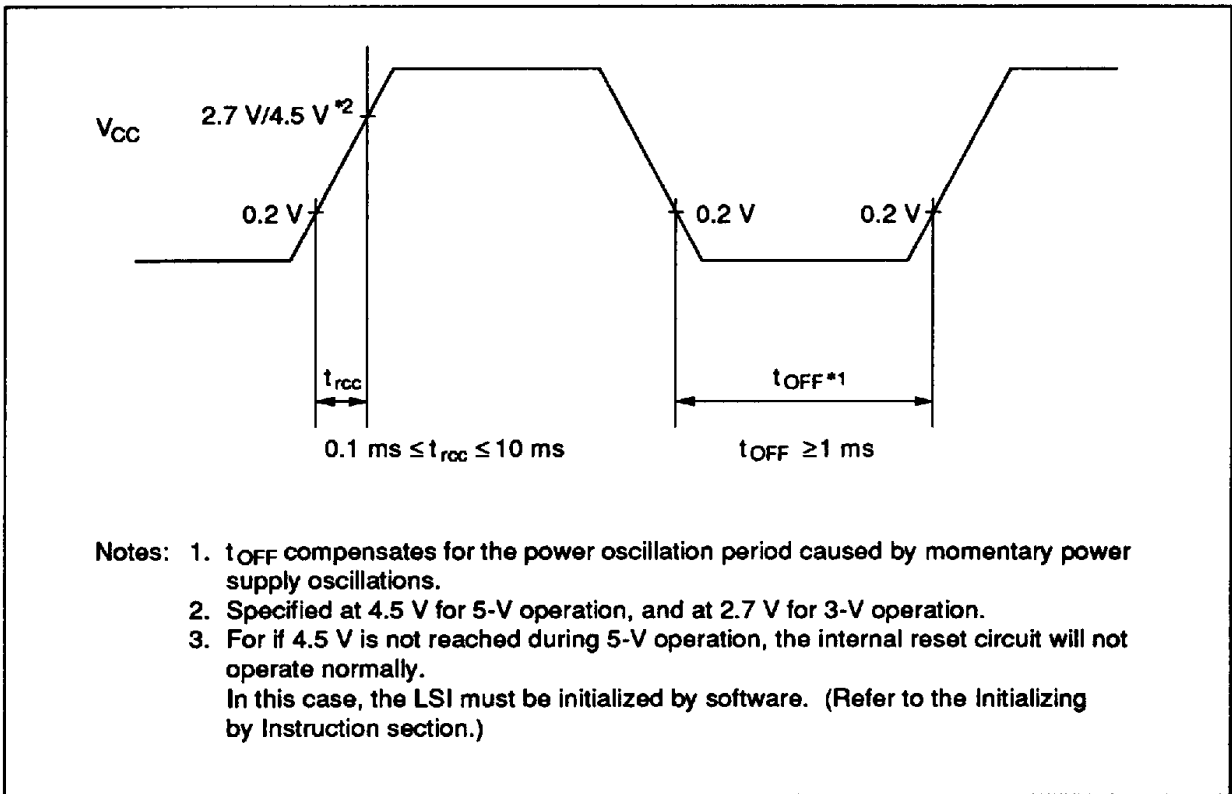


Figure 37 Internal Power Supply Reset